TLV902x-Q1 and TLV903x-Q1 High-Precision Dual and Quad Automotive Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- 1.65 V to 5.5 V supply range
- Power-On Reset (POR) for known start-up
- Precision input offset voltage 300 µV
- 100ns Typ propagation delay
- Low quiescent current 16 µA per channel
- Rail-to-Rail input voltage range exceeds the rails
- Open-drain output option (TLV902x-Q1)
- Push-pull output option (TLV903x-Q1)
- 2 kV ESD Protection

2 Applications

- Automotive
  - HEV/EV and power train
  - Infotainment and cluster
  - Body control module
- Industrial

3 Description

The TLV902x-Q1 and TLV903x-Q1 are a family of Automotive grade dual and quad channel comparators. The family offers low input offset voltage, integrated Power-On Reset (POR) circuitry, and fault-tolerant inputs with an excellent speed-to-power combination with a propagation delay of 100 ns. Operating voltage range of 1.65 V to 5.5 V with a quiescent supply current of 18 µA per channel.

This device family also includes a Power-on Reset (POR) feature that ensures the output is in a known state until the minimum supply voltage has been reached and a small time period passed before the output starts responding to the inputs. This prevents output transients during system power-up and power-down.

These comparators also feature no output phase inversion with fault-tolerant inputs that can go up to 6-V without damage. This makes this family of comparators well suited for precision voltage monitoring in harsh, noisy environments.

The TLV902x-Q1 comparators have an open-drain output stage that can be pulled below or beyond the supply voltage, making it appropriate for low voltage logic and level translators.

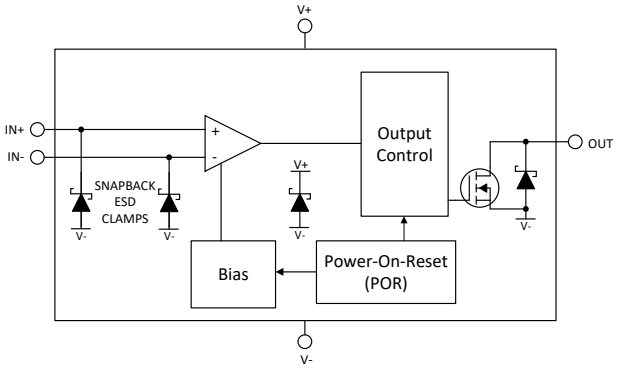
The TLV903x-Q1 comparators have a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate.

The TLV902x-Q1 and TLV903x-Q1 are specified for the Automotive temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

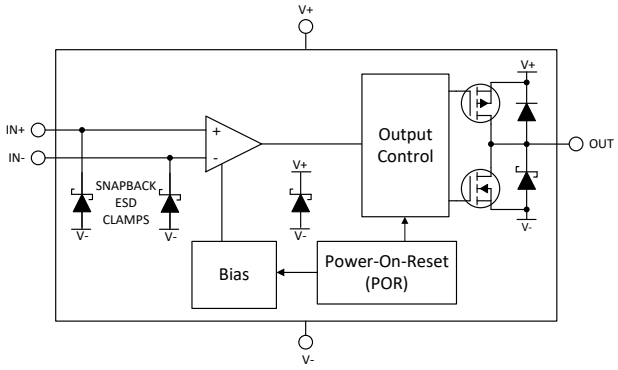
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV9022-Q1, TLV9032-Q1 (Dual)	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	2.00 mm × 2.00 mm
	SOT-23-THN (8)	1.60 mm × 2.90 mm
TLV9024-Q1, TLV9034-Q1 (Quad)	SOIC (14) (Preview)	3.91 mm × 8.65 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	SOT-23 (14) (Preview)	4.20 mm x 2.00 mm
	WQFN (16) (Preview)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TLV9022-Q1 and TLV9024-Q1 Block Diagram



TLV9032-Q1 and TLV9034-Q1 Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2021) to Revision C (January 2022)	Page
• Updated VSSOP status in Device Info table	1

Changes from Revision A (December 2020) to Revision B (August 2021)	Page
• Added status to Device Info table	1

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added tables for Quad	5
• Added Typical Graphs	11

5 Pin Configuration and Functions

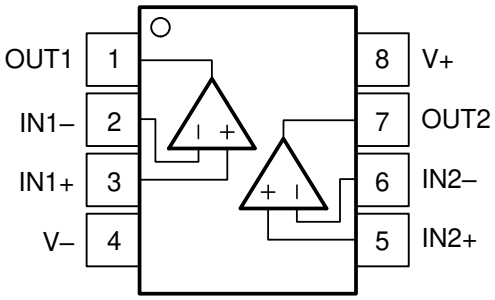
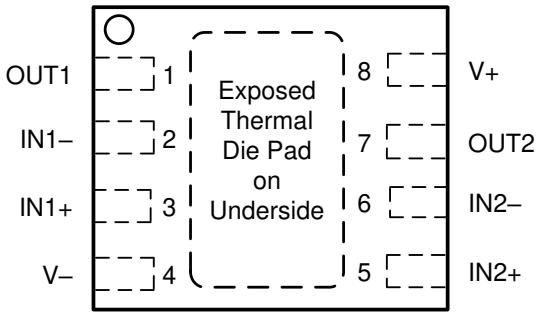


Figure 5-1. D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23-8 Top View



NOTE: Connect exposed thermal pad directly to V- pin.

Figure 5-2. DSG Package, 8-Pad WSON With Exposed Thermal Pad, Top View

Pin Functions: TLV90x2-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V–	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to V- pin

Pin Functions: TLV90x4-Q1

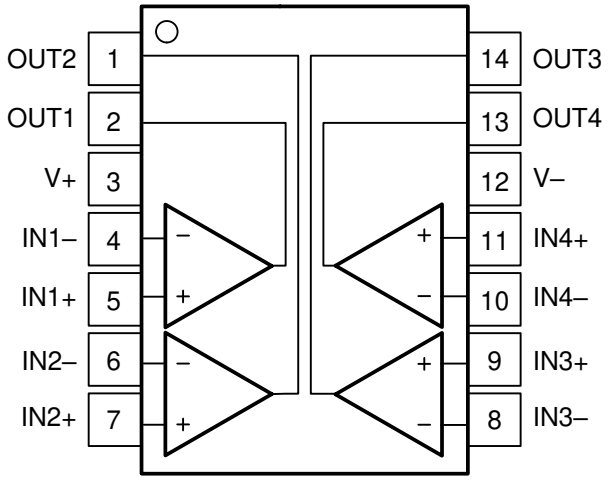
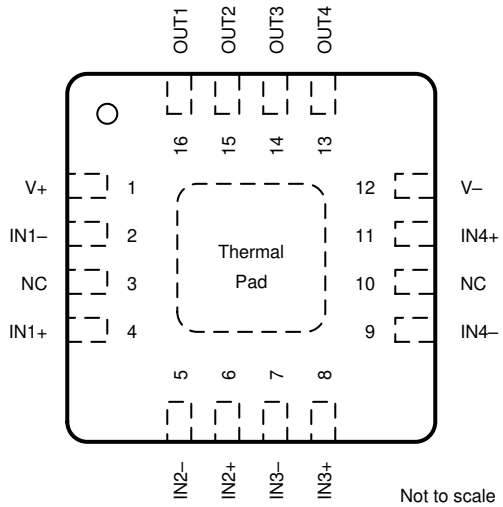


Figure 5-3. D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23, Top View



NOTE: Connect exposed thermal pad directly to V- pin.

Figure 5-4. RTE Package, 16-Pad WQFN With Exposed Thermal Pad, Top View

Table 5-1. Pin Functions: TLV90x4-Q1

PIN			I/O	DESCRIPTION
NAME[1]	SOIC	WQFN		
OUT2	1	15	Output	Output pin of the comparator 2
OUT1	2	16	Output	Output pin of the comparator1
V+	3	1	—	Positive supply
IN1–	4	2	Input	Negative input pin of the comparator 1
IN1+	5	4	Input	Positive input pin of the comparator 1
IN2–	6	5	Input	Negative input pin of the comparator 2
IN2+	7	6	Input	Positive input pin of the comparator 2
IN3–	8	7	Input	Negative input pin of the comparator 3
IN3+	9	8	Input	Positive input pin of the comparator 3
IN4–	10	9	Input	Negative input pin of the comparator 4
IN4+	11	11	Input	Positive input pin of the comparator 4
V–	12	12	—	Negative supply
OUT4	13	13	Output	Output pin of the comparator 4
OUT3	14	14	Output	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to V- pin.

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in channel naming convention.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	6	V
Input pins (IN+, IN–) from V–(2)	–0.3	6	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) from V–, open drain only(3)	–0.3	6	V
Output (OUT) from V–, push-pull only	–0.3	(V+) + 0.3	V
Output short circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, Tstg	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less. Additionally, Inputs (IN+, IN–) can be greater than V+ and OUT as long as it is within the –0.3 V to 6 V range
(3) Output (OUT) for open drain can be greater than V+ and inputs (IN+, IN–) as long as it is within the –0.3 V to 6 V range
(4) Short-circuit to V– or V+. Short circuits from outputs can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.65	5.5	V
Input voltage range (IN+, IN–) from (V–)	–0.2	5.7	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information, TLV90x2-Q1

THERMAL METRIC (1)		TLV90x2-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	167.7	221.7	215.8	175.2	240.0	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	107.0	109.1	105.2	178.1	151.0	°C/W
R_{qJB}	Junction-to-board thermal resistance	111.2	152.5	137.5	139.5	157.0	°C/W
y_{JT}	Junction-to-top characterization parameter	53.1	36.4	39.6	47.2	32.8	°C/W
y_{JB}	Junction-to-board characterization parameter	110.4	150.7	135.9	138.9	155.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	127.3	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information, TLV90x4-Q1

THERMAL METRIC(1)		TLV90x4-Q1				UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)	DYY (SOT-23)	
		14 PINS	14 PINS	16 PINS	14 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	136.0	155.0	134.1	–	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	91.2	82.0	122.6	–	°C/W
R_{qJB}	Junction-to-board thermal resistance	92.0	98.5	109.3	–	°C/W
y_{JT}	Junction-to-top characterization parameter	46.9	25.7	30.9	–	°C/W
y_{JB}	Junction-to-board characterization parameter	91.6	97.6	108.3	–	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	98.7	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = (V–) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 Vx	–1.5	±0.3	1.5	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–2		2	
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		16	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			35	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull verison)	75	95		dB
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C (open drain version)	80	95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	60	70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal differential voltage amplification	For open drain version only	50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = 25°C (push-pull only)		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = –40°C to +125°C (push-pull only)			175	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C (open drain only)		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	90	100		mA
I_{SC}	Short-circuit current	V_S = 5 V, Sourcing (push-pull only)	90	100		mA

6.7 Switching Characteristics,

For V_S (Total Supply Voltage) = (V+) – () = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		100		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (for push-pull only)		115		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		150		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		3		ns
T_{RISE}	5V Output Rise Time, 20% to 80%	V_{ID} = 100 mV (for push-pull only)		3		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ for open drain only)		3		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (V–), V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ for open drain only)		20		µs

6.8 Electrical Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = (V–) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 Vx	–1.5	±0.3	1.5	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–2		2	
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		16	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			35	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull version)			177.8	µV/V
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull version)	75	95		dB
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (open drain version)			100	µV/V
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (open drain version)	80	95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	60	70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal differential voltage amplification	For open-drain version only	50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = 25°C (push-pull only)		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = –40°C to +125°C (push-pull only)			175	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C (open drain only)		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	90	100		mA
I_{SC}	Short-circuit current	V_S = 5 V, Sourcing (push-pull only)	90	100		mA

6.9 Switching Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		100		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (for push-pull only)		115		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		150		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		3		ns
T_{RISE}	5V Output Rise Time, 20% to 80%	V_{ID} = 100 mV, for push-pull only		3		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ for open drain only)		3		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (V–), V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ for open drain only)		30		µs

6.10 Typical Characteristics

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

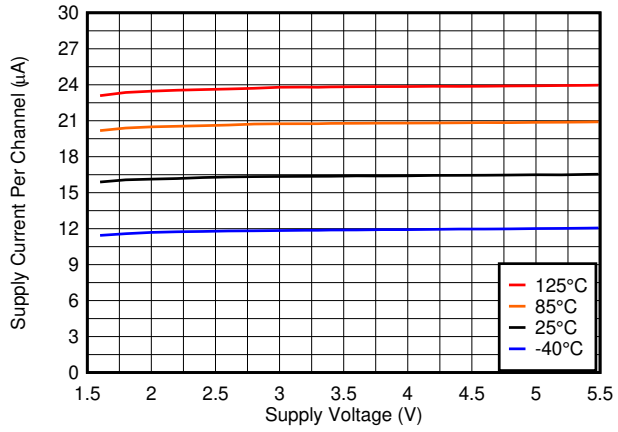


Figure 6-1. Supply Current vs. Supply Voltage

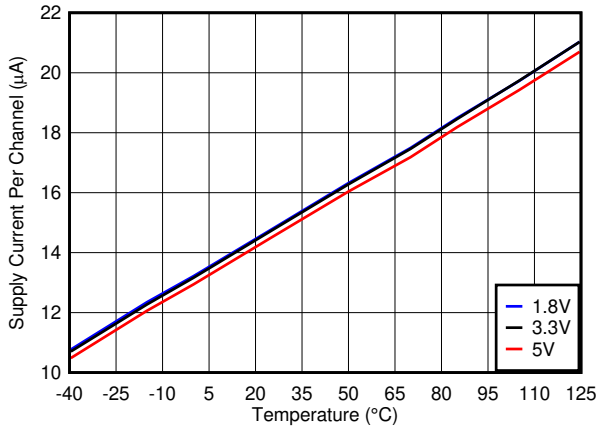


Figure 6-2. Supply Current vs. Temperature

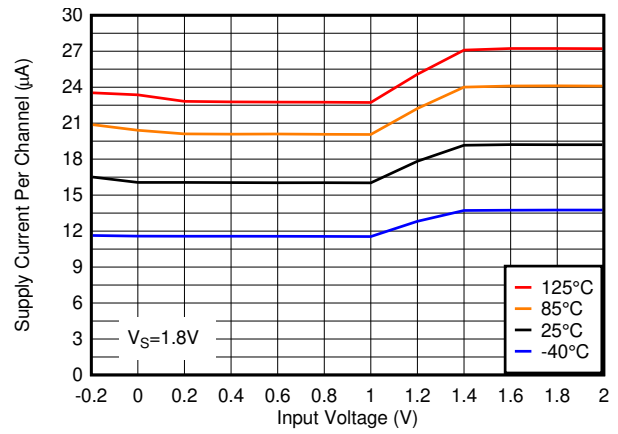


Figure 6-3. Supply Current vs. Input Voltage, 1.8V

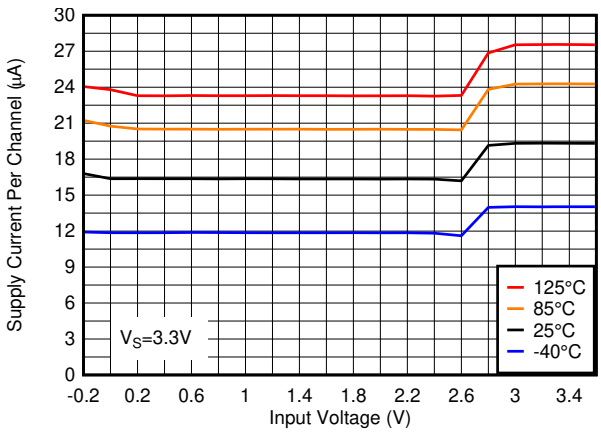


Figure 6-4. Supply Current vs. Input Voltage, 3.3V

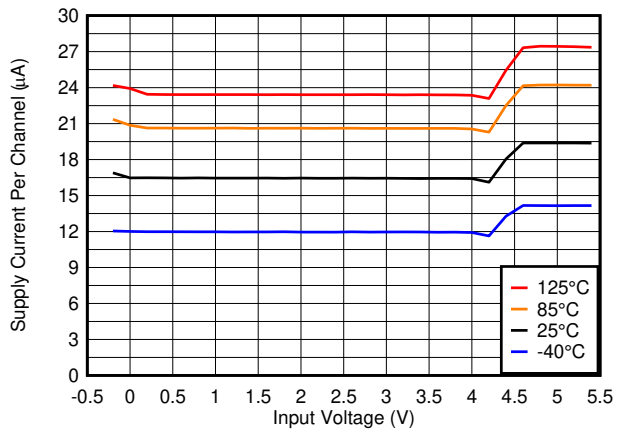


Figure 6-5. Supply Current vs. Input Voltage, 5V

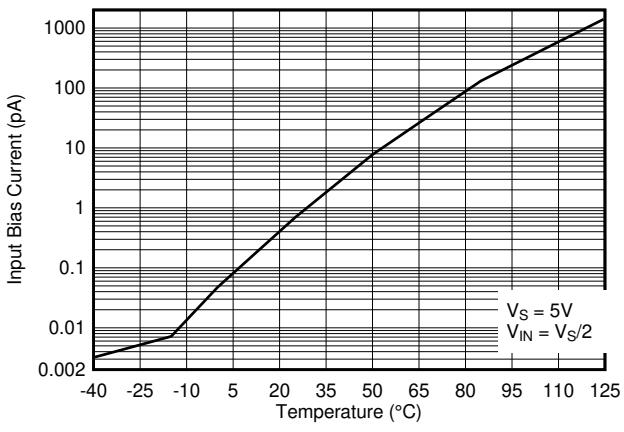


Figure 6-6. Input Bias Current vs. Temperature

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

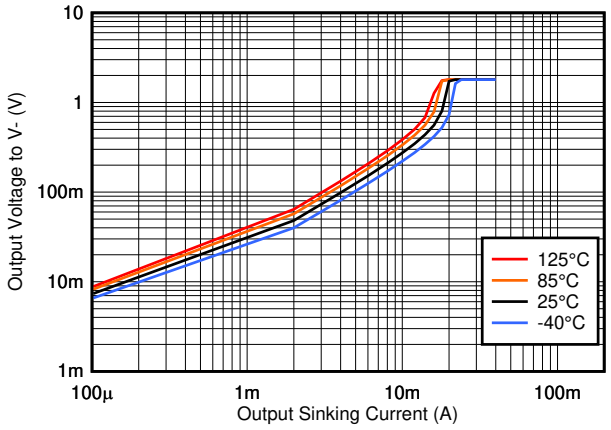


Figure 6-7. Output Sinking Current vs. Output Voltage, 1.8V

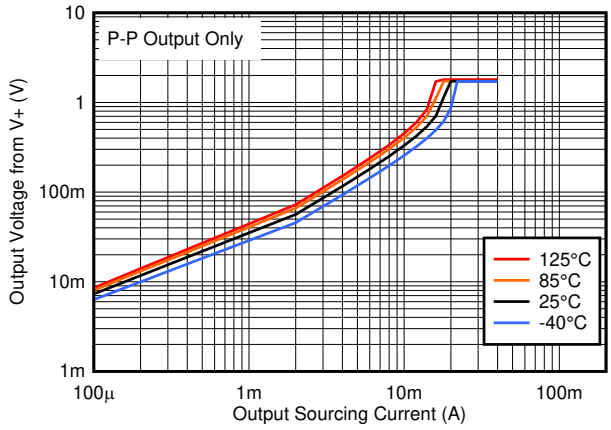


Figure 6-8. Output Sourcing Current vs. Output Voltage, 1.8V

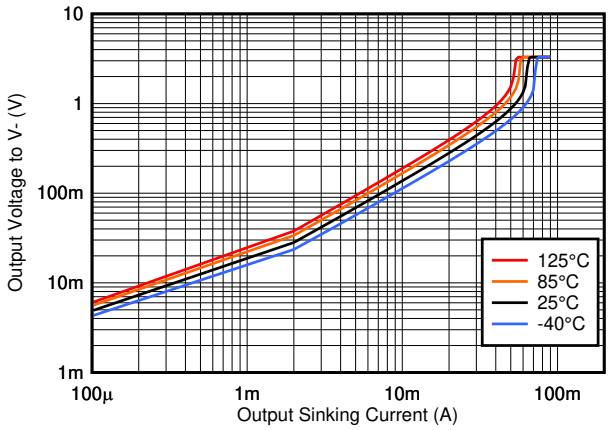


Figure 6-9. Output Sinking Current vs. Output Voltage, 3.3V

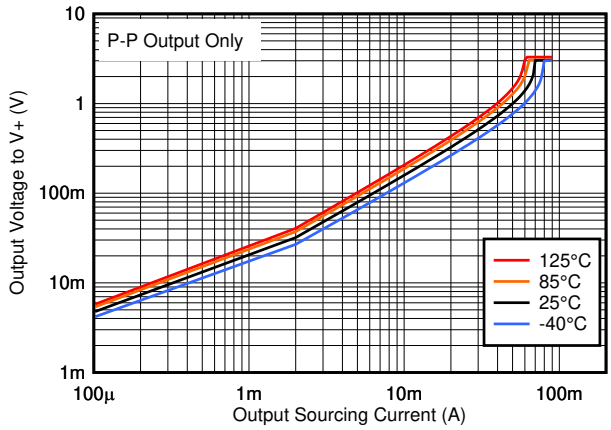


Figure 6-10. Output Sourcing Current vs. Output Voltage, 3.3V

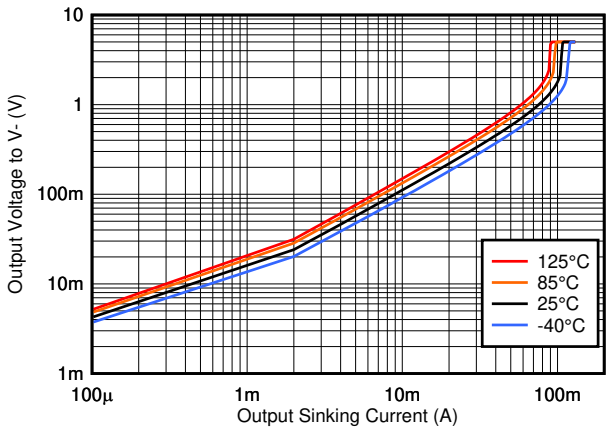


Figure 6-11. Output Sinking Current vs. Output Voltage, 5V

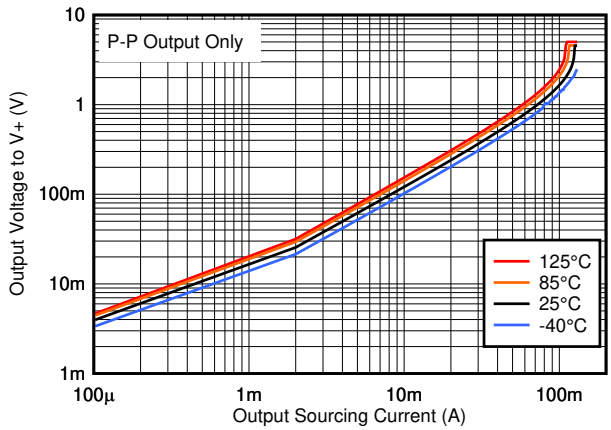


Figure 6-12. Output Sourcing Current vs. Output Voltage, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

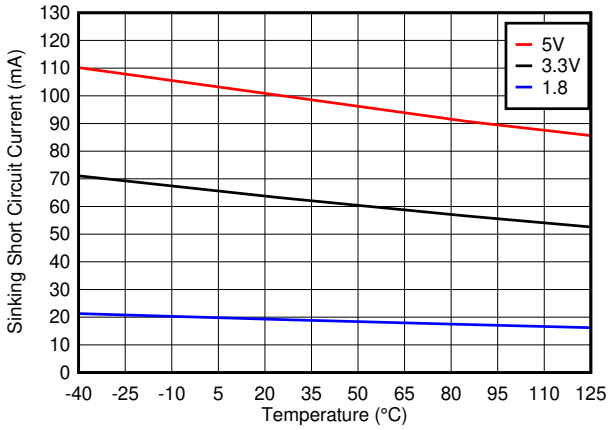


Figure 6-13. Sinking Short Circuit Current vs. Temperature

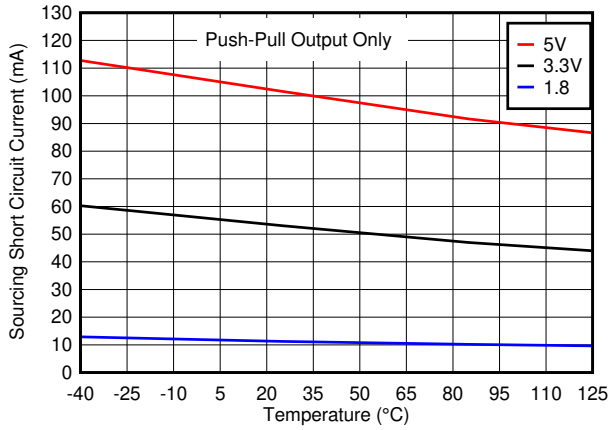


Figure 6-14. Sourcing Short Circuit Current vs. Temperature

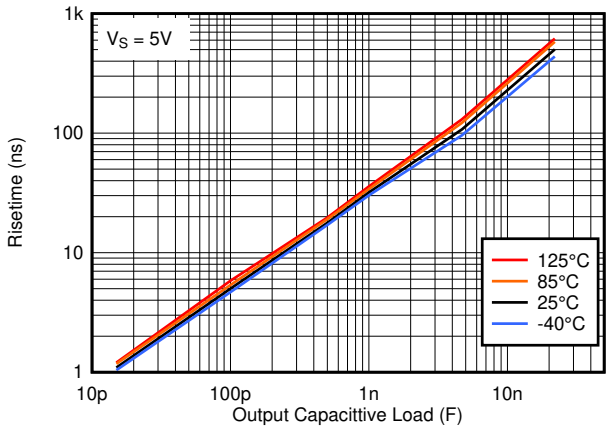


Figure 6-15. Risetime vs. Capacitive Load

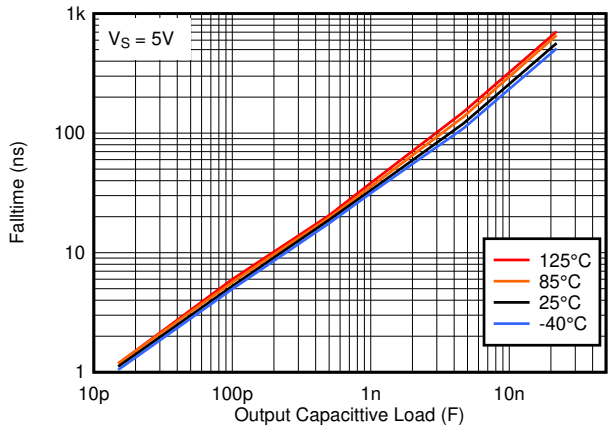


Figure 6-16. Falltime vs. Capacitive Load

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

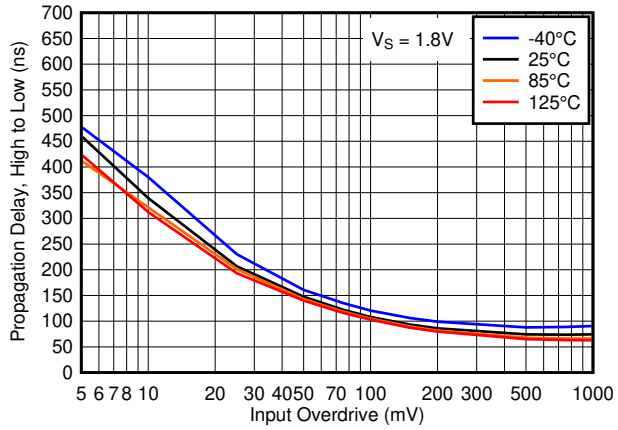


Figure 6-17. Propagation Delay, High to Low, 1.8V

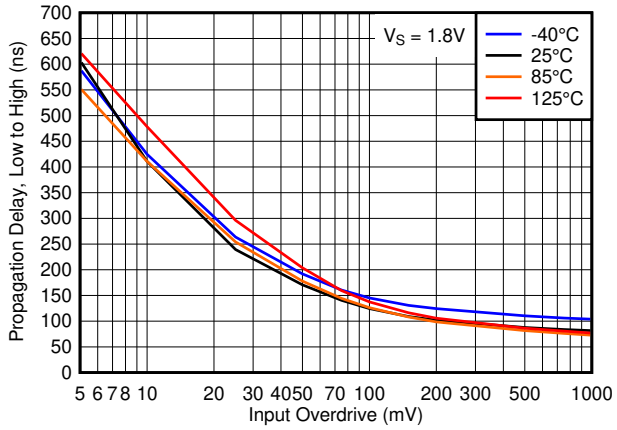


Figure 6-18. Propagation Delay, Low to High, 1.8V

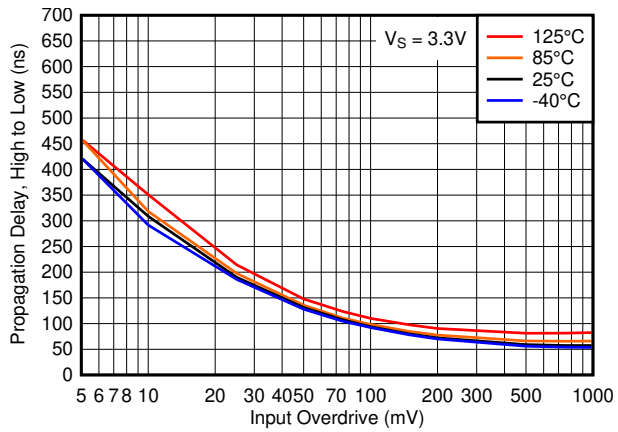


Figure 6-19. Propagation Delay, High to Low, 3.3V

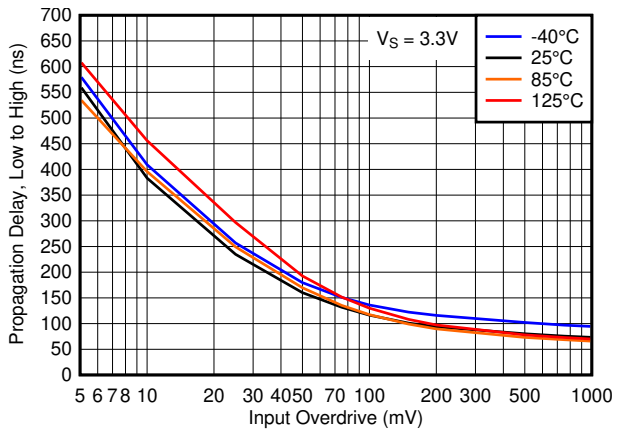


Figure 6-20. Propagation Delay, Low to High, 3.3V

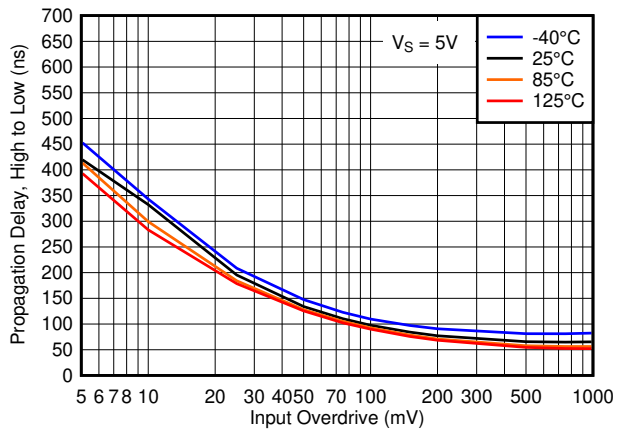


Figure 6-21. Propagation Delay, High to Low, 5V

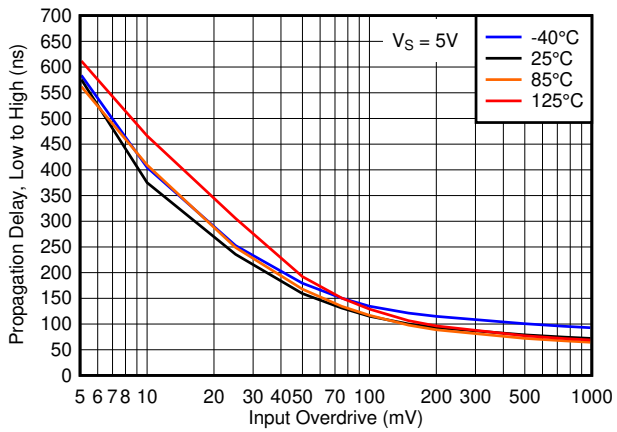


Figure 6-22. Propagation Delay, Low to High, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

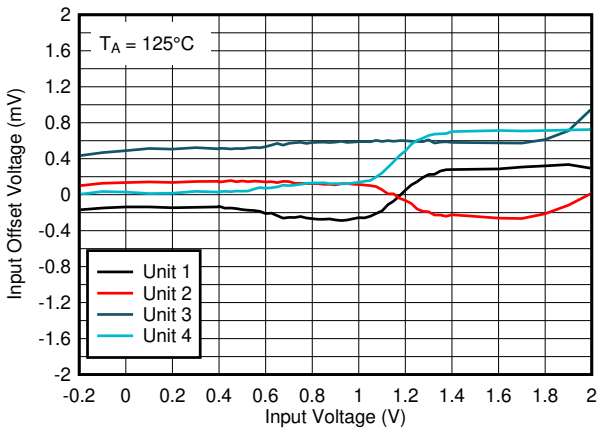


Figure 6-23. Offset Voltage vs. Input Votlage at 125°C, 1.8V

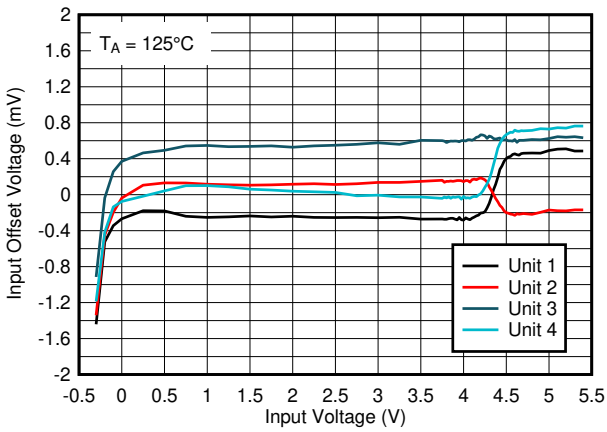


Figure 6-24. Offset Voltage vs. Input Votlage at 125°C, 5V

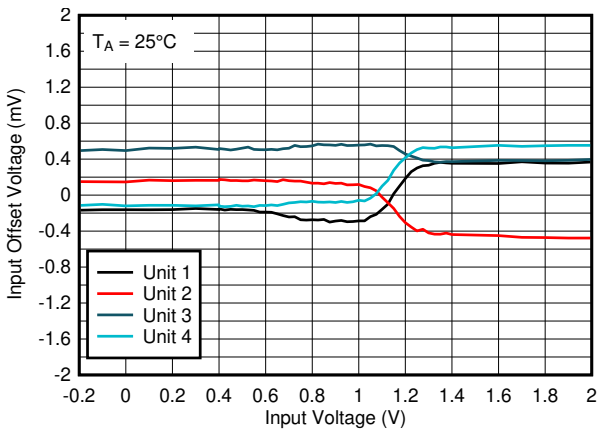


Figure 6-25. Offset Voltage vs. Input Votlage at 25°C, 1.8V

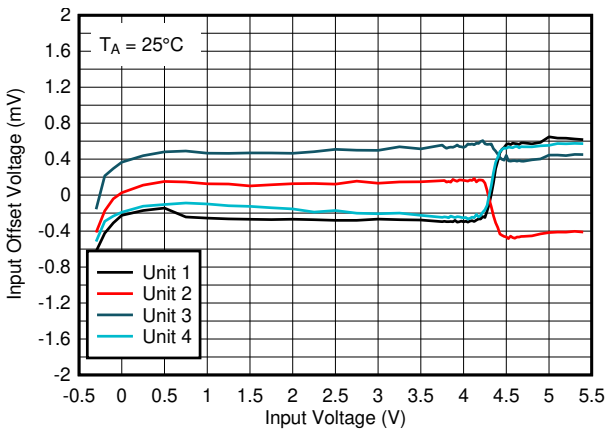


Figure 6-26. Offset Voltage vs. Input Votlage at 25°C, 5V

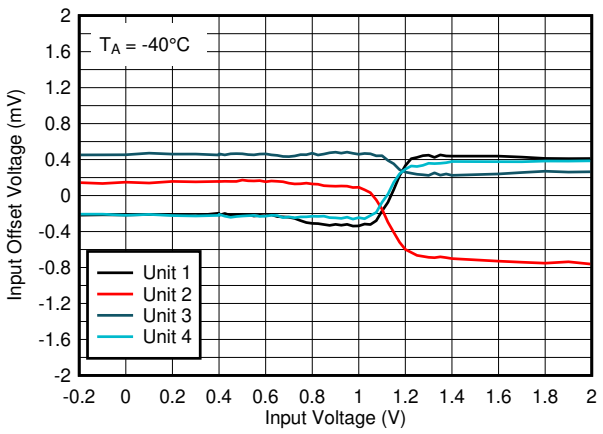


Figure 6-27. Offset Voltage vs. Input Votlage at -40°C, 1.8V

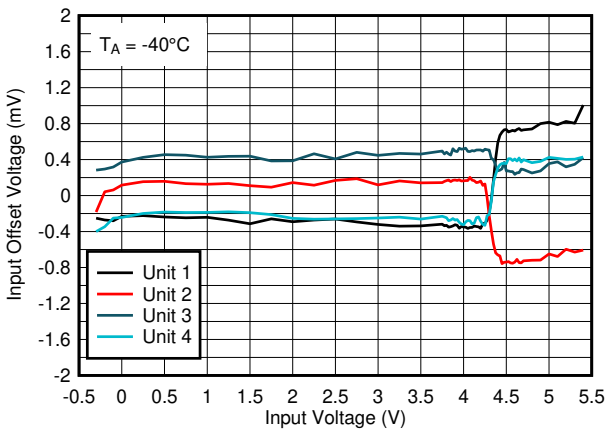


Figure 6-28. Offset Voltage vs. Input Votlage at -40°C, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

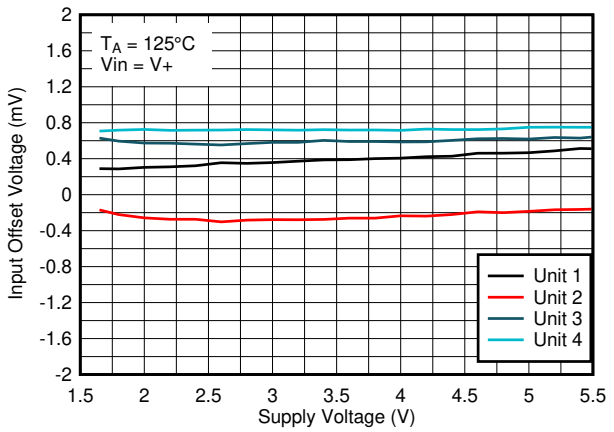


Figure 6-29. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V+

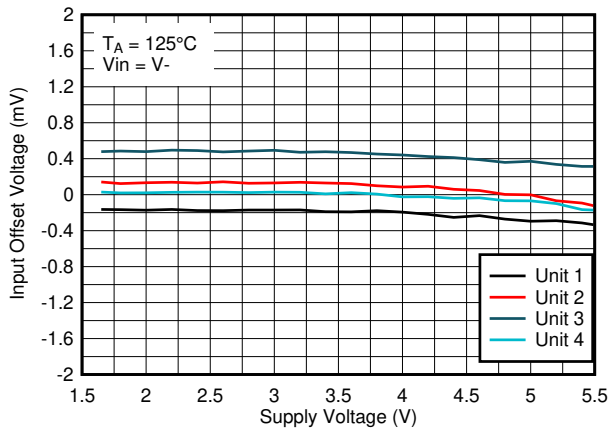


Figure 6-30. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V-

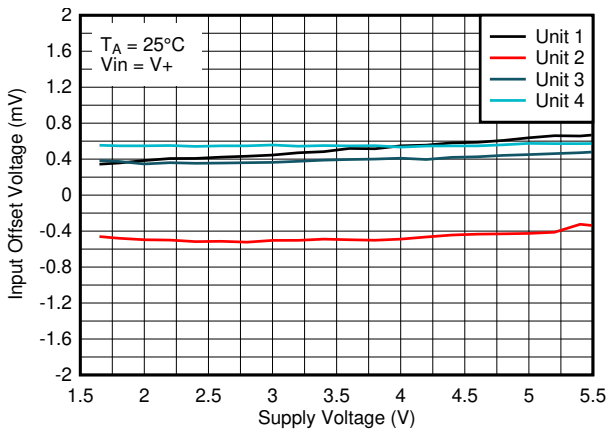


Figure 6-31. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V+

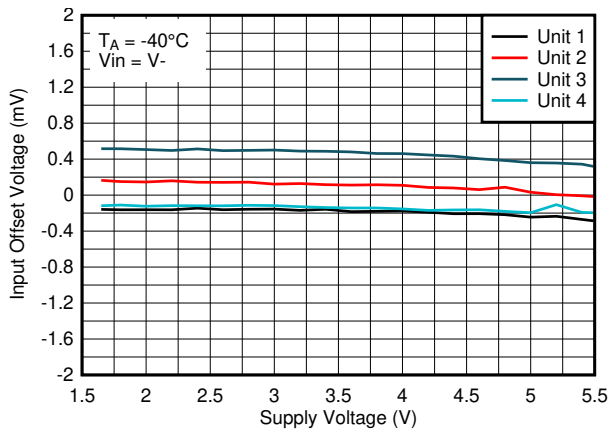


Figure 6-32. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V-

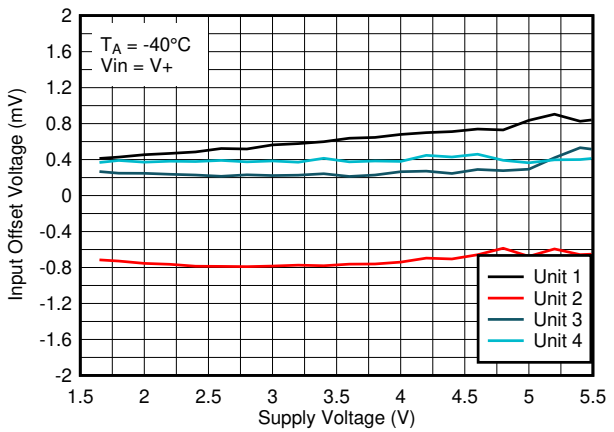


Figure 6-33. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V+

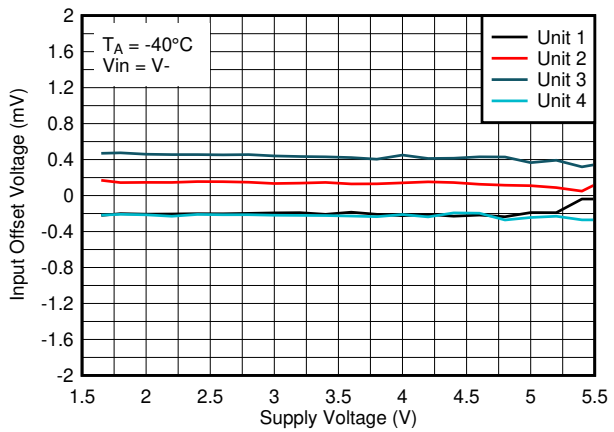


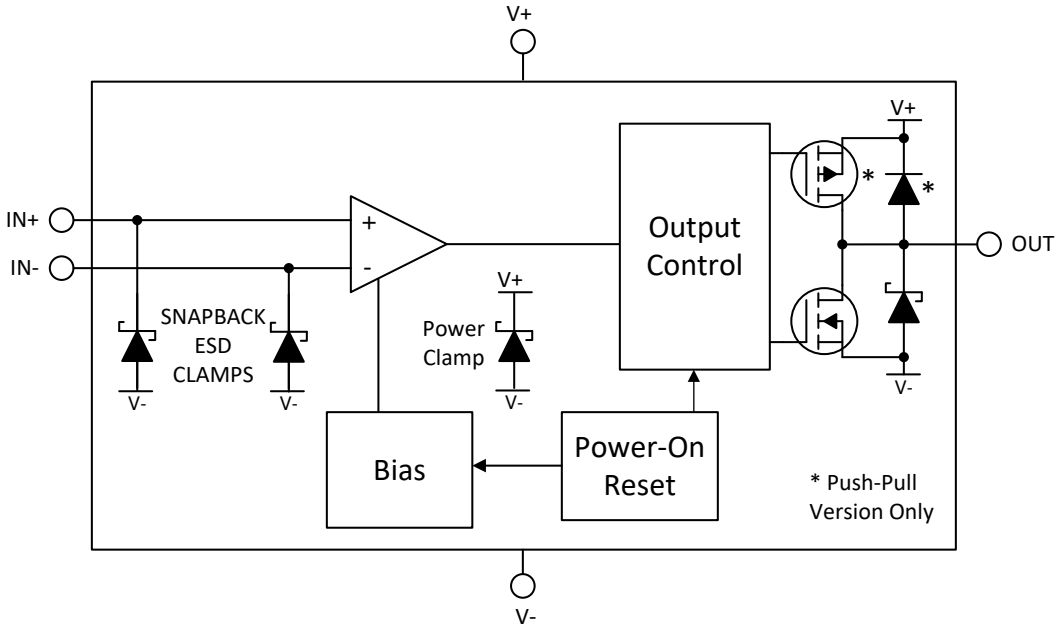
Figure 6-34. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V-

7 Detailed Description

7.1 Overview

The TLV902x-Q1 and TLV903x-Q1 devices are dual-channel, micro-power comparators with push-pull and open-drain outputs and low input offset voltage. Operating down to 1.65 V while only consuming only 16 µA per channel, the TLV902x-Q1 and TLV903x-Q1 are ideally suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV902x-Q1 (open-drain output) and TLV903x-Q1 (push-pull output) devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The TLV90xx-Q1 family feature a rail-to-rail input stage capable of operating up to 200 mV beyond the power supply rails. The comparators also feature push-pull and open-drain output stage options and Power-on Reset for known start-up conditions.

7.4 Device Functional Modes

7.4.1 Outputs

7.4.1.1 TLV9022-Q1 and TLV9024-Q1 Open Drain Output

The TLV902x-Q1 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 5.5 V, independent of the comparator supply voltage (V_S). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime will be dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) will create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs must be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 125 mA, the total combined current for all channels must be less than 200 mA.

7.4.1.2 TLV9032-Q1 and TLV9034-Q1 Push-Pull Output

The TLV903x-Q1 features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200 mA.

7.4.2 Power-On Reset (POR)

The TLV90xx-Q1 has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V_s) is ramping up or ramping down, the POR circuitry will be activated for up to 30µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit will keep the output high impedance (HI-Z) during the POR period (t_{on}).

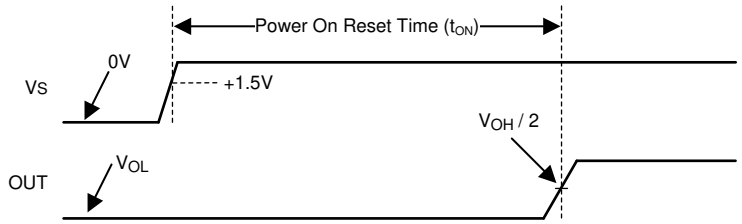


Figure 7-1. Power-On Reset Timing Diagram

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

For the TL903x-Q1 push-pull output devices, the output is "floating" during the POR period. A light pull-up (to V+) or pull-down (to V-) resistor can be used to pre-bias the output condition to prevent the output from floating. If output high is the desired start-up condition, then use the open collector TL902x-Q1, since a pull-up resistor is already required.

7.4.3 Inputs

7.4.3.1 Rail to Rail Input

The TLV90xx-Q1 input voltage range extends from 200mV below V- to 200 mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V+ or V-.

7.4.3.2 Fault Tolerant Inputs

The TLV90xx-Q1 inputs are fault tolerant up to 5.5V independent of V_S. Fault tolerant is defined as maintaining the same high input impedance when V_S is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0 V and 5.5 V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.

2. When IN- is outside the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain datasheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

7.4.3.3 Input Protection

The input bias current is typically 5 pA for input voltages between V+ and V-. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.4 ESD Protection

The TLV90xx-Q1 family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The TLV902x-Q1 open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

The TLV903x-Q1 push-pull output protection consists of a ESD clamp between the output and V-, but also includes a ESD diode clamp to V+, as the output must not exceed the supply rails.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents must the clamps conduct. The current must be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks. TI does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output could exceed the maximum ratings as part of normal operation.

7.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients).

7.4.6 Hysteresis

The TLV90xx-Q1 family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on it's own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 8.1.2 in the following section.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 8-1 and is measured from the mid-point of the input to the midpoint of the output.

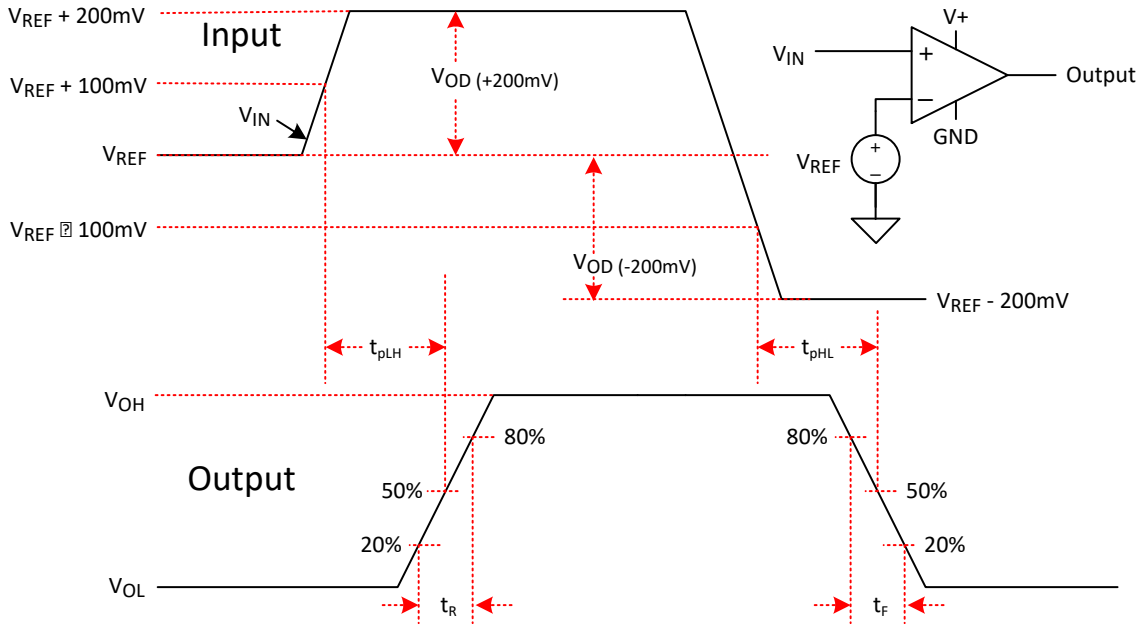


Figure 8-1. Comparator Timing Diagram

8.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 8-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

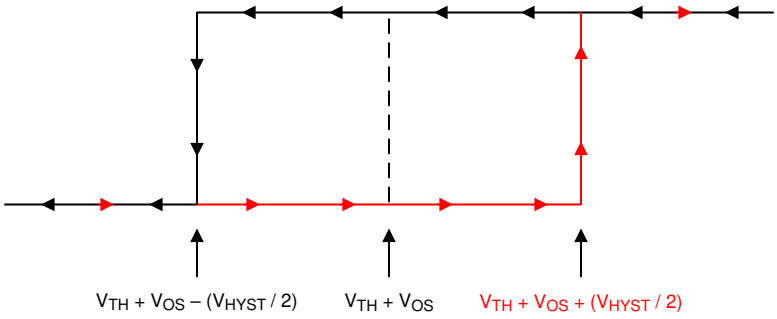


Figure 8-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in Figure 8-3.

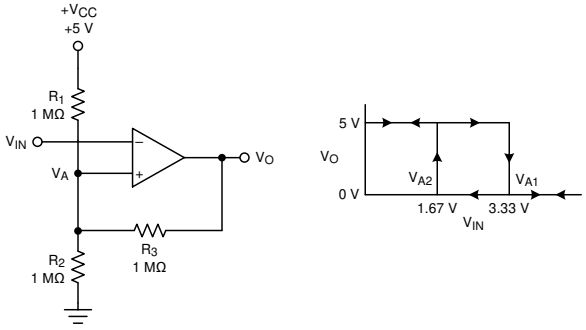


Figure 8-3. TLV903x-Q1in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-3.

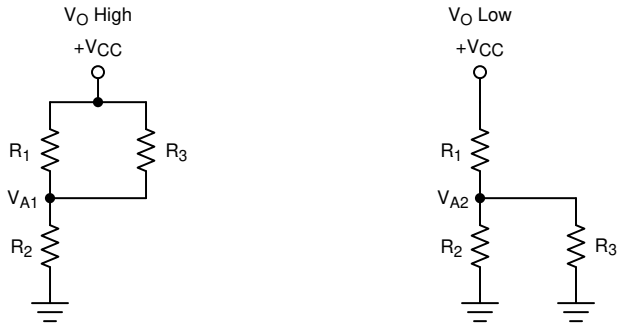


Figure 8-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 8-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

8.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-5,

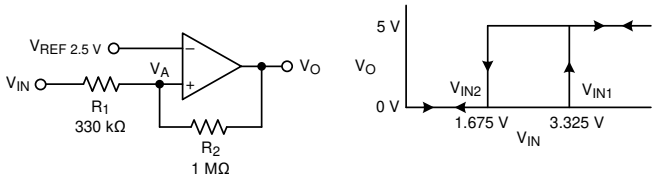


Figure 8-5. TLV903x-Q1 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-6.

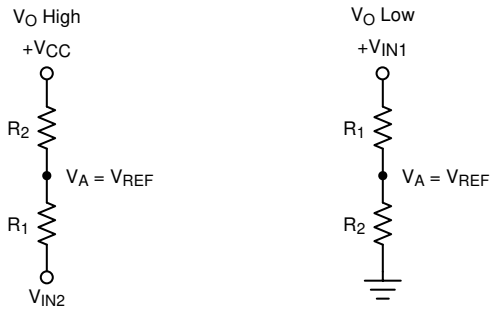


Figure 8-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV902x-Q1, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV902x-Q1) if the outputs are directly connected together.

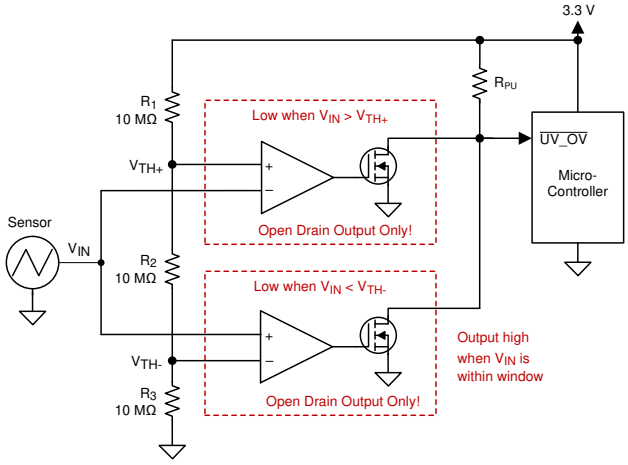


Figure 8-7. Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 8-7. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in Figure 8-8.

8.2.1.3 Application Curve

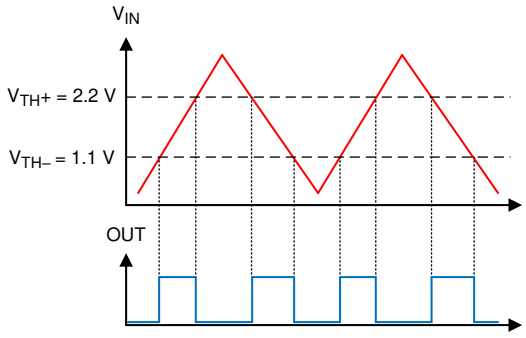


Figure 8-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV903x-Q1) is recommended for best symmetry.

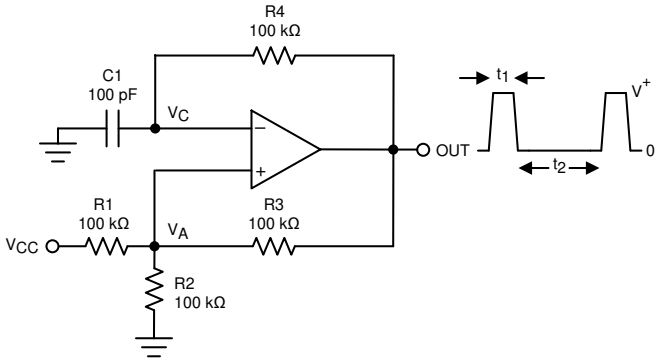


Figure 8-9. Square-Wave Oscillator

8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. R4 must be over several kilo-ohms to minimize loading the output.

8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

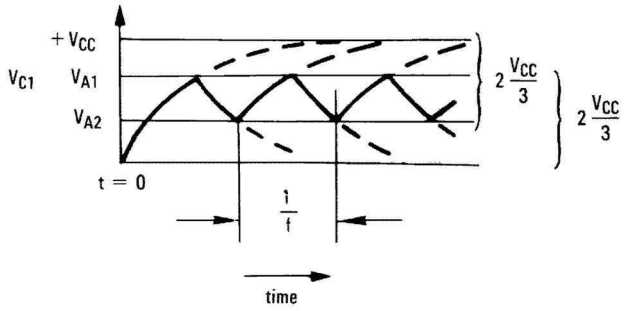


Figure 8-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 8-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\ R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times In2) \quad (9)$$

8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10 pF

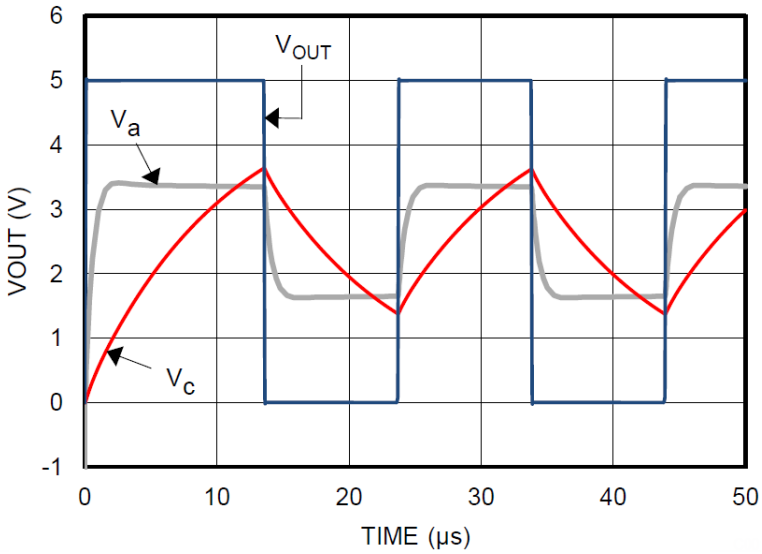


Figure 8-11. Square-Wave Oscillator Output Waveform

8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

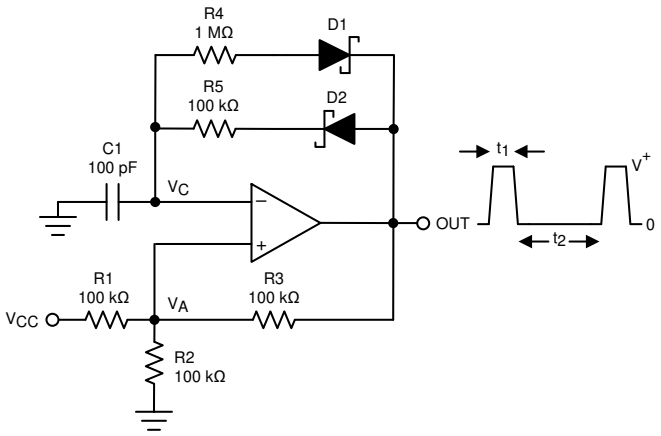


Figure 8-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

8.2.4 Time Delay Generator

The circuit shown in Figure 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

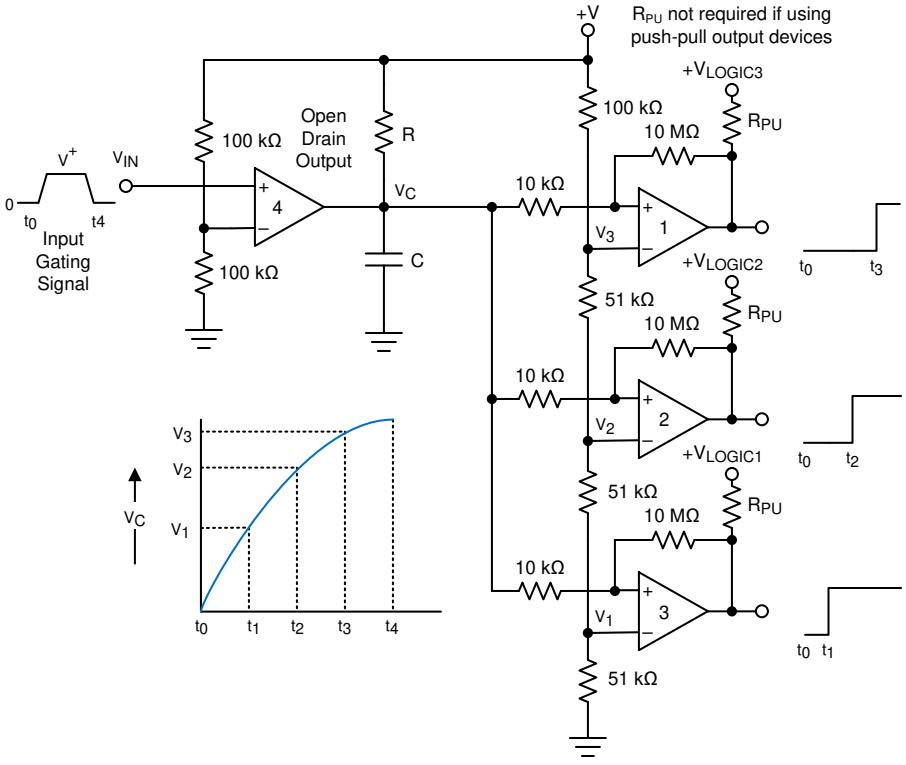


Figure 8-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 swtich to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10 kΩ and 10 MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100 kΩ and C = 0.01 µF to 1 µF.

All outputs will immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x-Q1), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

8.2.5 Logic Level Shifter

The output of the TLV902x-Q1 is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

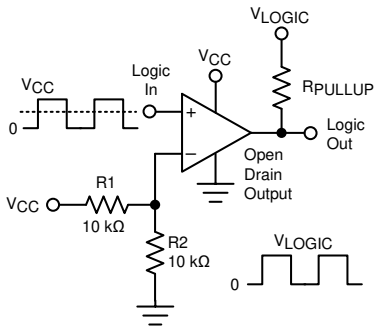


Figure 8-14. Universal Logic Level Shifter

The two 10 kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage must match the driven logic input "high" level.

8.2.6 One-Shot Multivibrator

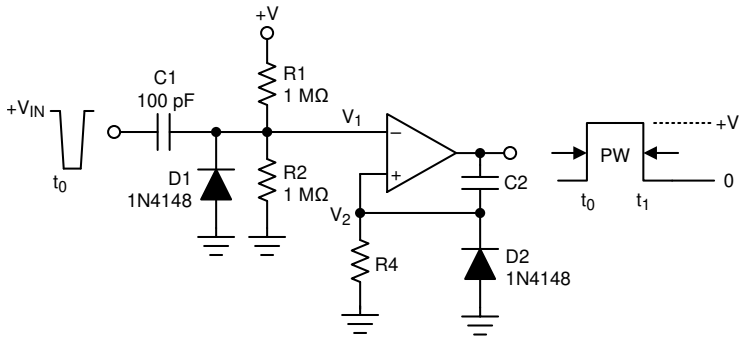


Figure 8-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

8.2.7 Bi-Stable Multivibrator

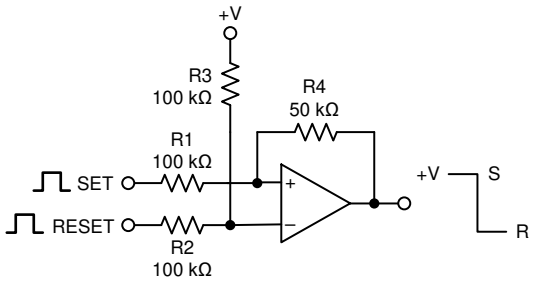


Figure 8-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

8.2.8 Zero Crossing Detector

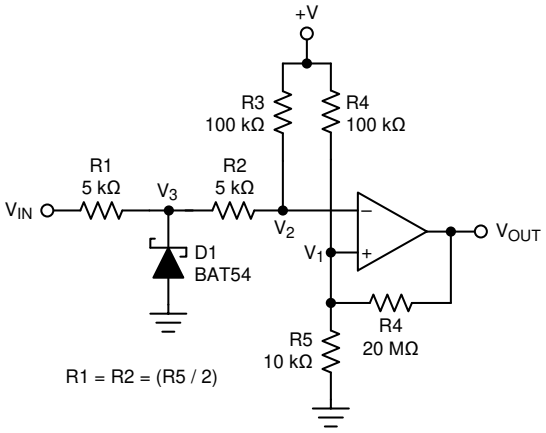


Figure 8-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The noninverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing V_{REF} average voltage.

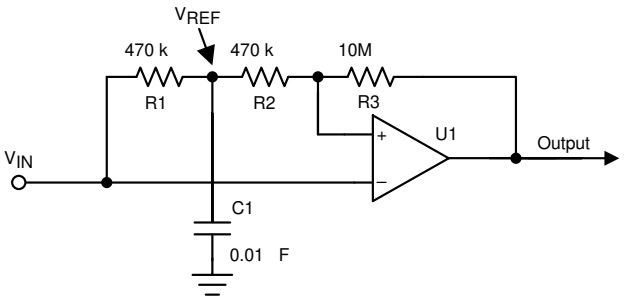


Figure 8-18. Pulse Slicer using TLV903x-Q1

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

The TLV902x-Q1 may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

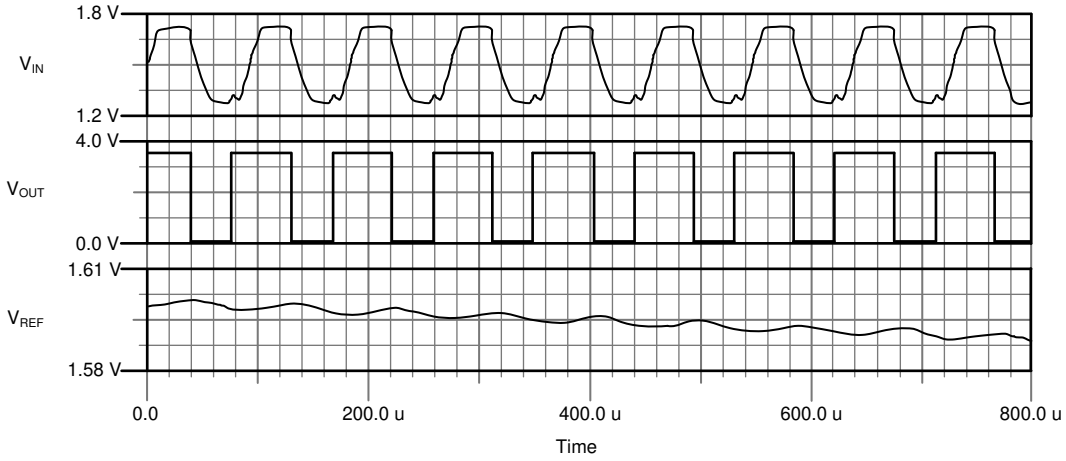


Figure 8-19. Pulse Slicer Waveforms

8.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from either "split" supplies (V+, V- & GND), or a "single" supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on "split" supplies, the ouptut will now swing "low" (V_{OL}) to V- potential and not GND.

9 Layout

9.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

9.2 Layout Example

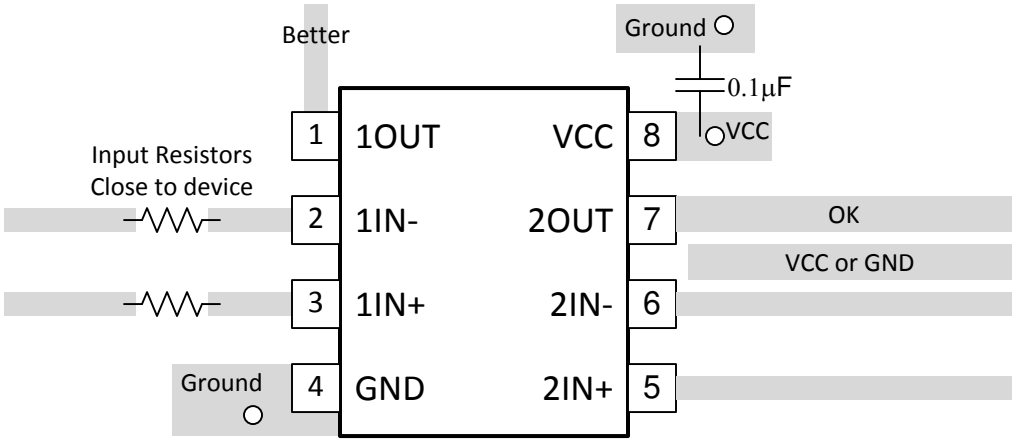


Figure 9-1. Dual Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

PWM generator circuit - SBOA212

How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41

A Quad of Independently Func Comparators - SNOA654

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9032QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TLV9022QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H3FQ	Samples
TLV9022QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IFTQ	Samples
TLV9022QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ022Q	Samples
TLV9022QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9022Q	Samples
TLV9024QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9024Q	Samples
TLV9032QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H2FQ	Samples
TLV9032QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IGTQ	Samples
TLV9032QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9032Q	Samples
TLV9032QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9032Q	Samples
TLV9034QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9034Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV9022-Q1, TLV9024-Q1, TLV9032-Q1, TLV9034-Q1 :

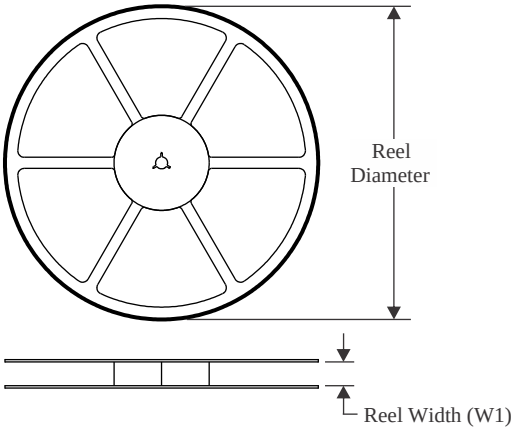
- Catalog : TLV9022, TLV9024, TLV9032, TLV9034

NOTE: Qualified Version Definitions:

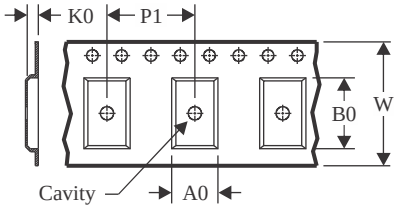
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

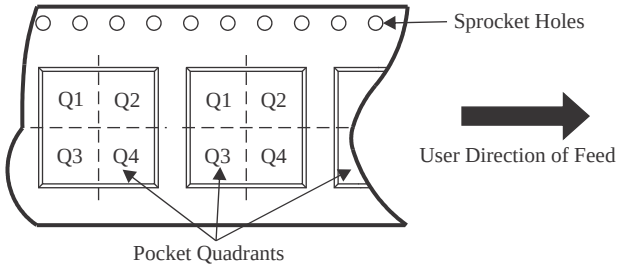


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

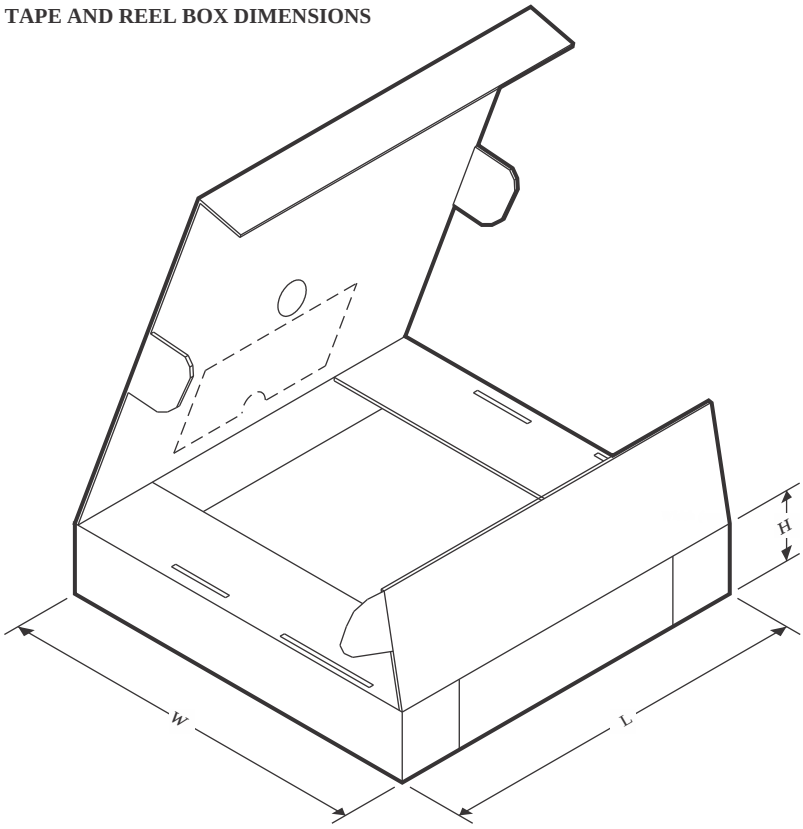
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9022QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9022QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9022QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9024QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9032QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9032QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9032QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9034QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

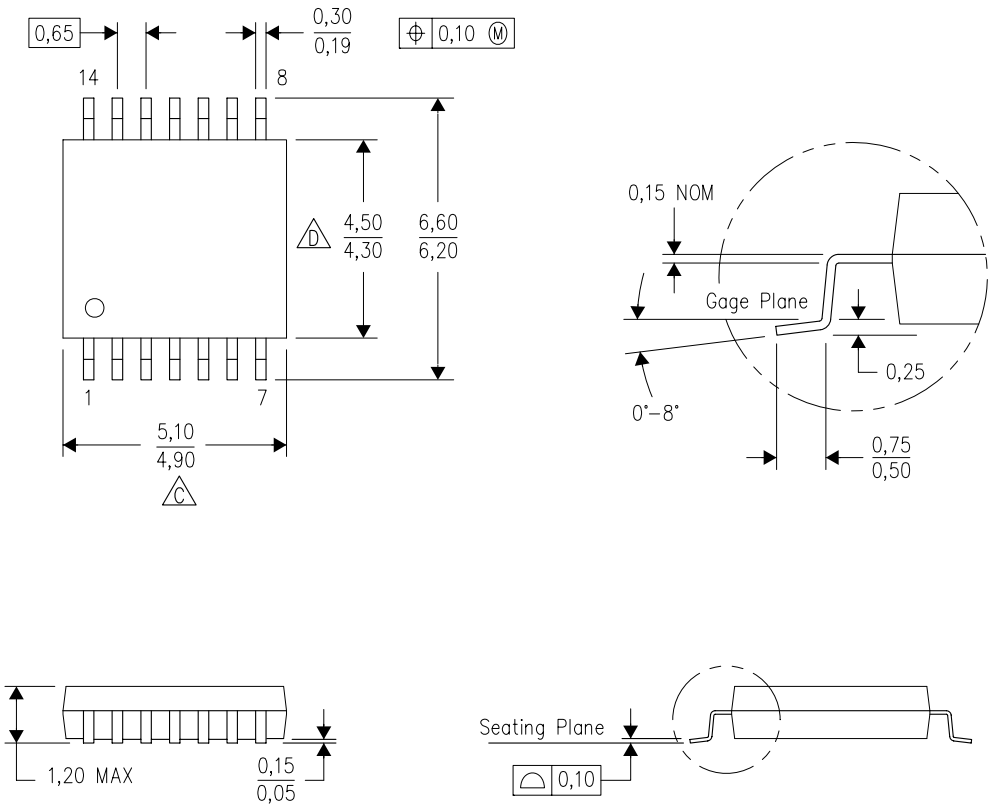
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9022QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9022QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9022QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV9024QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV9032QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9032QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9032QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV9034QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

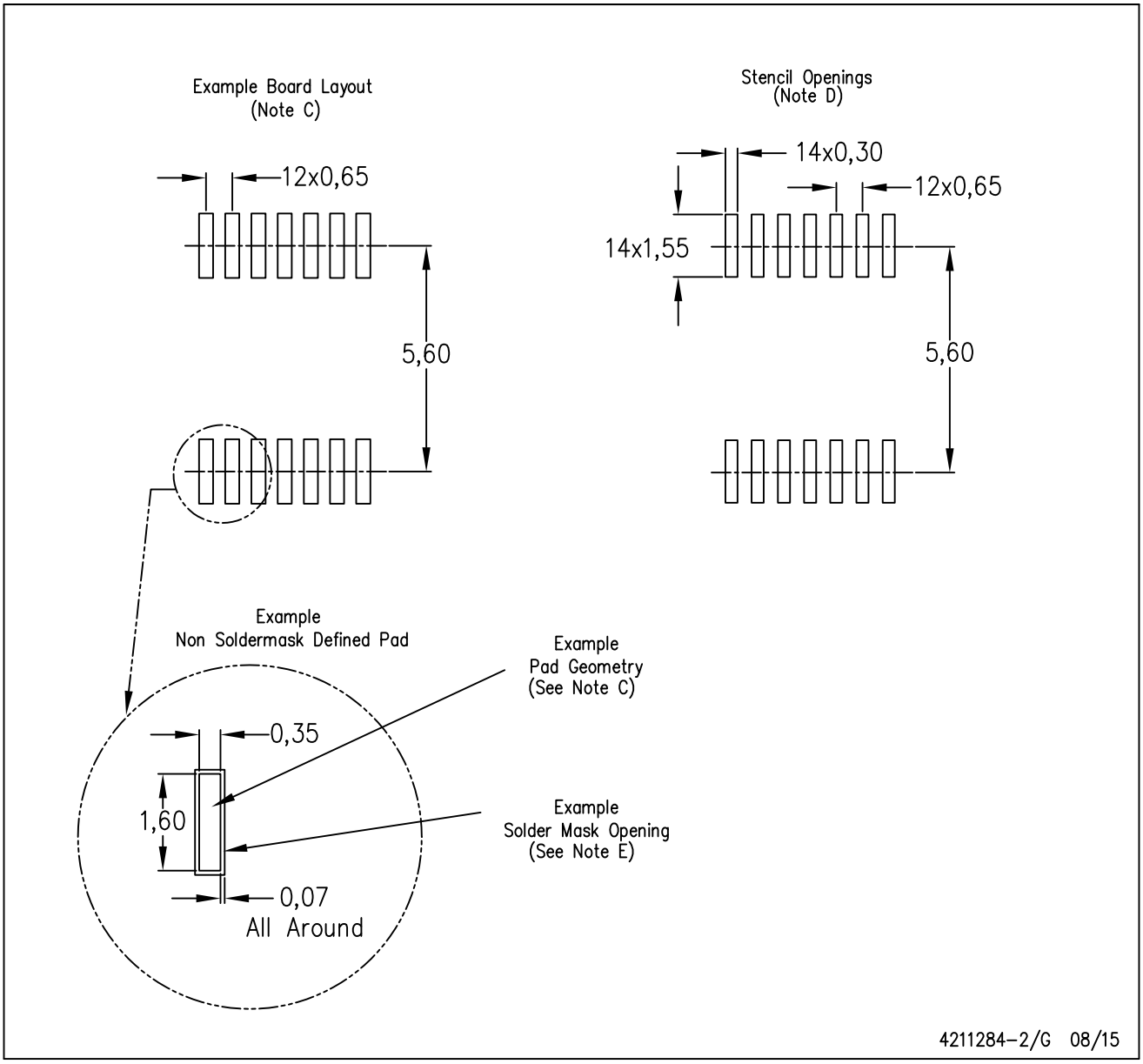
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



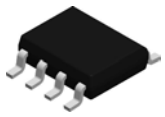
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

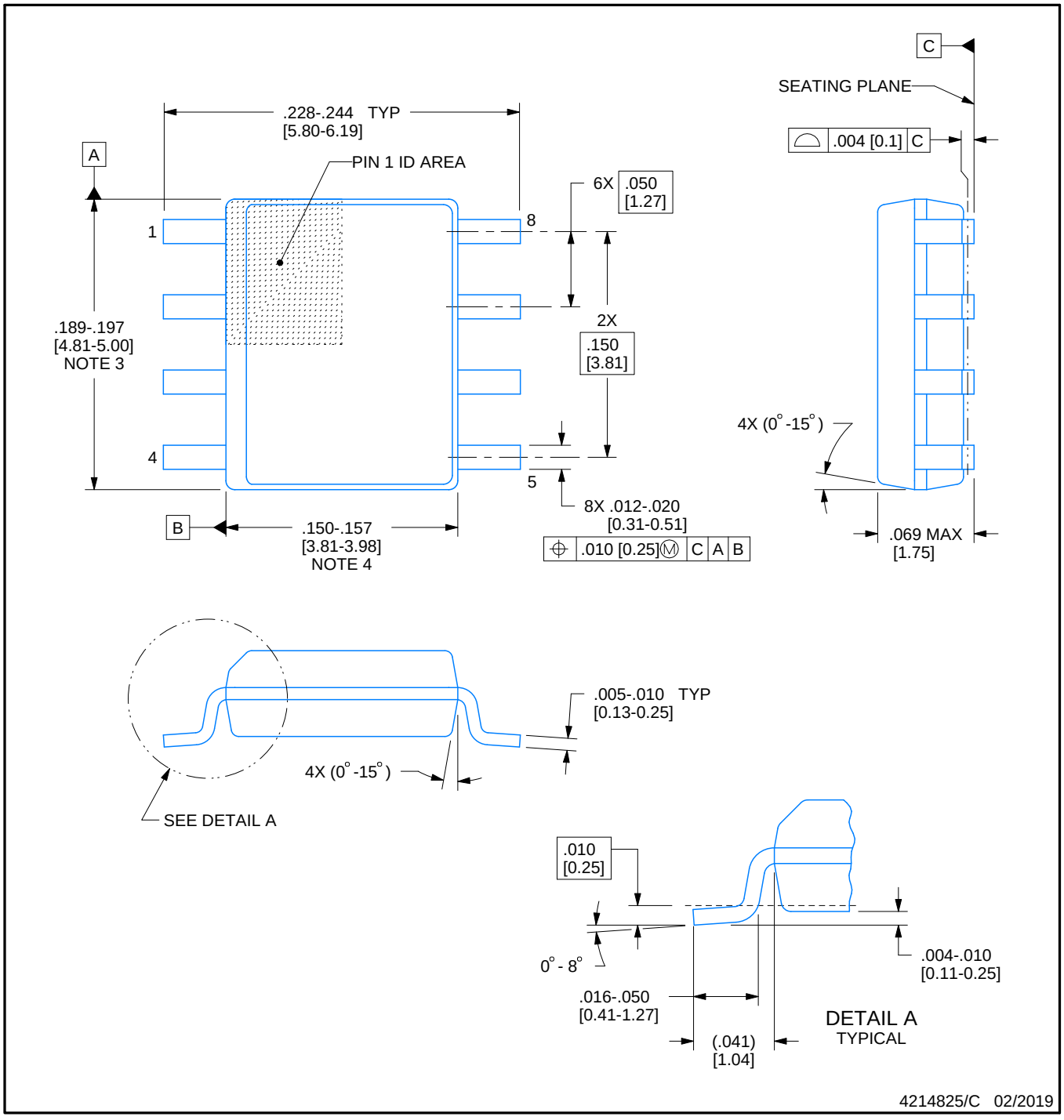


PACKAGE OUTLINE

D0008A

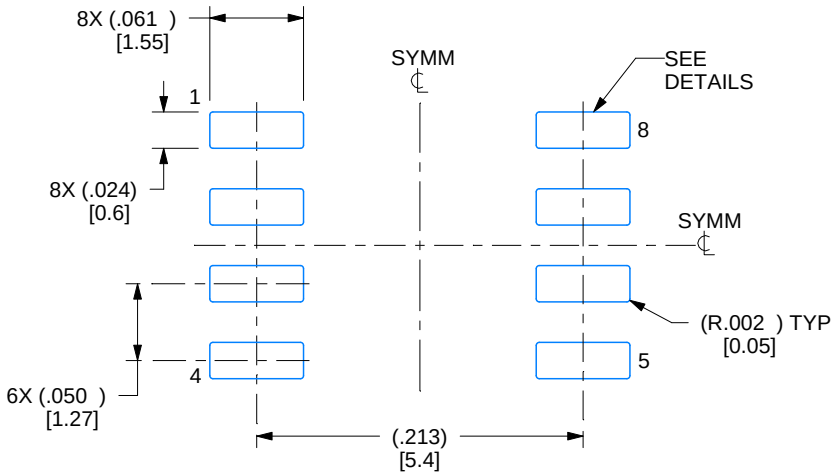
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

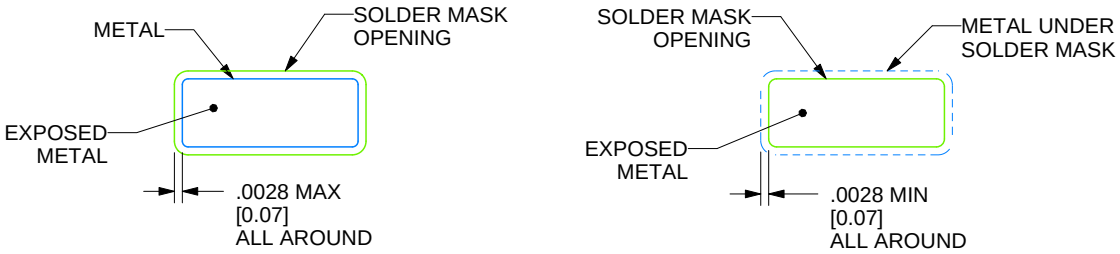


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

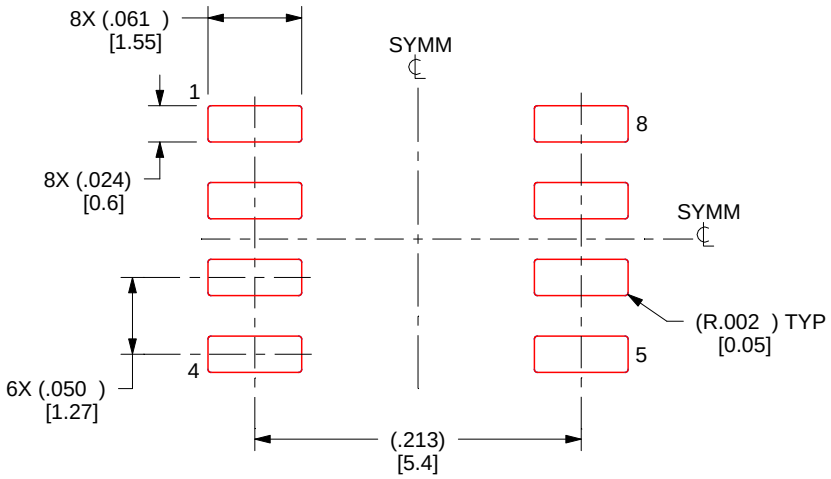
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



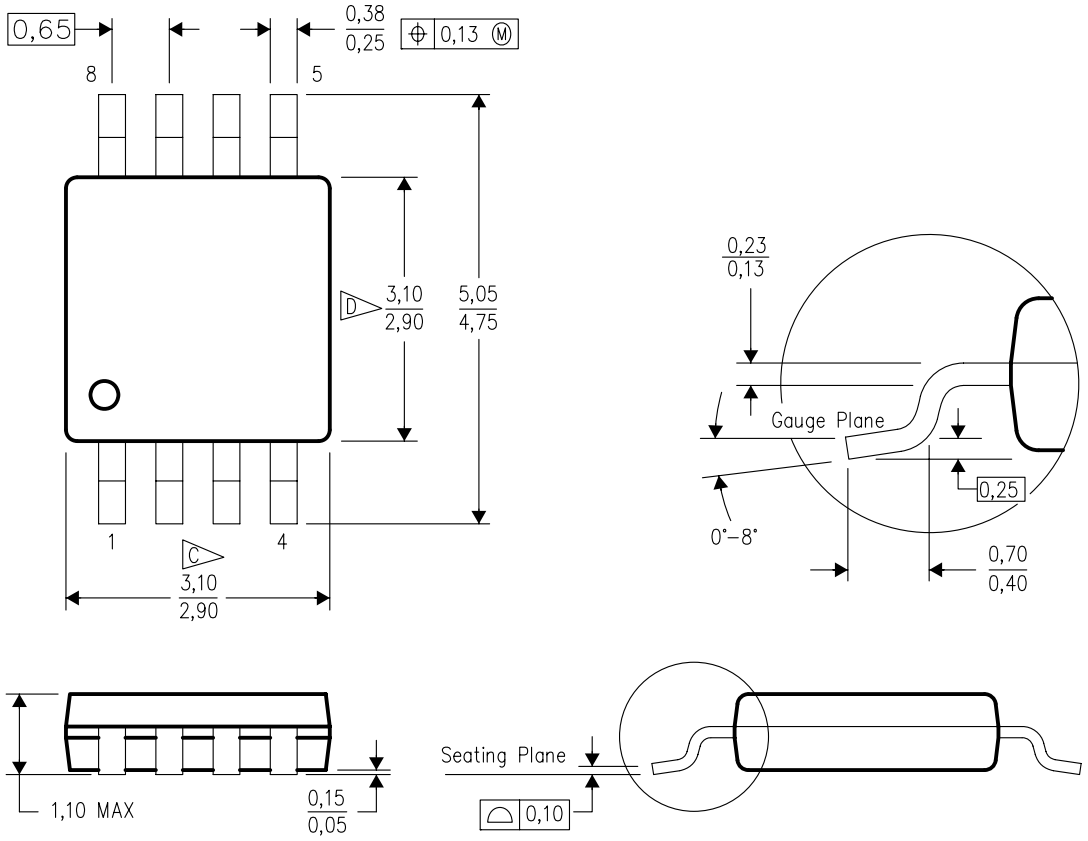
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

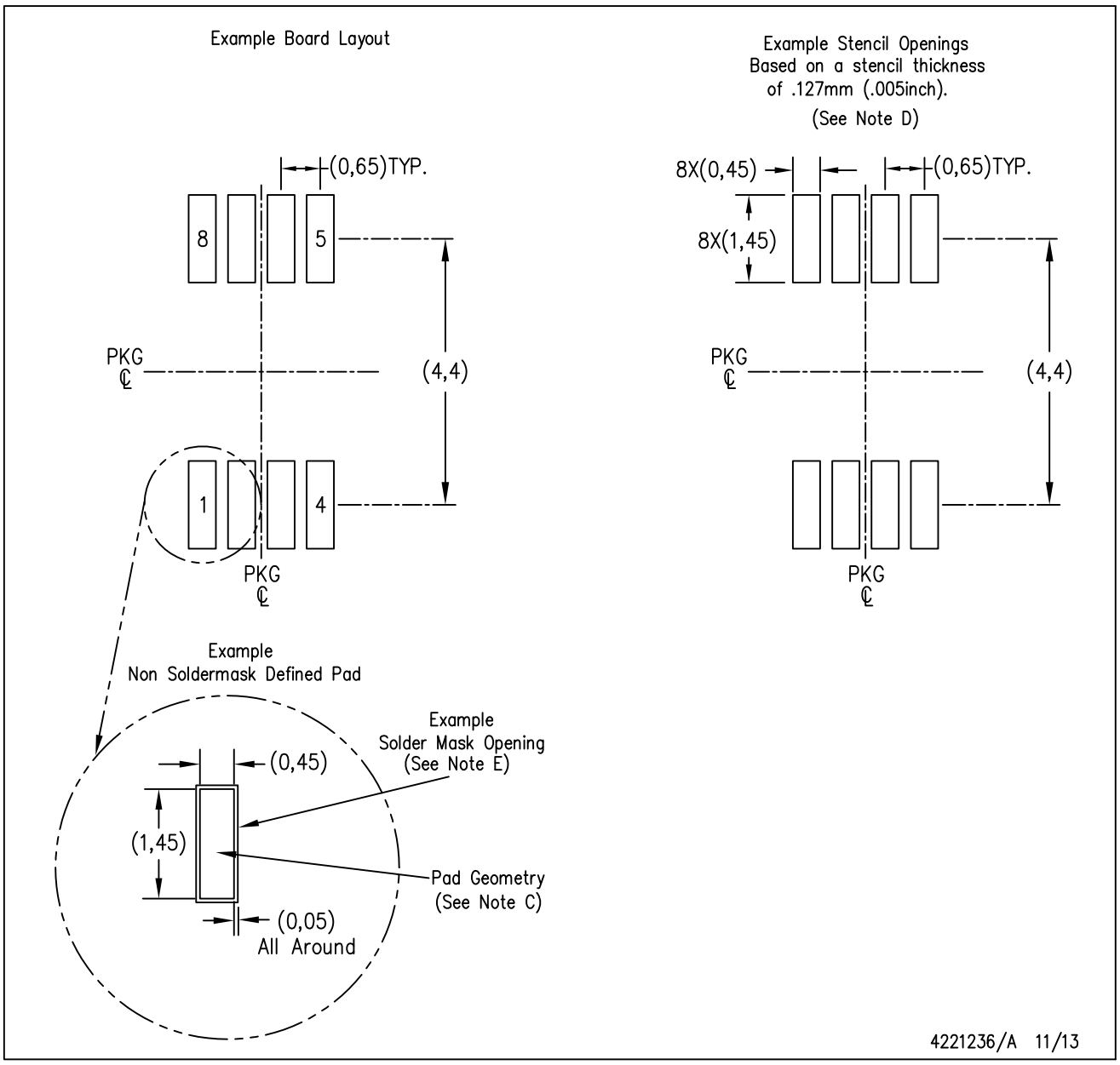
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



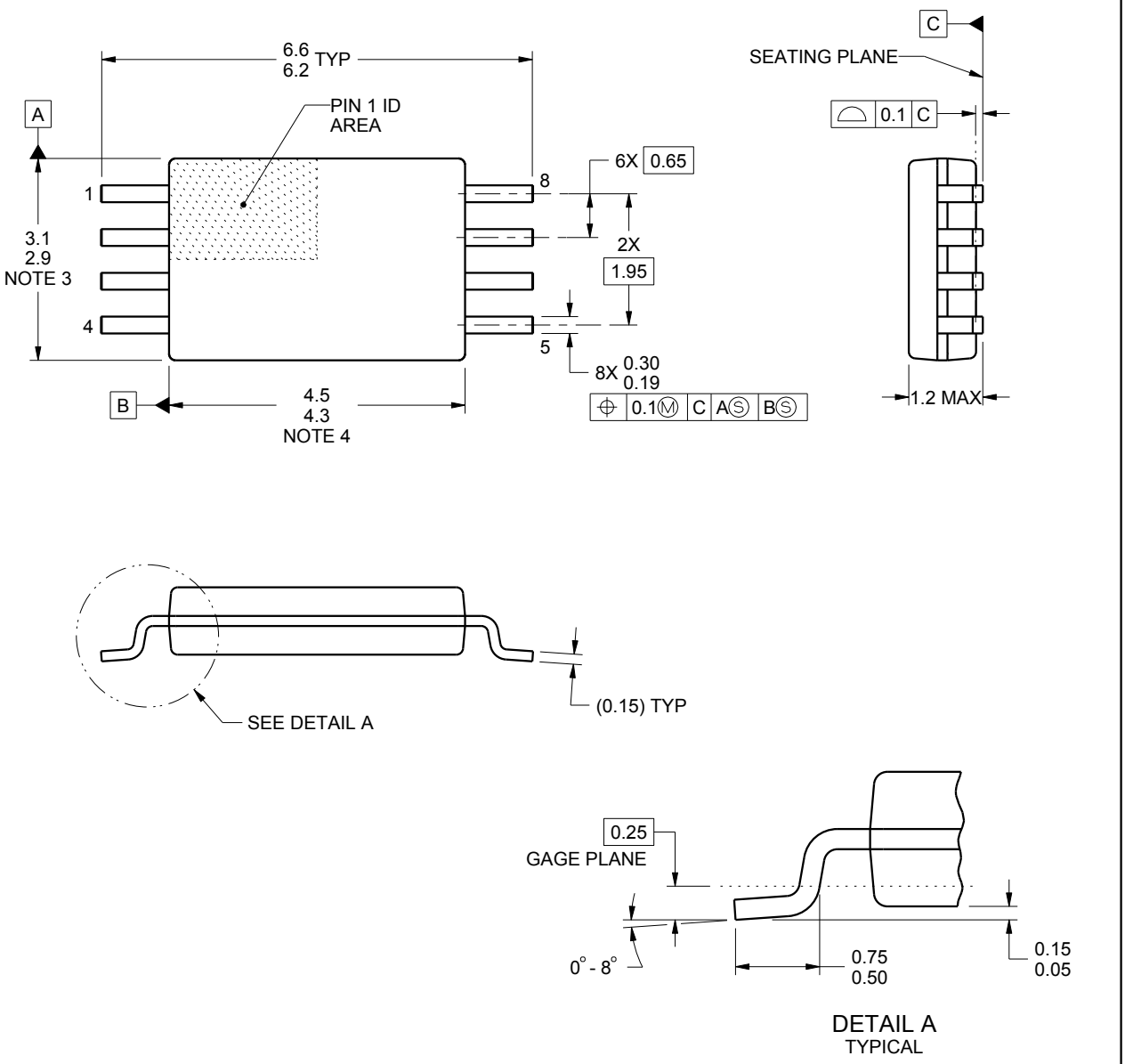
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

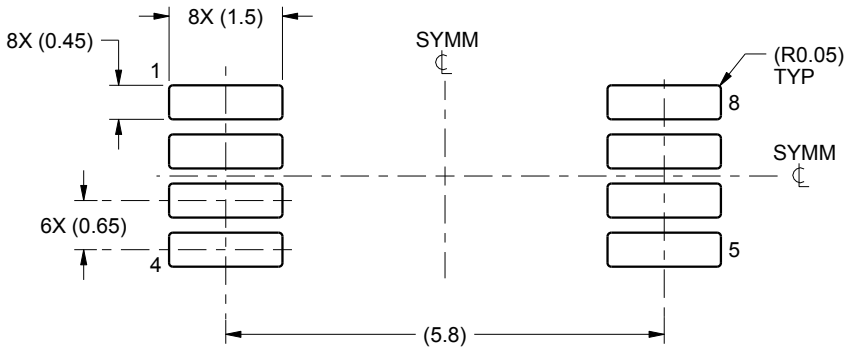
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

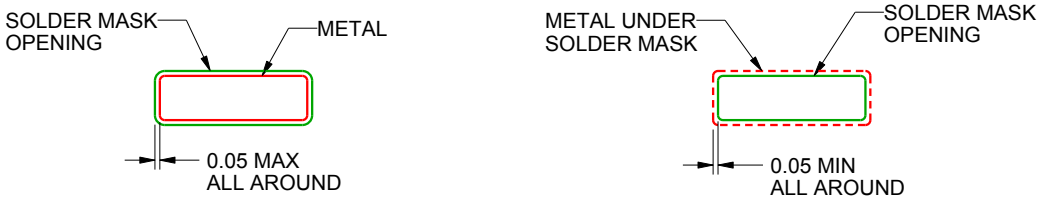


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

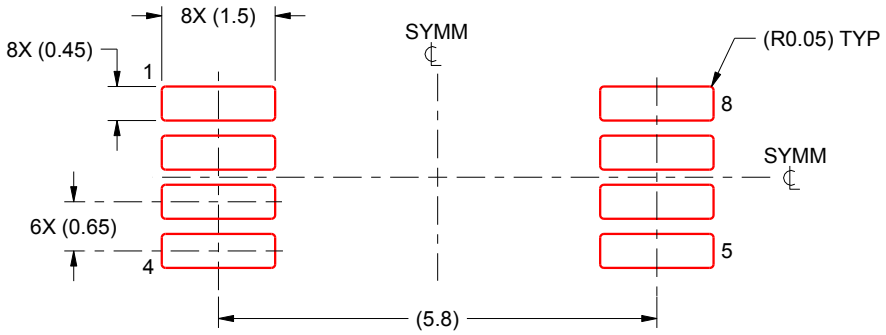


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

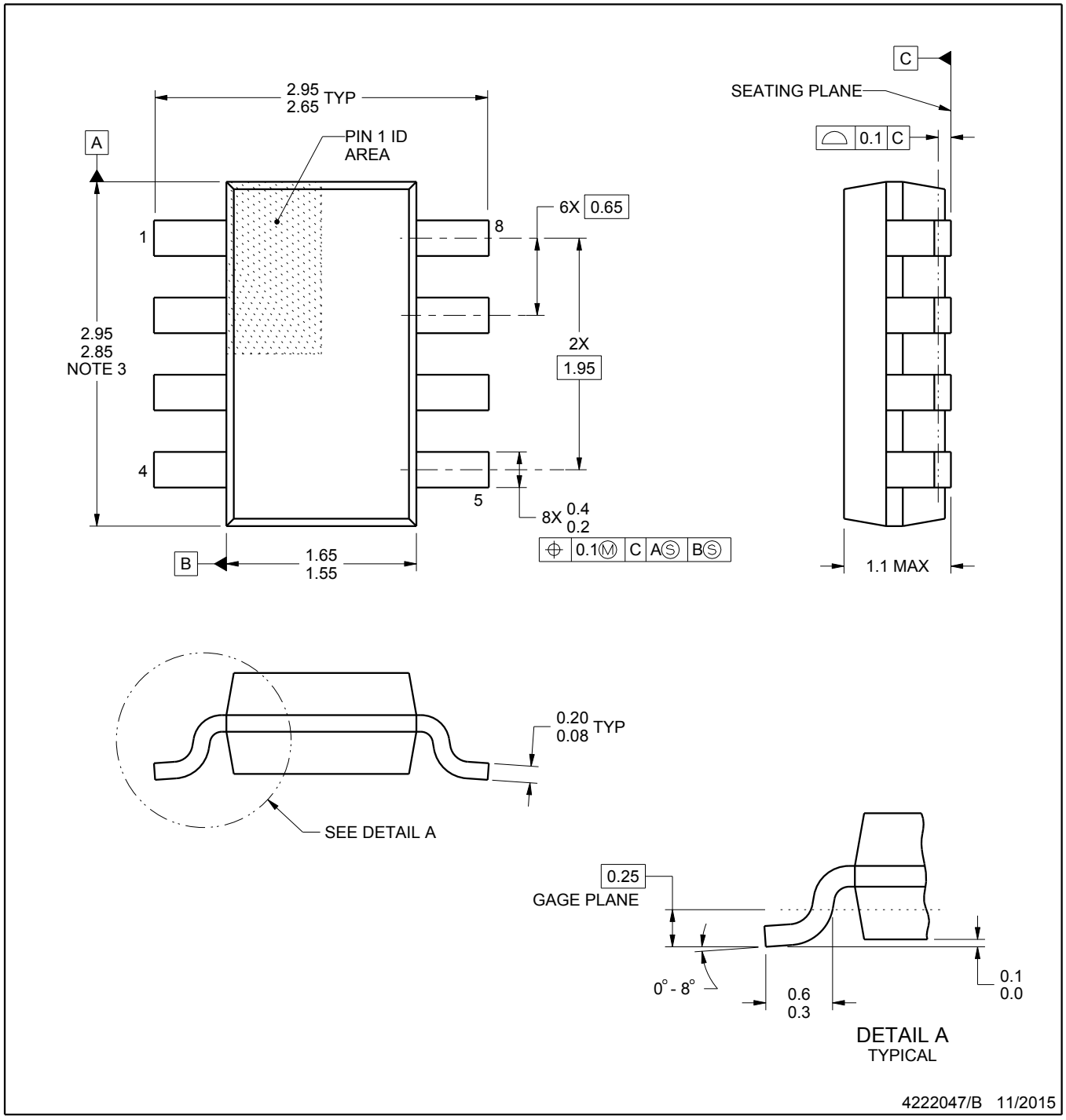
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

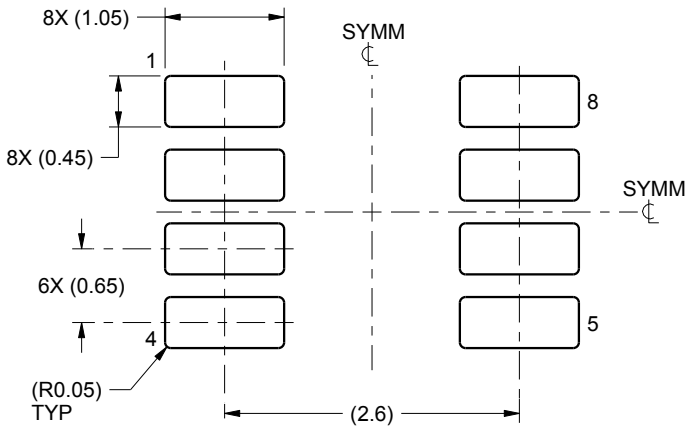
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

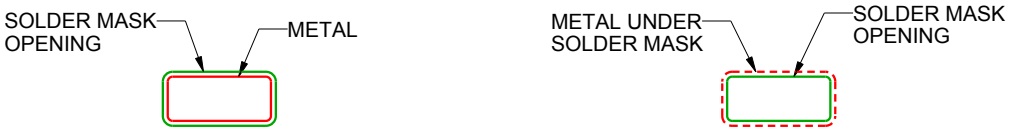


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

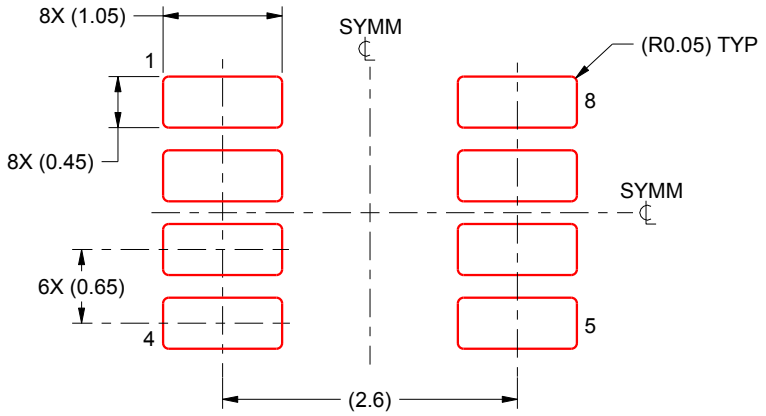
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TLV902x-Q1 and TLV903x-Q1 High-Precision Dual and Quad Automotive Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- 1.65 V to 5.5 V supply range
- Power-On Reset (POR) for known start-up
- Precision input offset voltage 300 µV
- 100ns Typ propagation delay
- Low quiescent current 16 µA per channel
- Rail-to-Rail input voltage range exceeds the rails
- Open-drain output option (TLV902x-Q1)
- Push-pull output option (TLV903x-Q1)
- 2 kV ESD Protection

2 Applications

- Automotive
  - HEV/EV and power train
  - Infotainment and cluster
  - Body control module
- Industrial

3 Description

The TLV902x-Q1 and TLV903x-Q1 are a family of Automotive grade dual and quad channel comparators. The family offers low input offset voltage, integrated Power-On Reset (POR) circuitry, and fault-tolerant inputs with an excellent speed-to-power combination with a propagation delay of 100 ns. Operating voltage range of 1.65 V to 5.5 V with a quiescent supply current of 18 µA per channel.

This device family also includes a Power-on Reset (POR) feature that ensures the output is in a known state until the minimum supply voltage has been reached and a small time period passed before the output starts responding to the inputs. This prevents output transients during system power-up and power-down.

These comparators also feature no output phase inversion with fault-tolerant inputs that can go up to 6-V without damage. This makes this family of comparators well suited for precision voltage monitoring in harsh, noisy environments.

The TLV902x-Q1 comparators have an open-drain output stage that can be pulled below or beyond the supply voltage, making it appropriate for low voltage logic and level translators.

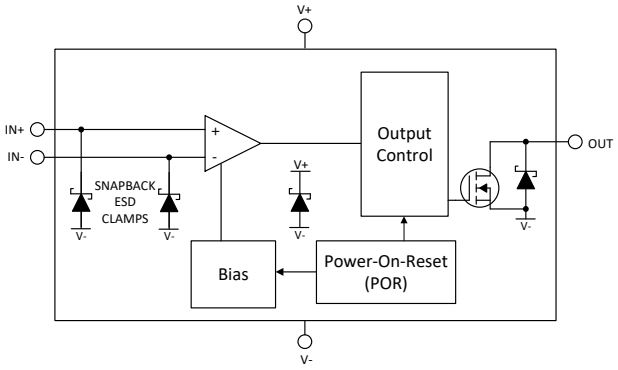
The TLV903x-Q1 comparators have a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate.

The TLV902x-Q1 and TLV903x-Q1 are specified for the Automotive temperature range of -40°C to +125°C and are available in a standard leaded and leadless packages.

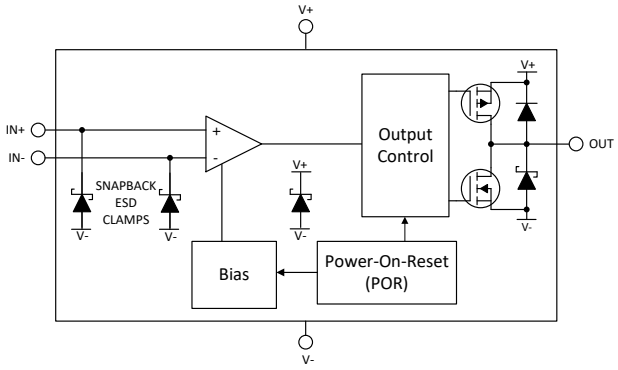
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV9022-Q1, TLV9032-Q1 (Dual)	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	2.00 mm × 2.00 mm
	SOT-23-THN (8)	1.60 mm × 2.90 mm
TLV9024-Q1, TLV9034-Q1 (Quad)	SOIC (14) (Preview)	3.91 mm × 8.65 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	SOT-23 (14) (Preview)	4.20 mm x 2.00 mm
	WQFN (16) (Preview)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TLV9022-Q1 and TLV9024-Q1 Block Diagram



TLV9032-Q1 and TLV9034-Q1 Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2021) to Revision C (January 2022)	Page
• Updated VSSOP status in Device Info table	1

Changes from Revision A (December 2020) to Revision B (August 2021)	Page
• Added status to Device Info table	1

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added tables for Quad	5
• Added Typical Graphs	11

5 Pin Configuration and Functions

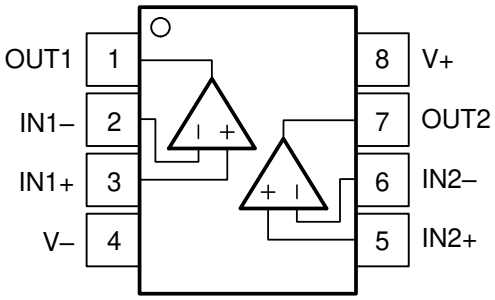
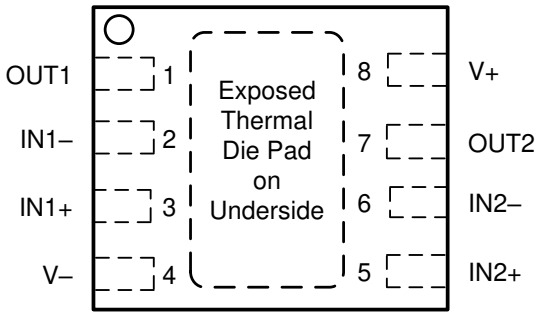


Figure 5-1. D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23-8 Top View



NOTE: Connect exposed thermal pad directly to V- pin.

Figure 5-2. DSG Package, 8-Pad WSON With Exposed Thermal Pad, Top View

Pin Functions: TLV90x2-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V–	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to V- pin

Pin Functions: TLV90x4-Q1

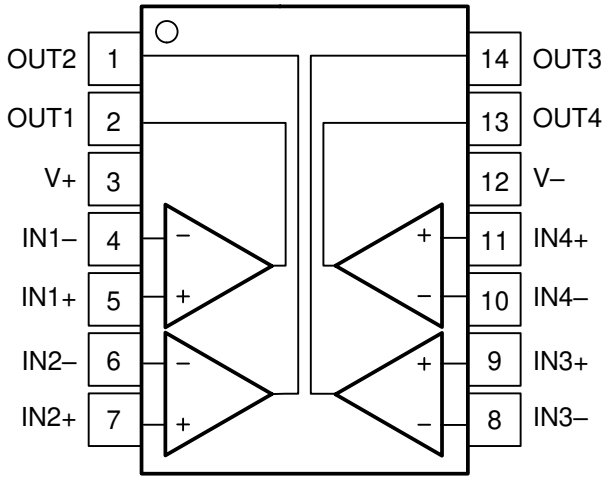
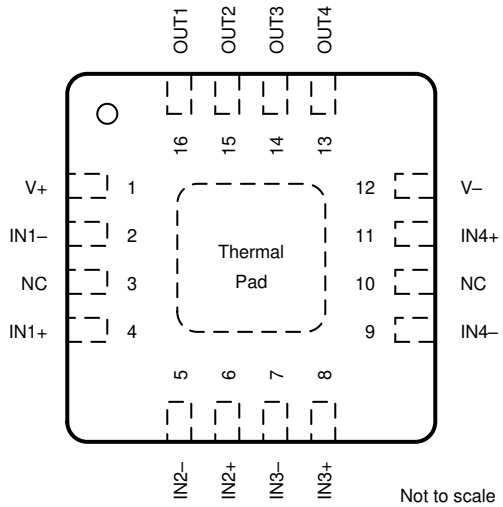


Figure 5-3. D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23, Top View



NOTE: Connect exposed thermal pad directly to V- pin.

Figure 5-4. RTE Package, 16-Pad WQFN With Exposed Thermal Pad, Top View

Table 5-1. Pin Functions: TLV90x4-Q1

PIN			I/O	DESCRIPTION
NAME[1]	SOIC	WQFN		
OUT2	1	15	Output	Output pin of the comparator 2
OUT1	2	16	Output	Output pin of the comparator1
V+	3	1	—	Positive supply
IN1–	4	2	Input	Negative input pin of the comparator 1
IN1+	5	4	Input	Positive input pin of the comparator 1
IN2–	6	5	Input	Negative input pin of the comparator 2
IN2+	7	6	Input	Positive input pin of the comparator 2
IN3–	8	7	Input	Negative input pin of the comparator 3
IN3+	9	8	Input	Positive input pin of the comparator 3
IN4–	10	9	Input	Negative input pin of the comparator 4
IN4+	11	11	Input	Positive input pin of the comparator 4
V–	12	12	—	Negative supply
OUT4	13	13	Output	Output pin of the comparator 4
OUT3	14	14	Output	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to V- pin.

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in channel naming convention.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	6	V
Input pins (IN+, IN–) from V–(2)	–0.3	6	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) from V–, open drain only(3)	–0.3	6	V
Output (OUT) from V–, push-pull only	–0.3	(V+) + 0.3	V
Output short circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, Tstg	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less. Additionally, Inputs (IN+, IN–) can be greater than V+ and OUT as long as it is within the –0.3 V to 6 V range
(3) Output (OUT) for open drain can be greater than V+ and inputs (IN+, IN–) as long as it is within the –0.3 V to 6 V range
(4) Short-circuit to V– or V+. Short circuits from outputs can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.65	5.5	V
Input voltage range (IN+, IN–) from (V–)	–0.2	5.7	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information, TLV90x2-Q1

THERMAL METRIC (1)		TLV90x2-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	167.7	221.7	215.8	175.2	240.0	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	107.0	109.1	105.2	178.1	151.0	°C/W
R_{qJB}	Junction-to-board thermal resistance	111.2	152.5	137.5	139.5	157.0	°C/W
y_{JT}	Junction-to-top characterization parameter	53.1	36.4	39.6	47.2	32.8	°C/W
y_{JB}	Junction-to-board characterization parameter	110.4	150.7	135.9	138.9	155.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	127.3	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information, TLV90x4-Q1

THERMAL METRIC(1)		TLV90x4-Q1				UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)	DYY (SOT-23)	
		14 PINS	14 PINS	16 PINS	14 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	136.0	155.0	134.1	–	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	91.2	82.0	122.6	–	°C/W
R_{qJB}	Junction-to-board thermal resistance	92.0	98.5	109.3	–	°C/W
y_{JT}	Junction-to-top characterization parameter	46.9	25.7	30.9	–	°C/W
y_{JB}	Junction-to-board characterization parameter	91.6	97.6	108.3	–	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	98.7	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = (V–) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 Vx	–1.5	±0.3	1.5	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–2		2	
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		16	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			35	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull verison)	75	95		dB
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C (open drain version)	80	95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	60	70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal differential voltage amplification	For open drain version only	50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = 25°C (push-pull only)		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = –40°C to +125°C (push-pull only)			175	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C (open drain only)		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	90	100		mA
I_{SC}	Short-circuit current	V_S = 5 V, Sourcing (push-pull only)	90	100		mA

6.7 Switching Characteristics,

For V_S (Total Supply Voltage) = (V+) – () = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		100		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (for push-pull only)		115		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		150		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		3		ns
T_{RISE}	5V Output Rise Time, 20% to 80%	V_{ID} = 100 mV (for push-pull only)		3		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ for open drain only)		3		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (V–), V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ for open drain only)		20		µs

6.8 Electrical Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = (V–) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 Vx	–1.5	±0.3	1.5	mV
V_{OS}	Input offset voltage	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	–2		2	
dV_{IO}/dT	Input offset voltage drift	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low		16	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8 V and 5 V, No Load, Output Low, T_A = –40°C to +125°C			35	
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull version)			177.8	µV/V
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (push-pull version)	75	95		dB
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (open drain version)			100	µV/V
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 5 V, T_A = –40°C to +125°C, (open drain version)	80	95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V and 5 V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	60	70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8 V, (V–) – 0.2 V < V_{CM} < (V+) + 0.2 V, T_A = –40°C to +125°C	50	60		dB
OPEN-LOOP GAIN						
A_{VD}	Large signal differential voltage amplification	For open-drain version only	50	200		V/mV
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = 25°C (push-pull only)		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4 mA, T_A = –40°C to +125°C (push-pull only)			175	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C (open drain only)		100		pA
I_{SC}	Short-circuit current	V_S = 5 V, Sinking	90	100		mA
I_{SC}	Short-circuit current	V_S = 5 V, Sourcing (push-pull only)	90	100		mA

6.9 Switching Characteristics,

For V_S (Total Supply Voltage) = (V+) – (V–) = 5 V, V_{CM} = V_S / 2, C_L = 15 pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{ID} = –100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		100		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (for push-pull only)		115		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{ID} = 100 mV; Delay from mid-point of input to mid-point of output (R_P = 2.5 KΩ for open drain only)		150		ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100 mV		3		ns
T_{RISE}	5V Output Rise Time, 20% to 80%	V_{ID} = 100 mV, for push-pull only		3		ns
F_{TOGGLE}	5V, Toggle Frequency	V_{ID} = 100 mV (R_P = 2.5 KΩ for open drain only)		3		MHz
POWER ON TIME						
P_{ON}	Power on-time	V_S = 1.8 V and 5 V, V_{CM} = (V–), V_{ID} = –0.1 V, $V_{PULL-UP}$ = V_S / 2, Delay from V_S / 2 to V_{OUT} = 0.1 x V_S / 2 (R_P = 2.5 KΩ for open drain only)		30		µs

6.10 Typical Characteristics

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

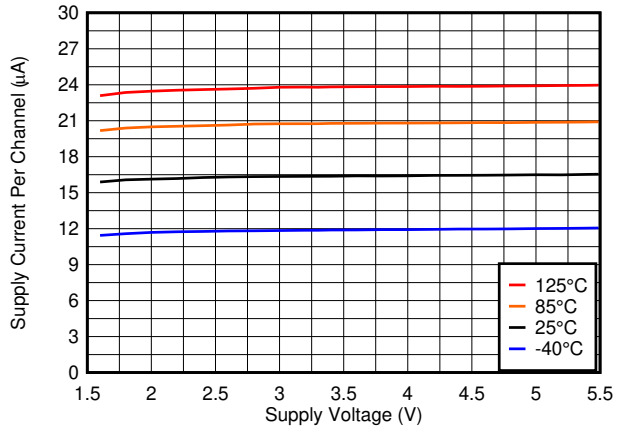


Figure 6-1. Supply Current vs. Supply Voltage

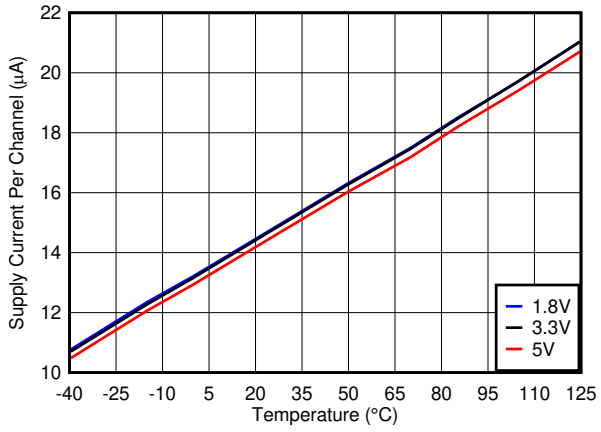


Figure 6-2. Supply Current vs. Temperature

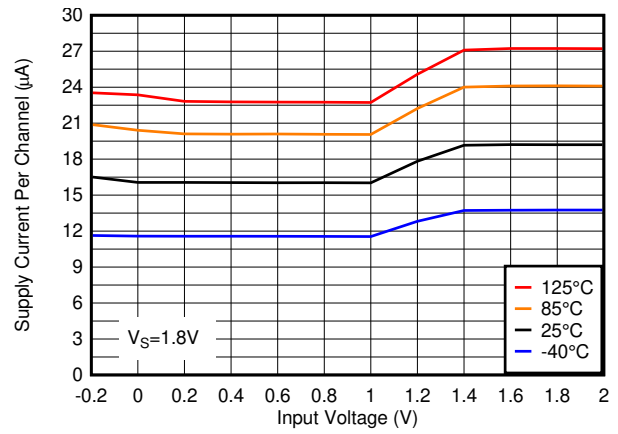


Figure 6-3. Supply Current vs. Input Voltage, 1.8V

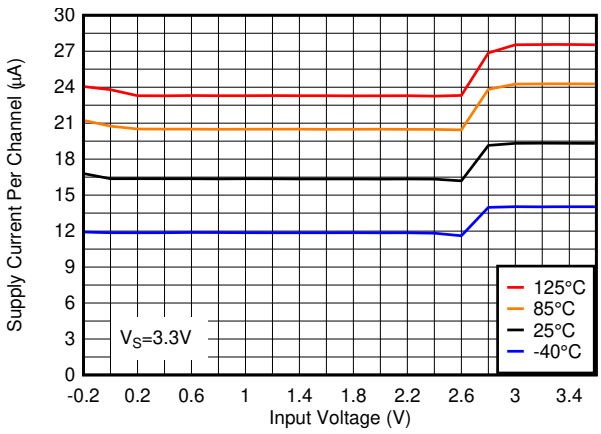


Figure 6-4. Supply Current vs. Input Voltage, 3.3V

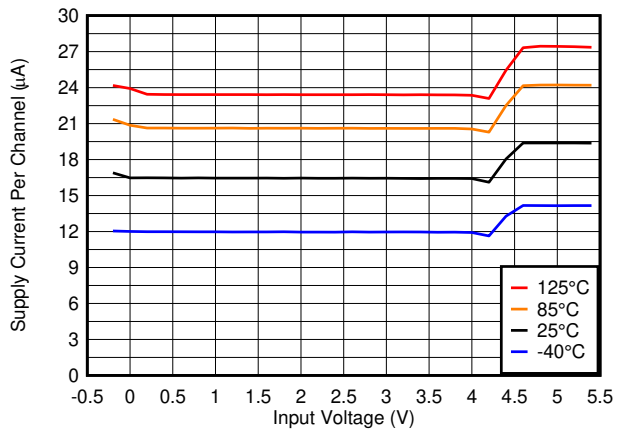


Figure 6-5. Supply Current vs. Input Voltage, 5V

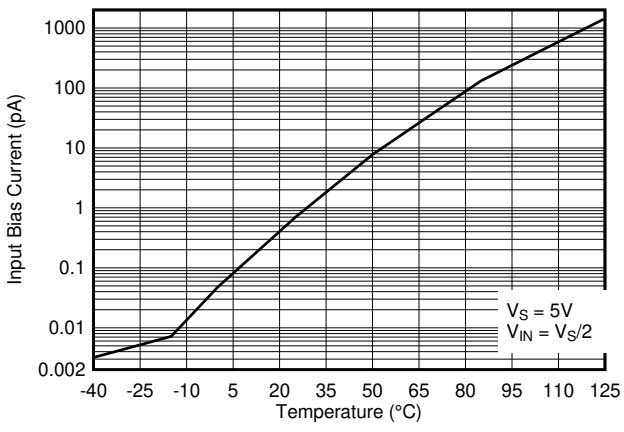


Figure 6-6. Input Bias Current vs. Temperature

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

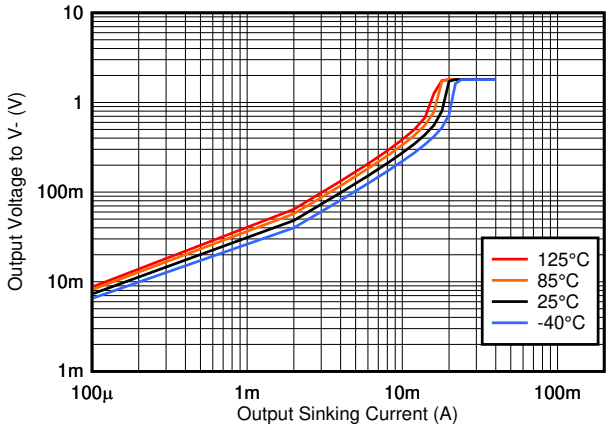


Figure 6-7. Output Sinking Current vs. Output Voltage, 1.8V

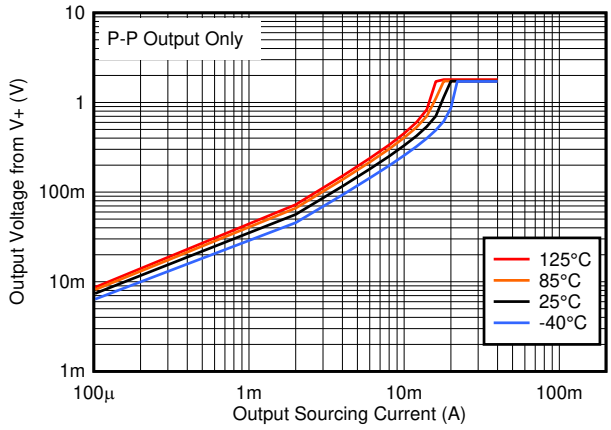


Figure 6-8. Output Sourcing Current vs. Output Voltage, 1.8V

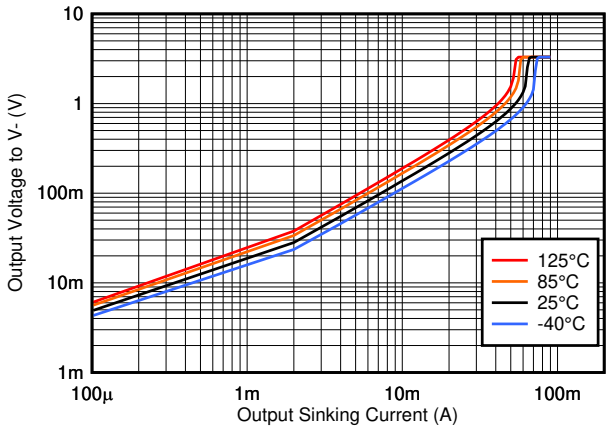


Figure 6-9. Output Sinking Current vs. Output Voltage, 3.3V

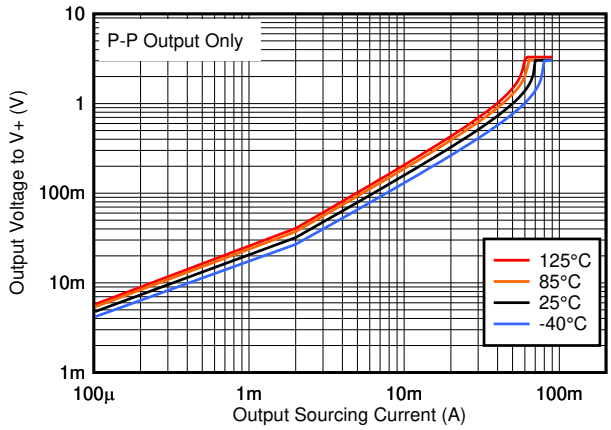


Figure 6-10. Output Sourcing Current vs. Output Voltage, 3.3V

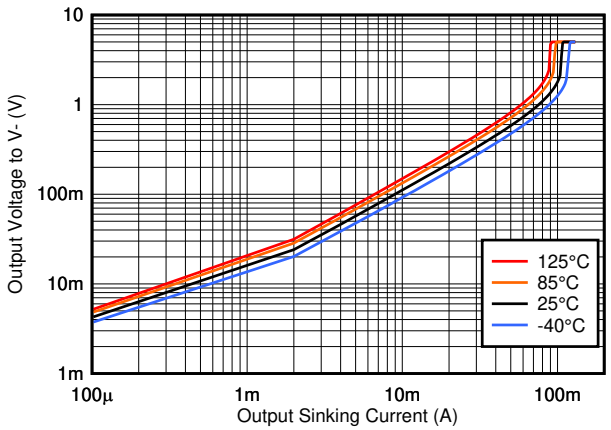


Figure 6-11. Output Sinking Current vs. Output Voltage, 5V

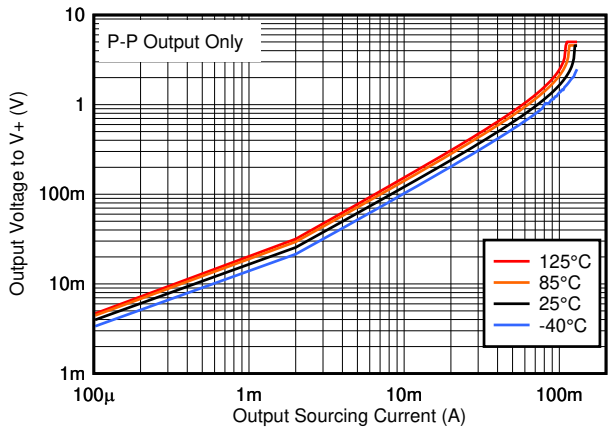


Figure 6-12. Output Sourcing Current vs. Output Voltage, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

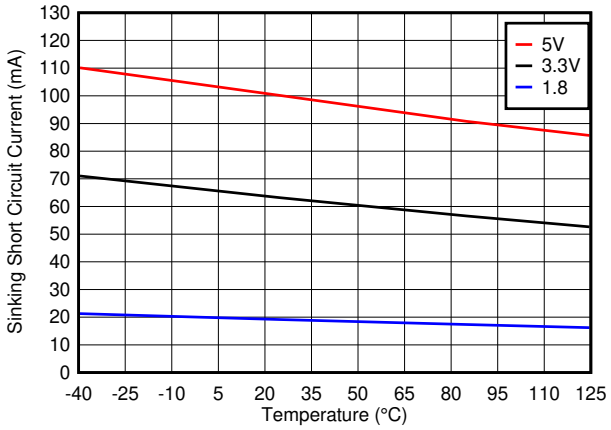


Figure 6-13. Sinking Short Circuit Current vs. Temperature

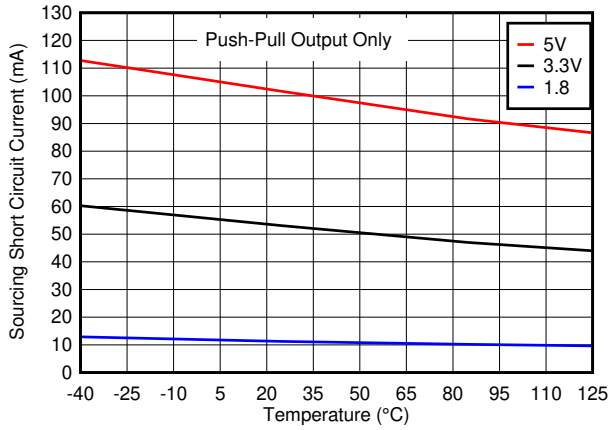


Figure 6-14. Sourcing Short Circuit Current vs. Temperature

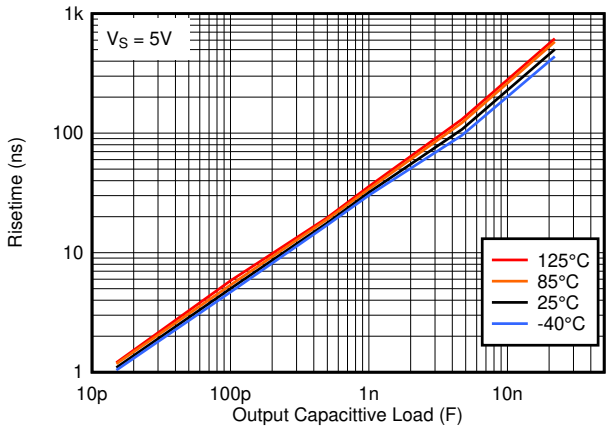


Figure 6-15. Risetime vs. Capacitive Load

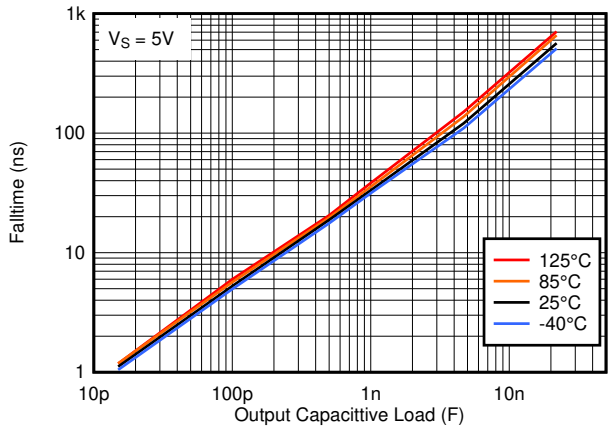


Figure 6-16. Falltime vs. Capacitive Load

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

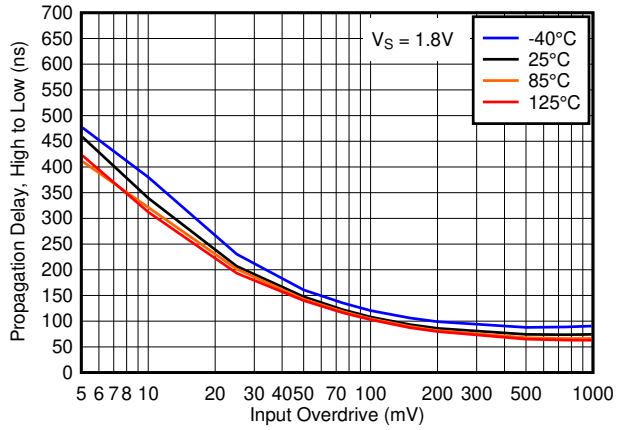


Figure 6-17. Propagation Delay, High to Low, 1.8V

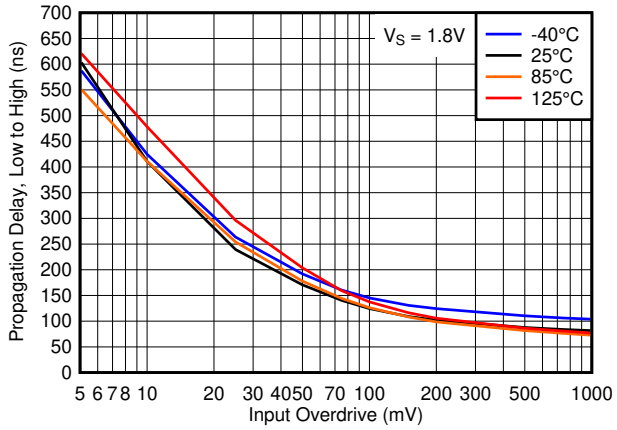


Figure 6-18. Propagation Delay, Low to High, 1.8V

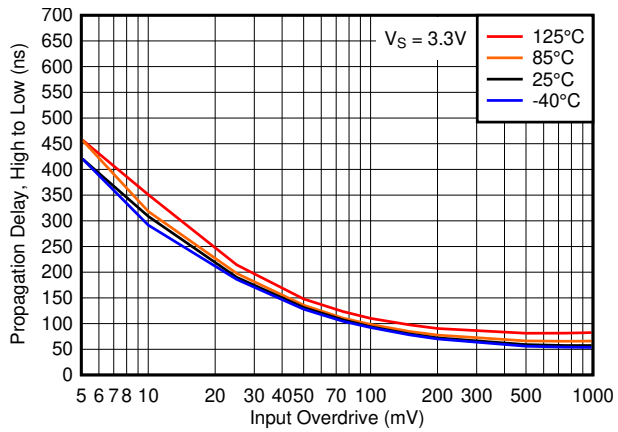


Figure 6-19. Propagation Delay, High to Low, 3.3V

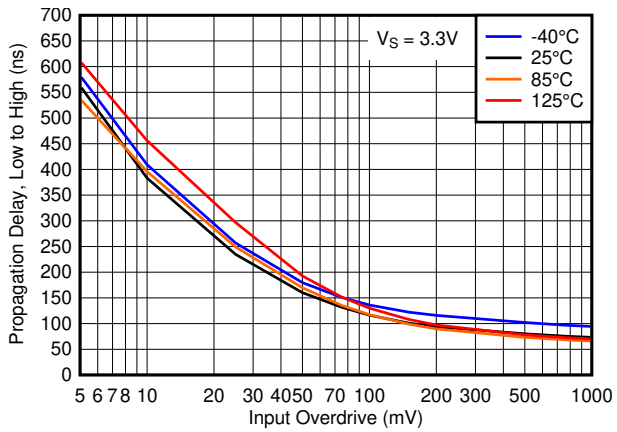


Figure 6-20. Propagation Delay, Low to High, 3.3V

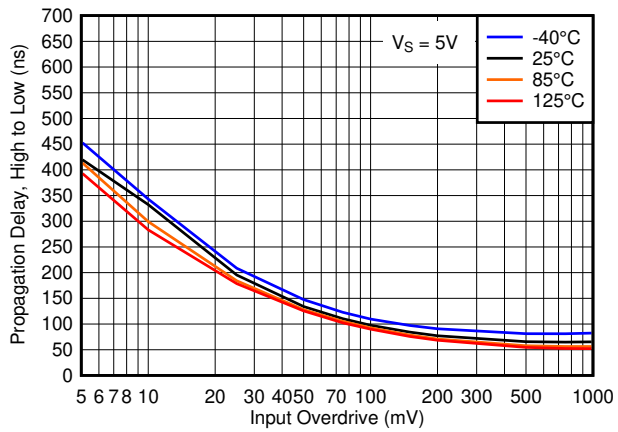


Figure 6-21. Propagation Delay, High to Low, 5V

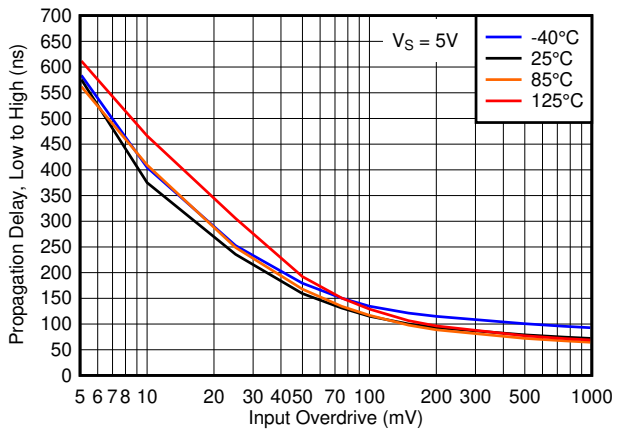


Figure 6-22. Propagation Delay, Low to High, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

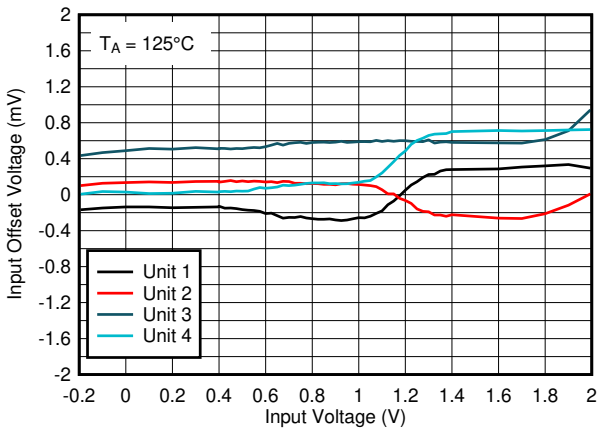


Figure 6-23. Offset Voltage vs. Input Votlage at 125°C, 1.8V

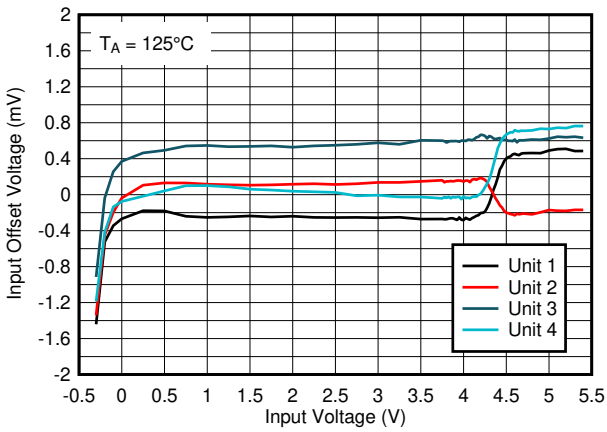


Figure 6-24. Offset Voltage vs. Input Votlage at 125°C, 5V

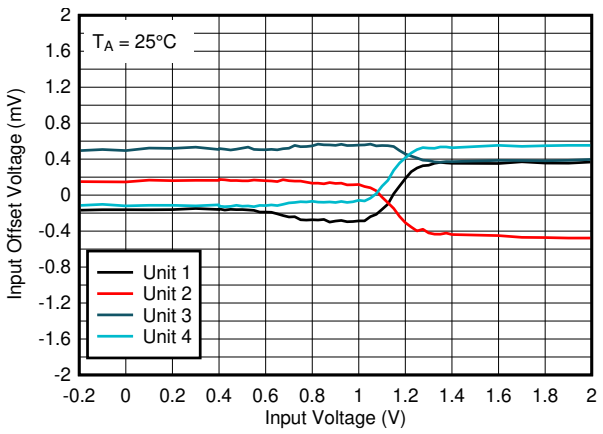


Figure 6-25. Offset Voltage vs. Input Votlage at 25°C, 1.8V

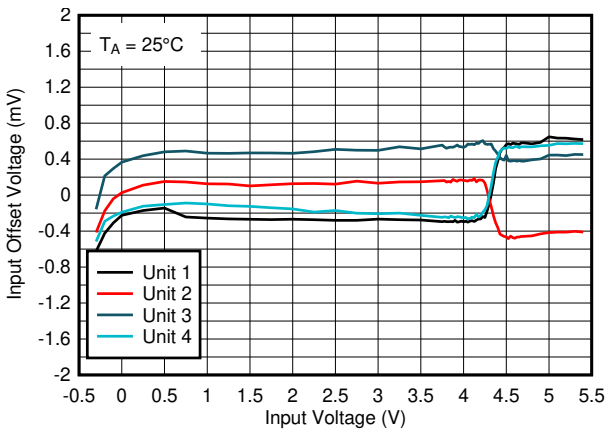


Figure 6-26. Offset Voltage vs. Input Votlage at 25°C, 5V

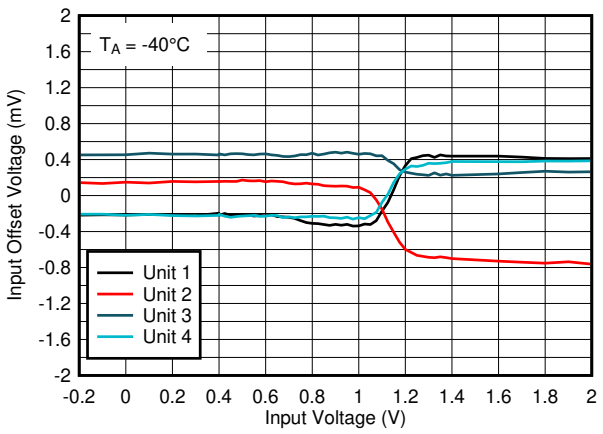


Figure 6-27. Offset Voltage vs. Input Votlage at -40°C, 1.8V

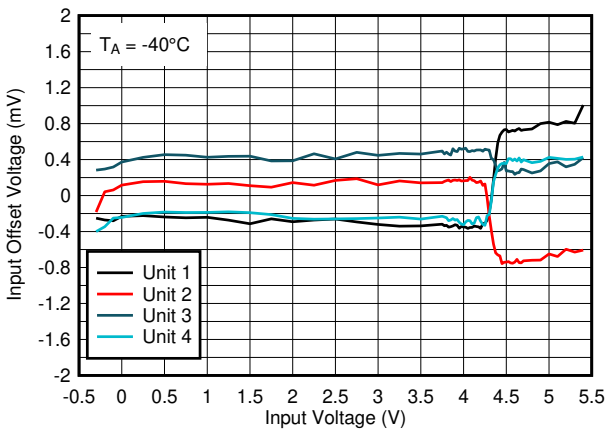


Figure 6-28. Offset Voltage vs. Input Votlage at -40°C, 5V

6.10 Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 2.5k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

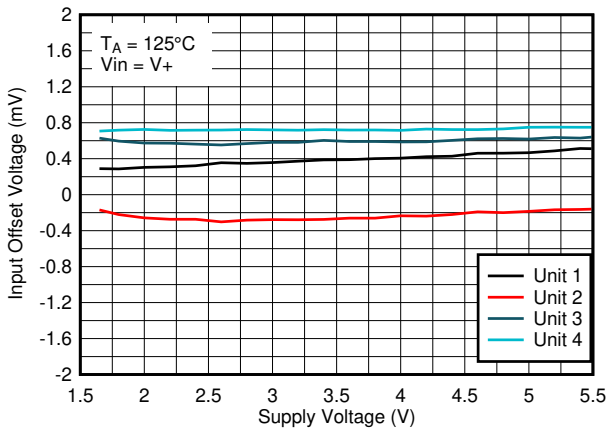


Figure 6-29. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V+

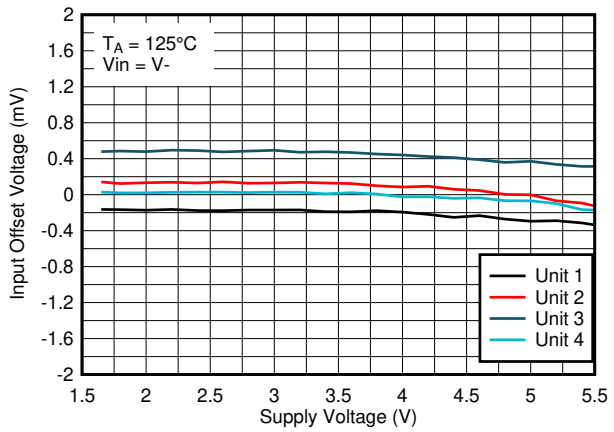


Figure 6-30. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V-

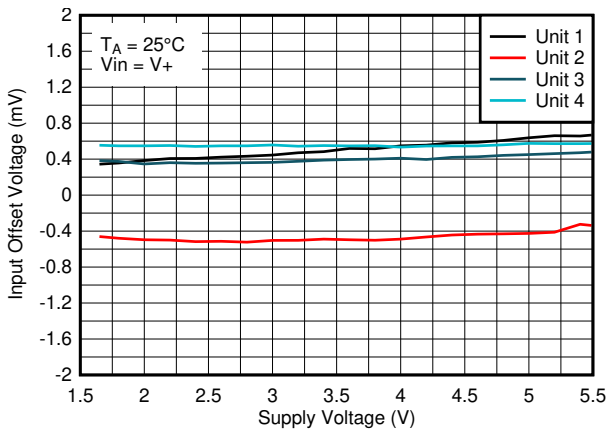


Figure 6-31. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V+

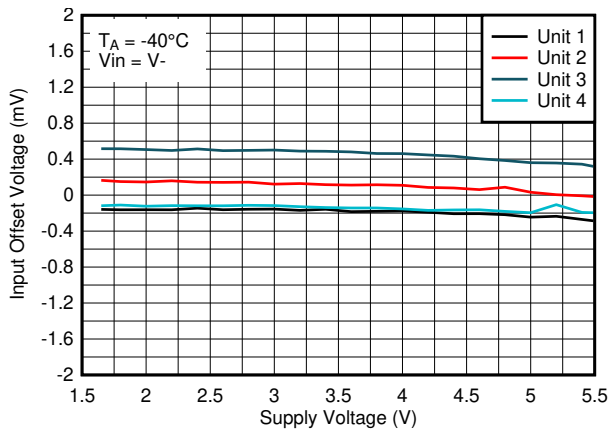


Figure 6-32. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V-

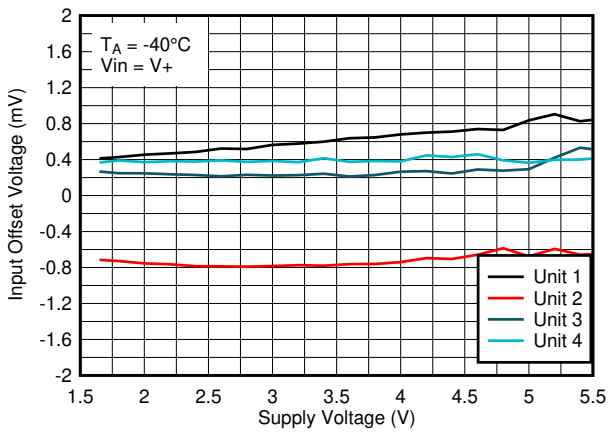


Figure 6-33. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V+

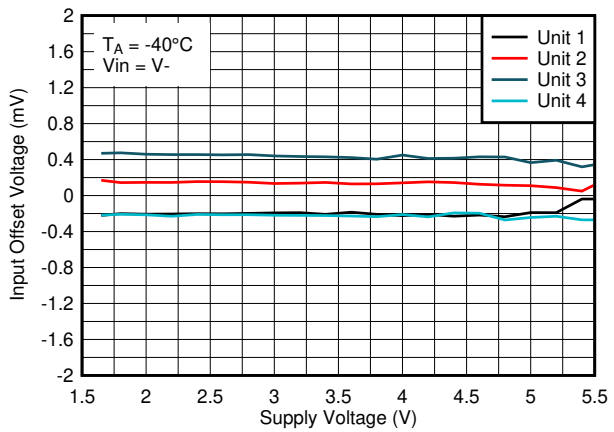


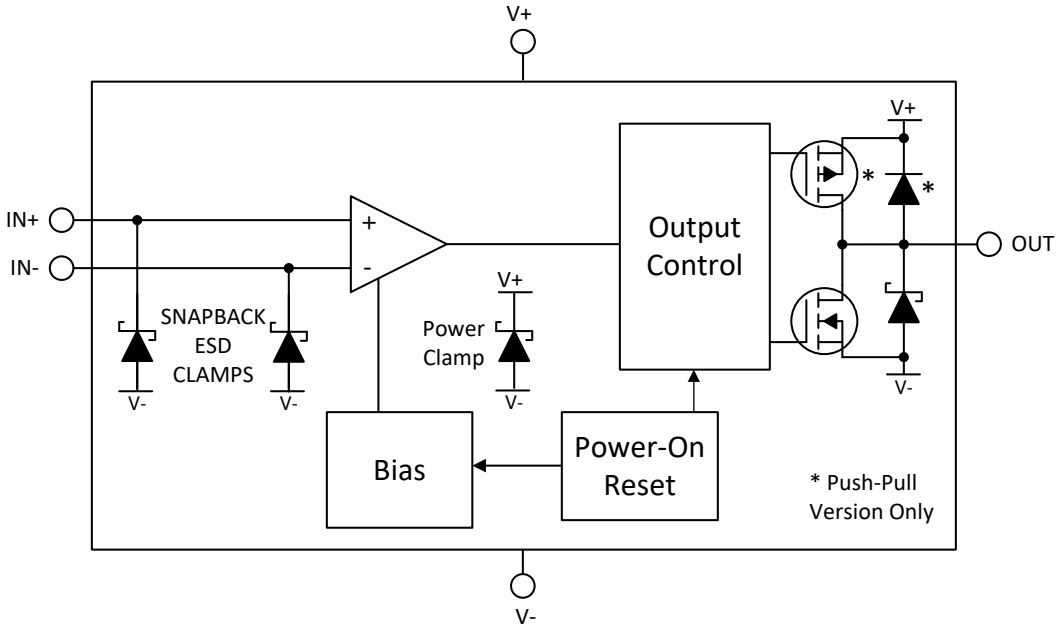
Figure 6-34. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V-

7 Detailed Description

7.1 Overview

The TLV902x-Q1 and TLV903x-Q1 devices are dual-channel, micro-power comparators with push-pull and open-drain outputs and low input offset voltage. Operating down to 1.65 V while only consuming only 16 µA per channel, the TLV902x-Q1 and TLV903x-Q1 are ideally suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down while fail-safe inputs can tolerate input transients without damage or false outputs.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV902x-Q1 (open-drain output) and TLV903x-Q1 (push-pull output) devices are micro-power comparators that have low input offset voltages and are capable of operating at low voltages. The TLV90xx-Q1 family feature a rail-to-rail input stage capable of operating up to 200 mV beyond the power supply rails. The comparators also feature push-pull and open-drain output stage options and Power-on Reset for known start-up conditions.

7.4 Device Functional Modes

7.4.1 Outputs

7.4.1.1 TLV9022-Q1 and TLV9024-Q1 Open Drain Output

The TLV902x-Q1 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 5.5 V, independent of the comparator supply voltage (V_S). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime will be dependant on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) will create an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs must be left floating, or can be tied to the V- pin if floating pins are not allowed. While an individual output can typically sink up to 125 mA, the total combined current for all channels must be less than 200 mA.

7.4.1.2 TLV9032-Q1 and TLV9034-Q1 Push-Pull Output

The TLV903x-Q1 features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output. While an individual output can typically sink and source up to 100mA, the total combined current for all channels must be less than 200 mA.

7.4.2 Power-On Reset (POR)

The TLV90xx-Q1 has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V_s) is ramping up or ramping down, the POR circuitry will be activated for up to 30µs after the minimum supply voltage threshold of 1.5V is crossed, or immediately when the supply voltage drops below 1.5V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit will keep the output high impedance (HI-Z) during the POR period (t_{on}).

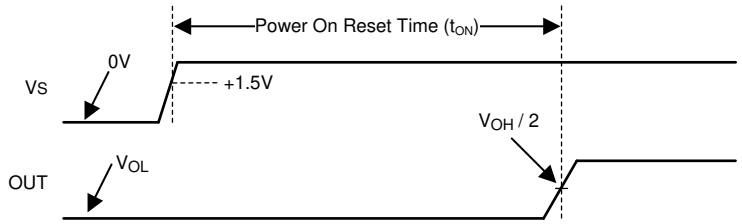


Figure 7-1. Power-On Reset Timing Diagram

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

For the TL903x-Q1 push-pull output devices, the output is "floating" during the POR period. A light pull-up (to V+) or pull-down (to V-) resistor can be used to pre-bias the output condition to prevent the output from floating. If output high is the desired start-up condition, then use the open collector TL902x-Q1, since a pull-up resistor is already required.

7.4.3 Inputs

7.4.3.1 Rail to Rail Input

The TLV90xx-Q1 input voltage range extends from 200mV below V- to 200 mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V+ or V-.

7.4.3.2 Fault Tolerant Inputs

The TLV90xx-Q1 inputs are fault tolerant up to 5.5V independent of V_S. Fault tolerant is defined as maintaining the same high input impedance when V_S is unpowered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0 V and 5.5 V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.

2. When IN- is outside the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain datasheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

7.4.3.3 Input Protection

The input bias current is typically 5 pA for input voltages between V+ and V-. The comparator inputs are protected from reverse voltage by the internal ESD diodes connected to V-. As the input voltage goes under V-, or above the input Absolute Maximum ratings the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for each 10°C temperature increase.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.4 ESD Protection

The TLV90xx-Q1 family incorporates internal ESD protection circuits on all pins. The inputs, and the open-drain output, use a proprietary "snapback" type ESD clamp from each pin to V-, which allows the pins to exceed the supply voltage (V+). While shown as Zener diodes, snapback "short" and go low impedance (like an SCR) when the threshold is exceeded, as opposed to clamping to a defined voltage like a Zener.

The TLV902x-Q1 open-drain output protection also consists of a ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 5.5V.

The TLV903x-Q1 push-pull output protection consists of a ESD clamp between the output and V-, but also includes a ESD diode clamp to V+, as the output must not exceed the supply rails.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents must the clamps conduct. The current must be limited 10 mA or less. This series resistance can be part of any resistive input dividers or networks. TI does not specify the performance of the ESD clamps and external clamping must be added if the inputs or output could exceed the maximum ratings as part of normal operation.

7.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ as long as the input is directly connected to the V+ pin to avoid transients).

7.4.6 Hysteresis

The TLV90xx-Q1 family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" (oscillate) when the absolute differential voltage near zero as the comparator triggers on it's own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 8.1.2 in the following section.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 8-1 and is measured from the mid-point of the input to the midpoint of the output.

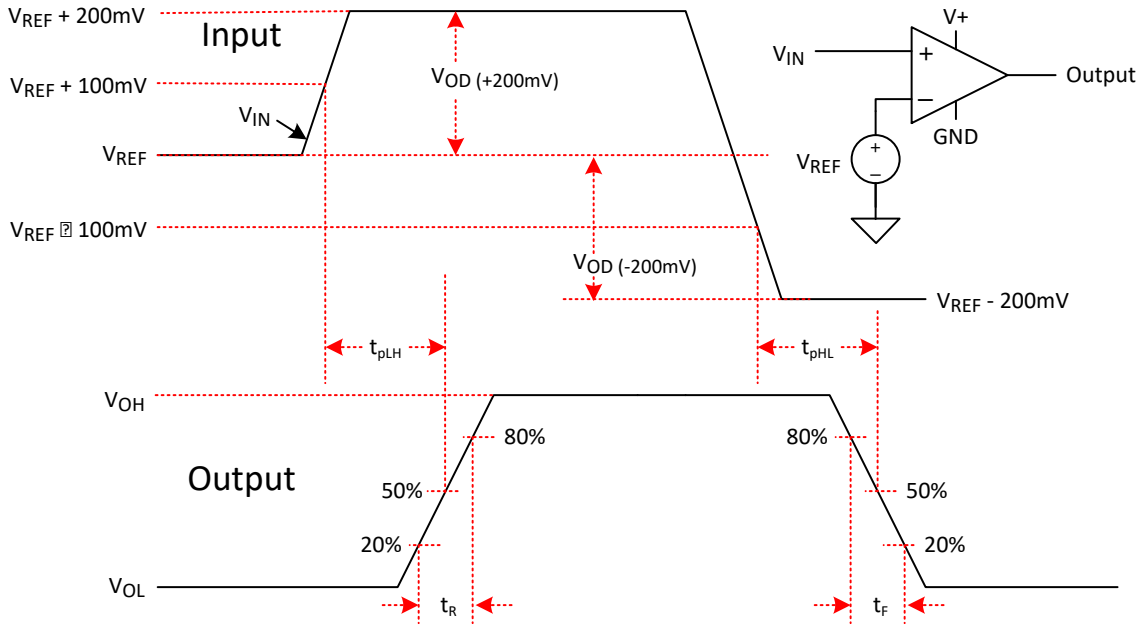


Figure 8-1. Comparator Timing Diagram

8.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 8-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

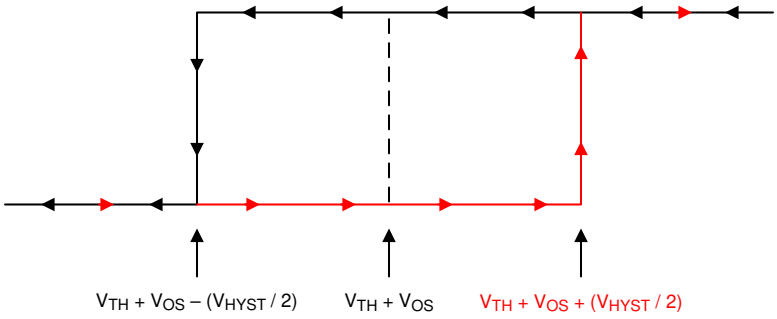


Figure 8-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V+), as shown in Figure 8-3.

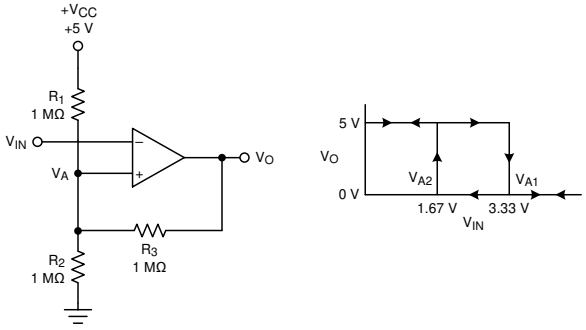


Figure 8-3. TLV903x-Q1in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-3.

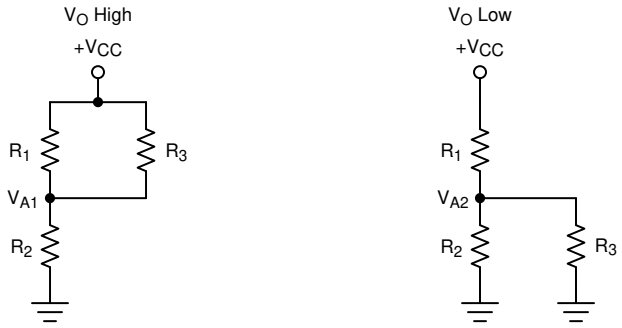


Figure 8-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 8-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

8.1.2.2 Non-Inverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-5,

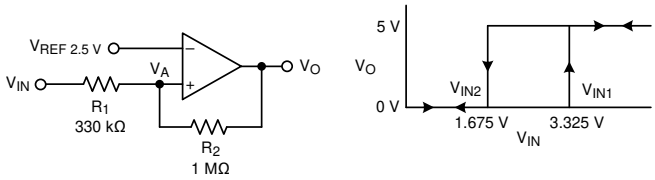


Figure 8-5. TLV903x-Q1 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-6.

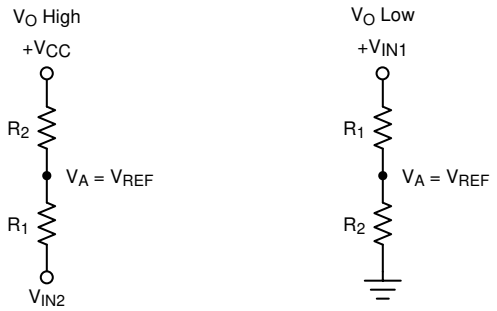


Figure 8-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV902x-Q1, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV902x-Q1) if the outputs are directly connected together.

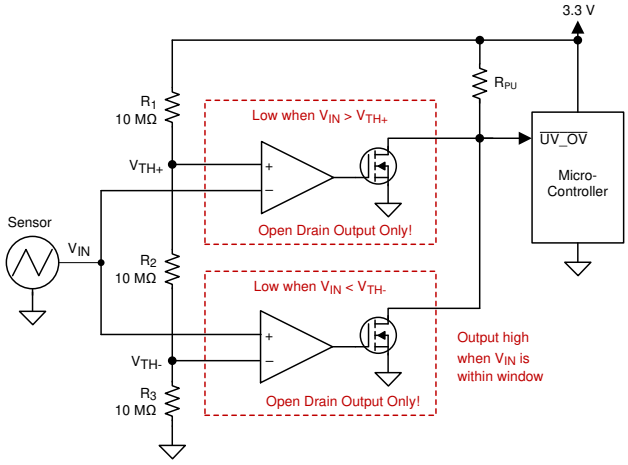


Figure 8-7. Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 8-7. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in Figure 8-8.

8.2.1.3 Application Curve

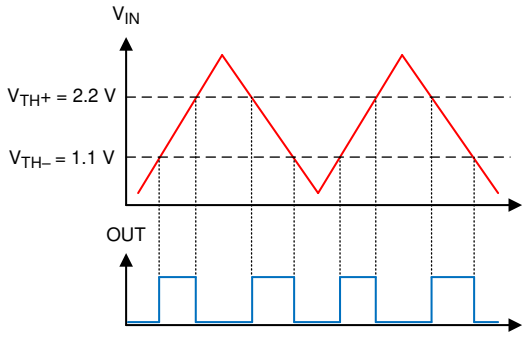


Figure 8-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV903x-Q1) is recommended for best symmetry.

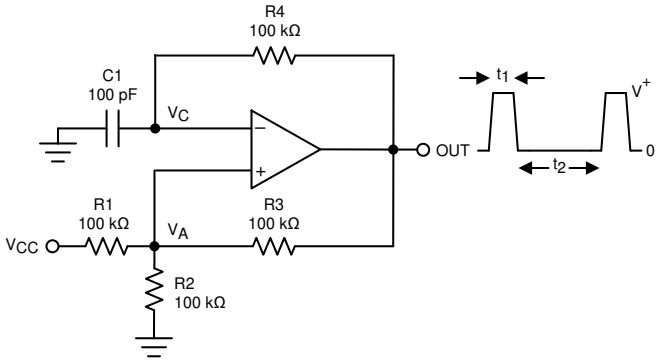


Figure 8-9. Square-Wave Oscillator

8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. R4 must be over several kilo-ohms to minimize loading the output.

8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

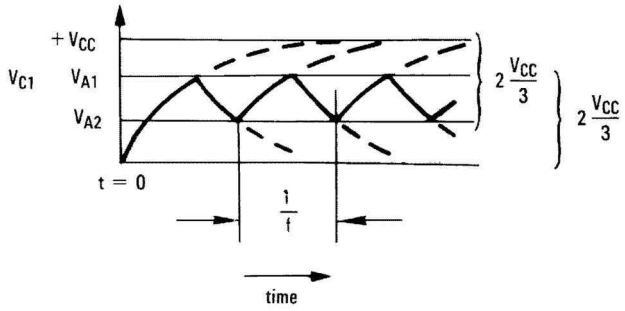


Figure 8-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 8-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2\ R_4C_1 \times \ln 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times In2) \quad (9)$$

8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10 pF

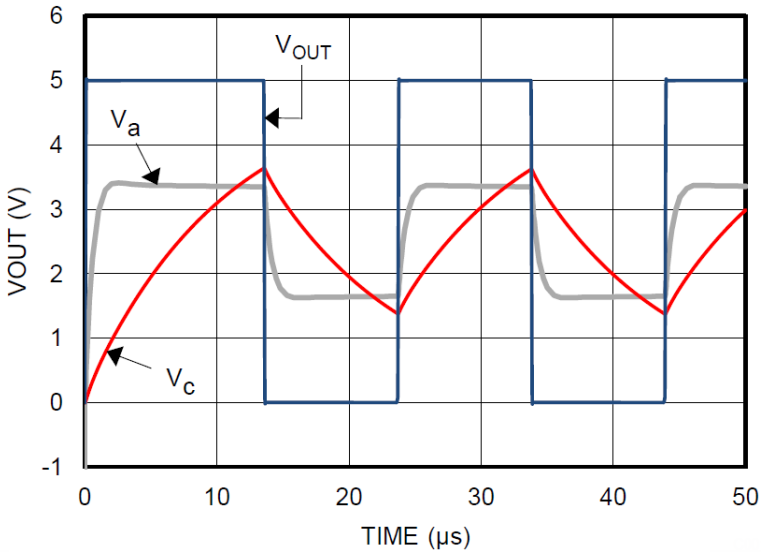


Figure 8-11. Square-Wave Oscillator Output Waveform

8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

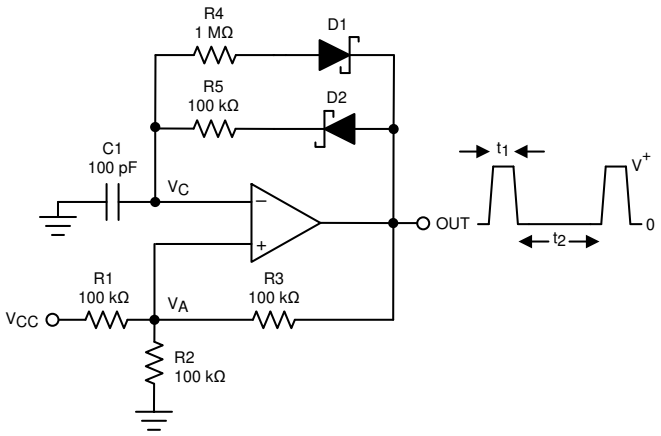


Figure 8-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

8.2.4 Time Delay Generator

The circuit shown in Figure 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

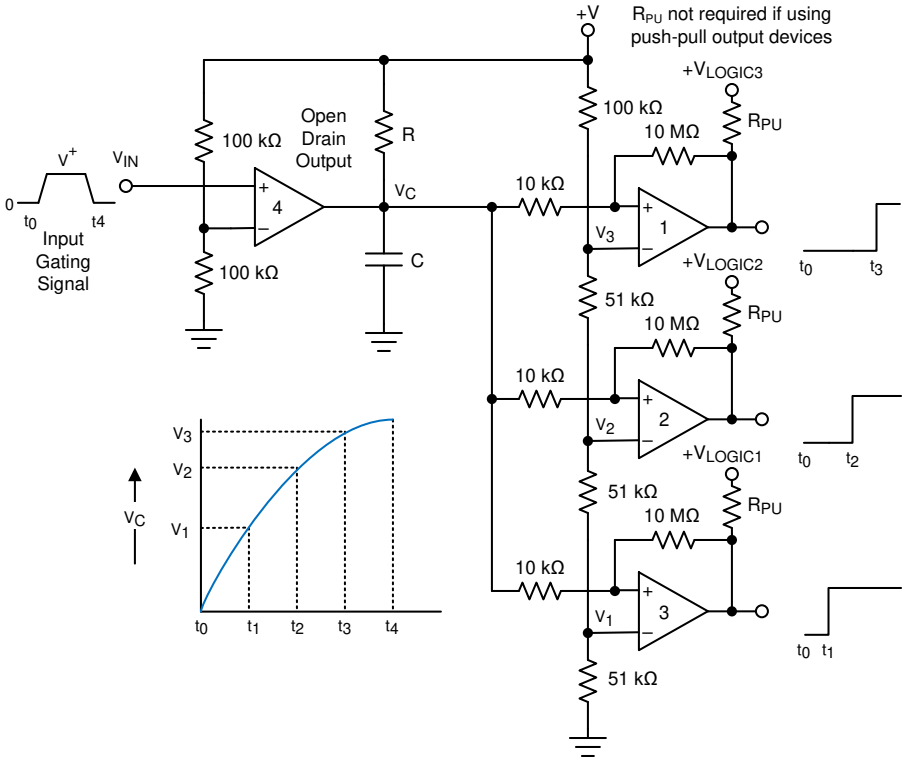


Figure 8-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 swtich to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10 kΩ and 10 MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100 kΩ and C = 0.01 µF to 1 µF.

All outputs will immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV902x-Q1), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

8.2.5 Logic Level Shifter

The output of the TLV902x-Q1 is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

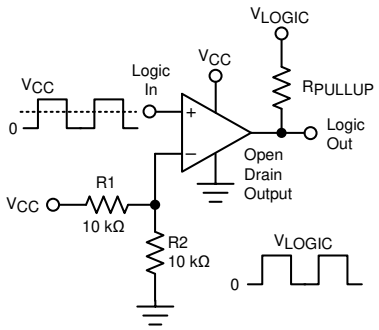


Figure 8-14. Universal Logic Level Shifter

The two 10 kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage must match the driven logic input "high" level.

8.2.6 One-Shot Multivibrator

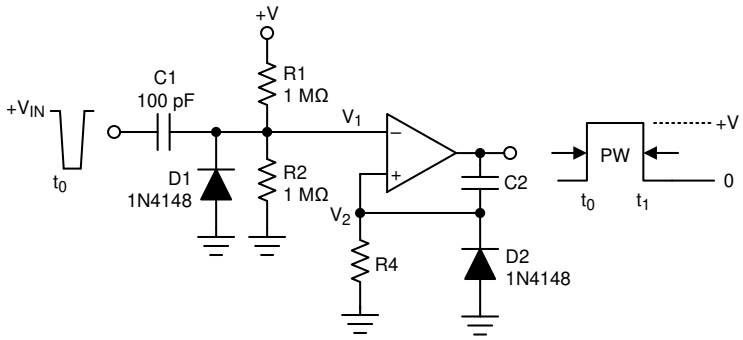


Figure 8-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

8.2.7 Bi-Stable Multivibrator

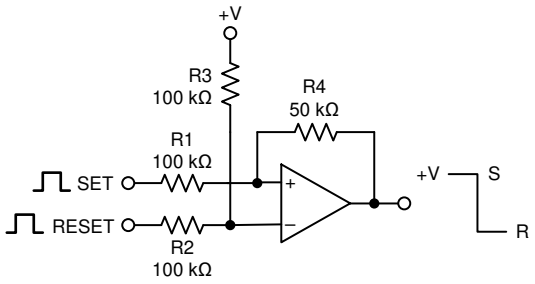


Figure 8-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

8.2.8 Zero Crossing Detector

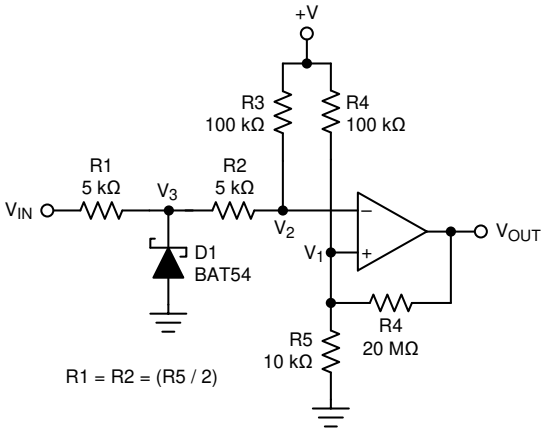


Figure 8-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The noninverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing V_{REF} average voltage.

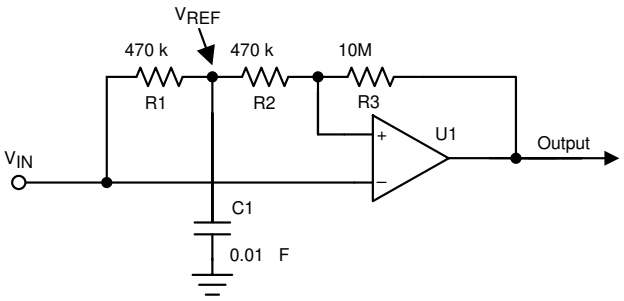


Figure 8-18. Pulse Slicer using TLV903x-Q1

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

The TLV902x-Q1 may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

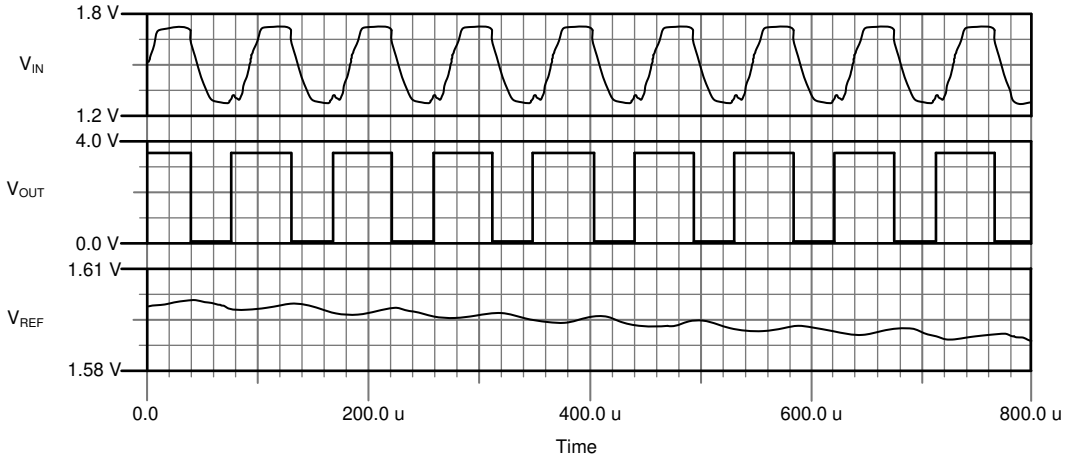


Figure 8-19. Pulse Slicer Waveforms

8.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from either "split" supplies (V+, V- & GND), or a "single" supply (V+ and GND), with GND applied to the V- pin.

Input signals must stay within the specified input range (between V+ and V-) for either type.

Note that on "split" supplies, the ouptut will now swing "low" (V_{OL}) to V- potential and not GND.

9 Layout

9.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

9.2 Layout Example

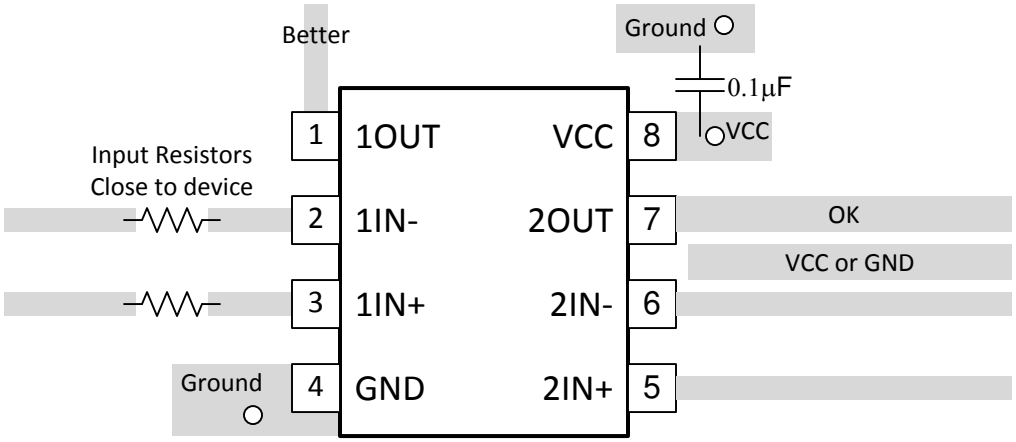


Figure 9-1. Dual Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

PWM generator circuit - SBOA212

How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41

A Quad of Independently Func Comparators - SNOA654

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9032QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TLV9022QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H3FQ	Samples
TLV9022QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IFTQ	Samples
TLV9022QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TQ022Q	Samples
TLV9022QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9022Q	Samples
TLV9024QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9024Q	Samples
TLV9032QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H2FQ	Samples
TLV9032QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IGTQ	Samples
TLV9032QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9032Q	Samples
TLV9032QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9032Q	Samples
TLV9034QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9034Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV9022-Q1, TLV9024-Q1, TLV9032-Q1, TLV9034-Q1 :

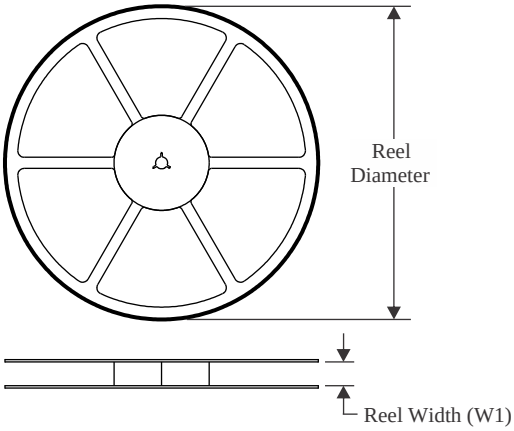
- Catalog : TLV9022, TLV9024, TLV9032, TLV9034

NOTE: Qualified Version Definitions:

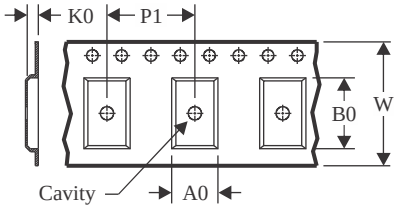
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

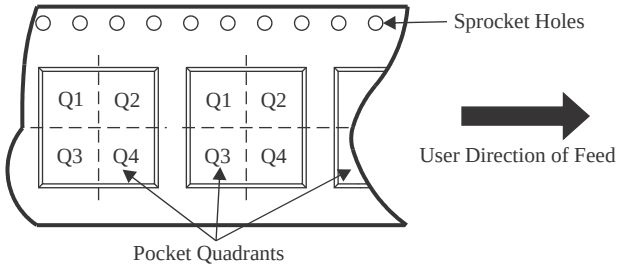


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

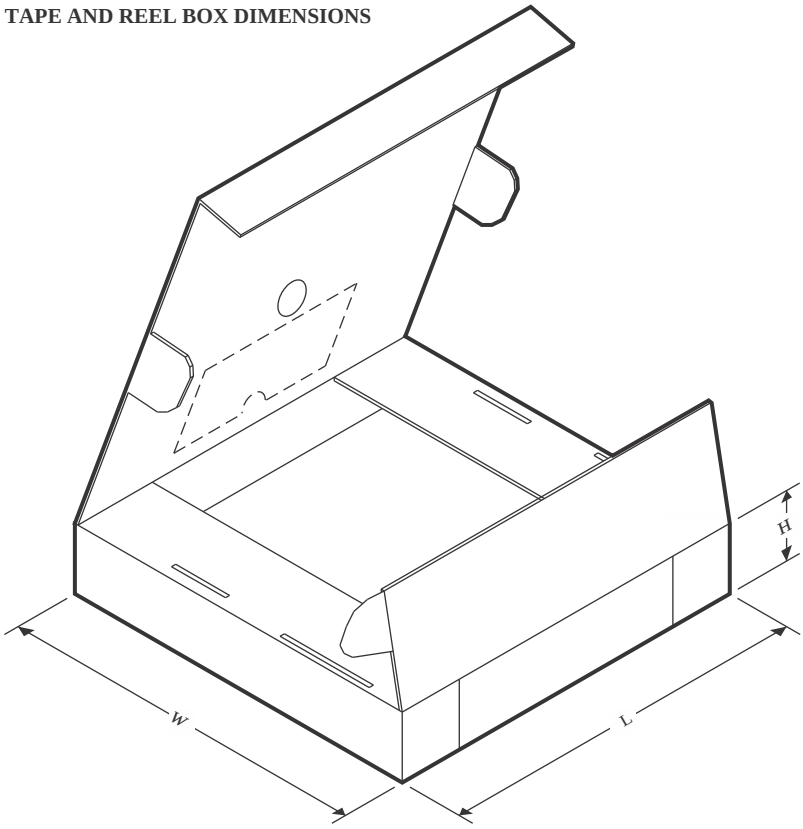
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9022QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9022QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9022QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9024QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9032QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9032QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9032QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9034QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

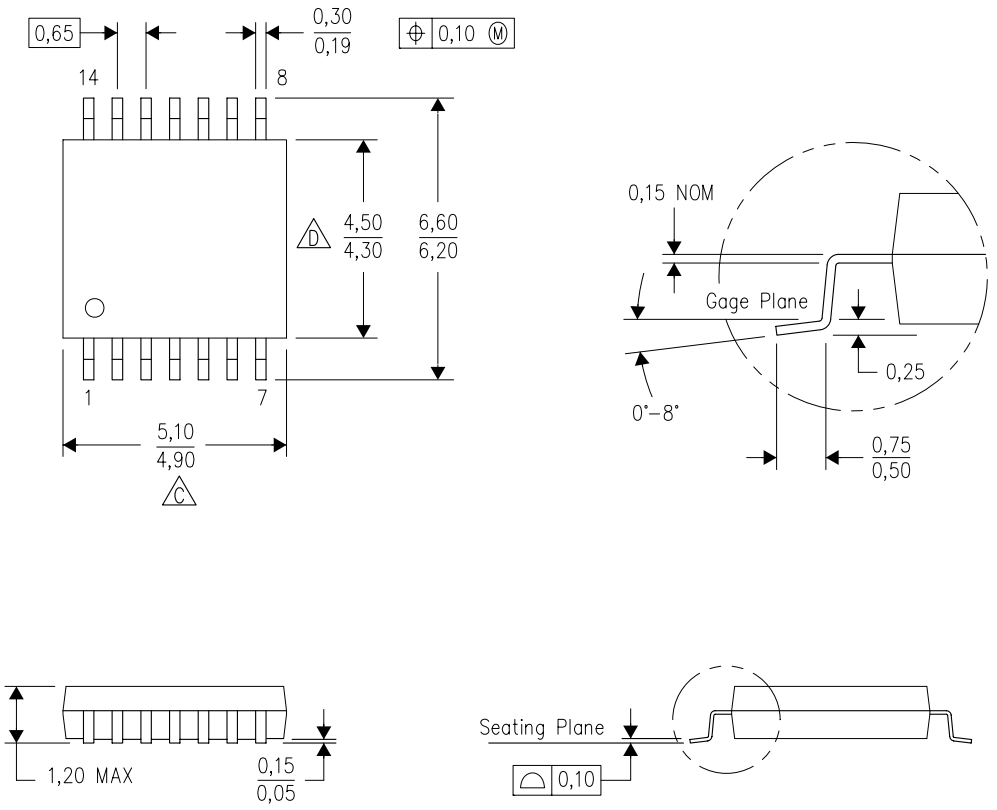
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9022QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9022QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9022QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV9024QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV9032QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9032QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9032QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV9034QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

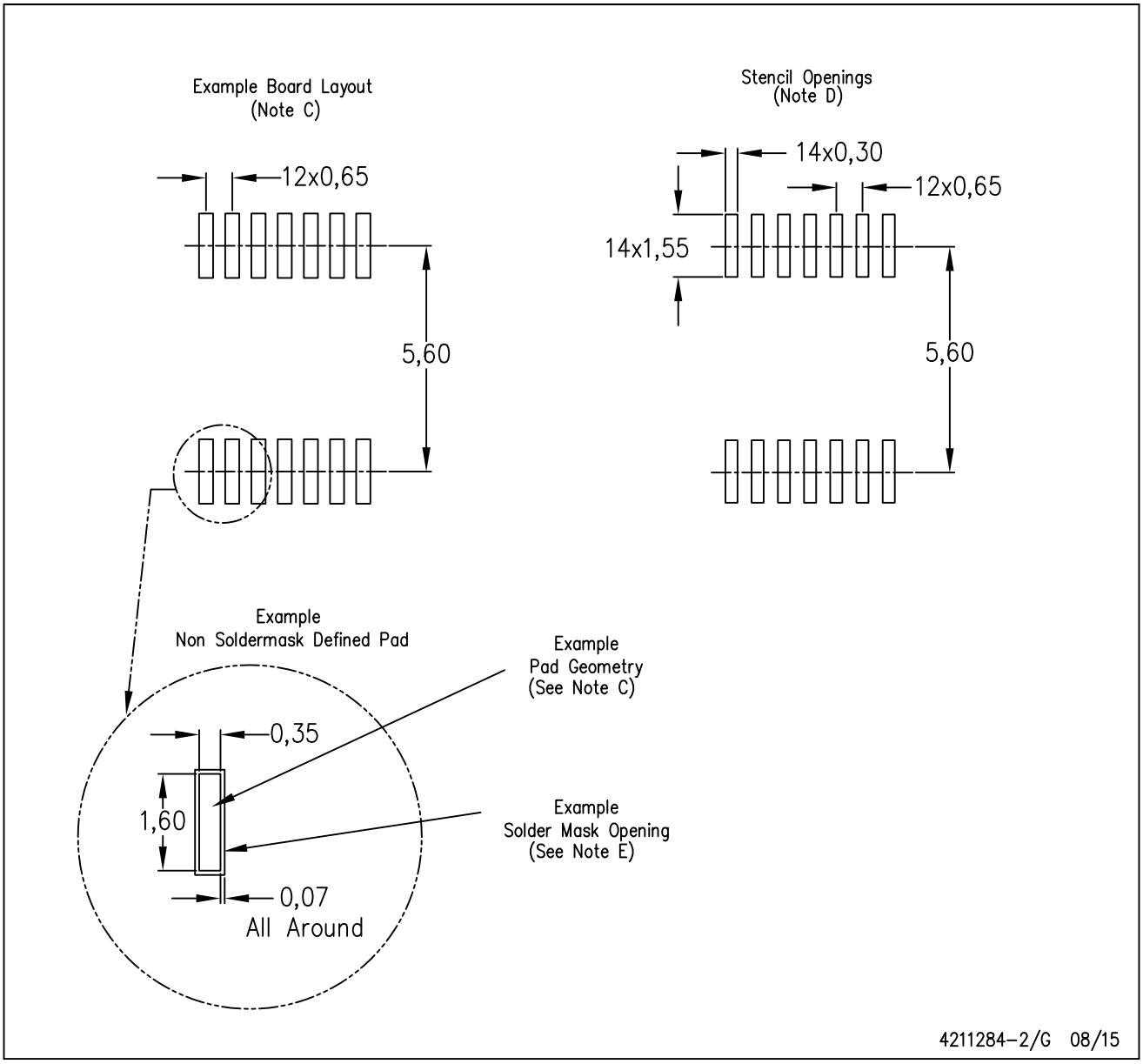
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



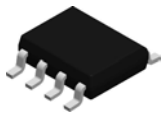
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

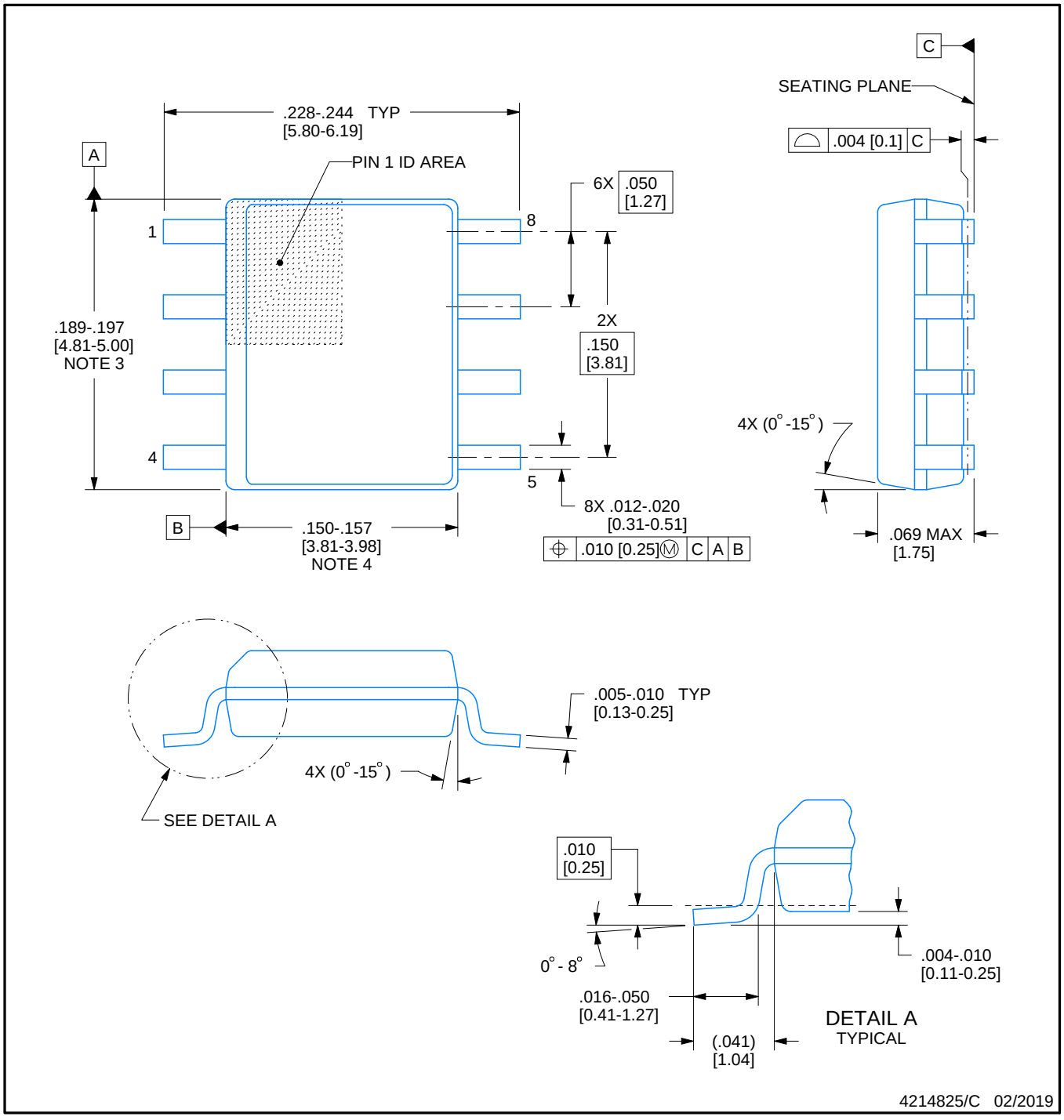


PACKAGE OUTLINE

D0008A

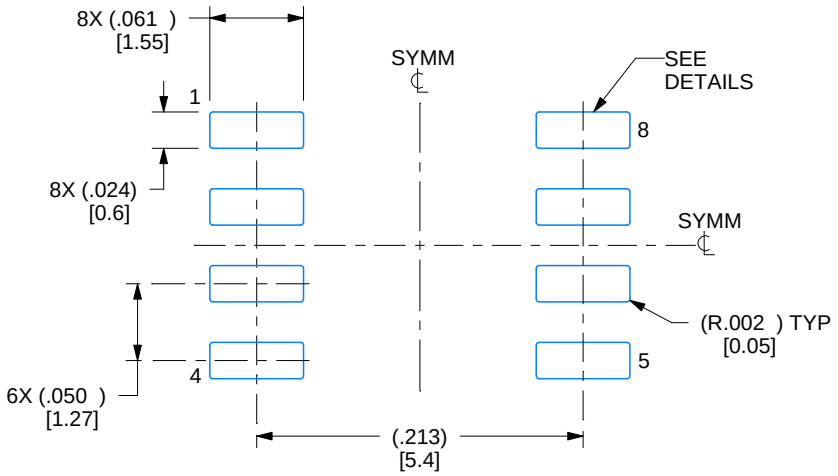
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

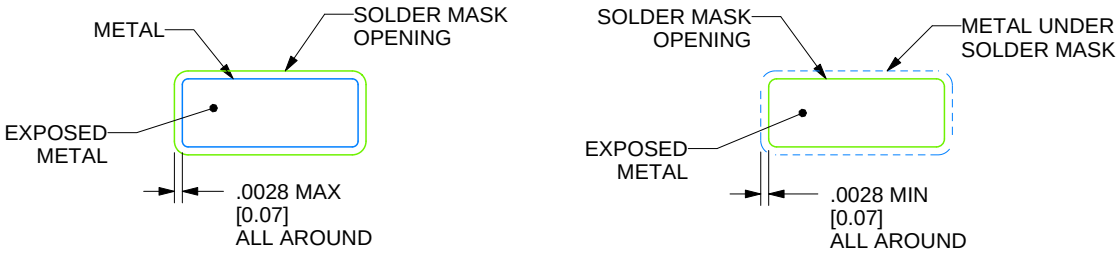


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

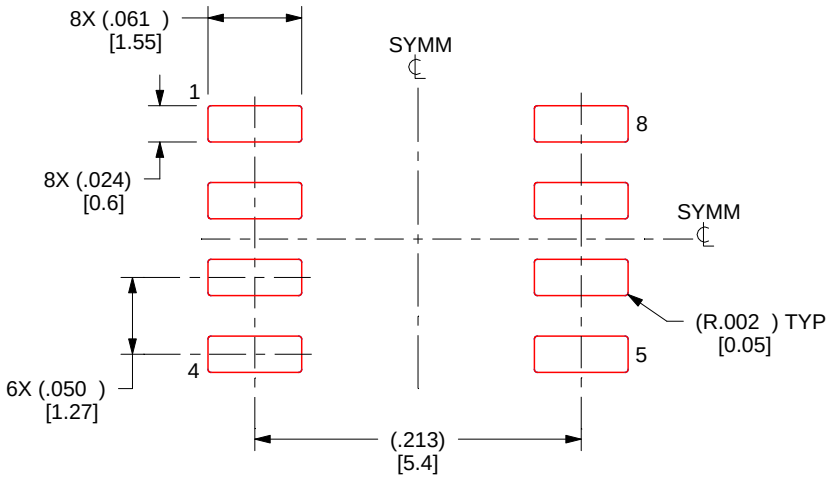
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



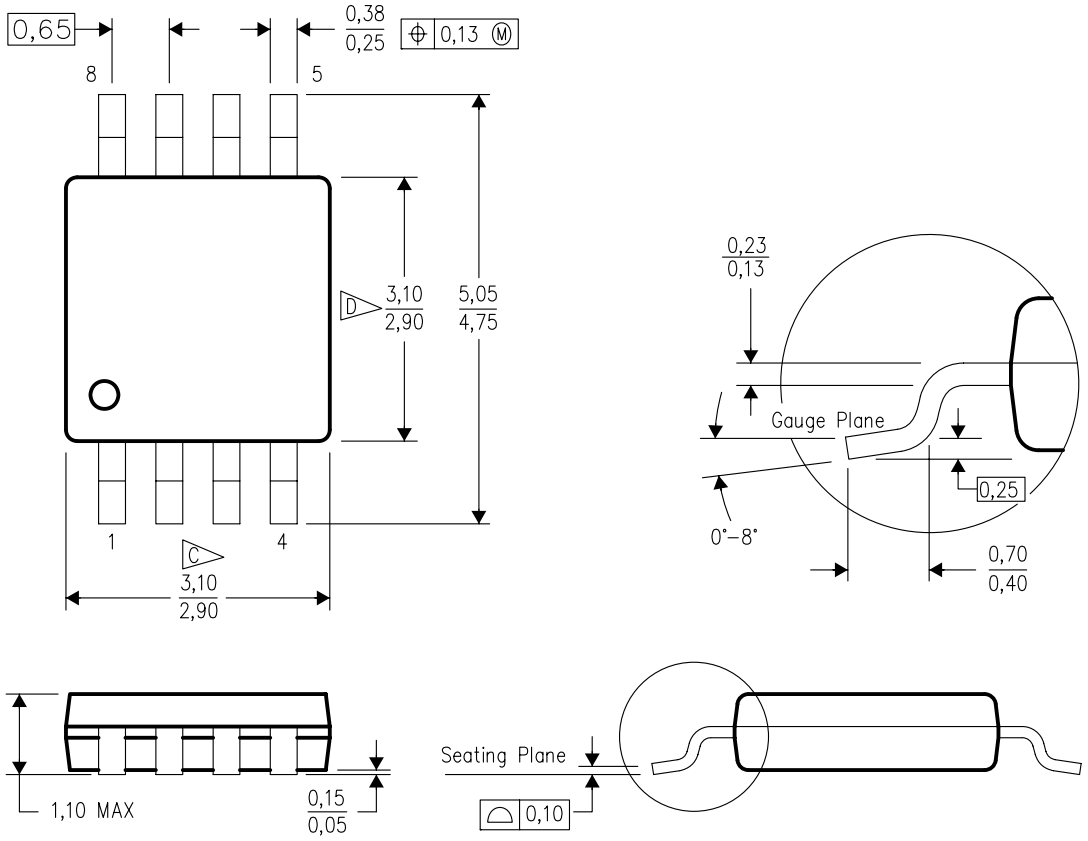
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

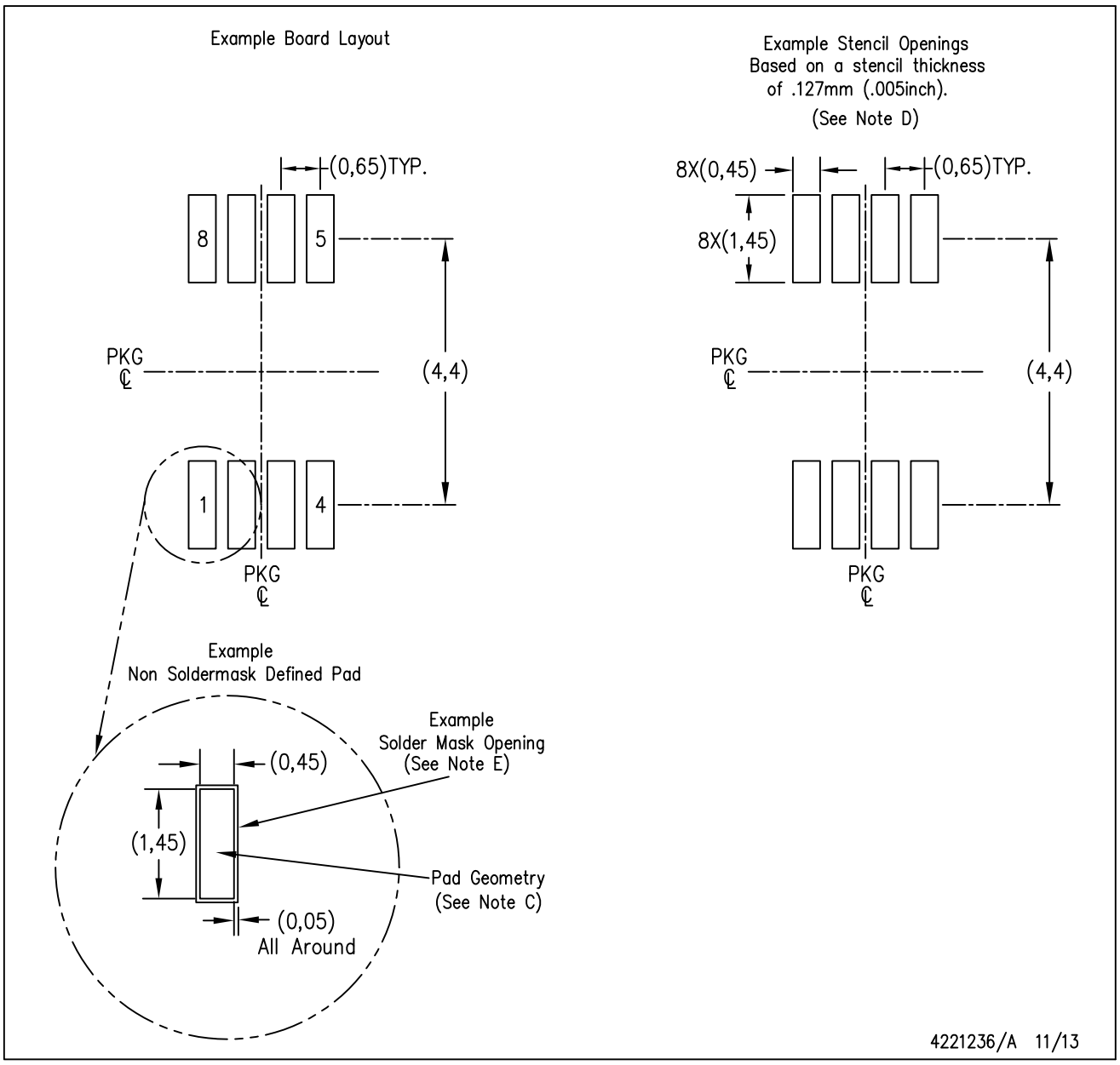
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



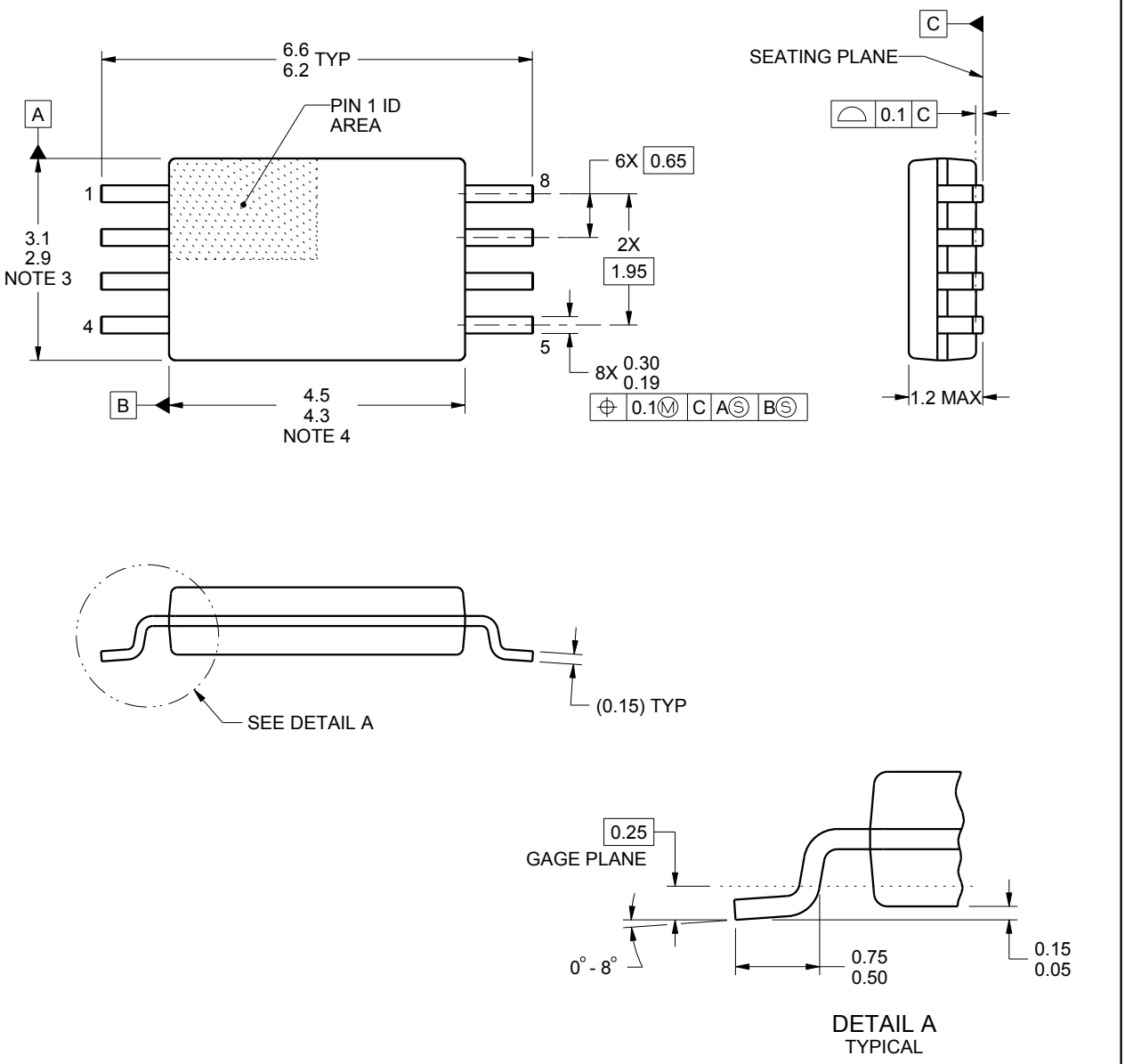
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

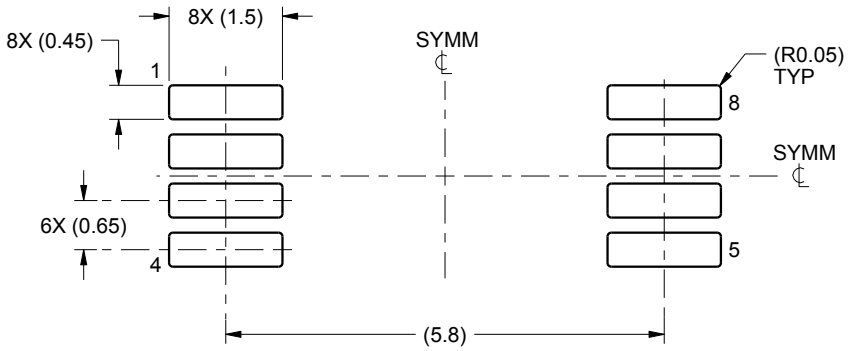
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

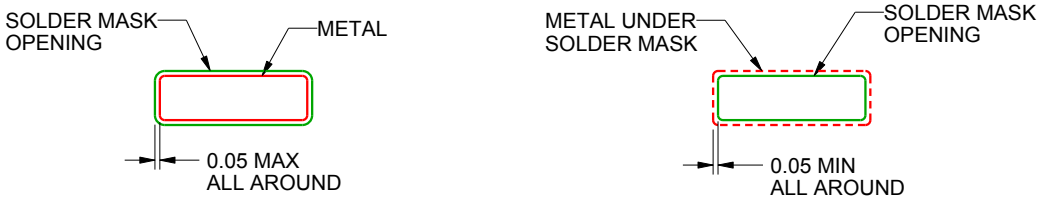


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

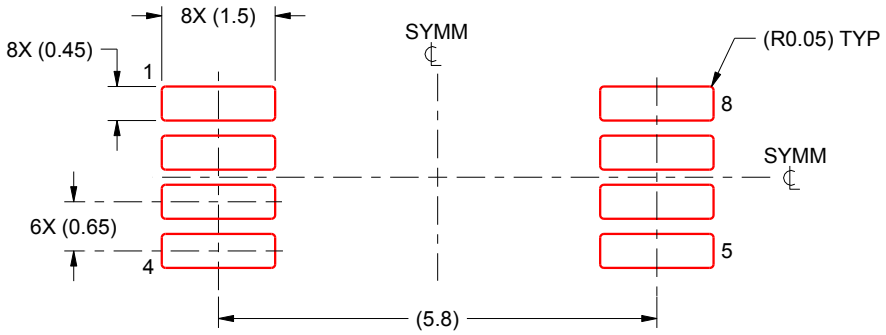


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

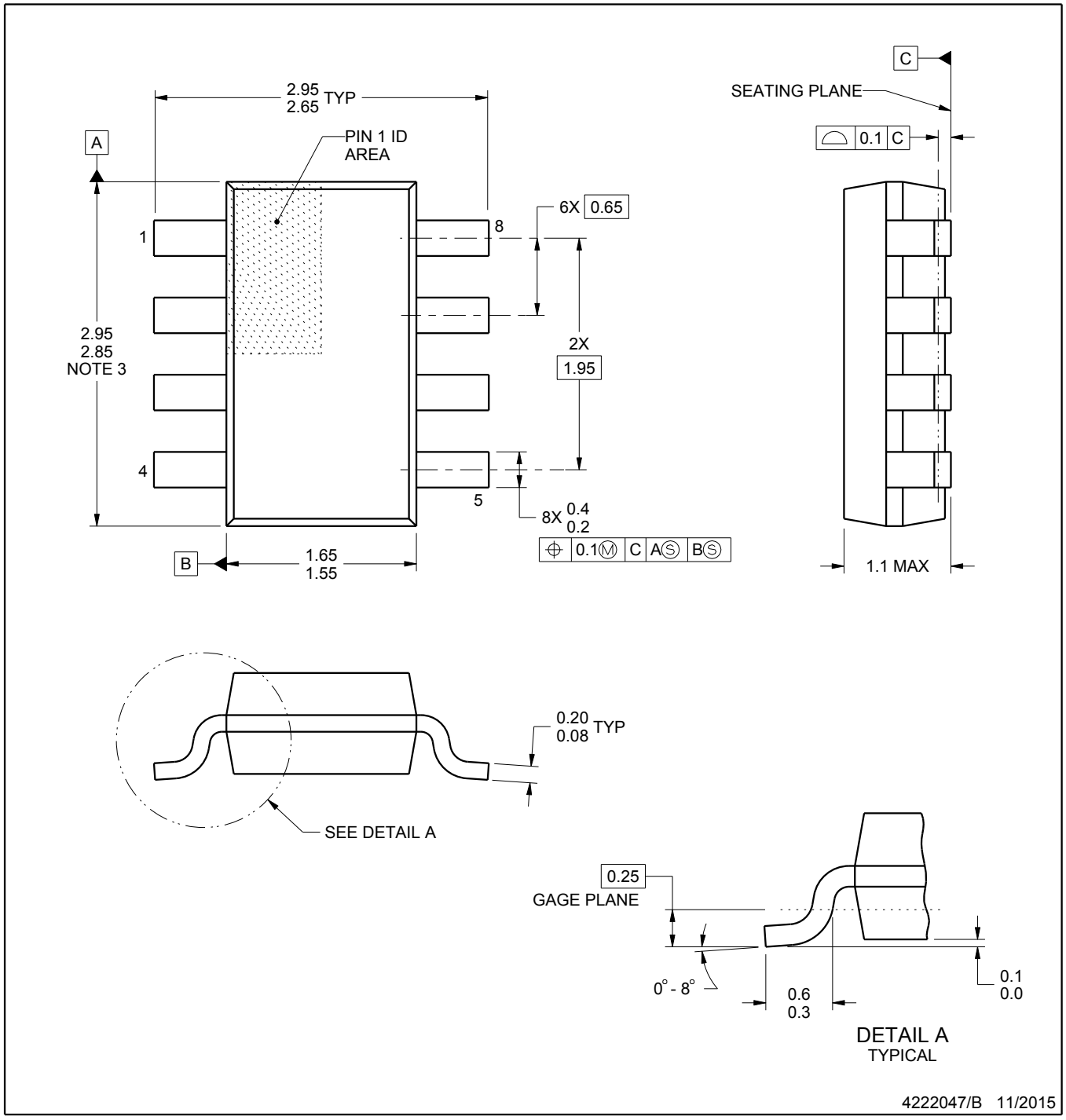
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

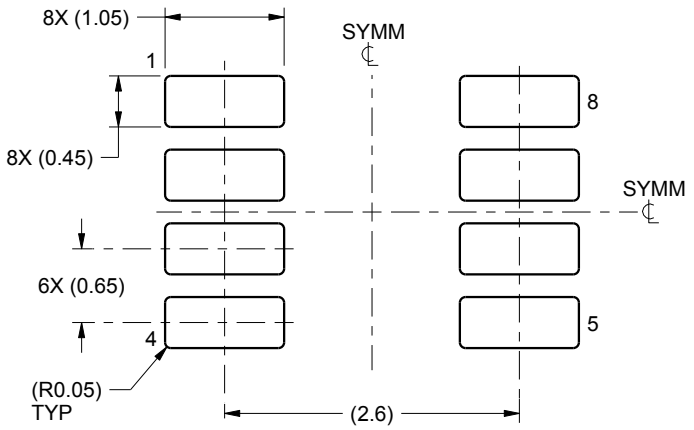
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

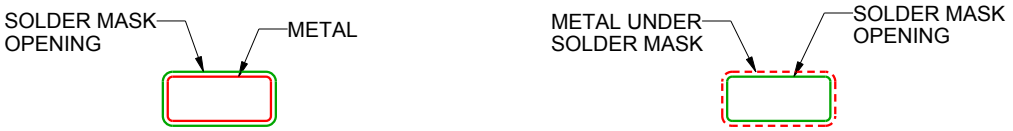


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

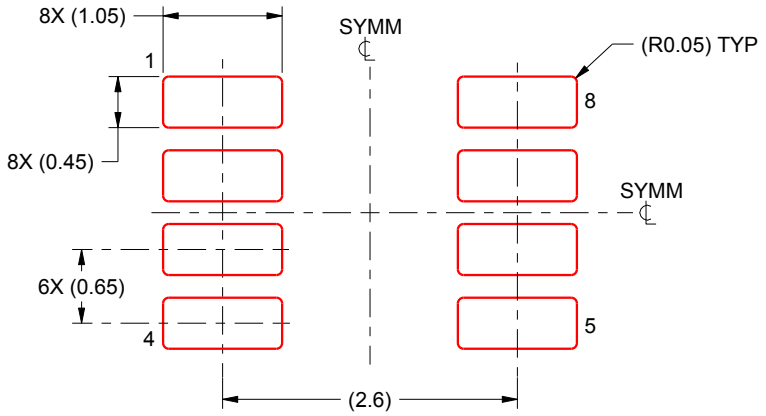
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TLVM13620
SLVSGL2 – APRIL 2022

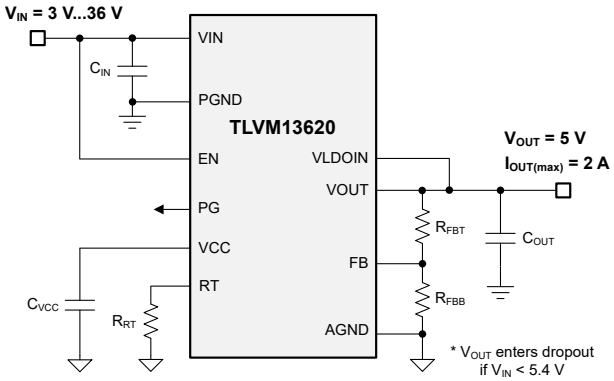
TLVM13620 High-Density, 3-V to 36-V Input, 1-V to 6-V Output, 2-A Power Module With Enhanced HotRod™ QFN Package

1 Features

- Versatile synchronous buck DC/DC module
  - Integrated MOSFETs, inductor, and controller
  - Wide input voltage range of 3 V to 36 V
  - Adjustable output voltage from 1 V to 6 V with 1% setpoint accuracy over temperature
  - 4-mm × 6-mm × 1.8-mm overmolded package
  - –40°C to 125°C junction temperature range
  - Frequency adjustable from 200 kHz to 2.2 MHz
  - Negative output voltage capability
- Ultra-high efficiency across the full load range
  - 93% peak efficiency at 12 V_{IN}, 5 V_{OUT}, 1 MHz
  - External bias option for improved efficiency
  - Shutdown quiescent current of 0.6 µA (typical)
  - 0.3-V typical dropout voltage at 2-A load
- Ultra-low conducted and radiated EMI signatures
  - Low-noise package with dual input paths and integrated capacitors reduces switch ringing
  - Constant-frequency FPWM mode of operation
  - Meets CISPR 11 and 32 class B emissions
- Suitable for scalable power supplies
  - Pin compatible with the TLVM13630 (36 V, 3 A)
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and V_{IN} UVLO
  - Hiccup-mode overcurrent protection
  - Thermal shutdown protection with hysteresis
- Create a custom design using the TLVM13620 with the WEBENCH® Power Designer

2 Applications

- Test and measurement, aerospace and defense
- Factory automation and control
- Buckand inverting buck-boost power supplies



Typical Schematic

3 Description

The TLVM13620 synchronous buck power module is a highly integrated 36-V, 2-A DC/DC solution that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

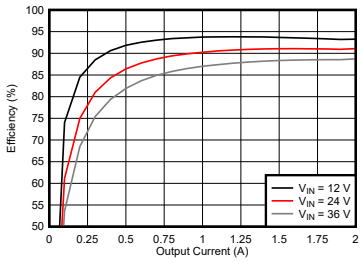
With an output voltage range from 1 V to 6 V, the TLVM13620 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total solution requires as few as four external components and eliminates the magnetics and compensation part selection from the design process.

Although designed for small size and simplicity in space-constrained applications, the TLVM13620 module offers many features for robust performance: precision enable with hysteresis for adjustable input-voltage UVLO, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, negative output voltage capability for inverting applications, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TLVM13620	B0QFN (30)	4.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Efficiency, V_{OUT} = 5 V, f_{SW} = 1 MHz

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2022	*	Initial Release

5 Device Comparison Table

Device	Orderable Part Number	Mode	Spread Spectrum	Output Voltage	External Sync	Junction Temperature
TLVM13620	TLVM13620RDHR	FPWM	No	Adjustable	No	–40°C to 125°C

6 Pin Configuration and Functions

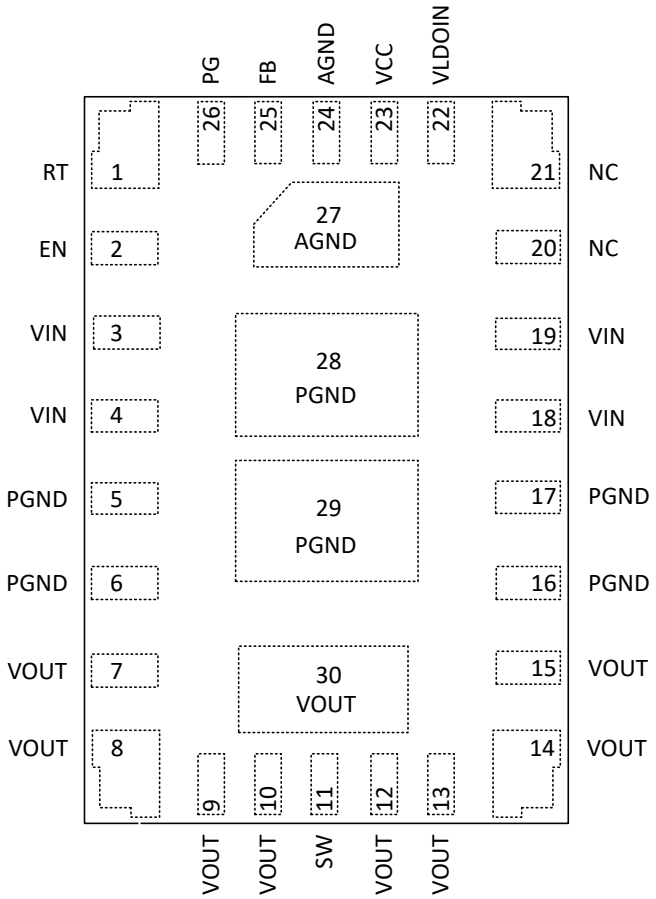


Figure 6-1. 30-Pin QFN, RDH Package (Top View)

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RT	1	I	Frequency setting pin. This analog pin is used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from this pin to AGND. Do not leave open or connect to ground.
EN	2	I	Precision enable input pin. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Place an external voltage divider between this pin, AGND, and VIN to create an external UVLO.
VIN	3, 4, 18, 19	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device. Refer to Section 11.2 for input capacitor placement example.
PGND	5, 6, 16, 17, 28, 29	G	Power ground. This pin is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See Section 11.2 for a recommended layout.
VOUT	7-10, 12–15, 30	P	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
SW	11	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
NC	20, 21	—	No connect. Do not connect these pins to ground, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
VLDOIN	22	P	Optional LDO supply input. Connect to VOUT or to other voltage rail to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. Do not connect to a voltage above 12 V or to a voltage greater than V_{IN}. If unused, connect this pin to ground.
VCC	23	O	Internal LDO output. Used as a supply to the internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF ceramic capacitor from this pin to PGND.
AGND	24, 27	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *This pin must be connected to PGND at a single point.* See Section 11.2 for a recommended layout.
FB	25	I	Feedback input. For the adjustable output version, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. When connecting with a feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See Section 11.2 for a feedback resistor placement.
PG	26	O	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to PGND.

(1) P = Power, G = Ground, I = Input, O = Output, NC = No connect

7 Specifications

7.1 Absolute Maximum Ratings

Limits apply over T_J = –40°C to 125°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND, PGND	–0.3	40	V
	VLDOIN to AGND, PGND	–0.3	16	
	EN to AGND, PGND	–0.3	40	
	RT to AGND, PGND	–0.3	5.5	
	FB to AGND, PGND	–0.3	16	
	PG to AGND, PGND	0	20	
	PGND to AGND	–1	2	
Output voltage	VCC to AGND, PGND	–0.3	5.5	V
	SW to AGND, PGND(2)	–0.3	40	
	VOUT to AGND, PGND	–0.3	6	
Input current	PG	—	10	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C
T_{stg}	Storage temperature	–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)	3		36	V
Input voltage	VLDOIN			12	V
Output voltage	VOUT(1)	1		6	V
Output current	IOUT(2)	0		2	A
Frequency	f_{SW} set by RT	200		2200	kHz
Input current	PG			2	mA
Output voltage	PG	0		16	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature	–40		105	°C

(1) Do not allow the output voltage be allowed to fall below 0 V.
(2) Maximum continuous DC current can be derated when operating with high switching frequency, high ambient temperature, or both. Refer to the *Typical Characteristics* section for details.

7.4 Thermal Information

THERMAL METRIC(1)		RDH (QFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63603 EVM)	29.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	21.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 64-mm × 83-mm four-layer PCB with 2-oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the *Layout* section.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1 mm from the device.

7.5 Electrical Characteristics

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, f_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over I_{OUT} range)	3.95		36	V
		Once operating (over I_{OUT} range)	3		36	V
V_{IN_HYS}	Hysteresis(1)			1.0		V
I_{Q_VIN}	Input operating quiescent current (non-switching)	T_A = 25°C, V_{EN} = 3.3 V, V_{FB} = 1.5 V		4		µA
I_{SDN_VIN}	VIN shutdown quiescent current	V_{EN} = 0 V, T_A = 25°C		3		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			0.91		V
V_{EN_HYS}	EN voltage hysteresis		0.275	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
I_{EN}	Input current into EN (non-switching)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		1.65		µA
t_{EN}	EN HIGH to start of switching delay(1)			0.7		ms
INTERNAL LDO VCC						
V_{CC}	Internal LDO VCC output voltage	3.4 V ≤ V_{LDOIN} ≤ 12.5 V		3.3		V
		V_{LDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{LDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis(2)	Hysteresis below V_{CC_UVLO}		1.1		V
I_{VLDOIN}	Input current into VLDOIN pin (non-switching, maximum at T_A = 125°C)(3)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		25	31.2	µA
FEEDBACK						
V_{OUT}	Adjustable output voltage range	Over the I_{OUT} range	1		6	V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Over the V_{IN} range, V_{OUT} = 1 V, I_{OUT} = 0 A, f_{SW} = 200 kHz	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 3 A		0.1%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4.0 V ≤ V_{IN} ≤ 36 V		0.1%		
I_{FB}	Input current into the FB pin	V_{FB} = 1.0 V		10		nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		2.0	A
I_{OCL}	Output overcurrent (DC) limit threshold			3.8		A
I_{L_HS}	High-side switch current limit	Duty cycle approaches 0%	4.48	4.87	5.32	A
I_{L_LS}	Low-side switch current limit		2.07	2.4	2.80	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time ("hiccup" time before soft start) (1)			80		ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{REF} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if the output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms

7.5 Electrical Characteristics (continued)

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, f_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PG_{OV}	PG upper threshold — rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG lower threshold — falling	% of V_{OUT} setting	92%	94%	96.5%	
PG_{HYS}	PG upper threshold hysteresis (rising and falling)	% of V_{OUT} setting		1.3%		
$V_{IN\_PG\_VALID}$	Input voltage for valid PG output	46-µA pullup, V_{EN} = 0 V	1.0			V
V_{PG_LOW}	Low level PG function output voltage	2-mA pullup to the PG pin, V_{EN} = 3.3 V			0.4	V
I_{PG}	Input current into the PG pin when open-drain output is high	V_{PG} = 3.3 V		10		nA
I_{OV}	Pulldown current at the SW node under overvoltage condition			0.5		mA
$t_{PG\_FLT\_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG\_FLT\_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by R_T or SYNC		200		2200	kHz
f_{SW_RT1}	Default switching frequency by R_T	R_{RT} = 66.5 kΩ	180	200	220	kHz
f_{SW_RT2}	Default switching frequency by R_T	V_{IN} = 12 V, R_{RT} = 5.76 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off high-side switch			2.1		V
t_{ON_MIN}	Minimum ON pulse width(1)	V_{OUT} = 1 V, I_{OUT} = 1 A		55	70	ns
t_{ON_MAX}	Maximum ON pulse width(1)			9		µs
t_{OFF_MIN}	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A		65	85	ns
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
T_{HYST}	Thermal shutdown hysteresis(1)			10		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) Production tested with V_{IN} = 3 V.
(3) This specification is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. This specification does not represent the total input current to the system while regulating. For additional information, reference the *Systems Characteristics* and the *Input Supply Current* sections.

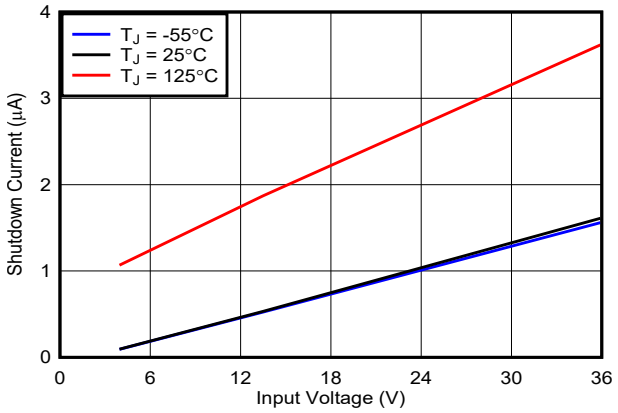
7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{EN} = V_{IN}, V_{VLDOIN} = V_{OUT}, f_{SW} = 800 kHz, I_{OUT} = 0 A		10		mA
OUTPUT VOLTAGE						
V_{FB}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.1 A to full load		1		mV
V_{FB}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 3 A		6		mV
V_{OUT}	Load transient	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 1 A to 2.5 A at 2 A/µs, $C_{OUT(derated)}$ = 49 µF		50		mV
EFFICIENCY						
η	Efficiency	V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 800 kHz		89.5%		
		V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 800 kHz		87.5%		
		V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 1 MHz		91%		
		V_{OUT} = 5 V, V_{IN} = 36 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 1 MHz		88.1%		
		V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 1.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 2 MHz		94.1%		

7.7 Typical Characteristics

V_{IN} = 24 V, unless otherwise specified



V_{EN} = 0 V

Figure 7-1. Shutdown Supply Current

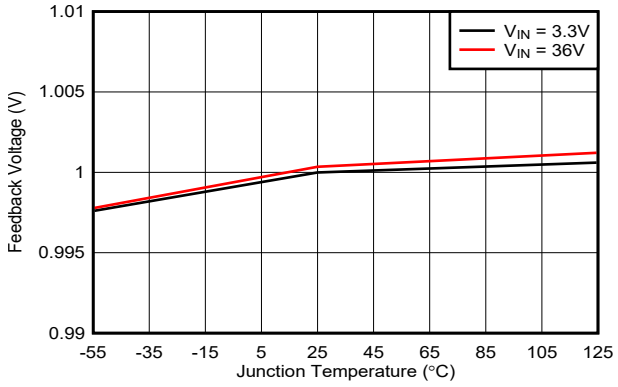


Figure 7-2. Feedback Voltage

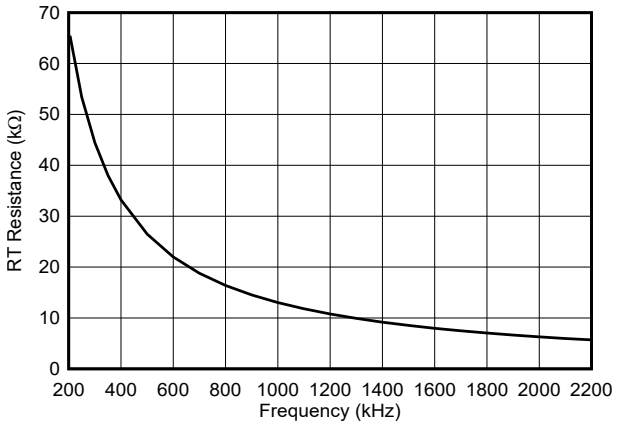


Figure 7-3. Switching Frequency Set by the RT Resistor

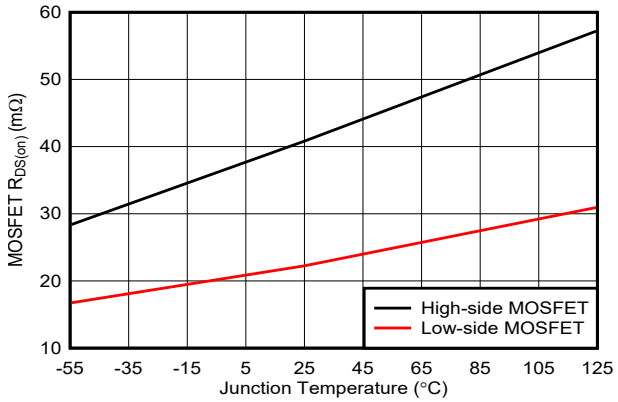


Figure 7-4. High-Side and Low-Side MOSFET $R_{DS(on)}$

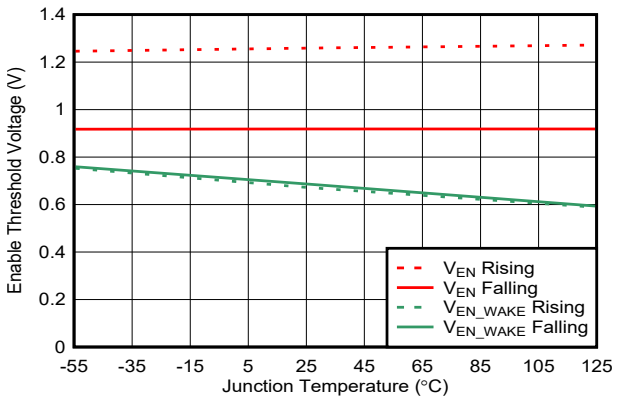


Figure 7-5. Enable Thresholds

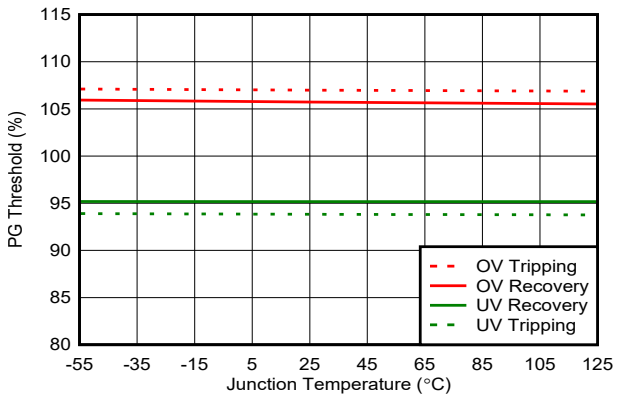
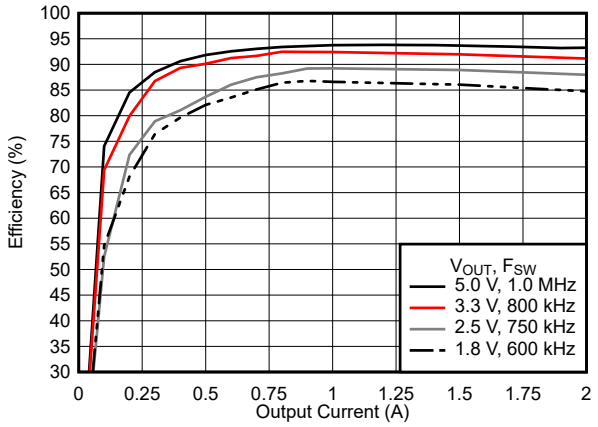


Figure 7-6. Power-Good (PG) Thresholds

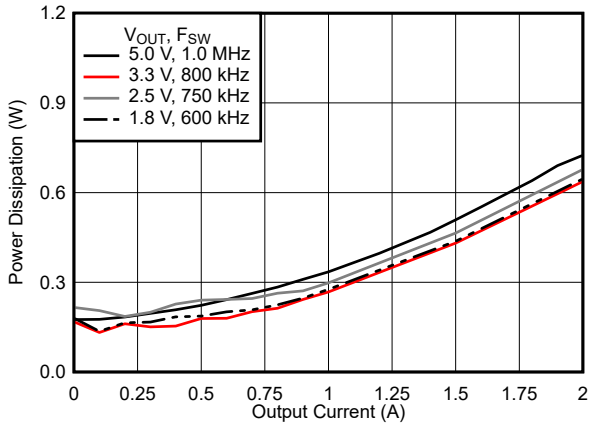
7.8 Typical Characteristics — 2-A Device (V_{IN} = 12 V)

Refer to Section 9.2 for circuit designs.



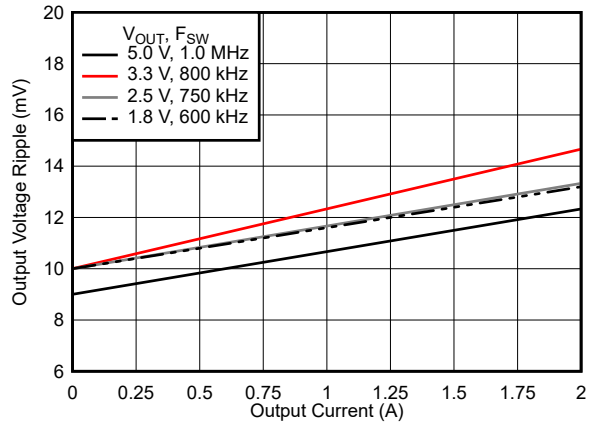
VLDOIN = VOUT

Figure 7-7. Efficiency



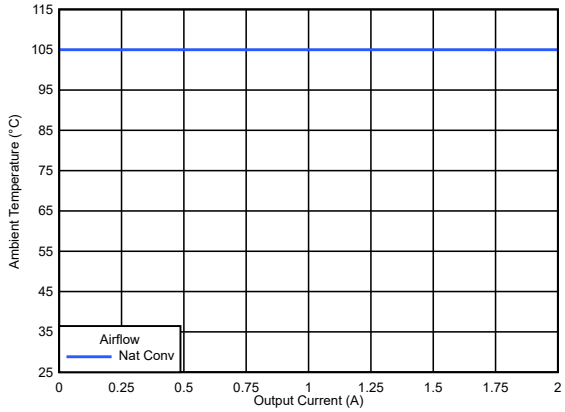
VLDOIN = VOUT

Figure 7-8. Power Dissipation



C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-9. Output Voltage Ripple

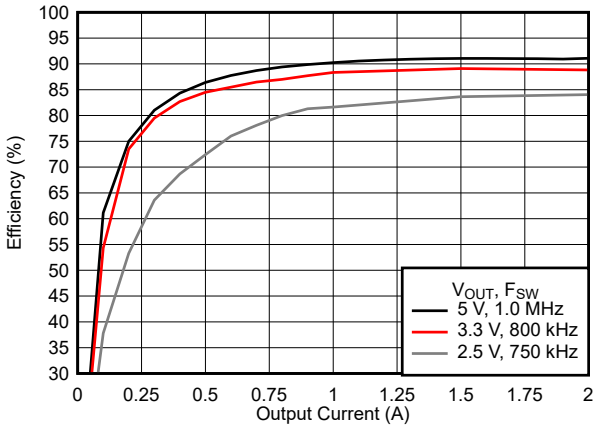


The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-10. Safe Operating Area (All V_{OUT})

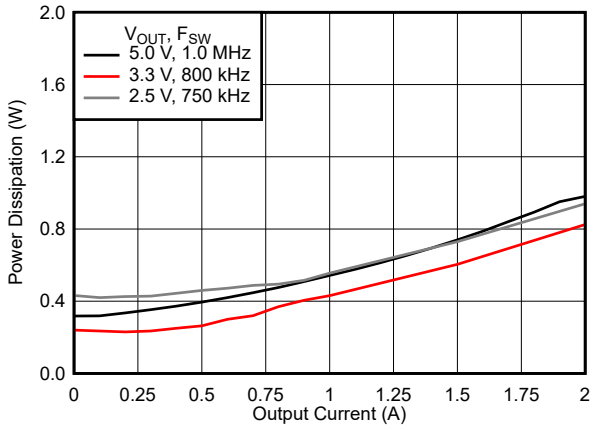
7.9 Typical Characteristics — 2-A Device (V_{IN} = 24 V)

Refer to Section 9.2 for circuit designs.



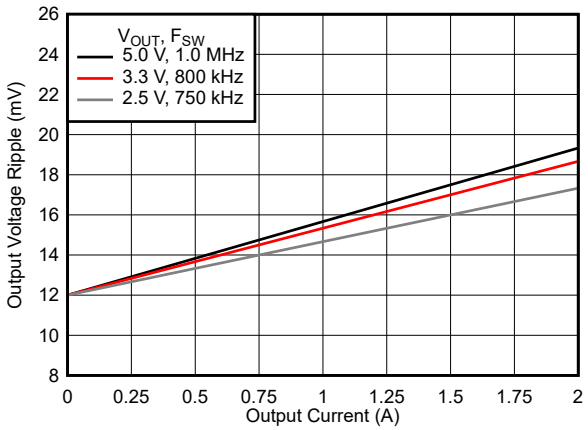
VLDOIN = VOUT

Figure 7-11. Efficiency



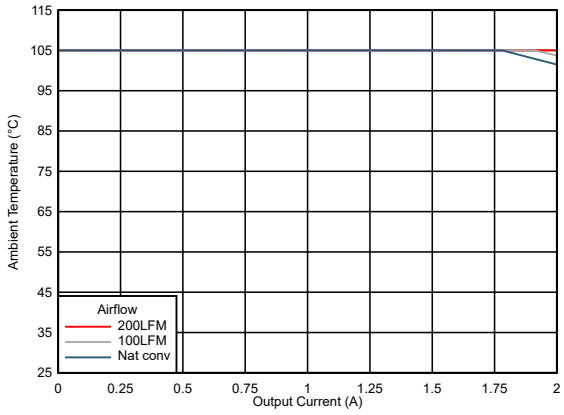
VLDOIN = VOUT

Figure 7-12. Power Dissipation



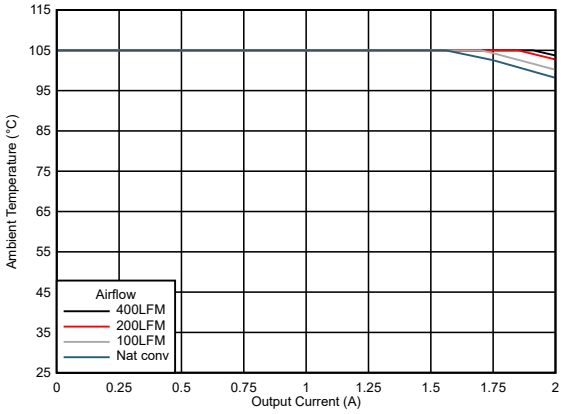
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-13. Output Voltage Ripple



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-14. Safe Operating Area (V_{OUT} = 3.3 V)

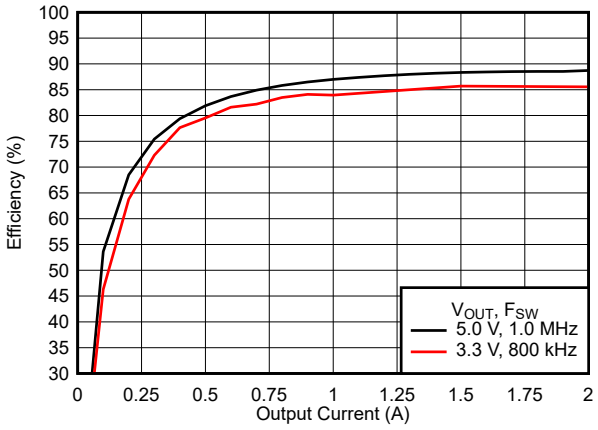


The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-15. Safe Operating Area (V_{OUT} = 5.0 V)

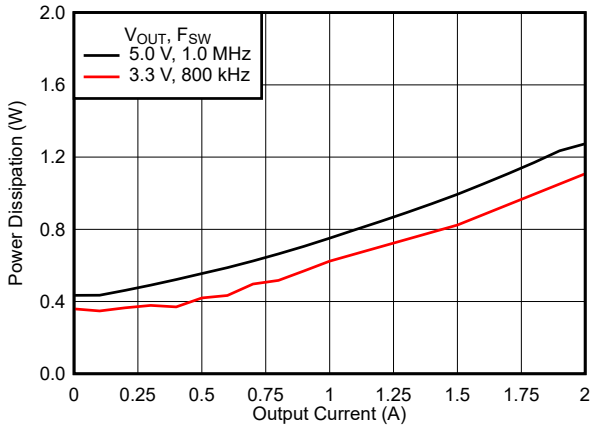
7.10 Typical Characteristics — 2-A Device (V_{IN} = 36 V)

Refer to Section 9.2 for circuit designs.



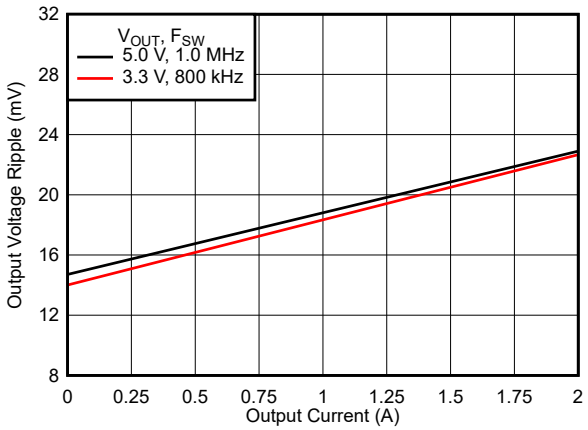
VLDOIN = VOUT

Figure 7-16. Efficiency



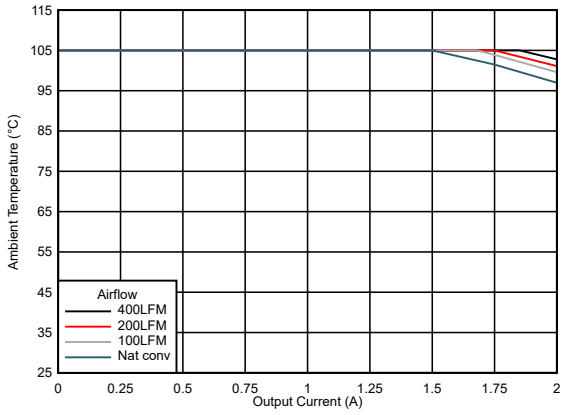
VLDOIN = VOUT

Figure 7-17. Power Dissipation



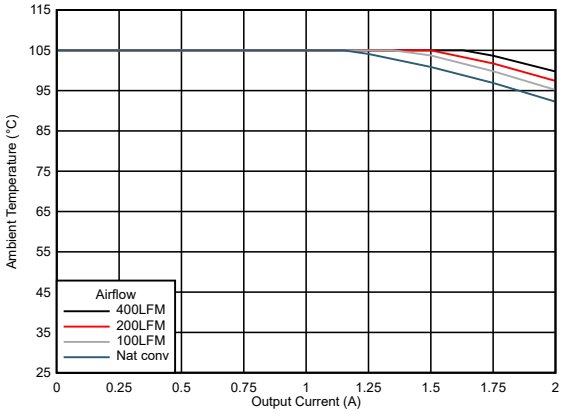
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-18. Output Voltage Ripple



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-19. Safe Operating Area (V_{OUT} = 3.3 V)



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-20. Safe Operating Area (V_{OUT} = 5.0 V)

8 Detailed Description

8.1 Overview

The TLVM13620 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, and 24-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TLVM13620 delivers up to 3-A DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin, the TLVM13620 incorporates specific features to improve EMI performance in noise-sensitive applications:

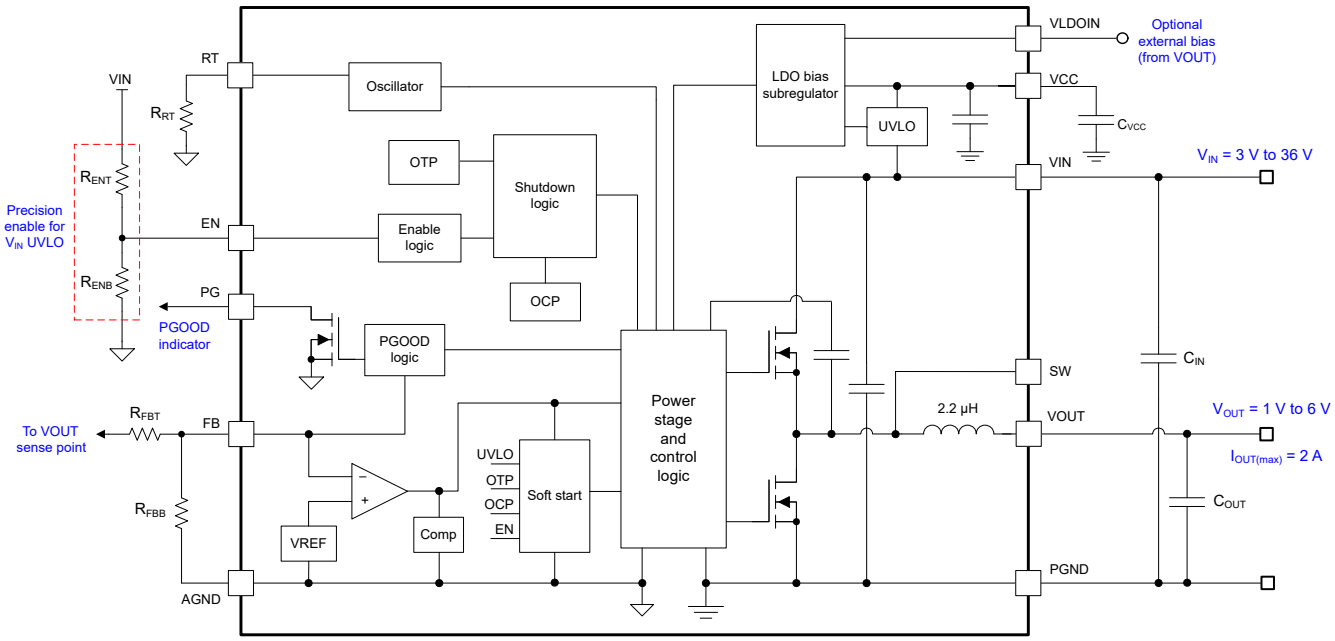
- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling.
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range.
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching.
- Adjustable switch-node slew rate allows optimization of EMI at higher frequency harmonics.

The TLVM13620 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components. See Section 11 for a layout example.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 36 V, the TLVM13620 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in Figure 8-1 shows all the necessary components to implement a TLVM13620-based buck regulator using a single input supply.

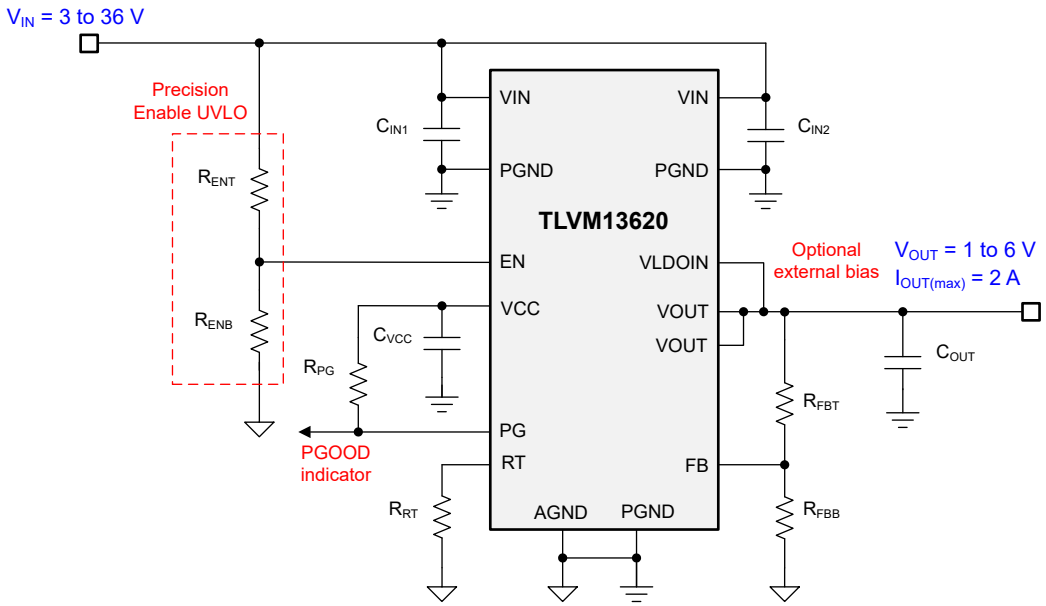


Figure 8-1. TLVM13620 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

Take extra care to make sure that the voltage at the VIN pins does not exceed the absolute maximum voltage rating of 40 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

8.3.2 Adjustable Output Voltage (FB)

The TLVM13620 has an adjustable output voltage range of 1 V to 6 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 8-2). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using Equation 1. Table 8-1 lists the standard resistor values for several output voltages and the recommended switching frequency. The minimum required output capacitance for each output voltage is also included in Table 8-1. The capacitance values listed represent the effective capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (1)$$

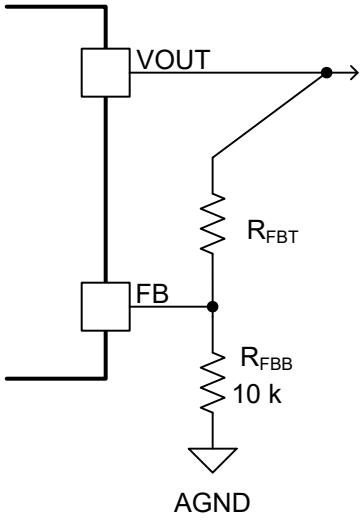


Figure 8-2. FB Resistor Divider

Table 8-1. Standard R_{FBT} Values, Recommended f_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ)(1)	Recommended f_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (Effective)	V_{OUT} (V)	R_{FBT} (kΩ)(1)	Recommended f_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (Effective)
1.0	Short	400	300	2.5	15	750	65
1.2	2	500	200	3.0	20	750	50
1.5	4.99	500	160	3.3	23.2	800	40
1.8	8.06	600	120	5.0	40.2	1000	25
2.0	10	600	100	6.0	49.9	1000	22

(1) R_{FBB} = 10 kΩ

Note that higher feedback resistances consume less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended because the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. Keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 11.

8.3.3 Input Capacitors

Input capacitors are required to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. Equation 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \quad (2)$$

where

- $D = V_{OUT} / V_{IN}$ is the module duty cycle.

Ideally, the DC and AC components of the input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT} – I_{IN}$) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resulting capacitive component of the AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 3 gives the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (3)$$

Equation 4 gives the input capacitance required for a particular load current.

$$C_{IN} \geq \frac{D \cdot (1 - D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \quad (4)$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TLVM13620 requires a minimum of 2 × 4.7-µF ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 8-2 includes a preferred list of capacitors by vendor.

Table 8-2. Recommended Input Capacitors

Vendor(1)	Dielectric	Part Number	Case Size	Capacitor Characteristics	
				Voltage Rating (V)	Capacitance (µF)(2)
TDK	X7R	C3216X7R1H475K160AC	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7
TDK	X7R	CGA6P3X7R1H475K250AB	1210	50	4.7
Murata	X7S	GCM31CC71H475KA03L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature.)

8.3.4 Output Capacitors

Table 8-1 lists the TLVM13620 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 8-3 for a preferred list of output capacitors by vendor.

Table 8-3. Recommended Output Capacitors

Vendor(1)	Temperature Coefficient	Part Number	Case Size	Capacitor Characteristics	
				Voltage (V)	Capacitance (µF)(2)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature.)

8.3.5 Switching Frequency (RT)

The switching frequency range of the TLVM13620 is 200 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Use Equation 5 to calculate the R_{RT} value for a desired frequency or simply select from Table 8-4. Note that a resistor value outside the recommended range can cause the device to shut down. This value prevents unintended operation if the RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization.

The switching frequency must be selected based on the output voltage setting of the device. See Table 8-4 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

$$R_{RT}\left[k\Omega\right] = \frac{13.46}{F_{SW}\left[MHz\right]} - 0.44 \quad (5)$$

Table 8-4. Switching Frequency Versus Output Voltage (I_{OUT} = A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} Range (V)		V_{OUT} Range (V)		V_{OUT} Range (V)		V_{OUT} Range (V)	
		Min	Max	Min	Max	Min	Max	Min	Max
200	66.5	1.0	2.0	1.0	2.0	1.0	1.5	1.0	1.5
400	33.2	1.0	3.0	1.0	4.0	1.0	3.3	1.2	3.0
600	22.1	1.0	3.5	1.0	6.0	1.5	6.0	1.8	5.0
800	16.5	1.0	3.5	1.0	6.0	1.5	6.0	2.5	6.0
1000	13.0	1.0	3.0	1.0	6.0	2.0	6.0	3.0	6.0
1200	10.7	1.0	3.0	1.5	6.0	2.5	6.0	3.5	6.0
1400	9.09	1.0	3.0	1.5	6.0	3.0	6.0	4.0	6.0
1600	8.06	1.0	3.0	1.5	6.0	3.0	6.0	4.5	6.0
1800	6.98	1.0	3.0	2.0	6.0	3.5	6.0	5.0	6.0
2000	6.34	1.2	2.5	2.0	6.0	4.0	6.0	5.5	6.0
2200	5.626	1.2	2.5	2.0	6.0	4.5	6.0	—	—

8.3.6 Output ON and OFF Enable (EN) and V_{IN} UVLO

The EN pin provides precision ON and OFF control for the TLVM13620. Once the EN pin voltage exceeds the threshold voltage and V_{IN} is above the minimum turn-on threshold, the device starts operation. The simplest way to enable the TLVM13620 is to connect EN directly to VIN, allowing the TLVM13620 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the employment of an enable divider network as shown in Figure 8-3, which establishes a precision input undervoltage lockout (UVLO). This network can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

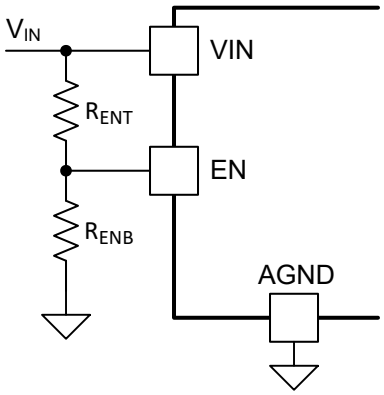


Figure 8-3. V_{IN} UVLO Using the EN Pin

R_{ENB} can be calculated using Equation 6.

$$R_{ENB}\left[k\Omega\right] = R_{ENT}\left[k\Omega\right] \cdot \left(\frac{V_{EN\_RISE}\left[V\right]}{V_{IN(on)}\left[V\right] - V_{EN\_RISE}\left[V\right]} \right) \quad (6)$$

where

- R_{ENT} is 100 kΩ (typical).
- V_{EN} is 1.263 V (typical).
- $V_{IN(ON)}$ is the desired start-up input voltage.

8.3.7 Power-Good Monitor (PG)

The TLVM13620 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. The PGOOD pin voltage goes low when the feedback voltage is outside of the PGOOD thresholds, which occurs during the following:

- While the device is disabled
- In current limit
- In thermal shutdown
- During normal start-up, when the output voltage has not reach its regulation value

A glitch filter prevents false flag operation for short excursions (< 120 µs typical) of the output voltage, such as during line and load transients.

PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 20 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in Figure 8-4, or for fault protection and output monitoring.

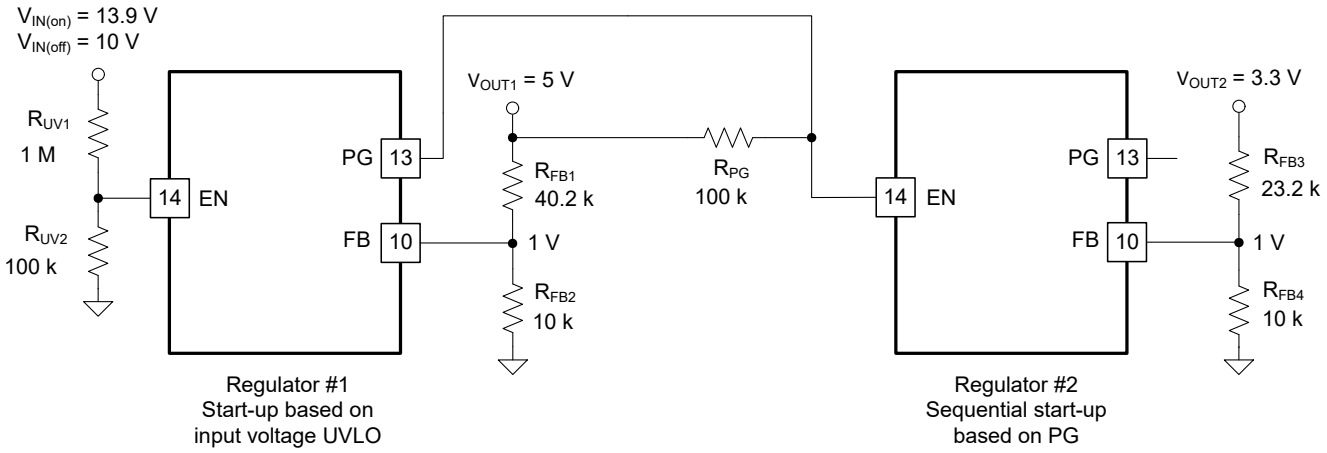


Figure 8-4. TLVM13620 Sequencing Implementation Using PG and EN

8.3.8 Internal LDO, VCC Output, and VLDOIN Input

The TLVM13620 has an internal LDO to power internal circuitry. The VCC pin is the output of the internal LDO. This pin must not be used to power external circuitry. Connect a high-quality, 1-µF capacitor from this pin to AGND, close to the device pins. Do not load the VCC pin or short it to ground.

The VLDOIN pin is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity.

The LDO generates the VCC voltage from one of the two inputs: V_{IN} or the VLDOIN input. When VLDOIN is tied to ground or below 3.1 V, the LDO is powered from V_{IN}. When VLDOIN is tied to a voltage higher than 3.1 V, the LDO input is powered from VLDOIN. VLDOIN voltage must be lower than both V_{IN} and 12.5 V.

The VLDOIN input is designed to reduce the LDO power loss. The LDO power loss is:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\_LDO} - V_{VCC}) \quad (7)$$

The higher the difference between the input and output voltages of the LDO, the more loss occurs to supply the same LDO output current. The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, to reduce the difference of the input and output voltages of the LDO, and reduce power loss. For example, if the LDO current were 10 mA at a certain frequency with V_{IN} = 24 V and V_{OUT} = 5 V. The LDO loss with VLDOIN tied to ground is:

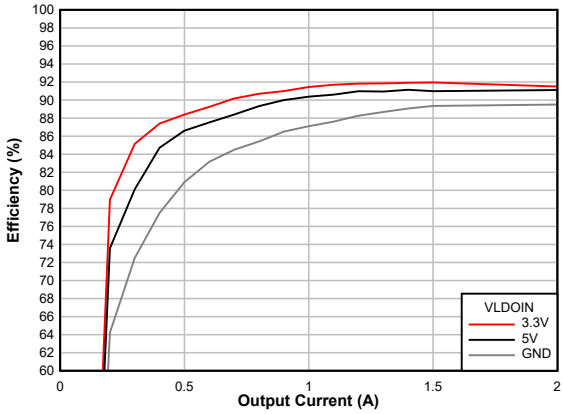
$$10\ mA \times (24\ V - 3.3\ V) = 207\ mW \quad (8)$$

The loss with VLDOIN tied to V_{OUT} (5 V) is:

$$10\ mA \times (5\ V - 3.3\ V) = 17\ mW \quad (9)$$

The efficiency improvement is more significant at light and mid loads because the LDO loss is a higher percentage of the total loss. The improvement is more significant with higher switching frequency because the LDO current is higher at higher switching frequency. The improvement is more significant when V_{IN} » V_{OUT} because the voltage difference is higher.

Figure 8-5 shows typical efficiency waveforms with VLDOIN powered by different input voltages.



V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz

I_{LDO} = 10 mA

Figure 8-5. Efficiency Improvements with VLDOIN (V_{OUT} = 5 V)

8.3.9 Overcurrent Protection (OCP)

The TLVM13620 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TLVM13620 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the regulator is shut down and kept off for 80 ms (typical) before the TLVM13620 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

8.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TLVM13620 attempts to restart when the junction temperature falls to 158°C (typical).

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TLVM13620. When V_{EN} is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The input quiescent current in shutdown mode drops to 0.6 µA (typical). The TLVM13620 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

8.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

8.4.3 Active Mode

The TLVM13620 is in active mode when V_{IN} and V_{EN} are above their relevant thresholds and no fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self-start–up when the applied input voltage exceeds the minimum start-up voltage.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TLVM13620 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. The following section describes the design procedure to configure the TLVM13620 power module. To expedite and streamline the design process, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases.

As mentioned previously, the TLVM13620 also integrates several optional features to meet system design requirements, including the following:

- Precision enable with hysteresis
- External adjustable UVLO
- Adjustable SW node slew rate
- A power-good indicator

The following application circuits show the TLVM13620 configuration options suitable for several application use cases.

9.2 Typical Applications

The following designs show sample typical applications and design procedures to implement the TLVM13620.

9.2.1 Design 1 — 2-A Synchronous Buck Regulator for Industrial Applications

Figure 9-1 shows the schematic diagram of a 5-V, 2-A buck regulator with a switching frequency of 1 MHz. The nominal input voltage for the sample design is 24 V. A 13-kΩ R_{RT} resistor sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency for this specific application.

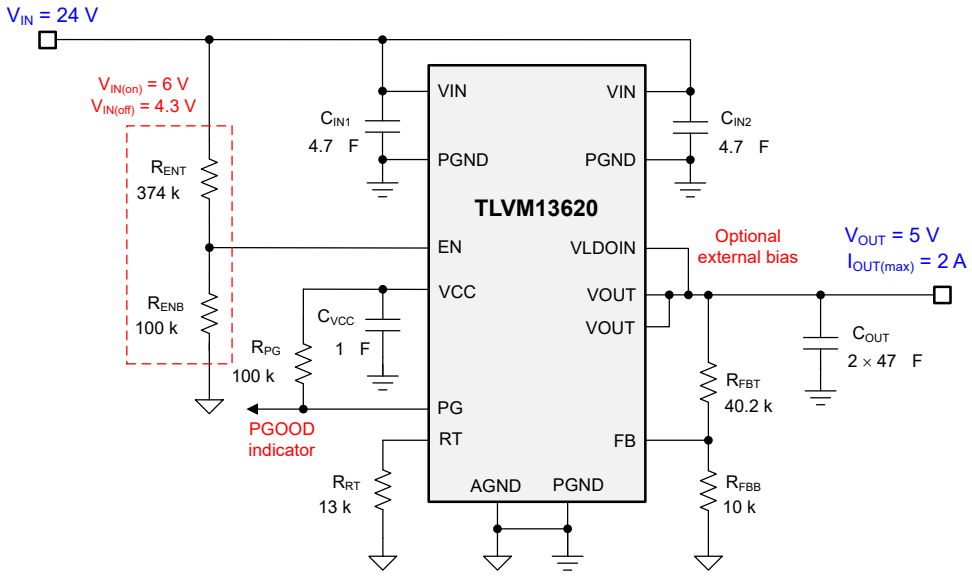


Figure 9-1. Circuit Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters and follow the design procedures in Section 9.2.1.2.

Table 9-1. Design Example Parameters

Design Parameter	Value
Input voltage	24 V
Output voltage	5 V
Output current	0 A to 2 A
Switching frequency	1 MHz

Table 9-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 9-2. List of Materials for Application Circuit 1

Reference Designator	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}	2	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 100 V, X7S, 1206, ceramic	Murata	GRM31CC72A475KE11L
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
		1 µF, 16 V, X5R, 0402, ceramic	Taiyo Yuden	EMK105BJ105KVHF
U_1	1	TLVM13620 36-V, 2-A synchronous buck module	Texas Instruments	TLVM13620RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TLVM13620 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLVM13620 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Output Voltage Setpoint

The output voltage of the TLVM13620 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBB} can be selected from Table 8-1 or calculated using Equation 10:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (10)$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

9.2.1.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 8-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND.

9.2.1.2.4 Input Capacitor Selection

The TLVM13620 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, select two 4.7-µF, 50-V, 1210 case size, ceramic capacitors.

9.2.1.2.5 Output Capacitor Selection

For a 5-V output, the TLVM13620 requires a minimum of 25 µF of effective output capacitance for proper operation (see Table 8-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

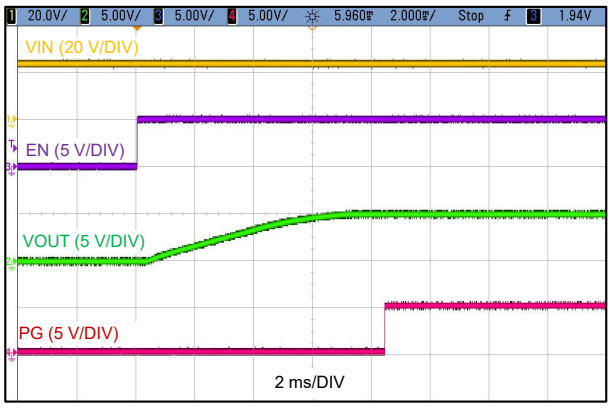
For this design example, select two 47-µF, 10-V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 48 µF at 5 V.

9.2.1.2.6 Other Connections

- Connect VLDOIN to VOUT to improve efficiency.
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

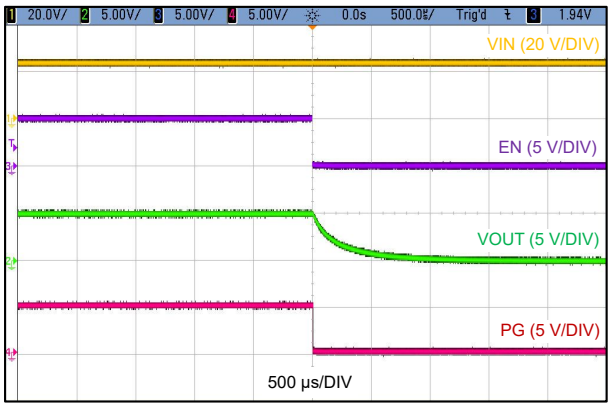
9.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 2 A), and f_{SW} = 1 MHz



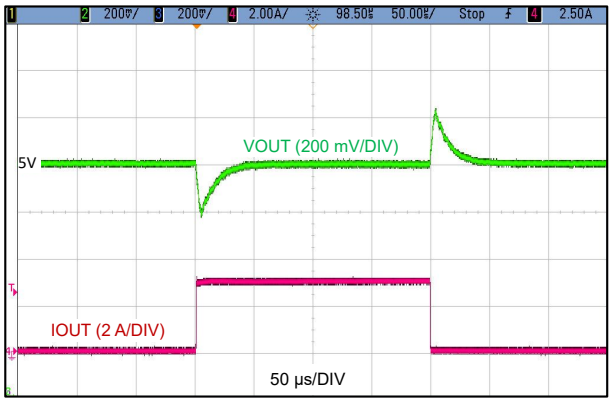
V_{IN} = 24 V V_{OUT} = 5 V

Figure 9-2. Start-Up Waveforms



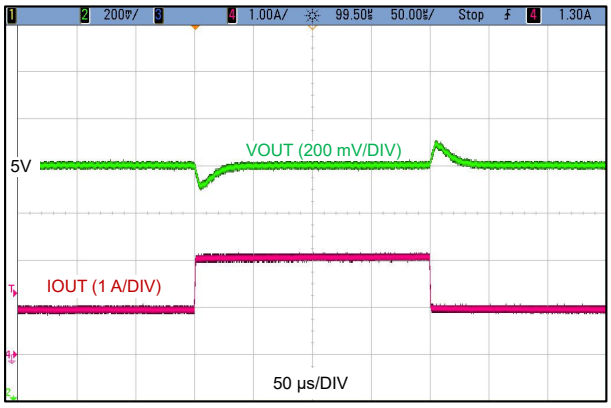
V_{IN} = 24 V V_{OUT} = 5 V

Figure 9-3. Shutdown Waveforms



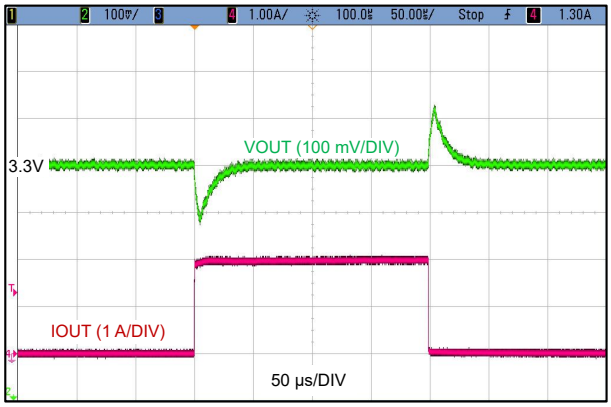
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-4. Load Transient, 0 A to 2 A, 1 A/µs



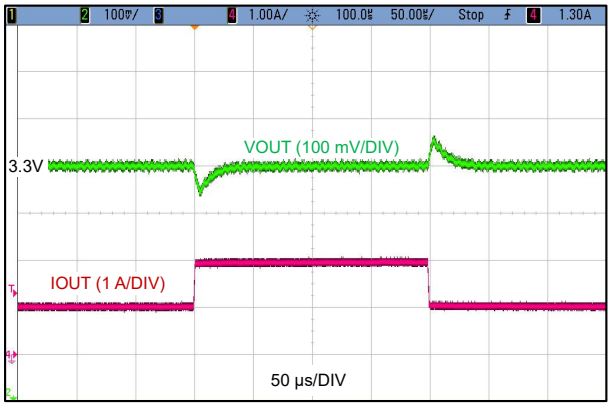
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-5. Load Transient, 1 A to 2 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-6. Load Transient, 0 A to 2 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-7. Load Transient, 1 A to 2 A, 1 A/µs

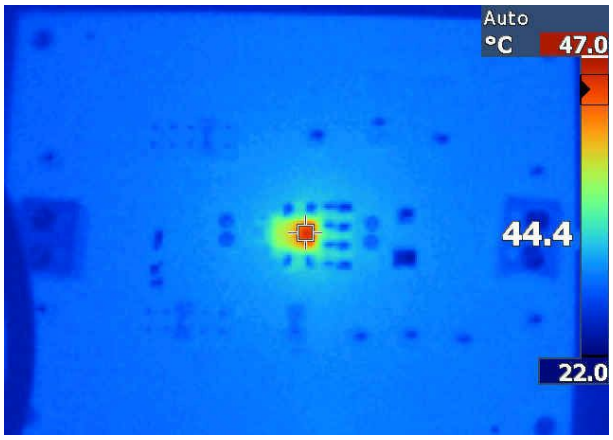


Figure 9-8. Thermal Image, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

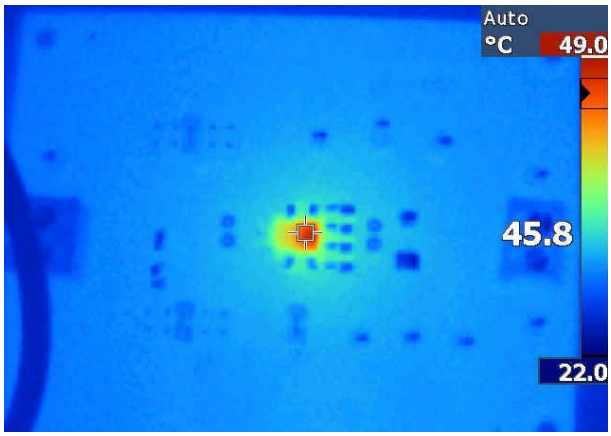


Figure 9-9. Thermal Image, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

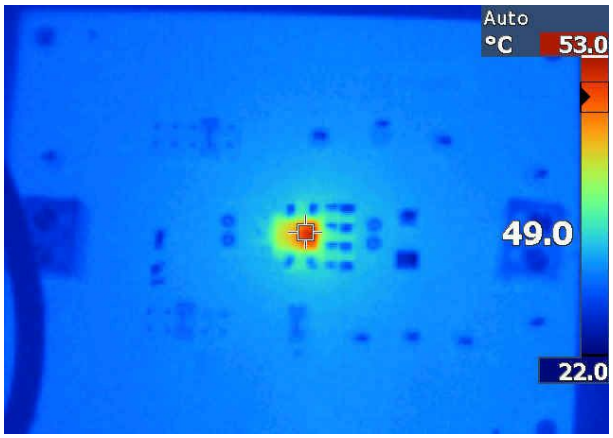


Figure 9-10. Thermal Image, V_{IN} = 24 V, V_{OUT} = 3.3 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

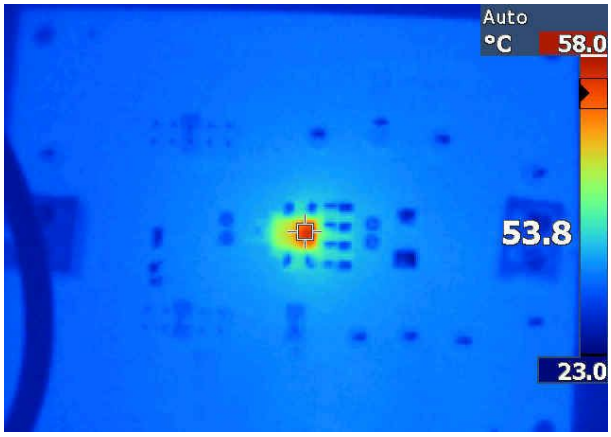


Figure 9-11. Thermal Image, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

9.2.2 Design 2 — Inverting Buck-Boost Regulator with a –5-V Output

Figure 9-12 shows the schematic diagram of a –5-V inverting buck-boost regulator with a switching frequency of 1 MHz. The input voltage range for the sample design is 12 V to 24 V.

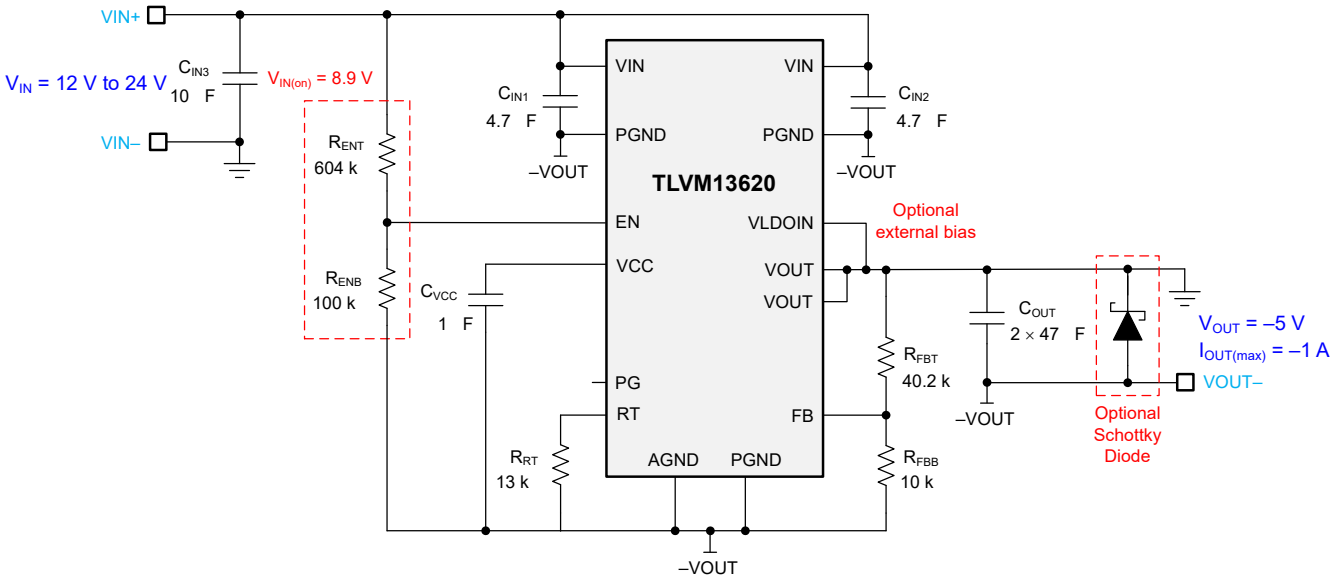


Figure 9-12. Circuit Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-3 as the input parameters and follow the design procedures in Section 9.2.2.2.

Table 9-3. Design Example Parameters

Design Parameter	Value
Input voltage	12 to 24 V
Output voltage	–5 V
Output current	0 A to 1 A
Switching frequency	1 MHz

Table 9-4 gives the selected module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 9-4. List of Materials for Application Circuit 2

Reference Designator	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}, C_{IN3}	3	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 50 V, X7S, 1206, ceramic	Murata	GCM31CC71H475KA03K
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
U_1	1	TLVM13620 36-V, 2-A synchronous buck module	Texas Instruments	TLVM13620RDLR

More generally, the TLVM13620 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Output Voltage Setpoint

The output voltage of the TLVM13620 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. Calculate the value for R_{FBT} using Equation 11.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \tag{11}$$

For the desired output voltage of –5 V, enter the absolute value of 5 V for V_{OUT} in Equation 11. The formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

9.2.2.2.2 IBB Maximum Output Current

The achievable output current with an IBB topology using the TLVM13620 is:

$$I_{OUT(max)} = I_{LDC(max)} \times (1 - D) \tag{12}$$

where

- $I_{LDC(max)}$ = 2 A is the rated current of the module.
- $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the module duty cycle.

Therefore, in the case of V_{IN} = 12 V and V_{OUT} = –5 V, the maximum output current is 1.4 A.

9.2.2.2.3 Switching Frequency Selection

To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND pins of the module based on Equation 5.

9.2.2.2.4 Input Capacitor Selection

The TLVM13620 requires a minimum input capacitance of 2 × 4.7-µF ceramic type between the VIN pins and PGND pins as close as possible to the module. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. In an inverting buck-boost configuration, the maximum voltage between VIN and PGND pin of the module is equal to $V_{IN} + |V_{OUT}|$.

For this design, two 4.7-µF, 50-V, 1210 case size, ceramic capacitors are selected.

9.2.2.2.5 Output Capacitor Selection

The TLVM13620 requires a minimum of 25 µF of effective output capacitance for proper operation. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, two 47-µF, 10-V, 1210 case size, ceramic capacitors are used, which have a total effective capacitance of approximately 48 µF at 5 V.

9.2.2.2.6 Other Connections

Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

The right-half-plane zero of an IBB topology is at its lowest frequency at minimum input voltage. However, it does not appear at low frequency for a –5-V output and has minimal effect on the loop response for this application.

In an inverting buck-boost configuration, the input capacitor, C_{IN}, and output capacitor, C_{OUT}, can form an AC capacitive divider during a fast V_{IN} transient or hot-plugged event at the input. This event will result in a positive voltage spike at the output that can disturb the load. In this case, an optional Schottky diode can be installed between –VOUT and GND as shown in Figure 9-12 to clamp the output spike.

9.2.2.2.7 EMI

The TLVM13620 is compliant with EN55011 radiated emissions. Figure 9-13, Figure 9-14, and Figure 9-15 show typical examples of radiated emission plots for the TPSM63603 , which is in the same family of parts. The graphs include the plots of the antenna in the horizontal and vertical positions.

9.2.2.2.7.1 EMI Plots

EMI plots were measured using the standard TPSM63603EVM.

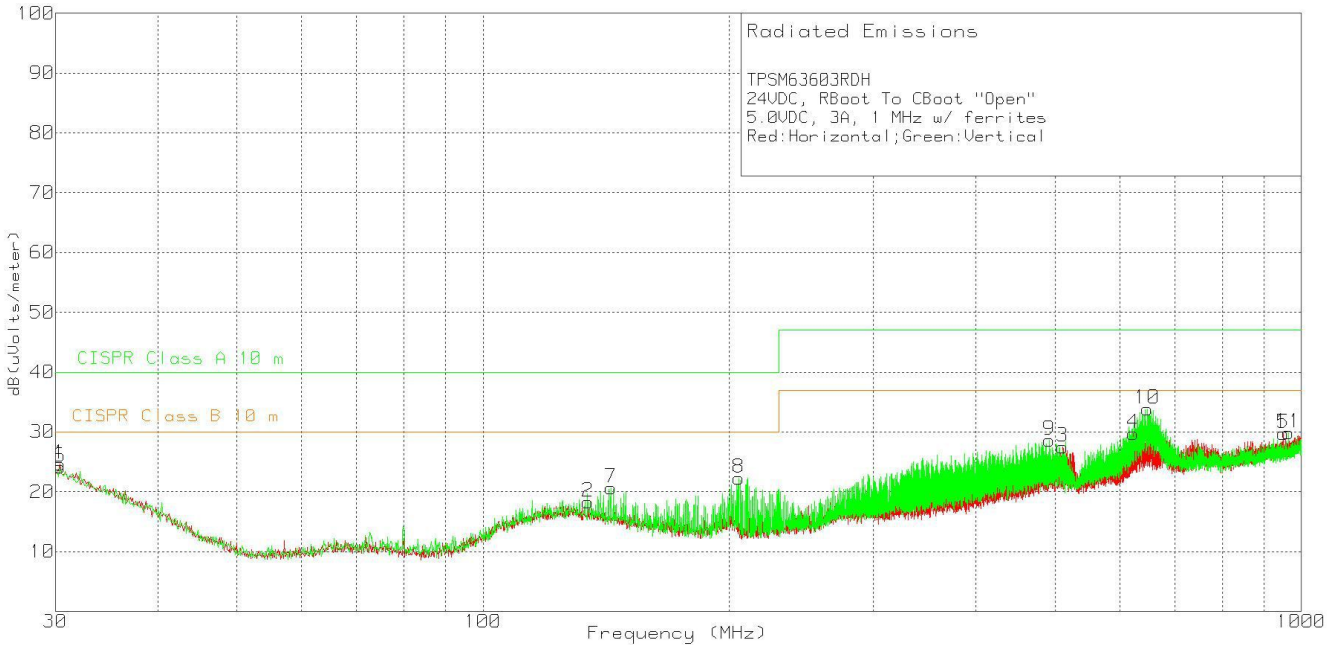


Figure 9-13. Radiated Emissions, 24-V Input, 5-V Output, 3-A Load

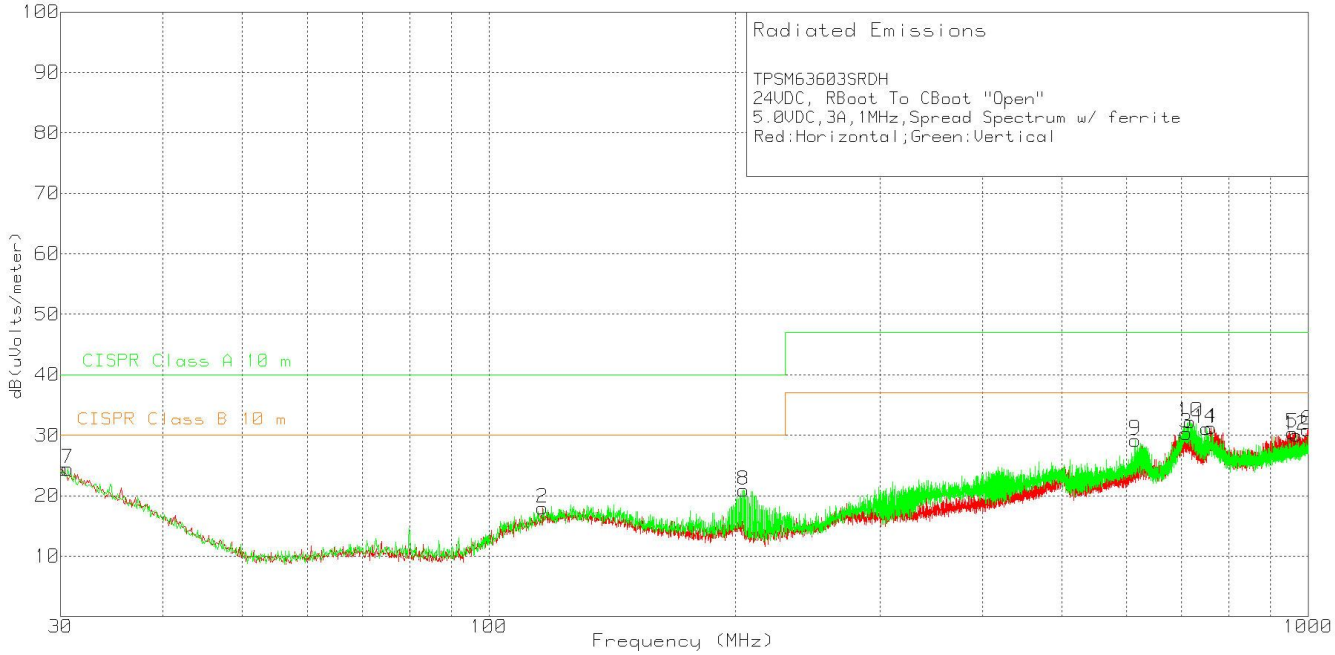


Figure 9-14. Radiated Emissions, 24-V Input, 5-V Output, 3-A Load, Spread Spectrum

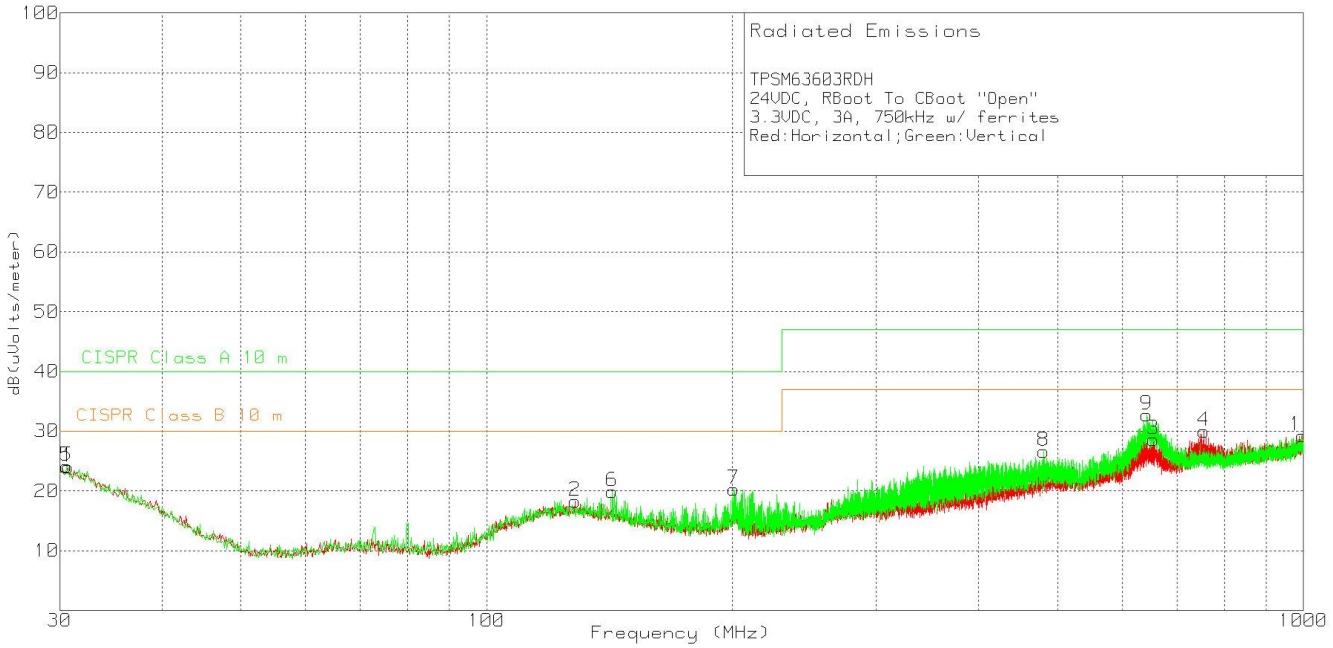


Figure 9-15. Radiated Emissions, 24-V Input, 3.3-V Output, 3-A Load

10 Power Supply Recommendations

The TLVM13620 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 13.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \ \eta} \tag{13}$$

where

- η is efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

11 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

11.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 11-1 and Figure 11-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high-frequency noise.
- Locate additional output capacitors between the ceramic capacitors and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

11.2 Layout Example

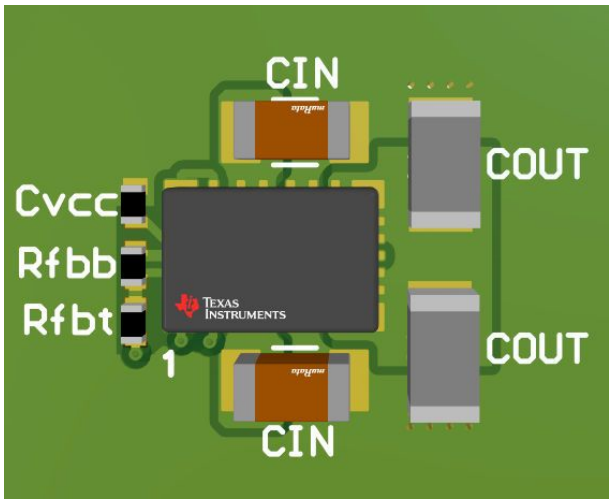


Figure 11-1. Typical Top-Layer Layout

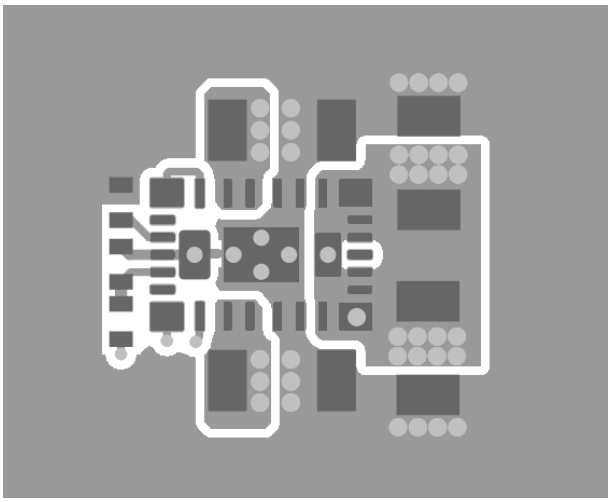


Figure 11-2. Typical Top Layer

11.2.1 Package Specifications

Table 11-1. Package Specifications Table

TLVM13620		Value	Unit
Weight		123	mg
Flammability	Meets UL 94 V-0		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	84	MHrs

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current from 2 A to 6 A, the TLVM13620, TLVM13630, TLVM13640, and TLVM13660 family of synchronous buck power modules specified in Table 12-1 provides flexibility, scalability and optimized solution size for a range of applications. These modules enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include RBOOT-configured switch-node slew rate control, fixed switching frequency, and integrated input bypass capacitors. All modules are rated for an ambient temperature up to 105°C.

Table 12-1. Synchronous Buck DC/DC Power Module Family

DC/DC Module	Rated I_{OUT}	Package	Dimensions	Features	EMI Mitigation
TLVM13620	2 A	B0QFN (30)	4.0 × 6.0 × 1.8 mm	RT adjustable F_{SW}, precision enable	Integrated BOOT capacitor
TLVM13630	3 A				
TLVM13640	4 A	B3QFN (20)	5.0 × 5.5 × 4.0 mm		Integrated input, VCC and BOOT capacitors
TLVM13660	6 A				

For development support, see the following:

- TLVM13620 *Quickstart Calculator*
- TLVM13620 *Simulation Models*
- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter.

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLVM13620 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.

- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602, TPSM53603, and TPSM53604 for Negative Output Inverting Buck-Boost Applications* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLVM13620RDHR	ACTIVE	B0QFN	RDH	30	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	13620	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

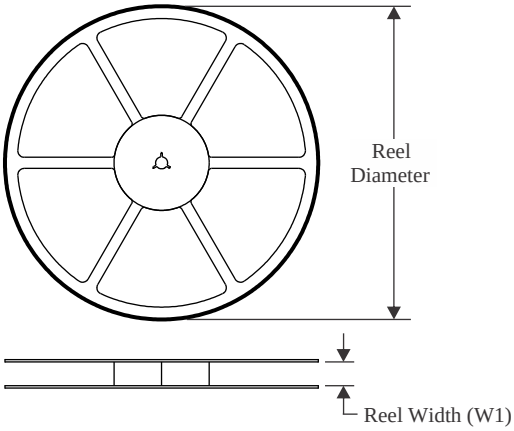
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

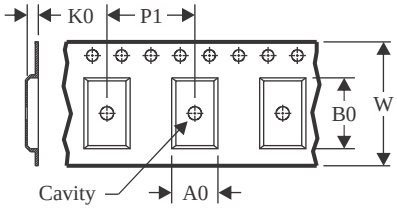
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

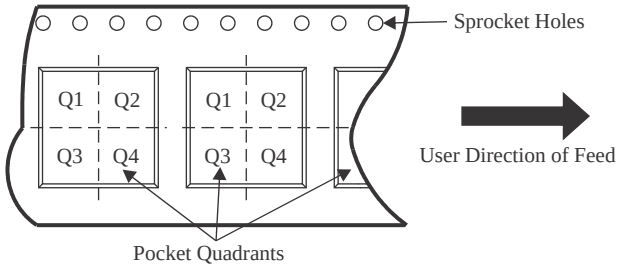


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

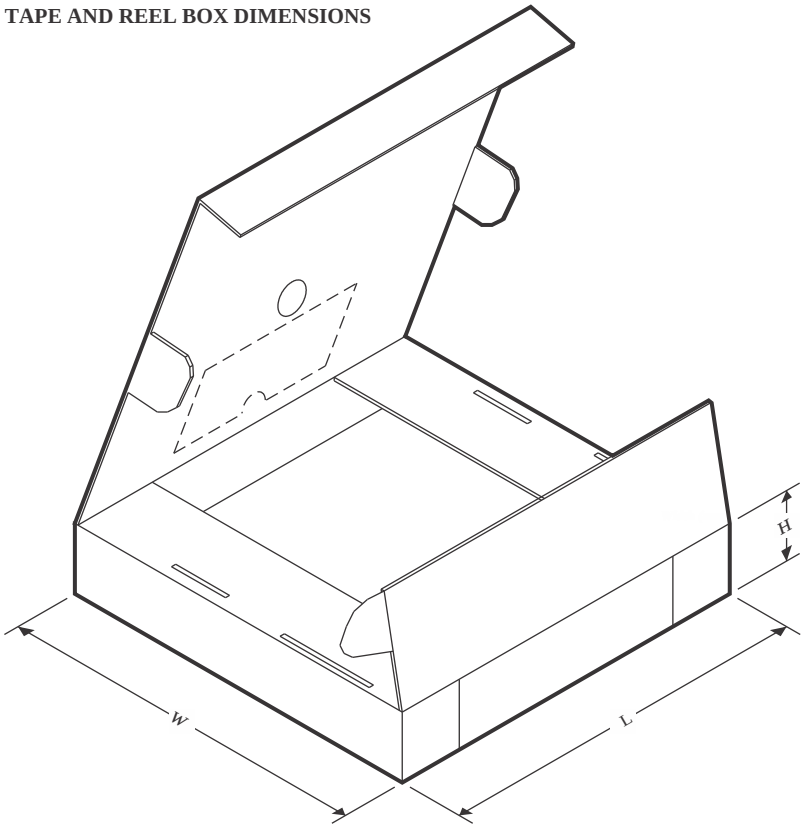
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLVM13620RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

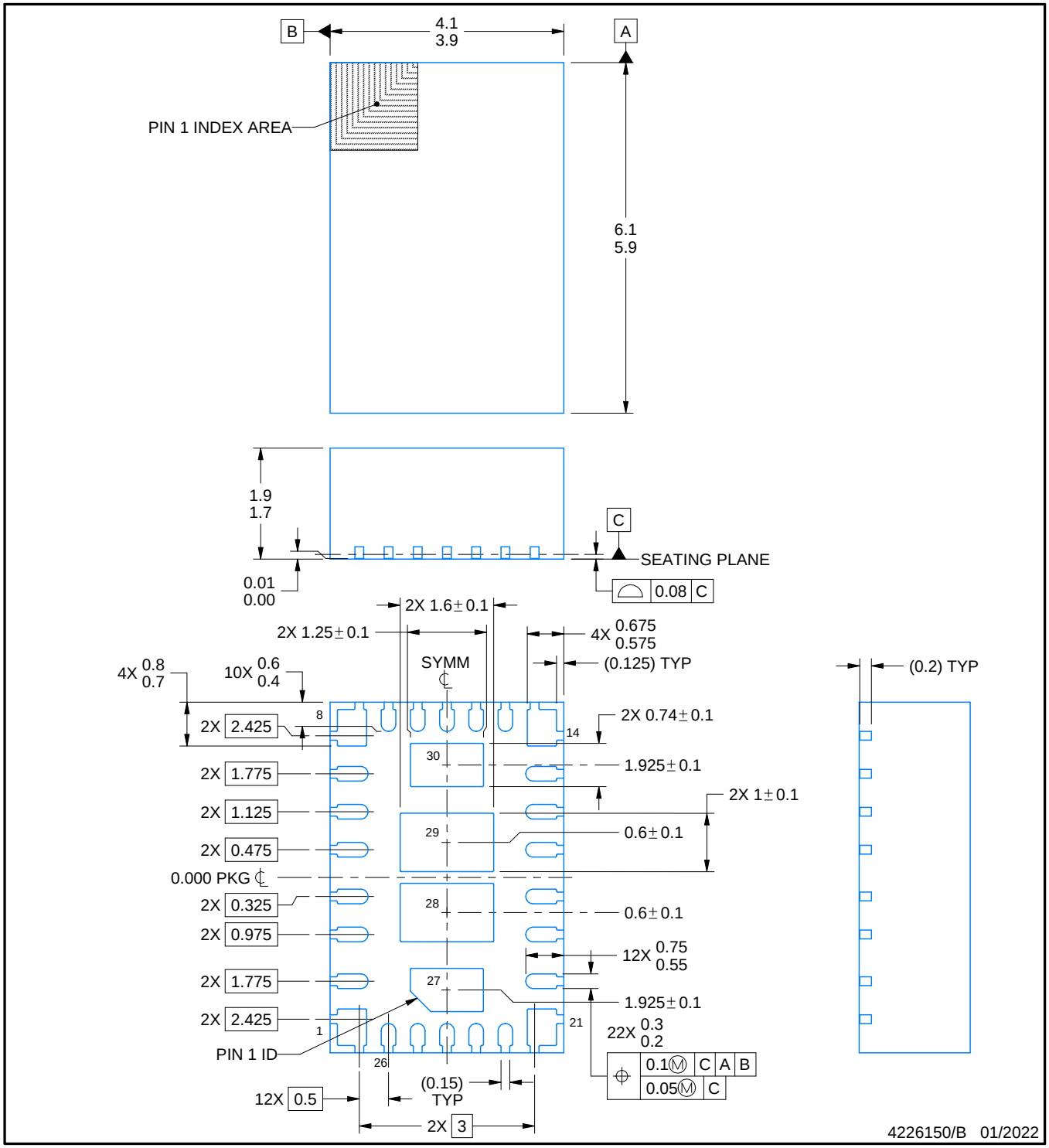
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLVM13620RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDH0030A

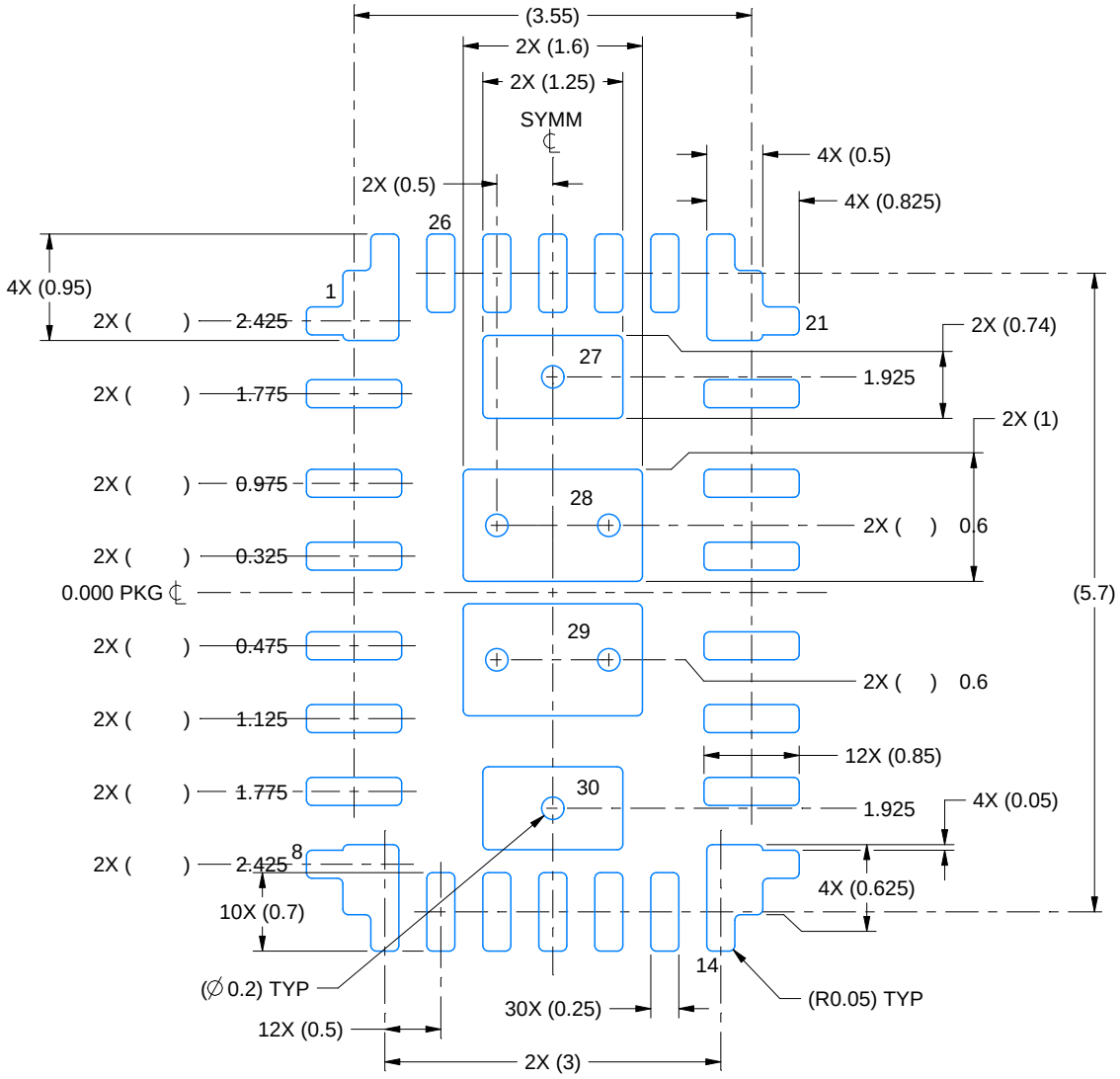
B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

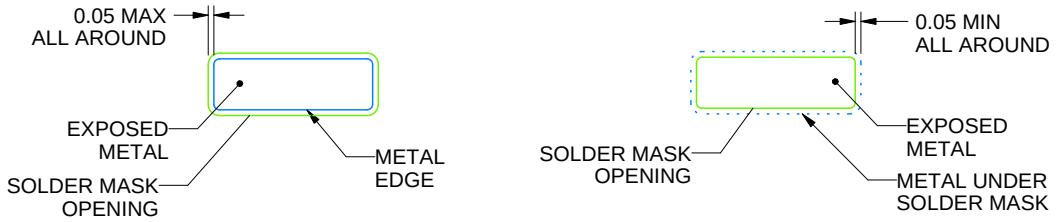


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

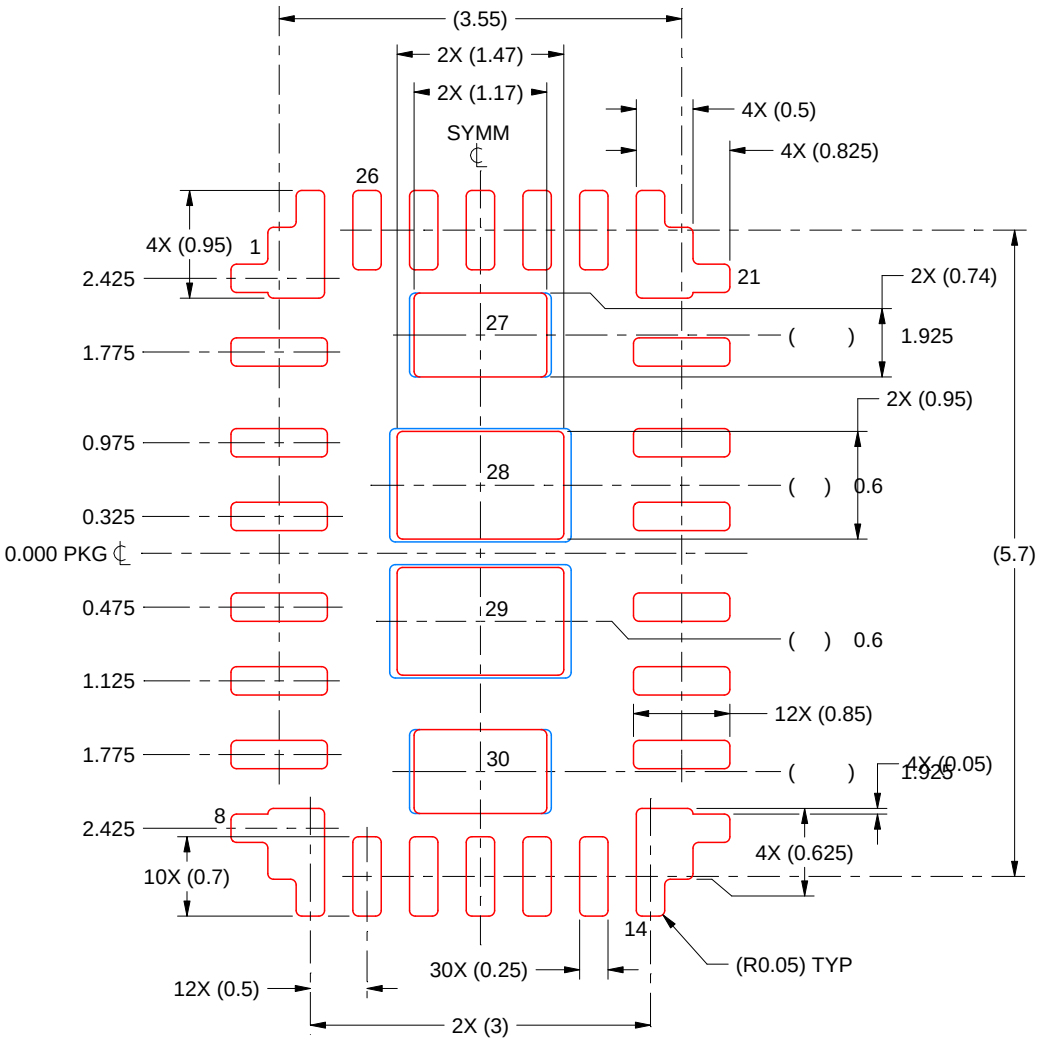


SOLDER MASK DETAILS

4226150/B 01/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 27 & 30:
94% PRINTED SOLDER COVERAGE BY AREA

EXPOSED PAD 28 & 29
87% PRINTED SOLDER COVERAGE BY AREA

SCALE:15X

4226150/B 01/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TLVM13630
SLVSFT6B – MAY 2021 – REVISED JANUARY 2022

TLVM13630 High-Density, 3-V to 36-V Input, 1-V to 6-V Output, 3-A Power Module With Enhanced HotRod™ QFN Package

1 Features

- Versatile synchronous buck DC/DC module
  - Integrated MOSFETs, inductor, and controller
  - Wide input voltage range of 3 V to 36 V
  - Adjustable output voltage from 1 V to 6 V with 1% setpoint accuracy over temperature
  - 4-mm × 6-mm × 1.8-mm overmolded package
  - –40°C to 125°C junction temperature range
  - Frequency adjustable from 200 kHz to 2.2 MHz
  - Negative output voltage capability
- Ultra-high efficiency across the full load range
  - 93% peak efficiency at 12 V_{IN}, 5 V_{OUT},1 MHz
  - External bias option for improved efficiency
  - Shutdown quiescent current of 0.6 µA (typical)
  - 0.4-V typical dropout voltage at 3-A load
- Ultra-low conducted and radiated EMI signatures
  - Low-noise package with dual input paths and integrated capacitors reduces switch ringing
  - Constant-frequency FPWM mode of operation
  - Meets CISPR 11 and 32 class B emissions
- Suitable for scalable power supplies
  - Pin compatible with the TLVM13620 (36 V, 2 A)
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and V_{IN} UVLO
  - Hiccup-mode overcurrent protection
  - Thermal shutdown protection with hysteresis
- Create a custom design using the TLVM13630 with the WEBENCH® Power Designer

2 Applications

- Test and measurement, aerospace and defense
- Factory automation and control
- Buck and inverting buck-boost power supplies

3 Description

The TLVM13630 synchronous buck power module is a highly integrated 36-V, 3-A DC/DC solution that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

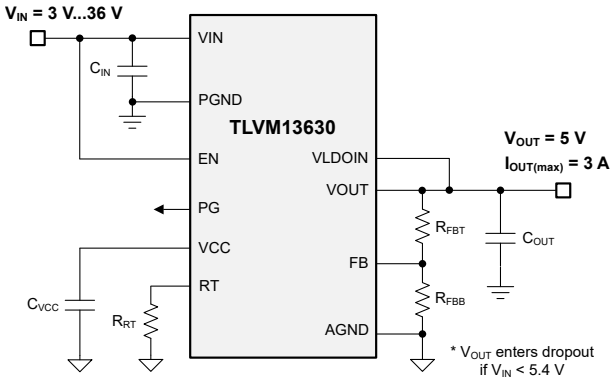
With an output voltage range from 1 V to 6 V, the TLVM13630 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total solution requires as few as four external components and eliminates the magnetics and compensation part selection from the design process.

Although designed for small size and simplicity in space-constrained applications, the TLVM13630 module offers many features for robust performance: precision enable with hysteresis for adjustable input-voltage UVLO, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, negative output voltage capability for inverting applications, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

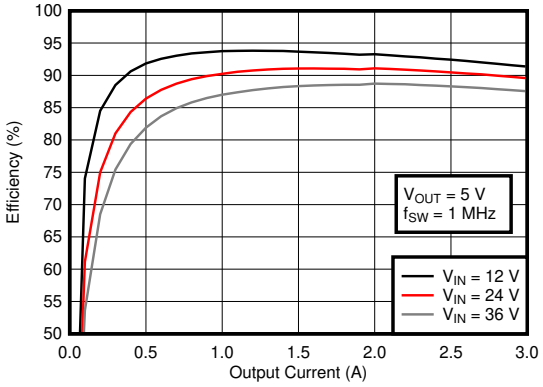
Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TLVM13630	B0QFN (30)	4.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Schematic



Typical Efficiency, V_{OUT} = 5 V, F_{SW} = 1 MHz

Table of Contents

4 Revision History

Changes from Revision * (March 2021) to Revision A (January 2022)	Page
• Changed document status from Advance Information to Production Data	1

Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	MODE	SPREAD SPECTRUM	OUTPUT VOLTAGE	EXTERNAL SYNC	JUNCTION TEMPERATURE
TLVM13630	TLVM13630RDHR	FPWM	No	Adjustable	No	–40°C to 125°C

5 Pin Configuration and Functions

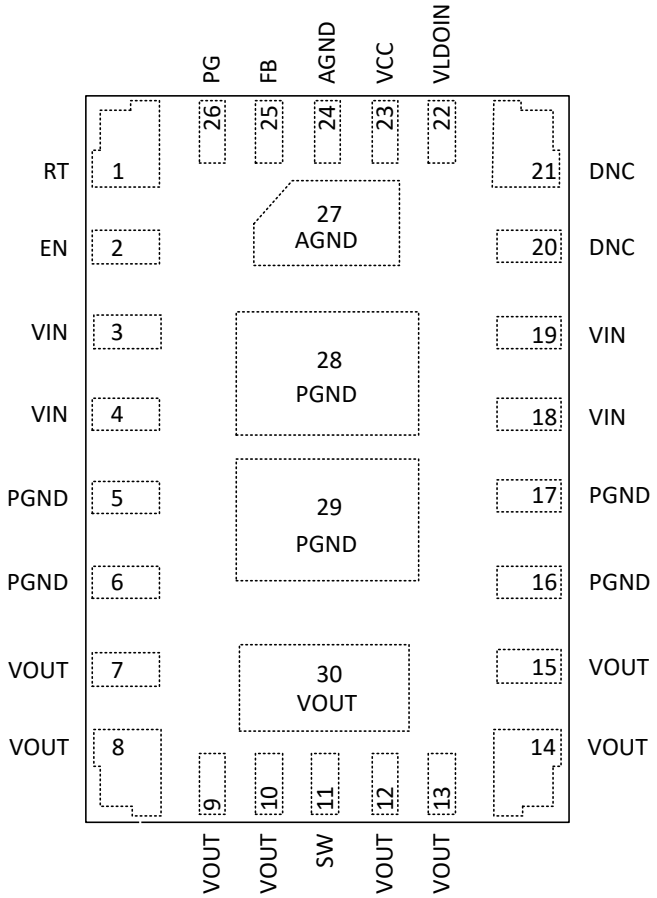


Figure 5-1. 30-Pin QFN, RDH Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	RT	I	Frequency setting pin. This analog pin is used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from this pin to AGND. Do not leave open or connect to ground.
2	EN	I	Precision enable input pin. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Place an external voltage divider between this pin, AGND, and VIN to create an external UVLO.
3, 4, 18, 19	VIN	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device. Refer to Section 10.2 for input capacitor placement example.
5, 6, 16, 17, 28, 29	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See Section 10.2 for a recommended layout.
7-10, 12–15, 30	VOUT	P	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
11	SW	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
20,21	DNC	–	Do Not Connect. Do not connect these pins to ground, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
22	VLDOIN	P	Optional LDO supply input. Connect to VOUT or to other voltage rail to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. Do not connect to a voltage above 12 V or to a voltage greater than VIN. If unused, connect this pin to ground..
23	VCC	O	Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF ceramic capacitor from this pin to PGND.
24, 27	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. **This pin must be connected to PGND at a single point.** See Section 10.2 for a recommended layout.
25	FB	I	Feedback input. For the adjustable output version, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. When connecting with feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See Section 10.2 for a feedback resistor placement.
26	PG	O	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to PGND.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Limits apply over T_J = –40°C to 125°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND, PGND	–0.3	40	V
	VLDOIN to AGND, PGND	–0.3	16	V
	EN to AGND, PGND	–0.3	40	V
	RT to AGND, PGND	–0.3	5.5	V
	FB to AGND, PGND	–0.3	16	V
	PG to AGND, PGND	0	20	V
	PGND to AGND	–1	2	V
Output voltage	VCC to AGND, PGND	–0.3	5.5	V
	SW to AGND, PGND(2)	–0.3	40	V
	VOUT to AGND, PGND	–0.3	6	V
Input current	PG	–	10	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C
T_{stg}	Storage temperature	–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)	3		36	V
Input voltage	VLDOIN			12	V
Output voltage	VOUT(1)	1		6	V
Output current	IOUT(2)	0		3	A
Frequency	F_{SW} set by RT	200		2200	kHz
Input current	PG			2	mA
Output voltage	PG	0		16	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature	–40		105	°C

(1) Under no conditions should the output voltage be allowed to fall below 0 V.
(2) Maximum continuous DC current may be derated when operating with high switching frequency, high ambient temperature, or both. Refer to the *Typical Characteristics* section for details.

6.4 Thermal Information

THERMAL METRIC(1)		TLVM13630 RDH (QFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63603 EVM)	29.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	21.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 64-mm x 83-mm four-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the Layout section.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over I_{OUT} range)	3.95		36	V
		Once operating (over I_{OUT} range)	3		36	V
V_{IN_HYS}	Hysteresis(1)			1.0		V
I_{Q_VIN}	Input operating quiescent current (non-switching)	T_A = 25°C, V_{EN} = 3.3 V, V_{FB} = 1.5 V		4		µA
I_{SDN_VIN}	VIN shutdown quiescent current	V_{EN} = 0 V, T_A = 25°C		3		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			0.91		V
V_{EN_HYS}	EN voltage hysteresis		0.275	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
I_{EN}	Input current into EN (non-switching)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		1.65		µA
t_{EN}	EN HIGH to start of switching delay(1)			0.7		ms
INTERNAL LDO VCC						
V_{CC}	Internal LDO VCC output voltage	3.4 V ≤ V_{LDOIN} ≤ 12.5 V		3.3		V
		V_{LDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{LDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis(2)	Hysteresis below V_{CC_UVLO}		1.1		V
I_{VLDOIN}	Input current into the VLDOIN pin (non-switching, maximum at T_A = 125°C)(3)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		25	31.2	µA
FEEDBACK						
V_{OUT}	Adjustable output voltage range	Over the I_{OUT} range	1		6	V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Over the V_{IN} range, V_{OUT} = 1 V, I_{OUT} = 0 A, F_{SW} = 200 kHz	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 3 A		0.1%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4.0 V ≤ V_{IN} ≤ 36 V		0.1%		
I_{FB}	Input current into the FB pin	V_{FB} = 1.0 V		10		nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		3.0	A
I_{OCL}	Output overcurrent (DC) limit threshold			4.9		A
I_{L_HS}	High-side switch current limit	Duty cycle approaches 0%	5.6	6.2	6.8	A
I_{L_LS}	Low-side switch current limit		2.9	3.4	3.8	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time ("hiccup" time before soft start) (1)			80		ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{REF} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms

6.5 Electrical Characteristics (continued)

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PG_{OV}	PG upper threshold – rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG lower threshold – falling	% of VOUT setting	92%	94%	96.5%	
PG_{HYS}	PG upper threshold hysteresis (rising and falling)	% of VOUT setting		1.3%		
$V_{IN\_PG\_VALID}$	Input voltage for valid PG output	46-µA pullup, V_{EN} = 0 V	1.0			V
V_{PG_LOW}	Low level PG function output voltage	2-mA pullup to the PG pin, V_{EN} = 3.3 V			0.4	V
I_{PG}	Input current into PG pin when open-drain output is high	V_{PG} = 3.3 V		10		nA
I_{OV}	Pulldown current at the SW node under overvoltage condition			0.5		mA
$t_{PG\_FLT\_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG\_FLT\_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by R_T or SYNC		200		2200	kHz
f_{SW_RT1}	Default switching frequency by R_T	R_{RT} = 66.5 kΩ	180	200	220	kHz
f_{SW_RT2}	Default switching frequency by R_T	V_{IN} = 12 V, R_{RT} = 5.76 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off the high-side switch			2.1		V
t_{ON_MIN}	Minimum ON pulse width(1)	V_{OUT} = 1 V, I_{OUT} = 1 A		55	70	ns
t_{ON_MAX}	Maximum ON pulse width(1)			9		µs
t_{OFF_MIN}	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A		65	85	ns
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
T_{HYST}	Thermal shutdown hysteresis (1)			10		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) Production tested with V_{IN} = 3 V
(3) This is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. It does not represent the total input current to the system while regulating. For additional information, reference the *System Characteristics* and the *Input Supply Current* section.

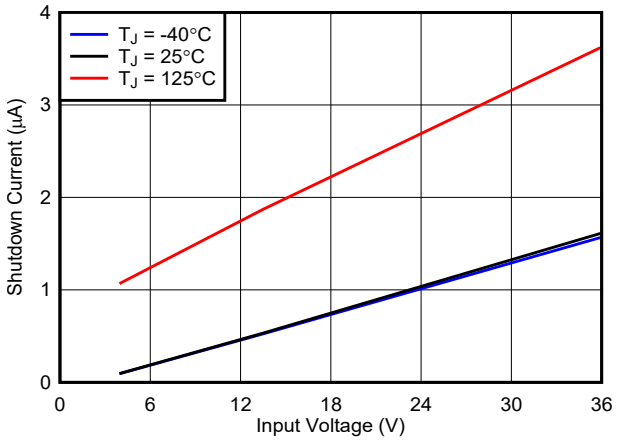
6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{EN} = V_{IN}, V_{VLDOIN} = V_{OUT}, F_{SW} = 800 kHz, I_{OUT} = 0 A		10		mA
OUTPUT VOLTAGE						
V_{FB}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.1 A to full load		1		mV
V_{FB}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 3 A		6		mV
V_{OUT}	Load transient	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 1 A to 2.5 A at 2 A/µs, $C_{OUT(derated)}$ = 49 µF		50		mV
EFFICIENCY						
η	Efficiency	V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 800 kHz		89.5%		
		V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 800 kHz		87.5%		
		V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 1 MHz		91%		
		V_{OUT} = 5 V, V_{IN} = 36 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 1 MHz		88.1%		
		V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 1.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 2 MHz		94.1%		

6.7 Typical Characteristics

V_{IN} = 24 V, unless otherwise specified.



V_{EN} = 0 V

Figure 6-1. Shutdown Supply Current

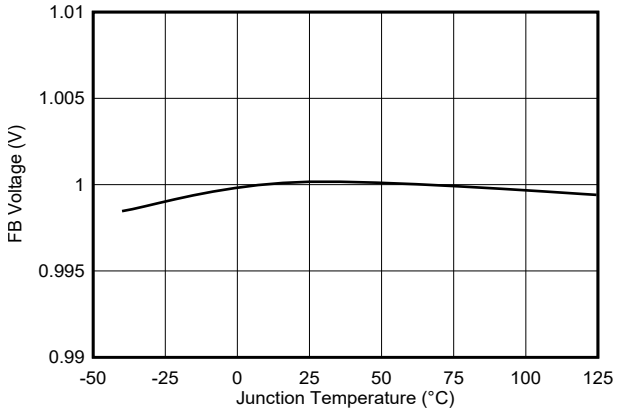


Figure 6-2. Feedback Voltage

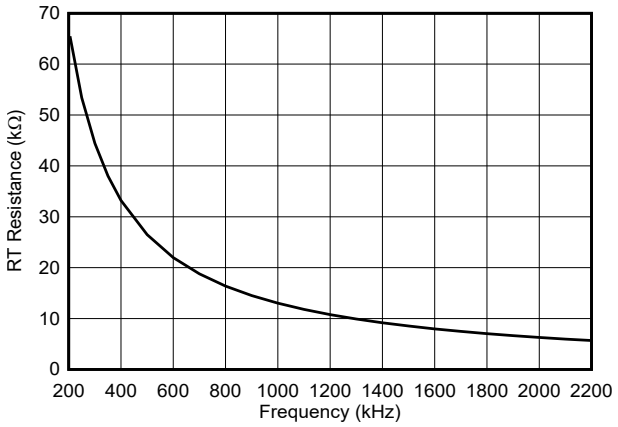


Figure 6-3. Switching Frequency Set by RT Resistor

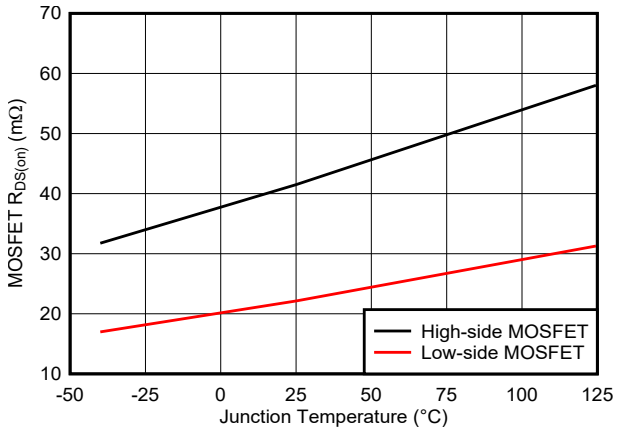


Figure 6-4. High-Side and Low-Side MOSFET $R_{DS(on)}$

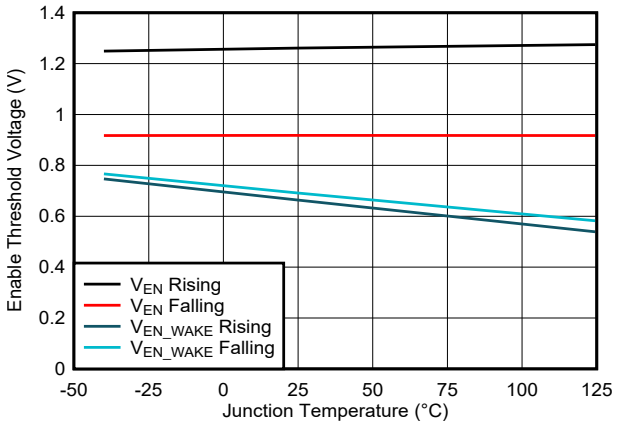


Figure 6-5. Enable Thresholds

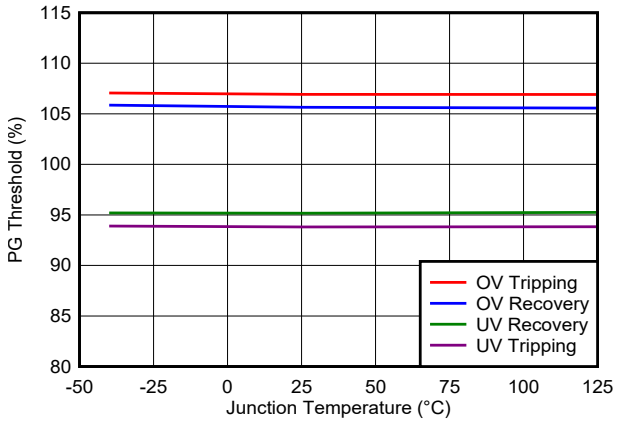
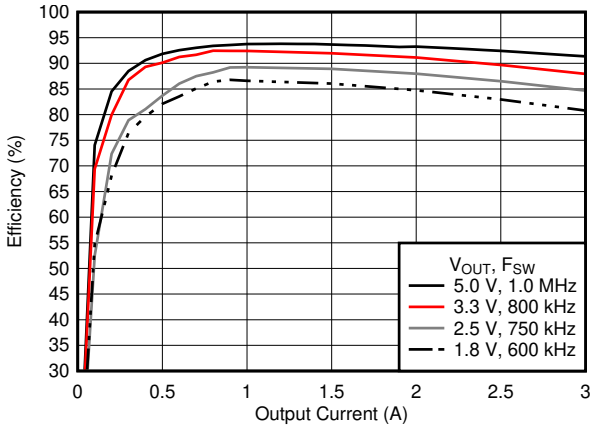


Figure 6-6. Power-Good (PG) Thresholds

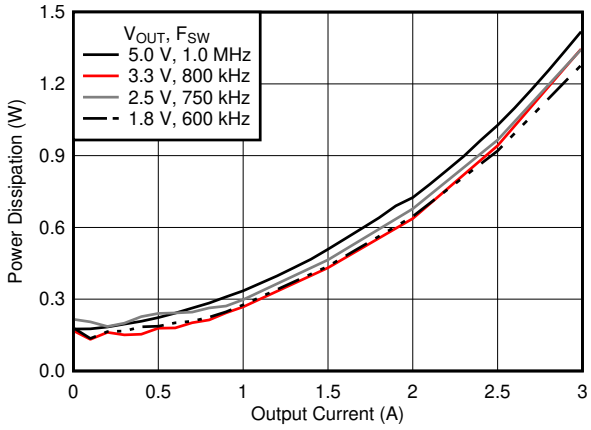
6.8 Typical Characteristics: V_{IN} = 12 V

Refer to Section 8.2 for circuit designs.



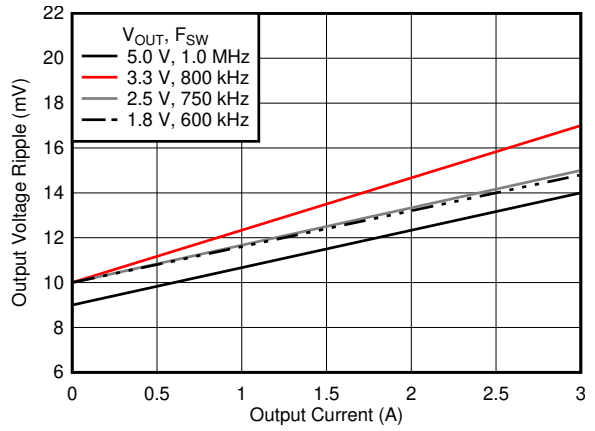
VLDOIN = VOUT

Figure 6-7. Efficiency



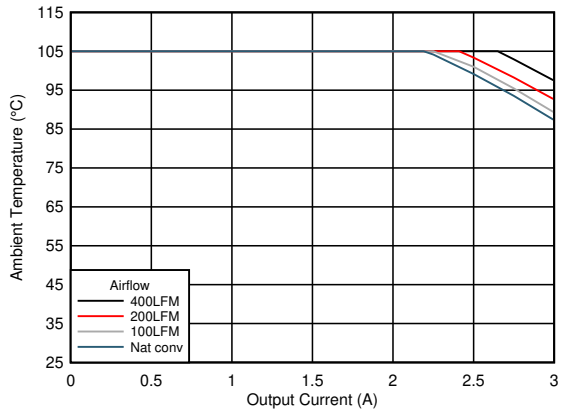
VLDOIN = VOUT

Figure 6-8. Power Dissipation



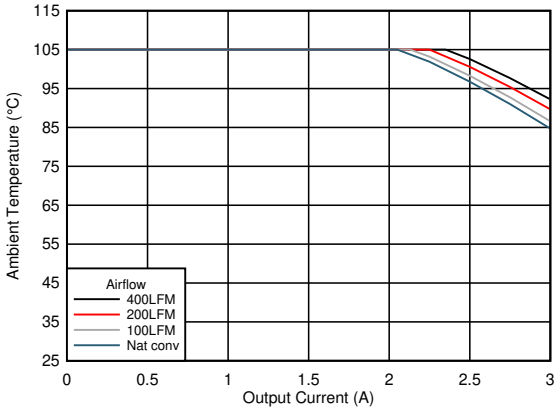
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-9. Output Voltage Ripple



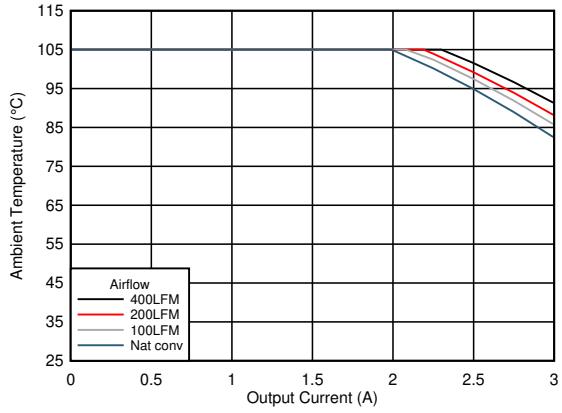
Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-10. Safe Operating Area
V_{OUT} = 1.8 V, F_{SW} = 600 kHz



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-11. Safe Operating Area
V_{OUT} = 3.3 V, F_{SW} = 800 kHz

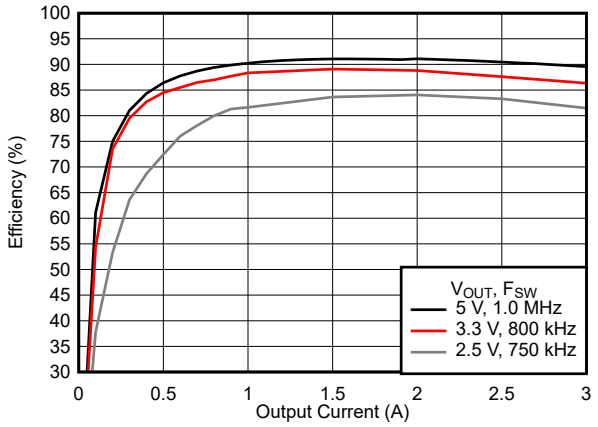


Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-12. Safe Operating Area
V_{OUT} = 5.0 V, F_{SW} = 1 MHz

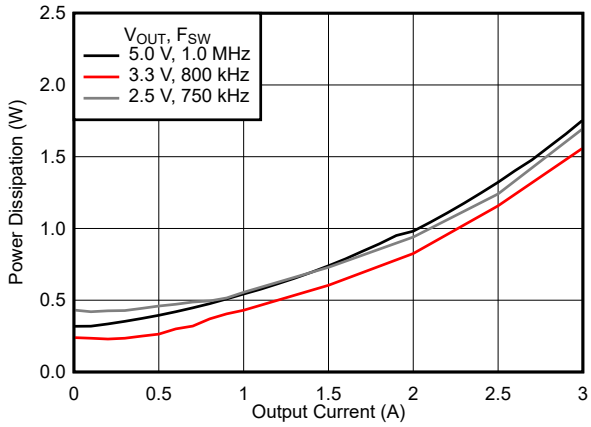
6.9 Typical Characteristics: V_{IN} = 24 V

Refer to Section 8.2 for circuit designs.



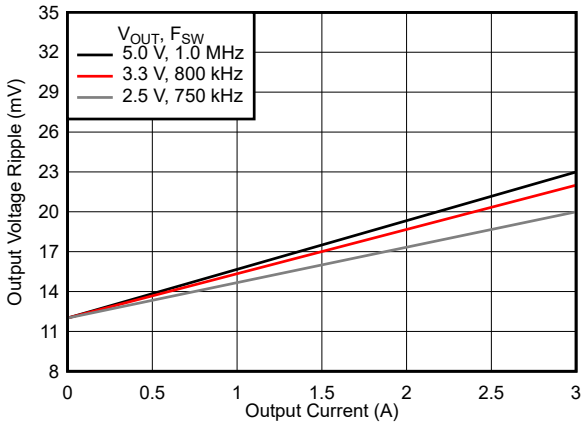
VLDOIN = VOUT

Figure 6-13. Efficiency



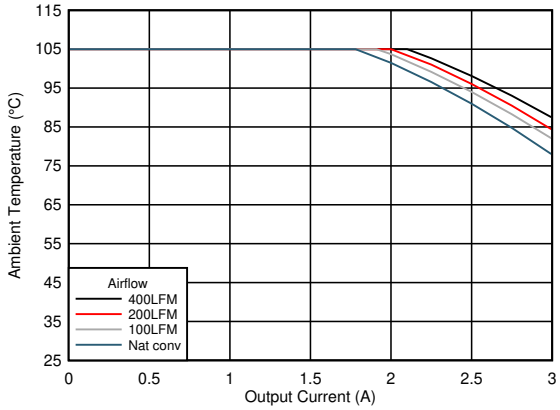
VLDOIN = VOUT

Figure 6-14. Power Dissipation



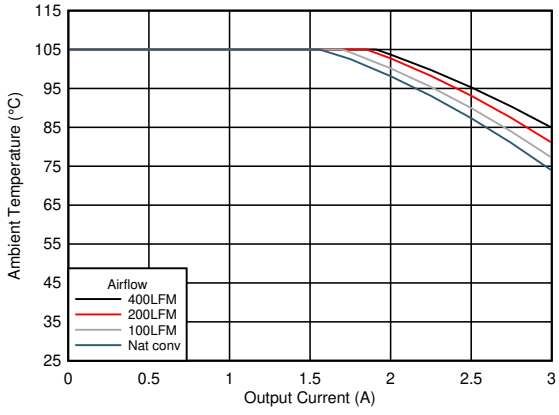
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-15. Output Voltage Ripple



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-16. Safe Operating Area
V_{OUT} = 3.3 V, F_{SW} = 800 kHz

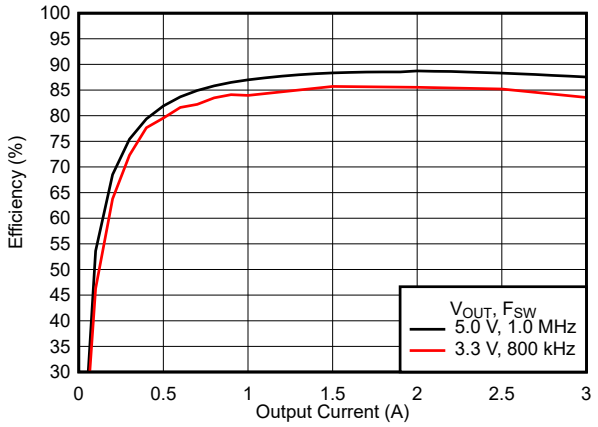


Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-17. Safe Operating Area
V_{OUT} = 5.0 V, F_{SW} = 1 MHz

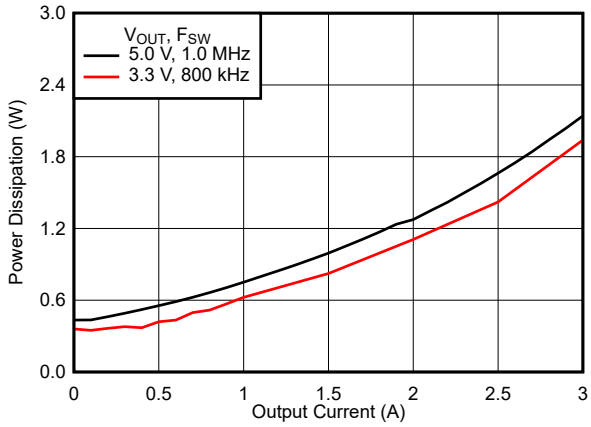
6.10 Typical Characteristics: V_{IN} = 36 V

Refer to Section 8.2 for circuit designs.



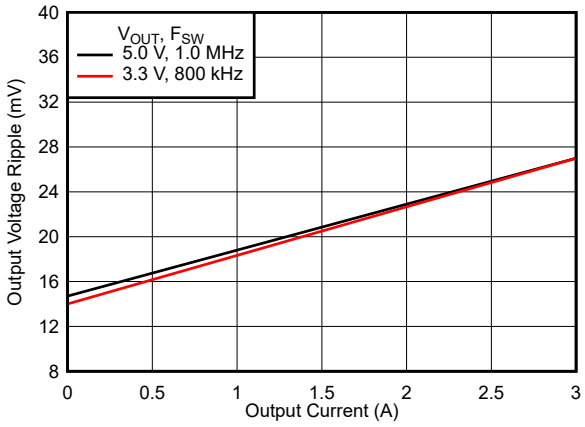
VLDOIN = VOUT

Figure 6-18. Efficiency



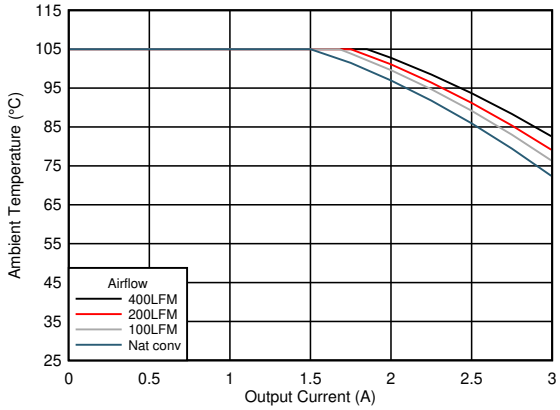
VLDOIN = VOUT

Figure 6-19. Power Dissipation



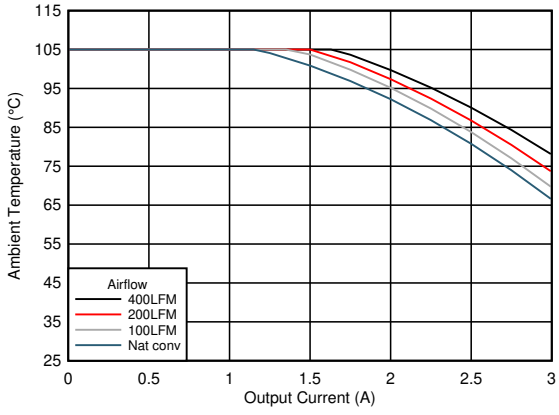
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-20. Output Voltage Ripple



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-21. Safe Operating Area
V_{OUT} = 3.3 V, F_{SW} = 800 kHz



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-22. Safe Operating Area
V_{OUT} = 5.0 V, F_{SW} = 1 MHz

7 Detailed Description

7.1 Overview

The TLVM13630 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, and 24-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TLVM13630 delivers up to 3-A DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin, the TLVM13630 incorporates specific features to improve EMI performance in noise-sensitive applications:

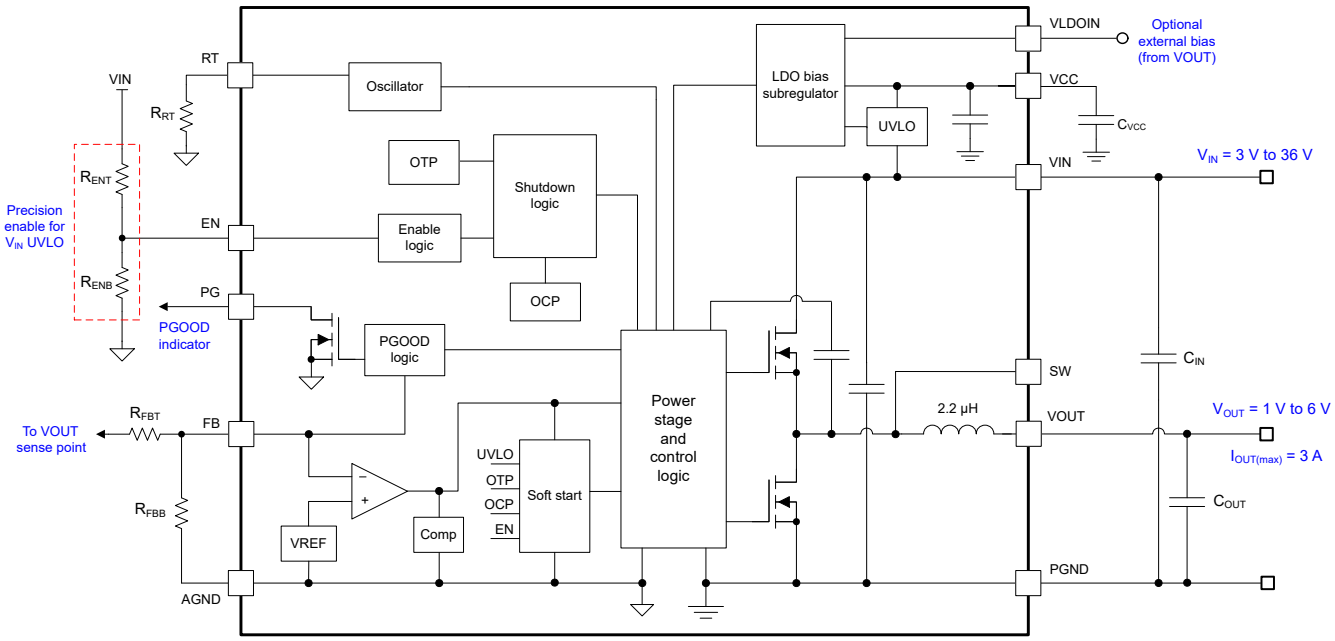
- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching
- Adjustable switch-node slew rate, which allows optimization of EMI at higher frequency harmonics

The TLVM13630 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON/OFF capability
- Internally fixed output-voltage soft start with monotonic startup into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery.

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple layout, requiring few external components. See Section 10 for layout example.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 36 V, the TLVM13630 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in Figure 7-1 shows all the necessary components to implement a TLVM13630-based buck regulator using a single input supply.

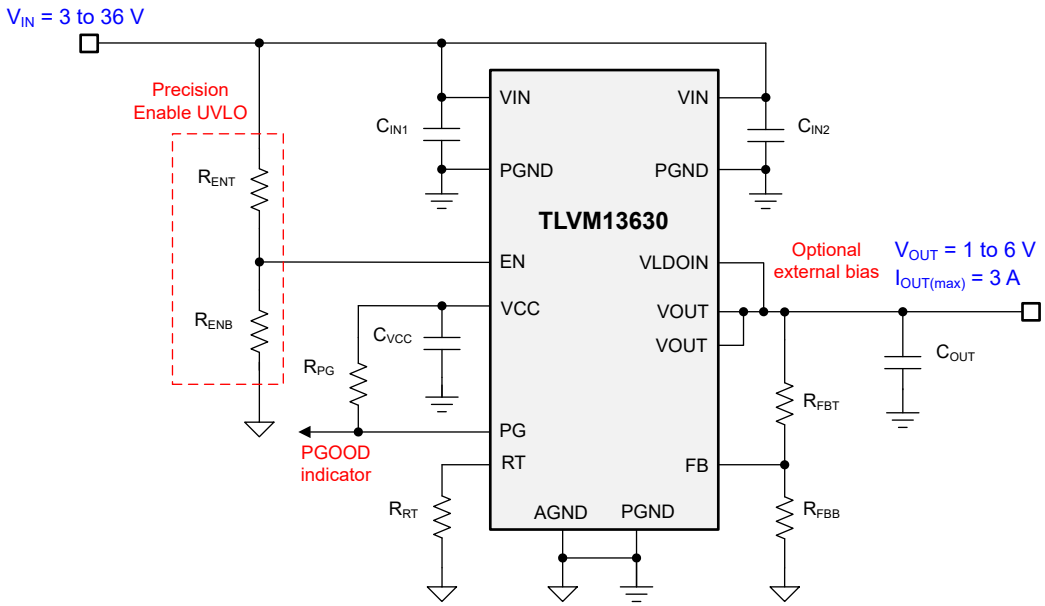


Figure 7-1. TLVM13630 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

Take extra care to make sure that the voltage at the VIN pins of the module does not exceed the absolute maximum voltage rating of 40 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

7.3.2 Adjustable Output Voltage (FB)

The TLVM13630 has an adjustable output voltage range of 1 V to 6 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 7-2). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using Equation 1. Table 7-1 lists the standard resistor values for several output voltages and the recommended switching frequency. The minimum required output capacitance for each output voltage is also included in Table 7-1. The capacitance values listed represent the effective capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (1)$$

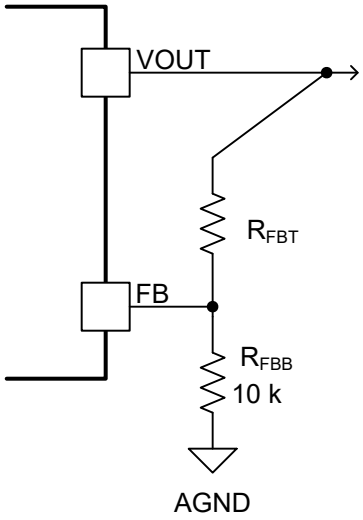


Figure 7-2. FB Resistor Divider

Table 7-1. Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	Short	400	300	2.5	15	750	65
1.2	2	500	200	3.0	20	750	50
1.5	4.99	500	160	3.3	23.2	800	40
1.8	8.06	600	120	5.0	40.2	1000	25
2.0	10	600	100	6.0	49.9	1000	22

(1) R_{FBB} = 10 kΩ.

Note that higher feedback resistances consume less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 10.

7.3.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. Equation 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors should be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \quad (2)$$

where

- $D = V_{OUT} / V_{IN}$ = the module duty cycle

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT} – I_{IN}$) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 3 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (3)$$

Equation 4 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \frac{D \cdot (1 - D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \quad (4)$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TLVM13630 requires a minimum of 2 × 4.7 µF of ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 7-2 includes a preferred list of capacitors by vendor.

Table 7-2. Recommended Input Capacitors

VENDOR(1)	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE RATING (V)	CAPACITANCE (2) (µF)
TDK	X7R	C3216X7R1H475K160AC	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7
TDK	X7R	CGA6P3X7R1H475K250AB	1210	50	4.7
Murata	X7S	GCM31CC71H475KA03L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.4 Output Capacitors

Table 7-1 lists the TLVM13630 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 7-3 for a preferred list of output capacitors by vendor.

Table 7-3. Recommended Output Capacitors

VENDOR(1)	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE(2) (µF)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.5 Switching Frequency (RT)

The switching frequency range of the TLVM13630 is 200 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Use Equation 5 to calculate the R_{RT} value for a desired frequency or simply select from Table 7-4. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization.

The switching frequency must be selected based on the output voltage setting of the device. See Table 7-4 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

$$R_{RT}\left[k\Omega\right] = \frac{13.46}{F_{SW}\left[MHz\right]} - 0.44 \quad (5)$$

Table 7-4. Switching Frequency Versus Output Voltage (I_{OUT} = A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
200	66.5	1.0	2.0	1.0	2.0	1.0	1.5	1.0	1.5
400	33.2	1.0	3.0	1.0	4.0	1.0	3.3	1.2	3.0
600	22.1	1.0	3.5	1.0	6.0	1.5	6.0	1.8	5.0
800	16.5	1.0	3.5	1.0	6.0	1.5	6.0	2.5	6.0
1000	13.0	1.0	3.0	1.0	6.0	2.0	6.0	3.0	6.0
1200	10.7	1.0	3.0	1.5	6.0	2.5	6.0	3.5	6.0
1400	9.09	1.0	3.0	1.5	6.0	3.0	6.0	4.0	6.0
1600	8.06	1.0	3.0	1.5	6.0	3.0	6.0	4.5	6.0
1800	6.98	1.0	3.0	2.0	6.0	3.5	6.0	5.0	6.0
2000	6.34	1.2	2.5	2.0	6.0	4.0	6.0	5.5	6.0
2200	5.626	1.2	2.5	2.0	6.0	4.5	6.0	-	-

7.3.6 Output ON/OFF Enable (EN) and V_{IN} UVLO

The EN pin provides precision ON and OFF control for the TLVM13630. Once the EN/SYNC pin voltage exceeds the threshold voltage and V_{IN} is above the minimum turn-on threshold, the device starts operation. The simplest way to enable the TLVM13630 is to connect EN directly to VIN. This allows the TLVM13630 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the employment of an enable divider network as shown in Figure 7-3, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

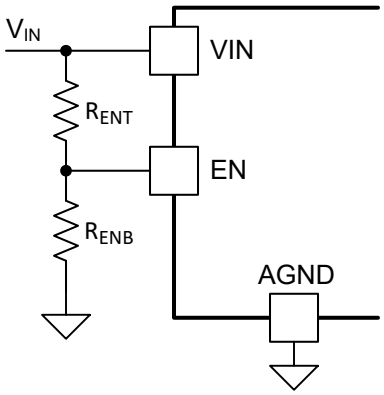


Figure 7-3. VIN UVLO Using the EN Pin

R_{ENB} can be calculated using Equation 6.

$$R_{ENB}\left[k\Omega\right] = R_{ENT}\left[k\Omega\right] \cdot \left(\frac{V_{EN\_RISE}\left[V\right]}{V_{IN(on)}\left[V\right] - V_{EN\_RISE}\left[V\right]} \right) \quad (6)$$

where

- A typical value for R_{ENT} is 100 kΩ.
- V_{EN} is 1.263 V (typical).
- $V_{IN(ON)}$ is the desired start-up input voltage.

7.3.7 Power Good Monitor (PG)

The TLVM13630 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. The PGOOD pin voltage goes low when the feedback voltage is outside of the PGOOD thresholds. This occurs during the following:

- While the device is disabled
- In current limit
- In thermal shutdown
- During normal start-up, when the output voltage has not reach its regulation value

A glitch filter prevents false flag operation for short excursions (<120 µs typical) of the output voltage, such as during line and load transients.

PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 20 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in Figure 7-4, or for fault protection and output monitoring.

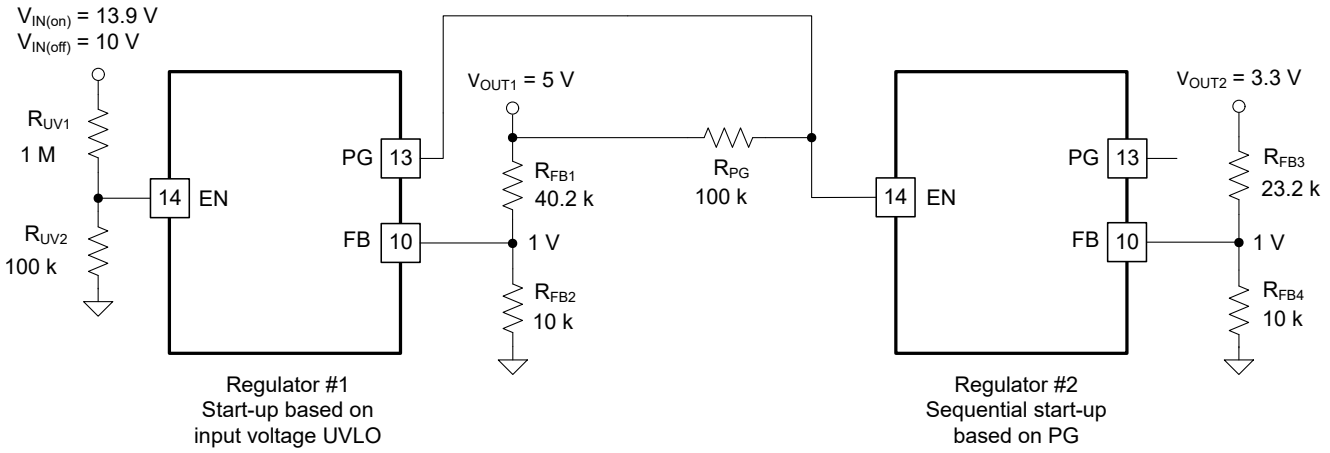


Figure 7-4. TLVM13630 Sequencing Implementation Using PG and EN

7.3.8 Internal LDO, VCC Output, and VLDOIN Input

The TLVM13630 has an internal LDO to power internal circuitry. The VCC pin is the output of the internal LDO. This pin must not be used to power external circuitry. Connect a high-quality, 1-µF capacitor from this pin to AGND, close to the device pins. Do not load the VCC pin or short it to ground.

The VLDOIN pin is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity.

The LDO generates the VCC voltage from one of the two inputs: V_{IN} or the VLDOIN input. When VLDOIN is tied to ground or below 3.1 V, the LDO is powered from V_{IN}. When VLDOIN is tied to a voltage higher than 3.1 V, the LDO input is powered from VLDOIN. VLDOIN voltage must be lower than both V_{IN} and 12.5 V.

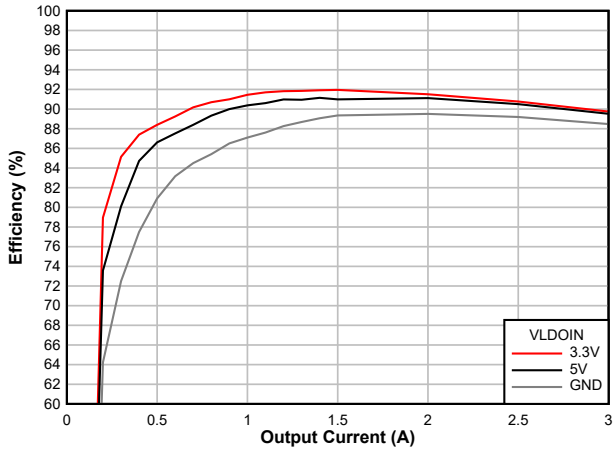
The VLDOIN input is designed to reduce the LDO power loss. The LDO power loss is:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\_LDO} - V_{VCC}) \quad (7)$$

The higher the difference between the input and output voltages of the LDO, the more loss occurs to supply the same LDO output current. The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, to reduce the difference of the input and output voltages of the LDO and reduce power loss. For example, if the LDO current is 10 mA at a certain frequency with V_{IN} = 24 V and V_{OUT} = 5 V. The LDO loss with VLDOIN tied to ground is equal to 10 mA × (24 V – 3.3 V) = 207 mW, while the loss with VLDOIN tied to V_{OUT} (5 V) is equal to 10 mA × (5 V – 3.3 V) = 17 mW.

The efficiency improvement is more significant at light and mid loads because the LDO loss is a higher percentage of the total loss. The improvement is more significant with higher switching frequency because the LDO current is higher at higher switching frequency. The improvement is more significant when V_{IN} » V_{OUT} because the voltage difference is higher.

Figure 7-5 shows typical efficiency waveforms with VLDOIN powered by different input voltages.



V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
I_{LDO} = 10 mA

Figure 7-5. Efficiency improvements with VLDOIN (VOUT = 5 V)

7.3.9 Overcurrent Protection (OCP)

The TLVM13630 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TLVM13630 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the regulator is shut down and kept off for 80 ms (typical) before the TLVM13630 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TLVM13630 attempts to restart when the junction temperature falls to 158°C (typical).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN/SYNC pin provides ON and OFF control for the TLVM13630. When V_{EN} is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The input quiescent current in shutdown mode drops to 0.6 µA (typical). The TLVM13630 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until $V_{EN/SYNC}$ rises above the precision enable threshold.

7.4.3 Active Mode

The TLVM13630 is in active mode when V_{IN} and V_{EN} are above their relevant thresholds and no fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLVM13630 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. The following section describes the design procedure to configure the TLVM13630 power module. To expedite and streamline the design process, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases.

As mentioned previously, the TLVM13630 also integrates several optional features to meet system design requirements, including the following:

- Precision enable with hysteresis
- External adjustable UVLO
- Adjustable SW node slew rate
- Power-good indicator

The following application circuit detailed shows the TLVM13630 configuration options suitable for several application use cases.

8.2 Typical Applications

The following are sample typical applications along with design procedure for the implemenation of TLVM13630.

8.2.1 Design 1: 3-A Synchronous Buck Regulator for Industrial Applications

Figure 8-1 shows the schematic diagram of a 5-V, 3-A buck regulator with a switching frequency of 1 MHz. The nominal input voltage for the sample design is 24 V. A resistor R_{RT} of 13 kΩ sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency for this specific application.

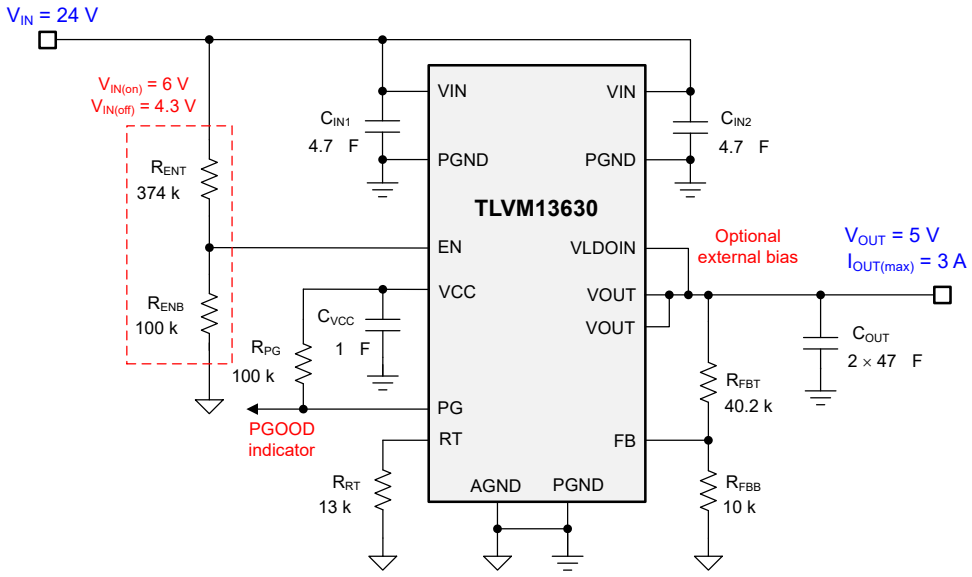


Figure 8-1. Circuit Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters and follow the design procedures in Section 8.2.1.2.

Table 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage	24 V
Output voltage	5 V
Output current	0 A to 3 A
Switching Frequency	1 MHz

Table 8-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 8-2. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{IN1}, C_{IN2}	2	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 100 V, X7S, 1206, ceramic	Murata	GRM31CC72A475KE11L
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
		1 µF, 16 V, X5R, 0402, ceramic	Taiyo Yuden	EMK105BJ105KVHF
U_1	1	TLVM13630 36-V, 3-A synchronous buck module	Texas Instruments	TLVM13630RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TLVM13630 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Setpoint

The output voltage of the TLVM13630 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBB} can be selected from Table 7-1 or calculated using Equation 8:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (8)$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

8.2.1.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 7-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND.

8.2.1.2.4 Input Capacitor Selection

The TLVM13630 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, select two 4.7-µF, 50-V, 1210 case size, ceramic capacitors.

8.2.1.2.5 Output Capacitor Selection

For a 5-V output, the TLVM13630 requires a minimum of 25 µF of effective output capacitance for proper operation (see Table 7-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

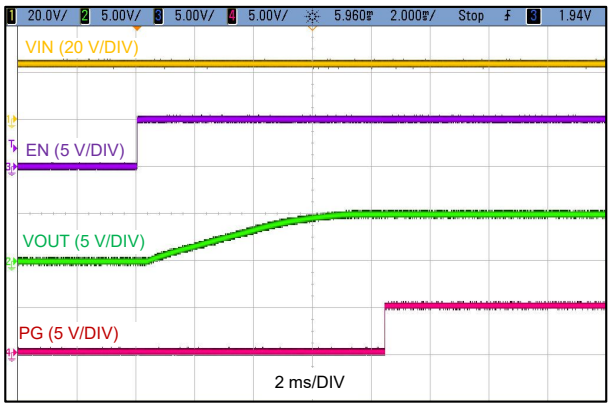
For this design example, select two 47-µF, 10-V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 48 µF at 5 V.

8.2.1.2.6 Other Connections

- Connect VLDOIN to VOUT to improve efficiency.
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

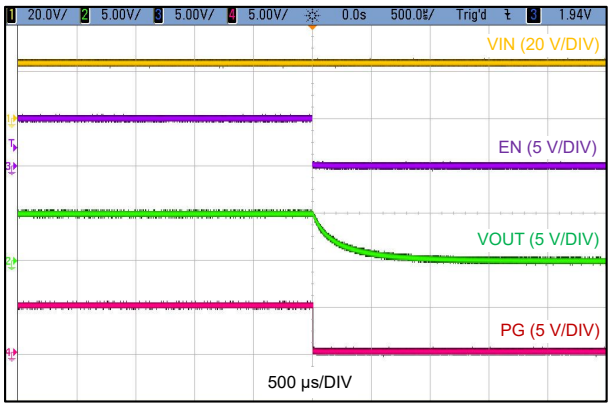
8.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 3 A, and F_{SW} = 1 MHz.



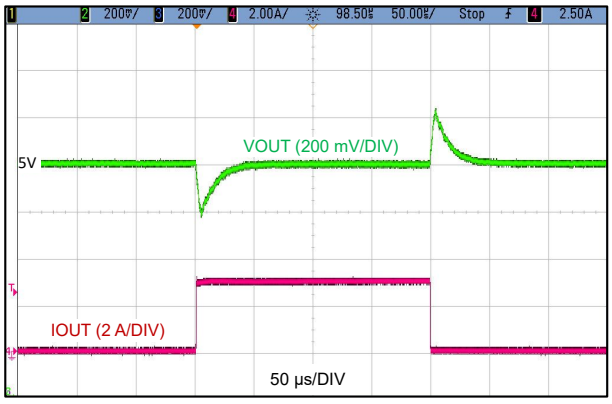
V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-2. Start-Up Waveforms



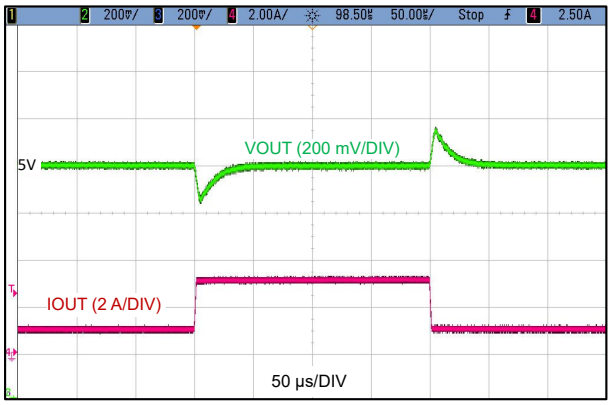
V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-3. Shutdown Waveforms



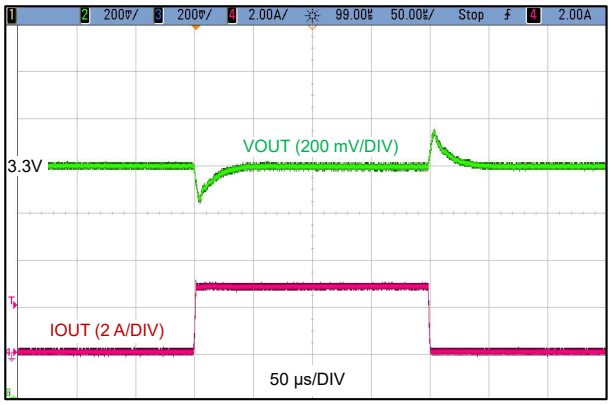
V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-4. Load Transient 0 A to 3 A, 1 A/µs



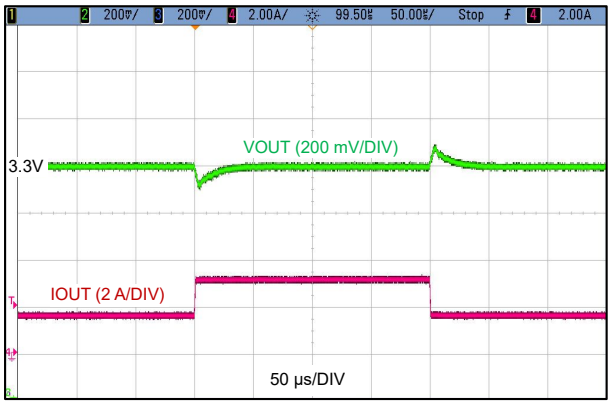
V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-5. Load Transient 1.5 A to 3 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-6. Load Transient 0 A to 3 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-7. Load Transient 1.5 A to 3 A, 1 A/µs

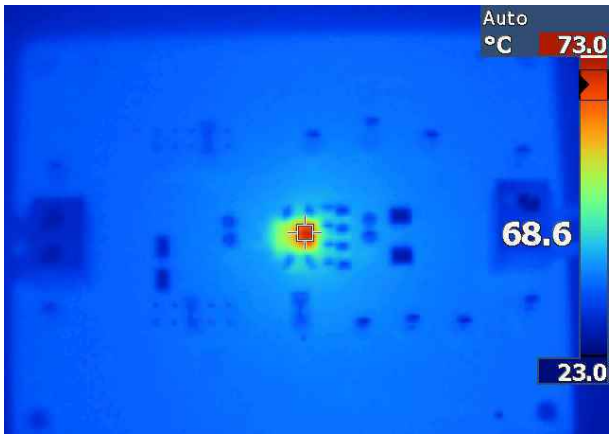


Figure 8-8. Thermal Image V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

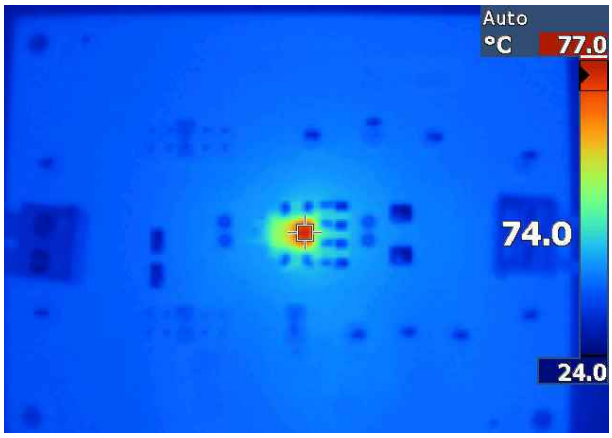


Figure 8-9. Thermal Image V_{IN} = 12 V, V_{OUT} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

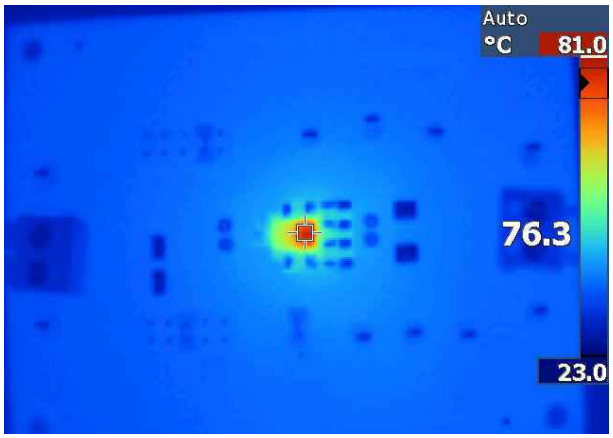


Figure 8-10. Thermal Image V_{IN} = 24 V, V_{OUT} = 3.3 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

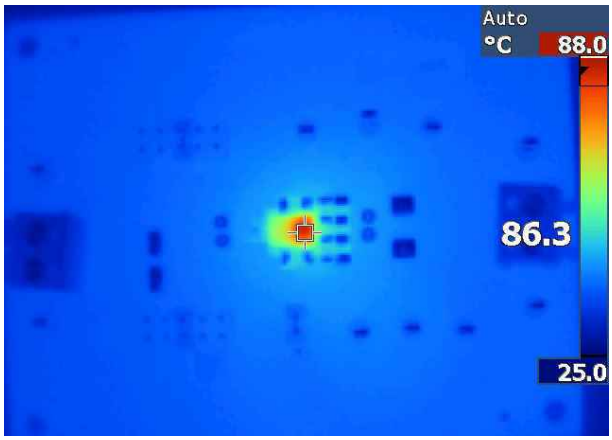


Figure 8-11. Thermal Image V_{IN} = 24 V, V_{OUT} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

8.2.2 Design 2: Inverting Buck-Boost Regulator with a –5-V Output

Figure 8-12 shows the schematic diagram of a –5-V inverting buck-boost regulator with a switching frequency of 1 MHz. The input voltage range for the sample design is 12 V to 24 V.

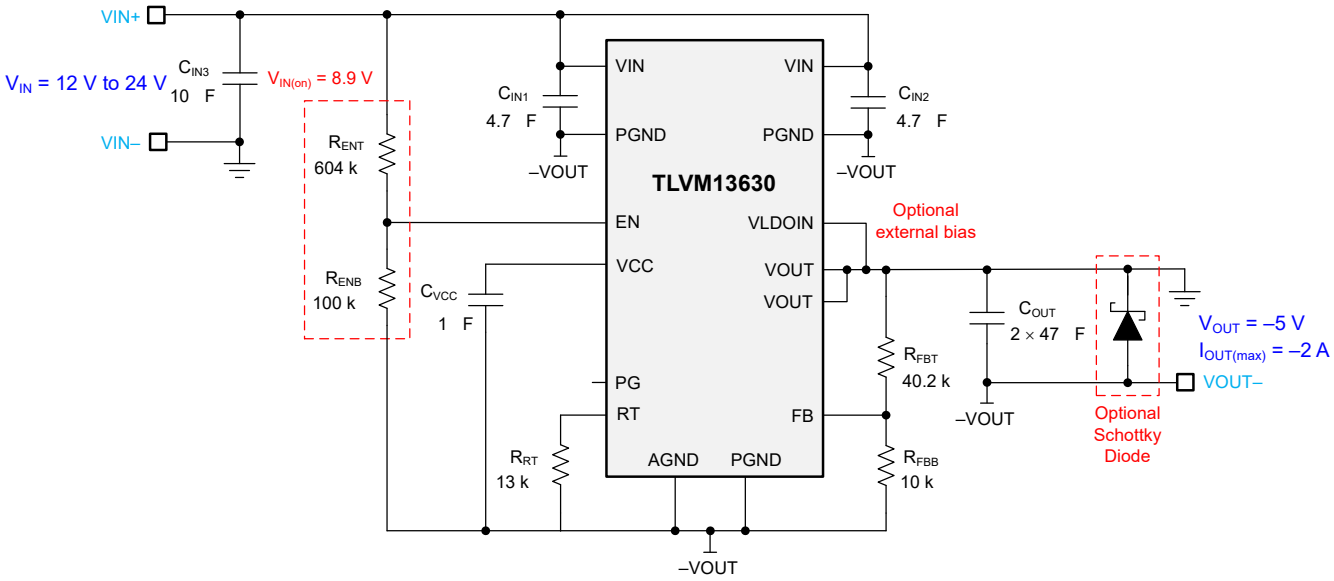


Figure 8-12. Circuit Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-3 as the input parameters and follow the design procedures in Section 8.2.2.2.

Table 8-3. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage	12 to 24 V
Output voltage	–5 V
Output current	0 A to 2 A
Switching frequency	1 MHz

Table 8-4 gives the selected module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 8-4. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{IN1}, C_{IN2}, C_{IN3}	3	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 50 V, X7S, 1206, ceramic	Murata	GCM31CC71H475KA03K
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
U_1	1	TLVM13630 36-V, 3-A synchronous buck module	Texas Instruments	TLVM13630RDLR

More generally, the TLVM13630 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Setpoint

The output voltage of the TLVM13630 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. Calculate the value for R_{FBT} using Equation 9:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \tag{9}$$

For the desired output voltage of – 5 V, enter the absolute value of 5 V for the V_{OUT} in Equation 9. The formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

8.2.2.2.2 IBB Maximum Output Current

The achievable output current with an *IBB topology* using the TLVM13630 is $I_{OUT(max)} = I_{LDC(max)} \times (1 – D)$, where $I_{LDC(max)}$ = 3 A is the rated current of the module and $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the module duty cycle. Therefore in the case of V_{IN} = 12 V and the V_{OUT} = –5 V, the maximum output current is 2.1 A.

8.2.2.2.3 Switching Frequency Selection

To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND pins of the module based on Equation 5.

8.2.2.2.4 Input Capacitor Selection

The TLVM13630 requires a minimum input capacitance of 2 × 4.7-µF ceramic type between the VIN pins and PGND pins as close as possible to the module. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. In the inverting buck-boost configuration the maximum voltage between VIN and PGND pin of the module is equal to $V_{IN} + |V_{OUT}|$.

For this design, two 4.7-µF, 50-V, 1210 case size, ceramic capacitors are selected.

8.2.2.2.5 Output Capacitor Selection

The TLVM13630 requires a minimum of 25 µF of effective output capacitance for proper operation. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, a two 47-µF, 10-V, 1210 case size, ceramic capacitors are used which have a total effective capacitance of approximately 48 µF at 5 V.

8.2.2.2.6 Other Connections

Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

The right-half-plane zero of an IBB topology is at its lowest frequency at minimum input voltage. However, it does not appear at low frequency for a –5 V output and thus has minimal effect on the loop response for this application.

In the inverting buck-boost configuration, the input capacitor C_{IN} and output capacitor C_{OUT} can formed an AC capacitive divider during a fast V_{IN} transient or hot-plugged event at the input. This event will resulted in a positive voltage spike at the output that may disturb the load. In this case, an optional Schottky diode may be installed between –VOUT and GND as shown in Figure 8-12 to clamp the output spike.

8.2.2.3 Application Curves

Unless otherwise indicated, V_{IN} = 12 V, V_{OUT} = –5 V, and F_{SW} = 1 MHz.

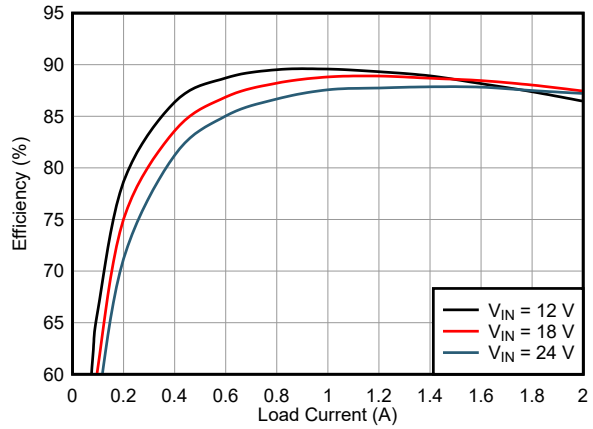


Figure 8-13. Efficiency Curves

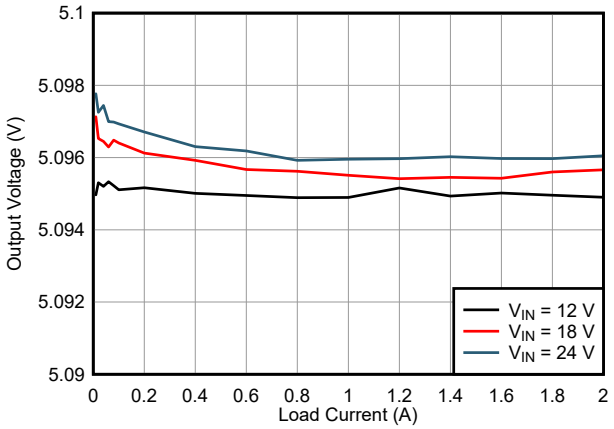
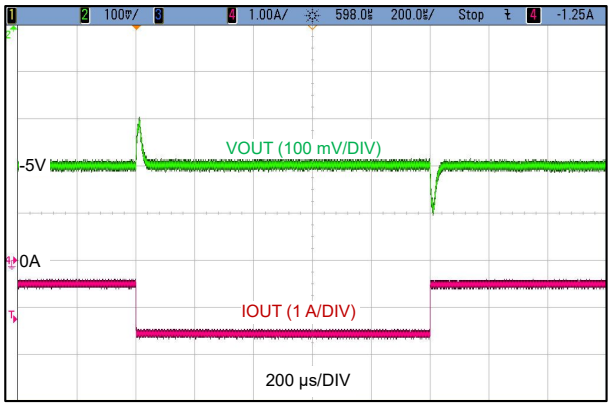
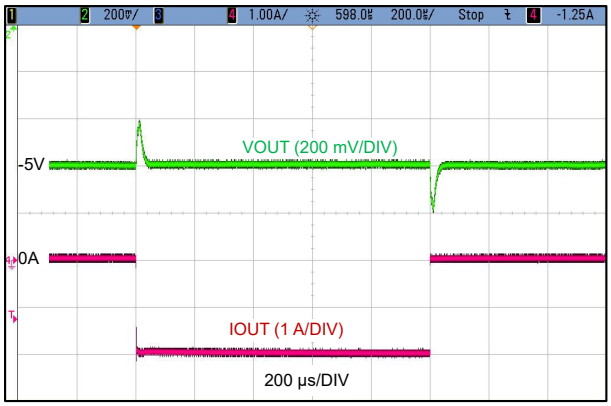


Figure 8-14. Load Regulation



V_{IN} = 12 V V_{OUT} = –5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 8-15. Load Transient –0.5 A to –1.5 A, 1 A/µs



V_{IN} = 12 V V_{OUT} = –5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 8-16. Load Transient 0 A to –2 A, 1 A/µs

8.2.2.3.1 EMI

The TLVM13630 is compliant with EN55011 radiated emissions. Figure 8-17, Figure 8-18, and Figure 8-19 show typical examples of radiated emission plots for the TPSM63603 which is in the same family of parts. The graphs include the plots of the antenna in the horizontal and vertical positions.

8.2.2.3.1.1 EMI Plots

EMI plots were measured using the standard TPSM63603EVM.

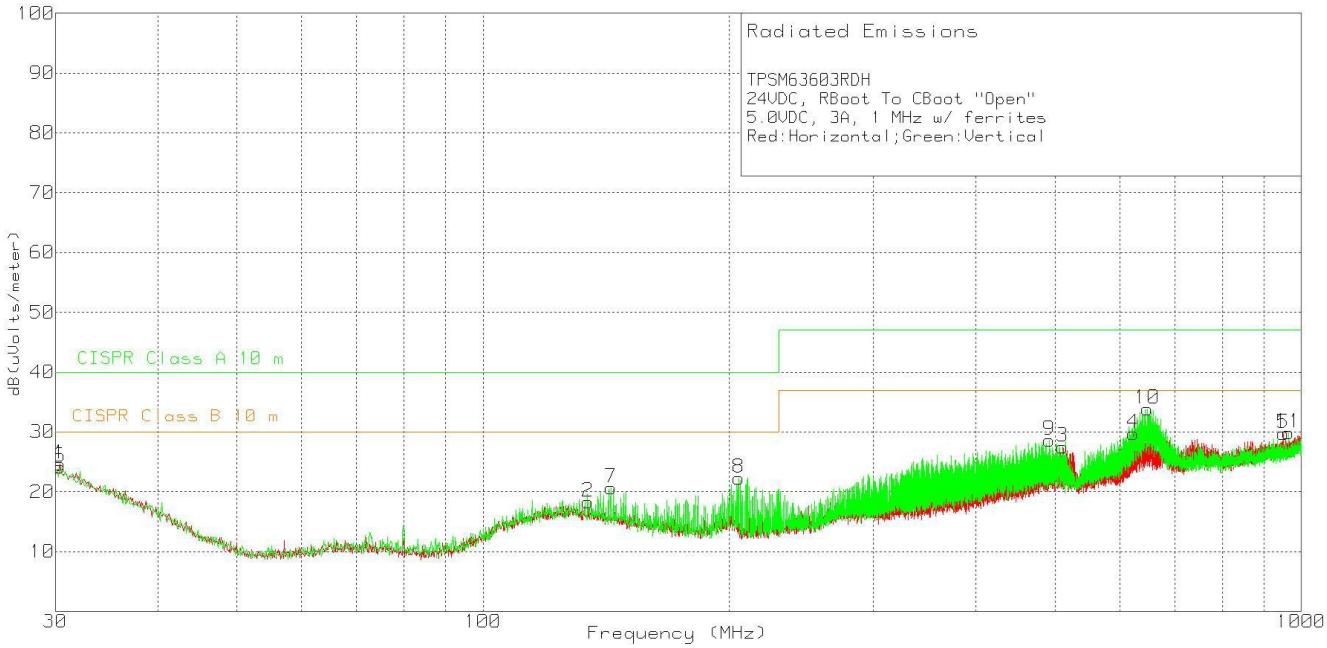


Figure 8-17. Radiated Emissions 24-V Input, 5-V Output, 3-A Load

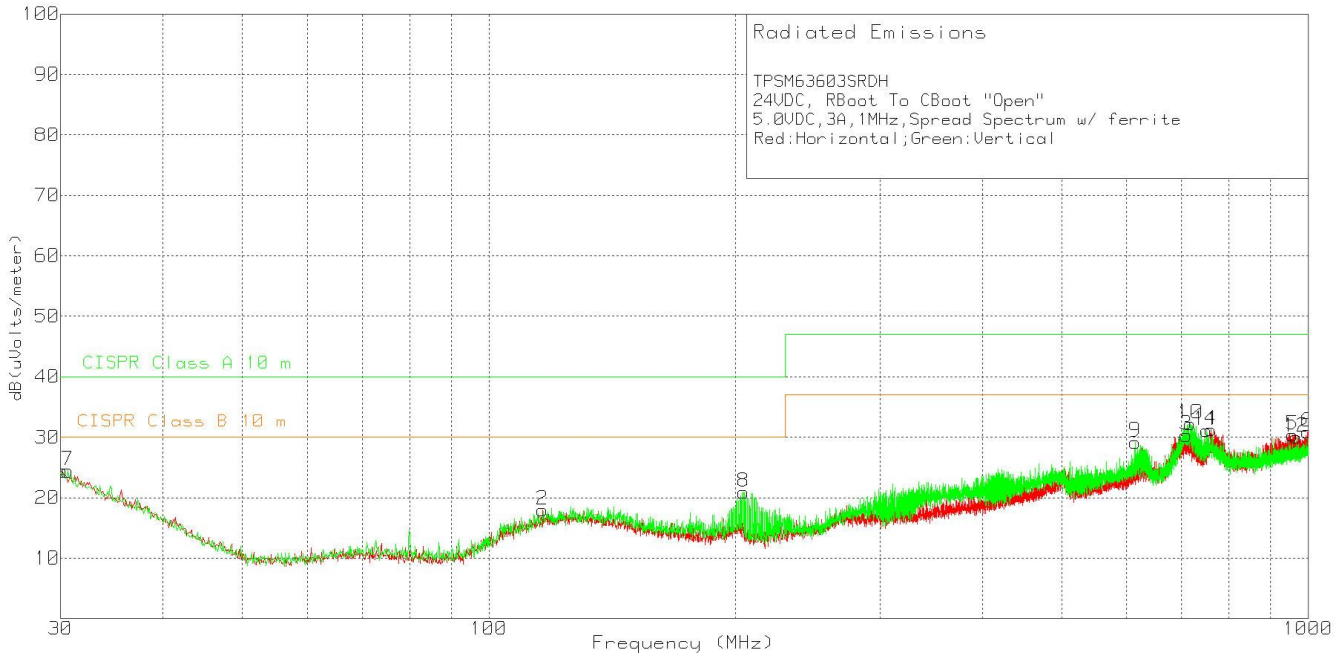


Figure 8-18. Radiated Emissions 24-V Input, 5-V Output, 3-A Load, Spread Spectrum

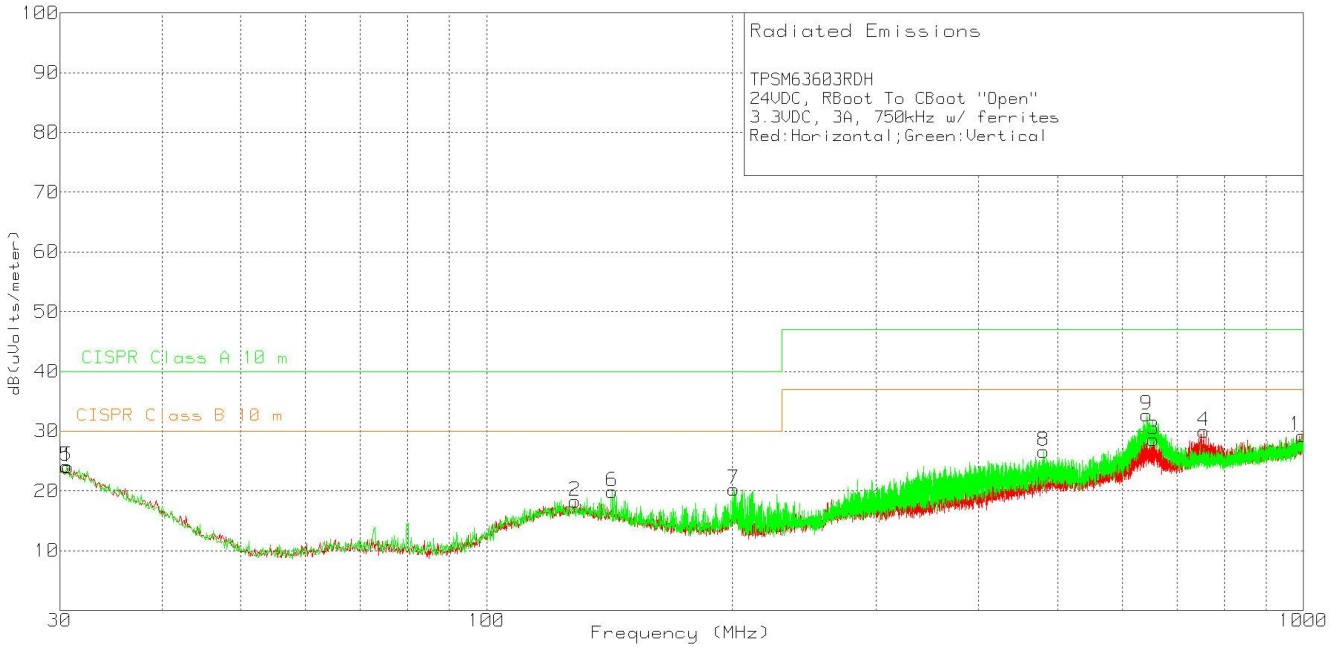


Figure 8-19. Radiated Emissions 24-V Input, 3.3-V Output, 3-A Load

9 Power Supply Recommendations

The TLVM13630 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 10.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \ \eta} \tag{10}$$

where

- η = efficiency

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 10-1 and Figure 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high-frequency noise.
- Locate additional output capacitors between the ceramic capacitors and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

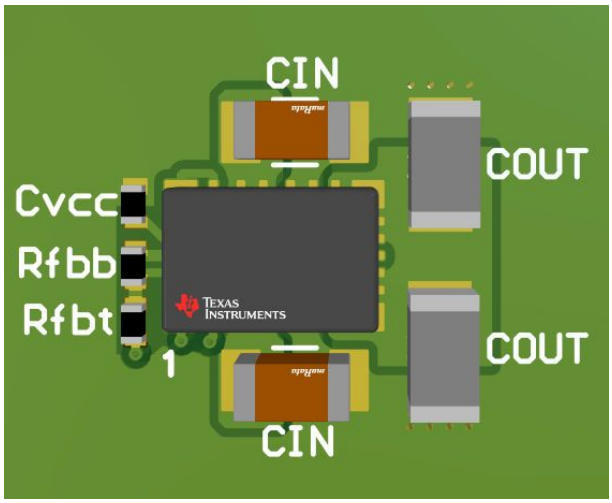


Figure 10-1. Typical Top-Layer Layout

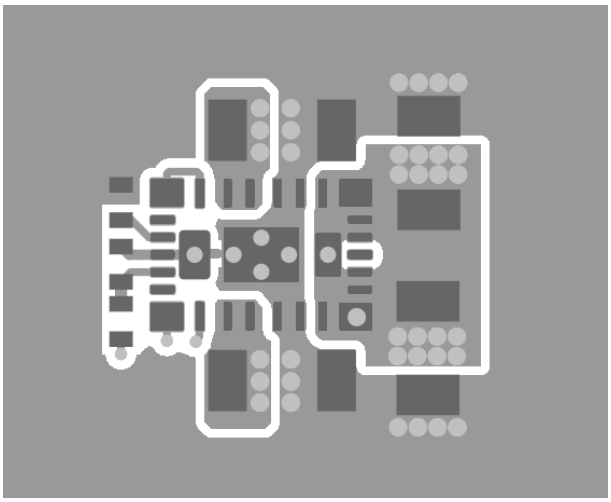


Figure 10-2. Typical Top-Layer

10.2.1 Package Specifications

Table 10-1. Package Specifications Table

TPSM63603		VALUE	UNIT
Weight		123	mg
Flammability	Meets UL 94 V-0		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	84	MHrs

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current from 2 A to 6 A, the TLVM13620/30/40/60 family of synchronous buck power modules specified in Table 11-1 provides flexibility, scalability and optimized solution size for a range of applications. These modules enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include RBOOT-configured switch-node slew rate control, fixed switching frequency, and integrated input bypass capacitors. All modules are rated for an ambient temperature up to 105°C.

Table 11-1. Synchronous Buck DC/DC Power Module Family

DC/DC MODULE	RATED I_{OUT}	PACKAGE	DIMENSIONS	FEATURES	EMI MITIGATION
TLVM13620	2 A	B0QFN (30)	4.0 × 6.0 × 1.8 mm	RT adjustable F_{SW}, precision enable	Integrated BOOT capacitor
TLVM13630	3 A				
TLVM13640	4 A	B3QFN (20)	5.0 × 5.5 × 4.0 mm		Integrated input, VCC and BOOT capacitors
TLVM13660	6 A				

For development support see the following:

- TLVM13630 *Quickstart Calculator*
- TLVM13630 *Simulation Models*
- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.

- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLVM13630RDHR	ACTIVE	B0QFN	RDH	30	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLVM13630RDHR	ACTIVE	B0QFN	RDH	30	3000	RoHS Exempt & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	13630	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

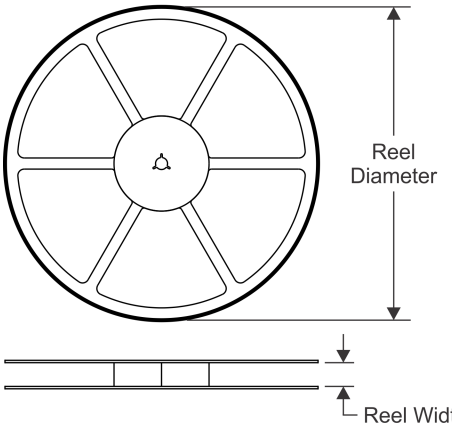
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

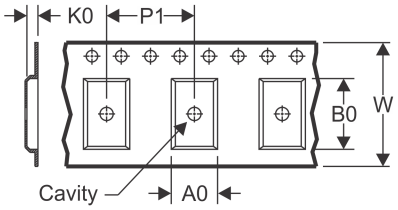
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

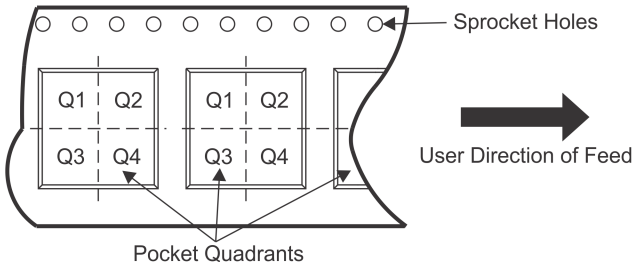


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

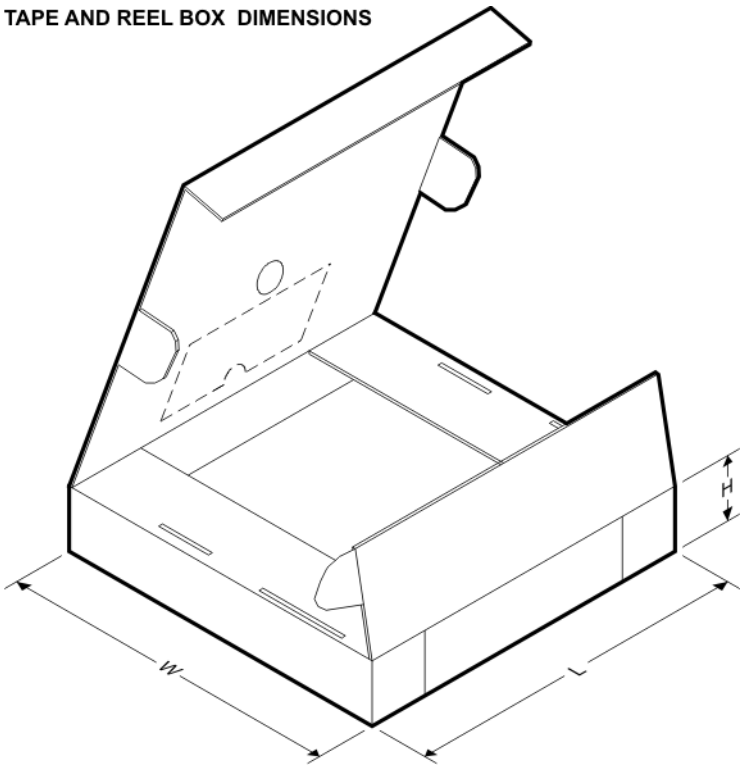
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLVM13630RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

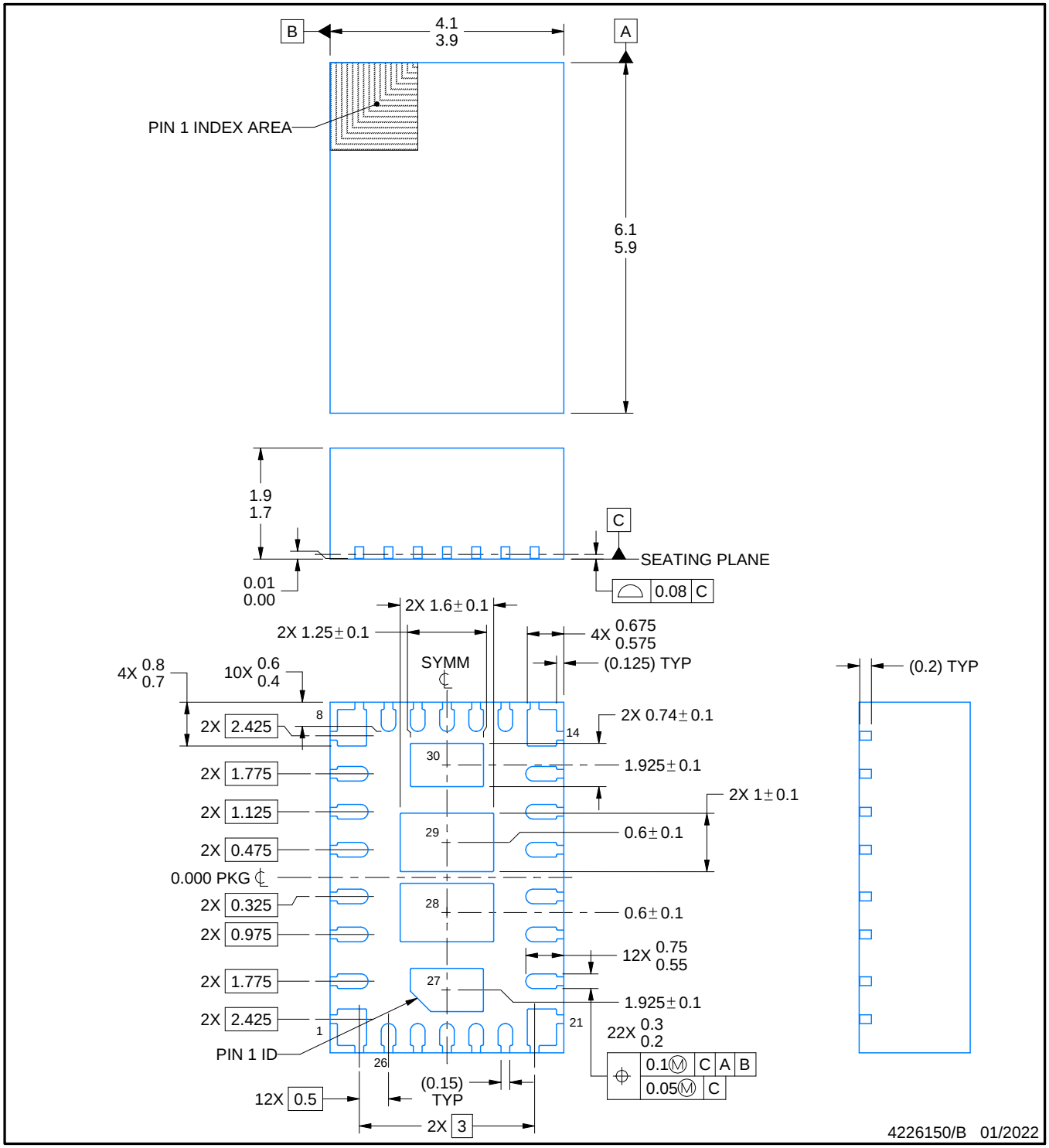
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLVM13630RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDH0030A

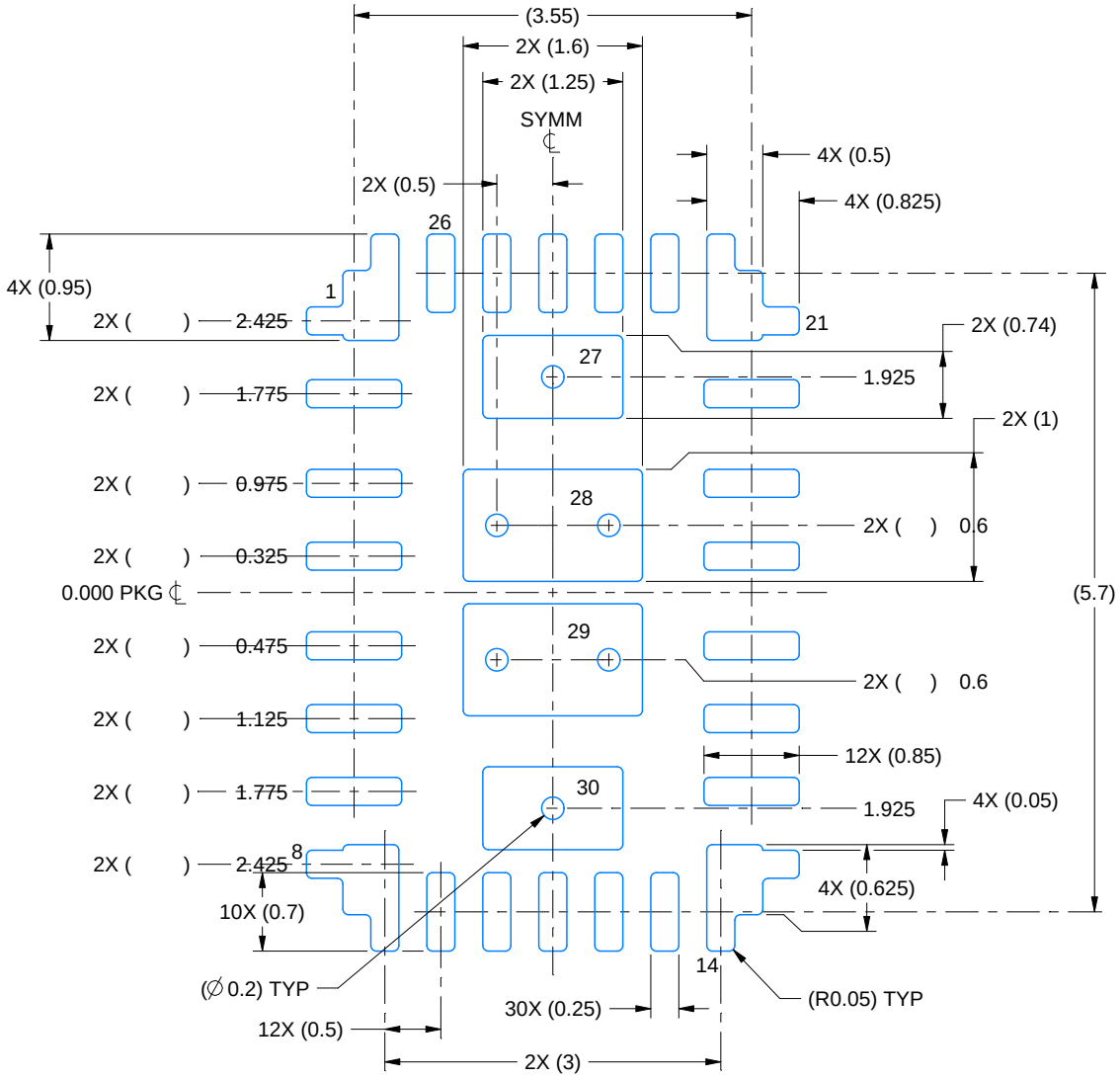
B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

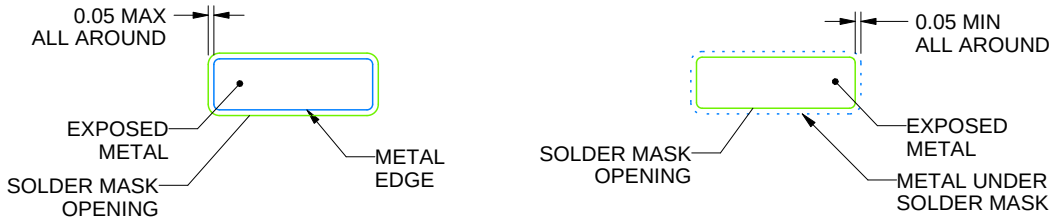


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

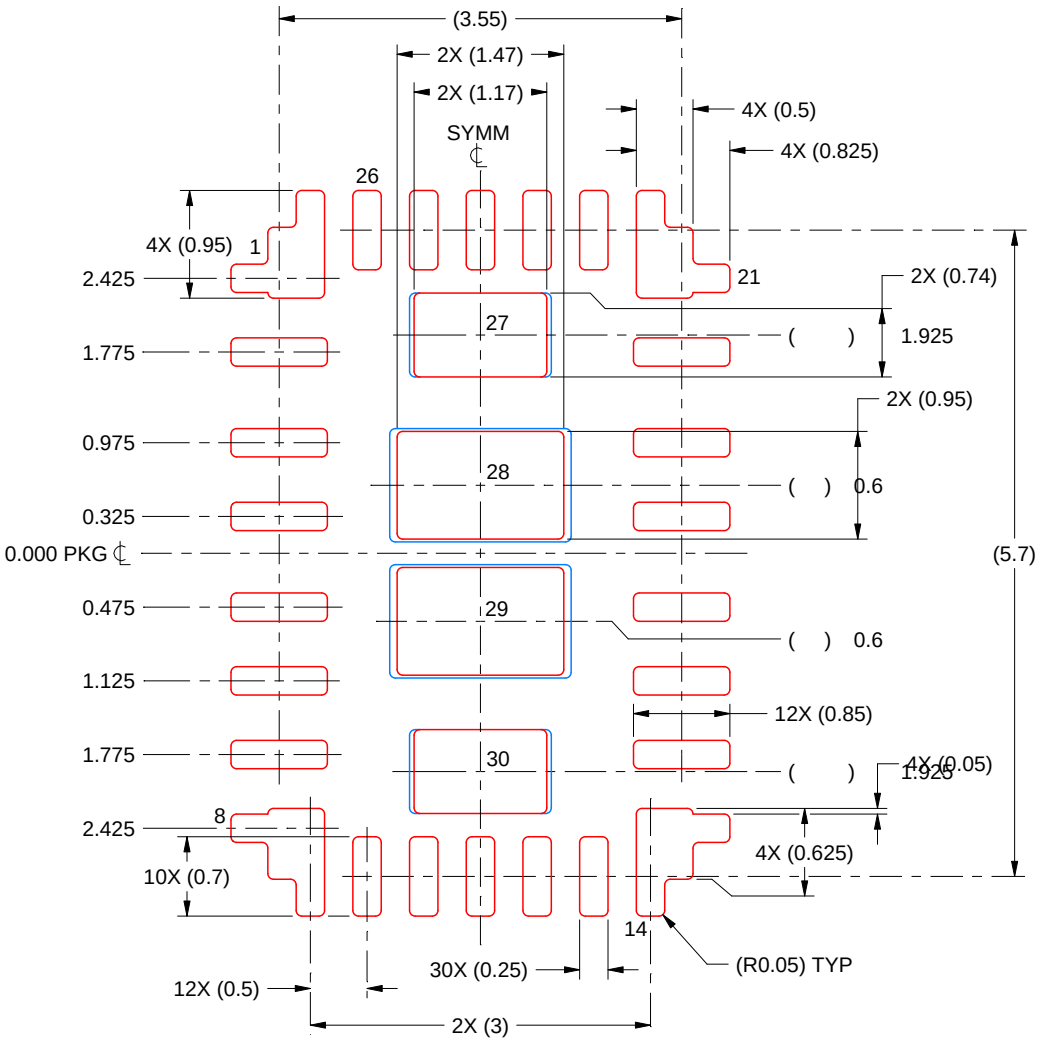


SOLDER MASK DETAILS

4226150/B 01/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 27 & 30:
94% PRINTED SOLDER COVERAGE BY AREA

EXPOSED PAD 28 & 29
87% PRINTED SOLDER COVERAGE BY AREA

SCALE:15X

4226150/B 01/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TMAG5328 Resistor-Adjustable, Low-Power Hall-Effect Switch

1 Features

- Adjustable B_{OP} from 2 mT to 15 mT
  - Using 2-kΩ to 15-kΩ resistors
  - or 160-mV to 1200-mV voltage source
- Omnipolar Hall switch
- Push-Pull output
- Low power consumption
  - 20-Hz versions: 1.4 µA at 3 V
- 1.65-V to 5.5-V operating V_{CC} range
- Industry-standard package and pinout
  - SOT-23 package
- –40°C to +125°C operating temperature range

2 Applications

- Battery-critical position sensing
- Electricity meter tamper detection
- Cell phone, laptop, or tablet case sensing
- E-locks, smoke detectors, appliances
- Medical devices, IoT systems
- Valve or solenoid position detection
- Contactless diagnostics or activation

3 Description

The TMAG5328 device is a high precision, low-power, resistor adjustable Hall effect switch sensor operating at low voltage.

The external resistor sets the B_{OP} value the device will operate from. By following a simple formula, it is easy to calculate what resistor value is needed to set up the right B_{OP} value. The Hysteresis value is fixed and therefore the B_{RP} value is defined as B_{OP}-Hysteresis.

With this adjustable threshold feature, the TMAG5328 allows for easy and quick prototyping, fast design to market, reuse across different platforms and easy last minute modifications in case of unexpected changes.

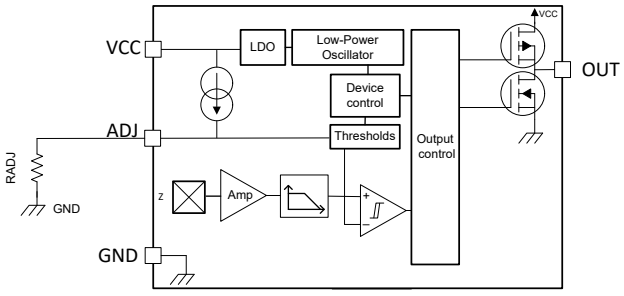
When the applied magnetic flux density exceeds the B_{OP} threshold, the device outputs a low voltage. The output stays low until the flux density decreases to less than B_{RP}, and then the output drives a high voltage. By incorporating an internal oscillator, the device samples the magnetic field and updates the output at a rate of 20 Hz for the lowest current consumption. Omnipolar magnetic response available.

The device operates from a V_{CC} range of 1.65 V to 5.5 V, and is packaged in a standard SOT-23-6 package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMAG5328	SOT-23 (6)	2.92 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
December 2021	*	Initial release.

5 Device Comparison

Table 5-1. Device Comparison

VERSION	THRESHOLD RANGE	MAGNETIC RESPONSE	OUTPUT TYPE	SAMPLING RATE	PACKAGES AVAILABLE
TMAG5328A1D	2 mT- 15 mT	Omnipolar active Low	Push-pull	20 Hz	SOT-23-6

6 Pin Configuration and Functions

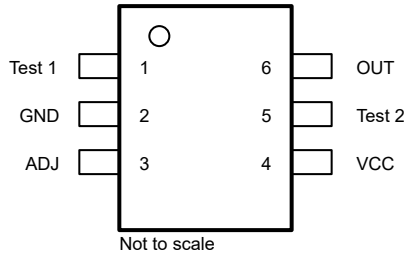


Figure 6-1. DBV Package 6-Pin SOT-23 Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT-23		
GND	2	—	Ground reference
OUT	6	O	Omnipolar output that responds to north and south magnetic poles
VCC	4	—	1.65-V to 5.5-V power supply. TI recommends connecting this pin to a ceramic capacitor to ground with a value of at least 0.1 µF
ADJ	3	I	This pin is used to set the thresholds up. Can either be connected to a resistor or voltage source.
Test 1	1	—	TI recommends to leave this pin floating
Test 2	5	—	TI recommends connecting this pin to GND

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power Supply Voltage	V_{CC}	–0.3	5.5	V
Output Pin Voltage	OUT	GND – 0.3	V_{CC} + 0.3	V
Output Pin current	OUT	-5	5	mA
Magnetic Flux Density,BMAX		Unlimited		T
Junction temperature, T_J	Junction temperature, T_J		150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	1.65	5.5	V
Vo	Output voltage	0	5.5	V
Io	Output current	-5	5	mA
T_A	Ambient temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMAG5328 SOT-23 (DBV) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	167.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADJ pin						
ADJ_ICC	Current output source			80		µA
ADJ_C	Maximum capacitance				50	pF
PUSH-PULL OUTPUT DRIVER						
V_{OH}	High-level output voltage	I_{OUT} = -0.5mA	Vcc-0.35	Vcc-0.1		V
V_{OL}	Low-level output voltage	I_{OUT} = 0.5mA		0.1	0.3	V
TMAG5328A1D						
fs	Frequency of magnetic sampling			20		Hz
ts	Period of magnetic sampling			50		ms
$I_{CC(AVG)}$	Average current consumption	Vcc=3V over temperature		1.4		µA
ALL VERSIONS						
$I_{CC(PK)}$	Peak current consumption			1.8		mA
$I_{CC(SLP)}$	Sleep current consumption			300		nA
t_{ON}	Power-on time			85		µs
P_{OS}	Power-on state	V_{CC}>$V_{CCmin,}$ t<t_{ON}		High		
t_{ACTIVE}	Active time period			65		µs

7.6 Magnetic Characteristics

Specified at 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TMAG5328						
$B_{OP(Range\ A)}$	Adjustable Operate Point		±2		±15	mT
$B_{RP(Range\ A)}$	Adjustable Release Point		±1		±14	mT
$V_{ADJ\ (Range\ A)}$	Voltage range		160		1200	mV
$R_{ADJ\ (Range\ A)}$	Resistor range		2		15	kΩ
$B_{OP}(R_{ADJ})$	B_{OP}/R			±1		mT/kΩ
$B_{OP\_ACC}(R_{ADJ})$	$\lvert(B_{OPMax} - B_{OPMin})/2\rvert$			0.5		mT
$B_{RP\_ACC}(R_{ADJ})$	$\lvert(B_{RPMax} - B_{RPMin})/2\rvert$			0.5		mT
$B_{HYSA}(R_{ADJ})$	Magnetic hysteresis $\lvert B_{OP} - B_{RP}\rvert$			1		mT

ADVANCE INFORMATION

8 Detailed Description

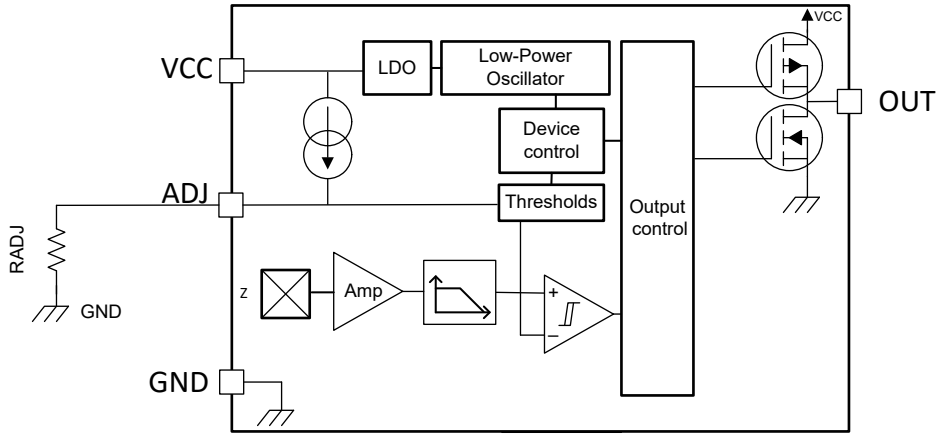
8.1 Overview

The TMAG5328 device is a magnetic sensor with a digital output that indicates when the magnetic flux density threshold has been crossed. The device integrates a Hall effect element, analog signal conditioning, and a low-frequency oscillator that enables ultra-low average power consumption.

While most of the Hall effect sensor have fixed threshold, the TMAG5328 offers an extra pin that allows the user to set up a specific threshold of operation. This pin can either be connected to a resistor or a voltage source. While the value can be set at production, it is also possible to allow dynamic change of either the resistor value or the voltage value to dynamically change the threshold value.

Operating from a 1.65-V to 5.5-V supply, the device periodically measures magnetic flux density, updates the output, and enters into a low-power sleep state.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Magnetic Flux Direction

Magnetic flux that travels from the bottom to the top of the package is considered positive in this data sheet. This condition exists when a south magnetic pole is near the top of the package. Magnetic flux that travels from the top to the bottom of the package results in negative millitesla values.

ADVANCE INFORMATION

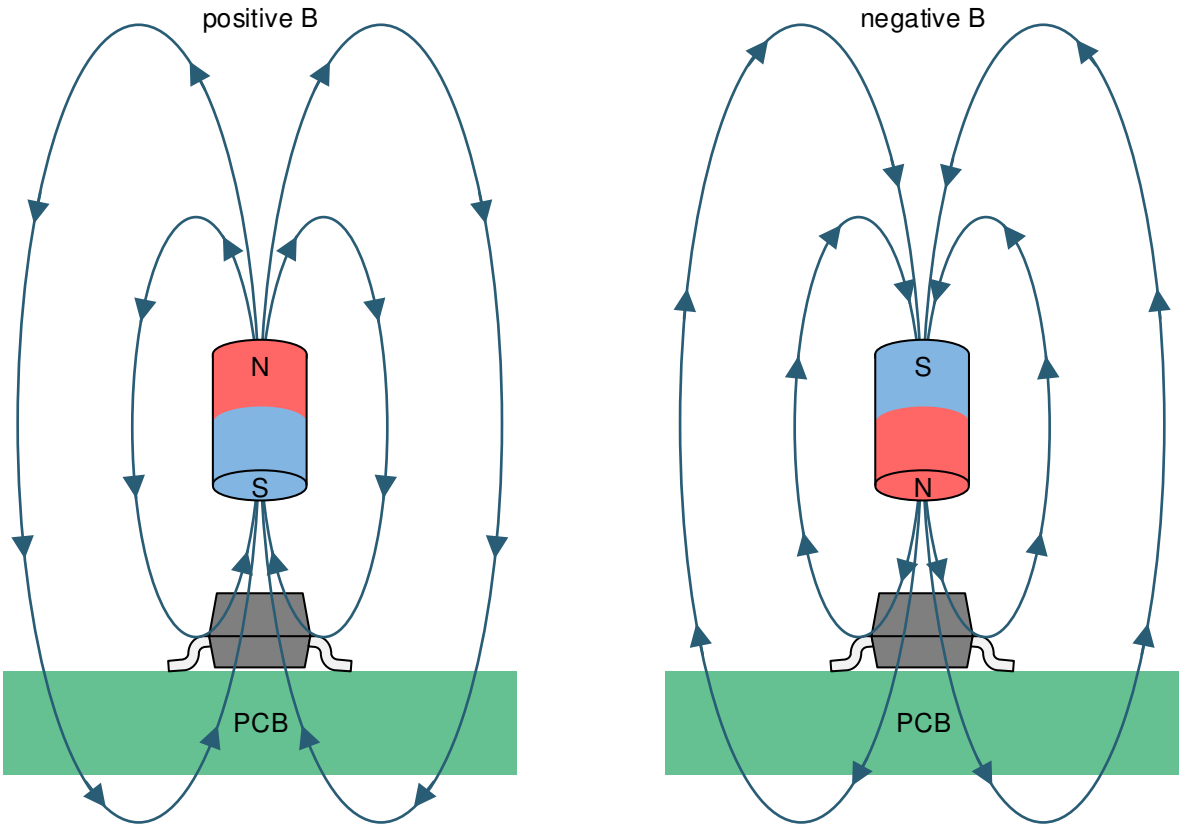


Figure 8-1. Flux Direction Polarity

8.3.2 Magnetic Response

The TMAG5328x1x device option have omnipolar functionality, and respond the same to north and south poles as shown in Figure 8-2.

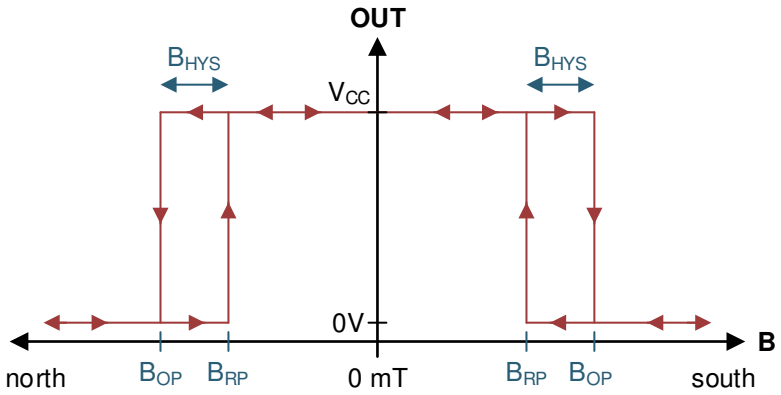


Figure 8-2. Omnipolar Functionality

8.3.3 Output Type

All version have push-pull CMOS outputs that can drive a V_{CC} or ground level.

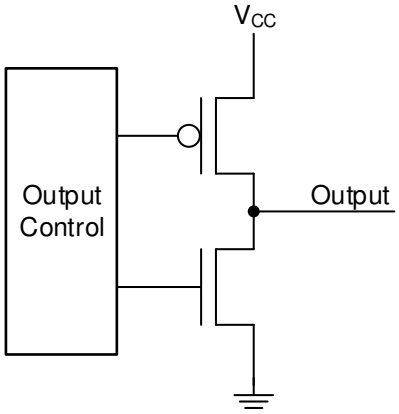


Figure 8-3. Push-Pull Output (Simplified)

8.3.4 Sampling Rate

When the TMAG5328 device powers up, the device measures the first magnetic sample and sets the output within the t_{ON} time. The output is latched, and the device enters an ultra-low-power sleep state. After each t_{Active} time has passed, the device measures a new sample and updates the output if necessary. If the magnetic field does not change between periods, the output also does not change.

While in active mode, the part will go through different steps. The content of the OTP (One-Time-Programmable Memory) is loaded first, and this steps takes about 35 µs and consumes around 350 µA. For the next 5 µs, the current source will be started and settled. The part now consumes around 650 µA in this step. Finally, the part conducts the Hall sensor conversion for about 25 µs and consumes the peak current of around 2 mA.

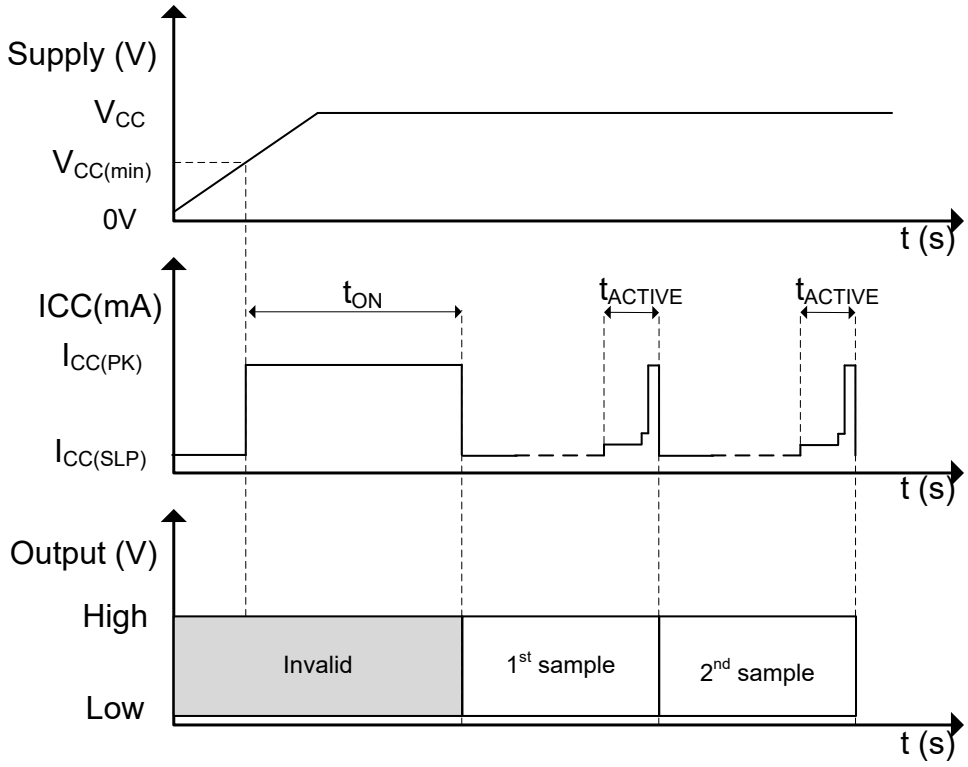


Figure 8-4. Timing Diagram

8.3.5 Adjustable Threshold

While most Hall Effect switch sensors have fixed magnetic characteristics, the TMAG5328 offers a wide range of adjustable thresholds. The user can use the "ADJ" pin to set the value of B_{OP} threshold. This pin can be used in two different ways. A resistor or a voltage source can be applied on "ADJ". In both scenarios, the resistor or voltage value will define the position of the B_{OP}. While the B_{OP} can be adjusted, the hysteresis has a fixed value. B_{RP} is therefore defined as B_{OP}-Hysteresis.

An 80-µA current is generated on pin "ADJ" when the part goes into active mode. The device then reads the "ADJ" pin and defines the value of B_{OP}. If the "ADJ" pin value is adjusted while the sensor is in sleep mode, the B_{OP} will update at the next active period of the device.

8.3.5.1 Adjustable Resistor

One way to setup the B_{OP} is to connect a resistor to the "ADJ" pin. The device generates a fixed current that is injected in the external resistor. This will generate a voltage that represent the B_{OP} value. The relationship between B_{OP} and resistance is define as $B_{OP}(mT) = R_{ADJ}(k\Omega)$

The device B_{OP} must be set to any value between 2 mT and 15 mT. This means R_{ADJ} must be set between 2 kΩ and 15 kΩ. Operating above and beyond those limits is not recommended and could result in either getting the wrong threshold set or locking up the device into a specific state without the possibility to quit.

Figure 8-5 shows the relationship between B_{OP} and R_{ADJ}.

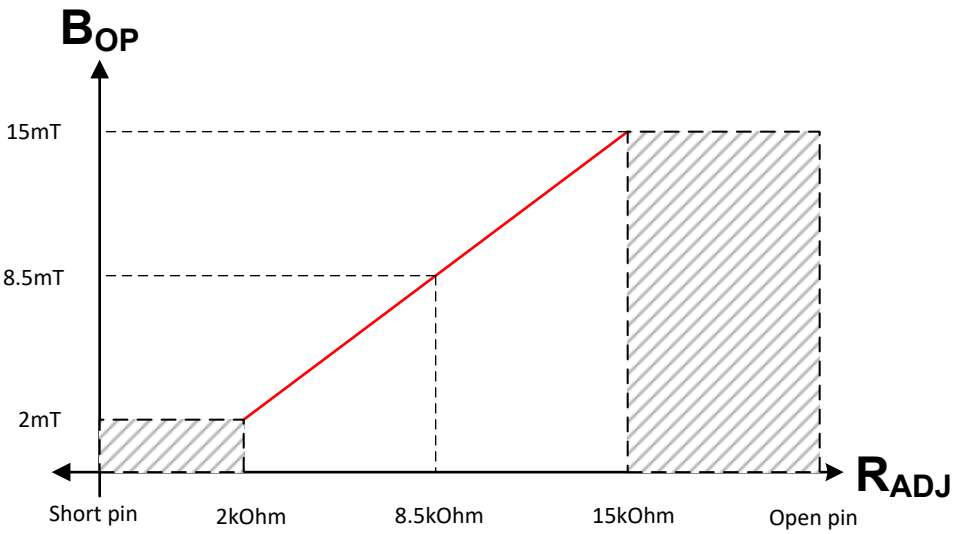


Figure 8-5. B_{OP} vs. R_{ADJ}

8.3.5.2 Adjustable Voltage

One other way to setup the B_{OP} is to apply a voltage to the "ADJ" pin. This voltage is directly proportional to the B_{OP} value. The relationship between B_{OP} and voltage is defined as $B_{OP}(mT) = V_{ADJ}(mV) \times 0.0125$

The device B_{OP} must be set to any value between 2 mT and 15 mT. This means V_{ADJ} must be set between 160 mV and 1200 mV. Operating above and beyond those limits is not recommended and could result in either getting the wrong threshold set or locking up the device into a specific state without the possibility to quit.

Figure 8-6 shows the relationship between B_{OP} and V_{ADJ}.

ADVANCE INFORMATION

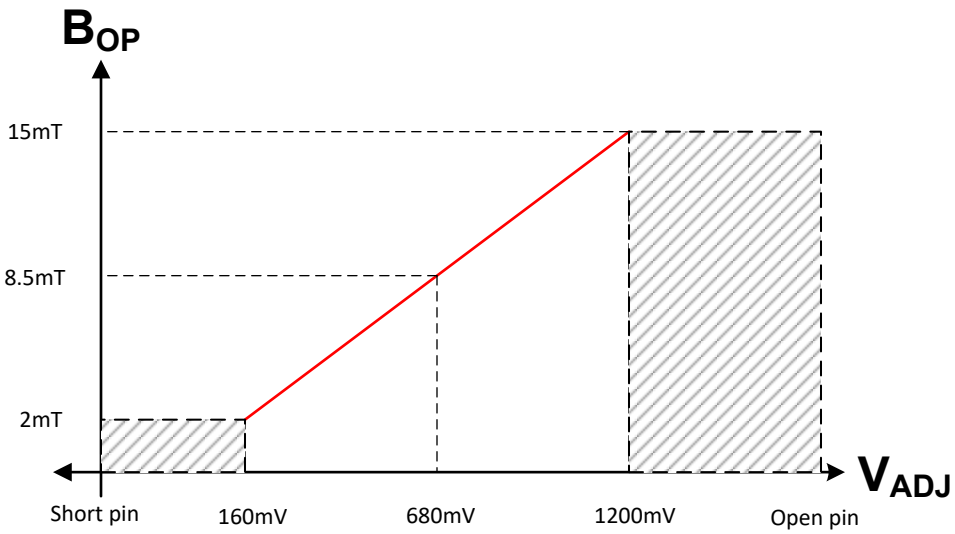
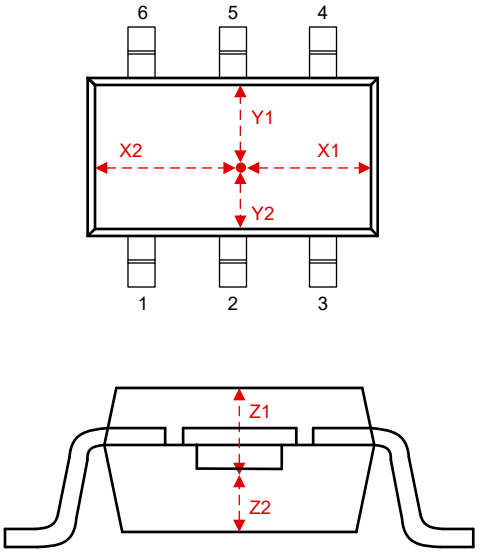


Figure 8-6. B_{OP} vs. R_{ADJ}

8.3.6 Hall Element Location

The sensing element inside the device is in the center positioned as presented below. Figure 8-7 shows the tolerances and side-view dimensions.



Sensor location:

X1: 1.468 mm
X2: 1.458

Y1: 0.9925 mm
Y2: 0.6335 mm

Z1: 0.665 mm
Z2: 0.475 mm

Figure 8-7. Hall Element Location

8.4 Device Functional Modes

The TMAG5328 device has one mode of operation that applies when the *Recommended Operating Conditions* are met.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Applications

The TMAG5328 can be used in a large variety of industrial applications. For almost all these applications, the sensor is fixed and the magnet is attached to a movable component in the system.

9.1.1 Refrigerator Door Open/Close Detection

This application section describes how to use the same device for two identical applications with different mechanical characteristic.

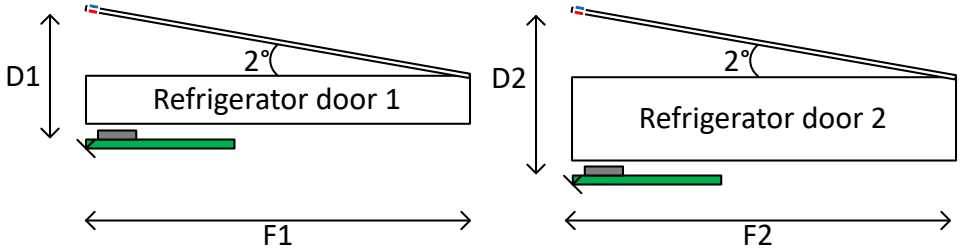


Figure 9-1. Fridge 1 and Fridge 2 Principal Diagram

9.1.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters for Fridge 1

DESIGN PARAMETER	EXAMPLE VALUE
Hall effect device	TMAG5328A1D
V_{CC}	5 V
Magnet	10 mm cubic N35
D1	7.12 mm
F1	500 mm
Door opening angle	2°
Calculated threshold needed (B_{OP})	7.87 mT
R_{ADJ}	7.87 kΩ

Table 9-2. Design Parameters for Fridge 2

DESIGN PARAMETER	EXAMPLE VALUE
Hall effect device	TMAG5328A1D
V_{CC}	5 V
Magnet	10 mm cubic N35
D2	16.12 mm
F2	500 mm
Door opening angle	2°
Calculated threshold needed (B_{OP})	3.49 mT
R_{ADJ}	3.48 kΩ

ADVANCE INFORMATION

9.1.1.2 Detailed Design Procedure

For both applications, the Hall sensor is used to detect if the refrigerator door is open or closed. Both refrigerator doors are different from each other and therefore have different mechanical design. This means the Hall sensor and the magnet are positioned differently from each other. In other terms, if the user wants to detect a specific distance for both refrigerator doors, they must use either a different magnet or a different sensor. For the purpose of this application, there is no flexibility in the choice of magnet. The electronic board will also be reused across platforms and therefore will use the same sensor.

The TMAG5328 is a resistor adjustable Hall effect switch that allows the user to set up whatever threshold is needed between 2 mT and 15 mT.

For this application the refrigerator door manufacturer can use the same PCB, with the same semiconductor content and only has to change the resistor value depending on which fridge version is manufactured.

For both refrigerator doors, the opening angle are the same. Now refrigerator door 1 is a thinner model than refrigerator door 2. This means the PCB is located further away for refrigerator door 2 and therefore the sensitivity required to detect the position of the door will be impacted.

Knowing the door length, the door opening angle required, and the distance from the magnet to the PCB, it is possible to use a simulation tool that will calculates the magnet strength at the desired position. For refrigerator door 1, the sensitivity calculated is 7.87 mT at a distance of 7.12 mm. For Fridge 2, the sensitivity is 3.49 mT at a distance of 16.12 mm. Based on those values, a resistor value can be selected from the E48 series. A resistor of 7.87 kΩ can be used for refrigerator door 1 and resistor of 3.48 kΩ can be used for refrigerator door 2.

10 Power Supply Recommendations

The TMAG5328 device is powered from 1.65-V to 5.5-V DC power supplies. A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.1 µF.

11 Layout

11.1 Layout Guidelines

Magnetic fields pass through most non-ferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards, which makes placing the magnet on the opposite side possible.

11.2 Layout Examples

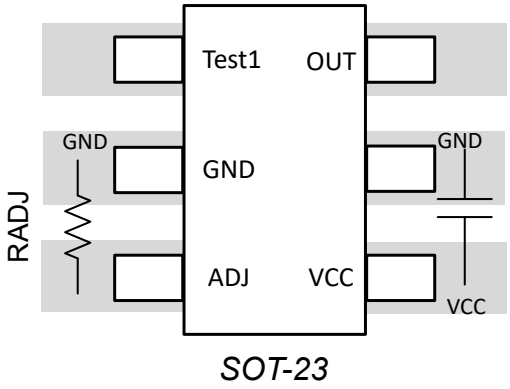


Figure 11-1. Layout Examples

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

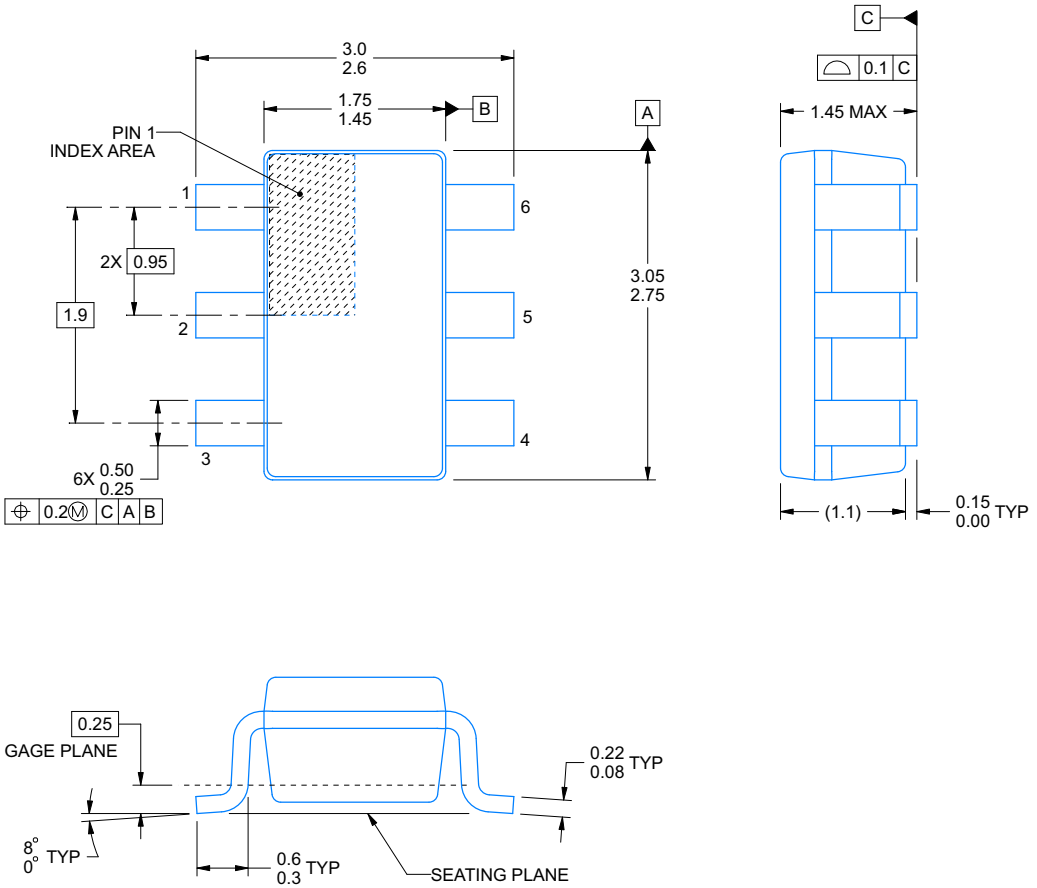
ADVANCE INFORMATION

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

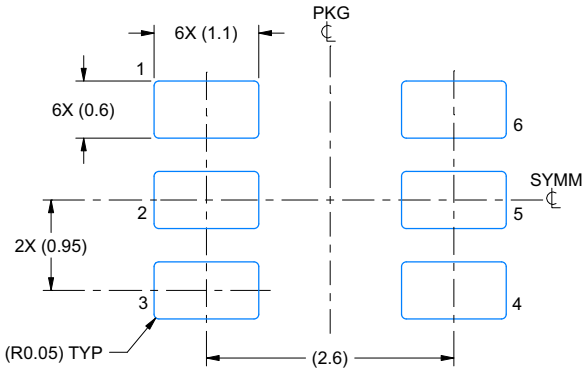
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

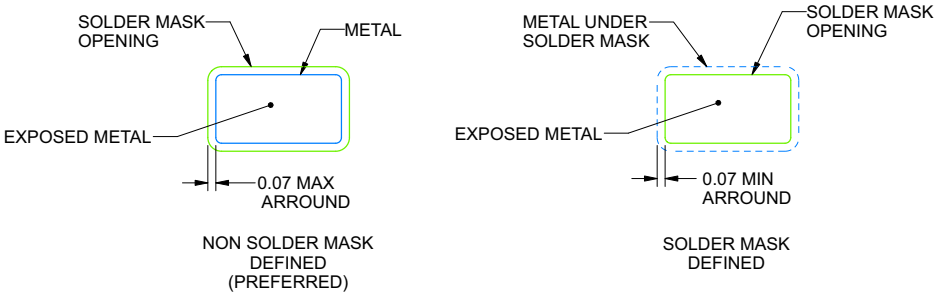
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

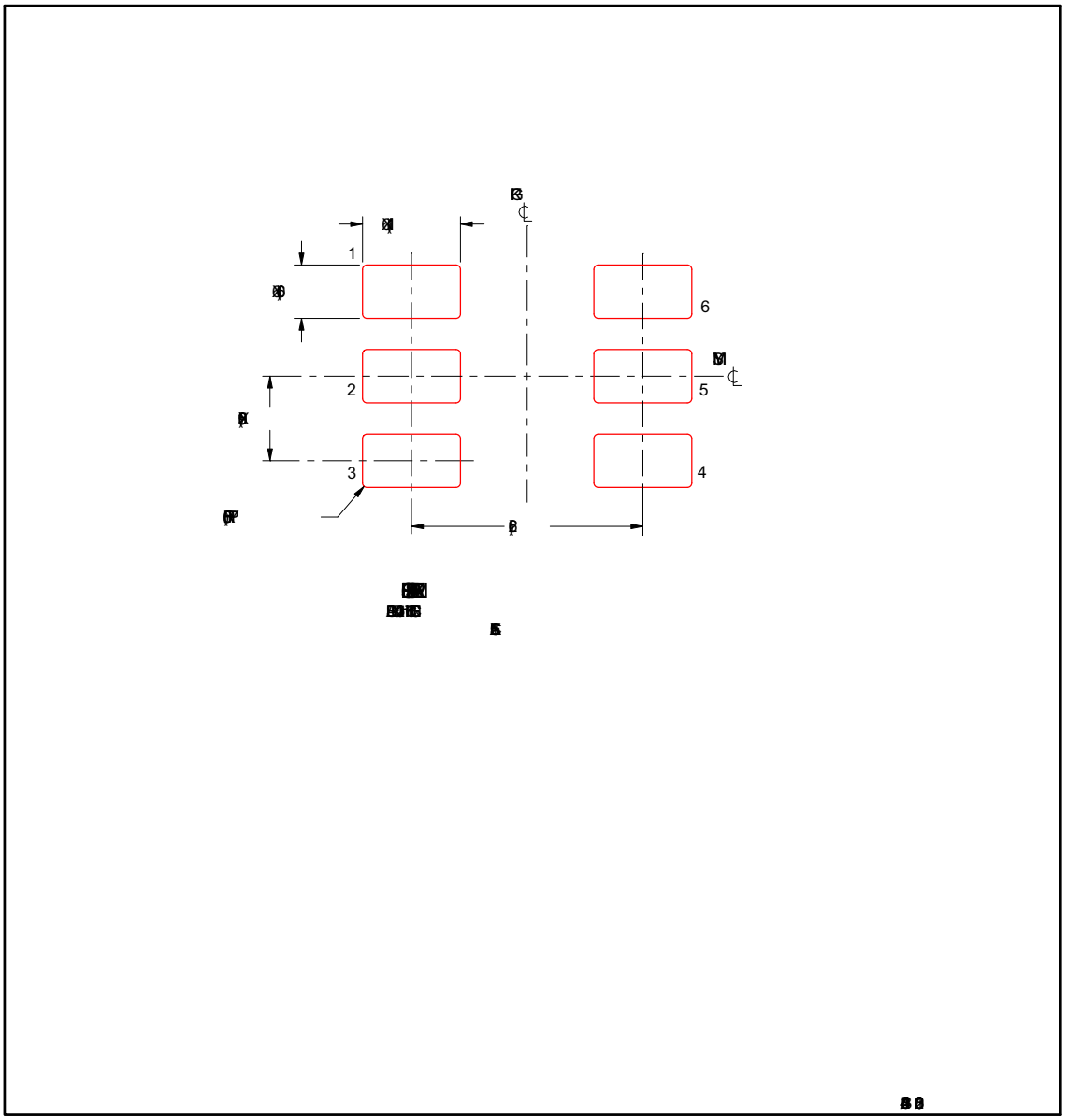
4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A — **SOT-23 - 1.45 mm max height**



ADVANCE INFORMATION

13.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PTMAG5328A1DQDBVR	ACTIVE	SOT-23	DBV	6	Call TI	Call TI	Call TI	Call TI	-40 to 125	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

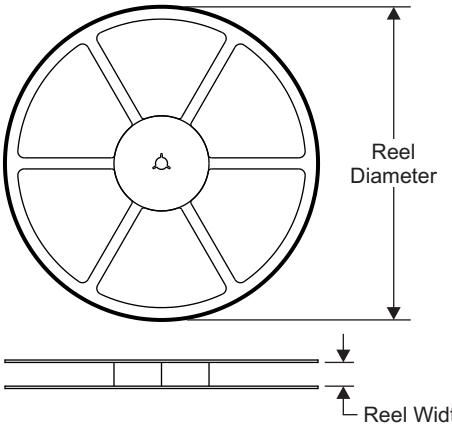
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

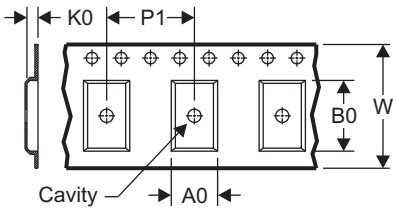
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

13.2 Tape and Reel Information

REEL DIMENSIONS

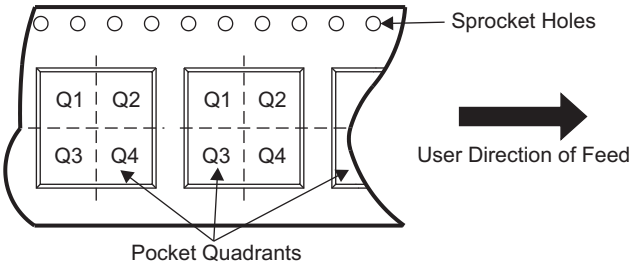


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

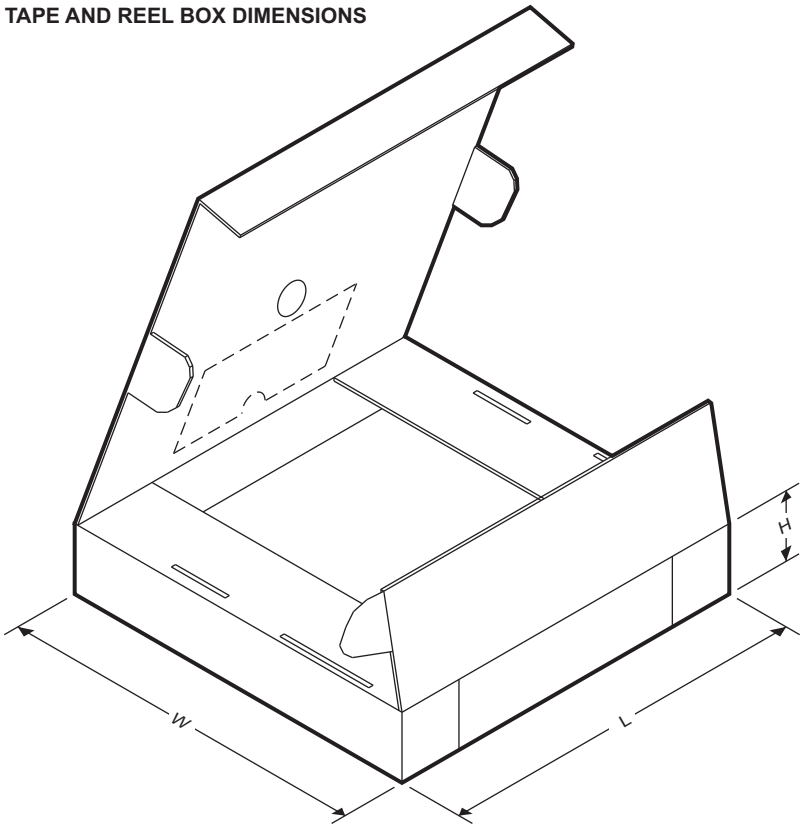


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMAG5328A1DQDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMAG5328A1DQDBVR	SOT-23	DBV	6	3000	Call TI	Call TI	Call TI

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMAG5328A1DQDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

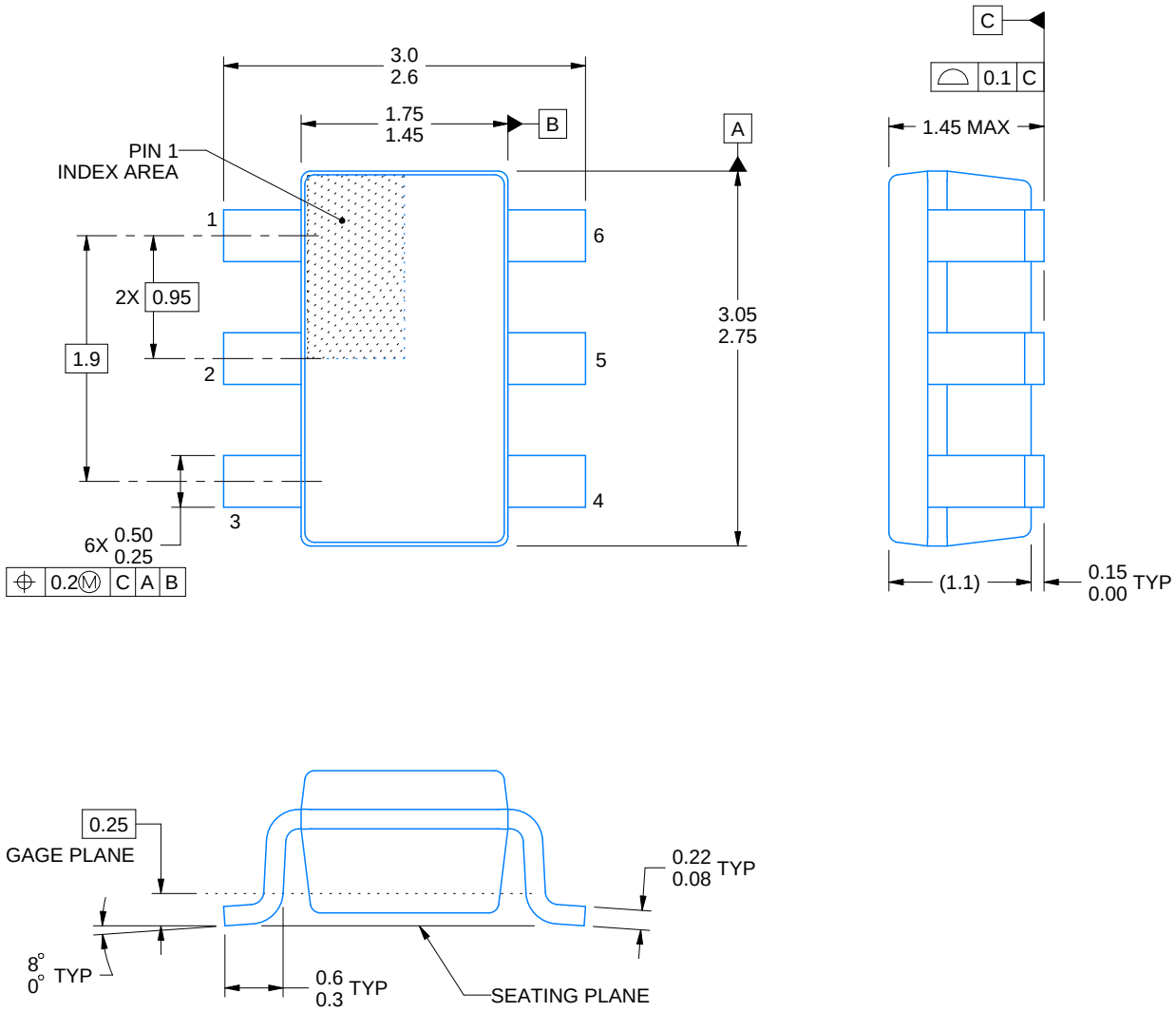
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

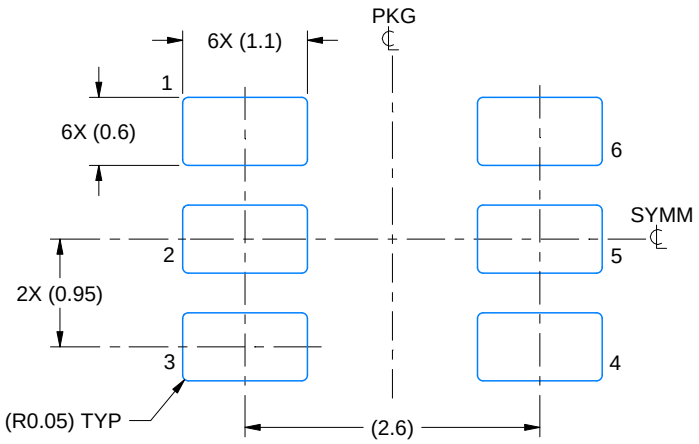
SMALL OUTLINE TRANSISTOR



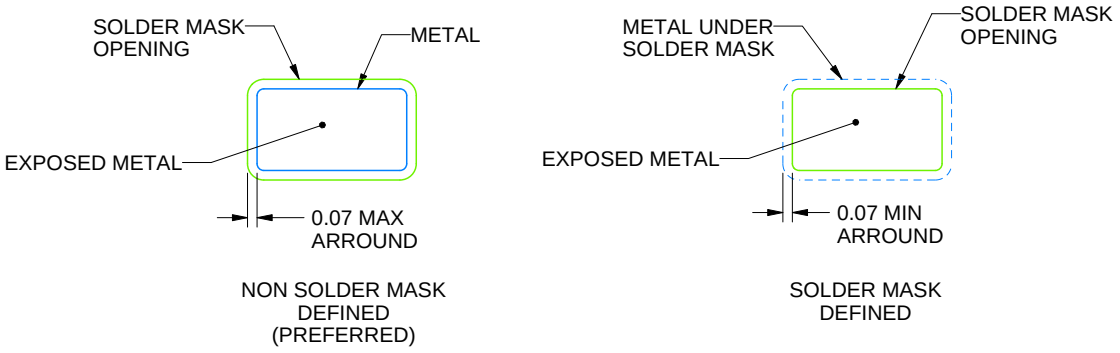
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

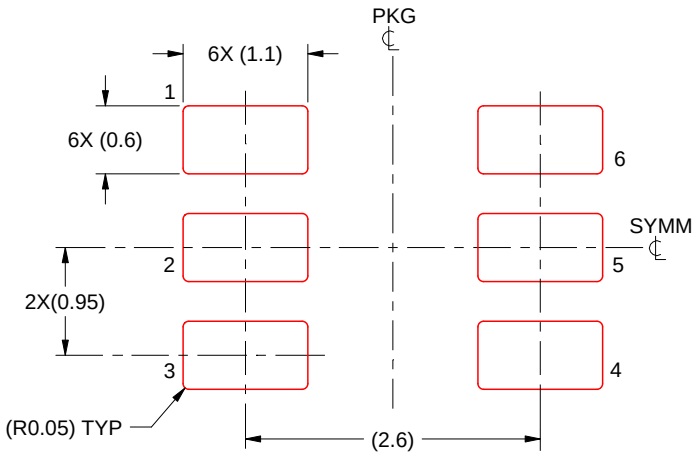


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TMP1826 Single-Wire, ±0.3°C Accurate Temperature Sensor With 2-Kbit EEPROM

1 Features

- Single-wire interface with multi-drop shared bus and CRC
- Bus powered with operating voltage from 1.7 V to 5.5 V
- IEC 61000-4-2 ESD for 8-kV contact discharge
- High-accuracy digital temperature sensor:
  - ±0.1°C (typical)/±0.3°C (maximum) from –20°C to +85°C
  - ±0.3°C (typical)/±0.5°C (maximum) from –40°C to +125°C
- Active current of 100-µA (typical) and shutdown current of 0.37 µA (typical)
- 16-bit temperature resolution: 7.8 m°C (1 LSB)
- Fast data rates of 90 kbps in overdrive speed
- 2-Kbit EEPROM features:
  - Write in 64-bit blocks
  - Continuous read mode
  - Read with write protection in 256-bit blocks
  - Read/write current of 95 µA/178 µA (typical)
- NIST traceable factory-programmed non erasable 64-bit identification number for device addressing
- 4 configurable open-drain digital input-output

2 Applications

- Factory automation and control
- Appliances
- Medical accessories
- CPAP machine
- Battery packs
- Cold chain applications
- Temperature transmitters
- EV charging infrastructure

3 Description

The TMP1826 is a high-accuracy, single-wire compatible digital output temperature sensor with integrated 2-Kbit EEPROM. The TMP1826 provides a high accuracy of ±0.1°C (typical)/±0.3°C (maximum) across the temperature range of –20°C to +85°C. Each device comes with a factory programmed 64-bit unique identification number for addressing and NIST traceability. The TMP1826 supports both standard speed for legacy application and over drive mode with 90-kbps data rate for low latency communication.

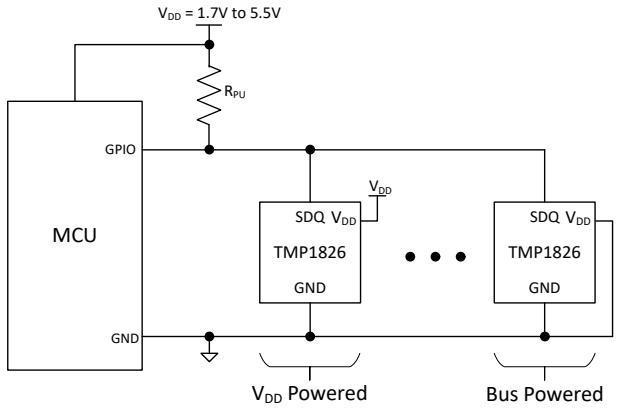
In the simplest mode of operation, the TMP1826 single-wire interface, with an integrated 8-kV IEC-61000-4-2 ESD protection on the data pin, requires only a single connection and a ground return in bus powered mode, which simplifies and reduces cost by reducing the number of wires and external protection components. Additionally, there is the V_{DD} power pin also available for applications that may want to have a dedicated power supply.

The 2-Kbit EEPROM on the TMP1826 allows the host to store application data in increments of 64 bits. With user programmable 256-bit page size write protection to avoid accidental overwrite, the EEPROM can be used as non-volatile, read-only memory. The four digital I/O pins are configurable for general purpose functions, temperature alert, or provide host to identify the position of the device on a shared bus.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMP1826	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial release.

5 Pin Configuration and Functions

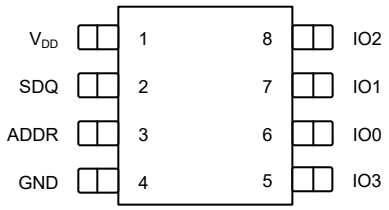


Figure 5-1. DGK 8-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	VSSOP		
ADDR	3	I	Reserved for future use. If unused, must be connected to ground
GND	4	—	Ground
IO0	6	I/O	General purpose digital IO. If unused, must be connected to ground
IO1	7	I/O	General purpose digital IO. If unused, must be connected to ground
IO2	8	I/O	General purpose digital IO or configurable as temperature alert. If unused, must be connected to ground
IO3	5	I/O	General purpose digital IO. If unused, must be connected to ground
SDQ	2	I/O	Serial bidirectional data. In bus power mode, the pin is used to power the internal capacitor
V_{DD}	1	I	Supply voltage in V_{DD} powered mode. In bus powered mode, must be connected to ground

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}		6.5	V
I/O voltage	SDQ, Bus powered mode	–0.3	6.5	V
	SDQ, Supply powered mode	–0.3	V_{DD} + 0.3	
I/O voltage	IO0, IO1, IO2, IO3	–0.3	6.5	V
Operating junction temperature, T_J		-55	155	°C
Storage temperature, T_{stg}		-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged-device model (CDM), per JEDEC specification per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V
		IEC 61000-4-2 Contact Discharge	SDQ pin	±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

ADVANCE INFORMATION

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage V_{DD} powered mode	1.70		5.5	V
V_{PUR}	Supply voltage bus powered mode(1)	1.70		5.5	V
$V_{I/O}$	All IO pins except SDQ	0		5.5	V
V_{SDQ}	SDQ pin in V_{DD} powered mode	0		V_{DD} + 0.3	V
T_A	Operating ambient temperature	-40		125	°C

(1) Bus powered mode from 1.7 V to 3.3 V supported in overdrive speed only.

6.4 Thermal Information

THERMAL METRIC(1)		TMP1826 DGK (VSSOP) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.5	°C/W
M_T	Thermal Mass	TBD	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy	-20 °C to 85 °C			±0.1	±0.3	°C
		-40 °C to 125°C			±0.3	±0.5	
PSR	DC power supply sensitivity					±0.03	°C/V
T_{RES}	Temperature resolution	Including sign bit			16		Bits
		LSB			7.8125		m°C
T_{REPEAT}	Repeatability(1)	V_{DD} = 3.3 V AVG_SEL = 1, CONV_TIME_SEL = 1 1-Hz conversion interval, 300 acquisition			2		LSB
T_{LTD}	Long-term stability and drift	1000 hours at 125°C(2)			TBD		°C
t_{RESP_L}	Reponse time (Stirred Liquid)	Single layer Flex PCB	τ = 63 % 25 °C to 75 °C		TBD		ms
		2-layer 62-mil Rigid PCB			TBD		ms
T_{HYST}	Temperature cycling and hysteresis	T_{START} = -40 °C T_{FINISH} = 125 °C T_{TEST} = 25 °C 3 cycles			4		LSB
t_{ACT}	Active Conversion time (No Averaging)	(Figure 7-8)			5.7		ms
t_{DELAY}	Command start-up delay for temperature conversion and EEPROM programming			100		300	µs
SDQ DIGITAL INPUT/OUTPUT							
C_{SDQ}	SDQ pin capacitance				40		pF
V_{IL}	Input logic low level(3)			–0.3		0.2 × V_S	V
V_{IH}	Input logic high level(3)			0.8 × V_S		V_S + 0.3	V

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{HYST}	Hysteresis				0.3		V
I_{IN}	Input leakage current				±0.5	TBD	µA
V_{OL}	Output low level	I_{OL} = –4 mA				0.4	V
GPIO CHARACTERISTICS							
C_{IN}	Input capacitance				10		pF
V_{IL}	Input logic low level(3)			–0.3		0.2 × V_S	V
V_{IH}	Input logic high level(3)			0.8 × V_S		V_S	V
I_{IN}	Input leakage current				0	TBD	µA
V_{HYST}	Hysteresis				0.175		V
V_{OL}	Output low level	I_{OL} = –4 mA				0.4	V
POWER SUPPLY							
I_{PU}	Pullup current(4)	Bus powered mode, serial bus inactive		300			µA
I_{DD_ACTIVE}	Supply current during active conversion	Active Conversion, serial bus inactive			100	TBD	µA
I_{DD_SB}	Standby current(5)	V_{DD} powered, serial bus inactive, continuous conversion mode	T_A = -40 °C to 85 °C		12.5	TBD	µA
			T_A = -40 °C to 125 °C			TBD	
I_{DD_SD}	Shutdown current	Bus powered, serial bus inactive, one shot conversion mode	T_A = -40 °C to 85 °C		0.37	TBD	µA
			T_A = -40 °C to 125 °C			TBD	
V_{POR}	Power-on reset threshold voltage	Supply rising (Figure 6-4, Figure 6-5)			1.25		V
	Brownout detect	Supply falling			1.15		V
t_{INIT}	Power on Reset Initialization Time	Time required by device to reset after power up (Figure 6-4, Figure 6-5)				2.0	ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 125 °C.
(3) In bus powered mode V_S = V_{PUR}. In supply powered mode, V_S = V_{DD}
(4) The pullup current parameter is required to size the bus pullup resistor for active temperature conversion or EEPROM read, erase and program operations.
(5) Quiescent current between conversions.

6.6 Single-Wire Interface Timing

Over free-air temperature range and V_{DD} = 1.70 V to 5.5 V (unless otherwise noted)

		STANDARD MODE		OVERDRIVE MODE		UNIT
		MIN	MAX	MIN	MAX	
BUS RESET AND BIT SLOT TIMING						
t_{RSTL}	Host to device bus reset pulse width (Figure 6-1) (1)	480	560	48	80	µs
t_{RSTH}	Device to host response time (Figure 6-1)(2)	480		48		µs
t_{PDH}	Device turnaround time for bus reset response (Figure 6-1)	15	60	2	8	µs
t_{PDL}	Device to host response pulse width (Figure 6-1)	60	240	8	24	µs
t_{SLOT}	Bit slot time (Figure 6-2, Figure 6-3)	60	120	11		µs
t_{REC}	Recovery time (Figure 6-2, Figure 6-3)	2		2		µs
t_{GF}	Glitch filter width (Figure 6-6)(3)	0.48		0.025		µs
t_F	Fall time		100		100	ns
BIT WRITE TIMING						
t_{WR0L}	Host write 0 width (Figure 6-2)	60	120	9	10	µs

ADVANCE INFORMATION

Over free-air temperature range and V_{DD} = 1.70 V to 5.5 V (unless otherwise noted)

		STANDARD MODE		OVERDRIVE MODE		UNIT
		MIN	MAX	MIN	MAX	
t_{WR1L}	Host write 1 width (Figure 6-2)	2	15	1	2	µs
t_{RDV}	Device read data valid time (Figure 6-2)	15		2		µs
t_{DSW}	Device read data window (Figure 6-2)	15	45	2	7	µs
BIT READ TIMING						
t_{RL}	Host drive read bit slot time (Figure 6-3)	2	5	1	2	µs
t_{RWAIT}	Host wait time before read data sampling window (Figure 6-3)(4)		$t_{RL}+t_{RC}$		$t_{RL}+t_{RC}$	µs
t_{MSW}	Host read data sampling window (Figure 6-3)	$t_{RL}+t_{RC}$	30	$t_{RL}+t_{RC}$	3	µs

(1) In bus powered mode, extending the t_{RSTL} above 600 µs may cause the device to power on reset
(2) The t_{RSTH} is the maximum time the host must wait to receive a response from the furthest device, taking into account the propagation delay and recovery time for all the devices.
(3) The glitch filter timing applies only on the rising edge of the SDQ signal
(4) The t_{RC} time is defined as the time taken for the bus voltage to rise from 0V to minimum V_{IH} of the host. This is a function of the bus pull up resistor and parasitic capacitance of the trace or cable.

6.7 EEPROM Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25°C and V_{DD} = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{PROG}	Programming time for 8-byte block		13.2	21	ms
$t_{READIDLE}$	Idle bus time for EEPROM 8-byte block read			400	µs
I_{DD_PROG}	Programming current		178	TBD	µA
Data Retention	at T_A = 125°C	25			years
Endurance		1000	20000		cycles

6.8 Timing Diagrams

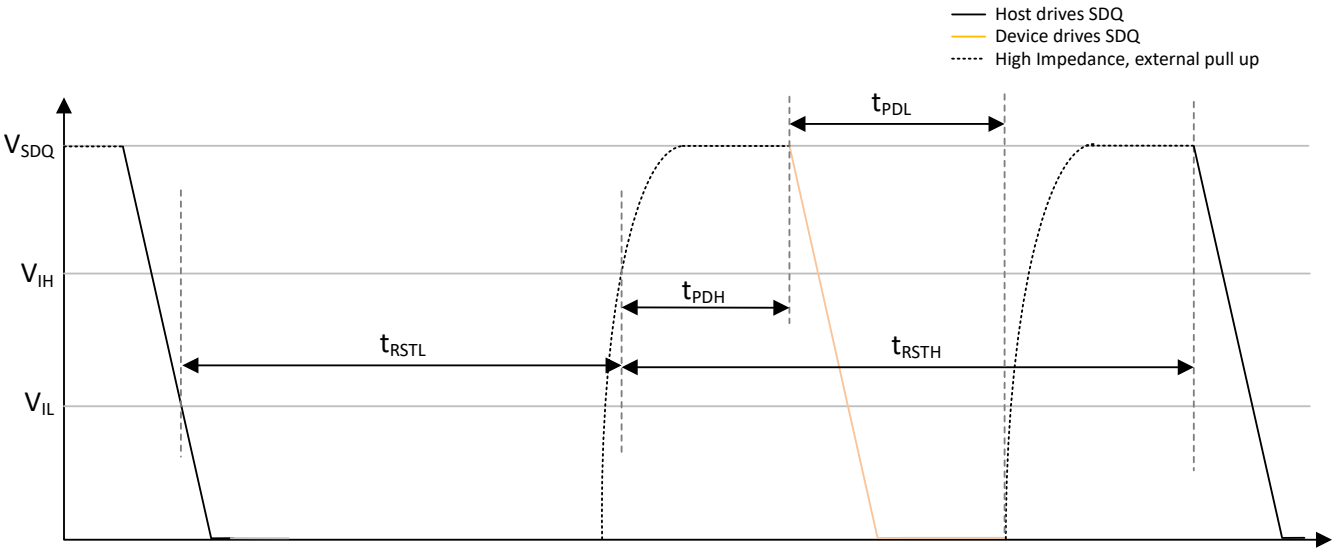


Figure 6-1. Bus Reset Timing Diagram

ADVANCE INFORMATION

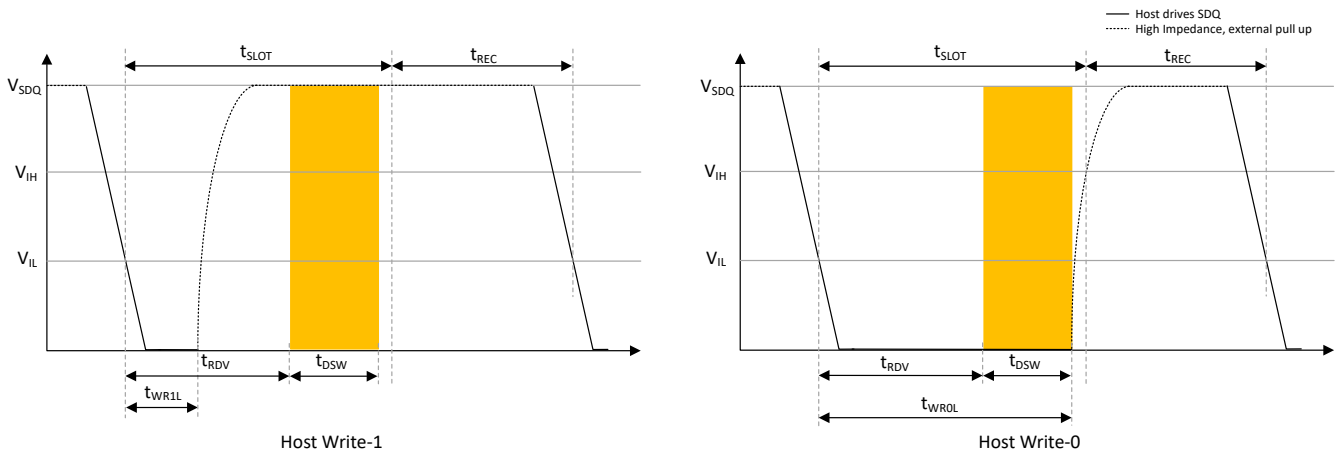


Figure 6-2. Write Timing Diagram

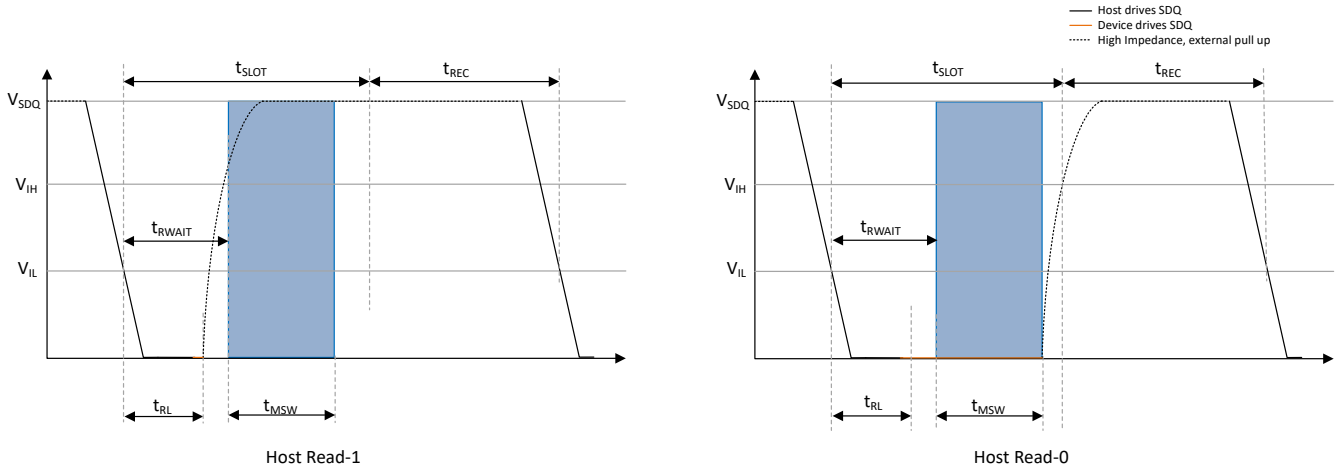


Figure 6-3. Read Timing Diagram

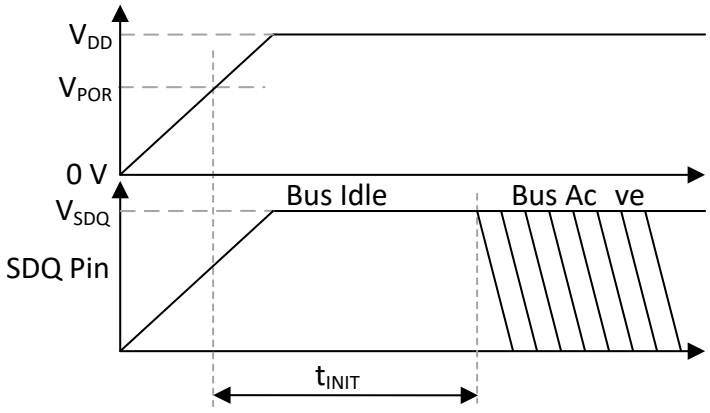


Figure 6-4. V_{DD} Powered Initialization Timing Diagram

ADVANCE INFORMATION

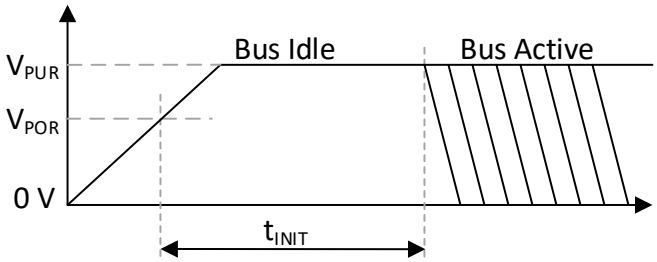


Figure 6-5. Bus Powered Initialization Timing Diagram

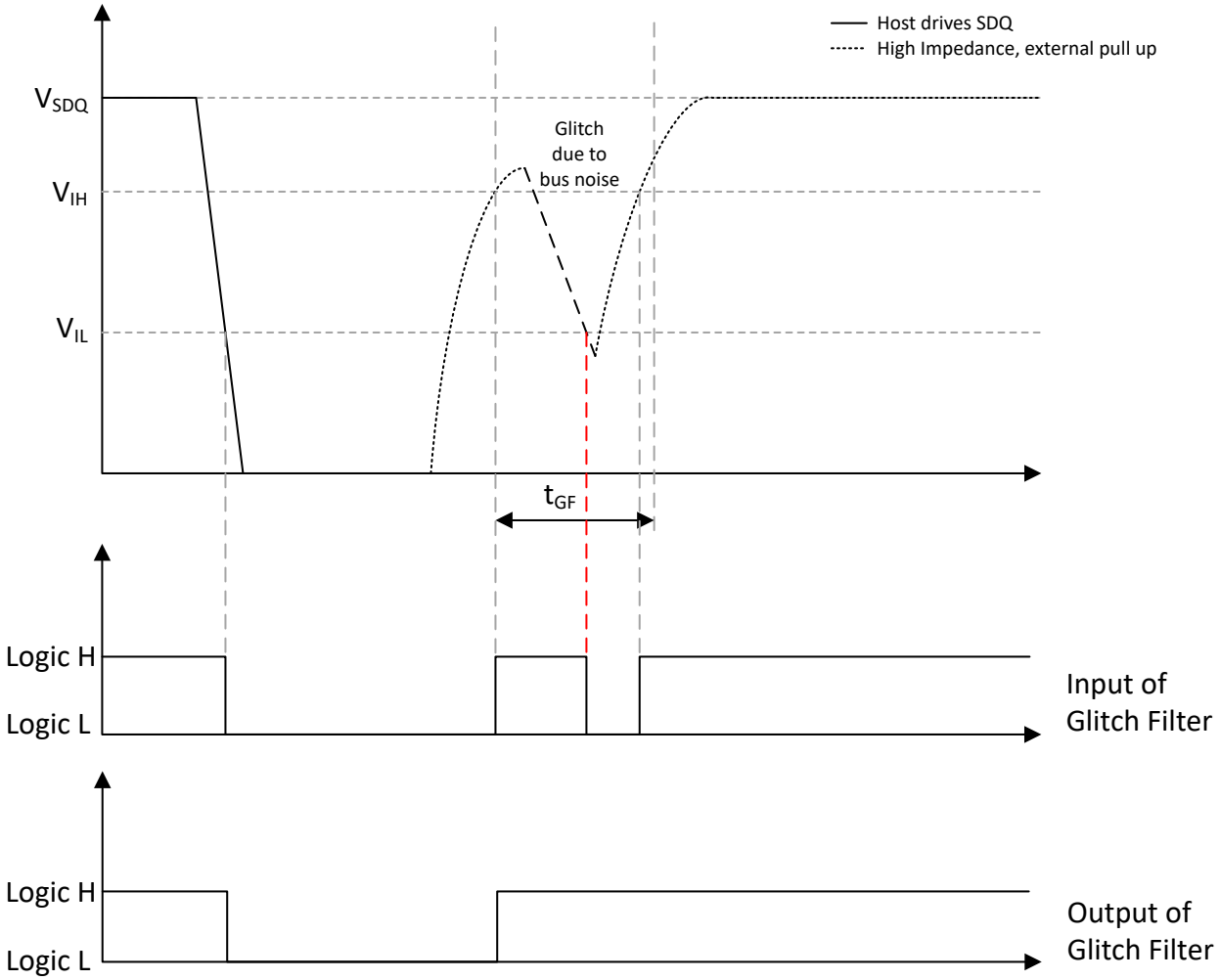


Figure 6-6. Glitch Filter Timing Diagram

6.9 Typical Characteristics

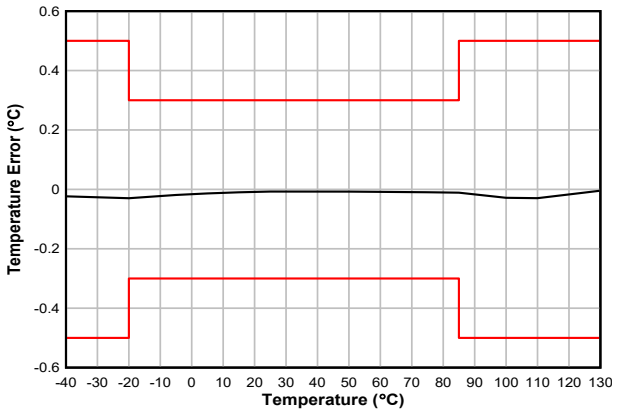


Figure 6-7. Temperature Error vs. Temperature

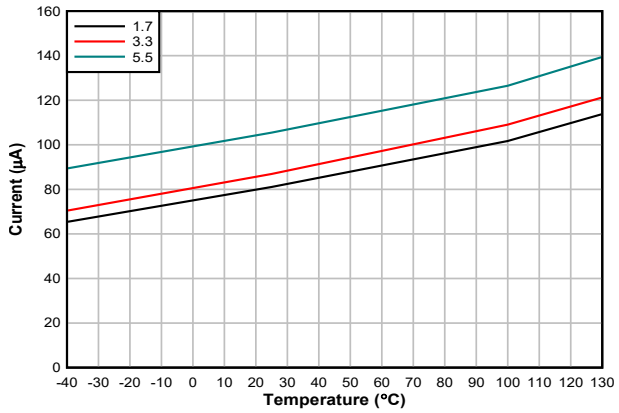


Figure 6-8. Active Current vs. Temperature

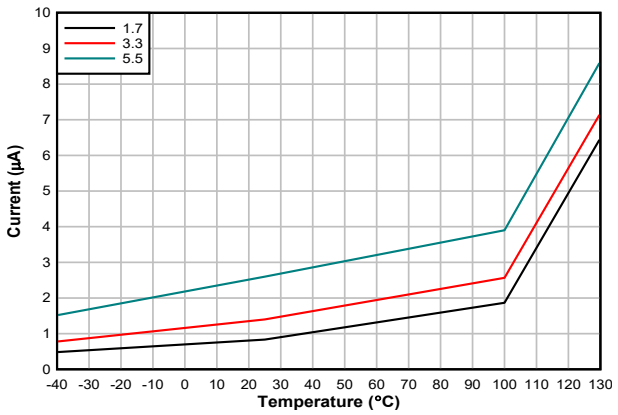
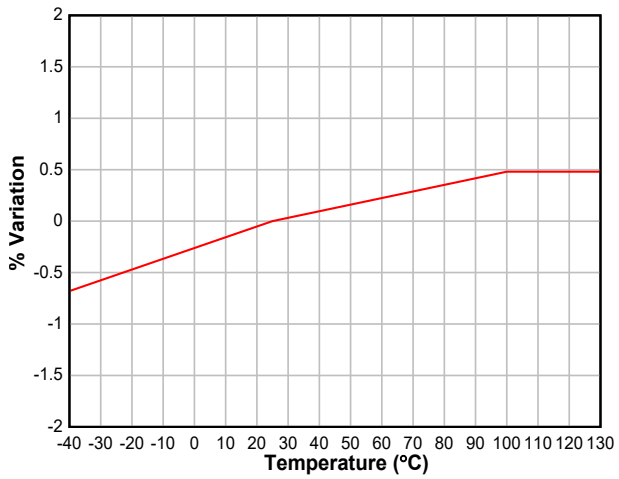
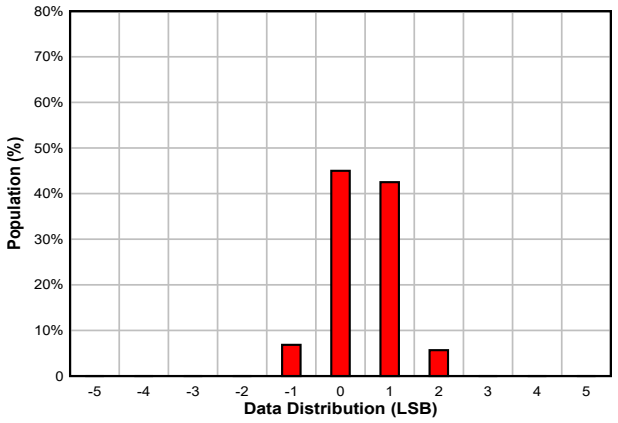


Figure 6-9. Shutdown Current vs. Temperature



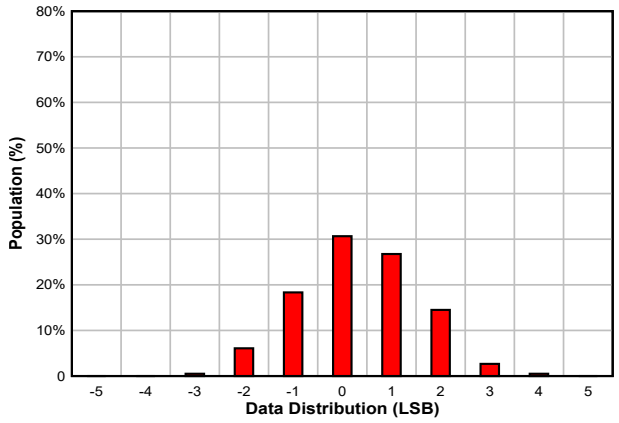
V_{DD} = 1.7 V to 5.5 V

Figure 6-10. Conversion Time vs. Temperature



T_A = 25 °C

Figure 6-11. Data Distribution With 5.5-ms Conversion Time and Averaging On

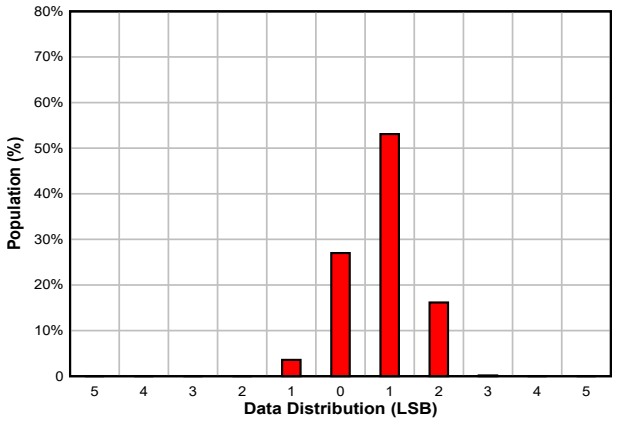


T_A = 25 °C

Figure 6-12. Data Distribution With 5.5-ms Conversion Time and Averaging Off

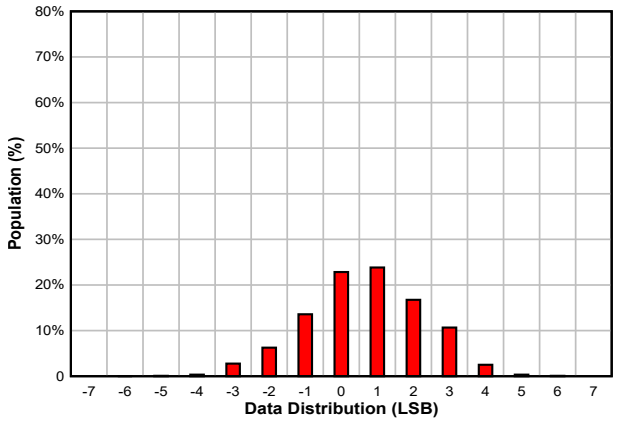
ADVANCE INFORMATION

6.9 Typical Characteristics (continued)



T_A = 25 °C

Figure 6-13. Data Distribution With 3-ms Conversion Time and Averaging On



T_A = 25 °C

Figure 6-14. Data Distribution With 3-ms Conversion Time and Averaging Off

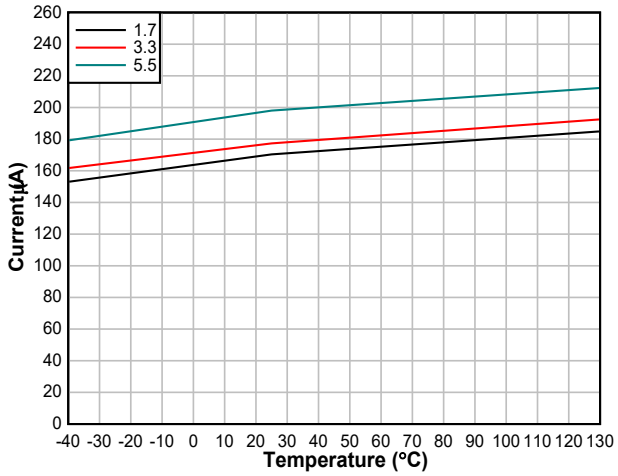


Figure 6-15. EEPROM Programming Current vs. Temperature

7 Detailed Description

7.1 Overview

The TMP1826 is a digital output temperature sensor designed for thermal-management and thermal-protection applications. The TMP1826 is a single-wire device which can operate in either supply powered or bus powered (parasitic powered) mode. The device features a 2-Kbit EEPROM. Figure 7-1 shows a block diagram of the TMP1826.

7.2 Functional Block Diagram

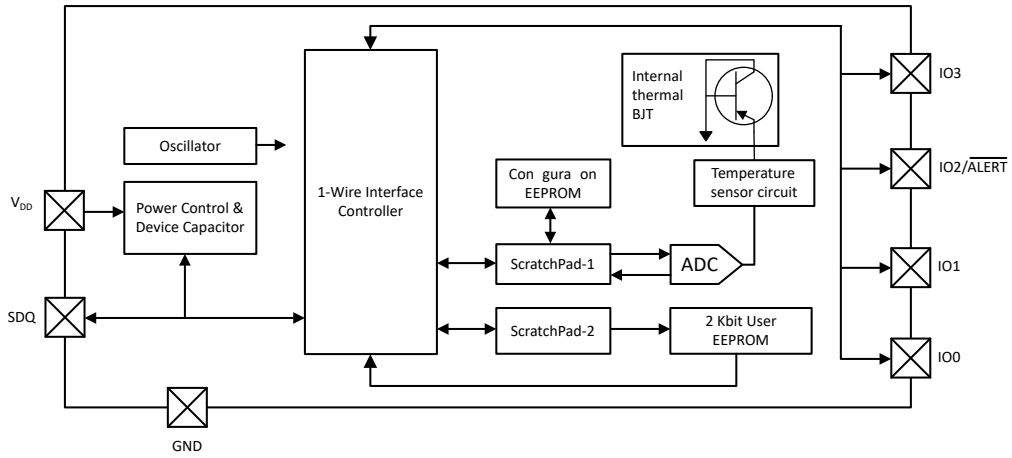


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Up

The device operates in both supply powered and bus powered mode. Irrespective of the mode, when the supply voltage reaches within the operating range, the device requires t_{INIT} to initialize itself. After t_{INIT}, the host MCU can begin accessing the device.

During initialization, the device may not respond to any bus activity. When initialization is complete, the device shall wait for the bus reset from the host. During the initialization for the device, the following events take place:

- The EEPROM content for STACKMODE_ADDR, TEMP_ALERT_LOW, TEMP_ALERT_HIGH and TEMP_OFFSET are restored to the respective registers.
- The EEPROM for the IO configuration register is read and contents of the IO_CONFIG register is restored.
- The EEPROM content for DEVICE_CONFIG1, DEVICE_CONFIG2 are restored to the respective registers.
  - If the ARB_MODE bits are set to value other than '00', then the device will respond to the SEARCHADDR in arbitration mode.
  - If OD_EN bit is set to '1', then the device shall communicate in overdrive speed, unless the first bus reset pulse from the host is sent in standard speed.
- The user memory protection bits are restored and appropriate protection to the user EEPROM block applied.

7.3.2 Power Mode Switch

The device is designed to operate in supply powered or bus powered mode. The dual mode implementation provides a unique method of redundancy that, even in cases where the power supply pin gets disconnected, the device can draw power from data pin, as long as the pullup resistor value used is as per the specification limit. This may be the system case where while operating in supply powered mode, the supply pin may accidentally get disconnected, especially under harsh operating conditions.

When the device switches from supply powered to bus powered mode, the device shall operate with the same settings until the internal capacitor is able to provide the current draw required by the device for communication and the external pullup resistor can charge the internal capacitor during bus idle time. If the internal voltage on the capacitor drops below the brown-out threshold, the device shall switch itself off and enter bus powered mode

ADVANCE INFORMATION

of communication on subsequent power up. The device may not complete the ongoing communication during this time. When the device completes the power-up initialization sequence, as described earlier, the device shall respond to first bus communication starting with the bus reset sequence.

7.3.3 Bus Pullup Resistor

The bus pullup resistance value selected, is important for communication as per the speed mode and ensuring that minimal possible energy is consumed in the application. If the resistor value is too small, it may violate the V_{OL} limits on the SDQ pin.

The total SDQ pin and bus capacitance must be considered along with the bus leakage current when selecting the pullup resistor. The pullup resistance value selected must also ensure that the signal level reaches V_{IH} as per the timing requirements for standard and overdrive mode.

In bus powered mode of operation, the device charges its internal capacitor through the SDQ pin and the pullup resistor. This charge on the capacitor is used during bus communication, when the SDQ pin low. For other high current functions like thermal conversion and EEPROM access, the bus is held idle to ensure that the device can draw current through the pullup resistor. The SDQ pin voltage during the high current operation must be maintained to ensure sufficient operating margins. Use Equation 1 to calculate the pullup resistor value.

$$R_{PUR} < (V_{PUR} - 1.6\ V) \div I_{PU(MIN)} \quad (1)$$

When the device is used in V_{DD} or supply powered mode, a larger pullup resistor value may be used, as the SDQ pin is used only for communication. The user must ensure that the pullup resistor value selected must be able to support the timing for the required bus speed of operation.

For low current consumption devices like TMP1826, selecting the correct pullup resistor value allows the application to avoid low impedance current path components for bus powered mode of operation while maintaining communication speeds and device parameters as per its electrical specification.

7.3.4 Temperature Results

The conversion is initiated by the host MCU by sending the temperature conversion command if the automatic conversion is disabled, or immediately after the presence detect is completed when the automatic conversion is enabled, or in continuous conversion mode if the device is V_{DD} powered. At the end of every conversion, the device updates the temperature registers TEMP_RESULT_L, TEMP_RESULT_H and the STATUS register bits. As shown in Figure 7-2, the device supports a high precision and legacy format, which can be configured through the TEMP_FMT bit in the device configuration-1 register.

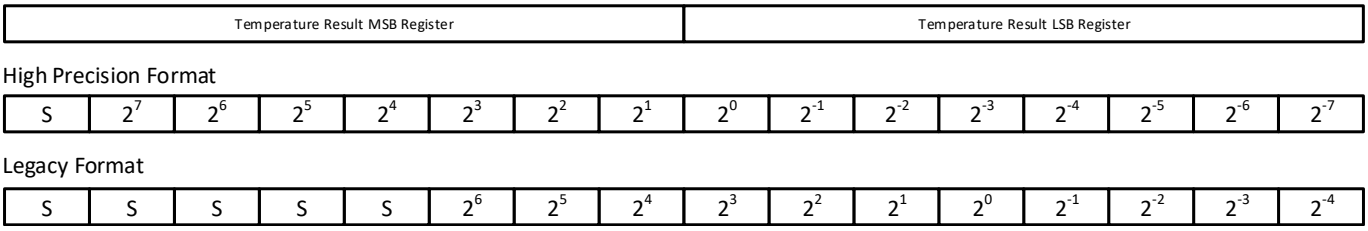


Figure 7-2. Temperature Format

If the format selected is the high precision 16-bit format, the data in the result registers is stored in two's complement form and has a resolution of 0.0078125°C. If the format selected is the legacy 12-bit format, the data in the result register is stored in sign extended form and has a resolution of 0.0625°C. The temperature register reads as 25°C in 16-bit mode before the first conversion. Table 7-1 shows examples of possible binary data that can be read from the temperature result registers and the corresponding hexadecimal and temperature equivalents for both formats.

Table 7-1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (PRECISION FORMAT)		DIGITAL OUTPUT (LEGACY FORMAT)	
	BINARY	HEXADECIMAL	BINARY	HEXADECIMAL
150	0100 1011 0000 0000	4B00	0000 0111 1111 1111	07FF

Table 7-1. Temperature Data Format (continued)

TEMPERATURE (°C)	DIGITAL OUTPUT (PRECISION FORMAT)		DIGITAL OUTPUT (LEGACY FORMAT)	
	BINARY	HEXADECIMAL	BINARY	HEXADECIMAL
127	0011 1111 1000 0000	3F80	0000 0111 1111 0000	07F0
100	0011 0010 0000 0000	3200	0000 0110 0100 0000	0640
25	0000 1100 1000 0000	0C80	0000 0001 1001 0000	0190
1	0000 0000 1000 0000	0080	0000 0000 0001 0000	0010
0.125	0000 0000 0001 0000	0010	0000 0000 0000 0010	0002
0.03125	0000 0000 0000 0100	0004	0000 0000 0000 0000	0000
0.0078125	0000 0000 0000 0001	0001	0000 0000 0000 0000	0000
0	0000 0000 0000 0000	0000	0000 0000 0000 0000	0000
–0.0078125	1111 1111 1111 1111	FFFF	0000 0000 0000 0000	0000
–0.03125	1111 1111 1111 1100	FFFC	0000 0000 0000 0000	0000
–0.125	1111 1111 1111 0000	FFF0	1111 1111 1111 1110	FFFE
–1	1111 1111 1000 0000	FF80	1111 1111 1111 0000	FFF0
–25	1111 0011 1000 0000	F380	1111 1110 0111 0000	FE70
–40	1110 1100 0000 0000	FC00	1111 1101 1000 0000	FD80
–55	1110 0100 1000 0000	F480	1111 1100 1001 0000	FC90

7.3.5 Temperature Offset

The temperature offset has the same format as the temperature result and is stored in the TEMP_OFFSET_L and TEMP_OFFSET_H registers.

The device, after every temperature conversion, shall apply the offset value, before the temperature is stored in the temperature result register. The host write to the registers can be stored in the device's configuration EEPROM, thereby reducing the overhead as the host does not need to reprogram the values at every power up. The offset features allow the device to achieve better accuracy at the temperature range for the application by performing a single point calibration.

7.3.6 Temperature Alert

The temperature alert feature uses the temperature alert low registers for low threshold comparison and temperature alert high registers for high threshold comparison. The format of the register is the same as the temperature results.

The device shall compare the result of the last conversion with the alert thresholds. If the temperature result is less than the low limit, or more than the high limits, then the device shall set the appropriate alert status flag for low or high temperature limits, in the status register. The alert status flags are cleared based on the ALERT_MODE setting in the device configuration-1 register.

Additionally, if the IO2 pin is configured as an alert pin, the alert status is reflected on the pin.

7.3.7 Standard Device Address

Every device comes with a unique 64-bit address that is factory programmed. This is described below.

7.3.7.1 Unique 64-Bit Device Address and ID

The device has a hard-coded, 64-bit address which is factory programmed and cannot be altered by the customer application. The unique 64-bit device address is used for device addressing in the end application and for NIST traceability. Figure 7-3 shows the format of the 64-bit address. When the host accesses the device or when the device sends its address, the 64-bit unique address is sent least significant bit first. The unique 64-bit address consists of 3 fields. The lower 8 bits consists of the device family code, followed by a 48-bit unique number and 8-bit CRC checksum on the 56 bits preceding it.

The device family code for TMP1826 shall read as 43h.

ADVANCE INFORMATION

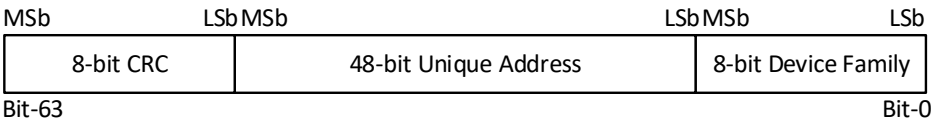


Figure 7-3. 64-Bit Device Address

7.3.8 CRC Generation

The TMP1826 implements a cyclic redundancy check (CRC) mechanism for data integrity check and communication robustness. Table 7-2 lists the properties of a 8-bit CRC.

Table 7-2. CRC-8 Rule

CRC-8 Rule	Attributes
CRC width	8 bits
CRC polynomial	$x^8 + x^5 + x^4 + 1$
Initial seed value	00h
Input data reflected	Yes
Output data reflected	Yes
XOR value	00h

When a new transaction is done, the shift register is initialized with the seed value of 00h and the data is shifted in LSB first. The CRC result is always part of the 64-bit unique address and is computed on the 56-bits that precede it. Additionally, when the host writes to the scratchpad-1 for the registers and scratchpad-2 for the memory, the device sends the CRC computed on the data bytes to provide a data integrity check for the host on the transaction. When the host reads the scratchpad-1 for reading the temperature register, the device shall append the CRC after the 8 bytes of scratchpad are sent.

The host must recalculate the CRC and compare it against the received CRC from the device. This is done by shifting the read data from the device along with CRC bits. If there is no bus error, then the shift register at the end of the bit shift will result in 00h. When writing the data to the device, the host must check the CRC received by processing the write data to ensure that there were no transmission errors and take appropriate corrective action before performing the next function.

7.3.9 Functional Register Map

The scratchpad-1 region and the IO register region together are referred to as the functional register map (see Figure 7-4). The scratchpad-1 region is 16 bytes deep, and consists of temperature result, device status, device configuration, stackmode address, temperature alert limit and temperature offset registers. The IO register region consists of the IO read and IO configuration registers. Some of the registers can be committed to the configuration EEPROM to ensure that the device setting are restored on power up without the host rewriting the configuration.

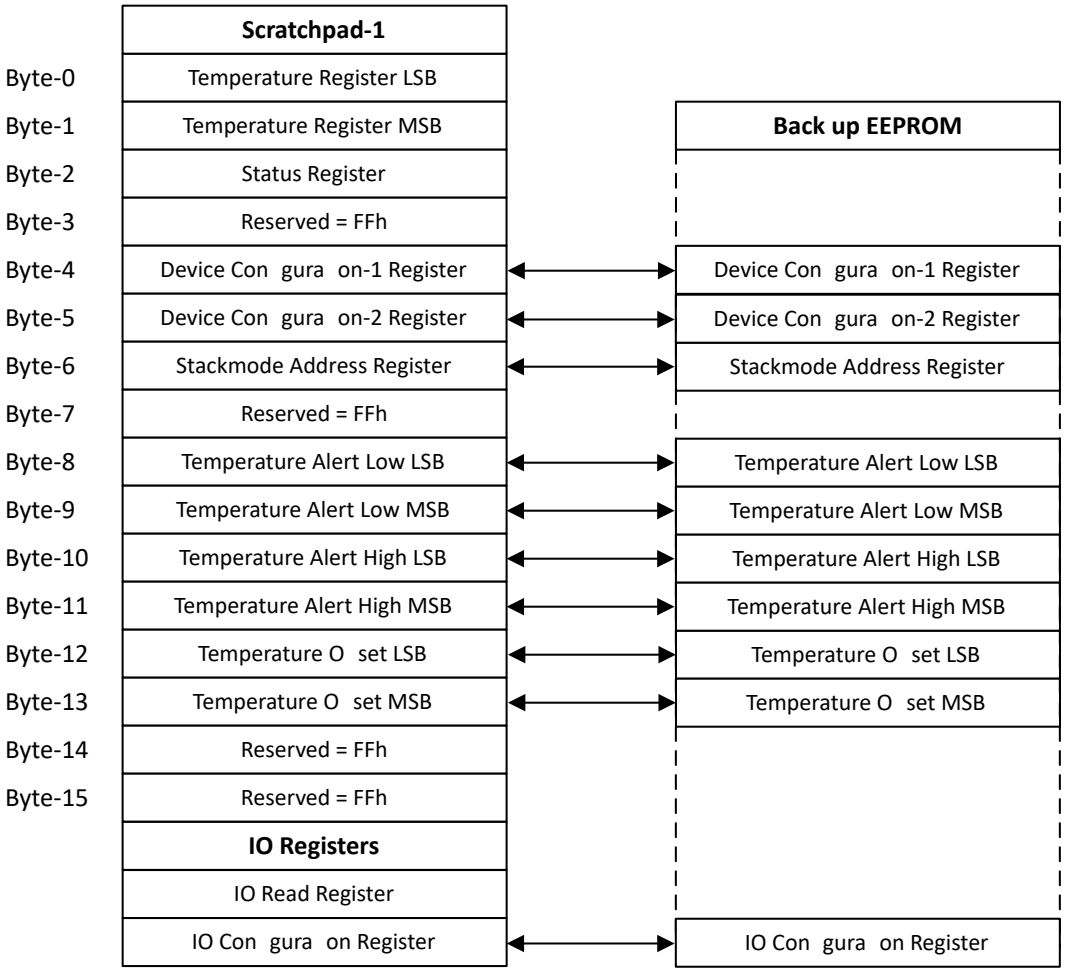


Figure 7-4. Functional Register Map (Scratchpad-1)

7.3.10 User Memory Map

The EEPROM memory is organized as 8 pages of 4 blocks each. Figure 7-5 shows that each block is 8 bytes or 64 bits. This results in a total user memory of 2048 bits. All memory access to the device shall be increments of a block size of 8 bytes. Access to the memory for programming is done through the scratchpad-2 register. The host writes to the scratchpad-2 register, which allows the device to perform a read before committing the content to the memory.

ADVANCE INFORMATION

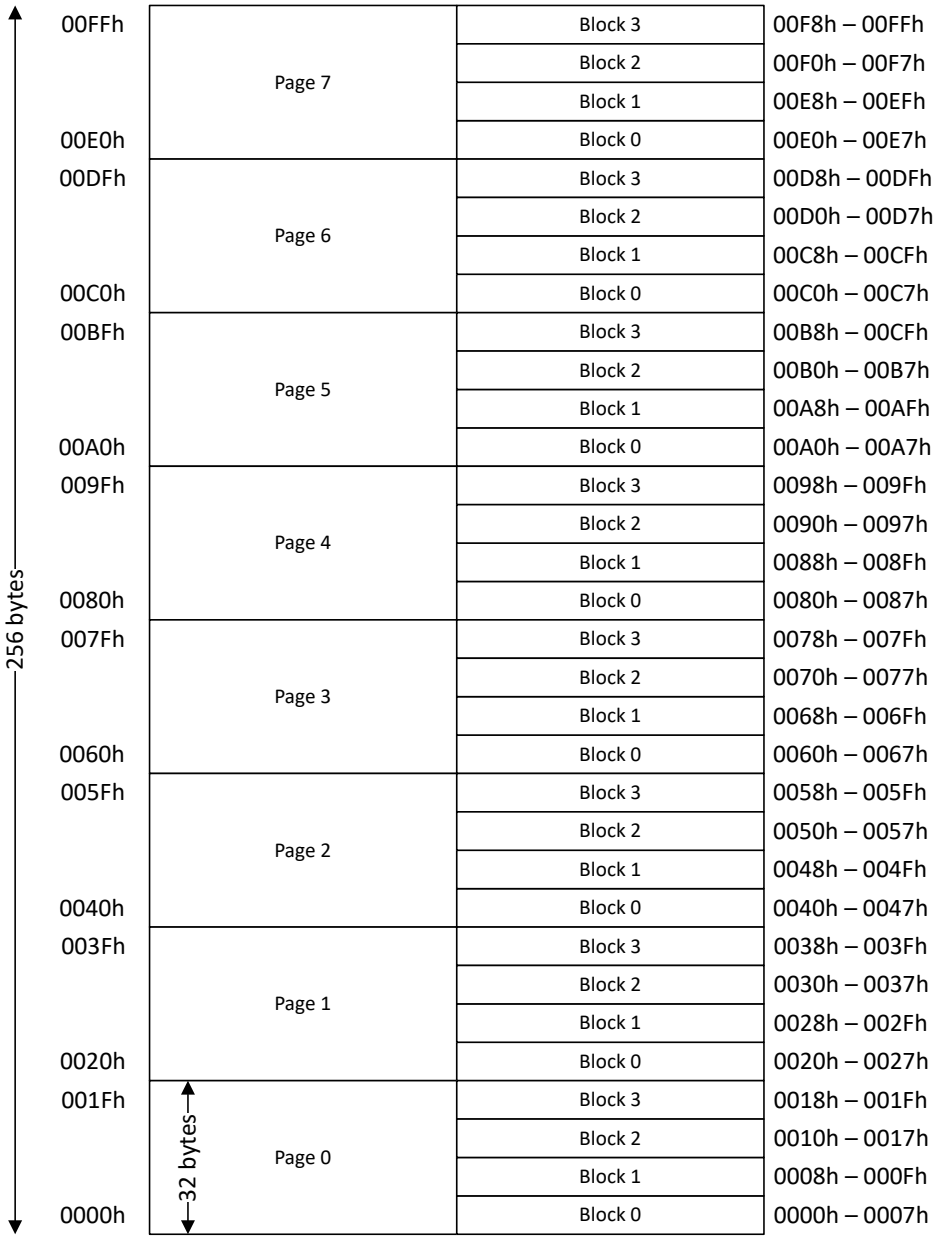


Figure 7-5. Address to EEPROM Page and Block Map

Note

The device shall return "1" for any device read without a CRC if the address is outside the user memory map.

7.3.11 Bit Communication

The single-wire interface communication does not have a reference clock, therefore all communication is performed asynchronously with fixed time slot (t_{SLOT}) and variable pulse width to indicate logic '0' and '1'. In idle state, the external pullup resistor holds the line high. All bit communication, whether it is a write or a read, are initiated by the host by driving the data line low to generate a falling edge and the bit value is decoded as the time for which the data line is held low or high after the falling edge.

Even though the communication is one bit at a time, the data exchanged between the host and device is performed at byte boundary. Every byte is sent least significant bit first. The device behavior is not ensured when incomplete bytes are sent.

7.3.11.1 Host Write/Device Read

A host write is the means by which the host sends the command, function and data to the device(s). A host write starts by the host driving the data line low as shown in Figure 7-6. If the host intends to transmit a logic '1', it releases the line after t_{WR1L} time. If the host intends to transmit a logic '0', it releases the line after t_{WR0L}. After releasing the data, the pullup resistor causes the line to become high till the beginning of the next time slot. The device samples the line after t_{RDV} has elapsed from the falling edge, for a time frame indicated by t_{DSW}. The host must factor the rise time due to the pullup resistor and bus capacitance to determine the release of the data line before the line is sampled by the device and the host drives the next write bit time slot.

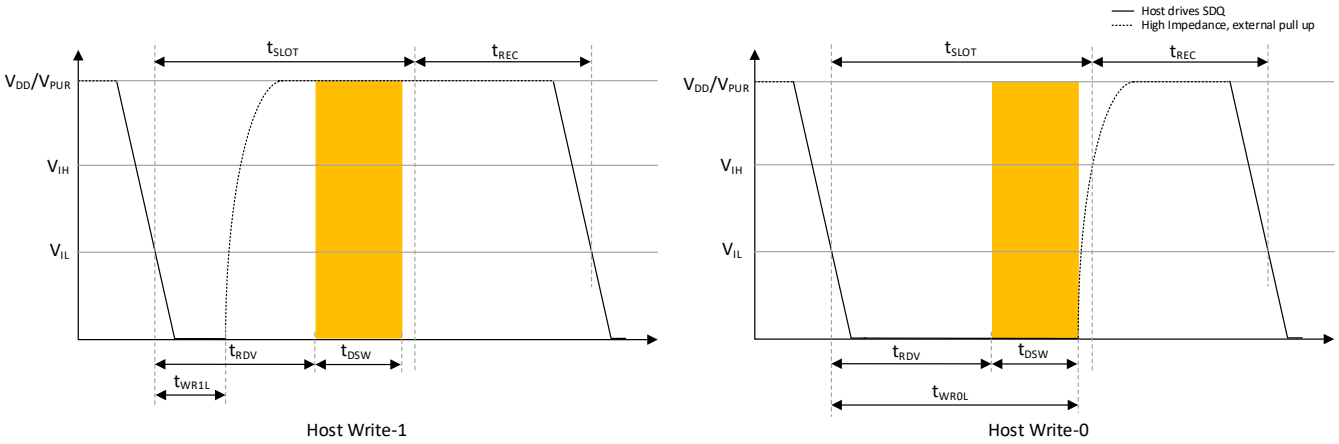


Figure 7-6. Host Write/Device Read

7.3.11.2 Host Read/Device Write

A host read is the means by which the hosts gets the data from the device or the CRC for data integrity check. A host read starts by the host driving the data line low as shown in Figure 7-7. When the device detects the falling edge, the device may drive the line low before the time t_{RL}. The host may release the bus from its side after the time $t_{RL(MIN)}$ elapses. If the device intends to transmit a logic '1', then it shall release the bus before $t_{RL(MAX)}$ elapses. If the device intends to transmit a logic '0', then it releases the bus after $t_{SLOT(MIN)}$. The host must sample the line after the time t_{RWAIT}, for a time frame indicated by t_{MSW}. The host must factor the rise time due to the pullup resistor and bus capacitance to determine the sampling window for the host to sample the bit level sent by the device or to drive the next read bit time slot.

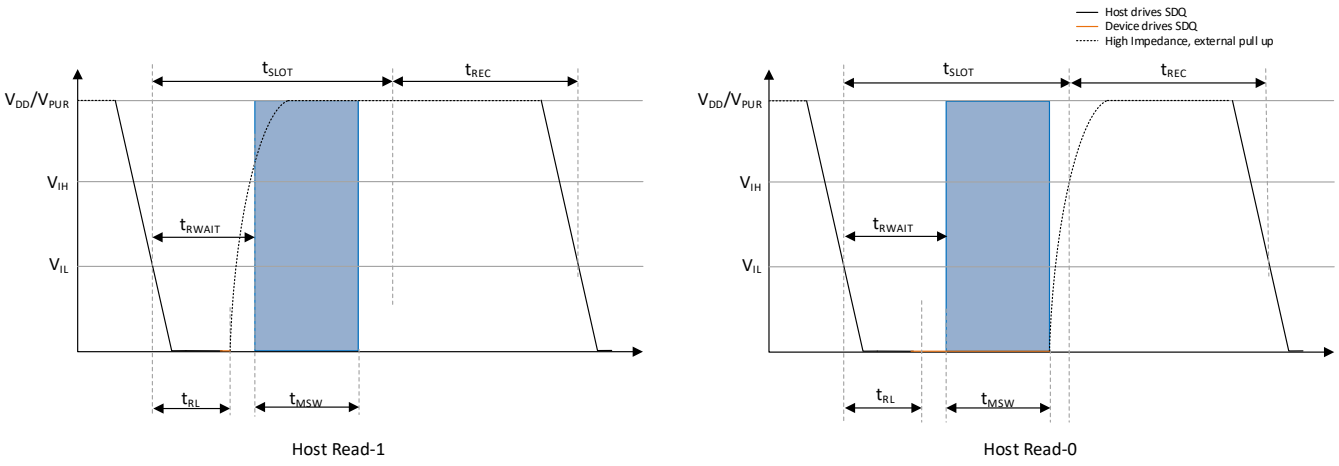


Figure 7-7. Host Read/Device Write

7.3.12 NIST Traceability

The accuracy of temperature testing is verified with equipment that is calibrated by an accredited lab that complies with ISO/IEC 17025 policies and procedures. Each device is tested and trimmed to conform to its respective data sheet specification limits.

7.4 Device Functional Modes

The TMP1826 device features flexible temperature conversion modes along with robust user EEPROM architecture, which is described in the sections below.

7.4.1 Conversion Modes

The TMP1826 supports both one-shot and continuous conversion modes. There are different methods for one-shot conversion modes, that may be used based on single device or multiple device bus network. The continuous conversion mode is only supported in V_{DD} powered mode. Each of the conversion modes are with single temperature sample, but the host can enable 8 samples averages in the device for improved accuracy.

7.4.1.1 Basic One-Shot Conversion Mode

The basic one-shot conversion mode is the default conversion mode. The device goes through a bus reset, address and function phase to initiate the temperature conversion. During the communication, the device is in shutdown mode. When the conversion request is registered by the device, the device starts active conversion and then goes back to low power shutdown mode as shown in Figure 7-8. If the device is in continuous conversion mode, then the one-shot conversion mode request is ignored.

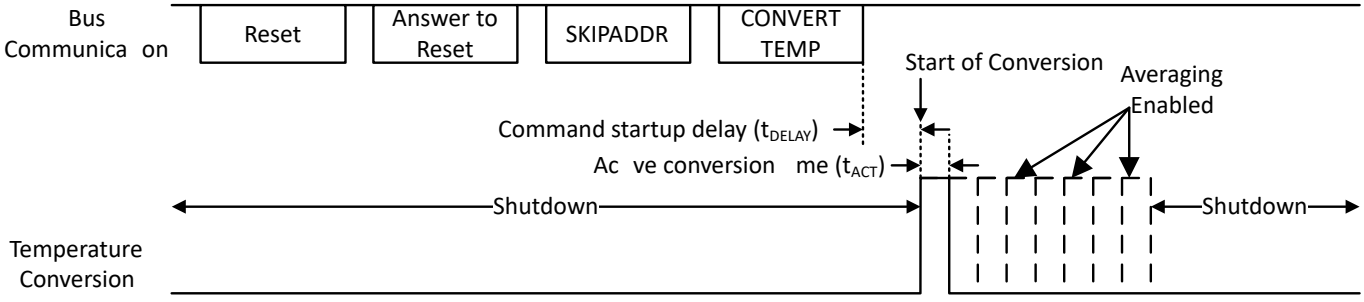


Figure 7-8. One-Shot Conversion Mode

As shown in Figure 7-9, there is no change in how one-shot conversion is performed when there are multiple devices on the bus. However, as there are multiple devices, the combined current drain in bus powered mode of operation may cause the bus voltage to drop. In such use cases, it is required that the host implement a low impedance current path using a FET/transistor switch. This path is switched on so as to meet the current

ADVANCE INFORMATION

requirement of the bus during an active conversion and after the active conversion duration is complete, it is switched off for bus communication.

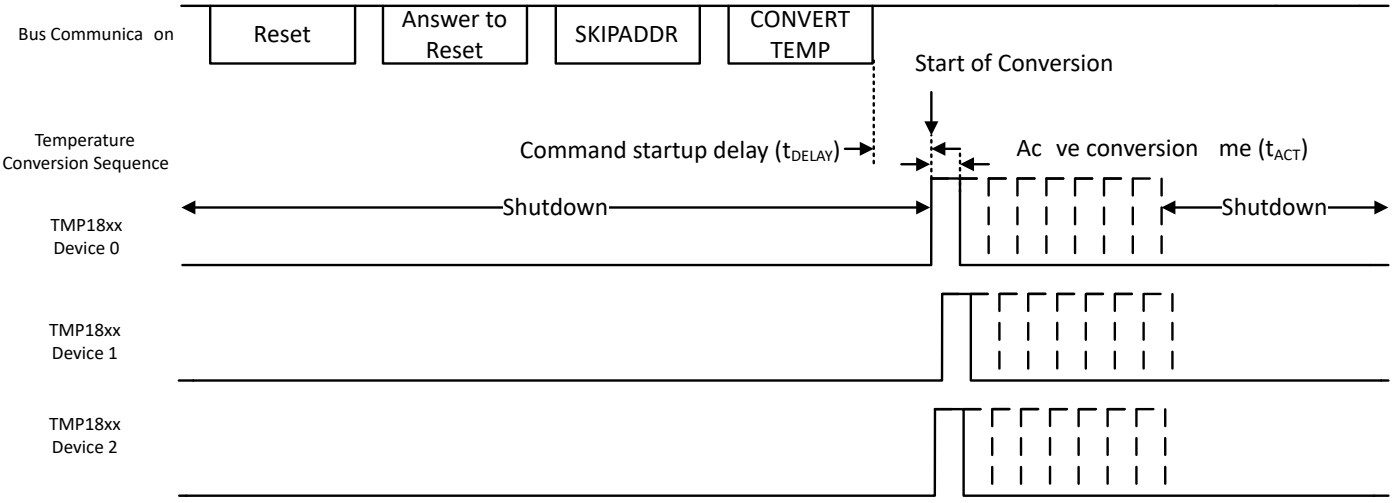


Figure 7-9. Multiple Device One-Shot Conversion Mode

7.4.1.2 Auto Conversion Mode

The auto conversion mode is a programmable feature in bus powered mode that can be enabled by setting the CONV_MODE_SEL as '10' in the device configuration-1 register. As shown in Figure 7-10, the host can skip the issue of the temperature conversion request and directly read the temperature data from the device when the auto conversion mode is enabled. This enables the application to speed up the temperature conversion and read, because the request command is no longer required. As in the case for multiple device bus, a low impedance current path is required to meet the current requirement of the bus during the active conversions.

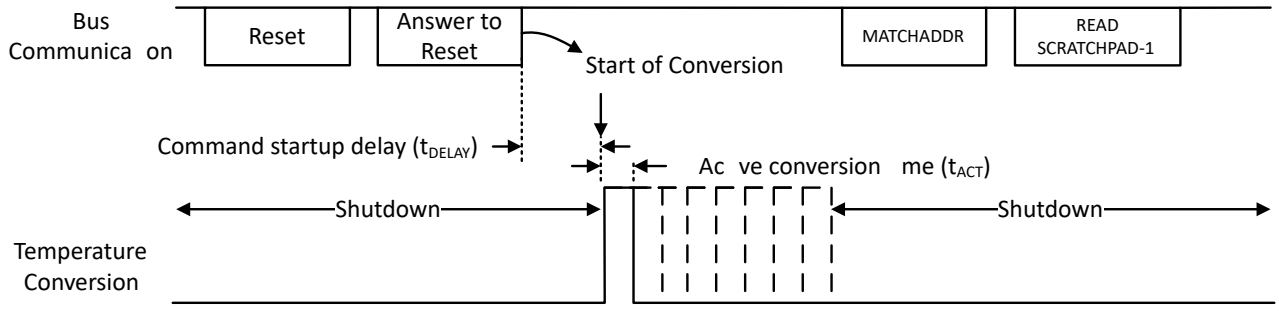


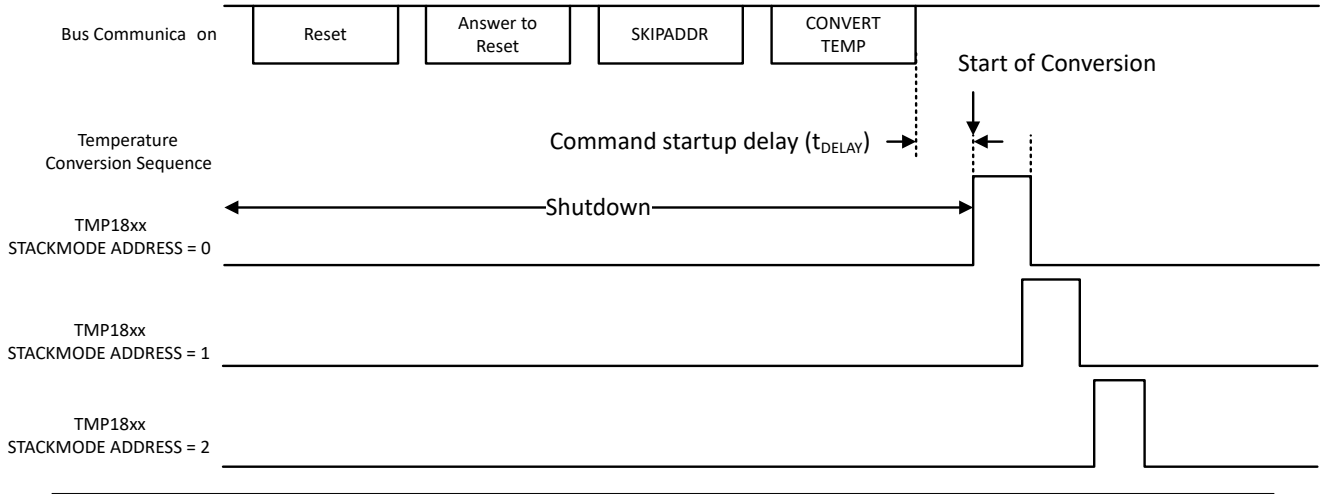
Figure 7-10. Auto Conversion Mode

7.4.1.3 Stacked Conversion Mode

The stacked conversion mode is a programmable feature in bus powered mode that can be enabled by setting CONV_MODE_SEL as '01' in the device configuration-1 register. As shown in Figure 7-11, the devices can use the address programmed in the stackmode address register to delay the temperature conversion for the devices when the stacked conversion mode is enabled. No more than two devices are actively converting at any given

ADVANCE INFORMATION

time, therefore the current drain in bus powered configuration is limited. This allows the application to avoid simultaneous temperature conversion by multiple parts and reducing the user system maximal supply current.



Note

The host controller must program all the device with the same setting for CONV_TIME_SEL and AVG_SEL to ensure that no more than two devices are actively converting to use the feature as it is intended.

Figure 7-11. Stacked Conversion Mode

7.4.1.4 Continuous Conversion Mode

The continuous conversion mode is applicable only in V_{DD} powered mode of operation for the device. This mode can be enabled by writing a value other than '000' to CONV_MODE_SEL bits in the device configuration-1 register. As shown in Figure 7-12, the device can perform periodic conversions at the interval programmed by the host and updates the temperature result register when continuous conversion mode is enabled. The device also performs the alert threshold check and sets the flags and alert pin, if configured accordingly. When in continuous conversion mode, the CONVERTTEMP function has no effect on the temperature conversion request. The application can at any time change the rate of conversion or put the device back into one-shot conversion mode, and this takes effect only after the current conversion is complete.

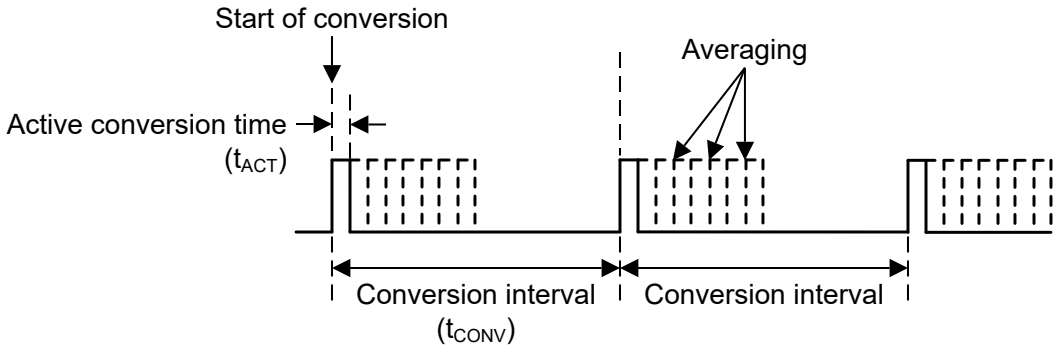


Figure 7-12. Continuous Conversion Mode

If due to any reason, the V_{DD} supply fails without the device going through a brown out, causing the device to move to bus powered mode of operation, the conversion mode automatically reverts to the setting in the configuration EEPROM.

ADVANCE INFORMATION

7.4.2 Alert Function

As described earlier, the built-in alert function can be used by the host to check if the temperature has crossed a certain threshold. The alert status bits are available in both bus powered and V_{DD} powered mode. The alert pin is available only in V_{DD} powered mode.

If the device is in V_{DD} powered mode and IO2 is configured to function as an ALERT pin, then the pin shall be driven active low when the threshold crossing occurs. The pin is open-drain, and therefore requires a pullup resistor. The ALERT pin deassertion is based on the setting of the ALERT_MODE setting in the device configuration-1 register.

7.4.2.1 Alert Mode

The device operates in alert mode, when the ALERT_MODE is set as '0'. In the alert mode of operation, the alert status flag and ALERT pin are asserted when the last temperature conversion is either higher than the temperature alert high limit or when it is lower than the temperature alert low limit register.

The alert status flag and ALERT pin are deasserted only when the host reads the status register or performs a successful ALERTSEARCH command as shown in Figure 7-13.

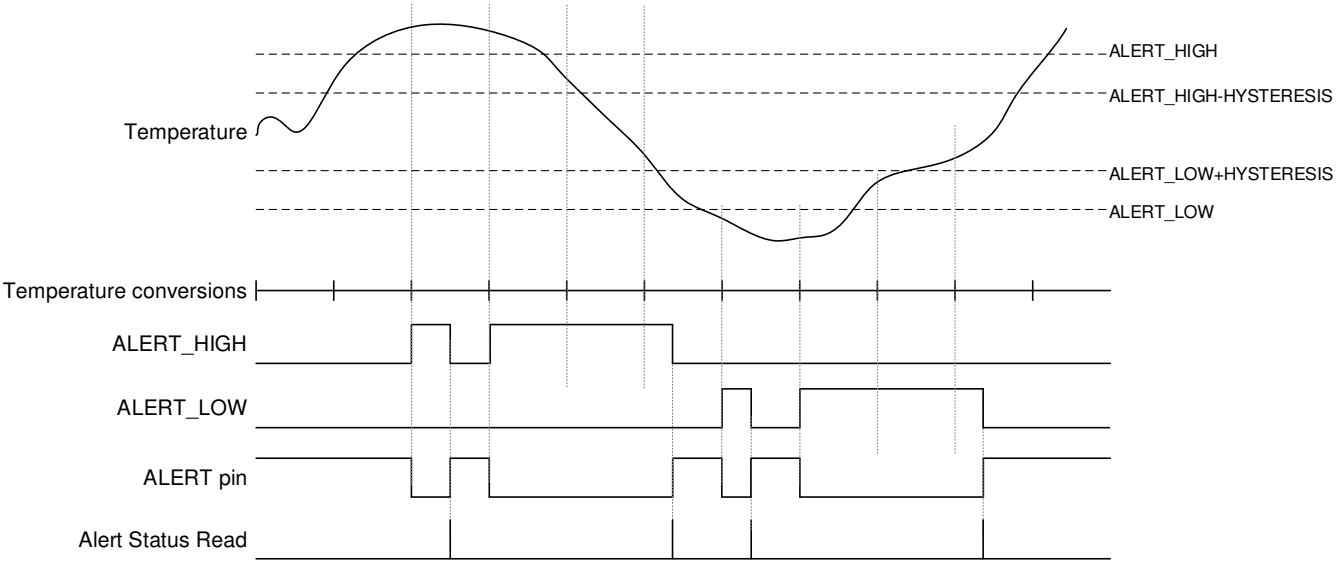


Figure 7-13. Alert Mode Timing Diagram

7.4.2.2 Comparator Mode

The device operates in comparator mode, when the ALERT_MODE is set as '1'. In the alert mode of operation, the alert status flag and ALERT pin are asserted when the last temperature conversion is either higher than the temperature alert high limit or when it is lower than the temperature alert low limit register.

The alert status flag and ALERT pin are deasserted only when the result of the last temperature conversion is less than the temperature alert high limit minus the hysteresis or above the temperature low limit plus the

ADVANCE INFORMATION

hysteresis as shown in Figure 7-14. The hysteresis is selectable using the HYSTERESIS bit field in the device configuration-2 register.

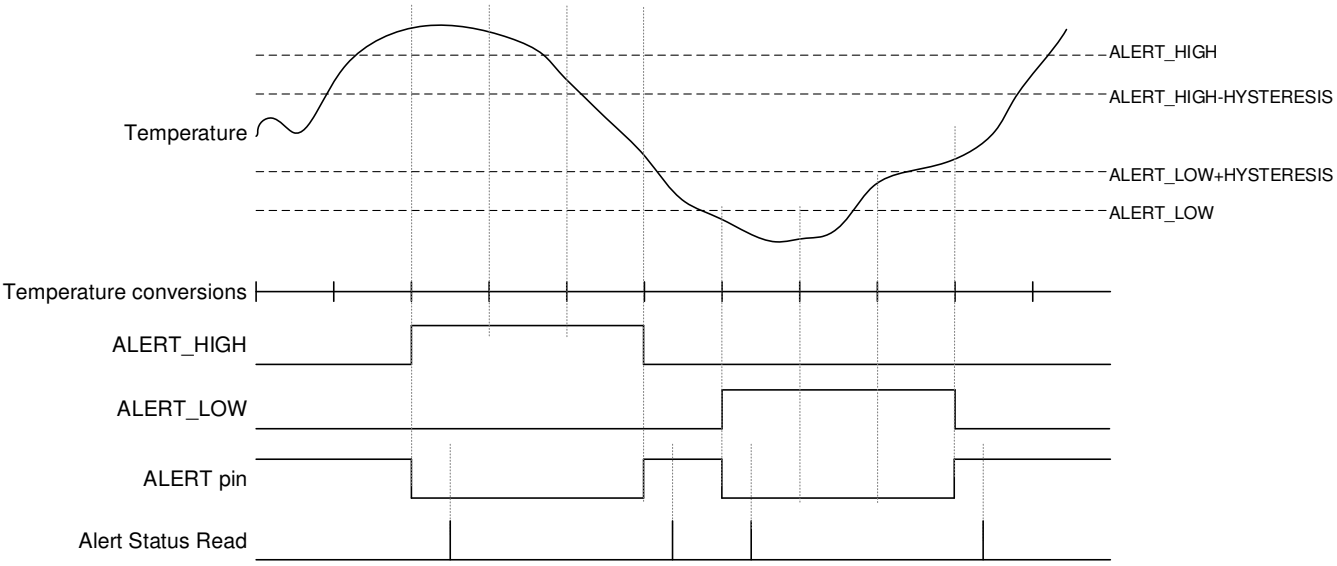


Figure 7-14. Comparator Mode Timing Diagram

7.4.3 Single-Wire Interface Communication

To leverage the features effectively, the device access consists of 3 distinct phases. As shown in Figure 7-15, any bus communication starts with a bus reset condition to which every device on the bus must respond. This is followed by a highly configurable address phase, where the host selects the device it wants to access. Finally, there is a function phase where the host provides the selected device(s) the action it wants to take.

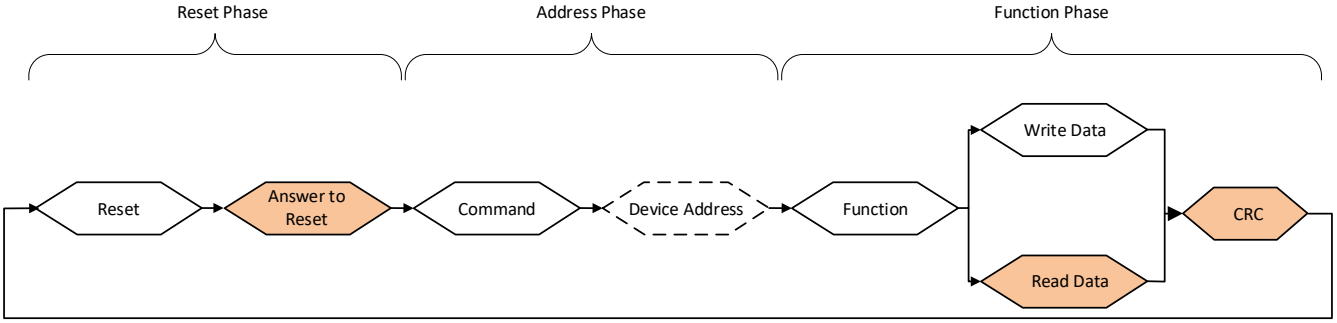


Figure 7-15. Single-Wire Bus Communication

In a single-wire bus, all write and reads are initiated by the host except for the answer to reset which is initiated by the devices on the bus.

7.4.3.1 Bus Reset Phase

The bus reset phase is the beginning of the communication. The phase is initiated by the host by holding the single-wire data line low for a period t_{RSTL}. All devices on the bus, irrespective of their current state shall respond to the bus reset, by reinitializing their internal state and responding to the host initiated bus reset. The devices respond after a minimum of t_{PDH}, by holding the single-wire low for a time period of t_{RSTH} as shown in Figure 6-1.

All devices are configured with the OD_EN bit set as '1' in the device configuration-2 register. If the host sends a bus reset pulse of 48 µs to 80 µs, then only devices operating in overdrive speed shall respond to the bus reset pulse, while devices operating in standard mode shall continue to wait for a standard mode bus reset.

If the host sends a bus reset pulse of minimum t_{RSTL} for standard mode, the device shall reset the OD_EN bit to '0' and respond to the bus reset in standard mode. If the bus consists of mixed standard and overdrive speed

devices, then sending a bus reset pulse in standard mode shall reset all devices to standard mode speed of operation.

It is illegal for the host to send the bus reset for a particular speed of operation and then communicate at the other speed mode. Also, if a bus reset pulse is sent which is greater than 80 µs (but less than 480 µs), then the device shall be reset, though the device operation is not ensured.

7.4.3.2 Address Phase

The address phase follows the bus reset phase as shown in Figure 7-16. During this phase the host presents 8-bit commands which may be followed by either host sending a 64-bit device addressor skipping the address. Some of the commands are used to discover the device address, while others are used to select the device.

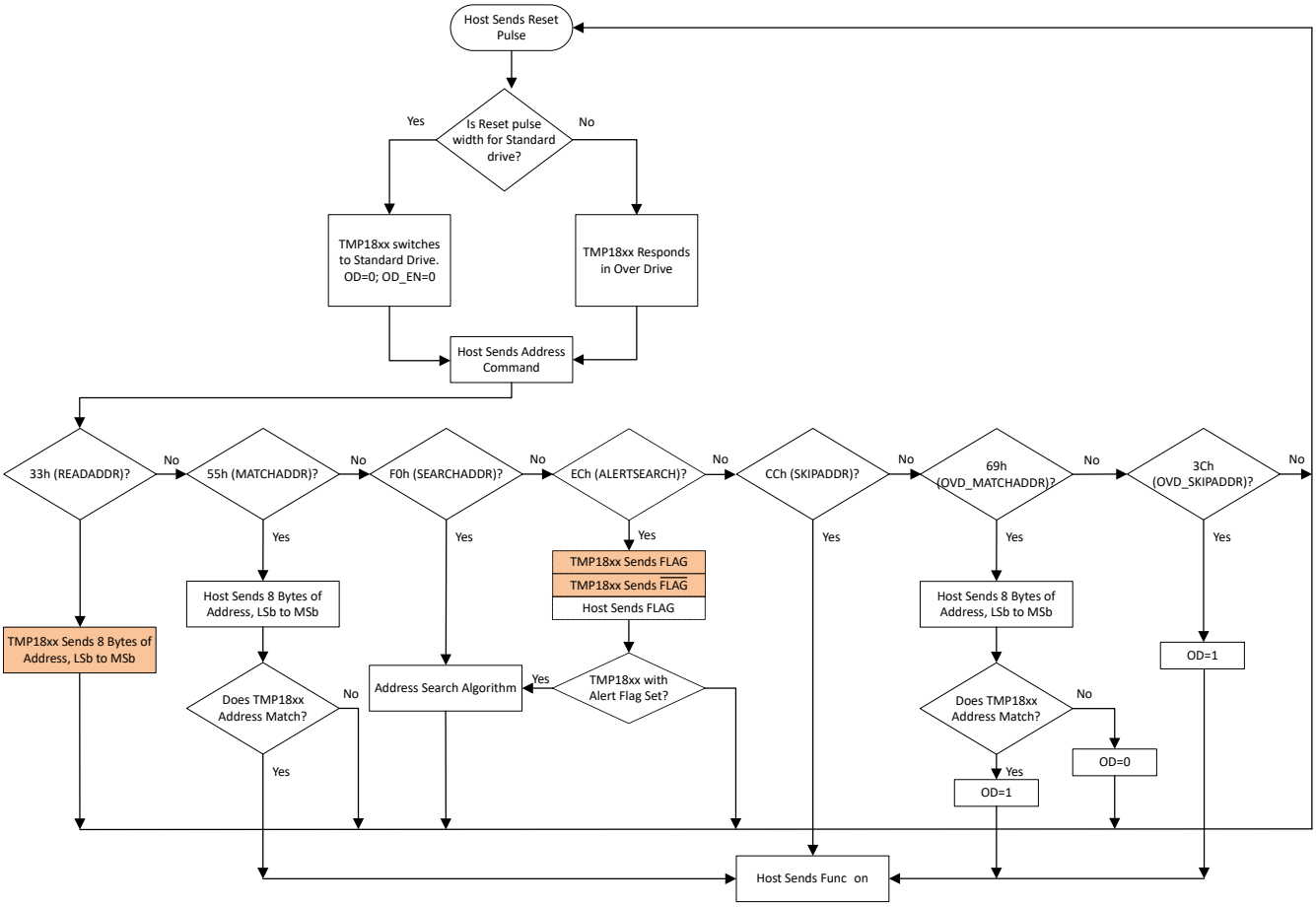


Figure 7-16. Address Phase Flowchart

7.4.3.2.1 READADDR (33h)

The command can be used by the host to read the 64-bit address of the device. This command must only be used when there is one device on the bus, as this command will cause a collision if multiple devices are present on the bus.

7.4.3.2.2 MATCHADDR (55h)

The command is used by the host and is followed by a 64-bit address that is used to select a single device on the bus. The address for each device is unique, therefore only one device can be selected by the command while all other devices continue to wait for a bus reset.

7.4.3.2.3 SEARCHADDR (F0h)

The command is used by the host to identify the 64-bit address of each of the devices on the bus after the system is powered up (see Figure 7-17). Additionally, this command may be run by the host to discover any

ADVANCE INFORMATION

new devices that may be added to the system later. When there is a single device bus, the host can skip the command and instead use the SKIPADDR command to access the device.

As shown in right side flow of Figure 7-17, when the fast arbitration mode is enabled by setting ARB_MODE bits as '11' in the device configuration-2 register, the devices check the bus for the transmitted bit. If the device reads a bit value other than what they had transmitted, they no longer respond to the command until the next bus reset. A device that wins the bus continues until the 64th bit, after which it does not respond to the next SEARCHADDR command until the arbitration mode is reenabled. The arbitration function allows the host a fast discovery of the devices without having to go through the complicated, memory intensive and longer discovery method using traditional SEARCHADDR command. At the same time, if the host has an issue on the bus, then it can simply perform a broadcast write to disable and enable the arbitration mode to restart the fast arbitration mode.

The device also features an optimized arbitration mode which is enabled by setting ARB_MODE bits as '10'. The devices check the transmitted bit, and if the devices detect a logic '0' when they send a logic '1', they do not participate in the SEARCHADDR command until the next SEARCHADDR command is sent. The device that is able to send all 64 bits successfully, wins the bus and does not participate in the arbitration till the mode is reenabled. As a result of the optimized arbitration mode, the host does not have to manage the complex memory structure to identify devices on the bus and can still use the legacy software search algorithm.

When the host has received the address of each device on the bus, the host must disable the arbitration mode and only enable it again if the host wants to use the SEARCHADDR command again when new devices are added to an existing bus.

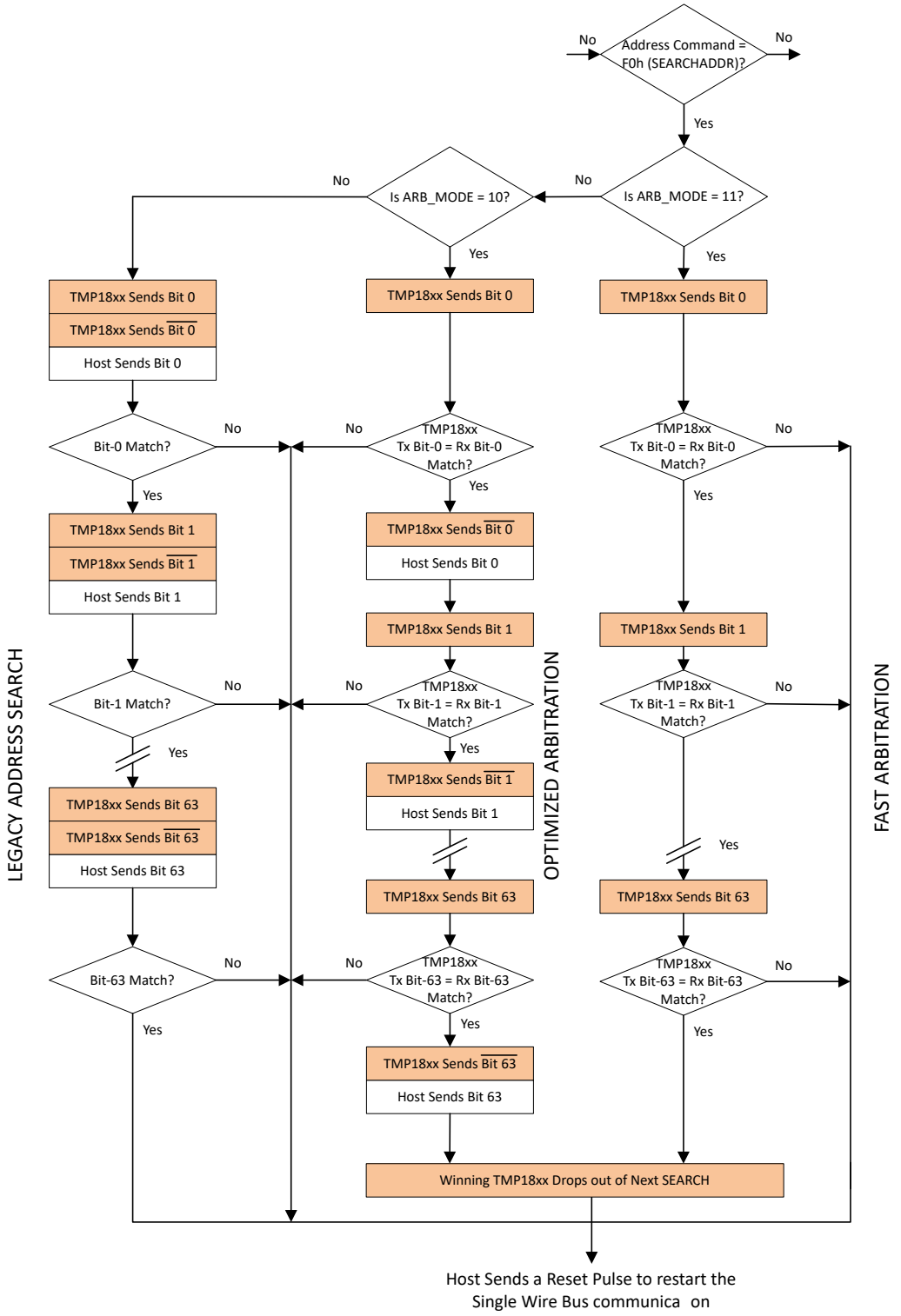


Figure 7-17. Address Search Algorithm Flowchart

7.4.3.2.4 ALERTSEARCH (ECh)

The command is used by the host to identify if any of the devices have an alarm condition that must be serviced. An alarm condition is set by the device when the temperature conversion is performed and the temperature result is higher than alert high temperature register or lower than alert low temperature register. The command uses the same method as the SEARCHADDR command, except that only devices with an alarm condition shall

ADVANCE INFORMATION

respond. If none of the devices have an alarm condition, then the host shall get all '1' followed by '1' on the bus and host can send a bus reset subsequently. If the device sends a '1' followed by '0', the host shall interpret it as either one or more devices have an alert condition, or all devices have an alert condition. If there is a bus noise, that causes the line to be sample erroneously, but if no device has an alert condition, then the host shall get all '1' on the bus during the address search phase.

Only devices that have an alert set shall participate when they receive an ALERTSEARCH address command and shall respond by sending its 64-bit address. A device shall no longer participate in the send address phase if it successfully transmits the device address, which automatically clears the internal alert flags, unless another temperature conversion results in the alert condition getting set.

7.4.3.2.5 SKIPADDR (CCh)

The host can issue this command to select all the devices on the bus. This is useful when the host wants to write to the scratchpad-1 or trigger the temperature conversion for all the devices on the bus. Additionally, the host can use the command to increase the overall bus data throughput when there is a single device on the bus.

The host must take care to not issue the command when there are multiple devices on the bus,. If the host intended to read the devices with this command, it would cause a collision on the bus.

7.4.3.2.6 OVD SKIPADDR (3Ch)

The host can issue this command to select all devices which support overdrive speed in a mixed speed bus. This is useful when the host wants to write to the scratchpad-1 or trigger the temperature conversion for all the devices on the bus that support overdrive speeds. Additionally, the host can use the command to increase the overall bus data throughput when there is a single device on the bus. When the command is issued, only devices that support overdrive mode shall set the internal OD flag as '1'.

The host must take care to not issue the command when there are multiple devices on the bus which support overdrive mode. If the host intended to read the devices with this command, it would cause a collision on the bus.

If the host issues a standard mode bus reset at any time, all devices which have OD flag set as '1' shall clear the same and revert back to standard mode speed.

7.4.3.2.7 OVD MATCHADDR (69h)

The command is used by the host and is followed by a 64-bit address that is used to select a single device on the bus in overdrive speed. The address for each device is unique, therefore only one device can be selected by the command while all other devices have to wait for a bus reset. The selected device shall set its internal OD flag as '1', and start all further communication in overdrive speed.

If the host issues a standard mode bus reset at any time, or selects another device using the OVD MATCHADDR, then all other devices which have OD flag set as '1' shall clear the same and revert back to standard mode speed.

7.4.3.3 Function Phase

The function phase follows the address phase as shown in Figure 7-18, Figure 7-19 and Figure 7-20. The host may present different functions during this phase, which is followed by either the host sending data to the device, reading device data, or starting a temperature conversion. Some of the functions may be broadcast to all the devices on the bus using SKIPADDR or OVD SKIPADDR. Read functions must always be unicast with a device selected during the address phase using MATCHADDR or OVD MATCHADDR. For cases, where there is a single device on the bus, the device address selection may be skipped.

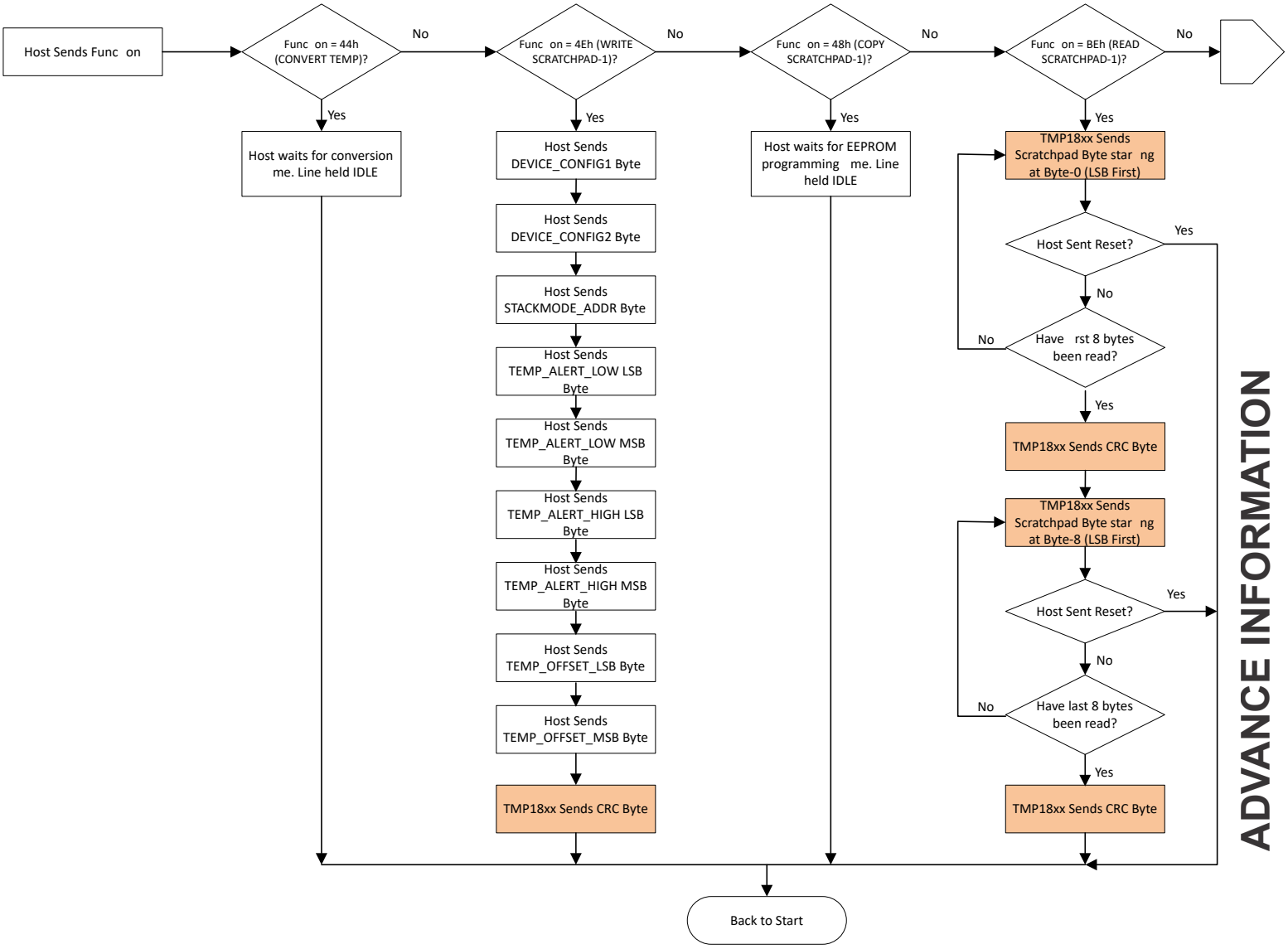


Figure 7-18. Function Phase Flowchart for Register Space

7.4.3.3.1 CONVERTTEMP (44h)

The function is issued by the host when the host wants the temperature sensors on the bus to perform a one-shot temperature conversion.

When the device is bus powered, the host must keep the bus idle for the duration of the active temperature conversion. The active temperature conversion time is dependent on the conversion mode. After temperature conversion has completed, the result is updated in temperature result LSB and temperature result MSB registers.

When automatic temperature conversion mode is enabled in the device configuration-1 register, the command may be skipped altogether, allowing faster access to the temperature result.

7.4.3.3.2 WRITE SCRATCHPAD-1 (4Eh)

The function is issued by the host to write the functional register for the temperature sensor. Following the function byte, the host transmits the device configuration registers, stackmode address register, temperature alert low limit registers, temperature alert high limit registers and temperature offset registers. After sending the 9 bytes, the device shall transmit the CRC computed on the 9 bytes and send the CRC back to the host for quick verification of data integrity.

Additionally, the host can issue a bus reset at any time during the transfer, though it is advised that the same may be done only at byte boundary to ensure that there is no register corrupted due to incomplete transfer.

Note

When updating the OD_EN and/or LOCK_EN bit in the device configuration-2 register, the host controller must send the 9 bytes and wait for the CRC transmission before the change of device speed or write protection of the register scratchpad can take effect. If the host terminates the transfer before the complete CRC transmission, then any update to OD_EN and/or LOCK_EN shall not take effect.

7.4.3.3.3 READ SCRATCHPAD-1 (BEh)

The function is issued by the host to read the temperature result, status bits, and functional registers from the register scratchpad. The selected device transmits the first 8 bytes of the register scratchpad followed by CRC of the 8 bytes. If the host wants to continue the read operation, the host will receive the next 8 bytes along with CRC for the last 8 bytes. The host can terminate the function at any point by issuing a bus reset.

7.4.3.3.4 COPY SCRATCHPAD-1 (48h)

The function is issued by the host to copy the functional registers content to the EEPROM. As shown in Figure 7-18, the temperature alert registers, configuration register, stackmode address register, and temperature offset registers are stored in the configuration EEPROM. There are 9 bytes being copied from the register space to the NVM, therefore the host must hold the bus in idle state for twice the EEPROM programming time before it performs the next access.

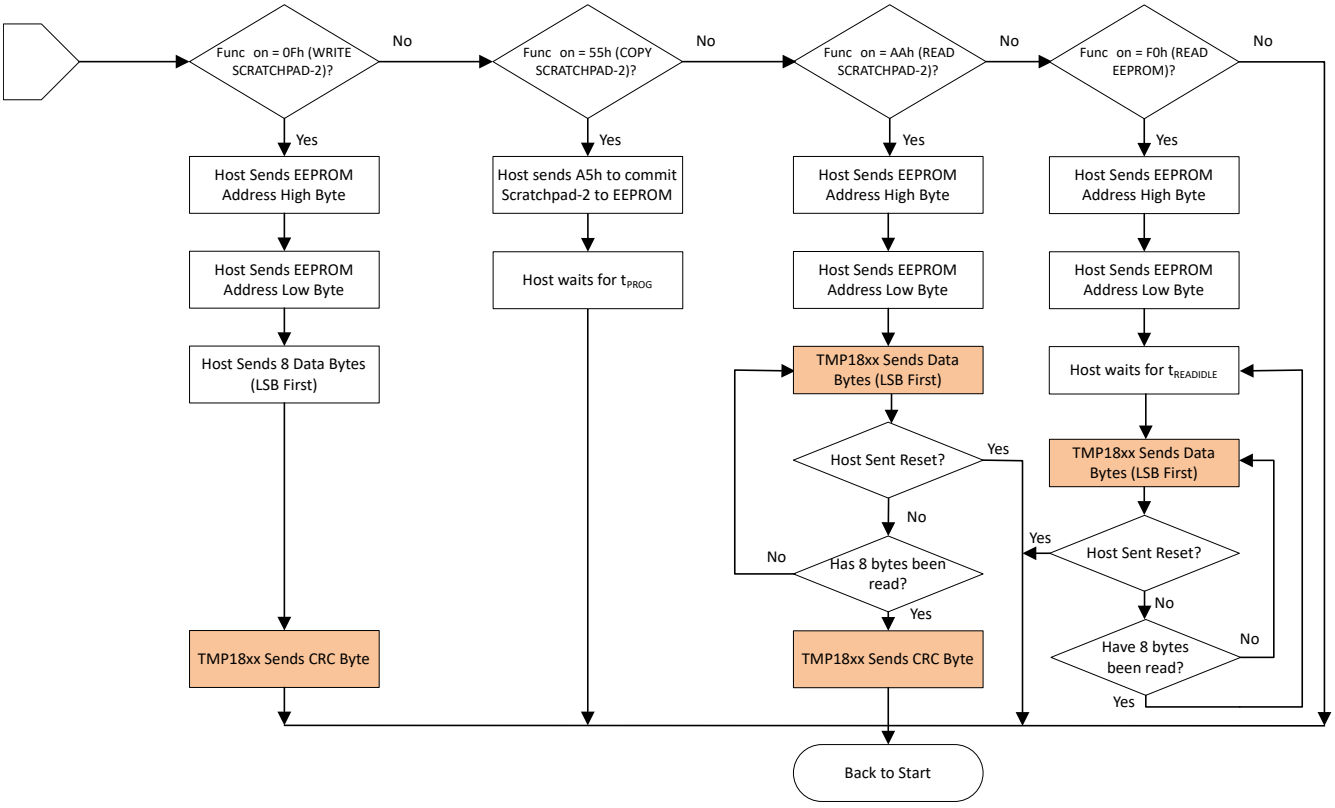


Figure 7-19. Function Phase Flowchart for Memory Access

7.4.3.3.5 WRITE SCRATCHPAD-2 (0Fh)

The function is issued by the host to prepare data write to the EEPROM using memory scratchpad.

The host first sends the 2 bytes for the EEPROM address as shown in Figure 7-19, followed by the 8 data bytes. On receiving the 8 data bytes, the device computes the CRC for total of 10 bytes of address and data received from the host for data integrity check. The function only copies the data to the memory scratchpad, to enable the

host to change data, before the final EEPROM erase and program. Additionally, the host may use the memory scratchpad as a 8-byte volatile buffer.

The device does not support byte wise access for EEPROM. All access to the scratchpad are done in increments of 8 bytes. Hence the host must send the address at the 8-byte block boundary. Any attempt to write data at a non-block boundary shall result in data being corrupted in the corresponding EEPROM page and block as shown in Figure 7-5.

7.4.3.3.6 READ SCRATCHPAD-2 (AAh)

The function is issued by the host to read the content of the memory scratchpad.

The host first sends the 2 bytes for the EEPROM address (see Figure 7-19). If the 2 bytes of address matches the address sent during the last WRITE SCRATCHPAD-2, the device responds by sending the 8 bytes of data that was written to the scratchpad-2 buffer earlier. The host can send a bus reset any time during the transfer. If the device sends all 8 bytes and no bus reset is received,the device transmits the CRC computed on the 2 byte of address sent by the host and 8 bytes of data sent by the device to the host for data integrity check.

If there is a mismatch in the address, the device shall go back to the start and wait for a bus reset to restart communication, and the host shall receive '1' on the bus for any subsequent read. This mechanism ensures that the host can detect an address byte corruption during both WRITE SCRATCHPAD-2 and READ SCRATCHPAD-2, as both the data bytes and CRC byte will read back as FFh.

7.4.3.3.7 COPY SCRATCHPAD-2 (55h)

The function is issued by the host to copy the contents of scratchpad-2 to the EEPROM. The EEPROM current is higher during the erase and program, therefore the application must size the external pullup resistor to ensure that there is sufficient current drawn by the multiple devices or implement a low impedance current path using an external FET/transistor switch parallel to the bus pullup resistor.

The host application must ensure that only WRITE SCRATCHPAD-2 or READ SCRATCHPAD-2, with address of the intended location in the user EEPROM, are issued before COPY SCRATCHPAD-2 is sent. The device stores and uses the address sent during WRITE SCRATCHPAD-2 to identify the location in the user EEPROM where the copy operation shall be performed. The host only needs to send one byte with A5h to initiate the copy of the memory content from scratchpad-2 to the user EEPROM, at the address location already specified, when performing the commit operation. The host must hold the bus in idle state for the EEPROM programming time before starting any new access on the bus.

7.4.3.3.8 READ EEPROM (F0h)

The function is issued by the host to read the EEPROM memory directly.

The host sends 2 bytes for the address of the EEPROM location, that it wants to read. The device then sends the data bytes starting from that location until the internal address pointer does not reach the end of the EEPROM or host does not issue a bus reset. If the internal address pointer reaches end of the EEPROM location, the device shall send 1's on the bus. After sending the 2 bytes for the address of the EEPROM location to access, and when moving between block boundary, the host must idle the bus for t_{IDLE} as specified in the EEPROM characteristics. Additionally, there is no CRC provided in the response from the device during the READ EEPROM function.

The device does not support byte wise access for EEPROM. All access to the memory is done in increments of 8 bytes. Hence the host must send the address at the 8-byte block boundary. Any attempt to read data to

ADVANCE INFORMATION

the scratchpad at a non-block boundary shall result in data being sent from the start of the block boundary corresponding to the address as shown in Figure 7-5.

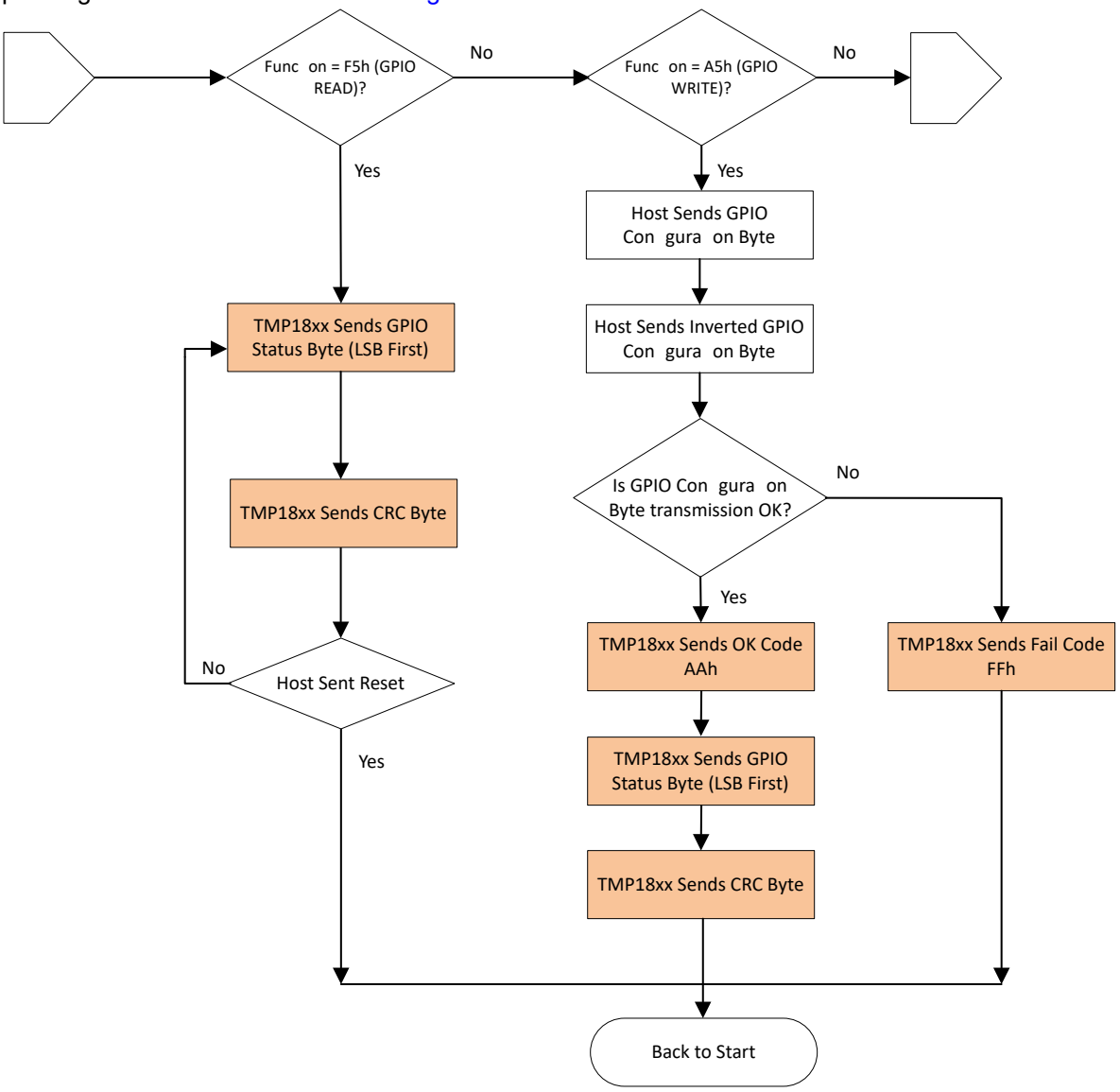


Figure 7-20. Function Phase Flowchart for IO Access

7.4.3.3.9 GPIO WRITE (A5h)

The function is issued by the host to configure and read the GPIO.

The host sends the IO configuration byte, followed by the inverted IO configuration byte value. This enables the device to check for bit error due to bus noise. If there errors detected, then the device shall transmit a fail code of FFh to the host, for the host to retry. If there are no errors detected, then the device shall transmit the success code of AAh. The host may issue a bus reset and terminate the transaction or may proceed to read of the IO state, where the device shall send the IO read byte, followed by the CRC byte for the IO status byte.

The host must send a bus reset to terminate the function and bring the device back to its idle state.

7.4.3.3.10 GPIO READ (F5h)

The function is issued by the host to read the GPIO.

After issuing the function, the device sends a byte which has the corresponding IO status, followed by the CRC for the IO status byte. The host may repeat the sequence or may send a bus reset to terminate the function.

7.4.4 NVM Operations

The TMP1826 device follows a common procedure for programming user data and enabling the memory protection for user data.

7.4.4.1 Programming User Data

Programming of user data to the memory use the functions WRITE SCRATCHPAD-2, READ SCRATCHPAD-2 and COPY SCRATCHPAD-2 as described earlier. The application must use the address in the provided functional memory map to write user data to the device.

1. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
2. Host issues a WRITE SCRATCHPAD-2 with the address as per the functional memory map and the 8 bytes of data.
3. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
4. Host issues a READ SCARTCHPAD-2 with the address as per the functional memory map, then reads the 8 bytes of data to ensure that it is same as what was written in the earlier step.
5. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
6. Host issues a COPY SCRATCHPAD-2 with the data bytes as A5h to commit the data to user EEPROM.

7.4.4.2 Register and Memory Protection

The TMP1826 provides user configurable protection for both the register scratchpad and the memory region as described below.

7.4.4.2.1 Register Protection

The device provides for a one-time write protection for the entire register map. All the writable registers, except for IO configuration, can be write-protected. To enable the write protection permanently, the host controller must set LOCK_EN bit in the device configuration-2 register, then copy the register to the configuration EEPROM. When the configuration EEPROM is programmed, the change is permanent and irreversible.

Additionally, the device provides temporary write protection mechanism. If the LOCK_EN bit is not committed to configuration EEPROM, the device shall prevent any write to the register scratchpad-1 region as long as power is applied. If the device goes through a POR, then the LOCK_EN bit shall be cleared to allow the host to update the register scratchpad-1.

7.4.4.2.2 User Memory Protection

The device provides a configurable one-time memory protection mechanism. Memory protection is available at page level of 32 bytes of 256 bits. There are two levels of memory protection that are available on the TMP1826:

- Public Read and Write: This is default memory option for factory-programmed parts. The host controller can read and write without any additional steps.
- Public Read with write protection: In this mode, the host controller can read the memory without any specific steps, but write access is not allowed.

Each page can be protected using a special address described below:

Table 7-3. User Memory Protection

USER MEMORY PROTECTION ADDRESS		COMMENTS
PROTECTION LEVEL OPERAND	PAGE NUMBER FIELD	
80h	00h	User memory page-0 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	01h	User memory page-1 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	02h	User memory page-2 cannot be erased and programmed in any mode. Public mode read access is allowed.

ADVANCE INFORMATION

Table 7-3. User Memory Protection (continued)

USER MEMORY PROTECTION ADDRESS		COMMENTS
PROTECTION LEVEL OPERAND	PAGE NUMBER FIELD	
80h	03h	User memory page-3 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	04h	User memory page-4 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	05h	User memory page-5 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	06h	User memory page-6 cannot be erased and programmed in any mode. Public mode read access is allowed.
80h	07h	User memory page-7 cannot be erased and programmed in any mode. Public mode read access is allowed.

The memory protection bits can be programmed only one time. Hence after a page is locked, it cannot be unlocked. The method to lock a user memory page in public read-only with write protection is described in the following sequence:

1. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
2. Host issues a WRITE SCRATCHPAD-2 with the address as 80XXh, where XX is the page number, and data byte as 55h.
3. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
4. Host issues a READ SCRATCHPAD-2 with the address as 80XXh, where the XX is the page number and reads the data byte to ensure it is 55h.
5. Host issues a bus reset, then waits for the response and sends the address command for the specific device.
6. Host issues a COPY SCRATCHPAD-2 with the data byte as A5h to commit the protection for the page.

7.5 Programming

The TMP1826 has multiple methods in which an application can access the device functions for temperature conversion and EEPROM programming. When accessing multiple device the MATCHADDR command must be used.

The sections below describe the sequences that must be followed to access the device functions properly.

7.5.1 Single Device Temperature Conversion and Read

Figure 7-21 shows the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result. As the temperature results are the first two bytes of the register scratchpad, the host may optionally stop the read after the device transmits the first two bytes by performing a bus reset.

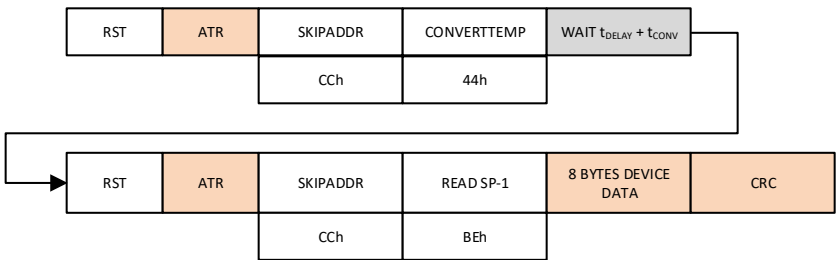


Figure 7-21. Single Device Temperature Conversion and Read Programming Flow

7.5.2 Multiple Device Temperature Conversion and Read

Figure 7-22 shows the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result for multiple devices. The host must use the MATCHADDR command to address each device on the bus, because the devices do not arbitrate on a read function.

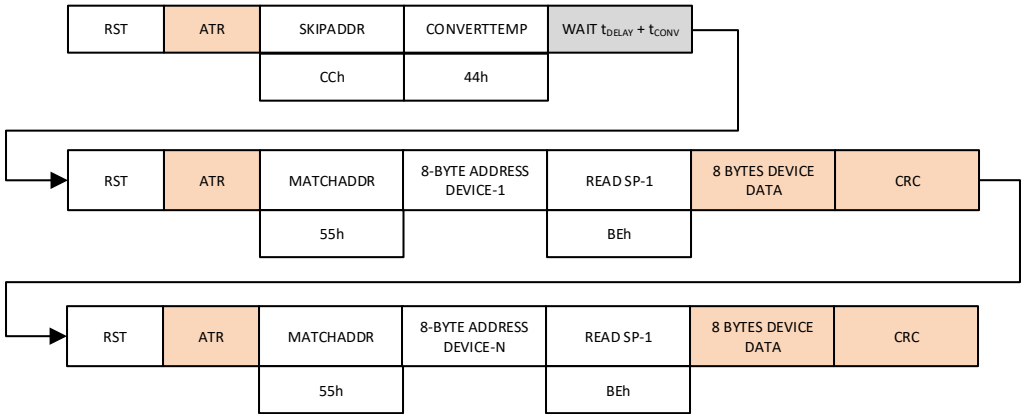


Figure 7-22. Multiple Device Temperature Conversion and Read Programming Flow

7.5.3 Register Scratchpad Update and Commit

Figure 7-23 shows the sequence the host must execute to update the register scratchpad and commit to the configuration EEPROM. The host must read the scratchpad to ensure it can perform the correct read modify write to the register locations, before it commits the same to the configuration EEPROM.

If the host has only one device, or if the application can guarantee no bus corruption, then it may use SKIPADDR command to globally update and commit the register scratchpad region. However once committed and locked, it is not possible for the host to update the locations anymore, and hence TI strongly advises that the host still read the locations before running the commit operation.

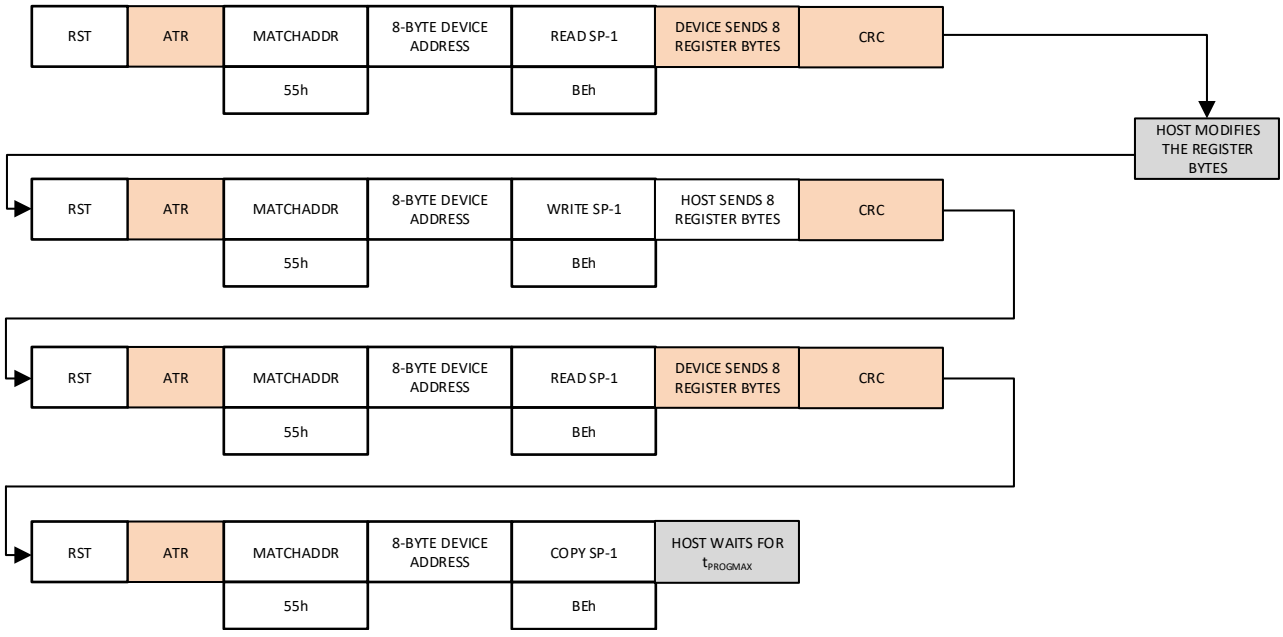


Figure 7-23. Register Scratchpad Update and Commit Programming Flow

ADVANCE INFORMATION

7.5.4 Single Device EEPROM Programming and Verify

Figure 7-24 shows the correct procedure the host must execute to update the EEPROM. When communicating with a single device, the host may use the SKIPADDR command. However when communicating with multiple devices, the host must use the MATCHADDR command to address the correct device. The host writes to the EEPROM scratchpad first, then reads it back to verify the content before it commits the same to the user EEPROM. The host shall repeat the sequence for every 8 byte page. After the locations are programmed, the host may issue an READ EEPROM function with the start address to read all the bytes. The device shall read back the bytes in page size and put a CRC byte after every page to ensure that the host shall be able to identify bit corruption using the CRC over a smaller data packet.

As long as the host continues the read operation, the device shall read back 8 bytes of data followed by a CRC byte. When the device reaches the end of the EEPROM block, the device shall return all 1's to the host.

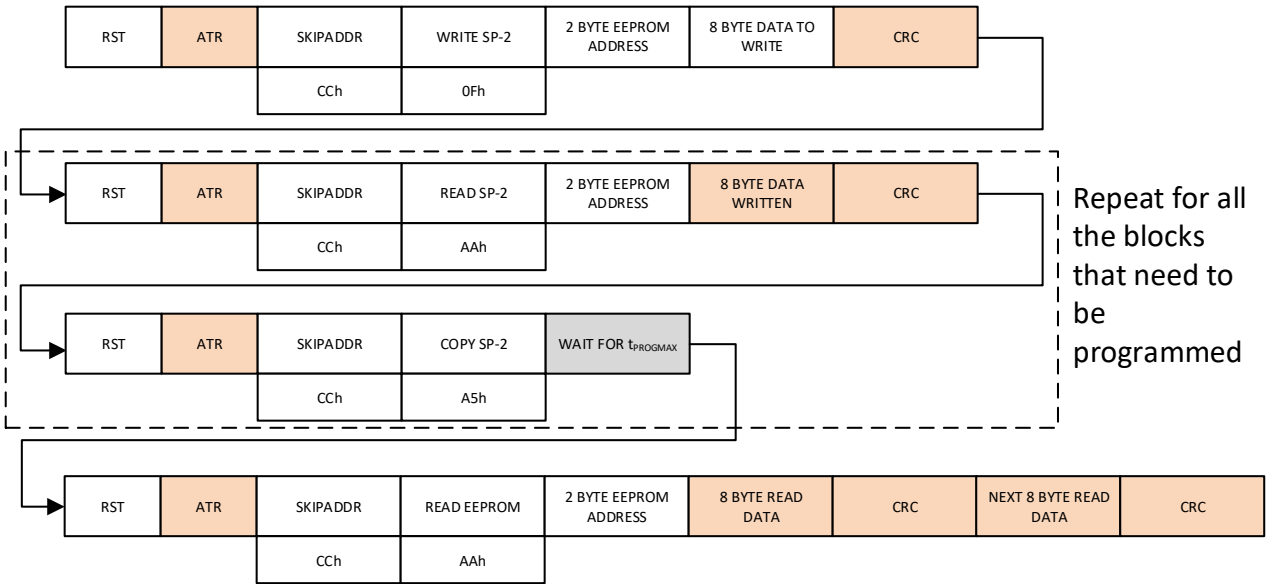


Figure 7-24. Single Device EEPROM Programming and Verify Flow

7.5.5 Single Device EEPROM Lock Operation

When the device EEPROM is successfully programmed as shown in Figure 7-24, the host shall execute the sequence, as shown in Figure 7-25, to write-protect the EEPROM block.

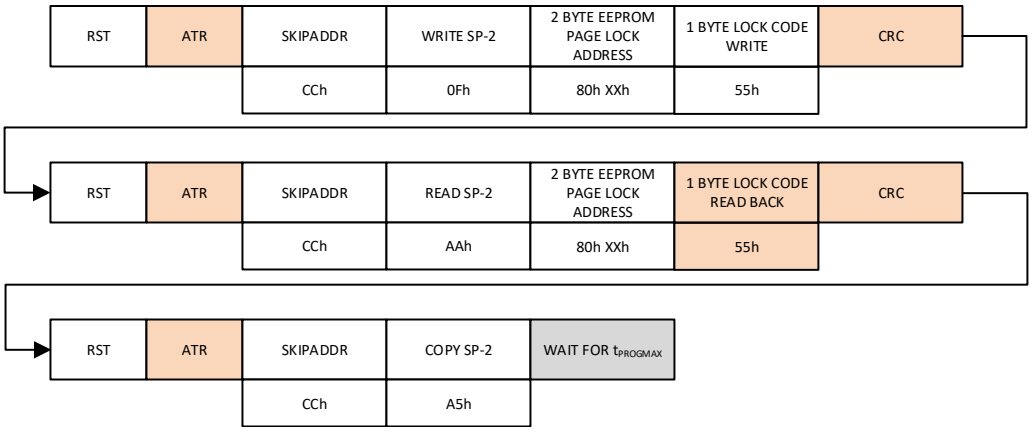


Figure 7-25. Single Device EEPROM Lock Operation Flow

7.5.6 Multiple Device IO Read

Figure 7-26 shows the program flow that the host MCU must execute for reading the IO from a device. The host selects the device it wants to communicate with and issues the GPIO READ function. The host must wait for the time it takes for the device to sample the IO, by keeping the bus idle, before the device returns the IO read register value along with the CRC for the byte. The device at this point shall again sample the IOs. If the host issues a bus reset during the sampling time, the device shall terminate the update process and it will hold the last sampled value. If the host continues, then the new sampled values shall be sent back by the device.

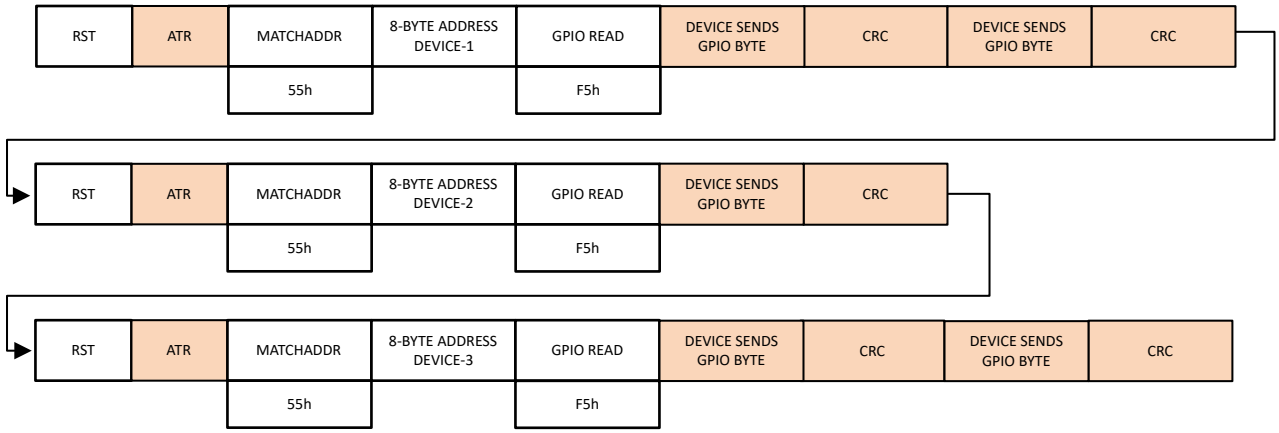


Figure 7-26. Multiple Device GPIO Read Flow

7.5.7 Multiple Device IO Write and Read

Figure 7-27 shows the program flow that the host MCU must execute for configuring the and reading the IO from a device. The host selects the device it wants to communicate with and issues the GPIO WRITE function. The host shall then send the IO configuration register followed by an inverted value, that allows the device to check for any bus transmission error. If the host receives a return code any other than AAh, it must terminate the transaction by sending a bus reset. When the host gets the return code of AAh from the device, it shall wait for the device to sample the bus and then read back the IO read register along with a CRC. If the host plans to read the device continuously, then it must send a bus reset and initiate a GPIO READ function.

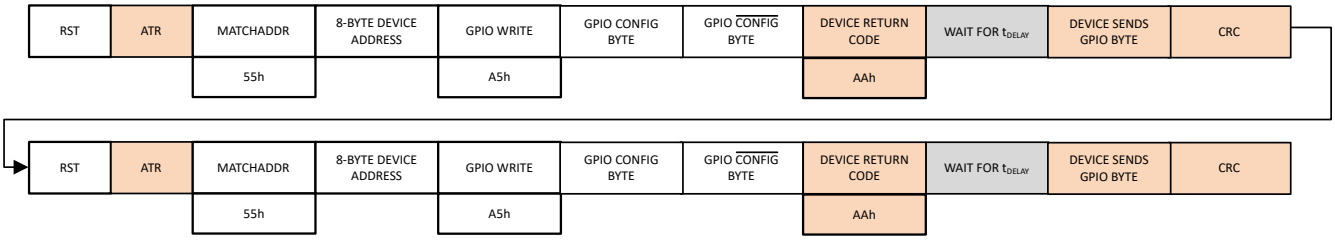


Figure 7-27. Multiple Device GPIO Write and Read Flow

7.6 Register Maps

Table 7-4. Register Map

SCRATCHPAD-1 BYTE	TYPE	RESET	REGISTER NAME	REGISTER DESCRIPTION	SECTION
00h	RO	80h	TEMP_RESULT_L	Temperature result LSB register	Go
01h	RO	0Ch	TEMP_RESULT_H	Temperature result MSB register	Go
02h	RO	3xh	STATUS_REG	Status register	Go
03h	RO	FFh	Reserved	Reserved	
04h	R/W	70h	CONFIG_REG1	Device Configuration-1 register	Go
05h	R/W	80h	CONFIG_REG2	Device Configuration-2 register	Go

ADVANCE INFORMATION

Table 7-4. Register Map (continued)

SCRATCHPAD-1 BYTE	TYPE	RESET	REGISTER NAME	REGISTER DESCRIPTION	SECTION
06h	R/W	00h	STACKMODE_ADDR	Stackmode address register	Go
07h	RO	FFh	Reserved	Reserved	
08h	R/W	00h	TEMP_ALERT_LOW_L	Temperature alert low limit LSB	Go
09h	R/W	00h	TEMP_ALERT_LOW_H	Temperature alert low limit MSB	Go
0Ah	R/W	F0h	TEMP_ALERT_HIGH_L	Temperature alert high limit LSB	Go
0Bh	R/W	07h	TEMP_ALERT_HIGH_H	Temperature alert high limit MSB	Go
0Ch	R/W	00h	TEMP_OFFSET_L	Temperature offset calibration LSB register	Go
0Dh	R/W	00h	TEMP_OFFSET_H	Temperature offset calibration MSB register	Go
0Eh	RO	FFh	Reserved	Reserved	
0Fh	RO	FFh	Reserved	Reserved	
—	RO	F0h	IO_READ	IO read register	Go
—	RW	00h	IO_CONFIG	IO configuration register	Go

Table 7-5. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 Temperature Result LSB Register (Scratchpad-1 offset = 00h) [reset = 80h]

The register is part of the 16-bit temperature result readout that stores the least significant byte of the output of the most recent conversion. Following a power up, the register has the value 80h until the first conversion is complete.

Return to Register Map.

Figure 7-28. Temperature Result LSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[7:0]							
R-80h							

Table 7-6. Temperature Result LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[7:0]	R	80h	Stores the LSB of the most recent temperature conversion results.

7.6.2 Temperature Result MSB Register (Scratchpad-1 offset = 01h) [reset = 0Ch]

The register is part of the 16-bit temperature result readout that stores the most significant byte of the output of the most recent conversion. Following a power up, the register has the value 0Ch until the first conversion is complete.

Return to Register Map.

Figure 7-29. Temperature Result MSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[15:8]							
R-0Ch							

Table 7-7. Temperature Result MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[15:8]	R	0Ch	Stores the MSB of the most recent temperature conversion results.

7.6.3 Status Register (Scratchpad-1 offset = 02h) [reset = 3Ch]

This register provides status of the alert flags, power mode, arbitration completion, and device lock. The lock flag is set after the device configuration EEPROM is locked by the application. The arbitration done flag is set after the device successfully sends its device address and is cleared only when the ARB_MODE bits in the configuration register are cleared. The power mode status flag value is decided based on the powering technique used for the device detected at power up.

The alert flags are set after the most recent conversion results are available and cleared when the status register is read by the host application. If the alert flag is set, it cannot be cleared by the device even if the result of the last conversion is between the alert limits.

Return to Register Map.

Figure 7-30. Status Register

7	6	5	4	3	2	1	0
ALERT_HIGH	ALERT_LOW	Reserved			POWER_MODE	ARB_DONE	LOCK_STATUS
RC-0b	RC-0b	R-111b			R-0b	R-0b	R-0b

Table 7-8. Status Register Field Description

Bit	Field	Type	Reset	Description
7	ALERT_HIGH	RC	0b	Alert high status flag 0b = Last temperature conversion result is less than alert high limit 1b = Last temperature conversion result is more than or equal to alert high limit
6	ALERT_LOW	RC	0b	Alert low status flag 0b = Last temperature conversion result is more than alert low limit 1b = Last temperature conversion result is less than or equal to alert low limit
5:3	Reserved	R	111b	Reserved
2	POWER_MODE	R	xb	Device power mode flag. 0b = V_{DD} powered mode 1b = Bus powered mode
1	ARB_DONE	R	0b	Arbitration complete flag 0b = Arbitration is not complete or not enabled 1b = Arbitration is complete

ADVANCE INFORMATION

Table 7-8. Status Register Field Description (continued)

Bit	Field	Type	Reset	Description
0	LOCK_STATUS	R	0b	Lock status flag. 0b = Device configuration registers can be updated 1b = Device configuration registers cannot be updated

7.6.4 Device Configuration-1 Register (Scratchpad-1 offset = 04h) [reset = 70h]

The register is used to configure the device functions like the number of valid bits in temperature readout, alert mode, averaging, and conversion type (one-shot, auto and stacked conversion in bus powered mode and one-shot or continuous conversion in V_{DD} powered mode). The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-31. Device Configuration-1 Register

7	6	5	4	3	2	1	0
TEMP_FMT	Reserved	CONV_TIME_SEL	ALERT_MODE	AVG_SEL	CONV_MODE_SEL[2:0]		
RW-0b	RW-1b	RW-1b	RW-1b	RW-0b	RW-000b		

Table 7-9. Device Configuration-1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TEMP_FMT	RW	0b	Selects the temperature format. 0b = 12-bit legacy format 1b = 16-bit high precision format
6	Reserved	RW	1b	Reserved
5	CONV_TIME_SEL	RW	1b	Selects the ADC conversion time 0b = 3 ms / 1b = 5.5 ms
4	ALERT_MODE	RW	1b	Alert pin function only available in V_{DD} powered mode 0b = Alert pin works in Alert Mode 1b = Alert pin works in Comparator Mode
3	AVG_SEL	RW	0b	Conversion averaging selection 0b = No averaging 1b = Averaging of 8 conversions
2:0	CONV_MODE_SEL[2:0]	RW	000b	Conversion mode selection bits. When device is in bus powered mode: 000b = Default one shot conversion mode using CONVERT TEMP function 001b = Stacked conversion mode is enabled. When enabled, the stackmode address is used to stagger the actual conversion start with respect to the conversion request. 010b = Auto temperature conversion mode is enabled 011b - 111b = Reserved. Device behavior is unspecified. When device is in V_{DD} powered mode: 000b = Default one shot conversion mode using CONVERT TEMP function 001b = One conversion every 8 seconds 010b = One conversion every 4 seconds 011b = One conversion every 2 seconds 100b = One conversion every 1 second 101b = One conversion every 0.5 second 110b = One conversion every 0.25 second 111b = One conversion every 0.125 second

7.6.5 Device Configuration-2 Register (Scratchpad-1 offset = 05h) [reset = 80h]

This register is used to configure the overdrive enable, arbitration mode during address discovery, and the hysteresis for alert status or pin (available only in V_{DD} powered mode for alert pin). The register can be used to

lock the writable registers for the device. The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Note

- When setting the overdrive enable or lock enable bits, the application must send all the scratchpad-1 data bytes and read the CRC from the device before the change of overdrive bit takes effect.

Return to Register Map.

Table 7-10. Device Configuration-2 Register

7	6	5	4	3	2	1	0
OD_EN	Reserved		ARB_MODE[1:0]		HYSTERSIS[1:0]		LOCK_EN
RW-1b	RW-00b		RW-00b		RW-00b		RW-0b

Table 7-11. Device Configuration-2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OD_EN	RW	1b	Overdrive mode enable 0b = Over drive speed is disabled 1b = Overdrive speed is enabled The bit when set cannot be cleared by host write and will automatically be cleared only by a standard speed bus reset.
6:5	Reserved	RW	00b	Reserved
4:3	ARB_MODE[1:0]	RW	00b	Arbitration mode 00b = Arbitration by device is disabled 01b = Reserved 10b = Arbitration by device is enabled in software compatible mode 11b = Fast Arbitration mode is enabled The arbitration feature is applicable only when address command is SEARCHADDR. Other commands and functions are not affected by the ARB_MODE bit.
2:1	HYSTERSIS[1:0]	RW	00b	Alert hysteresis selection 00b = 5 °C hysteresis 01b = 10 °C hysteresis 10b = 15 °C hysteresis 11b = 20 °C hysteresis
0	LOCK_EN	RW	0b	Register lock protection enable/disable bit 0b = The register protection is disabled 1b = The register protection is enabled. When set the bit cannot be cleared by writing to the register to unlock the register protection. The feature when enabled, prevents application write to the temperature offset, temperature alert low, temperature alert high, stackmode address and device configuration registers.

7.6.6 Stackmode Address Register (Scratchpad-1 offset = 06h) [reset = 00h]

The register is used to program the stackmode address for the device. The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Table 7-12. Stackmode Address Register

7	6	5	4	3	2	1	0
STACKMODE_ADDRESS[7:0]							

ADVANCE INFORMATION

Table 7-12. Stackmode Address Register (continued)

7	6	5	4	3	2	1	0
RW-00h							

Table 7-13. Stackmode Address Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STACKMODE_ADDRESS[7:0]	RW	00h	Stores the stackmode address for the device when stacked conversion mode is used to stagger the temperature conversions.

7.6.7 Temperature Alert Low LSB Register (Scratchpad-1 offset = 08h) [reset = 00h]

This register provides the LSB for the low temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is less than the threshold set, then the device shall update the alert low status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-32. Temperature Alert Low Register

7	6	5	4	3	2	1	0
ALERT_LOW[7:0]							
RW-00h							

Table 7-14. Temperature Alert Low Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ALERT_LOW[7:0]	RW	00h	Stores the LSB of the alert low limit for comparison with the last temperature conversion result

7.6.8 Temperature Alert Low MSB Register (Scratchpad-1 offset = 09h) [reset = 00h]

This register provides the MSB for the low temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is less than the threshold set, then the device shall update the alert low status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Table 7-15.

7	6	5	4	3	2	1	0
ALERT_LOW[15:8]							
RW-00h							

Table 7-16.

Bit	Field	Type	Reset	Description
7:0	ALERT_LOW[15:8]	RW	00h	Stores the MSB of the alert low limit for comparison with the last temperature conversion result

7.6.9 Temperature Alert High LSB Register (Scratchpad-1 offset = 0Ah) [reset = F0h]

This register provides the LSB for the high temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is more than the threshold set, then the device shall update the alert high status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-33. Temperature Alert High Register

7	6	5	4	3	2	1	0
ALERT_HIGH[7:0]							
RW-F0h							

Table 7-17. Temperature Alert High Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ALERT_HIGH[7:0]	RW	F0h	Stores the LSB of the alert high limit for comparison with the last temperature conversion result

7.6.10 Temperature Alert High MSB Register (Scratchpad-1 offset = 0Bh) [reset = 07h]

This register provides the MSB for the high temperature alert threshold to compare with the latest temperature conversion result. The register on the first power up has the alert threshold set in legacy format. If there is a change of format, then the application must update the register in the new format. If the latest temperature conversion result is more than the threshold set, then the device shall update the alert high status flag in the status register, respond with the status bit flagged for an alert during the ALERTSEARCH command, and set the alert pin low if the device is in V_{DD} powered mode.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-34. Temperature Alert High MSB Register

7	6	5	4	3	2	1	0
ALERT_HIGH[15:8]							
RW-07h							

Table 7-18. Temperature Alert High MSB Register Field Description

Bit	Field	Type	Reset	Description
7:0	ALERT_HIGH[15:8]	RW	07h	Stores the MSB of the alert high limit for comparison with the last temperature conversion result

7.6.11 Temperature Offset LSB Register (Scratchpad-1 offset = 0Ch) [reset = 00h]

The register is used to store the LSB of the offset calibration for the temperature sensor. The register on the first power up has the temperature offset set in legacy format. If there is a change of format, then the application must update the register in the new format. After every temperature conversion, the offset calibration is automatically applied to the temperature result, before being stored in the TEMP_RESULT_L and TEMP_RESULT_H registers.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-35. Temperature Offset LSB Register

7	6	5	4	3	2	1	0
TEMP_OFFSET_L[7:0]							
RW-00h							

Table 7-19. Temperature Offset LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_OFFSET_L[7:0]	RW	00h	Stores the offset correction LSB for the temperature result

7.6.12 Temperature Offset MSB Register (Scratchpad-1 offset = 0Dh) [reset = 00h]

The register is used to store the MSB of the offset calibration for the temperature sensor. The register on the first power up has the temperature offset set in legacy format. If there is a change of format, then the application must update the register in the new format. After every temperature conversion, the offset calibration is automatically applied to the temperature result, before being stored in the TEMP_RESULT_L and TEMP_RESULT_H registers.

The host can store the updated setting to the configuration EEPROM using the COPY SCRATCHPAD-1 function command. At power-on reset, the register setting is automatically restored from the configuration EEPROM.

Return to Register Map.

Figure 7-36. Temperature Offset MSB Register

7	6	5	4	3	2	1	0
TEMP_OFFSET_H[15:8]							
RW-00h							

Table 7-20. Temperature Offset MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_OFFSET_H[15:8]	RW	00h	Stores the offset correction MSB for the temperature result

7.6.13 IO Read Register [reset = F0h]

The register is used to read the state of the IO0 to IO3 pin. The register values are updated when the GPIO READ function is issued by the host or when the GPIO configuration is written using the GPIO WRITE function. When IO2 is configured to function as an alert pin, it provides a status of the alert pin.

Return to Register Map.

Figure 7-37. IO Read Register

7	6	5	4	3	2	1	0
nIO3_STATE	nIO2_STATE	nIO1_STATE	nIO0_STATE	IO3_STATE	IO2_STATE	IO1_STATE	IO0_STATE
R-1b	R-1b	R-1b	R-1b	R-0b	R-0b	R-0b	R-0b

Table 7-21. IO Read Register Field Descriptions

Bit	Field	Type	Reset	Description
7	nIO3_STATE	R	1b	Read inverted value of the IO3 pin when configured as a digital input or output
6	nIO2_STATE	R	1b	Read inverted value of the IO2 pin when configured as a digital input or output
5	nIO1_STATE	R	1b	Read inverted value of the IO1 pin when configured as a digital input or output
4	nIO0_STATE	R	1b	Read inverted value of the IO0 pin when configured as a digital input or output
3	IO3_STATE	R	0b	Read value of the IO3 pin when configured as a digital input or output

Table 7-21. IO Read Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IO2_STATE	R	0b	Read value of the IO2 pin when configured as a digital input or output
1	IO1_STATE	R	0b	Read value of the IO1 pin when configured as a digital input or output
0	IO0_STATE	R	0b	Read value of the IO0 pin when configured as a digital input or output

7.6.14 IO Configuration Register [reset = 00h]

The register is used to select the IO function for the pins marked IO0-IO3 on the device. When selected to function as a digital open-drain output, the pin shall be able to drive a 0 or 1 externally for controlling the gate or base of a transistor on IO0 to IO3 pin.

Return to Register Map.

Figure 7-38. IO Configuration Register

7	6	5	4	3	2	1	0
IO3_SEL[1:0]		IO2_SEL[1:0]		IO1_SEL[1:0]		IO0_SEL[1:0]	
RW-00b		RW-00b		RW-00b		RW-00b	

Table 7-22. IO Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	IO3_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO3 is configured as input buffer and can be read 01b = Reserved 10b = IO3 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO3 is configured as an output in open drain mode and the IO is driven as '1'
5:4	IO2_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO2 is configured as input buffer and can be read 01b = IO2 is configured as an open drain active low alert 10b = IO2 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO2 is configured as an output in open drain mode and the IO is driven as '1'
3:2	IO1_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO1 is configured as input buffer and can be read 01b = Reserved 10b = IO1 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO1 is configured as an output in open drain mode and the IO is driven as '1'
1:0	IO0_SEL[1:0]	RW	00b	Selects the function of the IO 00b = IO0 is configured as input buffer and can be read 01b = Reserved 10b = IO0 is configured as an output in open drain mode and the IO is driven as '0' 11b = IO0 is configured as an output in open drain mode and the IO is driven as '1'

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMP1826 can operate as a single-wire half duplex bus, either in supply or bus powered mode. The TMP1826 features a thermal sensor with an integrated 2-Kbit user EEPROM for applications requiring identification with lesser number of components due to space constraints. The device also features an integrated CRC that may be used for ensuring data integrity during communication.

The bus powered mode is designed for applications working without a dedicated power supply pin and can reduce cabling costs. As the device current consumption during thermal conversion and EEPROM operations is low, the device may not require a low impedance current path, thereby reducing the need for additional FET or load switch and current limiting resistor to bypass the bus pullup resistor. The pullup resistor used during bus powered mode must be correctly sized to ensure that sufficient current can be supplied during a thermal conversion and EEPROM operation, and input pin voltage does not fall below the $V_{IH(MIN)}$.

Additionally, if the host needs to reset the device when operating in bus powered mode, the host must pull the communication line low for at least 100 ms. This allows the internal capacitor of the device to discharge and prepare the device for power on reset.

8.2 Typical Applications

8.2.1 Bus Powered Application

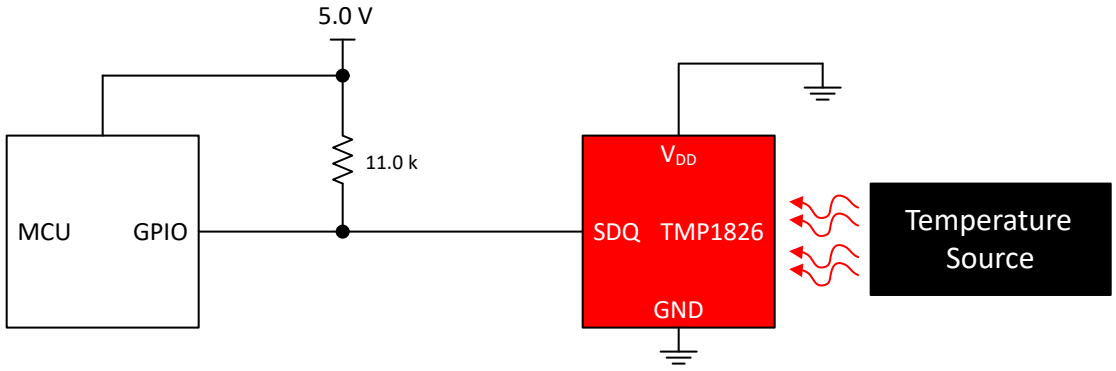


Figure 8-1. Bus Powered Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed below:

Table 8-1. Design Parameters

Parameter	Value
Power mode	Bus Powered
Supply (V_{DD})	5.0 V
Pullup resistor (R_{PUR})	11.0 kΩ

8.2.1.2 Detailed Design Procedure

To reduce the wire count, the bus powered mode for TMP1826 is the primary mode of operation. The V_{DD} pin of the device must be connected to GND and the SDQ pin of the device must be connected to the host GPIO with a pullup resistor.

To calculate the maximum value of the pullup resistor, substitute the value for V_{PUR} and $I_{PU(MIN)}$ in Equation 1.

$R_{PUR} < (5.0\ V - 1.6\ V) \div 300\ \mu A$

$R_{PUR} < 11.333\ k\Omega$

The actual value of the pull-up resistor can then be adjusted based on the speed of communication and bus or cable parasitic capacitance.

When the V_{DD} is activated, the TMP1826 draws current through the pullup resistor to charge its internal capacitors. When the internal capacitor is charged to the pullup voltage, the host can start communication. The bus idle state is high, which is maintained by the pullup resistor, when the host puts its GPIO in high impedance state.

The TMP1826 uses the stored charge to operate when the SDQ pin is low and measures the low period to decode bus reset, logic high and logic low sent by the host. Similarly, when the host reads data from the TMP1826, it changes the state of the bus from high to low and releases the bus. Depending on whether the device has to send a logic low or logic high, the device shall either hold the bus low or release the bus immediately.

8.2.2 Supply Powered Application

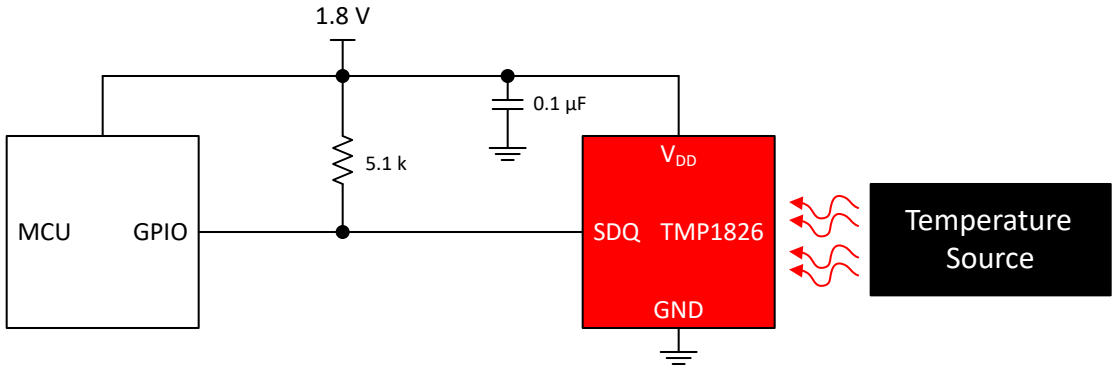


Figure 8-2. Supply Powered Application

8.2.2.1 Design Requirements

For this design example, use the parameters listed below:

Table 8-2. Design Parameters

Parameters	
Power mode	V_{DD} Powered
Supply (V_{DD})	1.8 V
Pullup resistor (R_{PUR})	5.1 kΩ

8.2.2.2 Detailed Design Procedure

The supply powered mode uses the V_{DD} pin connected to the same supply rail as the host and pullup resistor. TI recommends to put a 0.1-µF bypass capacitor close to the V_{DD} pin of the TMP1826.

The pullup resistor value of 5.1 kΩ, is large enough to provide proper communication with standard speed and avoid V_{OL} violation when the device is sending data to the host. The user may change the value based on the total bus load and application operating requirements.

ADVANCE INFORMATION

The communication protocol for supply powered mode is same as that for bus powered mode, which allows the entire software stack to be reused. This mode of operation is useful for onboard thermal sensing applications as it provides for continuous conversion and alert function.

8.2.3 UART Interface for Communication

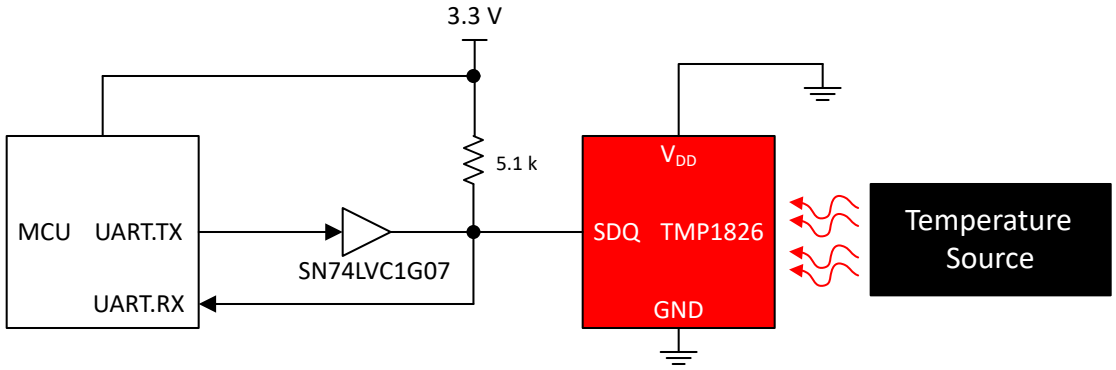


Figure 8-3. Using UART to interface TMP1826

8.2.3.1 Design Requirements

For this design example, use the parameters listed below:

Table 8-3. Design Parameters

Parameter	Value
Power Mode	Bus powered
Supply (V_{DD})	3.3 V
Pullup resistor (R_{PUR})	5.1 kΩ

8.2.3.2 Detailed Design Procedure

If using GPIO for communication is not possible due to any reason, it is also possible to use UART peripheral that is available on most host controllers to interface with the TMP1826. UART is a push-pull full duplex bus and to interface with TMP1826, it requires a buffer with open-drain driver like the SN74LVC1G07.

The input of the buffer is connected to the UART transmit pin and the output of the buffer is connected to the SDQ pin on the TMP1826. The output of the buffer is also connected to the UART receive pin on the host. As the output is open-drain, it requires a pullup resistor which can be calculated using Equation 1. Substituting the value for V_{PUR} = 3.3 V and $I_{PU(MIN)}$ = 300 µA, the R_{PUR} value selected must be less than 5.67 kΩ.

In software, the application must adjust its baud rate so that it can send bus reset to the device by sending 00h. The start bit of the UART frame which is always 0, provides the required falling edge for data sent to the TMP1826. When sending a logic high to the device, the UART shall send FFh to the TMP1826 and, when sending a logic low to the device, the UART shall send C0h. As UART is a full duplex bus, the host must flush its receive buffers during a transmit operation.

When receiving data from the TMP1826, the host shall send FFh and the device when transmitting a logic high will detect and release the bus, while when transmitting a logic low will detect and hold the bus. As a result, the host shall receive a FFh for a logic high and F0h for a logic low depending on the baud rate configured.

ADVANCE INFORMATION

9 Power Supply Recommendations

The TMP1826 operates with a power supply in the range of 1.7 V to 5.5 V in both V_{DD} powered and bus powered modes. When operating in V_{DD} powered mode, a power-supply bypass capacitor is required for precision and stability. Place this power-supply bypass capacitor as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

In bus powered mode, the V_{DD} pin must be connected to ground. The internal capacitor in the device is sufficient to provide power during bus communication. The internal capacitor is recharged through the external pullup resistor during the recovery period. In cases, where there is a long bus length or at higher temperatures, it may be necessary for the host to provide additional time for bus recovery or to use the overdrive speed in which the part uses the internal capacitor charge less.

When using IO pins to control external circuits, take care that currents to these pins do not heat the part and offset temperature measurements.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins when in supply powered mode. The recommended value of the capacitor is 0.1 µF. The open-drain SDQ pin requires an external pullup resistor which must not be higher than R_{PUR}.

When in bus powered mode, only the external pullup resistor is required for the open-drain SDQ pin.

To achieve a high precision temperature reading for a rigid PCB, do not solder the thermal pad. For a flexible PCB, the user may solder the thermal pad to the increase board level reliability. If the thermal pad is soldered, then it should be connected to the ground.

10.2 Layout Example

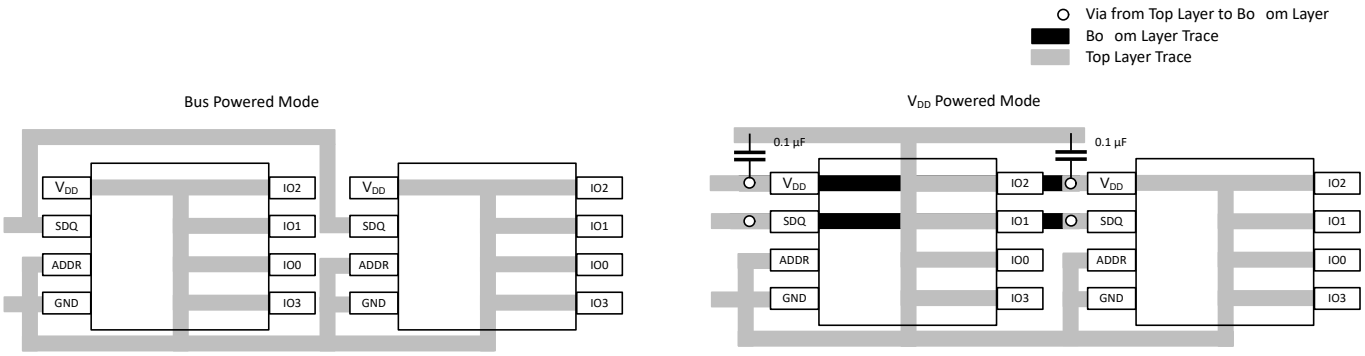


Figure 10-1. Layout Example

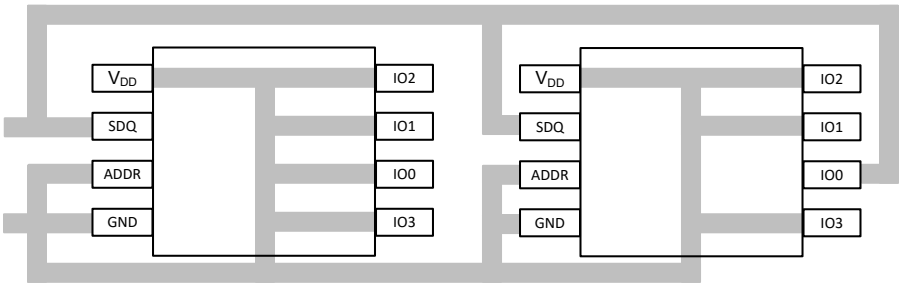


Figure 10-2. IO Hardware Address in Bus Powered Mode

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP1826DGKT	ACTIVE	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

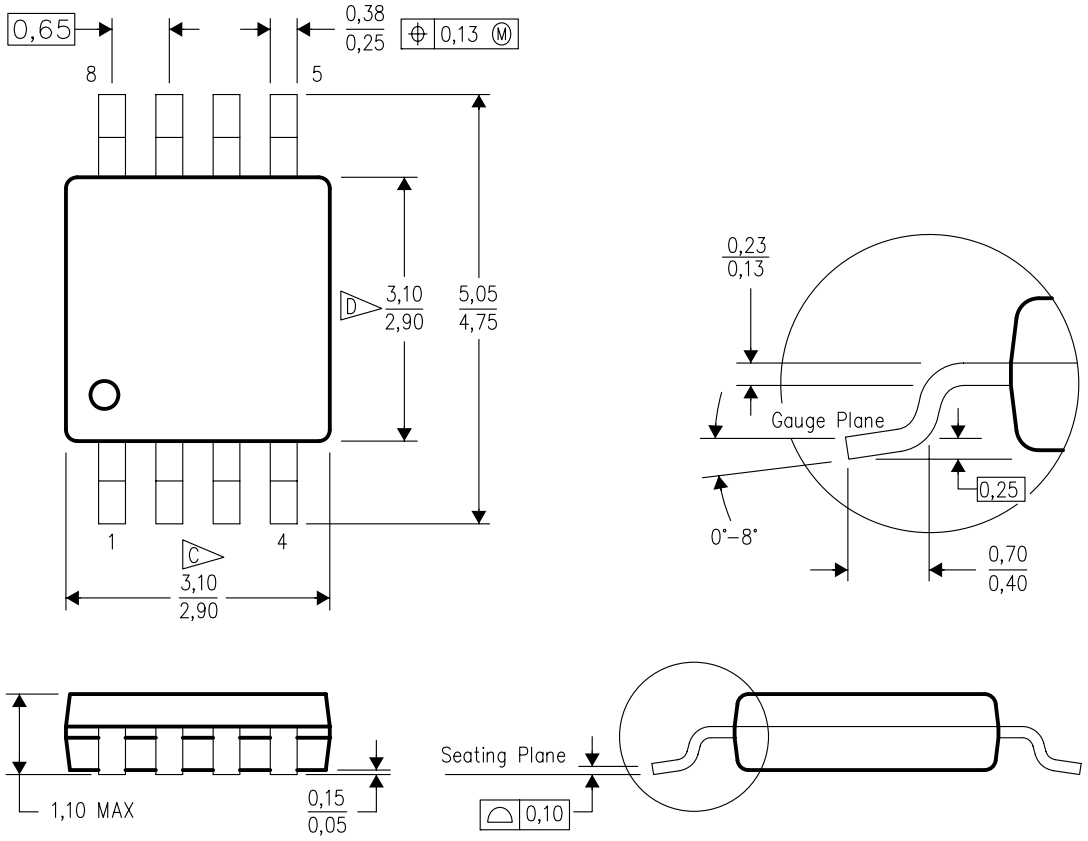
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TMUX7236 44 V, Low-RON, 2:1 (SPDT), 2-Channel Precision Switch With Latch-Up Immunity and 1.8 V Logic

1 Features

- Latch-up immune
- Dual supply range: ±4.5 V to ±22 V
- Single supply range: 4.5 V to 44 V
- Low on-resistance: 2 Ω
- High current support: 330 mA (maximum) (WQFN)
- –40°C to +125°C operating temperature
- 1.8 V logic compatible
- Integrated pull-down resistor on logic pins
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional operation

2 Applications

- Gas meters
- Flow transmitters
- Factory automation and industrial controls
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test
- Data acquisition systems
- Ultrasound scanners
- Optical networking
- Optical test equipment
- Remote radio units
- Wired networking
- Patient monitoring and diagnostics

3 Description

The TMUX7236 is a complementary metal-oxide semiconductor (CMOS) switch with latch-up immunity in a dual channel, 2:1 configuration. The device works well with dual supplies (±5 V to ±22 V), a single supply (5 V to 44 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The TMUX7236 supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

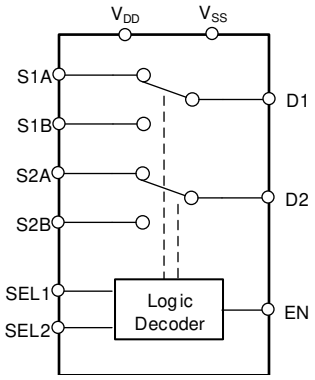
All logic control inputs support logic levels from 1.8 V to V_{DD}, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX72xx family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments.

Device Information(1)

DEVICE NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX7236	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Block Diagram

Table of Contents

4 Revision History

Changes from Revision * (March 2022) to Revision A (July 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

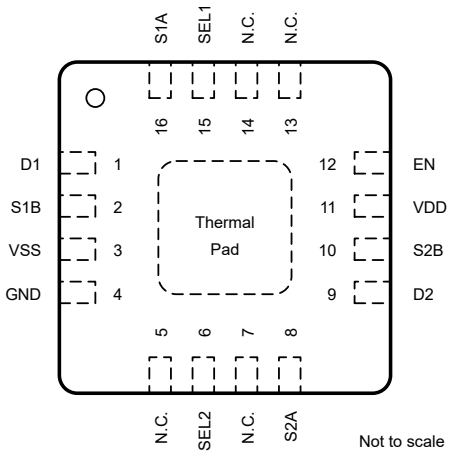


Figure 5-1. RUM Package, 16-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D1	1	I/O	Drain pin. Can be an input or output.
D2	9	I/O	Drain pin. Can be an input or output.
GND	4	P	Ground (0 V) reference
NC	5, 7, 13, 14	—	No internal connection. Can be shorted to GND or left floating.
S1A	16	I/O	Source pin 1A. Can be an input or output.
S1B	2	I/O	Source pin 1B. Can be an input or output.
S2A	8	I/O	Source pin 2A. Can be an input or output.
S2B	10	I/O	Source pin 2B. Can be an input or output.
EN	12	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
SEL1	15	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in Section 8.4.
SEL2	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in Section 8.4.
V_{DD}	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
V_{SS}	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad		—	The thermal pad is not connected internally. There is no requirement to electrically connect this pad. If connected, however, it is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN)(5)		1650	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.2mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX7236 RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) [2]		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
RUM (WQFN)	+44 V Single Supply[1]	330	220	120	mA
	±15 V Dual Supply	330	220	120	mA
	+12 V Single Supply	260	180	110	mA
	±5 V Dual Supply	240	160	100	mA
	+5 V Single Supply	180	120	80	mA

(1) Specified for nominal supply voltage only.
(2) Refer to the total power dissipation (P_{tot}) limits in the *Absolute Maximum Ratings* table, which must be followed with the maximum continuous current specification.

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		2	2.7	Ω
			–40°C to +85°C			3.4	Ω
			–40°C to +125°C			4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.2	0.46	Ω
			–40°C to +85°C			0.65	Ω
			–40°C to +125°C			0.7	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–20		20	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.6	0.1	0.6	nA
			–40°C to +85°C	–7		7	nA
			–40°C to +125°C	–45		45	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to On-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–20		20	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1.5	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		35	56	µA
			–40°C to +85°C			65	µA
			–40°C to +125°C			80	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		5	20	µA
			–40°C to +85°C			24	µA
			–40°C to +125°C			35	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		110	125	ns
			–40°C to +85°C			140	ns
			–40°C to +125°C			155	ns
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		95	120	ns
			–40°C to +85°C			135	ns
			–40°C to +125°C			145	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		125	160	ns
			–40°C to +85°C			175	ns
			–40°C to +125°C			190	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-before-make Time	25°C		27		ns
			–40°C to +85°C	5			ns
			–40°C to +125°C	5			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		720		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Charge Injection	25°C		30		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–107		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Crosstalk	25°C		–93		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		40		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		45		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		55		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		165		pF

6.8 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		1.7	2.5	Ω
			–40°C to +85°C			3.2	Ω
			–40°C to +125°C			3.8	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10 mA Refer to On-Resistance	25°C		0.3	0.6	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.95	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–40°C to +125°C	–33		33	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–2.2	0.22	2.2	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–70		70	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V Refer to On-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–40°C to +125°C	–33		33	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1.2	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		33	65	µA
			–40°C to +85°C			74	µA
			–40°C to +125°C			90	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		7	26	µA
			–40°C to +85°C			30	µA
			–40°C to +125°C			45	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.9 ±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		100	160	ns
			–40°C to +85°C			170	ns
			–40°C to +125°C			180	ns
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		95	140	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			180	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		125	150	ns
			–40°C to +85°C			165	ns
			–40°C to +125°C			190	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-before-make Time	25°C		28		ns
			–40°C to +85°C	5			ns
			–40°C to +125°C	5			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		740		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Charge Injection	25°C		45		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–107		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Crosstalk	25°C		–93		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		35		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.14		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		45		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		55		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		165		pF

6.10 44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		2	2.4	Ω
			–40°C to +85°C			3.2	Ω
			–40°C to +125°C			3.8	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 40 V I_D = –10 mA Refer to On-Resistance	25°C		0.65	0.8	Ω
			–40°C to +85°C			1.1	Ω
			–40°C to +125°C			1.2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.007		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–7		7	nA
			–40°C to +125°C	–50		50	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to Off-Leakage Current	25°C	–2.2	0.12	2.2	nA
			–40°C to +85°C	–15		15	nA
			–40°C to +125°C	–115		115	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V Refer to On-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–7		7	nA
			–40°C to +125°C	–50		50	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		1	2.75	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1.2	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		44	79	µA
			–40°C to +85°C			88	µA
			–40°C to +125°C			105	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.11 44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		85	145	ns
			–40°C to +85°C			155	ns
			–40°C to +125°C			185	ns
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		90	130	ns
			–40°C to +85°C			140	ns
			–40°C to +125°C			160	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		125	160	ns
			–40°C to +85°C			170	ns
			–40°C to +125°C			180	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-before-make Time	25°C		27		ns
			–40°C to +85°C	10			ns
			–40°C to +125°C	10			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.14		ms
			–40°C to +85°C		0.15		ms
			–40°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		900		ps
Q_{INJ}	Charge injection	V_S = 22 V, C_L = 100 pF Refer to Charge Injection	25°C		104		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Crosstalk	25°C		–93		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		35		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–66		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22 V, V_{BIAS} = 22 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1 MHz	25°C		45		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1 MHz	25°C		55		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1 MHz	25°C		165		pF

6.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		2.8	5.4	Ω
			–40°C to +85°C			6.8	Ω
			–40°C to +125°C			7.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.13	0.21	Ω
			–40°C to +85°C			0.23	Ω
			–40°C to +125°C			0.25	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.8	1.7	Ω
			–40°C to +85°C			1.9	Ω
			–40°C to +125°C			2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	–0.25	0.01	0.25	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–16		16	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	–0.6	0.12	0.6	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–34		34	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to On-Leakage Current	25°C	–0.25	0.01	0.25	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–16		16	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2.25	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1.25	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	44	µA
			–40°C to +85°C			52	µA
			–40°C to +125°C			62	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		90	160	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			225	ns
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		190	235	ns
			–40°C to +85°C			260	ns
			–40°C to +125°C			280	ns
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		160	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			245	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-before-make Time	25°C		30		ns
			–40°C to +85°C	9			ns
			–40°C to +125°C	9			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		770		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF Refer to Charge Injection	25°C		12		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Crosstalk	25°C		–93		dB
BW	–3 dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		50		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.25		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		52		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		68		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		170		pF

6.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

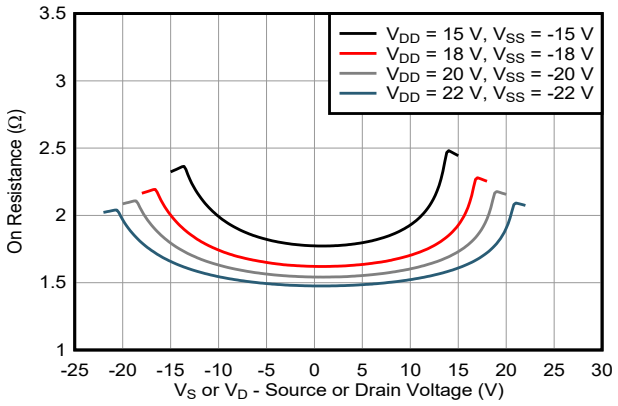


Figure 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

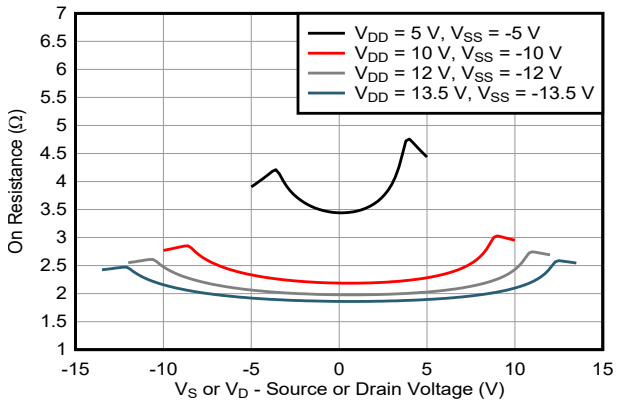


Figure 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

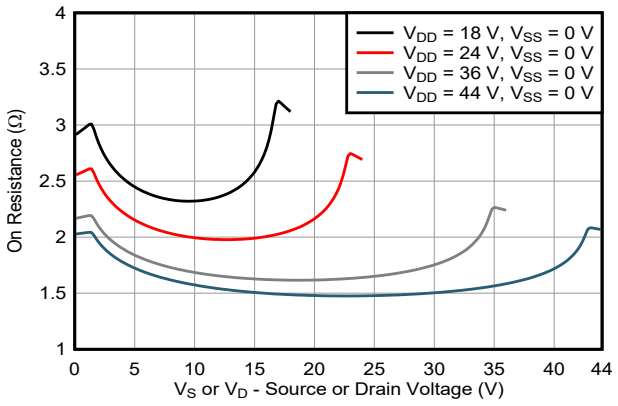


Figure 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

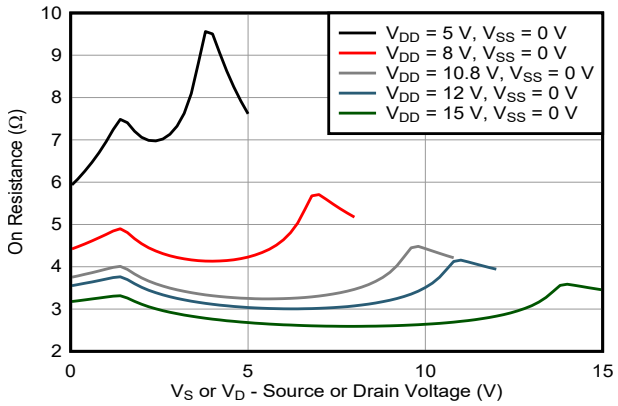


Figure 6-4. On-Resistance vs Source or Drain Voltage – Single Supply

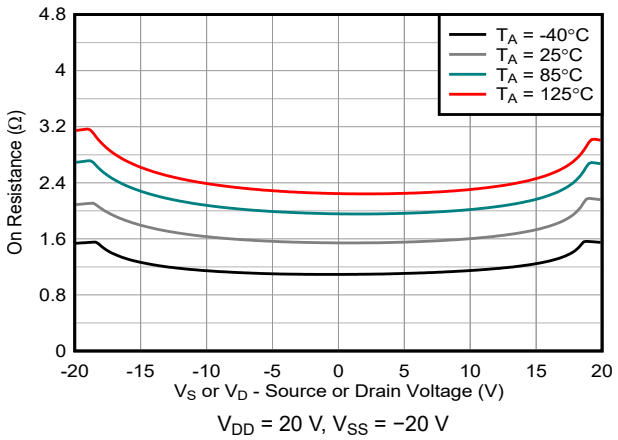


Figure 6-5. On-Resistance vs Temperature

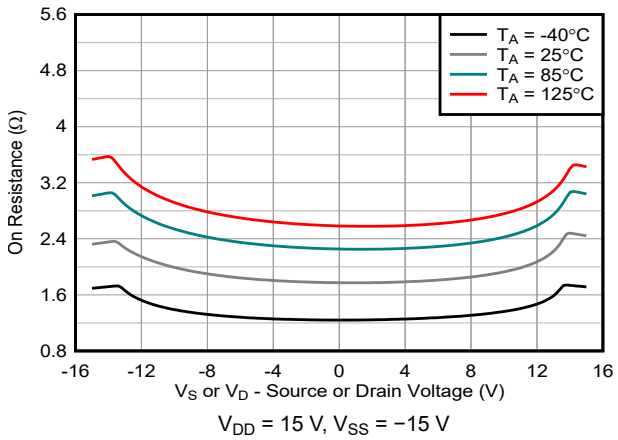
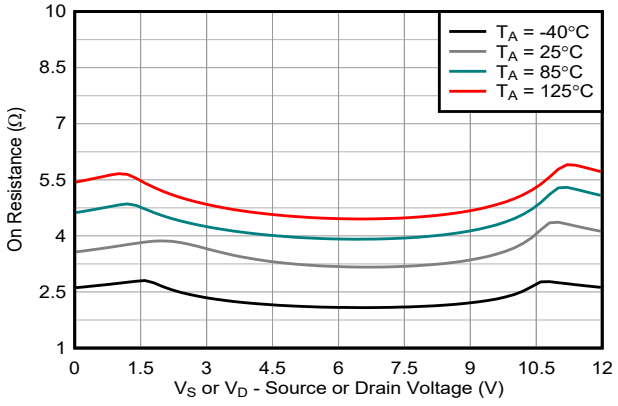


Figure 6-6. On-Resistance vs Temperature

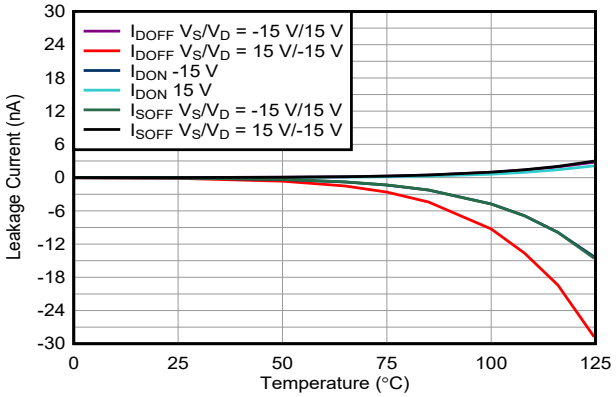
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



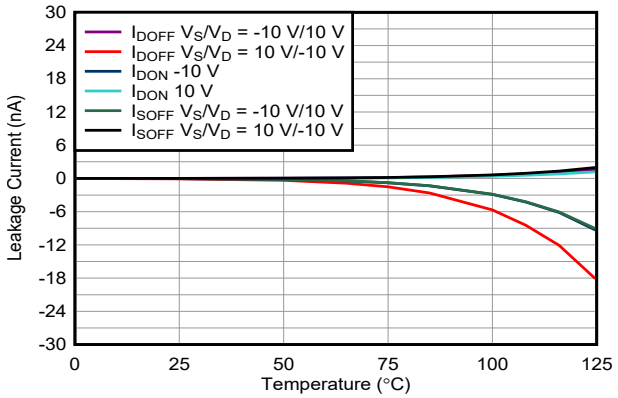
V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-7. On-Resistance vs Temperature



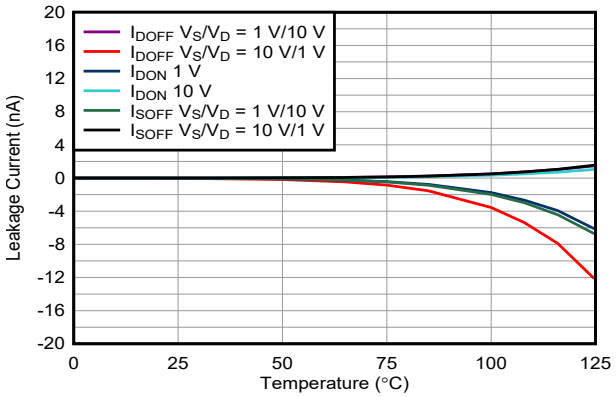
V_{DD} = 20 V, V_{SS} = −20 V

Figure 6-8. On-Leakage vs Temperature



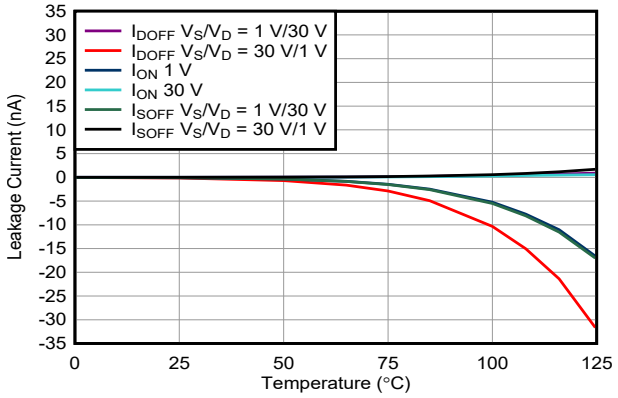
V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-9. On-Leakage vs Temperature



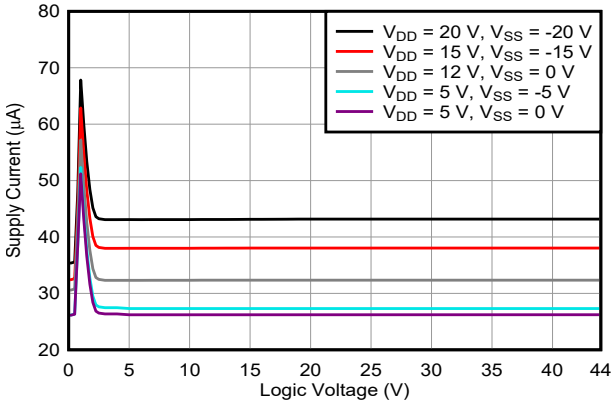
V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-10. On-Leakage vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 6-11. On-Leakage vs Temperature



All channels on

Figure 6-12. Supply Current vs Logic Voltage

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

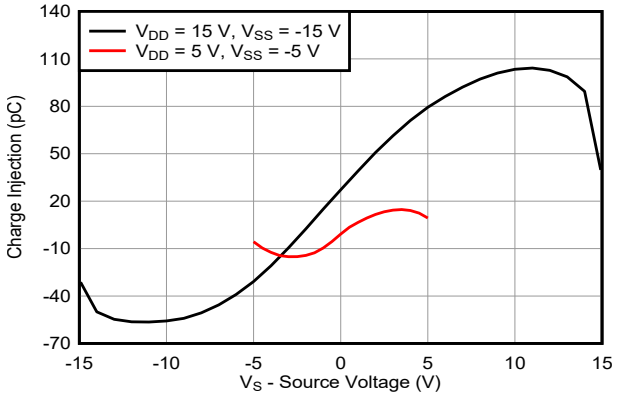


Figure 6-13. Charge Injection vs Source Voltage – Dual Supply

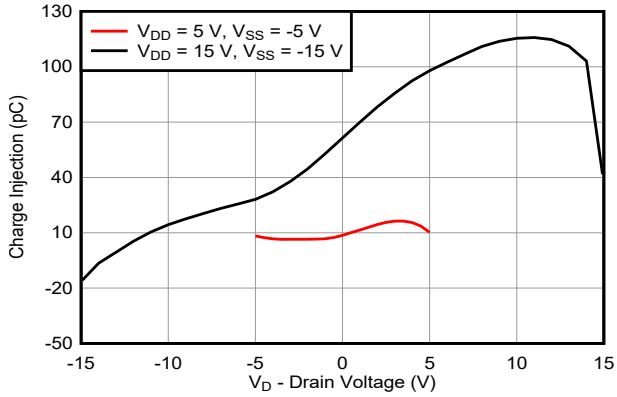


Figure 6-14. Charge Injection vs Drain Voltage – Dual Supply

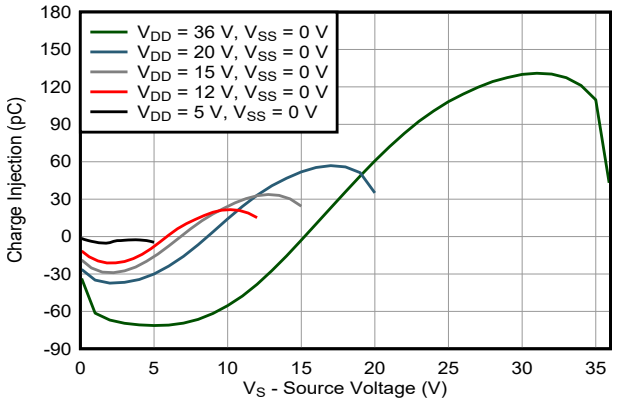


Figure 6-15. Charge Injection vs Source Voltage – Single Supply

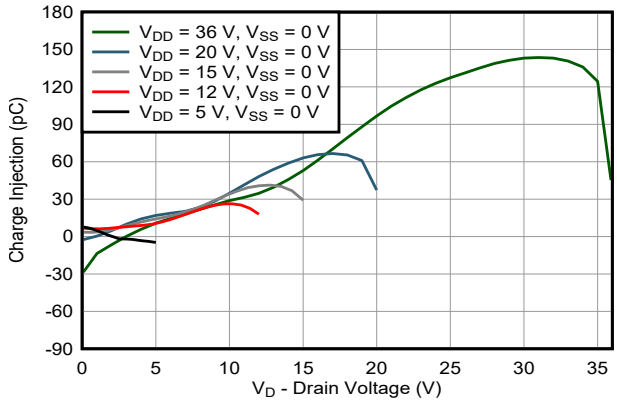


Figure 6-16. Charge Injection vs Drain Voltage – Single Supply

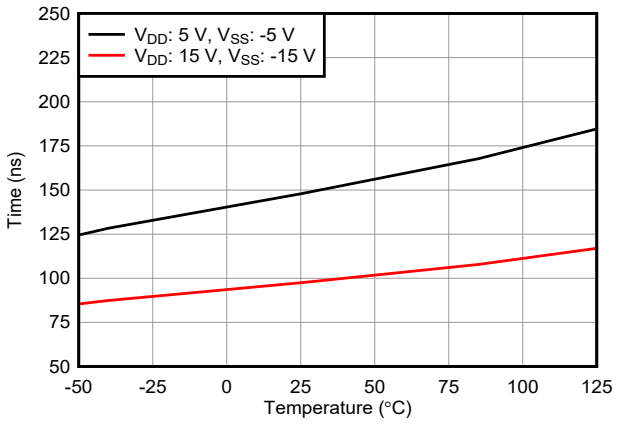


Figure 6-17. $T_{TRANSITION}$ vs Temperature

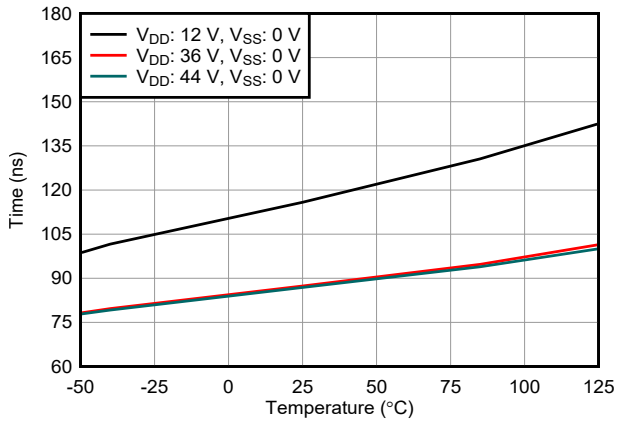
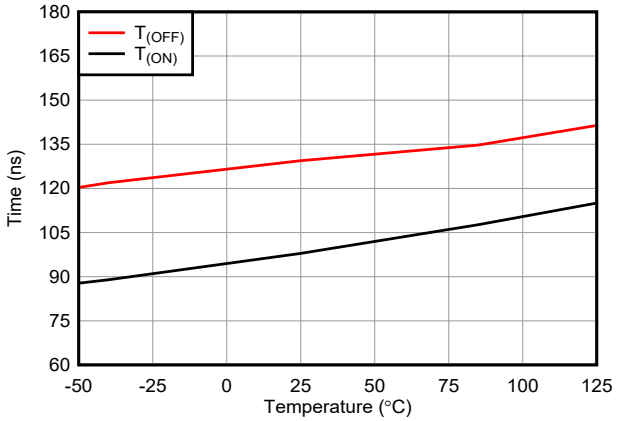


Figure 6-18. $T_{TRANSITION}$ vs Temperature

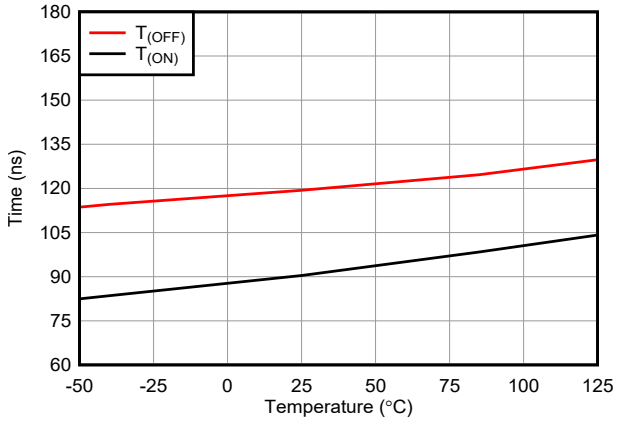
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



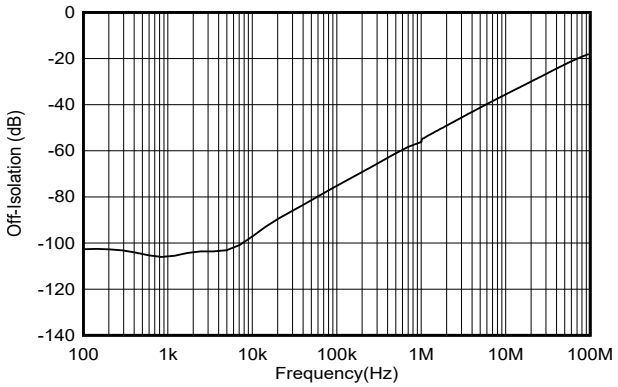
V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-19. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature



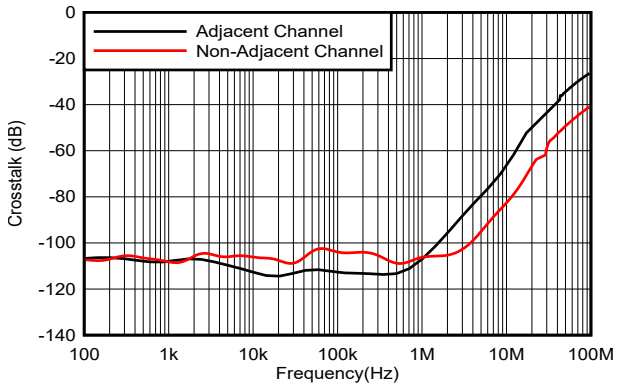
V_{DD} = 44 V, V_{SS} = 0 V

Figure 6-20. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature



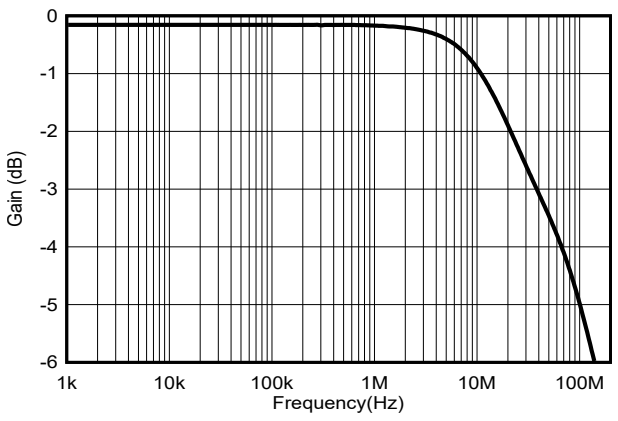
V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-21. Off-Isolation vs Frequency



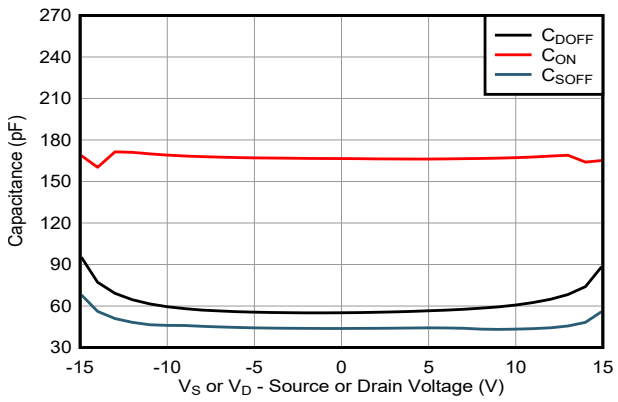
V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-22. Crosstalk vs Frequency



V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-23. On Response vs Frequency

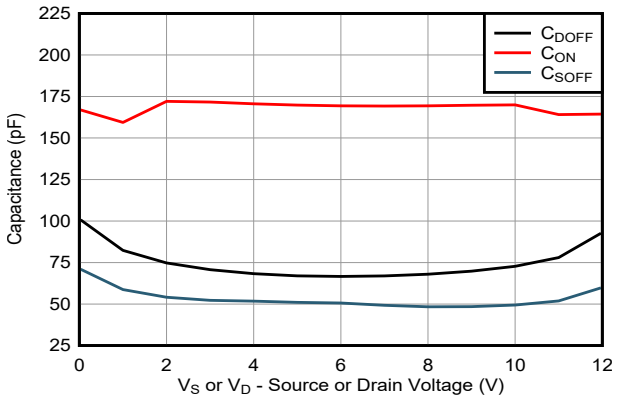


V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-24. Capacitance vs Source or Drain Voltage

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-25. Capacitance vs Source or Drain Voltage

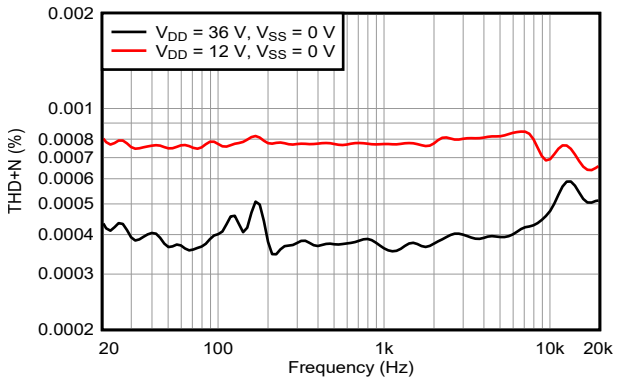


Figure 6-26. THD+N vs Frequency – Single Supply

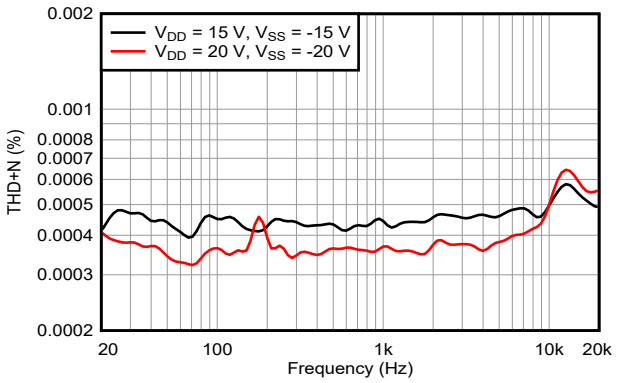
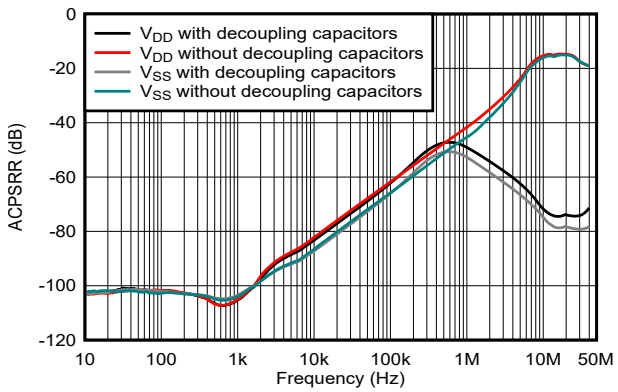


Figure 6-27. THD+N vs Frequency – Dual Supply



V_{DD} = 15 V, V_{SS} = −15 V

Figure 6-28. ACPSRR vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

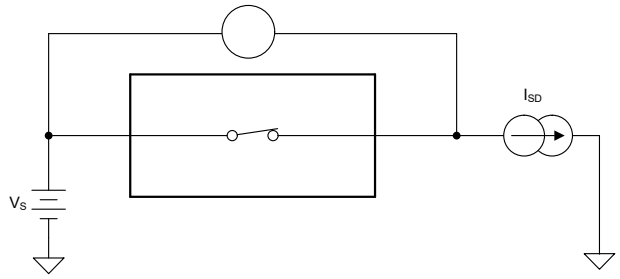


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.

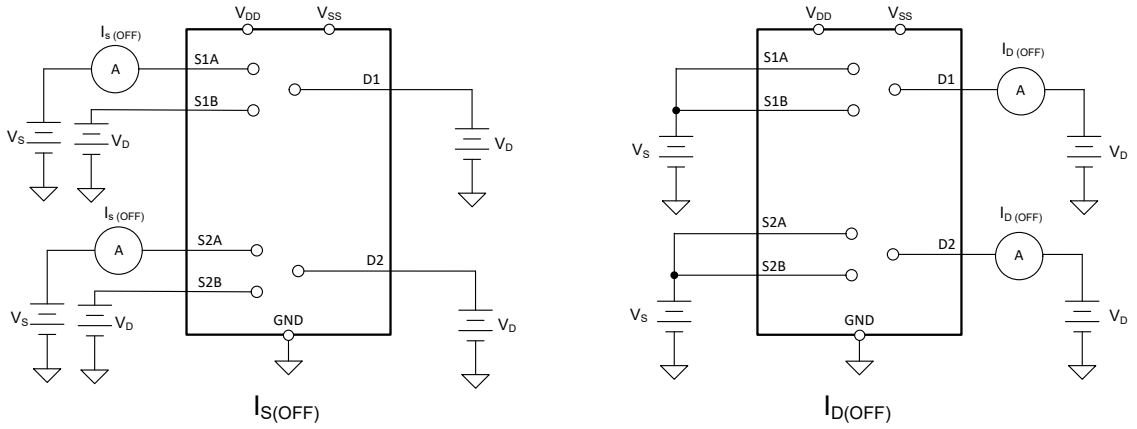


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

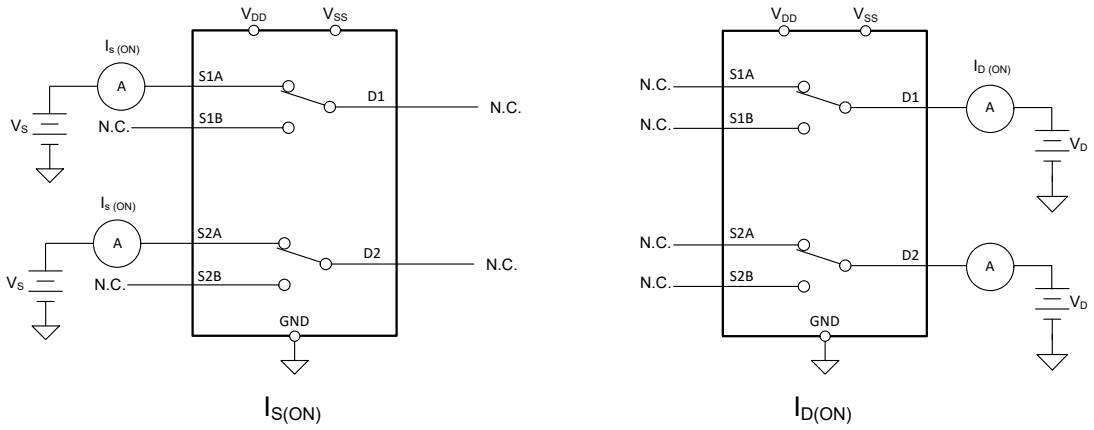


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

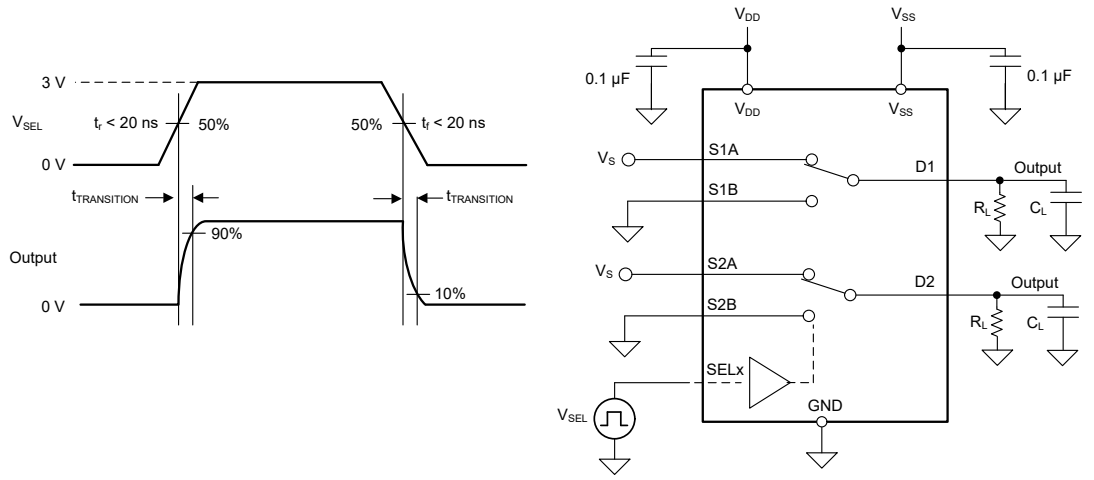


Figure 7-4. Transition-Time Measurement Setup

7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-7 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-7 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

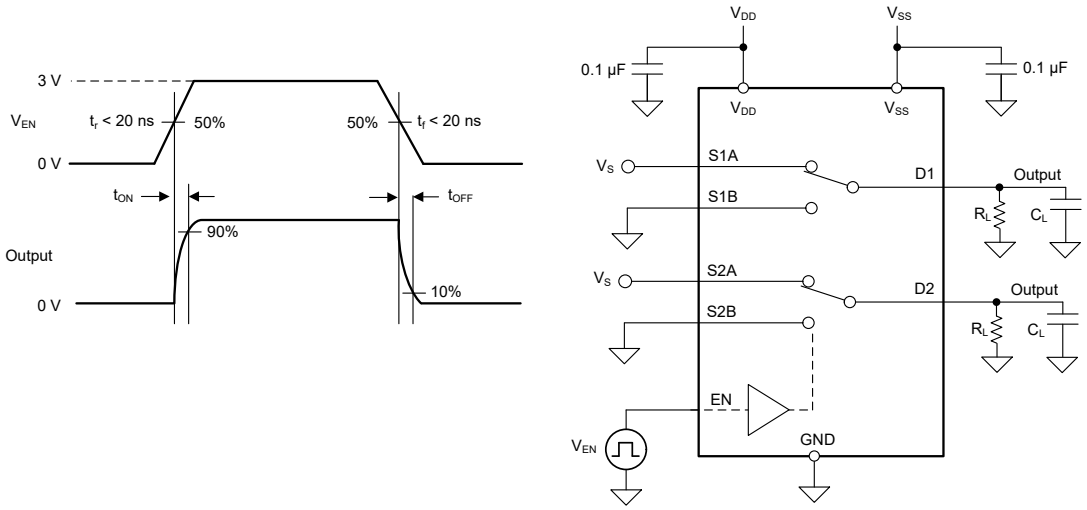


Figure 7-5. Turn-On and Turn-Off Time Measurement Setup

7.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

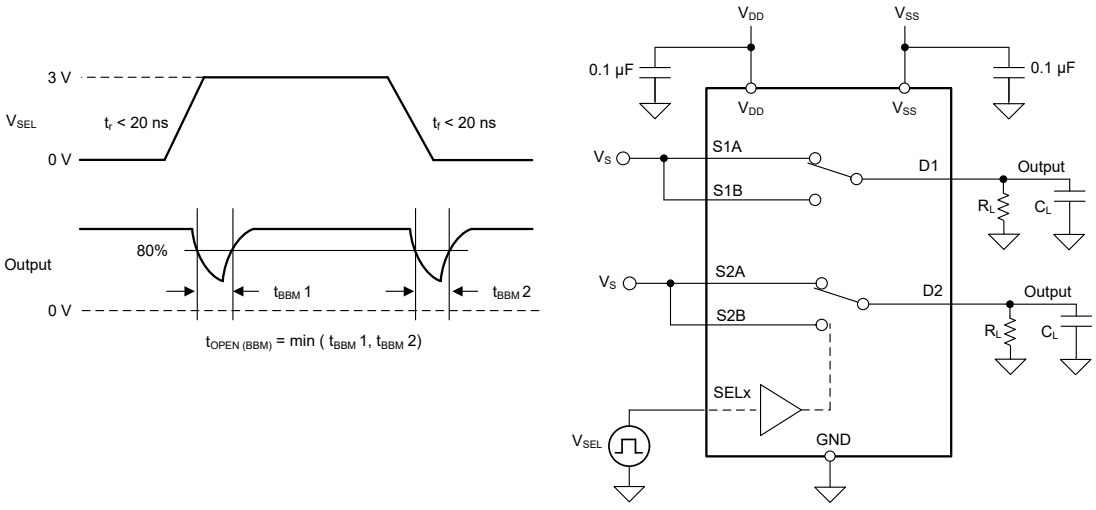


Figure 7-6. Break-Before-Make Delay Measurement Setup

7.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

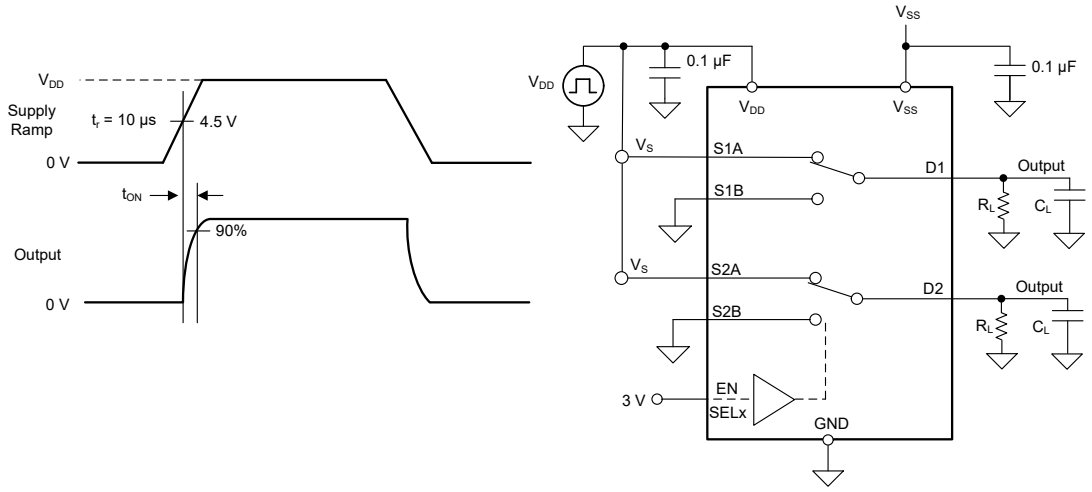


Figure 7-7. $t_{ON\ (VDD)}$ Time Measurement Setup

7.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

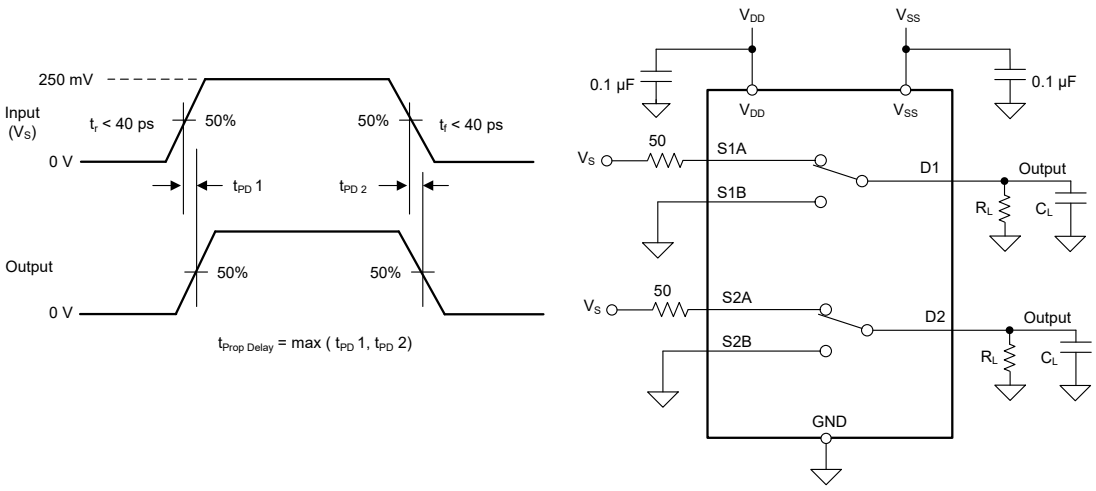


Figure 7-8. Propagation Delay Measurement Setup

7.9 Charge Injection

The TMUX7236 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

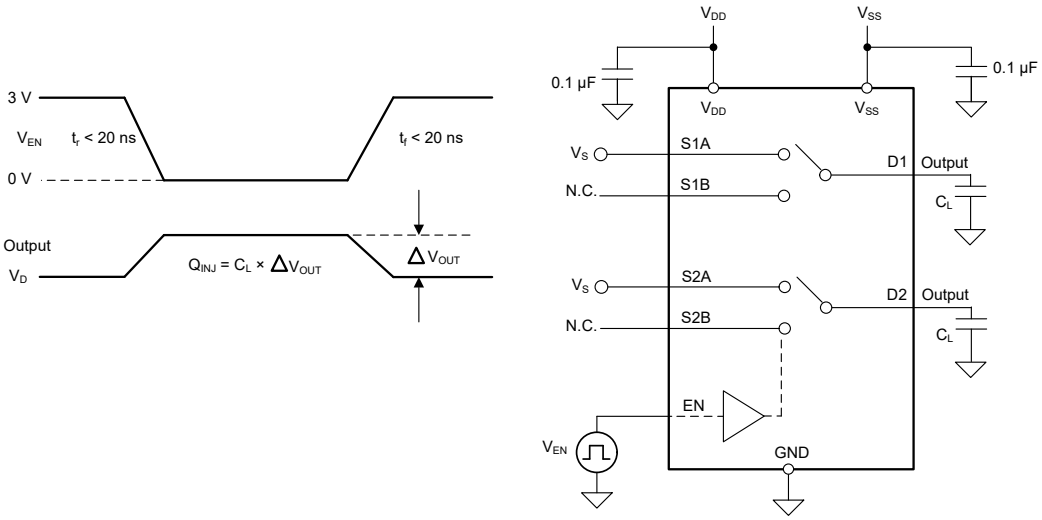


Figure 7-9. Charge-Injection Measurement Setup

7.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-10 shows the setup used to measure, and the equation used to calculate off isolation.

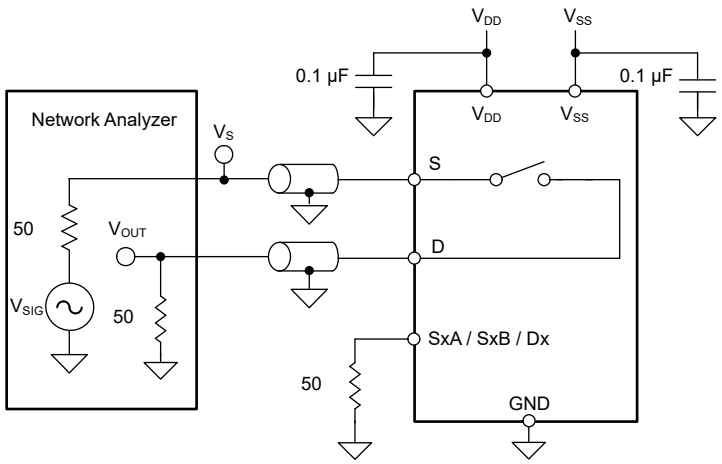


Figure 7-10. Off Isolation Measurement Setup

7.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 7-11 shows the setup used to measure and the equation used to calculate crosstalk.

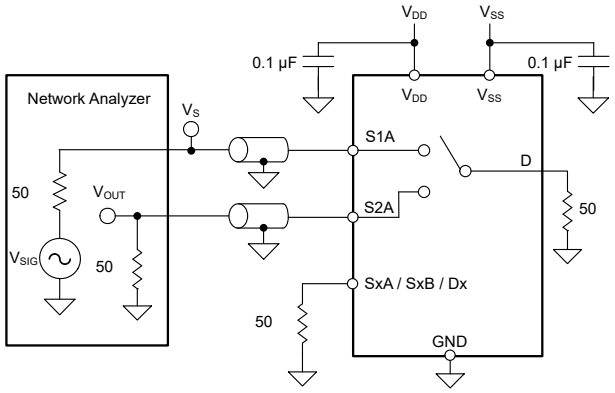


Figure 7-11. Crosstalk Measurement Setup

7.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 7-12 shows the setup used to measure bandwidth.

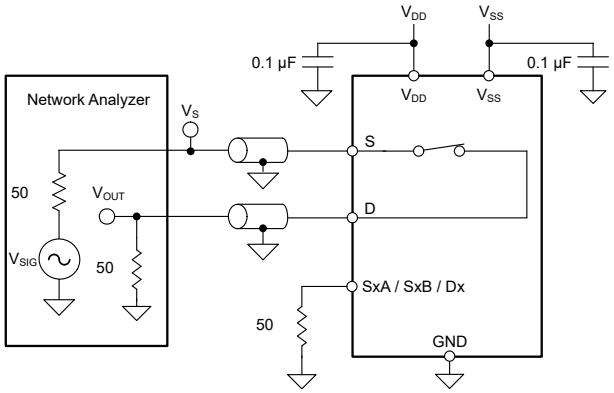


Figure 7-12. Bandwidth Measurement Setup

7.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

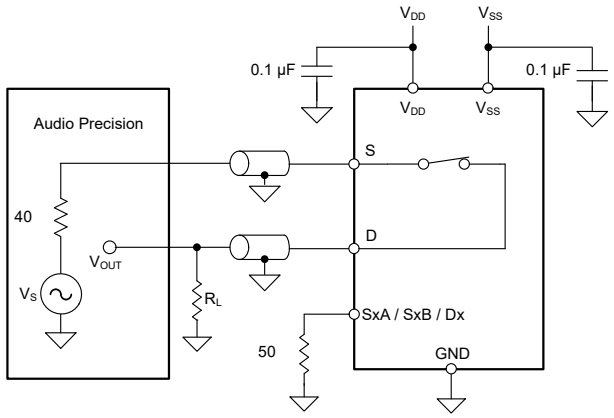


Figure 7-13. THD Measurement Setup

7.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

Figure 7-14 shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.

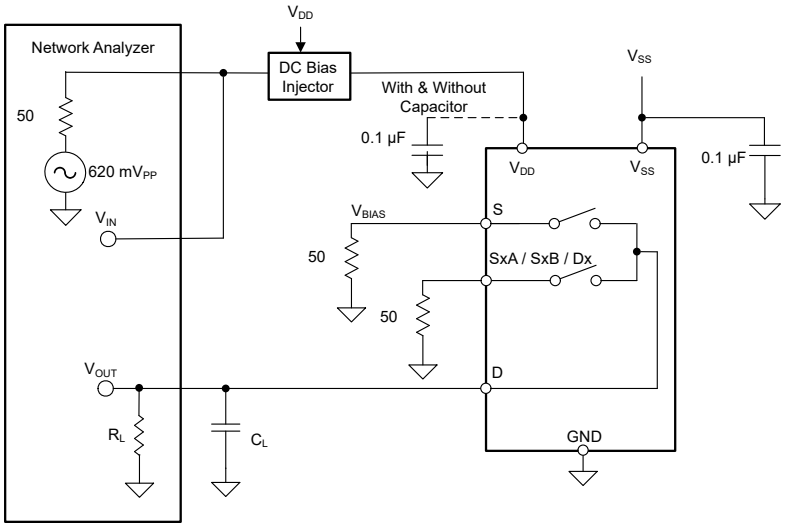
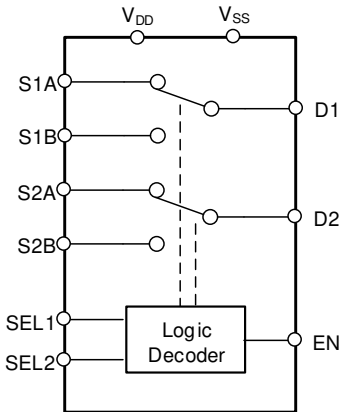


Figure 7-14. ACPSRR Measurement Setup

8 Detailed Description

8.1 Functional Block Diagram

The TMUX7236 is a 2:1, 2-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the select lines and enable pin.



8.2 Feature Description

8.2.1 Bidirectional Operation

The TMUX7236 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.2.2 Rail to Rail Operation

The valid signal path input or output voltage for TMUX7236 ranges from V_{SS} to V_{DD}.

8.2.3 1.8 V Logic Compatible Inputs

The TMUX7236 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX7236 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of materials (BOM) cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.2.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX7236 has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to three external components and reduces system size and cost.

8.2.5 Fail-Safe Logic

The TMUX7236 supports Fail-Safe Logic on the control input pins (EN and SEL) allowing the device to operate up to 44 V above V_{SS}, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX7236 to be ramped to +44 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +44 V in the powered-off condition, but does not offer protection against negative overvoltage conditions.

8.2.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. The latch-up condition is caused by a trigger (current injection or overvoltage); but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7236 is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7236 to be used in harsh environments. For more information on latch-up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.2.7 Ultra-Low Charge Injection

Figure 8-1 shows how the TMUX7236 device has a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

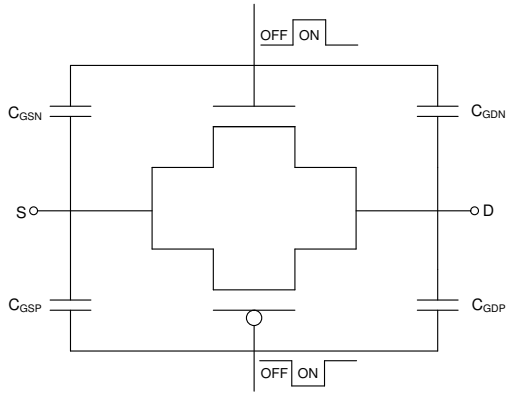


Figure 8-1. Transmission Gate Topology

The TMUX7236 contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition is pushed into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). Figure 8-2 shows charge injection variation with different compensation capacitors on the Source side. Figure 8-2 was captured on the TMUX7219 as part of the TMUX72xx family with a 100 pF load capacitance.

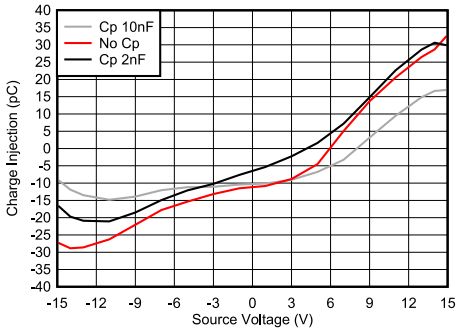


Figure 8-2. Charge Injection Compensation

8.3 Device Functional Modes

When the EN pin of the TMUX7236 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 44 V.

8.4 Truth Tables

Table 8-1 show the truth tables for the TMUX7236.

Table 8-1. TMUX7236 Truth Table

EN	SELx	Selected Input Connected To Drain (D) Pin
0	X(1)	All channels are off (Hi-Z)
1	0	SxB
1	1	SxA

(1) X denotes *do not care*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX7236 is part of the precision switches and multiplexers family of devices. This device operates with dual supplies (±4.5 V to ±22 V), a single supply (4.5 V and 44 V), or asymmetric supplies (such as, V_{DD} = 12 V and V_{SS} = −5 V), and offers rail-to-rail input and output. The TMUX7236 offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX7236 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

One application for the TMUX7236 is in data acquisition systems. For these types of input modules, accuracy and precision is key. To help account for drift over time and temperature, a calibration path is often added to calibrate the input in real time before a measurement. An SPDT switch can be used to switch in this calibration path, which the TMUX7236 is ideal for. This device offers a very low on-resistance, leakage, and charge injection, which ensures a high measurement fidelity and reduces error. The break-before-make feature allows switching from the calibration path without shorting the inputs together. This device also offers on-resistance mismatch, which makes this device suitable for high precision systems. As Figure 9-1 shows, the TMUX7236 can be used in both voltage and current acquisition.

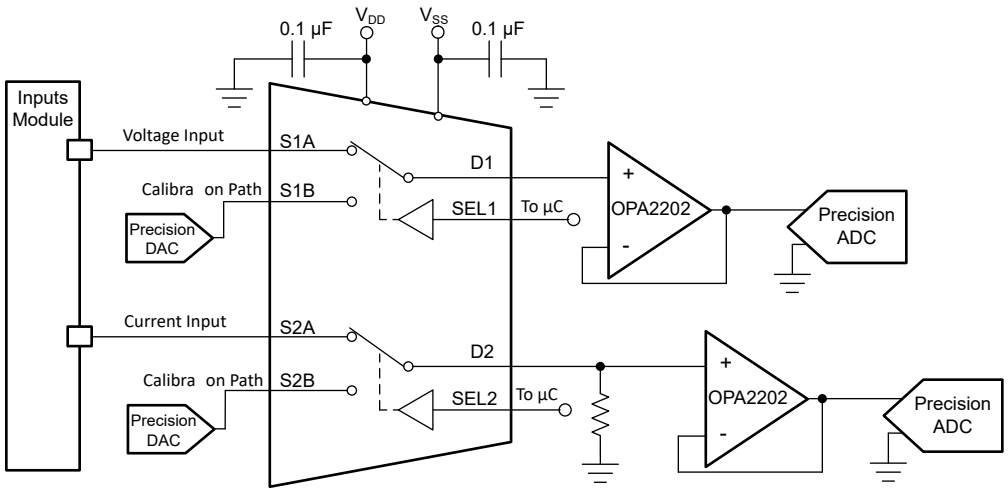


Figure 9-1. Data Acquisition Systems (DAQ) Calibration

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15 V
Supply (V_{SS})	−15 V
MUX I/O signal range	−15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatiable (up to V_{DD})
EN	EN pulled high to enable the switch

9.2.2 Detailed Design Procedure

The TMUX7236 can operate without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommended operating conditions of the TMUX7236, including signal range and continuous current. The signal range for this design can be up to −15 V to +15 V and the maximum continuous current can be up to 330 mA for wide-range current measurement with a positive supply of 15 V on V_{DD} and negative supply of −15 V on V_{SS} (for more information, see Section 6.4). The TMUX7236 device is a bidirectional, single-pole double-throw (SPDT) switch that offers low on-resistance, low leakage, and low power. These features make this device suitable for precision and power sensitive applications.

9.2.3 Application Curve

The low on-resistance of TMUX7236 and ultra-low charge injection performance make this device ideal for implementing high precision systems. Figure 9-2 shows the plot for the on-resisitance versus temperature. Additionally, the TMUX7236 features a very low mismatch between channels, which is important for this application because it reduces the difference between the calibration and non-calibration paths. The TMUX7236 features mismatch between channels <180 mΩ and 100 mΩ typically.

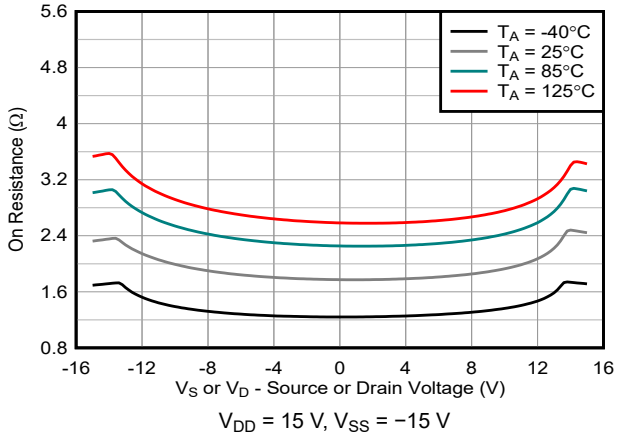


Figure 9-2. On-Resistance vs Temperature

9.2.3.1 On-Resistance Mismatch Between Channels

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω

10 Power Supply Recommendations

The TMUX7236 operates across a wide supply range of of ±4.5 V to ±22 V (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

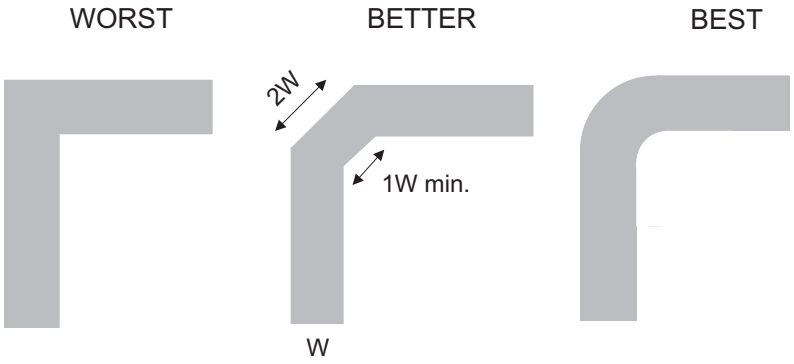


Figure 11-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. TI recommends a 0.1-µF and 1-µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

11.2 Layout Example

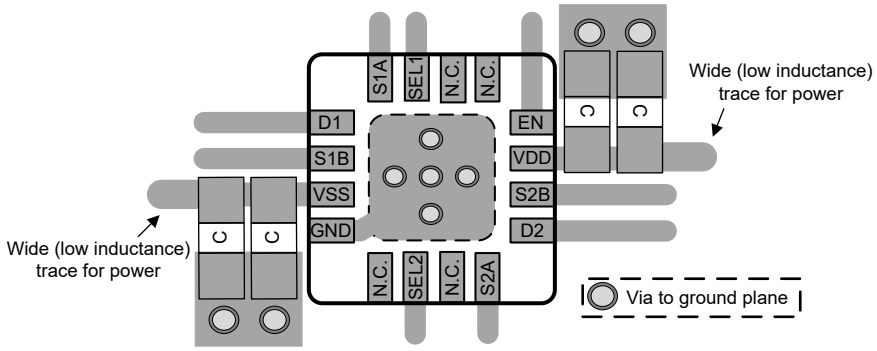


Figure 11-2. TMUX7236 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*
- Texas Instruments, *QFN/SON PCB Attachment*
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX7236RUMR	ACTIVE	WQFN	RUM	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX7236RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX T236	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

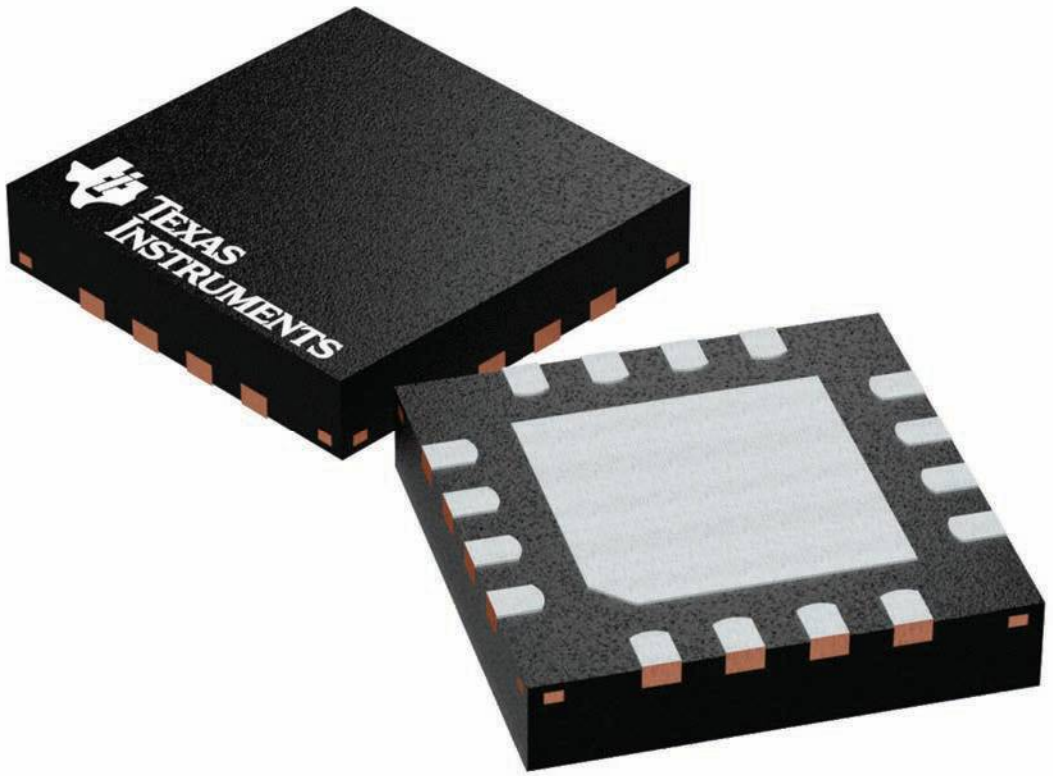
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



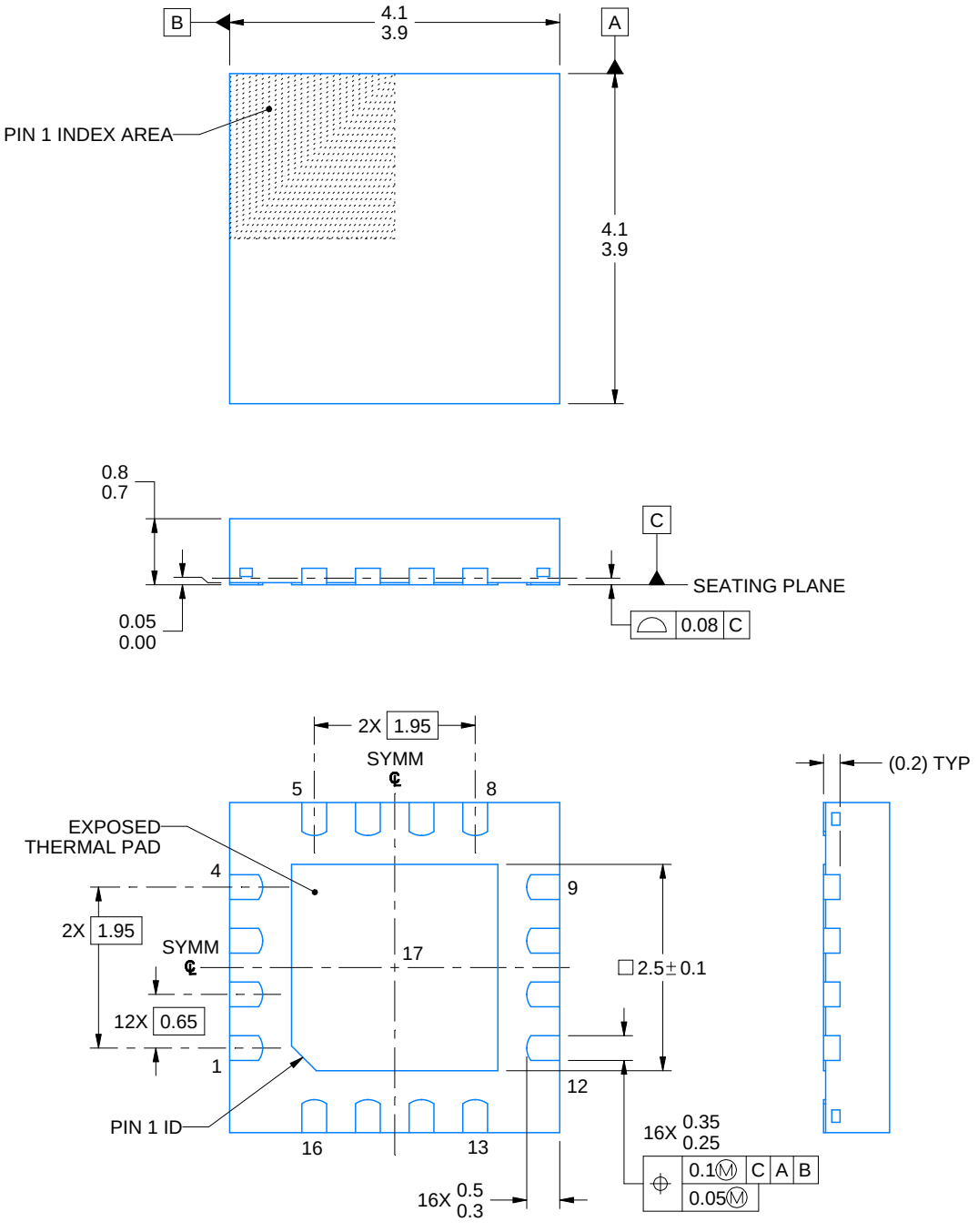
4224843/A

RUM0016E

PACKAGE OUTLINE

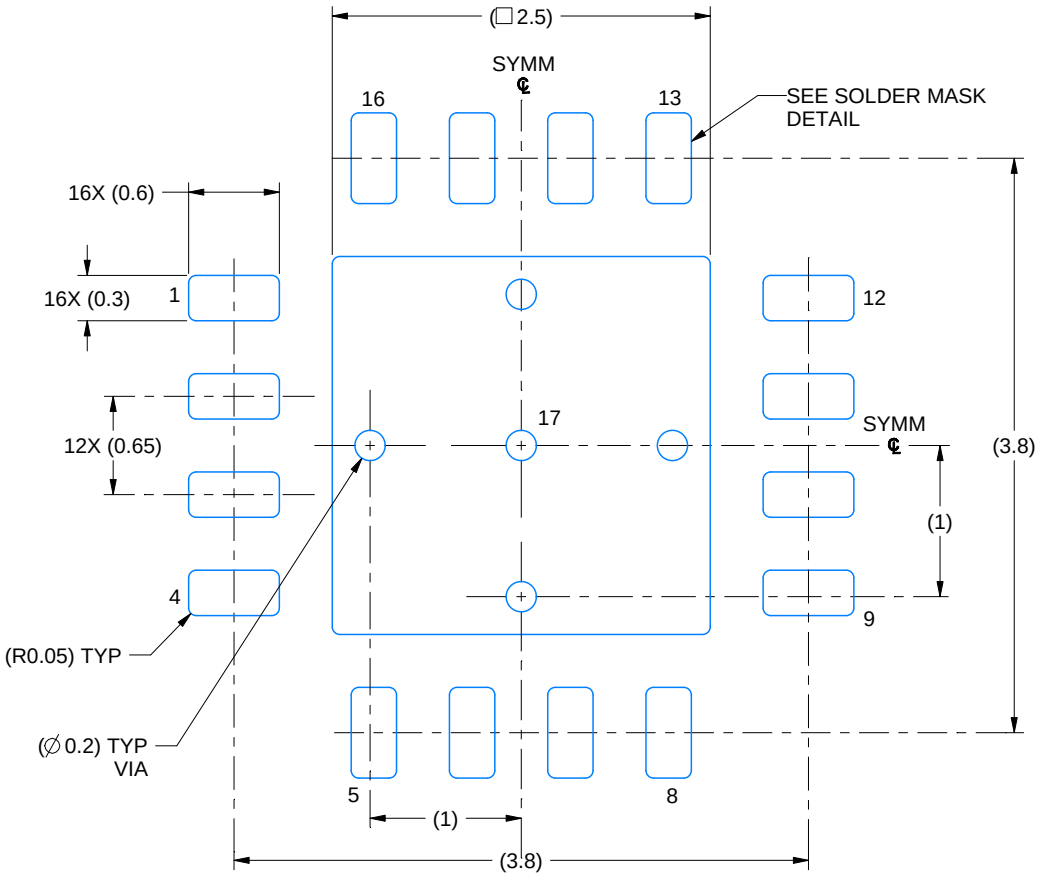
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

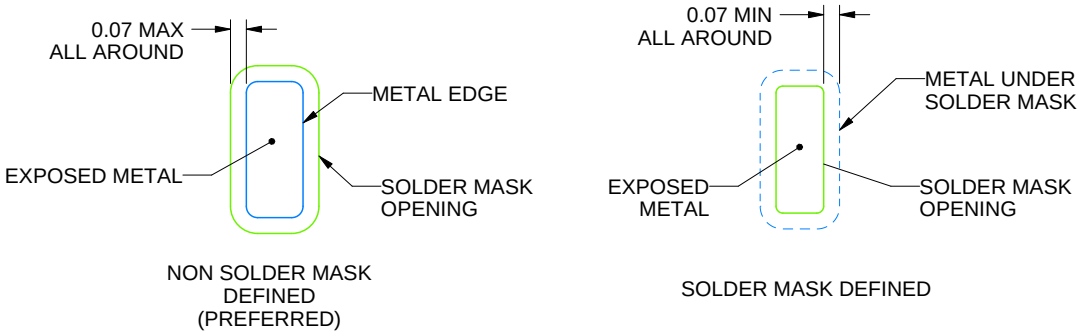


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224815/A 02/2019

NOTES: (continued)

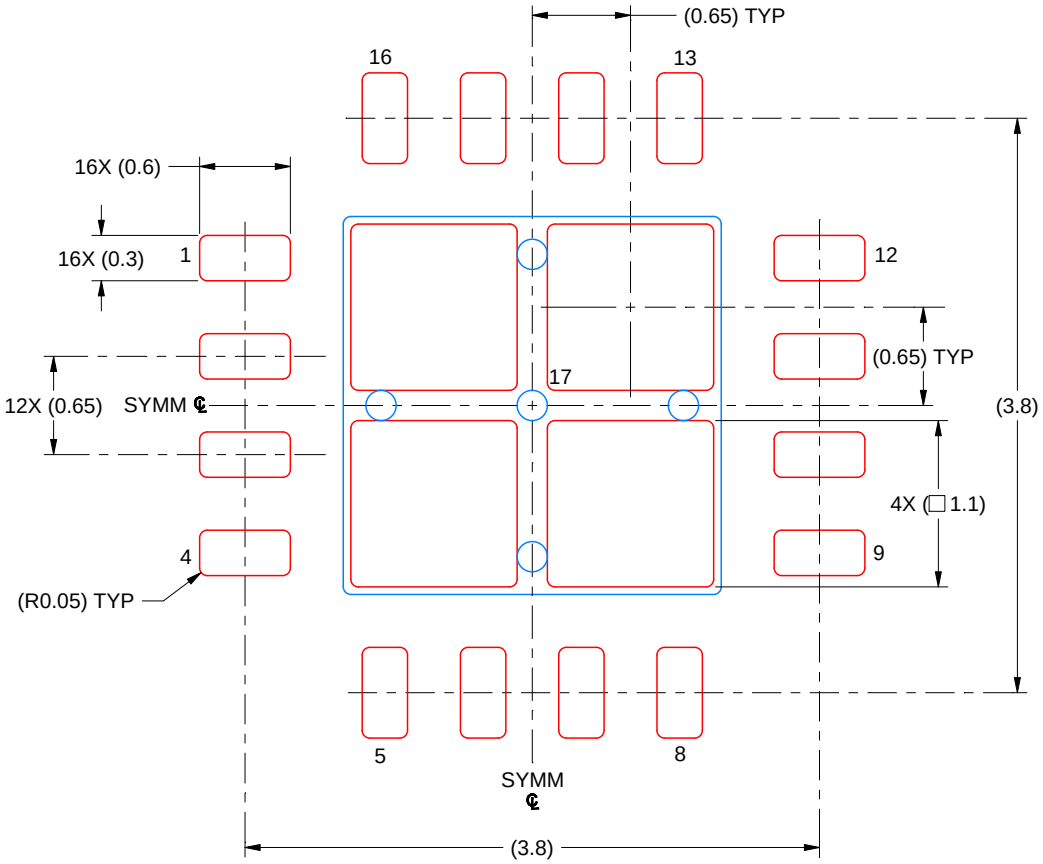
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPS7A74 1.5-A, Low-Dropout Linear Regulator With Programmable Soft-Start

1 Features

- V_{OUT} range: 0.65 V to 3.6 V
- Ultra-low V_{IN} range: 0.65 V to 6 V
- V_{BIAS} range: 1.7 V to 6 V
- Low dropout: 150 mV typical at 1.5 A, V_{BIAS} = 5 V
- Noise: 7.1 μV_{RMS}
- PSRR:
  - 70 dB at 1 kHz
  - 60 dB at 10 kHz
  - 55 dB at 100 kHz
  - 50 dB at 1 MHz
- 1.5% accuracy over line, load, and temperature
- Programmable soft-start provides linear voltage start-up
- V_{BIAS} permits low V_{IN} operation with good transient response
- UVLO on both IN and BIAS
- Stable with any output capacitor ≥ 10 µF
- Package: Small, 3-mm × 3-mm × 0.8-mm WSON-8

2 Applications

- High-performance computing
- Microservers
- Desktop and PC motherboards
- Data concentrators
- Rugged PC laptops

3 Description

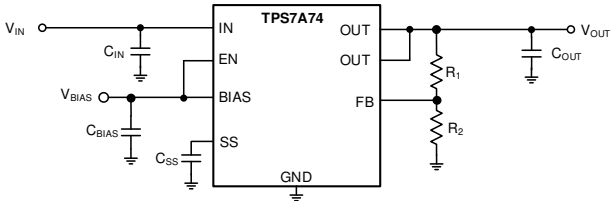
The TPS7A74 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start up. The soft-start is monotonic and well-suited for powering many different types of processors and application-specific integrated circuits (ASICs). The enable input allows for easy sequencing with external regulators. This complete flexibility allows a solution to be configured that meets the sequencing requirements of field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and other applications with special start-up requirements.

A precision reference and error amplifier deliver 1.5% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 10 µF, and is fully specified for T_J = –40°C to +125°C. The TPS7A74 is offered in a small, 3-mm × 3-mm, WSON-8 package, yielding a highly compact, total solution size.

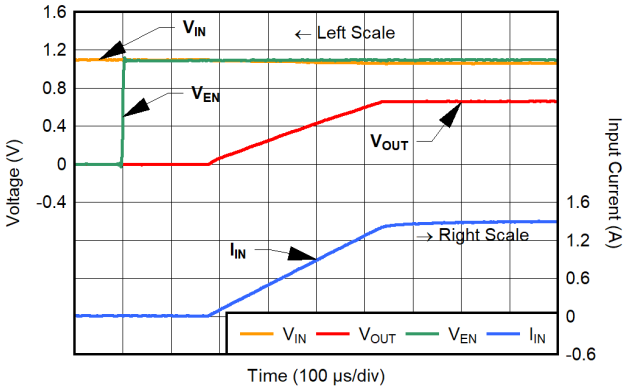
Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A74	WSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit (Adjustable)



Loaded Start-Up

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (July 2022)	Page
• Changed document status from *advance information* to *production data*	1

5 Pin Configuration and Functions

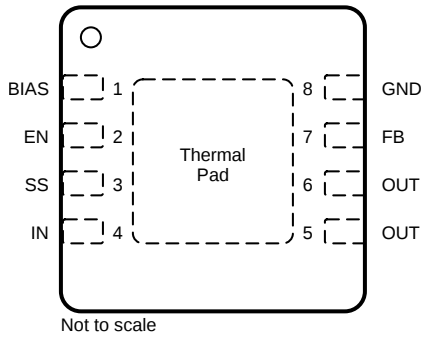


Figure 5-1. DSD Package, 8-Pin WSON With Thermal Pad (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	BIAS	I	Bias input voltage for error amplifier, reference, and internal control circuits. Use a 0.1 µF or larger input capacitor for optimal performance. If IN is connected to BIAS, a 4.7 µF or larger capacitor must be used.
2	EN	I	Enable pin.
3	SS	I	Soft-start pin. This pin must be connected to a capacitor to GND.
4	IN	I	Input to the device. Use a 1 µF or larger input capacitor for optimal performance.
5, 6	OUT	O	Regulated output voltage. A small capacitor (total typical capacitance of ≥ 10 µF, ceramic) is required from this pin to ground to assure stability.
7	FB	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
8	GND	—	Ground.
—	Thermal Pad	—	Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	6.5	V
Bias voltage	BIAS	–0.3	6.5	V
Enable voltage	EN	–0.3	6.5	V
Soft-start voltage	SS	–0.3	6.5	V
Feedback voltage	FB	–0.3	2	V
Output voltage	OUT	–0.3	V_{IN} + 0.3	V
Maximum output current	I_{LIMIT}	Internally limited		
Output short-circuit duration	I_{SC}	Indefinite		
Continuous total power dissipation	P_{DISS}	See Thermal Information		
Junction Temperature	T_J	–40	150	°C
Storage Temperature	T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	0.65		V_{BIAS} – 0.1	V
V_{BIAS} (1)	BIAS supply voltage	1.7		6	V
V_{EN}	Enable voltage			6	V
V_{OUT}	Output voltage	0.65		3.6	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	10			µF
C_{IN}	Input capacitor(2)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A74		UNIT
		DSD (WSON) (2)	DSD (WSON) (3)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.3	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.3	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.3	18.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) JEDEC standard. (2s2p, no vias to internal planes and bottom layer).
(3) TPS7A74 thermal characteristics on EVM.

6.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 10 nF, I_{OUT} = 10 mA, V_{BIAS} = 5.0 V (3), and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (adj.)		0.641	0.65	0.659	V
	Output accuracy (1) (4) (5)	2.97 V ≤ V_{BIAS} ≤ 6 V, 0 mA ≤ I_{OUT} ≤ 1.5 A	–1.5	±0.5	1.5	%
	Line regulation (V_{BIAS})	Max(2.7 V, V_{OUT} + 1.6 V) ≤ V_{BIAS} ≤ 6 V		0.2	0.32	%/V
	Line regulation (V_{IN})	$V_{OUT(nom)}$ + 0.15 V ≤ V_{IN} ≤ 6 V		0.01	0.05	%/V
	Load regulation	0 mA ≤ I_{OUT} ≤ 1.5 A		0.33		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 2.8 V		150	180	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}		1.1	1.3	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2	2.7	3.3	A
I_{BIAS}	BIAS pin current	I_{OUT} = 10 mA		0.25	0.33	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 6 V, V_{BIAS} = 6 V		1	55	µA
I_{FB}	Feedback pin current		–1	0.15	1	µA
$V_{BIAS(UVLO)}$	Bias rail UVLO rising threshold		1.04	1.4	1.65	V
$V_{BIAS(UVLO),HYST}$	Bias rail UVLO hysteresis		0.02	0.06	0.07	V

6.5 Electrical Characteristics (continued)

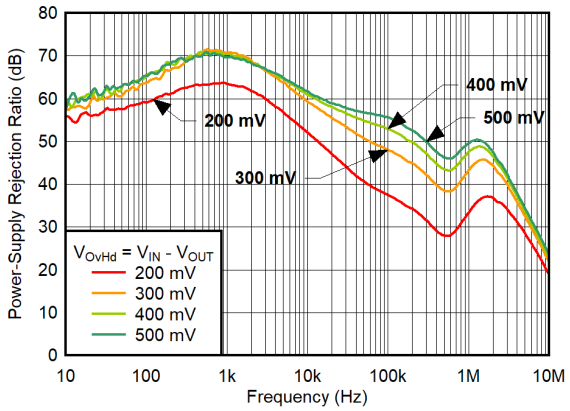
at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 10 nF, I_{OUT} = 10 mA, V_{BIAS} = 5.0 V (3), and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(UVLO),\ rising}$	In rail UVLO rising threshold		0.39	0.455	0.5	V
$V_{IN(UVLO),\ falling}$	In rail UVLO falling threshold		0.21	0.26	0.3	V
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open	55		310	µs
I_{SS}	Soft-start charging current	V_{SS} = 0 V	8	17	31	µA
V_{SS}	Soft-start pin disable voltage	V_{EN} = 0 V		0	50	mV
PSRR	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, Iout = 1.5 A, Vin = 1.8 V, Vout = 1.5 V		57		dB
		300 kHz, Iout = 1.5 A, Vin = 1.8 V, Vout = 1.5 V		27		
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	BW = 10 Hz to 1 MHz, I_{OUT} = 1 A, V_{IN} = 2.05 V, V_{OUT} = 1.8 V		27		dB
Vn	Output voltage noise	BW = 10 Hz to 100 kHz, I_{OUT} = 1 A, V_{IN} = 0.95 V, V_{OUT} = 0.65 V		7.1		μV_{RMS}
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.2	µA
$R_{PULLDOWN(OUT)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			0.6	1	kΩ
$R_{PULLDOWN(FB)}$	V_{BIAS} = 5 V, V_{EN} = 0 V			120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.65 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) V_{BIAS} = $V_{DO\_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.4 V
(4) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

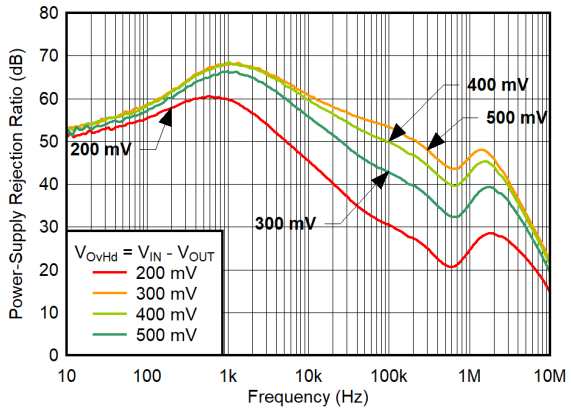
6.6 Typical Characteristics

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



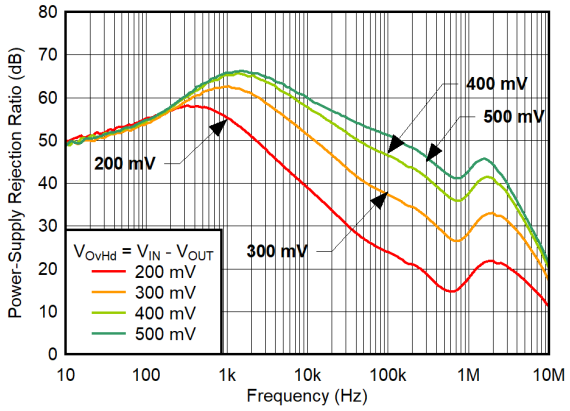
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-1. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 400 mA, V_{OUT} = 1.8 V



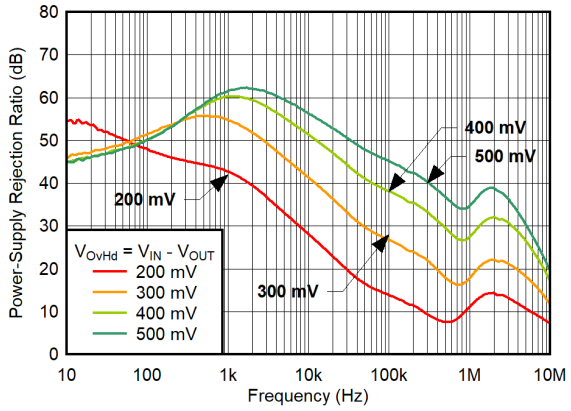
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-2. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 750 mA, V_{OUT} = 1.8 V



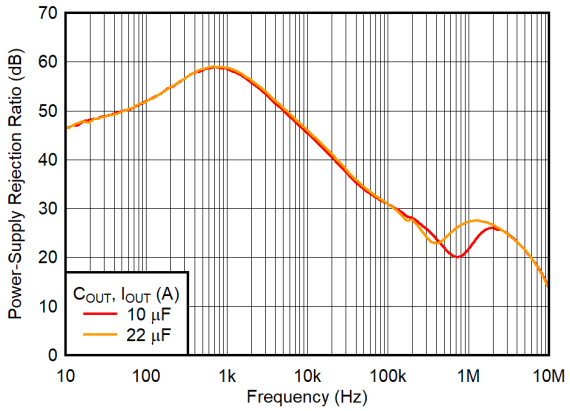
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-3. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 1.1 A, V_{OUT} = 1.8 V



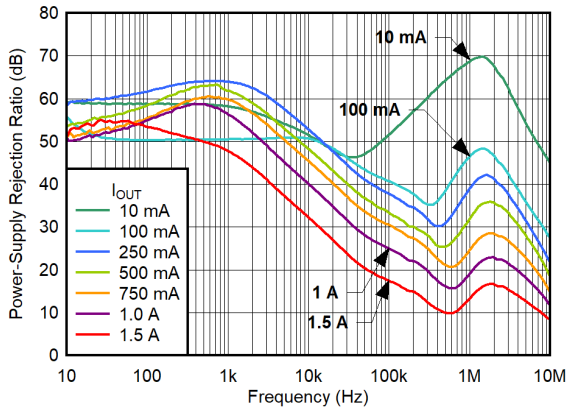
C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-4. PSRR vs Frequency and Overhead (OvHd) Voltage for I_{OUT} = 1.5 A, V_{OUT} = 1.8 V



C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A

Figure 6-5. PSRR vs Frequency and C_{OUT} for V_{OUT} = 1.8 V

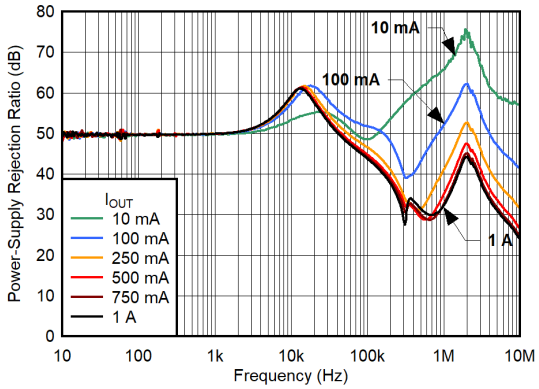


C_{IN} = 0 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-6. PSRR vs Frequency and I_{OUT} for V_{OvHd} = 200 mV

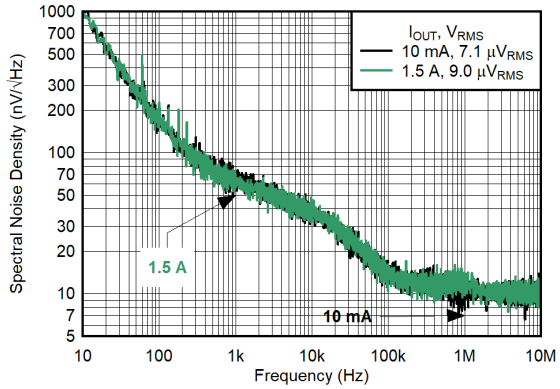
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



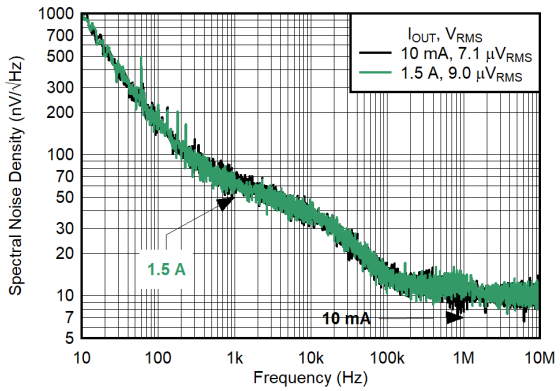
V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0 µF, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-7. Bias Rail PSRR vs Frequency and I_{OUT}



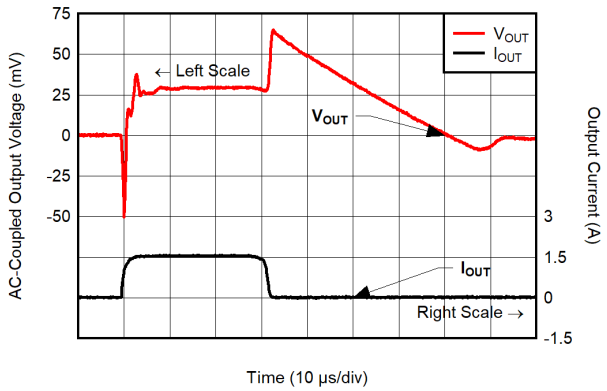
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-8. Noise vs Frequency and I_{OUT} for V_{OUT} = 0.65 V



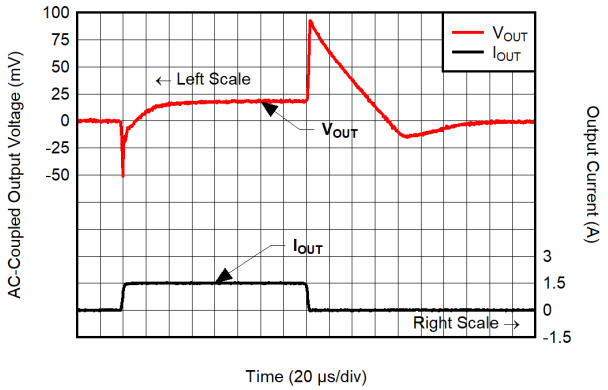
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF

Figure 6-9. Noise vs Frequency and I_{OUT} for V_{OUT} = 3.3 V



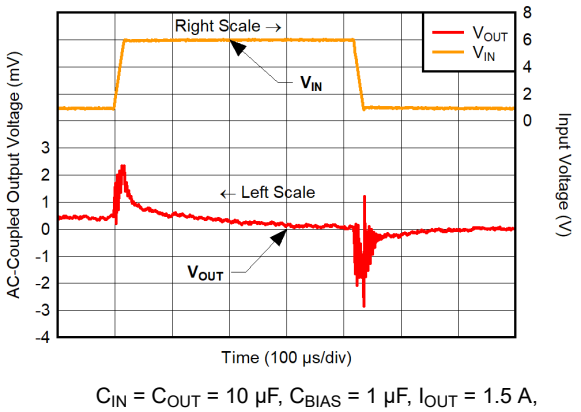
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 10 mA to 1.5 A to 10 mA at 1 A/µs

Figure 6-10. Load Transient for V_{OUT} = 0.65 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 10 mA to 1.5 A to 10 mA at 1 A/µs

Figure 6-11. Load Transient for V_{OUT} = 3.3 V

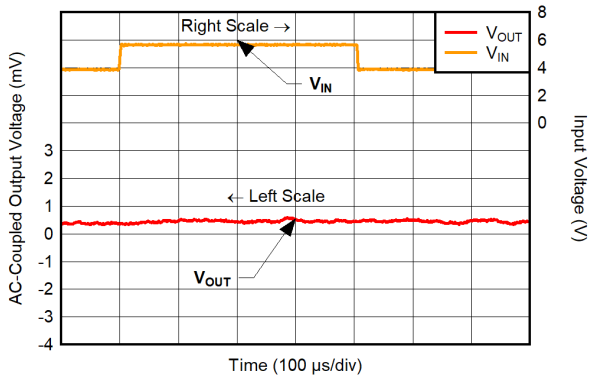


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 0.95 V to 6 V to 0.95 V at 1 V/µs

Figure 6-12. Line Transient for V_{OUT} = 0.65 V

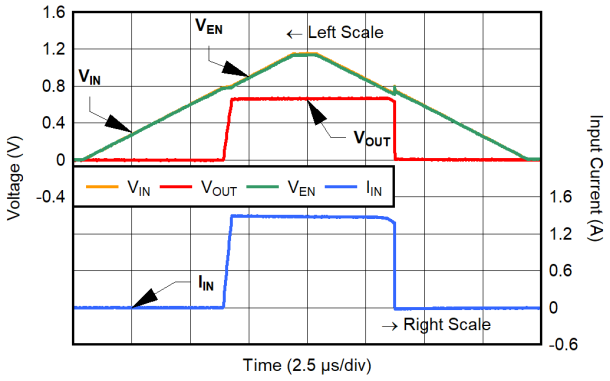
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



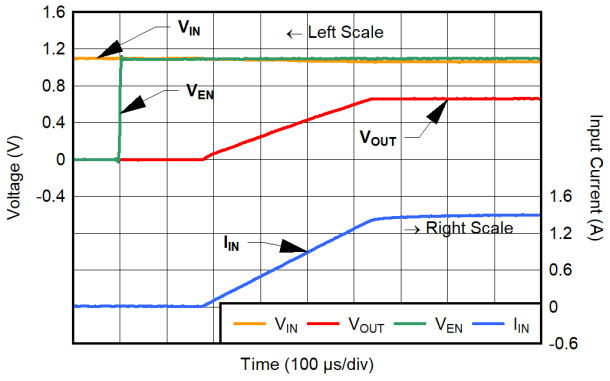
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 3.9 V to 5.8 V to 3.9 V at 1 V/µs

Figure 6-13. Line Transient for V_{OUT} = 3.3 V



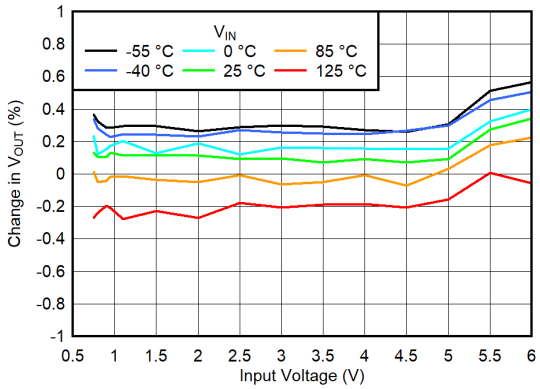
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{BIAS} = 5 V

Figure 6-14. Input Ramp-Up and Ramp-Down



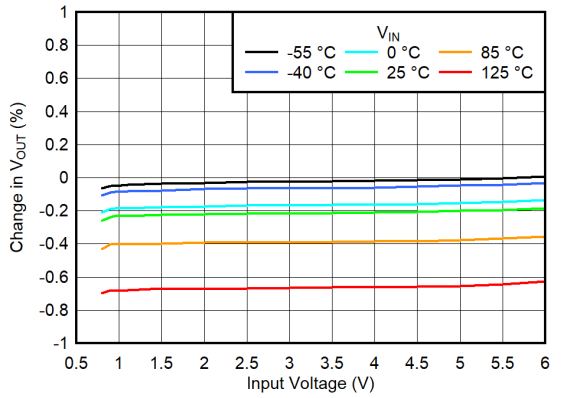
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{BIAS} = 5 V

Figure 6-15. Input Ramp With Fast Soft-Start



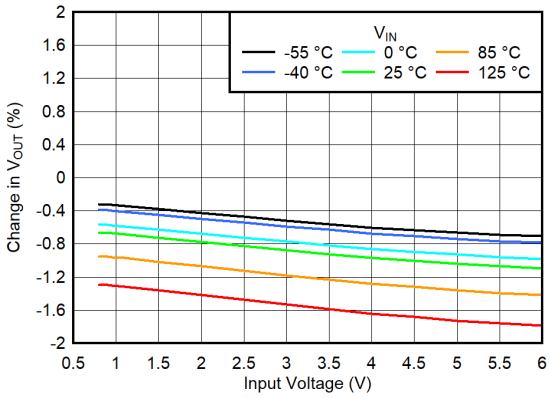
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-16. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-17. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 10 mA

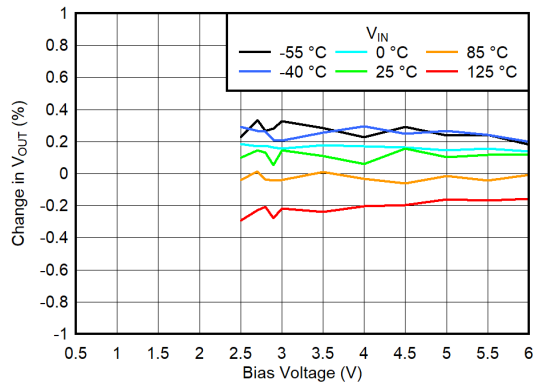


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-18. IN Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 1.5 A

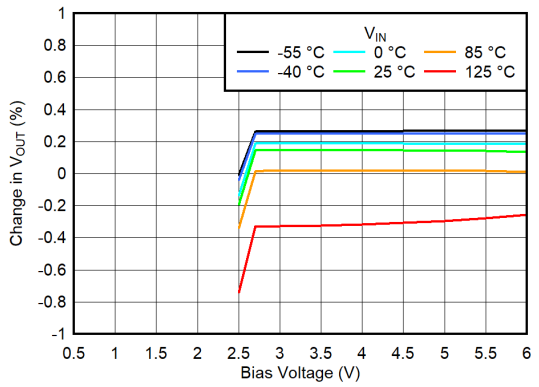
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



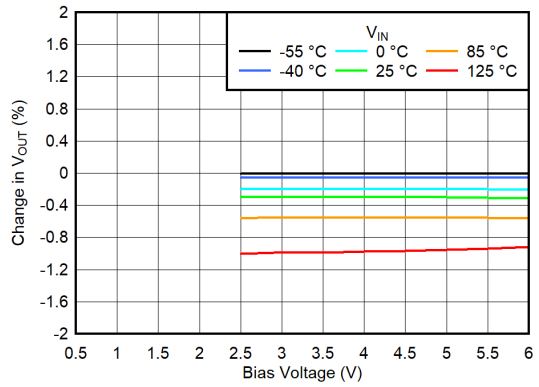
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-19. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 0 A



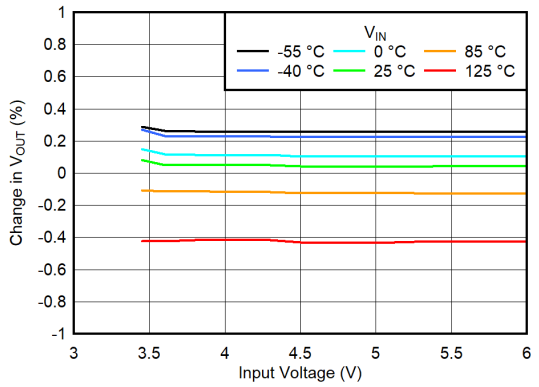
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-20. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 10 mA



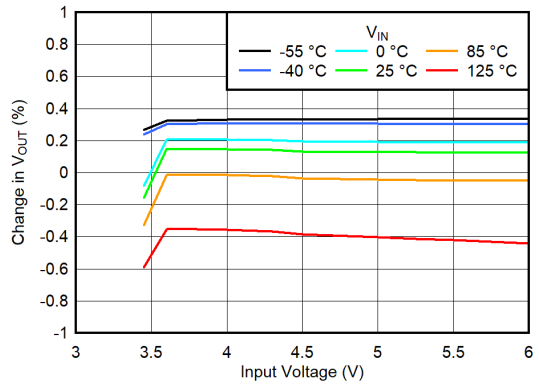
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-21. BIAS Line Regulation for V_{OUT} = 0.65 V, I_{OUT} = 1.5 A



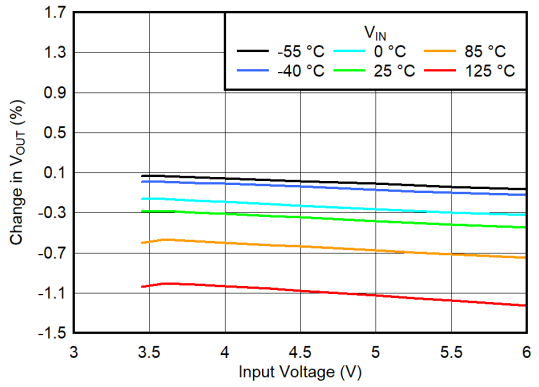
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-22. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-23. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 10 mA

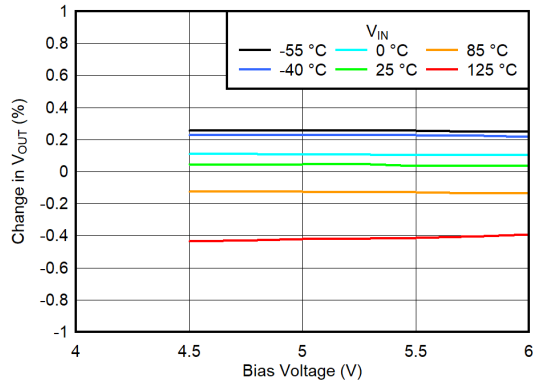


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-24. IN Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 1.5 A

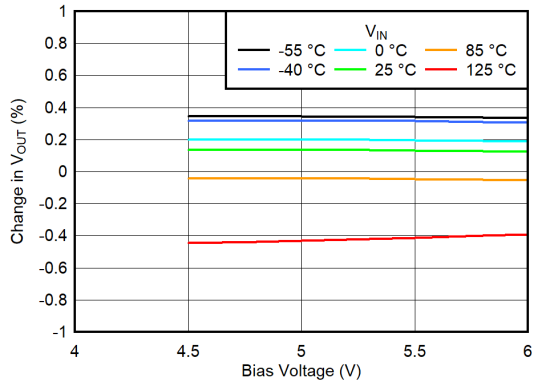
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



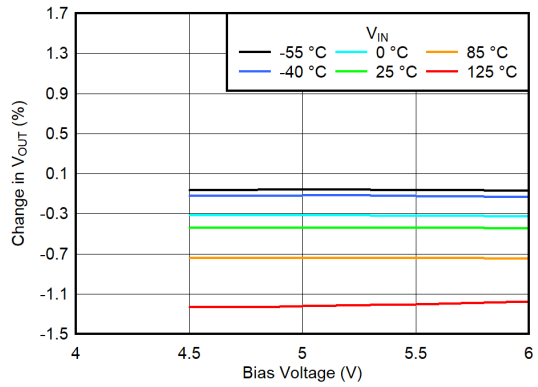
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-25. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 0 A



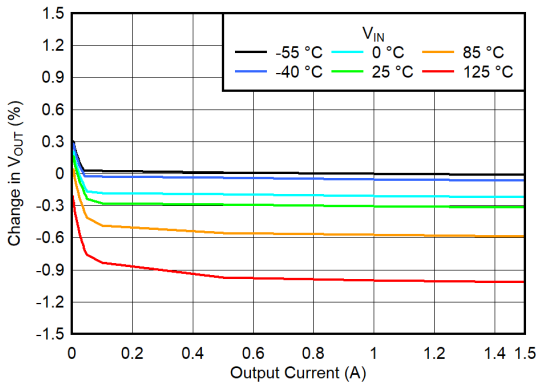
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-26. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 10 mA



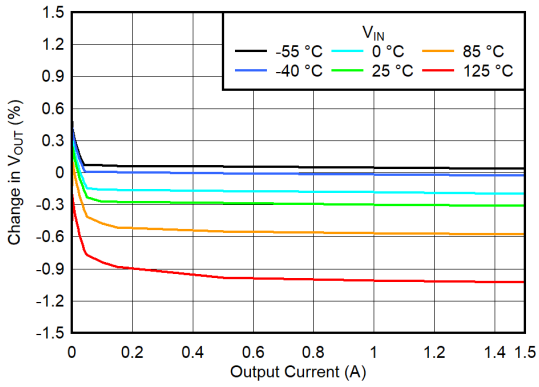
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 3.6 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.1 V

Figure 6-27. BIAS Line Regulation for V_{OUT} = 3.3 V, I_{OUT} = 1.5 A



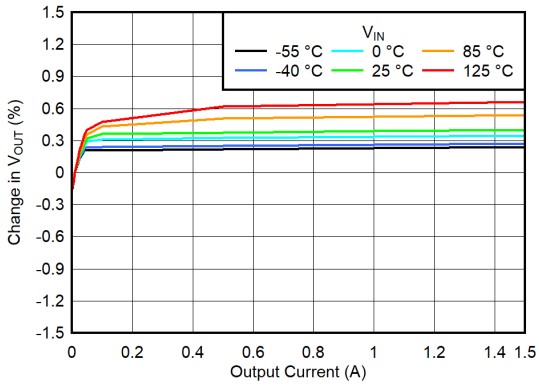
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, 2.3 V ≤ V_{BIAS} ≤ 5 V, V_{EN} = 1.1 V

Figure 6-28. Load Regulation for I_{OUT} = 0 A to Load, V_{OUT} = 0.65 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-29. Load Regulation for I_{OUT} = 0 A to Load, V_{OUT} = 3.3 V

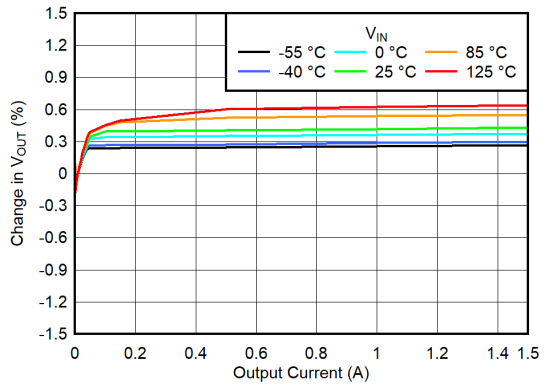


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, 2.3 V ≤ V_{BIAS} ≤ 5 V, V_{EN} = 1.1 V

Figure 6-30. Load Regulation for I_{OUT} = 10 mA to Load, V_{OUT} = 0.65 V

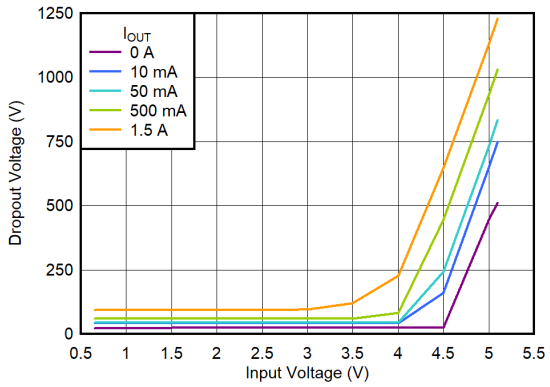
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



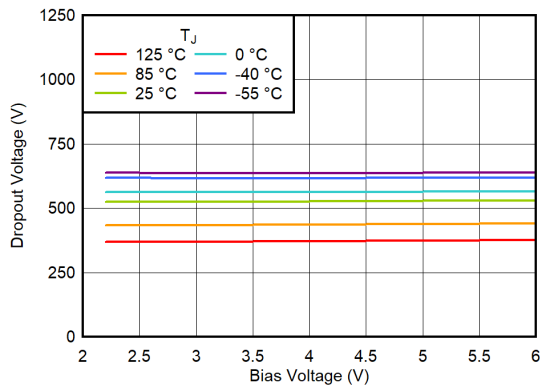
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-31. Load Regulation for I_{OUT} = 10 mA to Load, V_{OUT} = 3.3 V



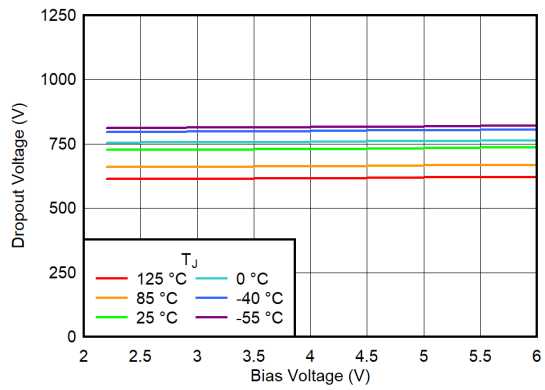
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-32. Dropout Voltage vs Input Voltage



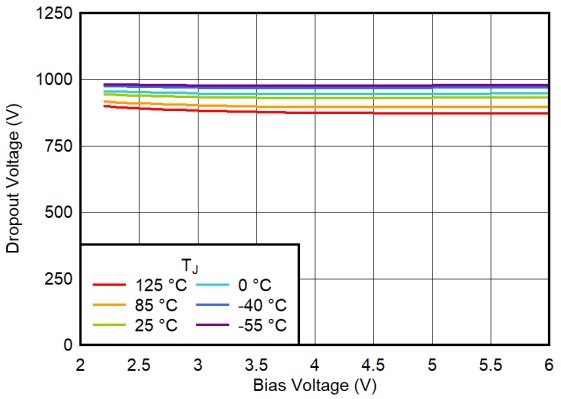
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-33. Dropout Voltage vs Bias Voltage for I_{OUT} = 0 A



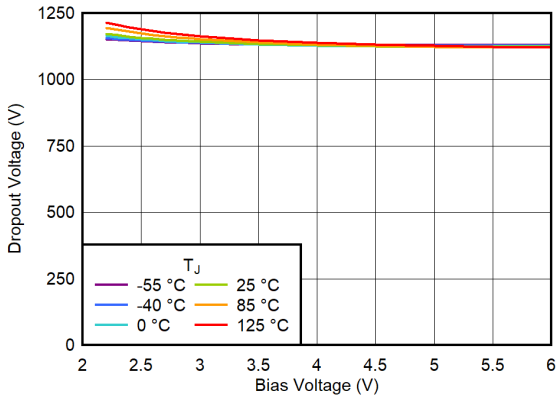
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-34. Dropout Voltage vs Bias Voltage for I_{OUT} = 50 mA



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-35. Dropout Voltage vs Bias Voltage for I_{OUT} = 500 mA

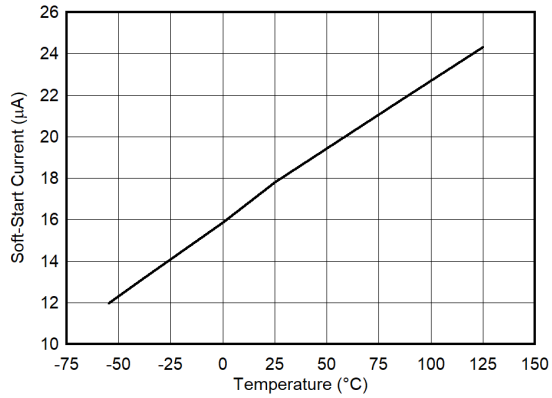


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN}, V_{EN} = 1.1 V

Figure 6-36. Dropout Voltage vs Bias Voltage for I_{OUT} = 1.5 A

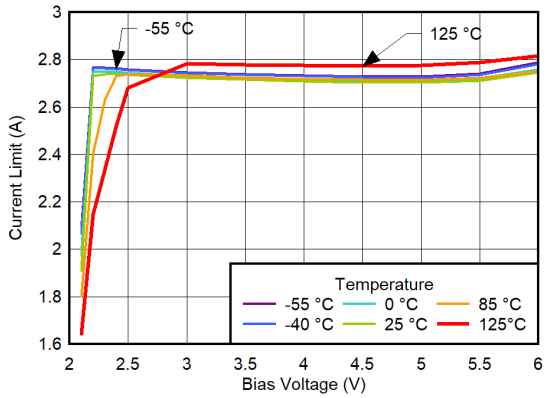
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



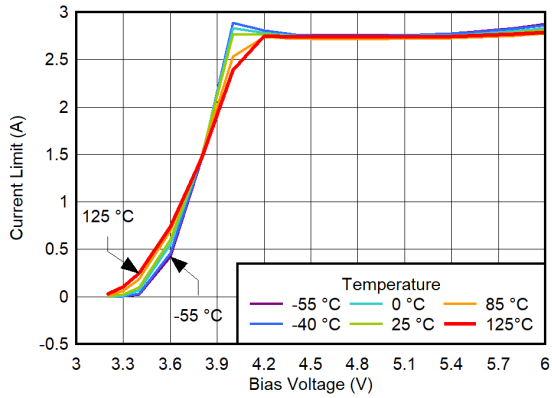
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = V_{IN} = 6 V, V_{OUT} = 0.65 V, V_{EN} = 1.5 V, I_{OUT} = 0 A

Figure 6-37. Soft-Start Current vs Temperature



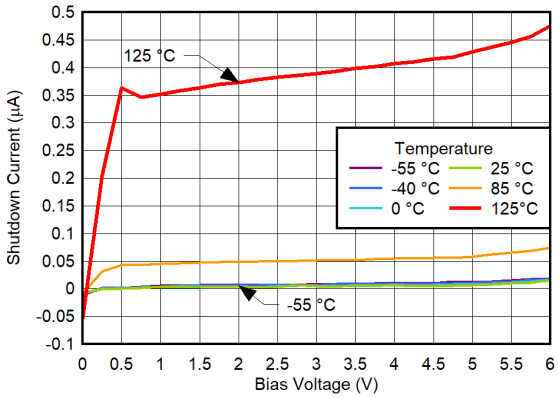
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 0.95 V, V_{EN} = 1.1 V

Figure 6-38. Current Limit vs Bias Voltage for V_{OUT} = 0.65 V



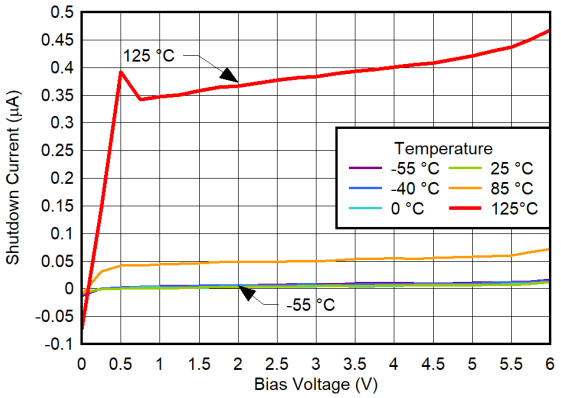
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{EN} = 1.1 V

Figure 6-39. Current Limit vs Bias Voltage for V_{OUT} = 3.3 V



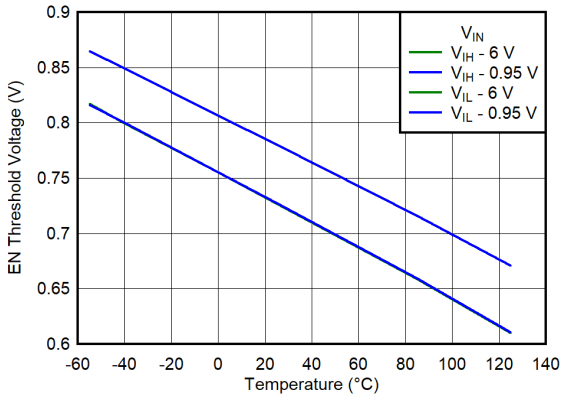
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{EN} = 0.4 V

Figure 6-40. Shutdown Current vs Bias Voltage for V_{IN} = 0.95 V



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{EN} = 0.4 V

Figure 6-41. Shutdown Current vs Bias Voltage for V_{IN} = 6 V

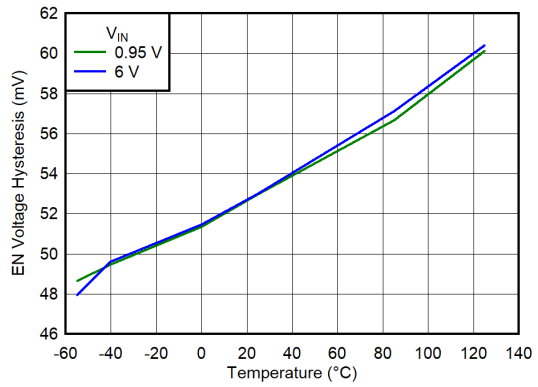


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V

Figure 6-42. Enable Voltage Threshold vs Temperature

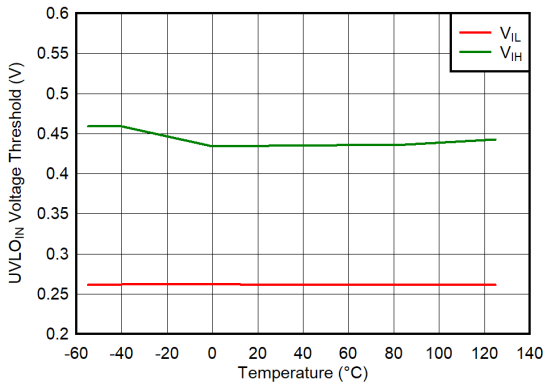
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



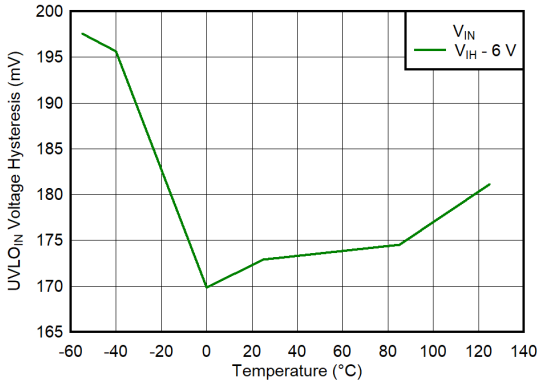
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V

Figure 6-43. Enable Voltage Hysteresis vs Temperature



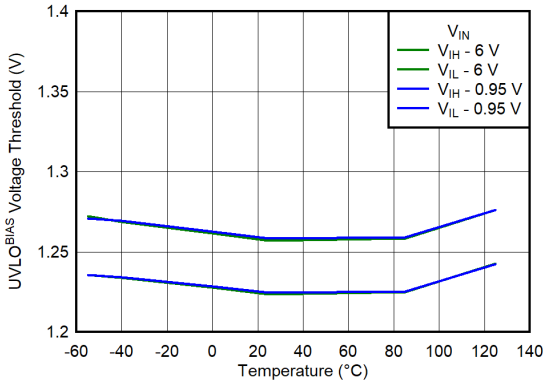
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-44. $UVLO_{IN}$ Voltage Threshold vs Temperature



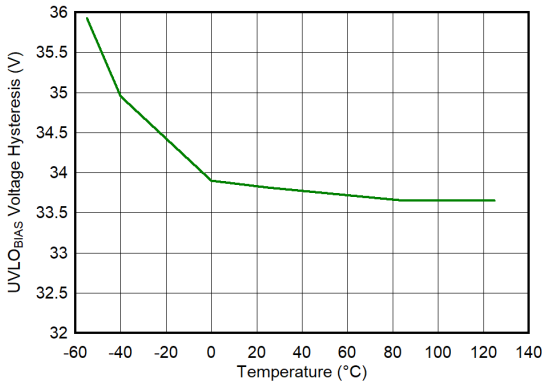
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-45. $UVLO_{IN}$ Voltage Hysteresis vs Temperature



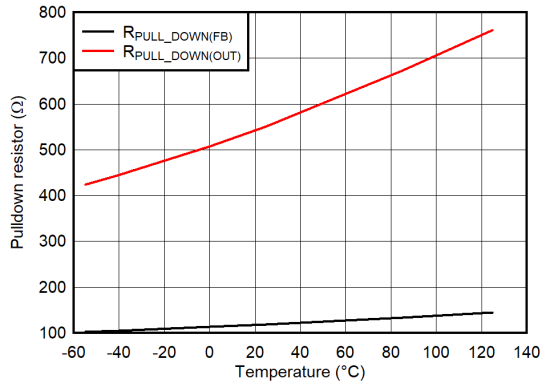
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-46. $UVLO_{BIAS}$ Voltage Threshold vs Temperature



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 5 V, 1.1 V ≤ V_{EN} ≤ 6 V

Figure 6-47. $UVLO_{BIAS}$ Voltage Hysteresis vs Temperature

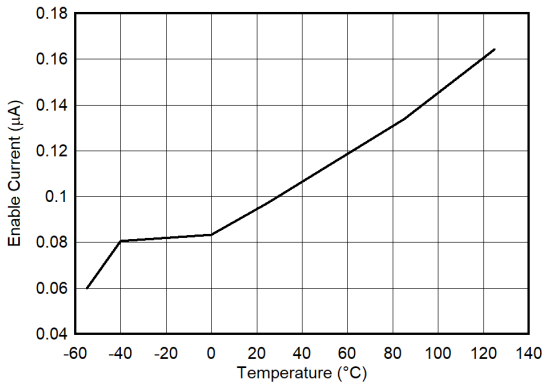


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{BIAS} = 6 V, V_{EN} ≤ 0.4 V

Figure 6-48. Pulldown Resistors vs Temperature

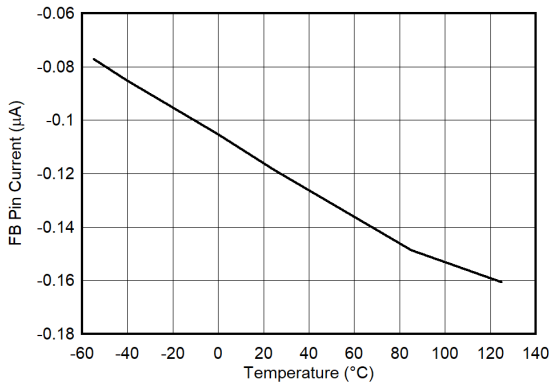
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



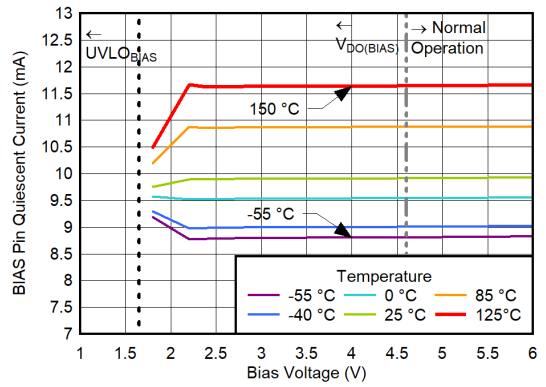
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 6 V, $V_{OUT(NOM)}$ = 0.65 V, V_{BIAS} = 6 V, I_{OUT} = 2 mA, V_{EN} = 6 V

Figure 6-49. EN Pin Current vs Temperature



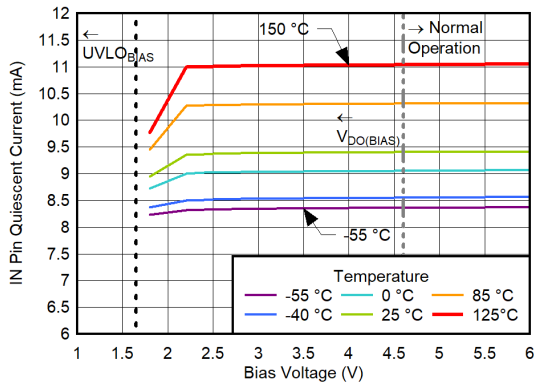
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, 0.95 V ≤ V_{IN} ≤ 6 V, $V_{OUT(NOM)}$ = 0.65 V, V_{BIAS} = 6 V, I_{OUT} = 2 mA, V_{EN} = 6 V

Figure 6-50. FB Pin Current vs Temperature



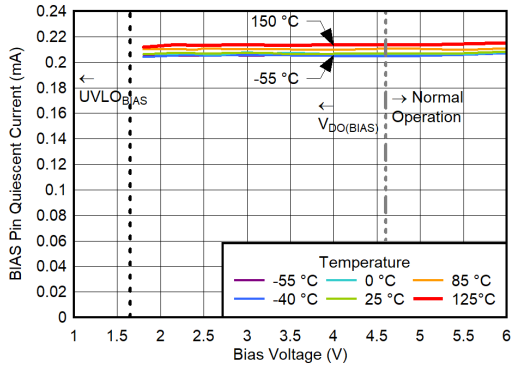
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-51. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 1.5 A



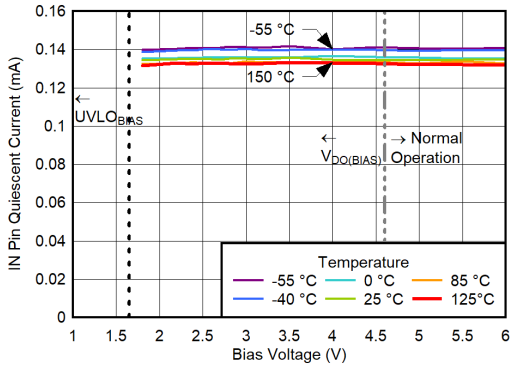
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-52. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 1.5 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-53. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 10 mA

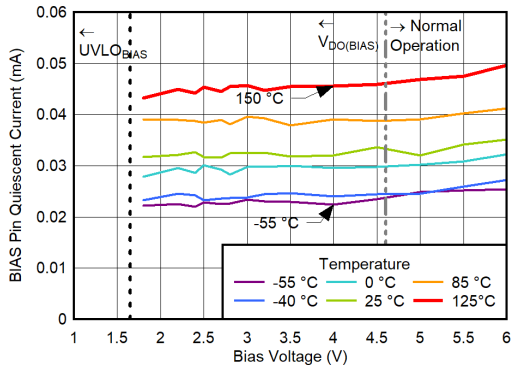


C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-54. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 10 mA

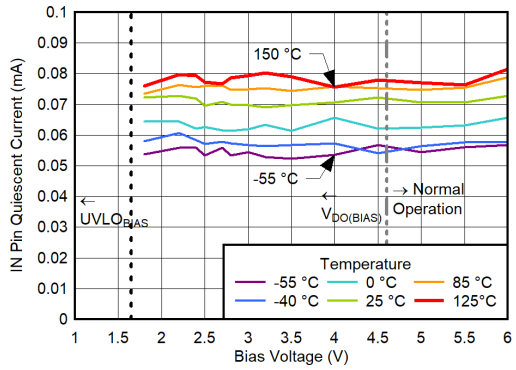
6.6 Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{BIAS} = 1 µF, and C_{OUT} = 10 µF (unless otherwise noted)



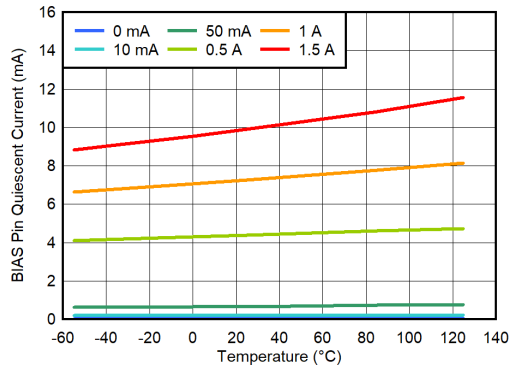
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-55. BIAS Pin Quiescent Current vs Bias Voltage for I_{OUT} = 0 A



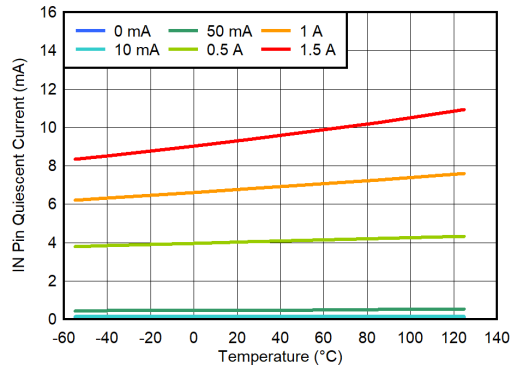
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{EN} = 1.1 V

Figure 6-56. IN Pin Quiescent Current vs Bias Voltage for I_{OUT} = 0 A



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-57. BIAS Pin Quiescent Current vs Temperature



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, C_{SS} = 0 nF, V_{IN} = 3.6 V, V_{OUT} = 3.3 V, V_{BIAS} = 5 V, V_{EN} = 1.1 V

Figure 6-58. IN Pin Quiescent Current vs Temperature

7 Detailed Description

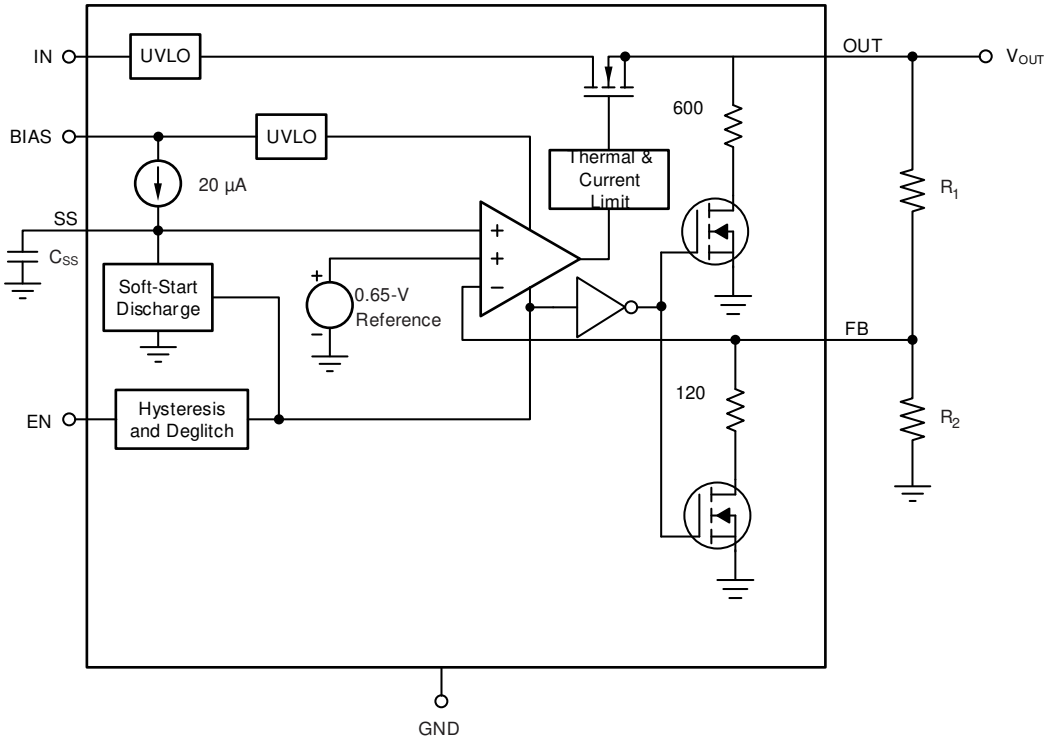
7.1 Overview

The TPS7A74 is a low-input, low-output, low-quiescent-current linear regulator optimized to support excellent transient performance. This regulator uses a low-current bias rail to power all internal control circuitry, allowing the n-type field effect transistor (NMOS) pass transistor to regulate very-low input and output voltages.

Using an NMOS-pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS7A74 to be stable with any ceramic capacitor 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS7A74 features a programmable voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4 V turns the regulator off, and setting V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.75 V and varies with temperature and process variations, see Figure 6-42. Temperature variation is approximately –1.2 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used.

If not used, EN can be connected to BIAS. Place the connection as close as possible to the bias capacitor.

7.3.2 Active Discharge

The TPS7A74 has two internal active pulldown circuits: one on the FB pin and one on the OUT pin.

Each active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled in order to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The first active pulldown circuit connects the output to GND through a 600-Ω resistor when the device is disabled.

The second circuit connects FB to GND through a 120-Ω resistor when the device is disabled. This resistor discharges the FB pin. Equation 1 calculates the output capacitor discharge time constant when OUT is shorted to FB, or when the output voltage is set to 0.65 V.

$$\tau_{OUT} = (600 \,||\, 120 \times R_L / (600 \,||\, 120 + R_L) \times C_{OUT} \quad (1)$$

If the LDO is set to an output voltage greater than 0.65 V, a resistor divider network is in place and minimizes the FB pin pulldown. Equation 2 and Equation 3 calculate the time constants set by these discharge resistors.

$$R_{DISCHARGE} = (120 \,||\, R_2) + R_1 \quad (2)$$

$$\tau_{OUT} = R_{DISCHARGE} \times R_L / (R_{DISCHARGE} + R_L) \times C_{OUT} \quad (3)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input and can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

See Figure 6-48 for additional information.

7.3.3 Global Undervoltage Lockout (UVLO) Circuit

Two undervoltage lockout (UVLO) circuits are present to prevent the TPS7A74 from turning on with an insufficient rail. One circuit is present on the BIAS pin and the other circuit is on the IN pin. The two UVLO signals are connected internally through an AND gate, as shown in Figure 7-1, that turns off the device when the voltage on either input is below their respective UVLO thresholds.

In other words, the output is disabled until the IN pin voltage reaches a value greater than $UVLO_{IN}$ and the BIAS pin voltage reaches a voltage greater than $UVLO_{BIAS}$.

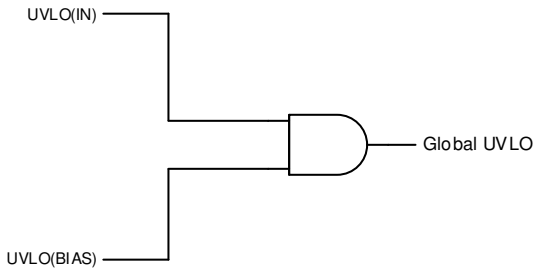


Figure 7-1. Global UVLO Circuit

7.3.4 Internal Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note. Figure 7-2 illustrates a diagram of the foldback current limit.

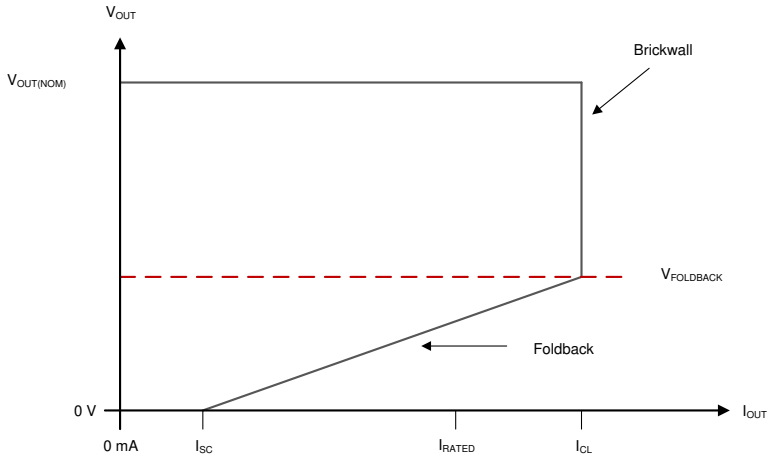


Figure 7-2. Foldback Current Limit

7.3.5 Thermal Shutdown Protection (T_{SD})

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T_J) of the pass transistor rises to the thermal shutdown temperature threshold, $T_{SD(shutdown)\ (typical)}$. The thermal shutdown circuit hysteresis ensures that the LDO resets (turns on) when the temperature falls to $T_{SD(reset)\ (typical)}$.

The thermal time constant of the semiconductor die is fairly short; thus, the device may cycle on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When operating in dropout, the ground current may increase. For dropout operation and its effect on the IN and BIAS current, see Figure 6-51 to Figure 6-56.

When the device is in a steady dropout state, defined as when the device is in dropout, ($V_{IN} < V_{OUT} + V_{DO}$ or $V_{BIAS} < V_{OUT} + V_{DO}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

7.5 Programming

7.5.1 Programmable Soft-Start

The TPS7A74 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because the soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). Equation 4 calculates the soft-start ramp time.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \tag{4}$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. The start-up time is given by Equation 5 in this case.

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \tag{5}$$

where:

- $V_{OUT(nom)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(min)}$ is the minimum current limit for the device

In applications where monotonic start up is required, the soft-start time given by Equation 4 must be set greater than Equation 5.

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF can be a problem in applications where the enable pin must be rapidly pulsed and the device must soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Table 7-2 lists suggested soft-start capacitor values.

Table 7-2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
1 nF	0.032 ms
5.6 nF	0.182 ms
10 nF	0.325 ms

(1) $t_{SS}(s) = \frac{V_{REF} \cdot C_{SS}}{I_{SS}} = \frac{0.65V \cdot C_{SS}(F)}{20\mu A}$, where $t_{SS}(s)$ = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor; see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note for more information.

7.5.2 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage
- If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}
- If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}
- If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor

Figure 7-3 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

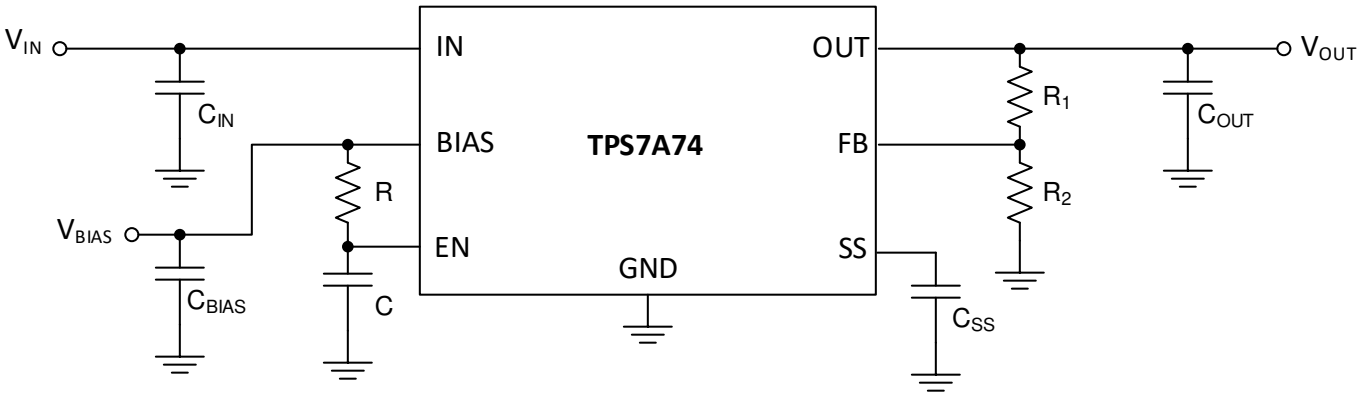


Figure 7-3. Soft-Start Delay Using an RC Circuit to Enable the Device

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A74 is a low-input, low-output (LILO) low-dropout regulator (LDO) that feature soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Adjusting the Output Voltage

Figure 8-1 shows the typical application circuit for the adjustable output device.

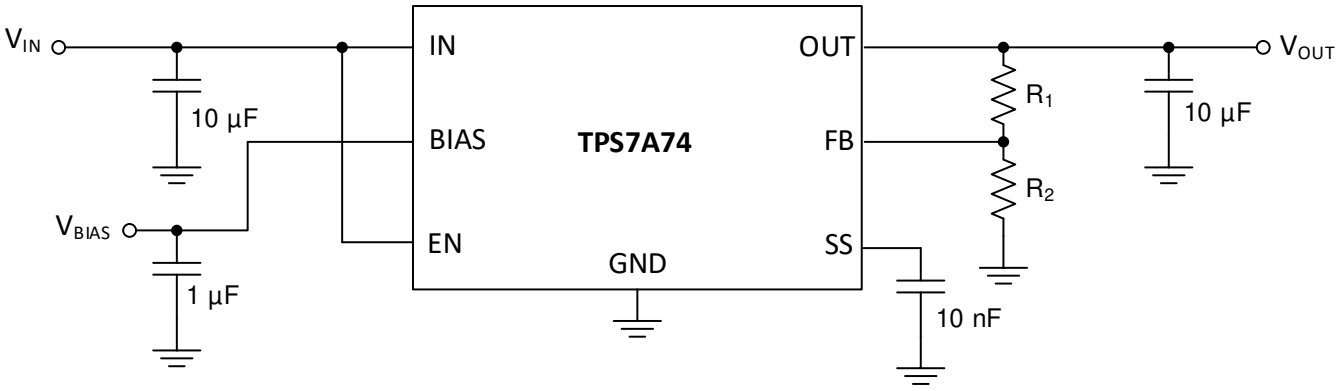


Figure 8-1. Typical Application Circuit for the TPS7A74 (Adjustable)

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 8-1. Table 8-1 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 must be ≤ 4.99 kΩ.

Table 8-1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	Targeted V_{OUT} (V)
Short	Open	0.65
0.768	4.99	0.75
2.43	4.53	1.00
2.72	4.42	1.05
3.48	4.99	1.10
4.22	4.99	1.20
4.99	3.83	1.50
4.99	2.80	1.80
4.99	1.74	2.51
4.99	1.21	3.33

(1) $V_{OUT} = 0.65 \times (1 + R_1 / R_2)$.

Note

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

Because this LDO has a relatively low quiescent current of 50 µA, some applications may benefit from using larger R_1 and R_2 resistor values. In such cases where resistor values greater than 5 kΩ are considered, adding a C_{ff} capacitor across R_1 may help improve stability.

8.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitor of values ≥ 10 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 µF and the minimum recommended capacitor for V_{BIAS} is 0.1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR and ESL capacitors improve high-frequency PSRR.

8.1.3 Transient Response

The TPS7A74 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see Figure 6-10 in the *Typical Characteristics* section. Because the TPS7A74 is stable with output capacitors as low as 10 µF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

8.1.4 Dropout Voltage

The TPS7A74 offers very low dropout performance, making the device well-suited for high-current, low V_{IN} and low V_{OUT} applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. Equation 6 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{6}$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

For this architecture, there are two different specifications for dropout voltage. The first specification (see Figure 8-2) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.8 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} + 2.8 V, the V_{IN} dropout is less than specified.

Note

2.8 V is a test condition of this device and can be adjusted by referring to the *Electrical Characteristics* table.

The second specification (illustrated in Figure 8-2) is referred to as *V_{BIAS} dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.3 V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

8.1.5 Output Noise

The TPS7A74 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF, soft-start capacitor, the output noise is reduced by half and is typically 7.1 μV_{RMS} for a 0.65-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. Equation 7 gives the RMS noise with a 1-nF, soft-start capacitor:

$$V_N\ (V_{RMS}) = 7.1 \cdot \left(\frac{V_{RMS}}{V}\right) \cdot V_{OUT}(V) \tag{7}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

8.1.6 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

Where P_D is the power dissipation shown by Equation 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

8.2 Typical Application

8.2.1 FPGA I/O Supply at 1.8 V With a Bias Rail

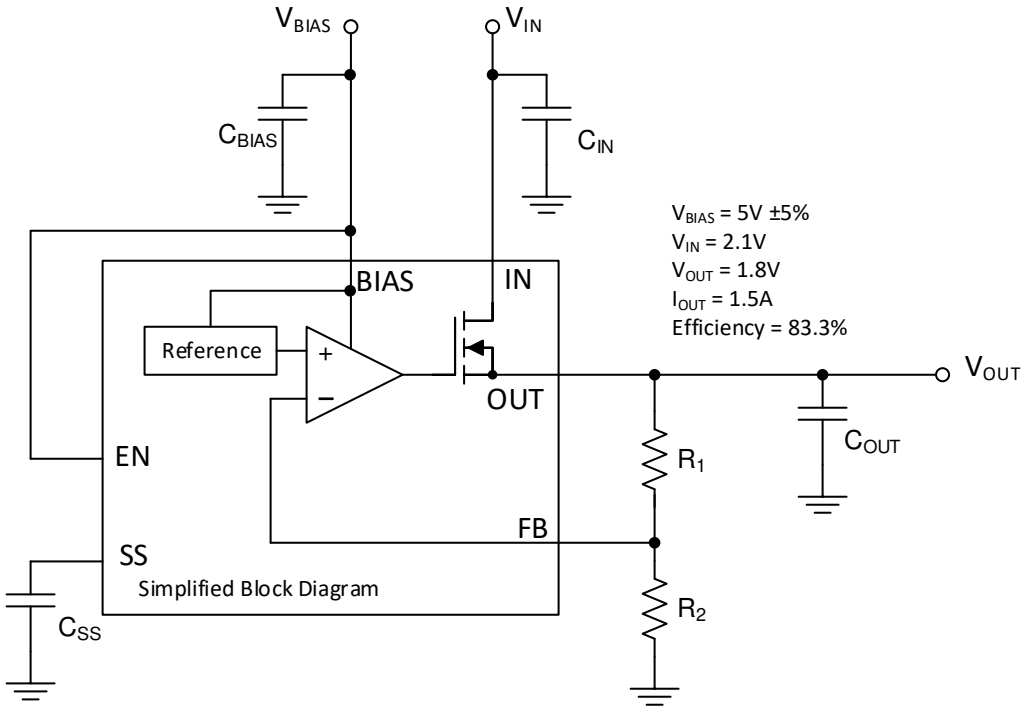


Figure 8-2. Typical Application Using an Auxiliary Bias Rail

8.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA , at $V_{OUT(nom)}$ = 1.8 V and $I_{OUT(dc)}$ = 1.5 A. The available external supply voltages are 2.1 V, 3.3 V, and 5 V.

Table 8-2 lists the parameters for this design example.

Table 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	2.1 V
V_{BIAS}	2.4 V to 5.5 V
V_{OUT}	1.8 V
I_{OUT}	600 mA (typical), 900 mA (peak)

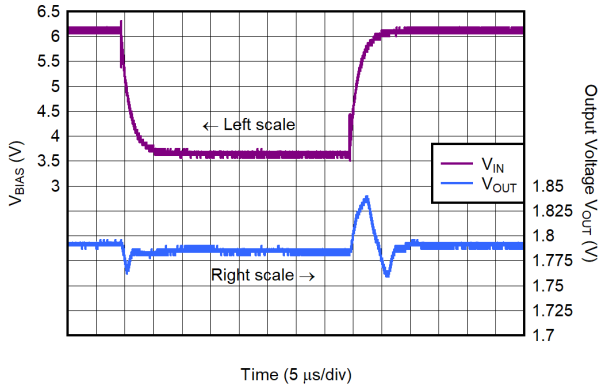
8.2.1.2 Detailed Design Procedure

First, determine what supplies to use for the input and bias rails. A 2.1-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 180 mV if V_{BIAS} is at least 2.8 V higher than V_{OUT}. To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in Equation 6 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As Table 8-1 describes, set R_1 = 4.99 kΩ and R_2 = 3.82 kΩ to obtain the required output voltage. The minimum capacitor sizing requires the total solution size footprint to be reduced; see the *Input, Output, and Bias Capacitor Requirements* section for C_{IN} = 1 µF, C_{BIAS} = 1 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 0.032-ms start-up time.

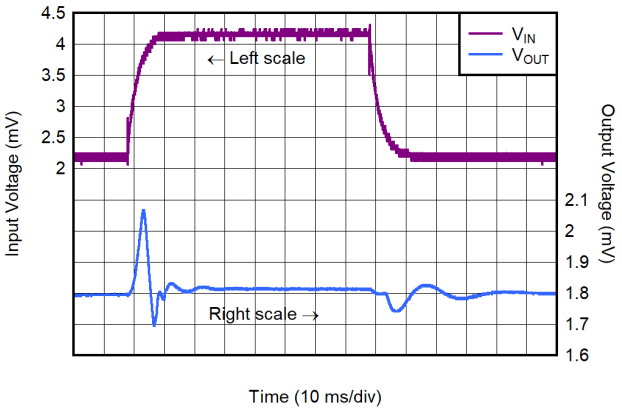
Figure 8-2 shows a simplified version of the final circuit.

8.2.1.3 Application Curves



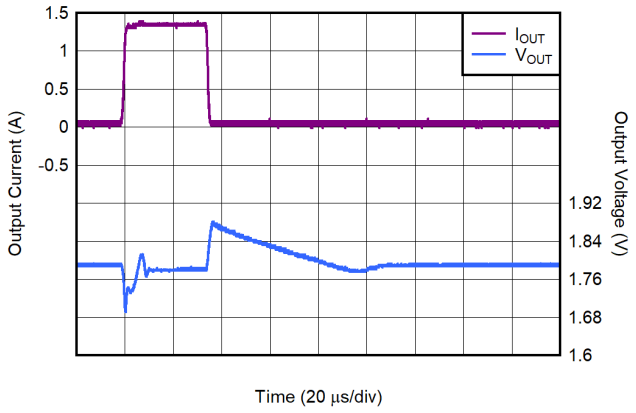
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{IN} = 2.1 V, V_{BIAS} = 6 V to 3.5 V to 6 V, I_{OUT} = 1.5 A

Figure 8-3. V_{BIAS} Line Transient



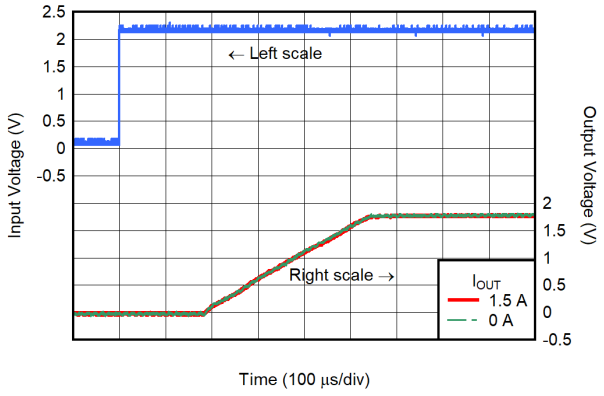
C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V to 4.1 V to 2.1 V, I_{OUT} = 1.5 A

Figure 8-4. V_{IN} Line Transient



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V, I_{OUT} = 10 mA to 1.5 A to 10 mA

Figure 8-5. Output Load Transient Response



C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{BIAS} = 5 V, V_{IN} = 2.1 V, I_{OUT} = 0 mA

Figure 8-6. Turn-On Response

8.3 Power Supply Recommendations

The TPS7A74 is designed to operate from an input voltage up to 6.0 V, provided the bias rail is at least 1.3 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1 µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7-µF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

8.4 Layout

8.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy,

the top side of R_1 in Figure 8-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation (P_D) of the device depends on input voltage and load conditions. Equation 9 calculates P_D.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{9}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DSD) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, this pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Equation 10 calculates the maximum junction-to-ambient thermal resistance.

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{10}$$

Note

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

8.4.1.1 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 11). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{11}$$

Where P_D is the power dissipation shown by Equation 9, T_T is the temperature at the center-top of the package, and T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*.

Note

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

8.4.2 Layout Example

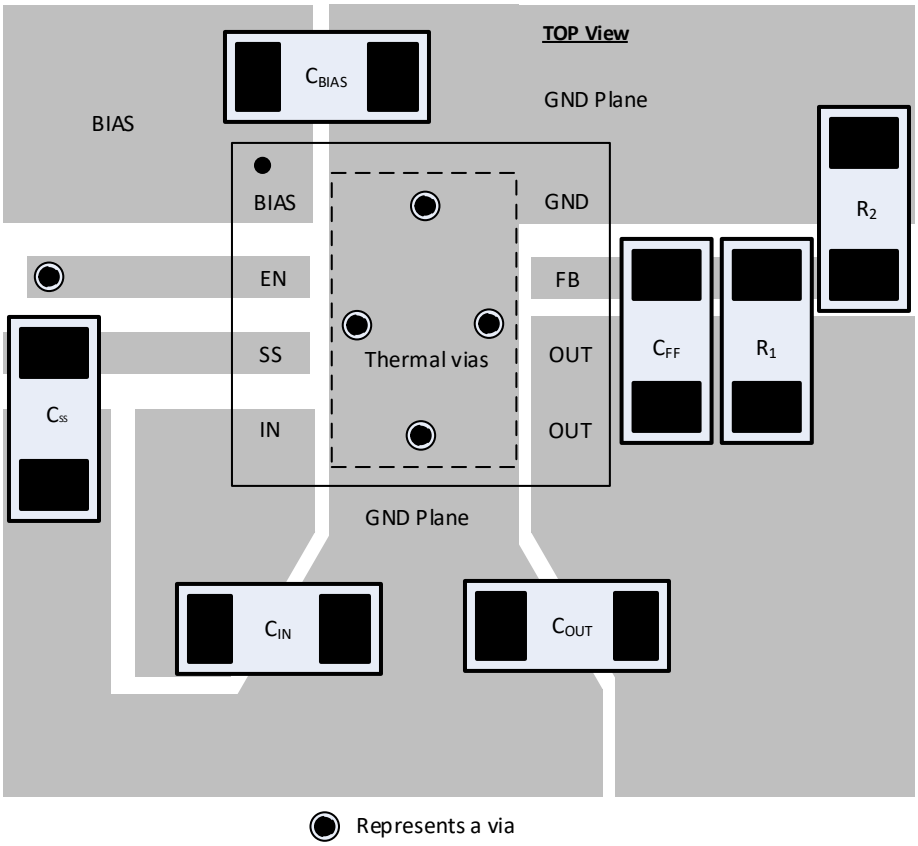


Figure 8-7. Example Layout (DSD Package)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A74. The evaluation module(and related user guide user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A74 is available through the product folders under *Tools & Software*.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Ultimate Regulation with Fixed Output Versions of TPS742xx, TPS743xx, and TPS744xx* application note
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *TPS74701EVM-177 and TPS74801EVM-177* user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A7401DSDR	ACTIVE	SON	DSD	8	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

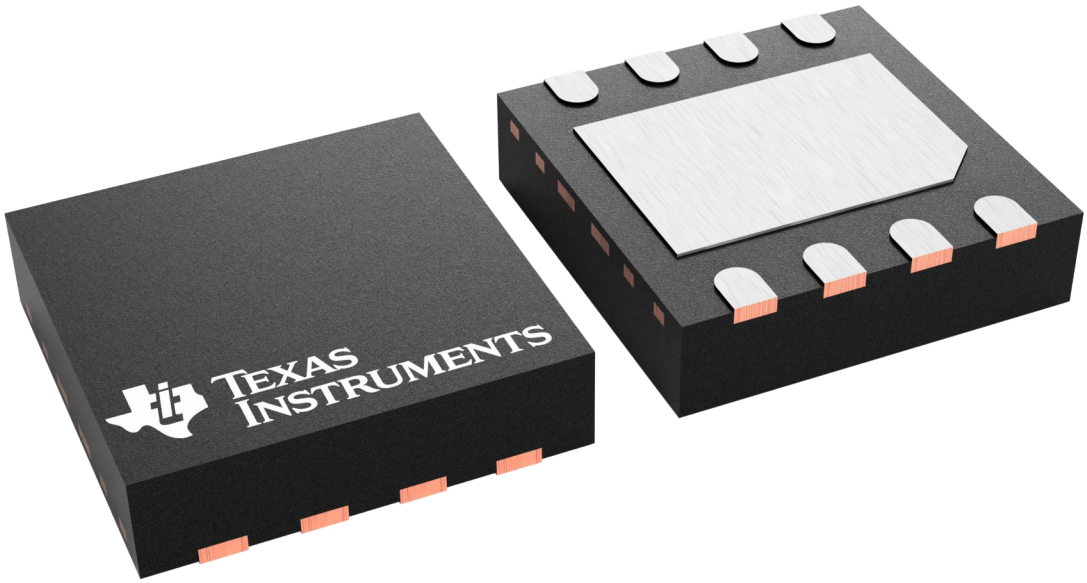
DSD 8

WSON - 0.8 mm max height

3 X 3, 0.8 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227007/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS7H5001-SP, TPS7H5002-SP, TPS7H5003-SP, TPS7H5004-SP
SLVSF07A – JULY 2021 – REVISED FEBRUARY 2022

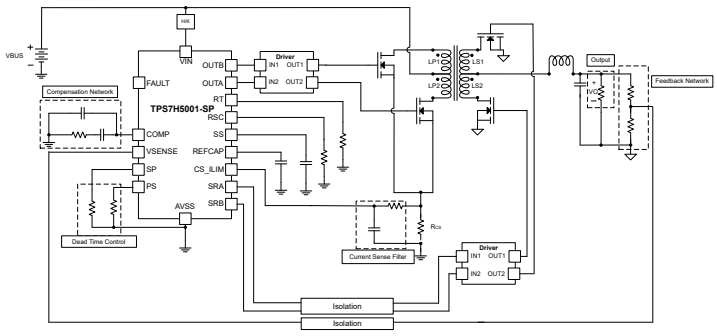
TPS7H500x-SP Radiation-Hardness-Assured 2-MHz Current Mode PWM Controllers

1 Features

- Radiation performance:
  - Radiation hardness assured (RHA) up to TID 100 krad(Si)
  - SEL, SEB, and SEGR immune to LET = 75 MeV-cm^2/mg
  - SET and SEFI characterized up to LET = 75 MeV-cm^2/mg
  - No cross-conduction events for controller outputs observed during SET characterization
- Input voltage: 4 V to 14 V
- 0.613-V ±1% voltage reference over temperature, radiation, and line and load regulation
- Switching frequency from 100 kHz to 2 MHz
- External clock synchronization capability
- Synchronous rectification outputs
  - TPS7H5001-SP, TPS7H5002-SP, TPS7H5003-SP
- Adjustable dead time
  - TPS7H5001-SP, TPS7H5002-SP
- Adjustable leading edge blank time
  - TPS7H5001-SP, TPS7H5002-SP, TPS7H5004-SP
- Configurable duty cycle limit
  - TPS7H5001-SP, TPS7H5002-SP, TPS7H5003-SP
- Adjustable slope compensation and soft start
- Thermally-enhanced CFP package

2 Applications

- Space satellite point of load supply for FPGAs, microcontrollers, data converters, and ASICs
- Communications payload
- Command and data handling
- Satellite electrical power system



Typical Application for TPS7H5001-SP

3 Description

The TPS7H500x-SP series (consisting of TPS7H5001-SP, TPS7H5002-SP, TPS7H5003-SP, and TPS7H5004-SP) is a family of high speed radiation-hardness-assured PWM controllers. The controllers provide a number of features that are beneficial for the design of DC-DC converter topologies intended for space applications. The controllers have a 0.613 V ±1 % accurate internal reference and configurable switching frequency up to 2 MHz. Each device offers programmable slope compensation and soft-start.

The TPS7H500x-SP series can be driven using an external clock through the SYNC pin or by using the internal oscillator at a frequency programmed by the user. The controller family offers the user various options for switching outputs, synchronous rectification capability, dead time (fixed or configurable), leading edge blank time (fixed or configurable), and duty cycle limit. Each device in the TPS7H500x-SP series has a 22-pin CFP package.

Table 3-1. Device Information

PART NUMBER(1)	GRADE(2)	PACKAGE
5962R1822201VXC	Flight grade QMLV-RHA 100 krad(Si)	CFP (22) 6.21 mm × 7.69 mm Mass = 415.6 mg(4)
5962R1822202VXC		
5962R1822203VXC		
5962R1822204VXC		
TPS7H5001HFT/EM	Engineering samples(3)	
TPS7H5002HFT/EM		
TPS7H5003HFT/EM		
TPS7H5004HFT/EM		
5962R1822201V9A	Flight grade QMLV-RHA KGD 100 krad(Si)	Die
TPS7H5001Y/EM	Engineering samples(3)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For additional information about part grade, view SLYB235.
(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.
(4) Mass is accurate to ±10%.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (February 2022)	Page
• Changed TPS7H5001-SP device status from *Advance Information* to *Production Data*	1

5 Device Comparison Table

Table 5-1. TPS7H500x-SP Device Comparison

DEVICE	PRIMARY OUTPUTS	SYNCHRONOUS RECTIFIER OUTPUTS	DEAD-TIME SETTING	LEADING EDGE BLANK TIME SETTING	DUTY CYCLE LIMIT OPTIONS
TPS7H5001-SP	2	2	Resistor programmable	Resistor programmable	50%, 75%, 100%
TPS7H5002-SP	1	1	Resistor programmable	Resistor programmable	75%, 100%
TPS7H5003-SP	1	1	Fixed (50-ns typical)	Fixed (50-ns typical)	75%, 100%
TPS7H5004-SP	2	0	Not applicable	Resistor programmable	50%

6 Pin Configuration and Functions

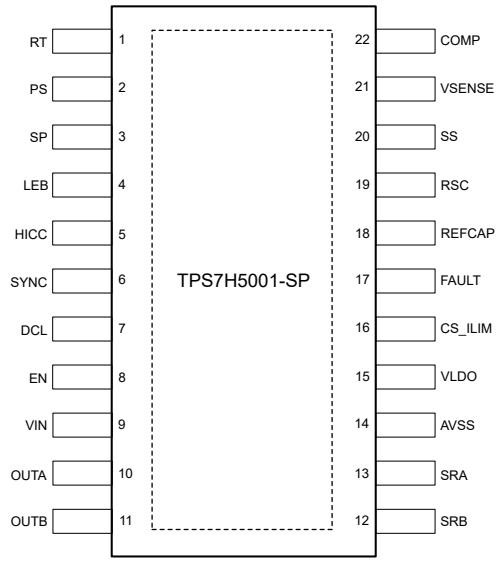


Figure 6-1. TPS7H5001-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

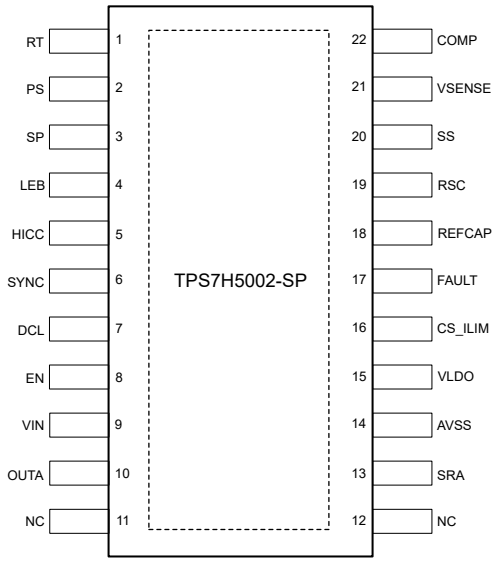


Figure 6-2. TPS7H5002-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

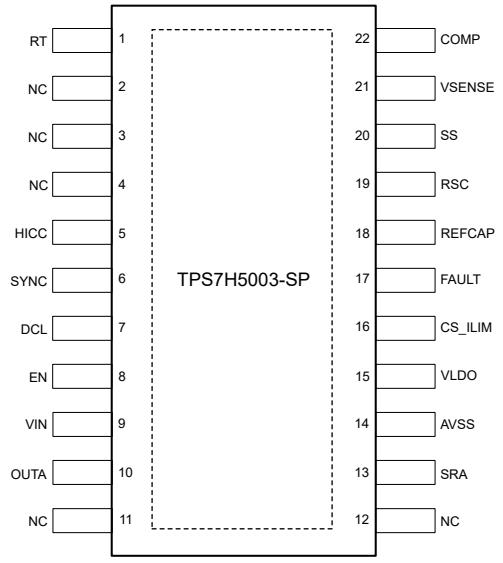


Figure 6-3. TPS7H5003-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

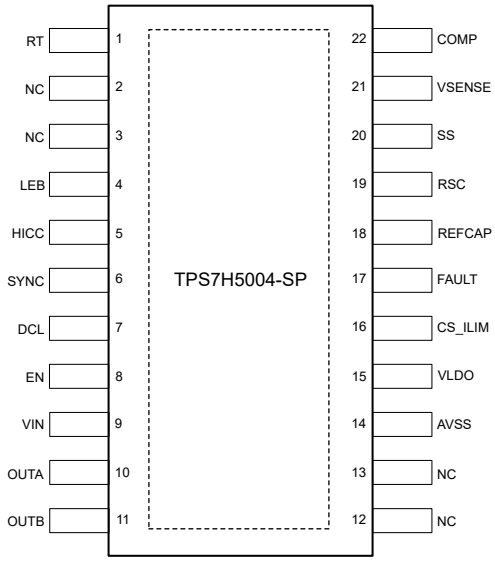


Figure 6-4. TPS7H5004-SP HFT Package 22-Pin CFP With Thermal Pad (Top View)

Table 6-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS7H5001-SP	TPS7H5002-SP	TPS7H5003-SP	TPS7H5004-SP		
RT	1	1	1	1	I/O	In internal oscillation mode, the RT pin must be populated with a resistor to AVSS. When the RT pin is floating, a 200-kHz to 4-MHz external clock is required at the SYNC pin. The frequency of the external clock must be twice the desired switching frequency.
PS	2	2	—	—	I/O	Primary off to synchronous rectifier on dead-time set. Programmable through an external resistor to AVSS.
SP	3	3	—	—	I/O	Synchronous rectifier off to primary on dead-time set. Programmable through an external resistor to AVSS.
LEB	4	4	—	4	I/O	Leading edge blank time set. Programmable through an external resistor to AVSS.
HICC	5	5	5	5	I/O	Cycle-by-cycle current limit time delay and hiccup time setting. Delay time and hiccup time determined by capacitor from HICC to AVSS. Connecting this pin to AVSS disables hiccup mode.
SYNC	6	6	6	6	I/O	When the RT pin is floating, SYNC is configured as an input for a 200-kHz to 4-MHz external clock. In this case, the external clock input gets inverted and the system clock will run at half the frequency of the external clock input. When the RT pin is populated with a resistor to AVSS, SYNC outputs a 200-kHz to 4-MHz clock signal at twice the device switching frequency in phase with the switching of the device.
DCL	7	7	7	7	I/O	Duty cycle limit configurability. For TPS7H5001-SP, connect to AVSS for 50% duty cycle limit, floating for 75%, and VLDO for 100%. For TPS7H5002-SP and TPS7H5003-SP, the DCL pin can be left floating or connected to VLDO to set the maximum duty cycle to 75% or 100%, respectively. For TPS7H5004-SP, this pin must be connected to AVSS in order to obtain the 50% maximum duty cycle.
EN	8	8	8	8	I	Connecting the EN pin to the VLDO pin or external source greater than 0.6 V enables the device. In addition, input undervoltage lockout (UVLO) can be adjusted with two resistors.
VIN	9	9	9	9	I	Input supply to the device. Input voltage range is from 4 V to 14 V.
OUTA	10	10	10	10	O	Primary switching output A.
OUTB	11	—	—	11	O	Primary switching output B. Active only when DCL = AVSS.
SRB	12	—	—	—	O	Synchronous rectifier output B. Active only when DCL = AVSS.
SRA	13	13	13	—	O	Synchronous rectifier output A.

Table 6-1. Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	TPS7H5001-SP	TPS7H5002-SP	TPS7H5003-SP	TPS7H5004-SP		
AVSS	14	14	14	14	—	Ground of the device. The thermal pad, lid, and seal ring of the device are internally connected to ground.
VLDO	15	15	15	15	O	Output of internal regulator. Requires at least 1-µF external capacitor to AVSS.
CS_ILIM	16	16	16	16	I/O	Current sense for PWM control and cycle-by-cycle overcurrent protection. An input voltage over 1.05 V on CS_ILIM will trigger an overcurrent in the PWM controller.
FAULT	17	17	17	17	I	Fault protection pin. When the rising threshold of the FAULT pin is exceeded, the outputs will stop switching. After the external voltage drops below the falling threshold, the device will restart after a set delay. Connect this pin to AVSS to disable FAULT.
REFCAP	18	18	18	18	O	1.2-V internal reference. Requires a 470-nF external capacitor to AVSS.
RSC	19	19	19	19	I/O	A resistor from RSC to AVSS sets the desired slope compensation.
SS	20	20	20	20	I/O	Soft start. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
VSENSE	21	21	21	21	I	Inverting input of the error amplifier.
COMP	22	22	22	22	I/O	Error amplifier output. Connect frequency compensation to this pin.
NC	N/A	11, 12	2, 3, 4, 11, 12	2, 3, 12, 13	—	No connect.

Table 6-2. TPS7H5001-SP Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	GND	Al (0.5% Cu)	3000 nm

Figure 6-5. TPS7H5001-SP Bare Die Diagram

Table 6-3. TPS7H5001-SP Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
RT	1	21.33	3775.77	111.33	3865.77
PS	2	21.33	3392.37	111.33	3482.37
SP	3	21.33	3233.115	111.33	3323.115
LEB	4	21.33	2955.015	111.33	3045.015
HICC	5	21.33	2695.905	111.33	2785.905
SYNC	6	32.13	2427.705	122.13	2517.705
DCL	7	32.13	2149.515	122.13	2239.515
NC	8	32.175	1923.165	122.175	2013.165
EN	9	32.13	1660.275	122.13	1750.275
VIN	10	28.665	1432.53	118.665	1522.53
VIN	11	28.665	1325.475	118.665	1415.475
OUTA	12	32.13	586.755	122.13	676.755
OUTB	13	32.13	433.35	122.13	523.35
SRB	14	2224.62	132.93	2314.62	222.93
SRA	15	2224.62	586.755	2314.62	676.755
AVSS	16	2235.42	1053.315	2325.42	1143.315
AVSS	17	2235.42	1221.435	2325.42	1311.435
AVSS	18	2235.42	1330.425	2325.42	1420.425
VLDO	19	2224.62	1803.51	2314.62	1893.51
VLDO	20	2224.62	1912.545	2314.62	2002.545
VLDO	21	2224.62	2021.58	2314.62	2111.58
CS_ILM	22	2224.62	2274.3	2314.62	2364.3
FAULT	23	2224.62	2513.16	2314.62	2603.16
REFCAP	24	2235.42	2766.285	2325.42	2856.285
RSC	25	2235.42	3033.36	2325.42	3123.36
SS	26	2235.42	3296.655	2325.42	3386.655
VSENSE	27	2235.42	3563.64	2325.42	3653.64
COMP	28	2235.42	3905.55	2325.42	3995.55

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input	VIN	–0.3	16	V
	RT, VSENSE, SS, RSC, COMP, PS, SP, HICC, LEB	–0.3	3.3	
	SYNC	–0.3	7.5	
	EN, FAULT	–0.3	7.5	
	DCL, CS_ILIM	–0.3	7.5	
Output	OUTA, OUTB, SRA and SRB	–0.3	7.5	V
	VLDO	–0.3	7.5	
	REFCAP	–0.3	3.3	
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage	4		14	V
SR_{VIN}	Input voltage slew rate			0.03	V/µs
T_J	Junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TP7H500x-SP CFP 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (top) thermal resistance	16.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: All Devices

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS						
VIN	Operating input voltage		4		14	V
IDD	Operating supply current	f_{SW} = 500 kHz, No load for OUTA, OUTB, SRA, and SRB		6.25	8	mA
		f_{SW} = 1 MHz, No load for OUTA, OUTB, SRA, and SRB		6.75	9.5	
		f_{SW} = 2 MHz, No load for OUTA, OUTB, SRA, and SRB		8.5	13.5	
		f_{SW} = 500 kHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		7.5	9.5	
		f_{SW} = 1 MHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		9	12	
		f_{SW} = 2 MHz, C_{LOAD} = 100 pF for OUTA, OUTB, SRA, and SRB		14	19.5	
$I_{DD(dis)}$	Standby current	EN = 0 V			3	mA
VLDO	Internal linear regulator output voltage	5 V ≤VIN ≤ 14 V, f_{sw} ≤ 1 MHz	4.75	5	5.2	V
VLDO	Internal linear regulator output voltage	5 V ≤ VIN ≤ 14 V, f_{sw} = 2 MHz	4.65	5	5.2	V
ENABLE AND UNDERVOLTAGE LOCKOUT						
V_{ENR}	EN threshold rising		0.57	0.6	0.65	V
V_{ENF}	EN threshold falling		0.47	0.5	0.55	V
V_{ENH}	EN hysteresis voltage		85	95	105	mV
I_{EN}	EN pin input leakage current	VIN = 14 V, EN = 5 V		5	50	nA
$VLDO_{UVLOR}$	VLDO UVLO rising		3.44	3.55	3.66	V
$VLDO_{UVLOF}$	VLDO UVLO falling		3.29	3.4	3.51	V
$VLDO_{UVLOH}$	VLDO UVLO hysteresis		115	135	160	mV
SOFT START						
I_{SS}	Soft-start current	SS = 0.3 V	1.98	2.7	3.32	µA
ERROR AMPLIFIER						
EA_{gm}	Transconductance	–2 µA < I_{COMP} < 2 µA, $V_{(COMP)}$ = 1 V	1150	1800	2500	µA/V
EA_{DC}	DC gain	V_{SENSE} = 0.6 V		10000		V/V
EA_{ISRC}	Error amplifier source current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	100		190	µA
EA_{ISNK}	Error amplifier sink current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive	100		190	µA
EA_{ro}	Error amplifier output resistance			7		MΩ
EA_{OS}	Error amplifier input offset voltage		–2		2	mV
EA_{IB}	Error amplifier input bias current				35	nA
EA_{BW}	Bandwidth			10		MHz
OSCILLATOR						
$SYNC_{IL}$	SYNC in low-level	VIN < 5 V			0.8	V
		VIN ≥ 5 V			0.8	
$SYNC_{IH}$	SYNC in high-level	VIN < 5 V	3.5			V
		VIN ≥ 5 V	3.5			
F_{SYNC}	SYNC in frequency range		200		4000	kHz
D_{SYNC}	SYNC in duty cycle	Duty cycle of external clock	40		60	%
$SYNC_{RT}$	SYNC out low-to-high rise time (10%/90%)	C_{LOAD} = 25 pF		6	15	ns

7.5 Electrical Characteristics: All Devices (continued)

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$SYNC_{FT}$	SYNC out high-to-low fall time (10%/90%)	C_{LOAD} = 25 pF		6	17	ns
$SYNC_{OL}$	SYNC out low level	I_{OL} = 10 mA			500	mV
VLDO – $SYNC_{OH}$	SYNC out high level (1)	I_{OH} = 10 mA			0.5	V
EXT_{DT}	Externally set frequency detection time	RT = Open, f = 200 kHz			20	µs
FSW_{EXT}	Externally set frequency	RT = 1.07 MΩ	95	105	115	kHz
		RT = 511 kΩ	190	210	230	
		RT = 90.9 kΩ	900	1000	1100	
		RT = 34.8 kΩ	1700	2000	2300	
VOLTAGE REFERENCE						
VREF	Internal voltage reference initial tolerance	Measured at COMP, 25°C	0.609	0.613	0.615	V
	Internal voltage reference	Measured at COMP, –55°C	0.607	0.609	0.612	
		Measured at COMP, 125°C	0.611	0.614	0.617	
REFCAP	REFCAP voltage	REFCAP = 470 nF	1.213	1.225	1.237	V
CURRENT SENSE, CURRENT LIMIT AND HICCUP						
CCSR	COMP to CS_ILIM ratio		2.00	2.06	2.12	
V_{CS_ILIM}	Current limit (overcurrent) threshold			1.05	1.09	V
I_{HICC_DEL}	Hiccup delay current	CS_ILIM = 1.3 V, COMP = 3 V, VSENSE = REFCAP/2 V, C_{HICC} = 3 nF, LEB = 49.9 kΩ, f_{sw} = 100 kHz		80		µA
I_{HICC_RST}	Hiccup restart current			1		µA
V_{HICC_PU}	Hiccup pull-up threshold			1.0		V
V_{HICC_SD}	Hiccup shut-down threshold			0.6		V
V_{HICC_RST}	Hiccup restart threshold			0.3		V
SLOPE COMPENSATION						
	Slope compensation	f_{SW} = 100 kHz, RSC = 1.18 MΩ		0.033		V/µs
		f_{SW} = 200 kHz, RSC = 562 kΩ		0.066		
		f_{SW} = 1000 kHz, RSC = 100 kΩ		0.333		
		f_{SW} = 2000 kHz, RSC = 49.9 kΩ		0.666		
FAULT						
V_{FLTR}	FLT threshold rising		0.57	0.6	0.65	V
V_{FLTF}	FLT threshold falling		0.47	0.5	0.55	V
V_{FLTH}	FLT hysteresis voltage		90	100	110	mV
T_{FLT}	FLT minimum pulse width	V_{FLT} = 1 V	0.4		1.4	µs
t_{DFLT}	FLT delay duration	f_{sw} = 100 kHz	140	152	169	µs
		f_{sw} = 200 kHz	66	78	86	
		f_{sw} = 1 MHz	14	17	21	
		f_{sw} = 2 MHz	7	11	14	
THERMAL SHUTDOWN						
	Thermal shutdown		165	175	185	°C
	Thermal shutdown hysteresis		10	15	20	°C
PRIMARY AND SYNCHRONOUS RECTIFIER OUTPUTS						
	Low-level threshold	I_{SINK} = 10 mA		0.5		V
	High-level threshold	I_{SOURCE} = 10 mA		4.5		V

7.5 Electrical Characteristics: All Devices (continued)

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Rise/fall time	R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF, 10% to 90%		10	17	ns
R_{SRC_P}	Output source resistance	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V		15		Ω
R_{SINK_P}	Output sink resistance	I_{OUT} = 20 mA, 5 V ≤ VIN ≤ 14 V		15		Ω

(1) Bench verified. Not tested in production.

7.6 Electrical Characteristics: TPS7H5001-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V			85	ns
TD_{PS}	Primary off to secondary on dead time	PS = floating, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	5	8	11	ns
		PS = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	43	50	55	
		PS = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	85	100	110	
TD_{SP}	Secondary off to primary on dead time	SP = floating, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	5	8	11	ns
		SP = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	43	50	55	
		SP = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	85	100	110	
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = AVSS	45	48	50	%
		DCL = floating, clock duty cycle = 50%	70	75	80	
		DCL = VLDO			100	

7.7 Electrical Characteristics: TPS7H5002-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V			85	ns
TD_{PS}	Primary off to secondary on dead time	PS = floating, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	5	8	11	ns
		PS = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	43	50	55	
		PS = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	85	100	110	
TD_{SP}	Secondary off to primary on dead time	SP = floating, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	5	8	11	ns
		SP = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	43	50	55	
		SP = 107 kΩ, 5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising, OUTx and SRx floating	85	100	110	
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = floating, clock duty cycle = 50%	70	75	80	%
		DCL = VLDO			100	

7.8 Electrical Characteristics: TPS7H5003-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

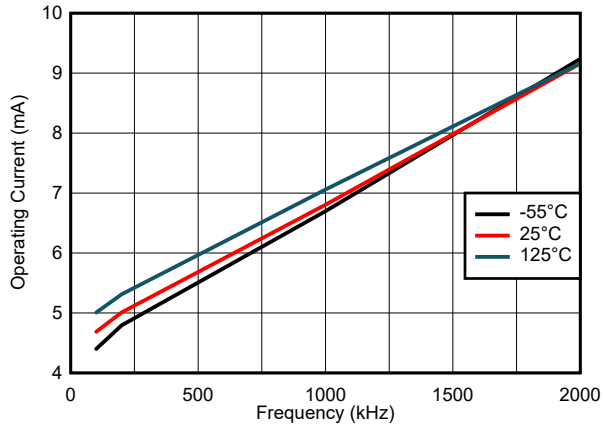
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME AND DEAD TIME						
t_{MIN}	Minimum on-time	5 V ≤ VIN ≤ 14 V			115	ns
TD_{PS}	Primary off to secondary on dead time	5 V ≤ VIN ≤ 14 V, 90% of OUTx falling to 10% of SRx rising, OUTx and SRx floating	40	50	60	ns
TD_{SP}	Secondary off to primary on dead time	5 V ≤ VIN ≤ 14 V, 90% of SRx falling to 10% of OUTx rising edge, OUTx and SRx floating	40	50	60	ns
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	5 V ≤ VIN ≤ 14 V	45	50	55	ns
D_{MAX}	Maximum duty cycle	DCL = floating, clock duty cycle = 50%	70	75	80	%
		DCL = VLDO			100	

7.9 Electrical Characteristics: TPS7H5004-SP

T_J = –55°C to 125°C, VIN = 4 V to 14 V (unless otherwise noted)

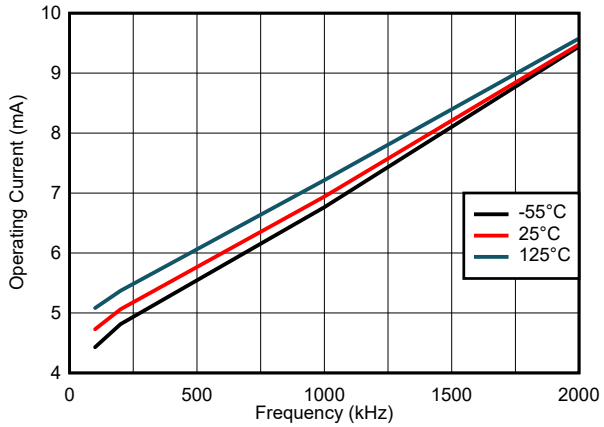
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM ON-TIME						
t_{MIN}	Minimum on-time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V			85	ns
LEADING EDGE BLANK TIME AND DUTY CYCLE						
T_{LEB}	Leading edge blank time	LEB = 10 kΩ, 5 V ≤ VIN ≤ 14 V	12	15	19	ns
		LEB = 49.9 kΩ, 5 V ≤ VIN ≤ 14 V	45	50	55	
		LEB = 110 kΩ, 5 V ≤ VIN ≤ 14 V	85	100	110	
D_{MAX}	Maximum duty cycle	DCL = AVSS	45	48	50	%

7.10 Typical Characteristics



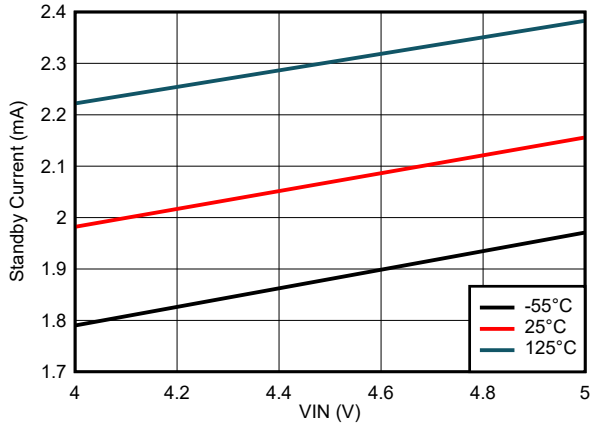
VIN = 5 V

Figure 7-1. Operating Current Variation



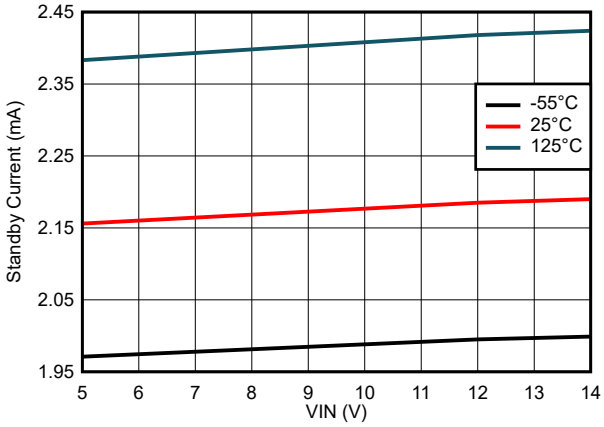
VIN = 12 V

Figure 7-2. Operating Current Variation



VIN = 4 V to 5 V

Figure 7-3. Standby Current Variation



VIN = 5 V to 14 V

Figure 7-4. Standby Current Variation

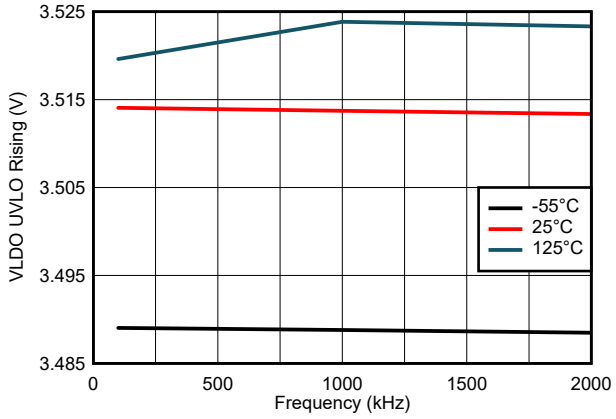


Figure 7-5. VLDO UVLO Rising Variation

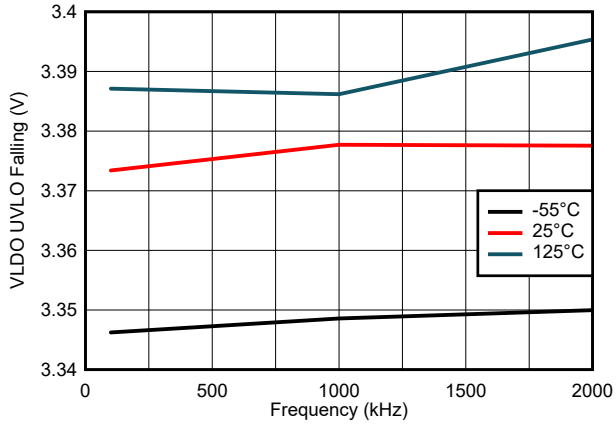


Figure 7-6. VLDO UVLO Falling Variation

7.10 Typical Characteristics (continued)

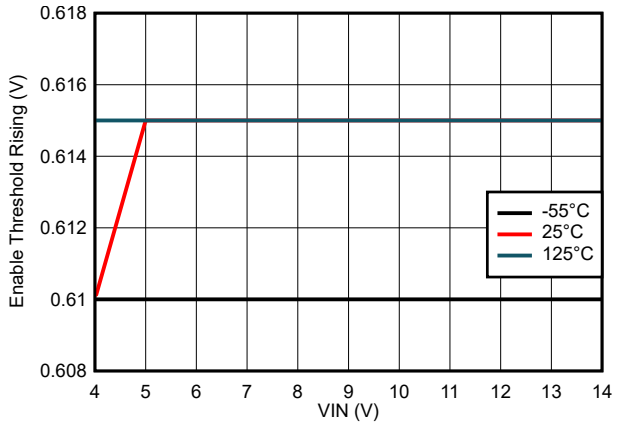


Figure 7-7. Enable Threshold Rising Variation

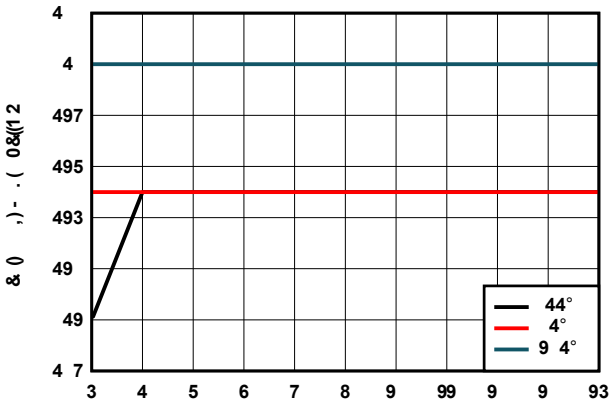
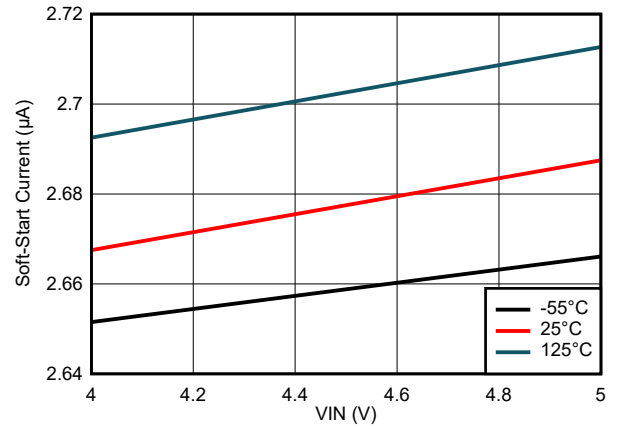
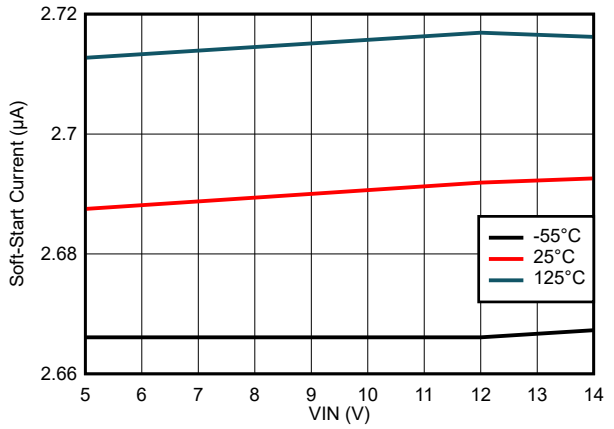


Figure 7-8. Enable Threshold Falling Variation



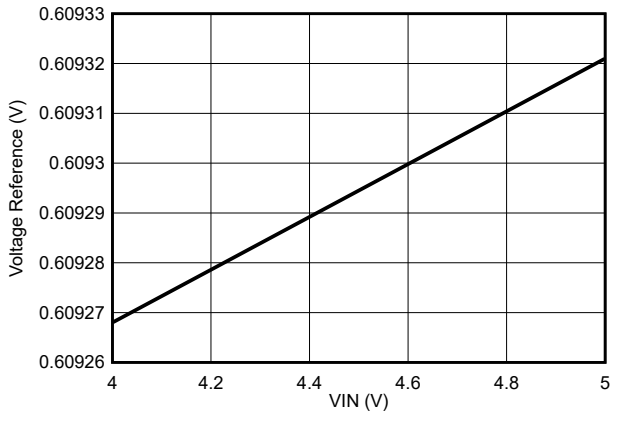
VIN = 4 V to 5 V

Figure 7-9. Soft-Start Current Variation



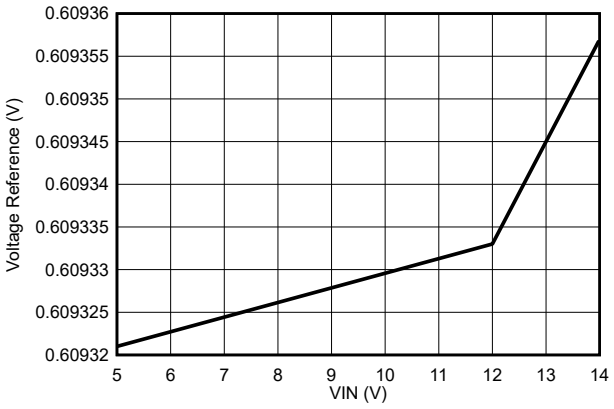
VIN = 5 V to 14 V

Figure 7-10. Soft-Start Current Variation



VIN = 4 V to 5 V
Temp. = –55°C

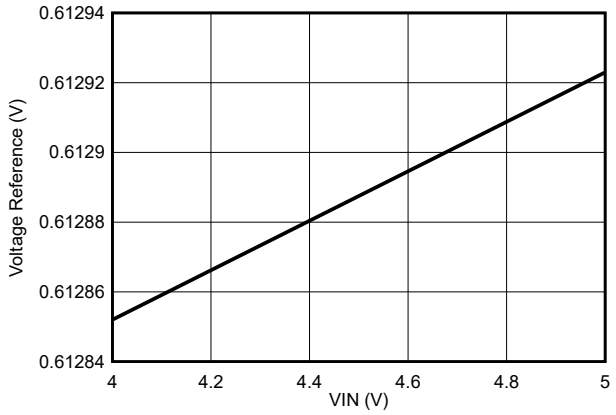
Figure 7-11. Voltage Reference Variation



VIN = 5 V to 14 V
Temp. = –55°C

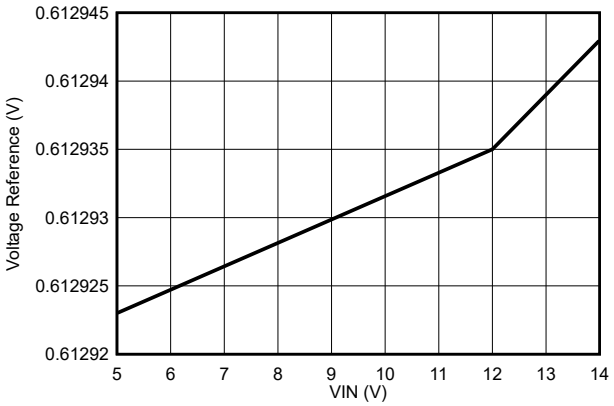
Figure 7-12. Voltage Reference Variation

7.10 Typical Characteristics (continued)



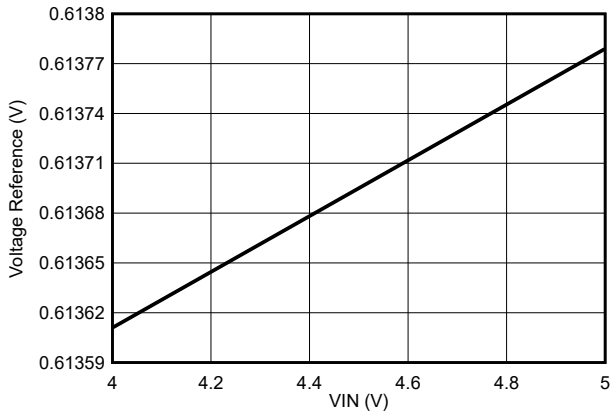
VIN = 4 V to 5 V
Temp. = 25°C

Figure 7-13. Voltage Reference Variation



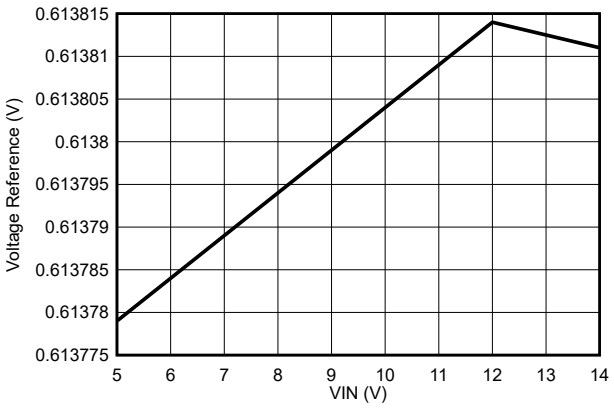
VIN = 5 V to 14 V
Temp. = 25°C

Figure 7-14. Voltage Reference Variation



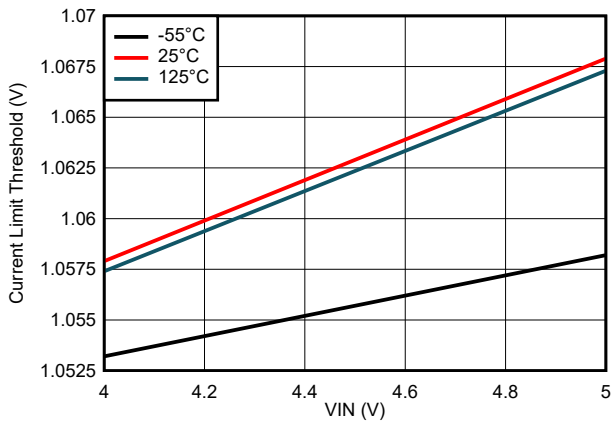
VIN = 4 V to 5 V
Temp. = 125°C

Figure 7-15. Voltage Reference Variation



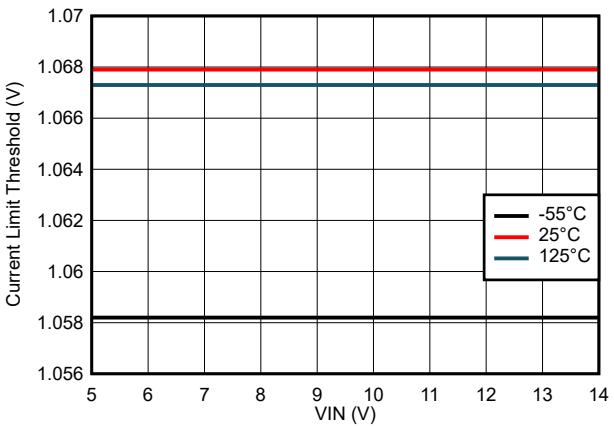
VIN = 5 V to 14 V
Temp. = 125°C

Figure 7-16. Voltage Reference Variation



VIN = 4 V to 5 V

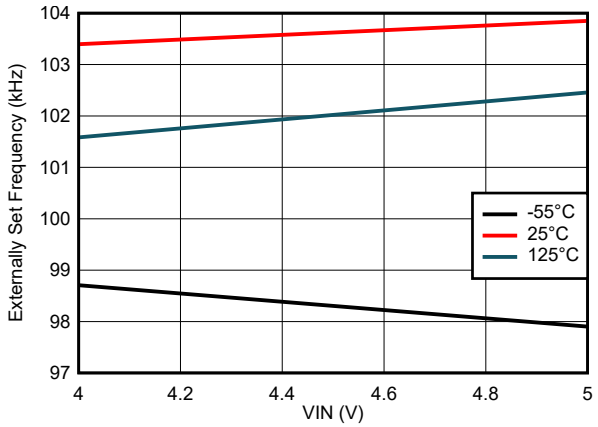
Figure 7-17. Current Limit Threshold Variation



VIN = 5 V to 14 V

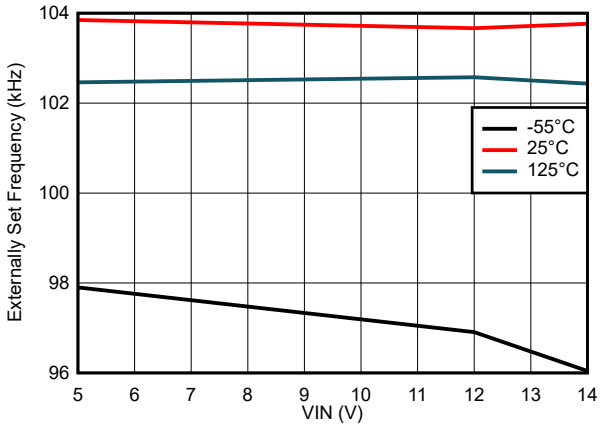
Figure 7-18. Current Limit Theshold Variation

7.10 Typical Characteristics (continued)



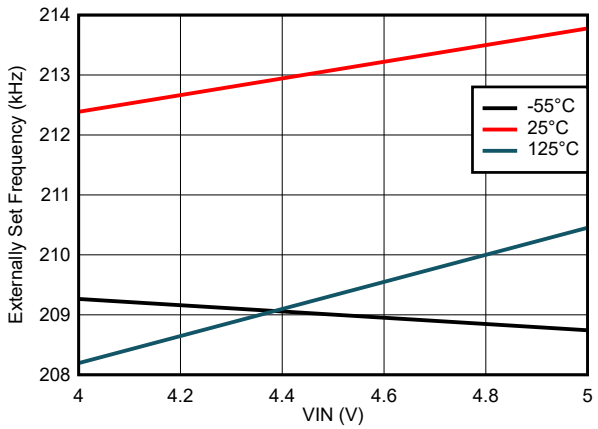
VIN = 4 V to 5 V
RT = 1.07 MΩ

Figure 7-19. Externally Set Frequency Variation



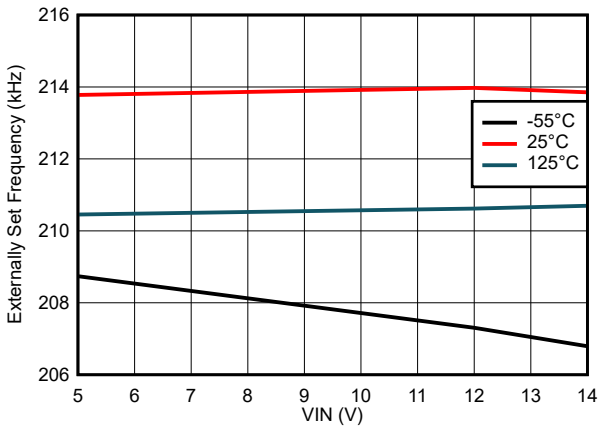
VIN = 5 V to 14 V
RT = 1.07 MΩ

Figure 7-20. Externally Set Frequency Variation



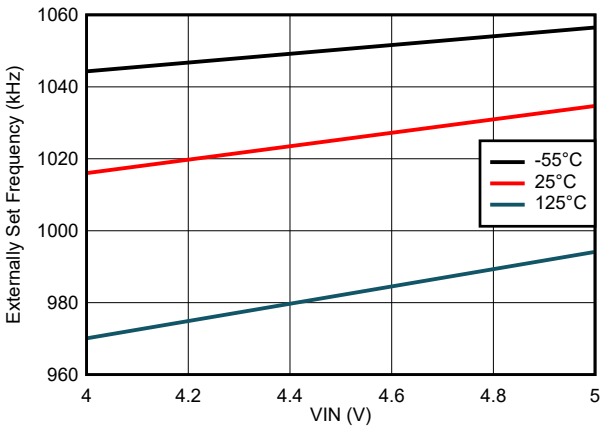
VIN = 4 V to 5 V
RT = 511 kΩ

Figure 7-21. Externally Set Frequency Variation



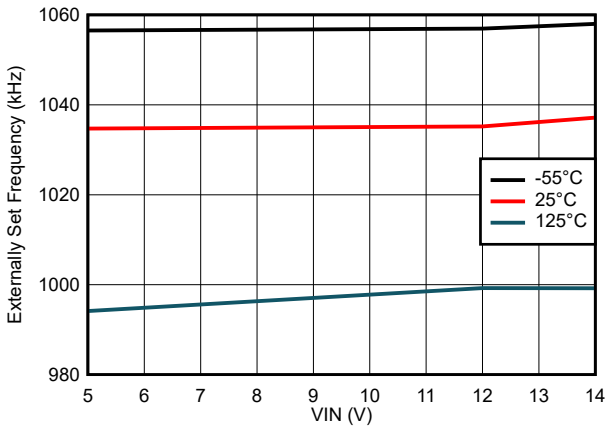
VIN = 5 V to 14 V
RT = 511 kΩ

Figure 7-22. Externally Set Frequency Variation



VIN = 4 V to 5 V
RT = 90.9 kΩ

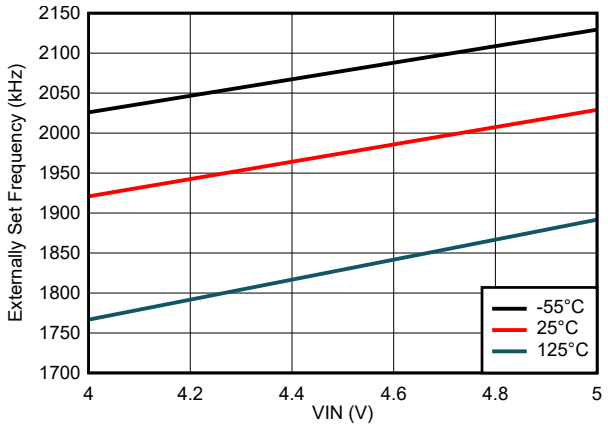
Figure 7-23. Externally Set Frequency Variation



VIN = 5 V to 14 V
RT = 90.9 kΩ

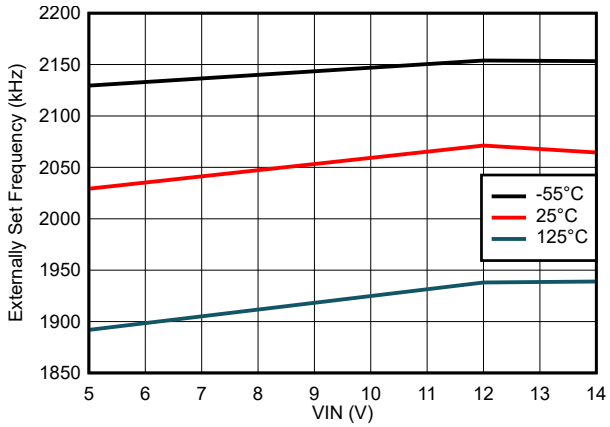
Figure 7-24. Externally Set Frequency Variation

7.10 Typical Characteristics (continued)



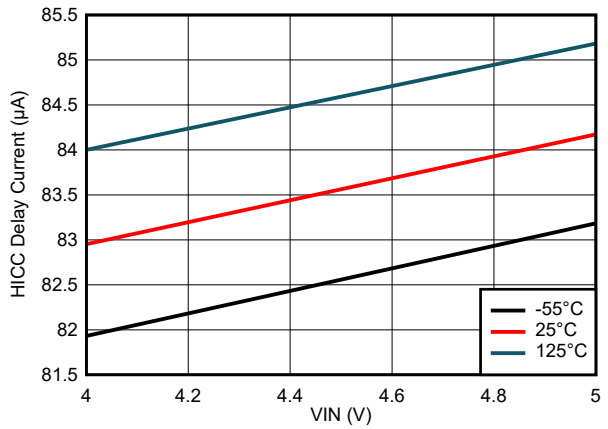
VIN = 4 V to 5 V
RT = 34.8 kΩ

Figure 7-25. Externally Set Frequency Variation



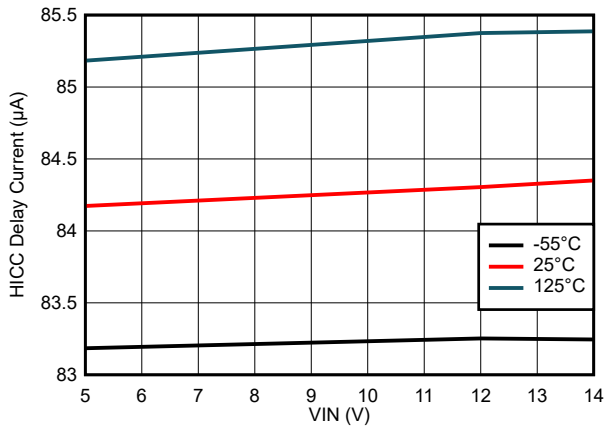
VIN = 5 V to 14 V
RT = 34.8 kΩ

Figure 7-26. Externally Set Frequency Variation



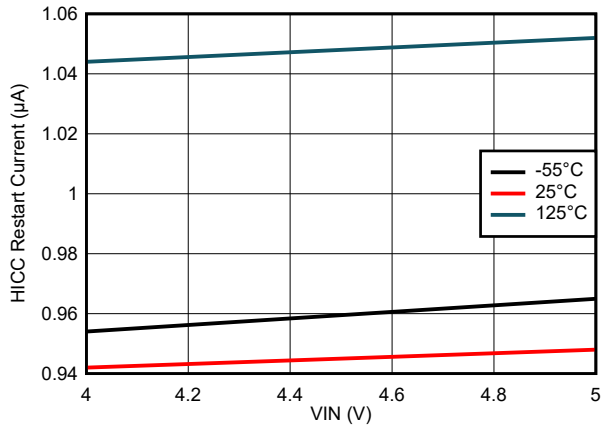
VIN = 4 V to 5 V

Figure 7-27. Hiccup Delay Current Variation



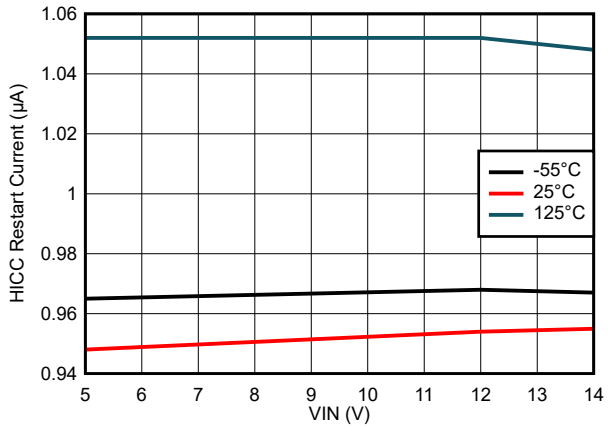
VIN = 5 V to 14 V

Figure 7-28. Hiccup Delay Current Variation



VIN = 4 V to 5 V

Figure 7-29. Hiccup Restart Current Variation



VIN = 5 V to 14 V

Figure 7-30. Hiccup Restart Current Variation

7.10 Typical Characteristics (continued)

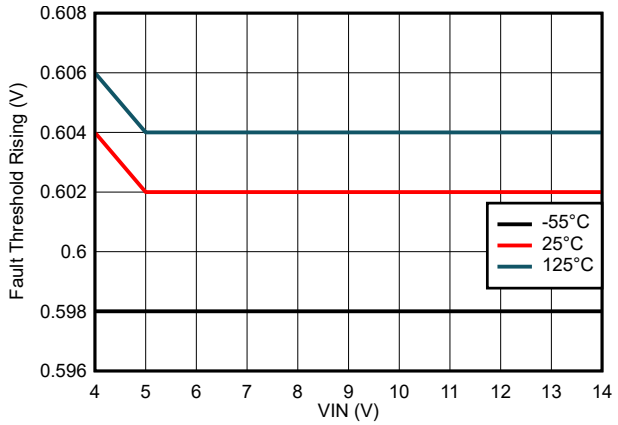


Figure 7-31. FAULT Threshold Rising Variation

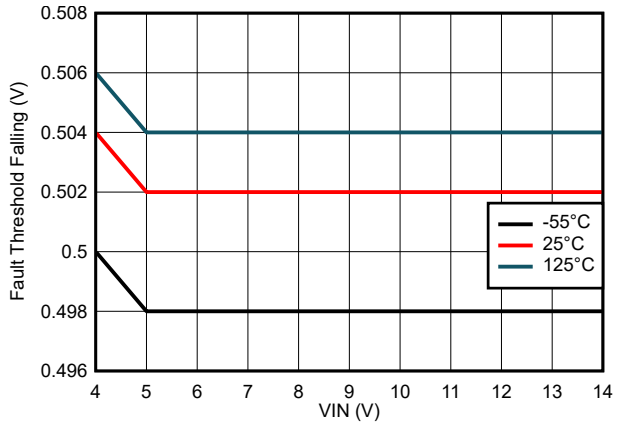
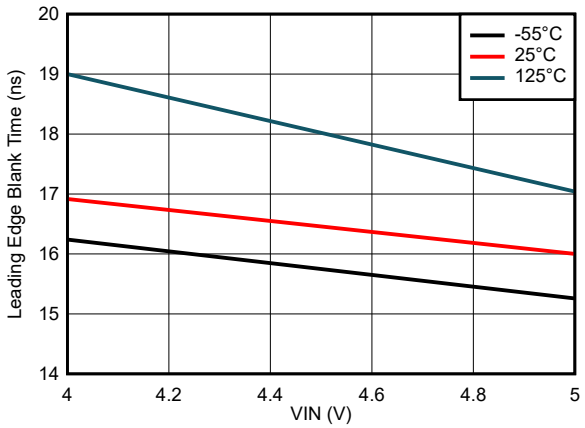
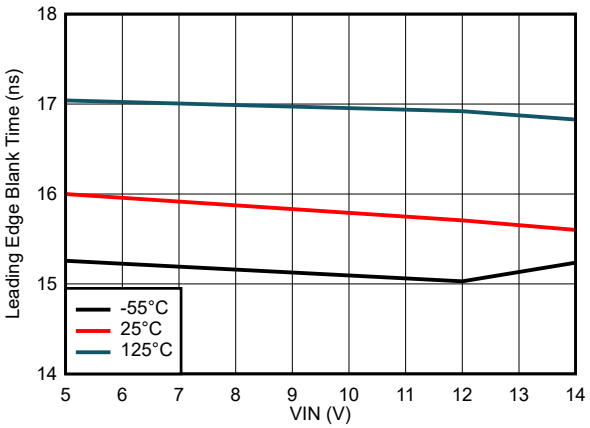


Figure 7-32. FAULT Threshold Falling Variation



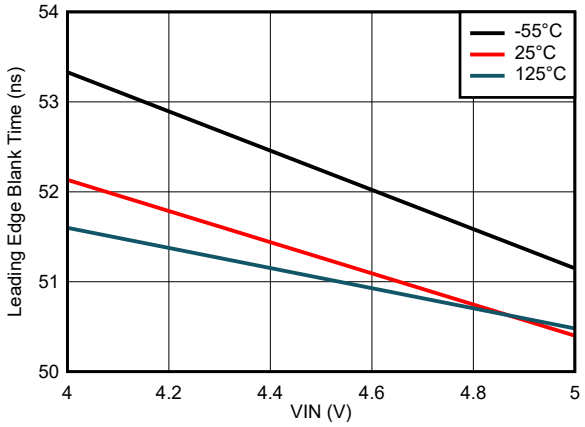
VIN = 4 V to 5 V
RT = 10 kΩ

Figure 7-33. Leading Edge Blank Time Variation



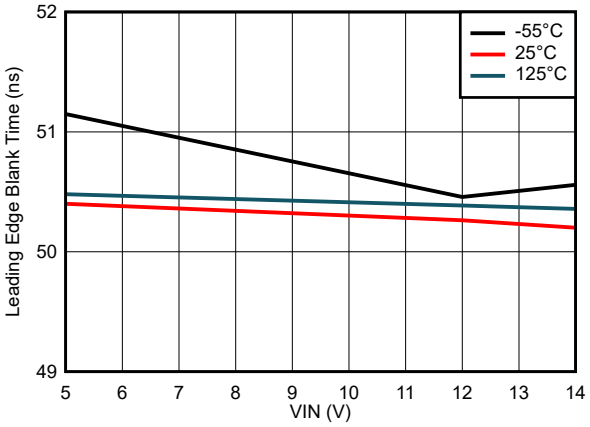
VIN = 5 V to 14 V
RT = 10 kΩ

Figure 7-34. Leading Edge Blank Time Variation



VIN = 4 V to 5 V
RT = 49.9 kΩ

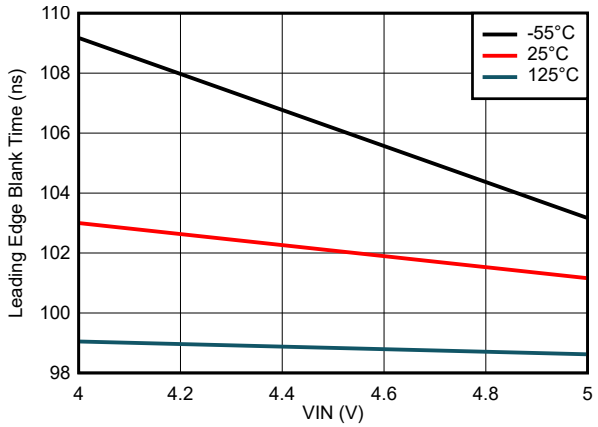
Figure 7-35. Leading Edge Blank Time Variation



VIN = 5 V to 14 V
RT = 49.9 kΩ

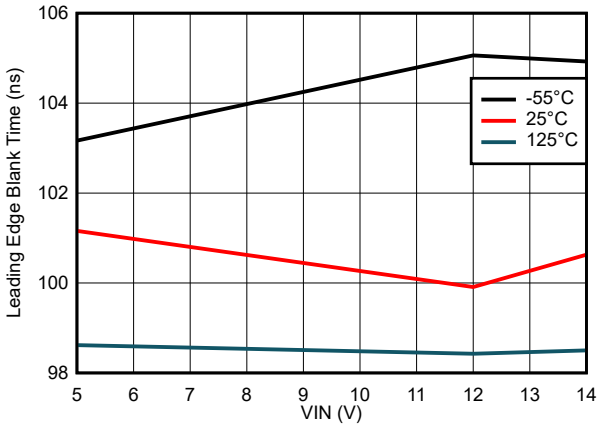
Figure 7-36. Leading Edge Blank Time Variation

7.10 Typical Characteristics (continued)



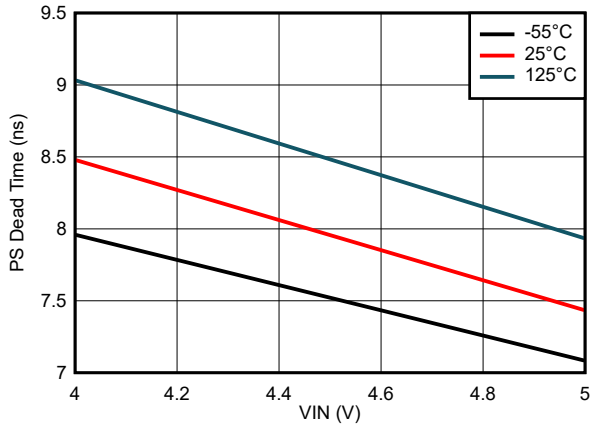
VIN = 4 V to 5 V
RT = 100 kΩ

Figure 7-37. Leading Edge Blank Time Variation



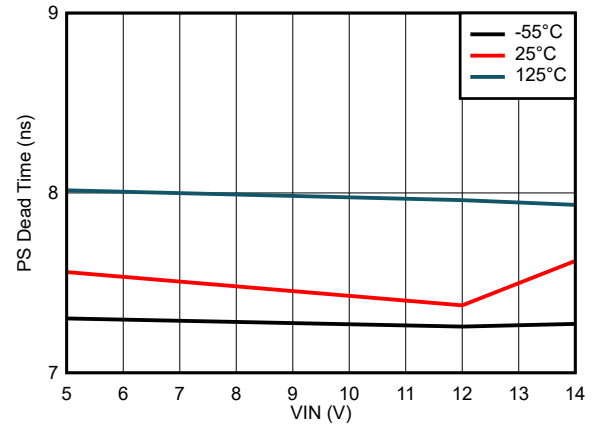
VIN = 5 V to 14 V
RT = 100 kΩ

Figure 7-38. Leading Edge Blank Time Variation



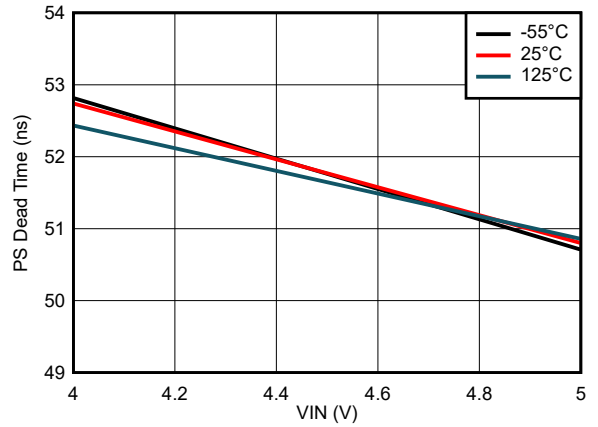
VIN = 4 V to 5 V
RT = Floating

Figure 7-39. PS Dead Time Variation



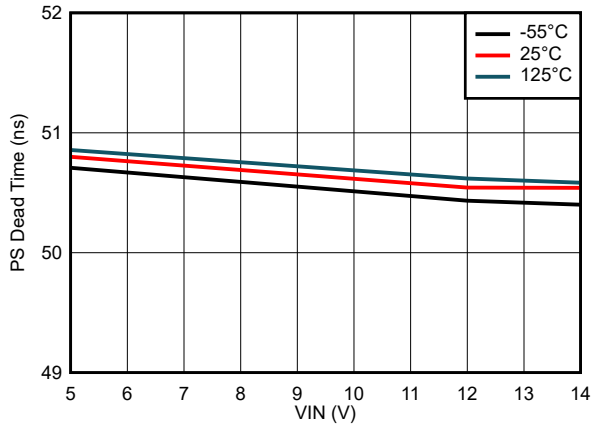
VIN = 5 V to 14 V
RT = Floating

Figure 7-40. PS Dead Time Variation



VIN = 4 V to 5 V
RT = 49.9 kΩ

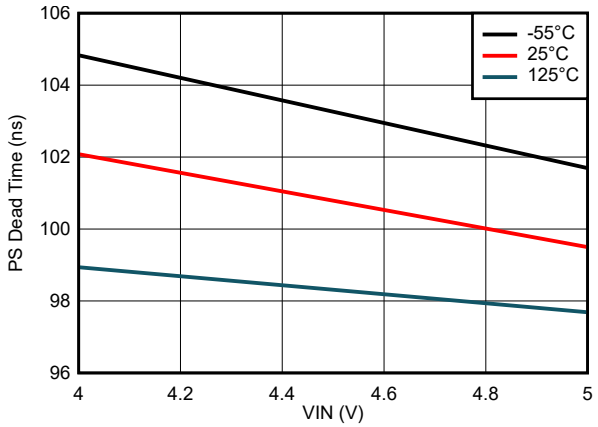
Figure 7-41. PS Dead Time Variation



VIN = 5 V to 14 V
RT = 49.9 kΩ

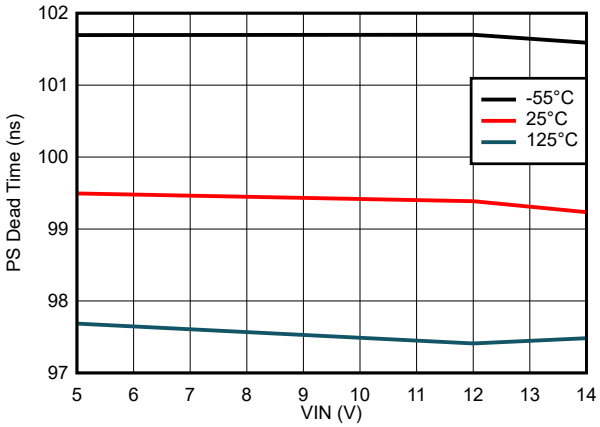
Figure 7-42. PS Dead Time Variation

7.10 Typical Characteristics (continued)



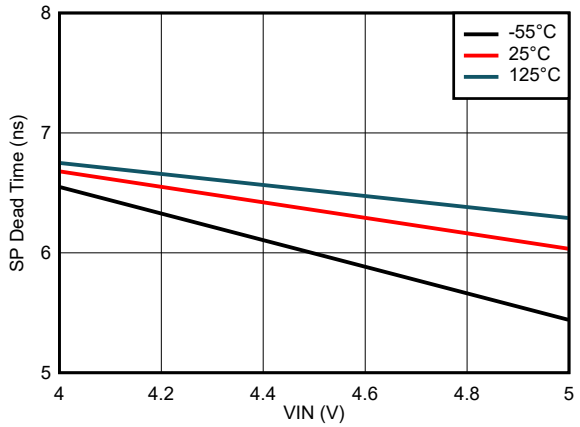
VIN = 4 V to 5 V
RT = 100 kΩ

Figure 7-43. PS Dead Time Variation



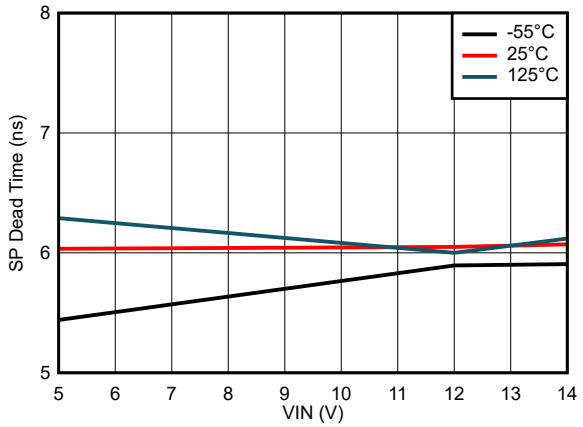
VIN = 5 V to 14 V
RT = 100 kΩ

Figure 7-44. PS Dead Time Variation



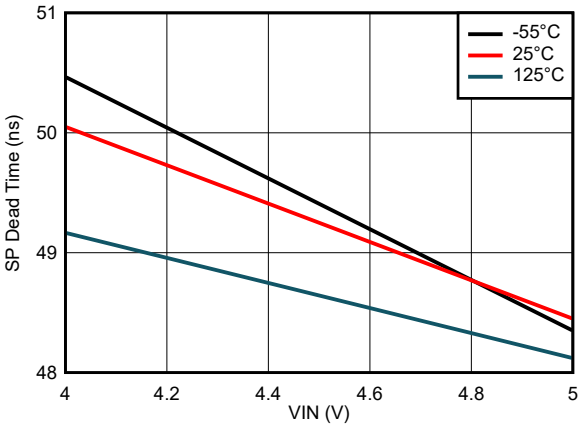
VIN = 4 V to 5 V
RT = Floating

Figure 7-45. SP Dead Time Variation



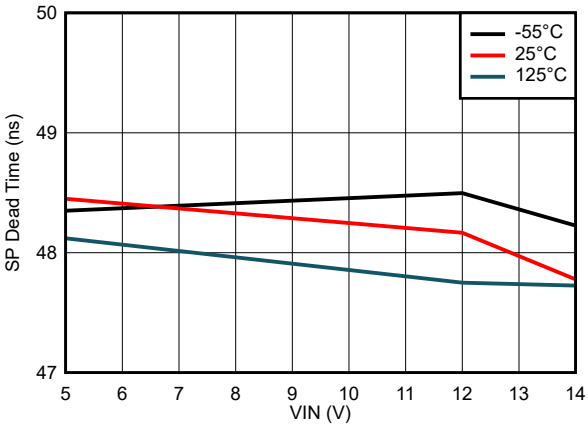
VIN = 5 V to 14 V
RT = Floating

Figure 7-46. SP Dead Time Variation



VIN = 4 V to 5 V
RT = 49.9 kΩ

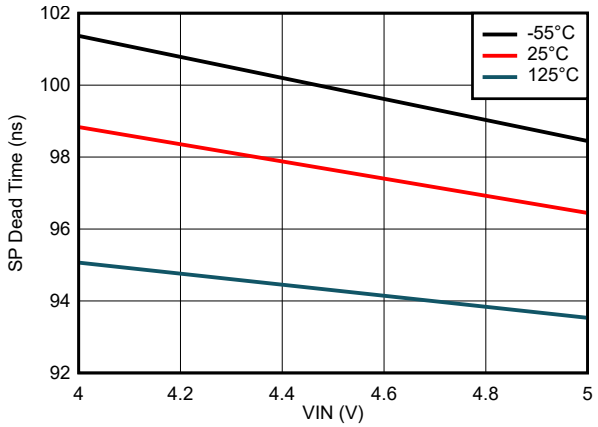
Figure 7-47. SP Dead Time Variation



VIN = 5 V to 14 V
RT = 49.9 kΩ

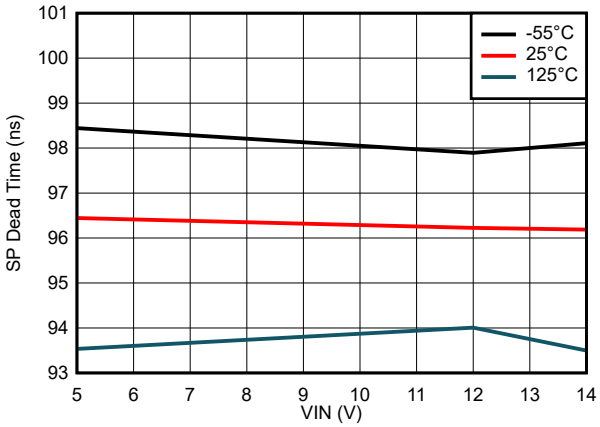
Figure 7-48. SP Dead Time Variation

7.10 Typical Characteristics (continued)



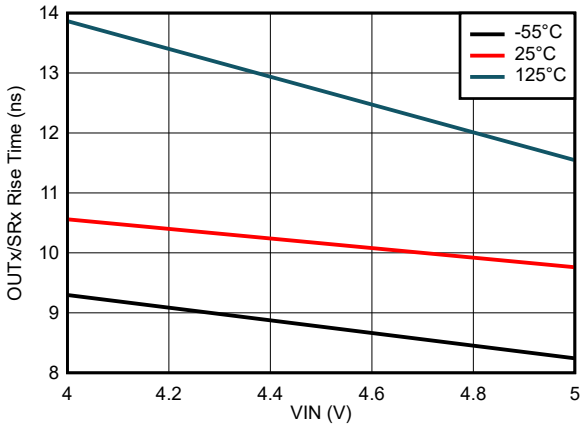
VIN = 4 V to 5 V
RT = 100 kΩ

Figure 7-49. SP Dead Time Variation



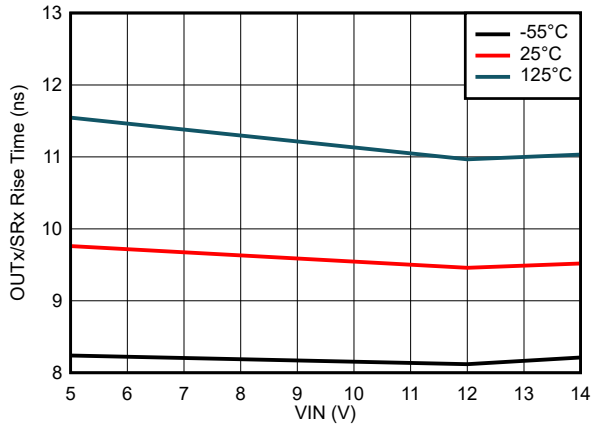
VIN = 5 V to 14 V
RT = 100 kΩ

Figure 7-50. SP Dead Time Variation



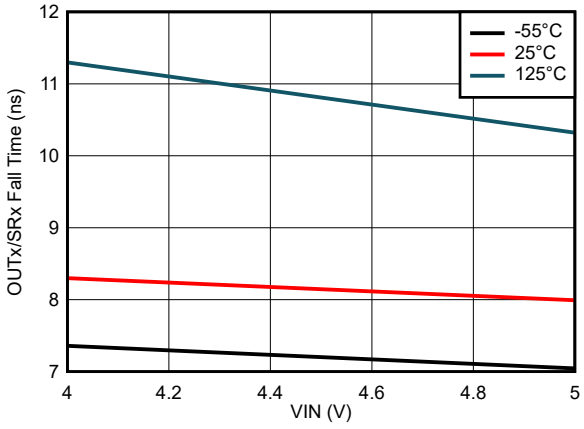
VIN = 4 V to 5 V

Figure 7-51. Output Rise Time Variation



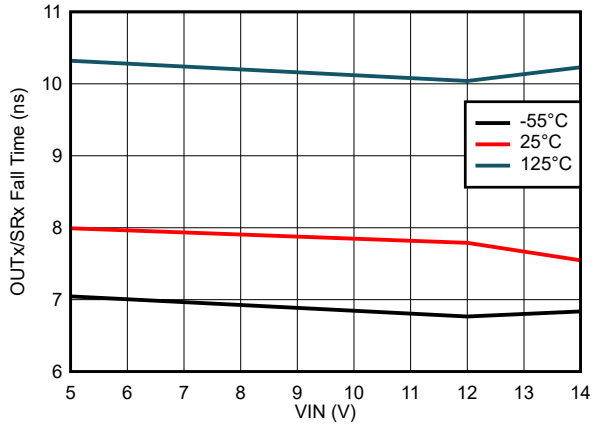
VIN = 5 V to 14 V

Figure 7-52. Output Rise Time Variation



VIN = 4 V to 5 V

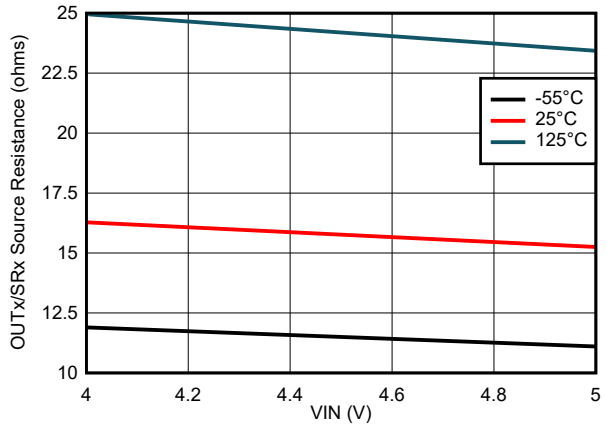
Figure 7-53. Output Fall Time Variation



VIN = 5 V to 14 V

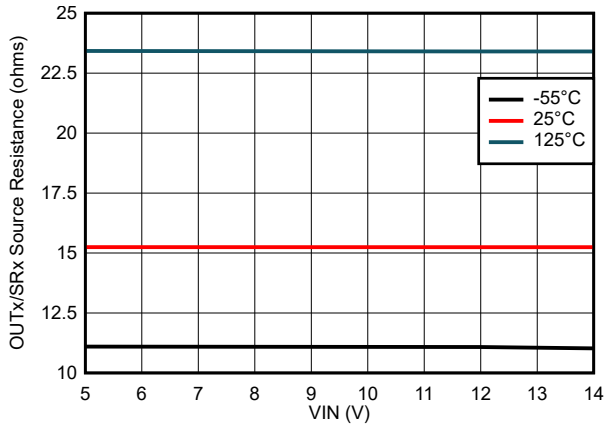
Figure 7-54. Output Fall Time Variation

7.10 Typical Characteristics (continued)



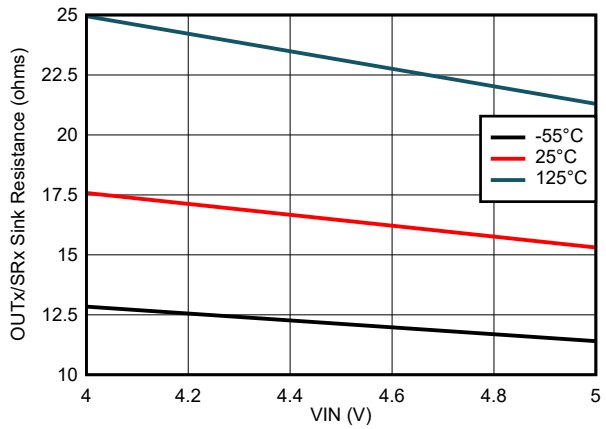
VIN = 4 V to 5 V

Figure 7-55. Output Source Resistance Variation



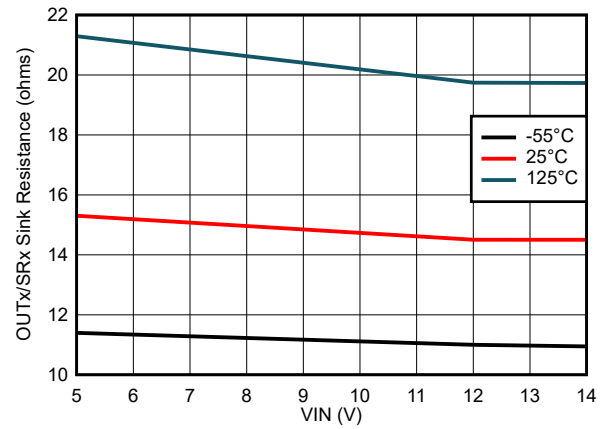
VIN = 5 V to 14 V

Figure 7-56. Output Source Resistance Variation



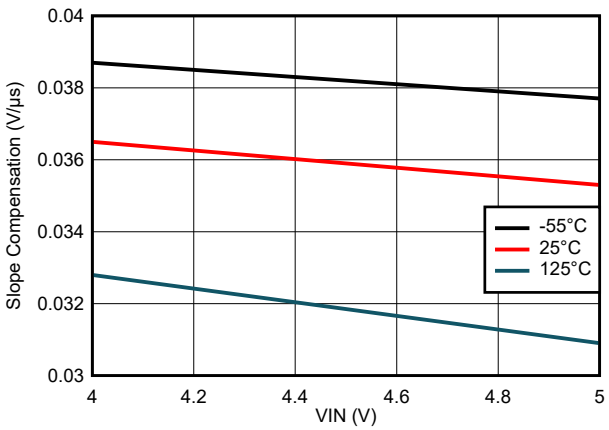
VIN = 4 V to 5 V

Figure 7-57. Output Sink Resistance Variation



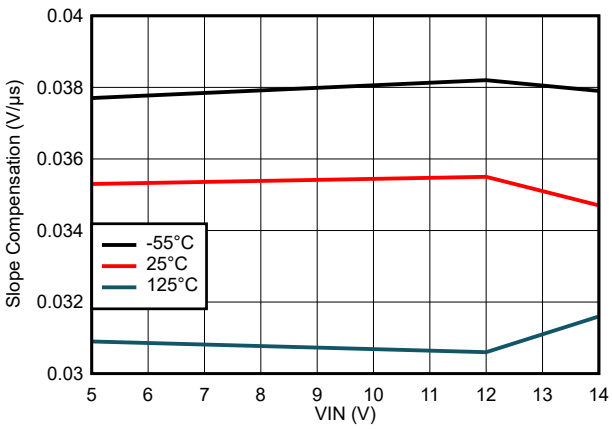
VIN = 5 V to 14 V

Figure 7-58. Output Sink Resistance Variation



VIN = 4 V to 5 V
RT = 1.18 MΩ

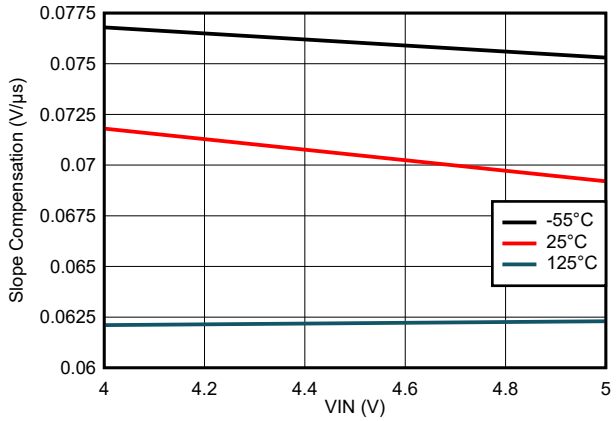
Figure 7-59. Slope Compensation Variation



VIN = 5 V to 14 V
RT = 1.18 MΩ

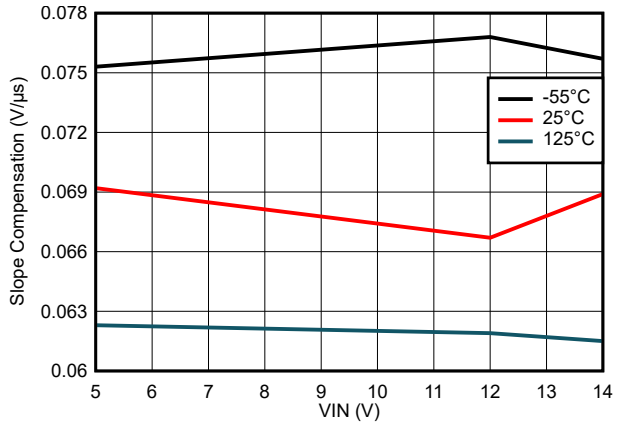
Figure 7-60. Slope Compensation Variation

7.10 Typical Characteristics (continued)



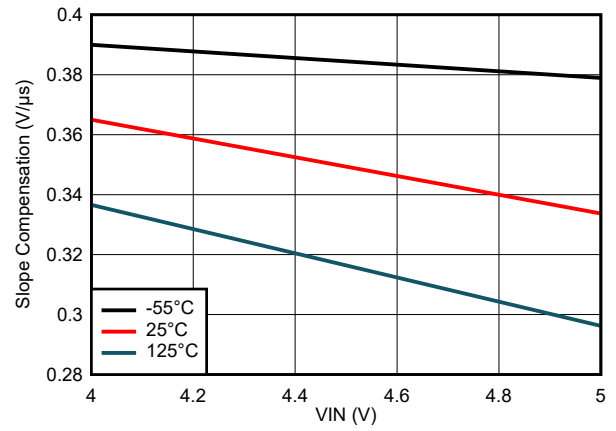
VIN = 4 V to 5 V
RT = 562 kΩ

Figure 7-61. Slope Compensation Variation



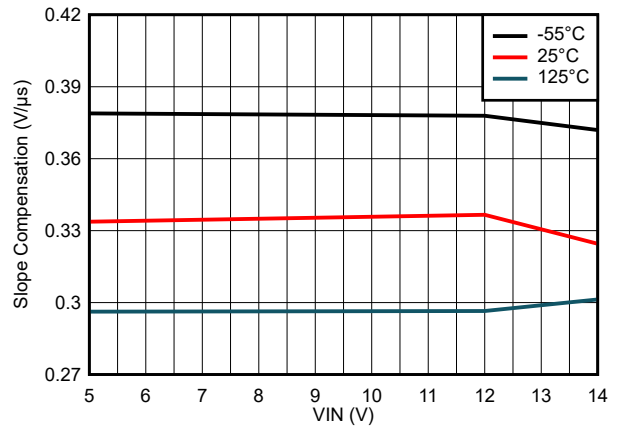
VIN = 5 V to 14 V
RT = 562 kΩ

Figure 7-62. Slope Compensation Variation



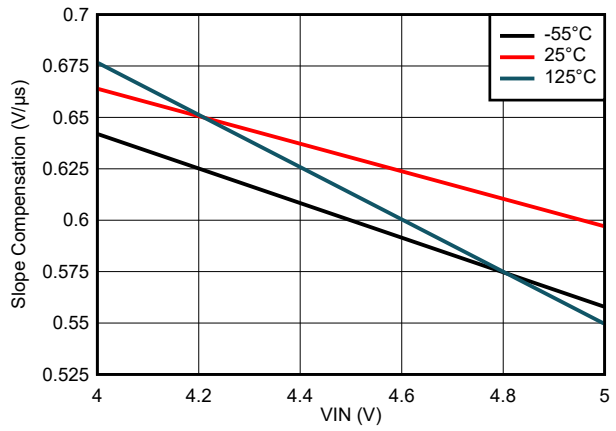
VIN = 4 V to 5 V
RT = 100 kΩ

Figure 7-63. Slope Compensation Variation



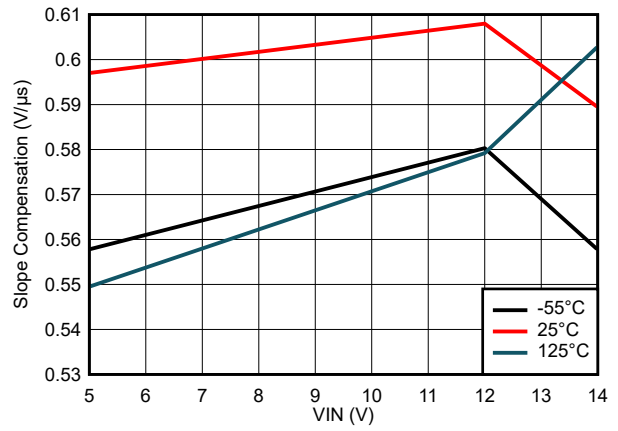
VIN = 5 V to 14 V
RT = 100 kΩ

Figure 7-64. Slope Compensation Variation



VIN = 4 V to 5 V
RT = 49.9 kΩ

Figure 7-65. Slope Compensation Variation



VIN = 5 V to 14 V
RT = 49.9 kΩ

Figure 7-66. Slope Compensation Variation

8 Detailed Description

8.1 Overview

The TPS7H500x-SP series is a family of radiation-hardness-assured PWM controllers. Each controller features a voltage reference of 0.613 V with accuracy of ±1%. The switching frequency is configurable from 100 kHz to 2 MHz, with external clock synchronization capability. The series consists of the full-featured device TPS7H5001-SP, as well as the three additional specialized controllers TPS7H5002-SP, TPS7H5003-SP, and TPS7H5004-SP.

The TPS7H5001-SP is a radiation-hardness-assured, current mode, dual output PWM controller optimized for silicon (Si) and gallium nitride (GaN) based DC-DC converters in space applications. The switching frequency of the TPS7H5001-SP can be configured from 100 kHz to 2 MHz while still maintaining a very low current consumption, which makes it ideal for fully exploiting the area reduction and high efficiency benefits of GaN based DC-DC converters. The device features integrated synchronous rectifier control outputs and dead-time programmability in order to target high efficiency and high performance topologies. In addition, the TPS7H5001-SP supports single-ended converter topologies by providing the user flexibility to control the maximum duty cycle. The 0.613-V ±1% accurate internal reference allows design of high-current buck converters for FPGA core voltages.

The TPS7H5002-SP is a single output radiation-hardness-assured PWM controller that supports buck applications and single ended isolated topologies. The controller contains an integrated synchronous rectification output. Optimized for GaN power semiconductor based applications, the controller has configurable dead time and configurable leading edge blank time. The controller can be configured for maximum duty cycle of 75% or 100%. As such, the DCL pin can be left floating or connected to VLDO. Connection of the DCL pin to AVSS is not permissible for this device.

The TPS7H5003-SP is also a single output radiation-hardness-assured PWM controller that contains an integrated synchronous rectification output. The dead time and leading edge blank time are fixed at 50 ns for this device. The controller can be configured for maximum duty cycle of 75% or 100%. As such, the DCL pin can be left floating or connected to VLDO. Connection of the DCL pin to AVSS is not permissible for this device.

The TPS7H5004-SP is a dual output radiation-hardness-assured PWM controller suited for usage in non-synchronous push-pull and full-bridge topologies. The controller has configurable leading edge blank time. The maximum duty cycle for this device is 50% and the DCL pin must be connected to AVSS.

8.2 Functional Block Diagram

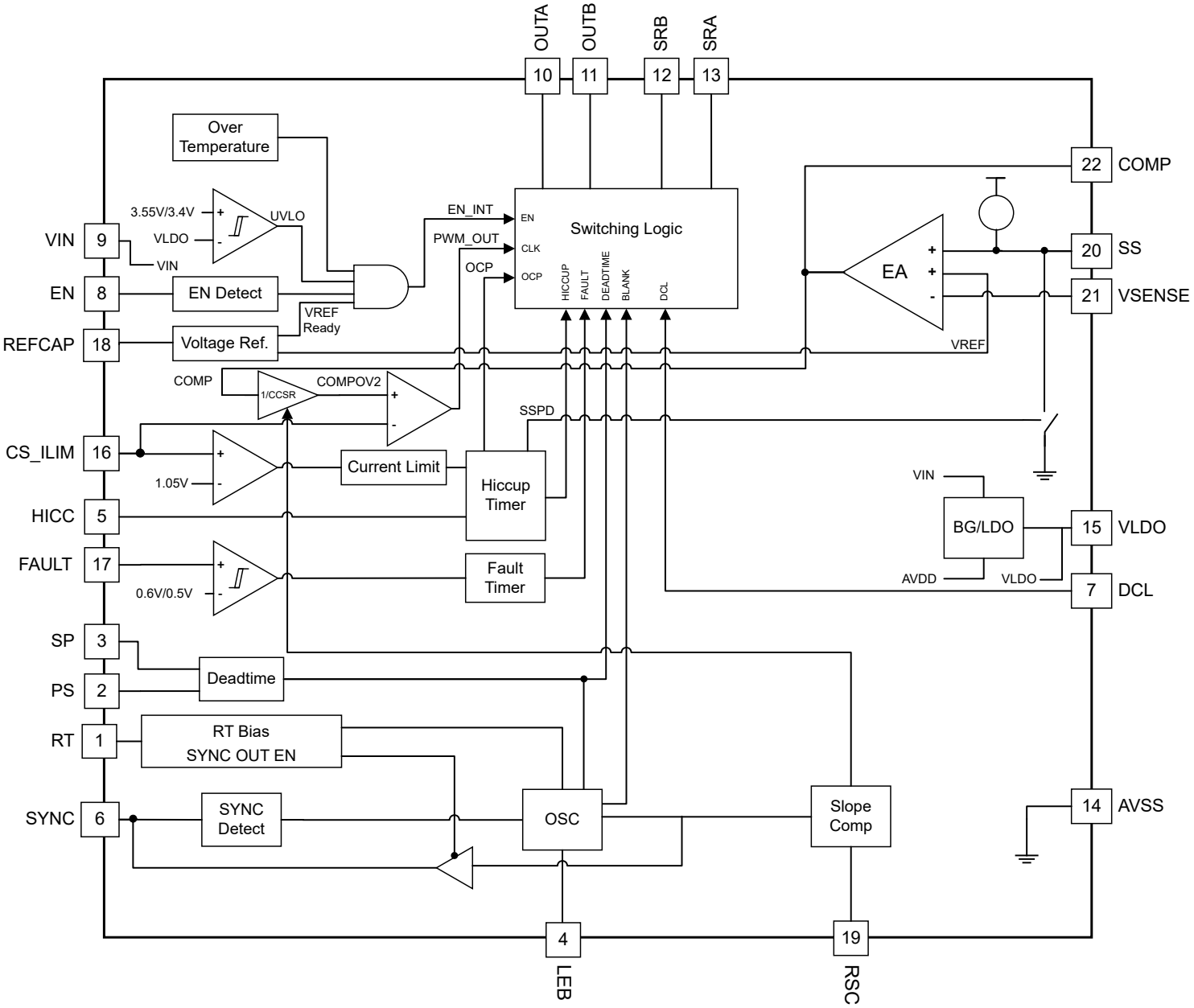


Figure 8-1. TPS7H5001-SP Functional Block Diagram

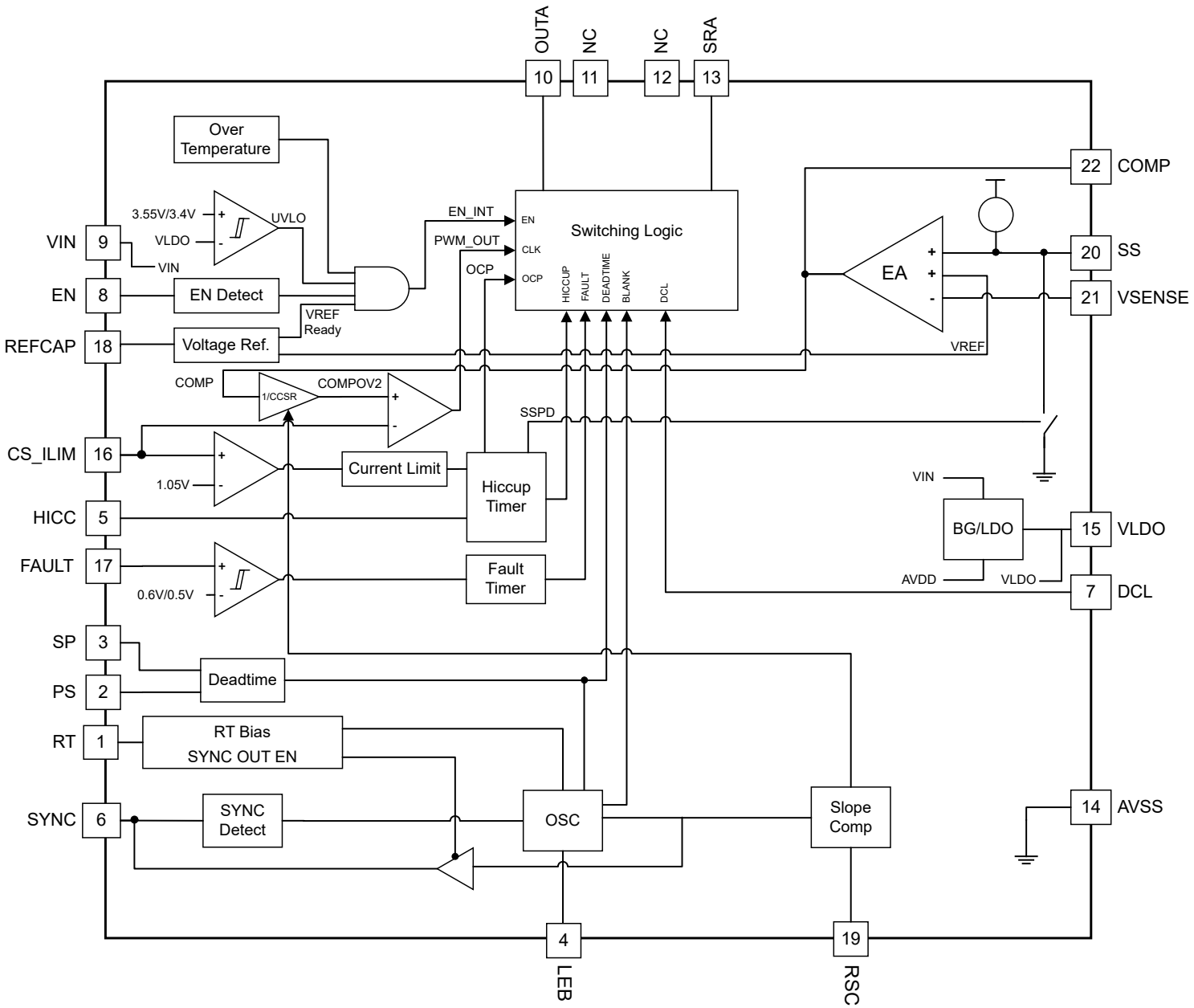


Figure 8-2. TPS7H5002-SP Functional Block Diagram

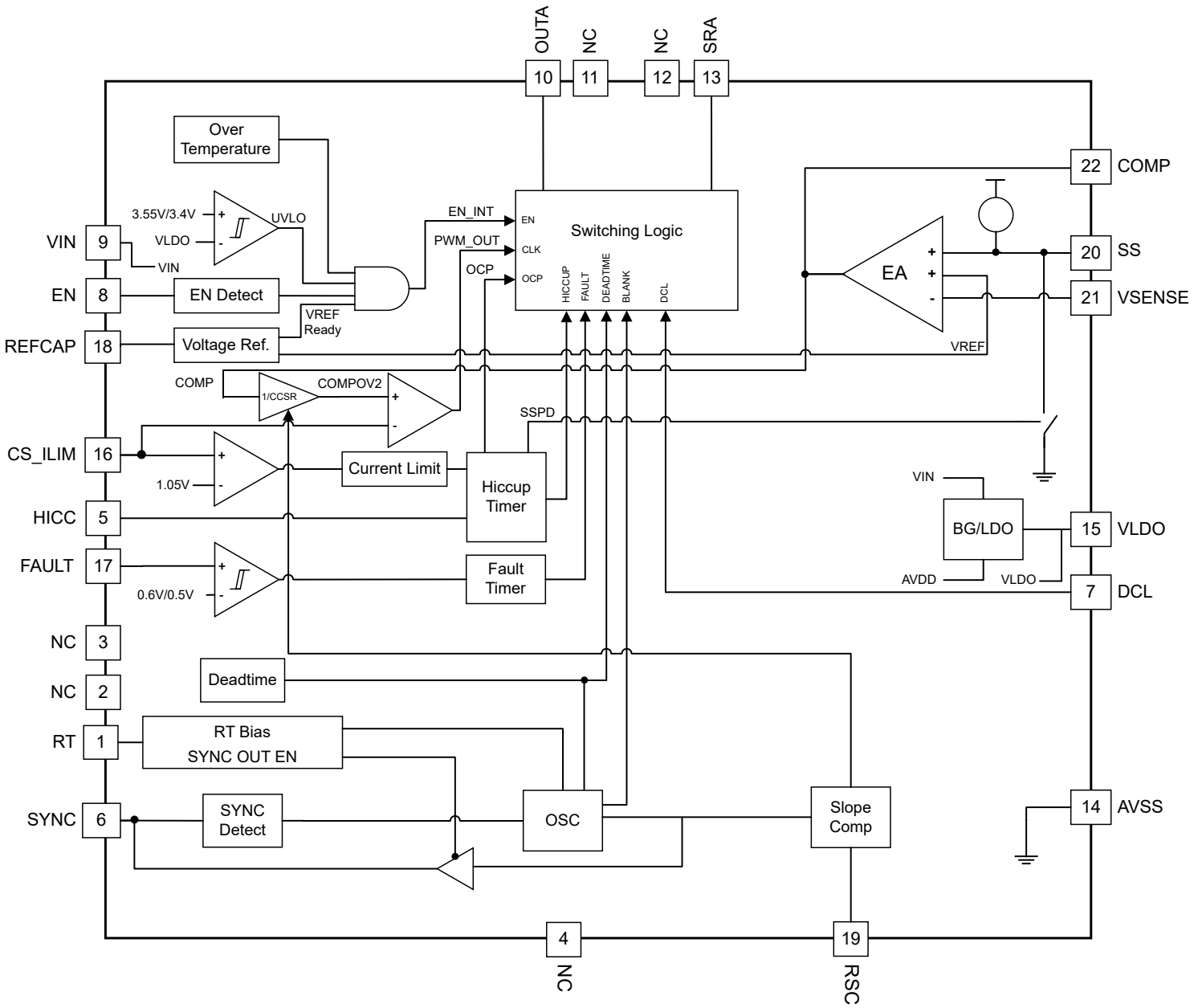


Figure 8-3. TPS7H5003-SP Functional Block Diagram

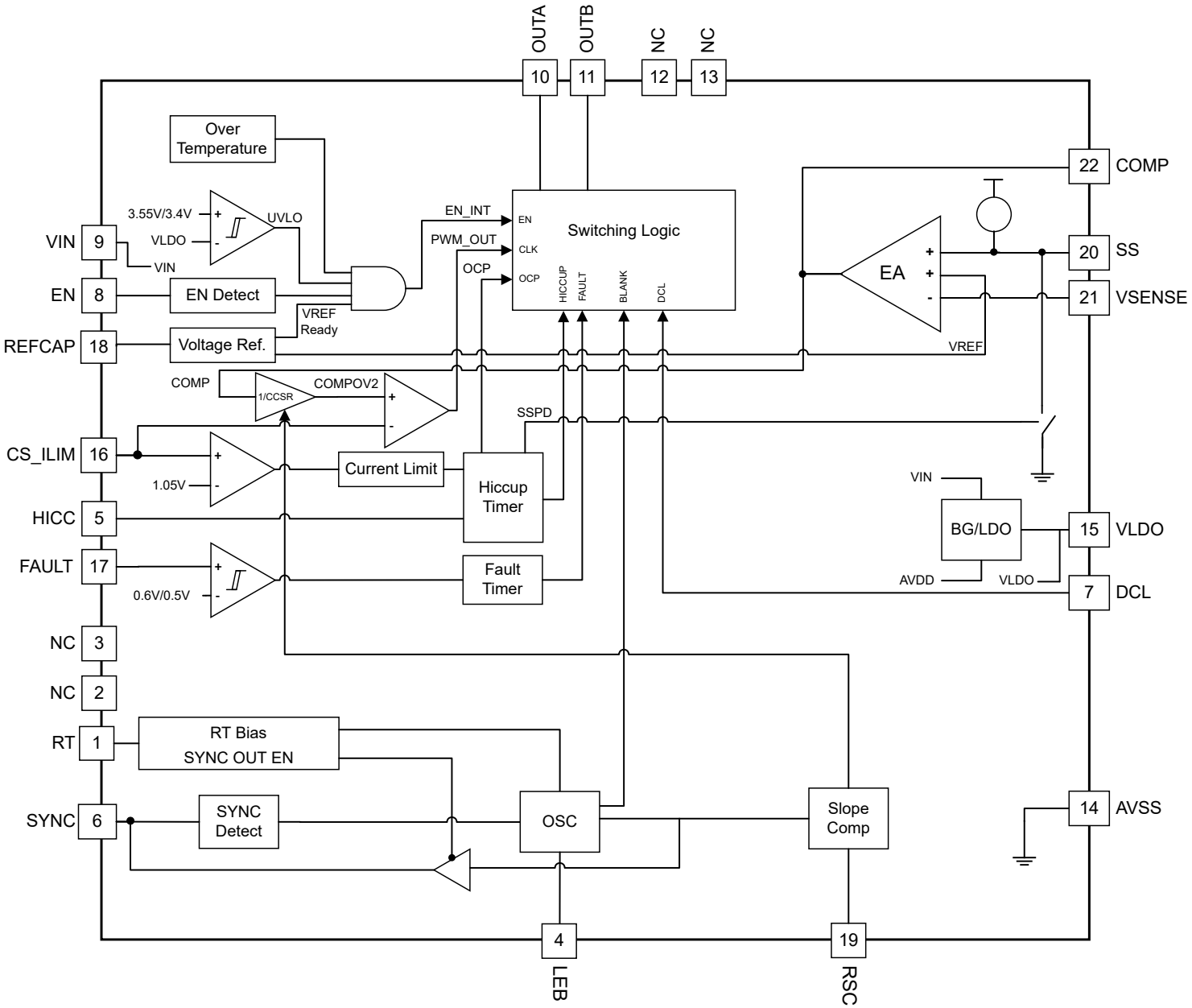


Figure 8-4. TPS7H5004-SP Functional Block Diagram

8.3 Feature Description

8.3.1 VIN and VLDO

During steady state operation, the input voltage of the TPS7H500x-SP must be between 4 V and 14 V. A minimum bypass capacitance of at least 0.1 µF is needed between VIN and AVSS. The input bypass capacitors should be placed as close to the controller as possible.

The voltage applied at VIN serves as the input for the internal regulator that generates the VLDO voltage (5 V). At input voltages less than 5 V, the VLDO voltage will follow the voltage at VIN. Recommended capacitance for VLDO is 1 µF. The EN and/or DCL pin can be tied to VLDO, but otherwise it is recommended to not externally load this pin due to limited output current capability.

A voltage divider connected between VIN and the EN pin can adjust the input voltage UVLO appropriately.

8.3.2 Start-Up

Before the primary outputs of the controller will start switching, the following conditions must be met:

- VLDO exceeds the rising UVLO threshold of 3.55 V (typical)
- The internal 0.613 V reference voltage is available
- The enable signal EN is above the rising voltage threshold of 0.6 V (typical)
- The FAULT pin voltage is below the rising voltage threshold of 0.6 V (typical)
- The device junction temperature is below the thermal shutdown threshold of 175°C (typical)

Once all of the aforementioned conditions are satisfied, the soft-start process will be initiated.

8.3.3 Enable and Undervoltage Lockout (UVLO)

There are several methods for enabling the TPS7H500x-SP through the EN pin. The pin can be tied directly to VLDO, which would allow for the device to be enabled as soon as the voltage on VLDO surpasses the rising edge voltage threshold of the EN pin. The pin can also be driven with an externally generated signal or a compatible PGOOD signal for instances in which sequencing is desired. Lastly, two resistors can be used to program the controller to enable when VIN surpasses a user determined threshold, as shown in Figure 8-5 . The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AVSS.

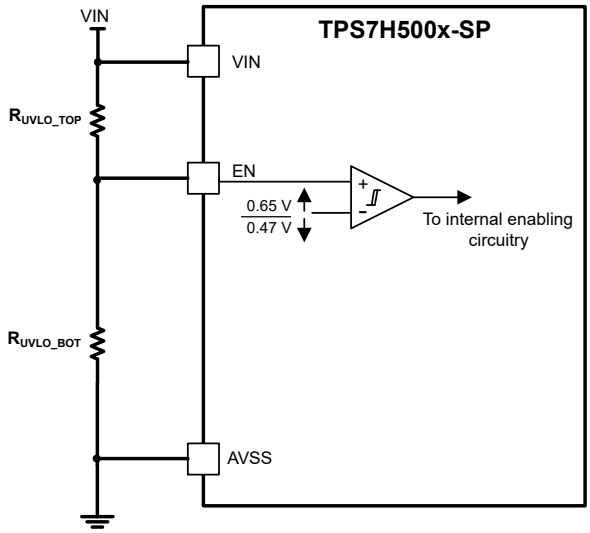


Figure 8-5. Enable Pin Configuration Using Two External Resistors

Using Equation 1, the user can calculate the value for R_{UVLO_TOP} for a chosen value of R_{UVLO_BOT} based on the desired maximum start-up voltage for the device. With these selected resistors Equation 2 can be used to determine the minimum start-up voltage.

$$R_{UVLO\_TOP} = R_{UVLO\_BOT} \times \left(\frac{V_{START,MAX}}{V_{EN\_RISING\_MAX}} - 1 \right) \quad (1)$$

$$V_{START,MIN} = V_{EN\_RISING\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (2)$$

In the two-resistor configuration of Figure 8-5, the controller will also shut down due to undervoltage lockout when the input voltage falls below a particular threshold. This is due to the hysteresis of the EN pin. In order to determine the voltages at which shutdown is expected to occur, use Equation 3 and Equation 4.

$$V_{STOP,MAX} = V_{EN\_FALLING\_MAX} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (3)$$

$$V_{STOP,MIN} = V_{EN\_FALLING\_MIN} \times \left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1 \right) \quad (4)$$

It is important to note that the user should take care when selecting the values for R_{UVLO_TOP} and R_{UVLO_BOT}. It is recommended to optimize the selection of these resistors for start-up in order to ensure proper operation. The UVLO value must be approximately 75% or less of the input voltage in order to ensure that the device turns on as expected under all circumstances. Setting the UVLO any higher may cause issues with the turn-on of the device. Figure 8-6 shows the expected start-up and UVLO voltages on a 12-V rail where the maximum start-up voltage is 90% of the nominal input voltage. In this instance, turn-off will occur when the input voltage falls to between 75% and 65% of its nominal value.

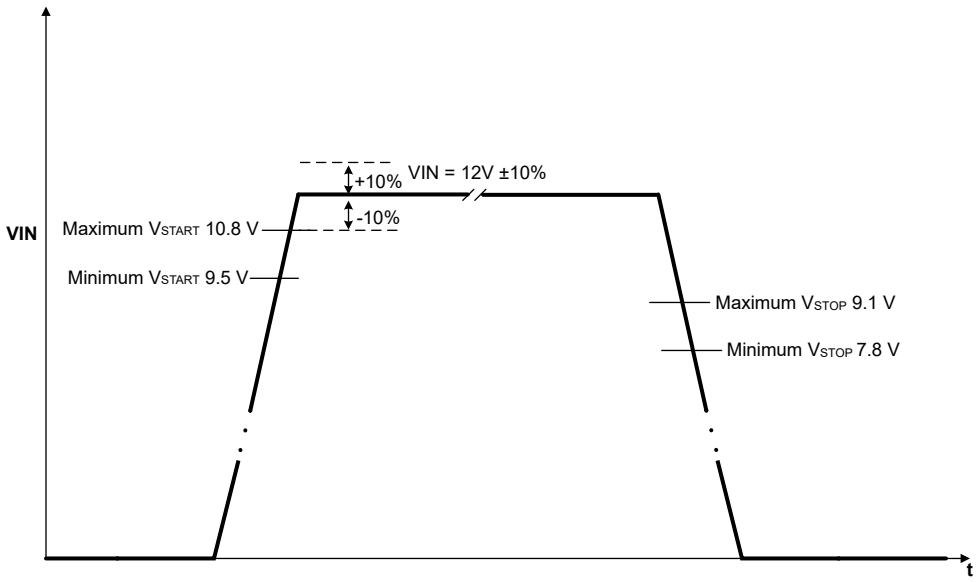


Figure 8-6. Start-Up and UVLO Values for Two-Resistor Configuration With VIN = 12 V

8.3.4 Voltage Reference

Each device generates an internal 1.23-V bandgap reference that is utilized throughout the various control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to 0.613 V to produce the reference for the error amplifier. The error amplifier reference is measured at the COMP pin to account for offsets in the error amplifier and maintains regulation within ±1% across line, load, temperature, and TID as shown in Section 7. This tight reference tolerance allows for the user to design a highly accurate power converter. A 470-nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

8.3.5 Error Amplifier

Each TPS7H500x-SP controller uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS pin voltage or the internal 0.613-V voltage reference. The transconductance of the error amplifier is 1800 µA/V during normal operation. The frequency compensation network is connected between COMP pin and AVSS. The error amplifier DC gain is typically 10,000 V/V.

8.3.6 Output Voltage Programming

The output voltage of the power converter is set by using a resistor divider from V_{OUT} of the converter to the VSENSE pin. The output voltage must be divided down to nominal voltage reference of 0.613 V. Equation 5 can be used to select R_{BOTTOM}.

$$R_{BOTTOM} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP} \quad (5)$$

where:

- V_{REF} is 0.613 V (typical)
- V_{OUT} is the desired output voltage
- R_{TOP} is the value of the top resistor, selected by the user (i.e. 10 kΩ)

The recommendation is to use high tolerance resistors (1% or less) for R_{BOTTOM} and R_{TOP} for improved output voltage setpoint accuracy.

8.3.7 Soft Start (SS)

The soft-start circuit increases the output voltage of the converter gradually until the steady-state programmed output is reached. During soft start, the error amplifier uses the voltage on the soft-start pin as its reference until the SS pin voltage rises above V_{REF}. Once the voltage at SS pin is above V_{REF}, the soft-start period is complete. Note that the voltage at SS pin will continue to rise and once it reaches 1 V, the synchronous rectifier outputs of the controller will become active.

A capacitor between the SS pin and AVSS controls the soft-start time of the PWM controller. The following equation can be used to select the capacitor for the desired soft-start time:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (6)$$

where:

- t_{SS} is the desired soft-start time
- V_{REF} is voltage reference of 0.613 V (typical)
- I_{SS} is the soft-start charging current of 2.7 µA (typical)

8.3.8 Switching Frequency and External Synchronization

Each TPS7H500x-SP controller has three modes for setting the switching frequency of the device: internal oscillator, external synchronization, and primary-secondary. The device is placed on one of these modes through unique configurations of the RT and SYNC pins. Primary-secondary mode can be used when it is desired for two controllers to have synchronized switching without the use of the external clock.

8.3.8.1 Internal Oscillator Mode

A resistor from the RT pin to AVSS sets the switching frequency of the device. The TPS7H500x-SP controller has a switching frequency range of 100 kHz to 2 MHz. In internal oscillator mode, the RT pin must be populated or the controller will not perform any switching. Equation 7 shows the calculation determining the RT value for a desired switching frequency. The curve in Figure 8-7 shows the RT value that corresponds to a given switching frequency for the TPS7H5001-SP.

$$RT = \frac{112000}{f_{sw}} - 19.7 \quad (7)$$

where:

- RT is in kΩ
- f_{sw} is in kHz

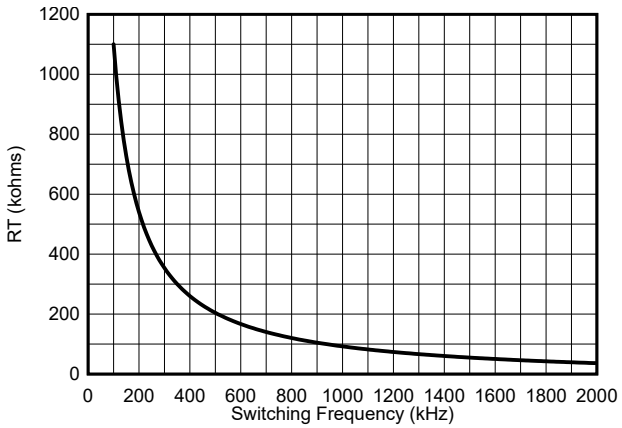


Figure 8-7. RT vs Switching Frequency

In this mode, the SYNC pin is configured as an output and produces a clock signal with a frequency that is twice that of the switching frequency set by RT. As such, this clock signal has a range of 200 kHz to 4 MHz. This SYNC output clock signal is in phase with the switching frequency of the device. Figure 8-8 shows typical waveforms for the controller in this mode of operation. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP.

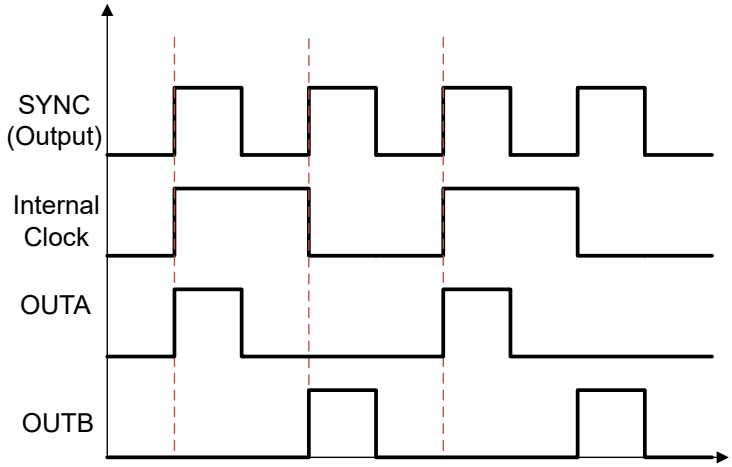


Figure 8-8. Switching Waveforms for Internal Oscillator Mode

8.3.8.2 External Synchronization Mode

Each controller can be used in external synchronization mode by leaving the RT pin floating and applying a clock to the SYNC pin. Note than the RT pin configuration sets the oscillator mode of the controller and must be left floating for this mode of operation. The external clock that is applied must be set to twice the desired switching frequency (i.e. a 1-MHz applied clock is needed for 500-kHz switching frequency). The external clock must be in the range of 200 kHz to 4 MHz with a duty cycle between 40% and 60%. It is recommended to use an external clock with 50% duty cycle. The controller will internally invert the clock signal that is applied at the SYNC pin during this mode. Since the controller does not perform any switching with RT floating, the applied clock must be present before OUTA and OUTB will become active for external synchronization mode. Figure 8-9 shows the

switching waveforms for the controller in external synchronization mode. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP.

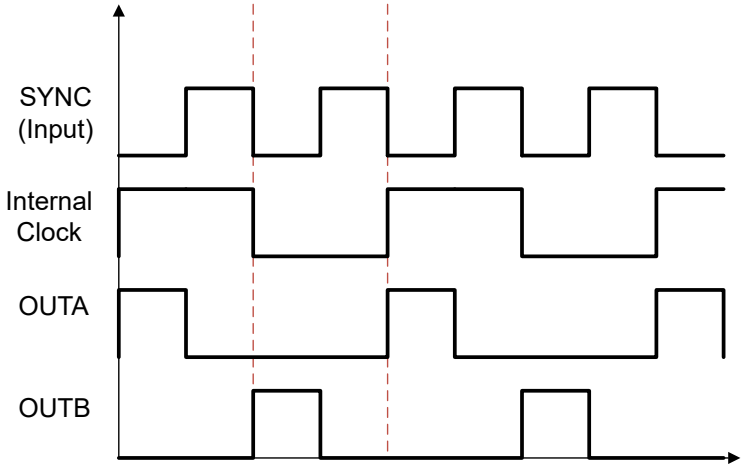


Figure 8-9. Switching Waveforms for External Synchronization Mode

8.3.8.3 Primary-Secondary Mode

Two TPS7H500x-SP controllers can be operated in a primary-secondary mode by utilizing the SYNC pin. As mentioned in the *Internal Oscillator* section, when RT is selected to provide the desired switching frequency, SYNC outputs a clock signal at twice the switching frequency. As such, the clock input generated by the primary device be used as the clock input at SYNC for the secondary controller, which would operate in external synchronization mode. This means that the RT pin of the primary device should be populated while the corresponding pin of the secondary device would be left floating.

The primary-secondary mode would be useful in a couple of scenarios. The first is for two independent converters that need to be synchronized to the same switching frequency. In this instance, the converters can be two converters can have different operating conditions or topologies. Besides the shared SYNC signal, there are no connections between the two converters.

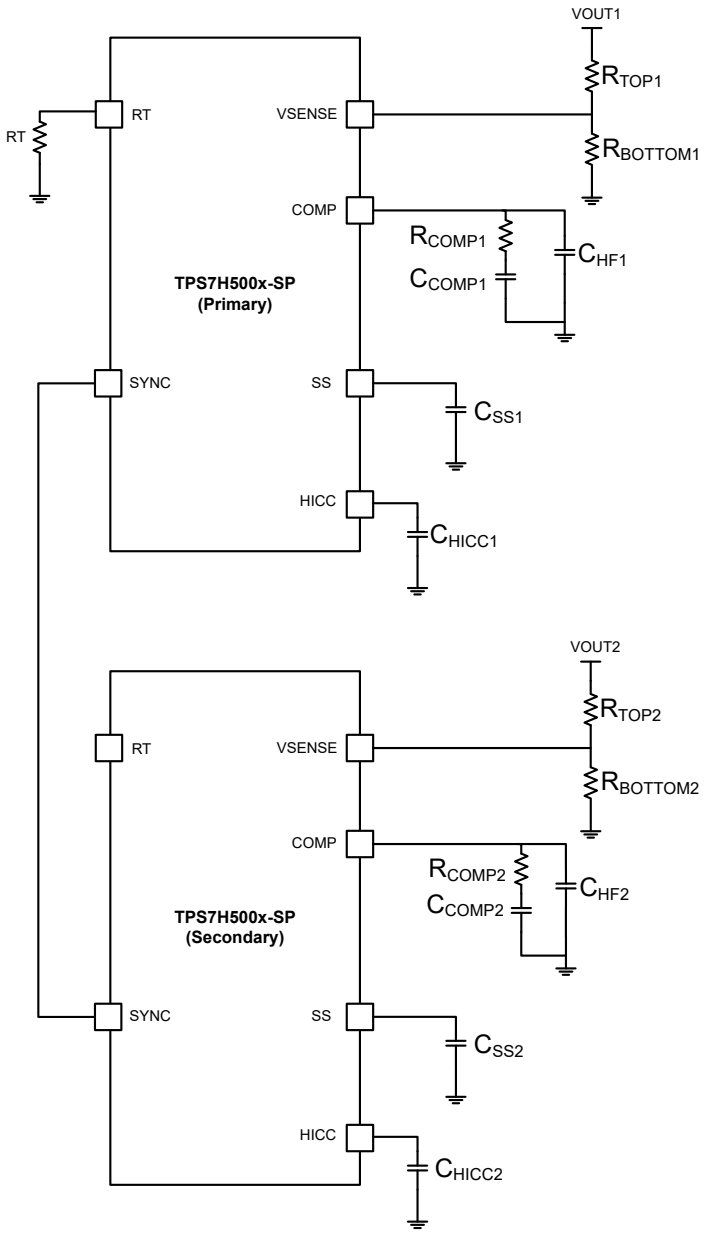


Figure 8-10. Primary-Secondary Mode Configuration for Two Independent Converters

In a second scenario, two controllers can be used to design a single interleaved converter with phases in parallel. In this design, the VSENSE, COMP, SS, and HICC pins would need to be connected in addition to the shared SYNC connection.

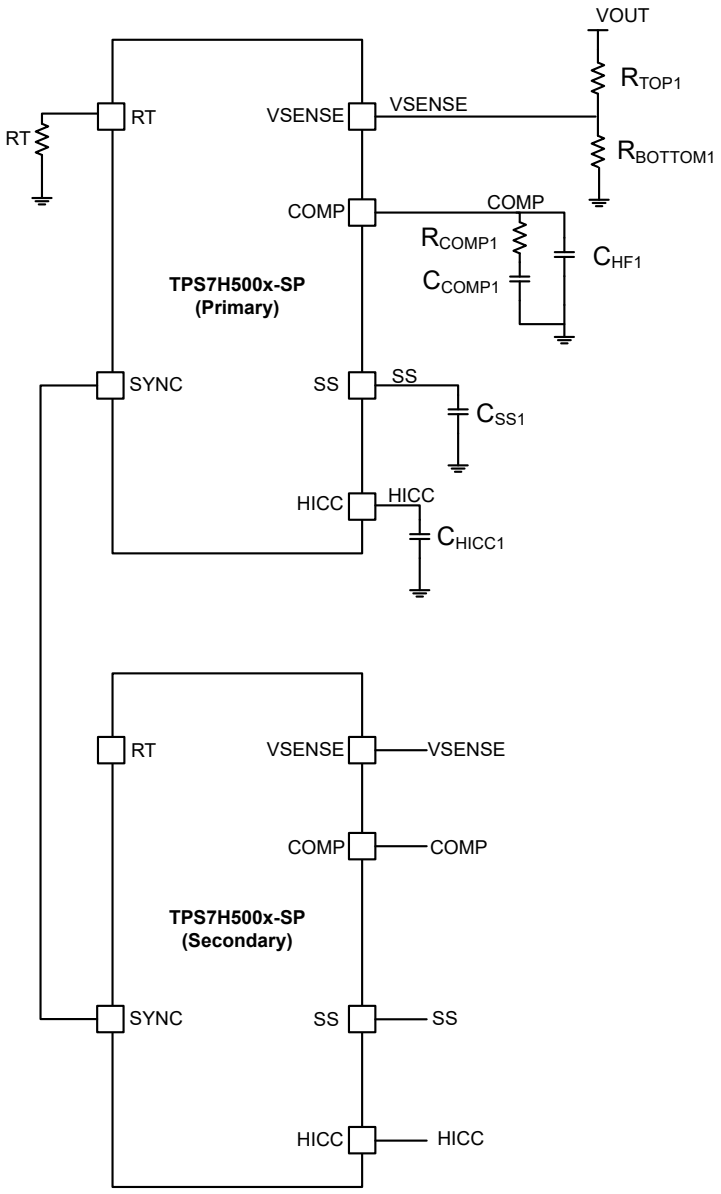


Figure 8-11. Primary-Secondary Mode Configuration for Parallel Operation

When using two controllers in primary-secondary mode, it is important to note that secondary controller will invert the clock signal that it receives from the primary controller. As such, there will be phase shift between the switching outputs of the primary and secondary controllers. This phase shift from an output (i.e. OUTA) on the primary controller to the corresponding output on the secondary controller will be 90° or 270°, depending on when the secondary device synchronizes to its clock input. Note that in Figure 8-12, the waveforms for OUTB are only applicable for TPS7H5001-SP and TPS7H5004-SP.

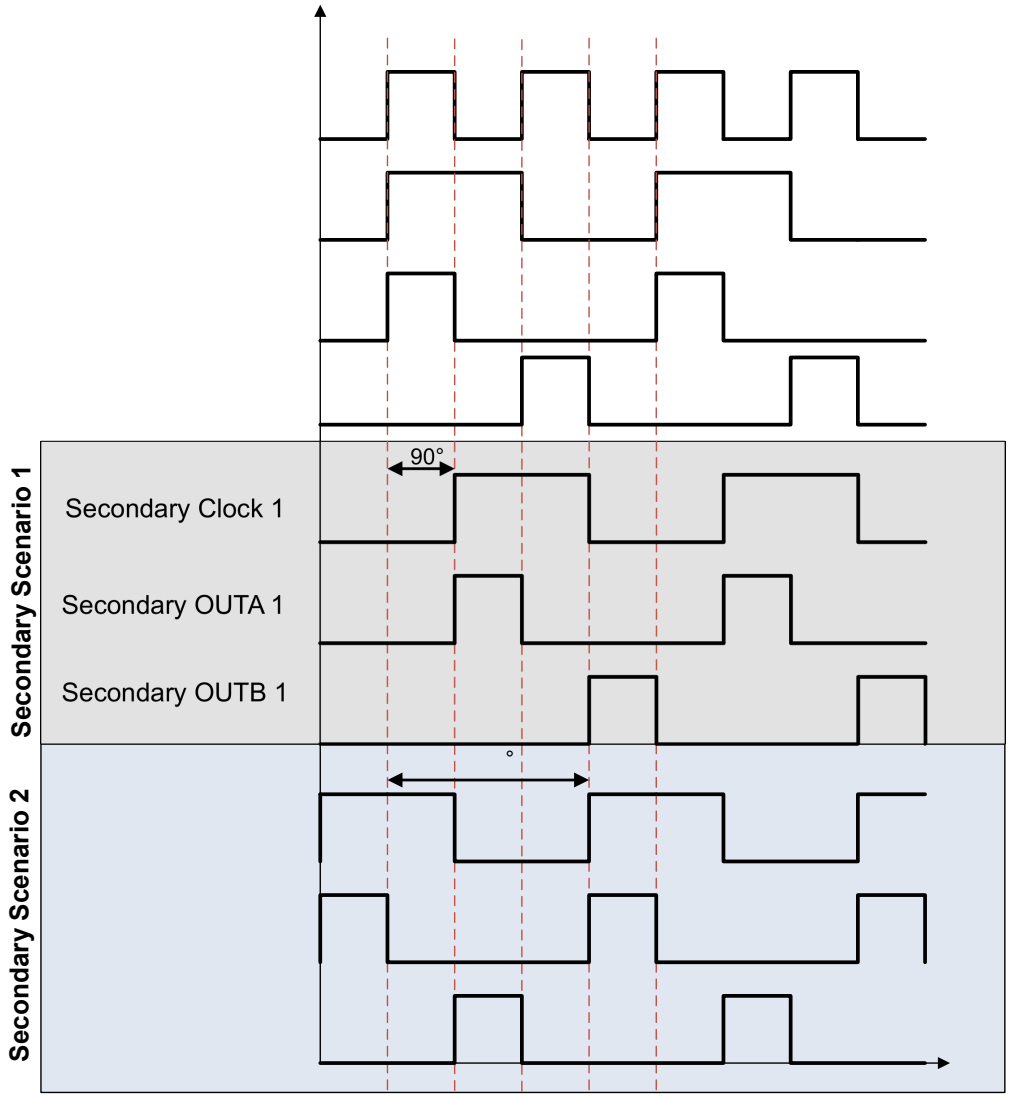


Figure 8-12. Switching Waveforms for Primary-Secondary Mode

The three operational modes for the controller are summarized in Table 8-1.

Table 8-1. Oscillator Modes and Configurations

MODE	RT	SYNC	SWITCHING FREQUENCY
Internal oscillator	Populated with resistor to AVSS.	Configured as output. Generates in-phase clock at twice the switching frequency.	Configurable from 100 kHz to 2 MHz depending on RT value.
External synchronization	Floating.	Configured as input. Accepts 200-kHz to 4-MHz external clock that is inverted internally.	Synchronized to SYNC input clock at 1/2 of the clock frequency. Switching is out-of-phase with external clock.
Primary-secondary	Populated with resistor to AVSS on primary device. Floating on secondary device.	Configured as output on primary device. Configured as input on secondary device. The SYNC pins of primary and secondary devices are connected.	Configurable from 100 kHz to 2 MHz depending on RT value of primary device. Secondary device switching is either 90° or 270° out-of-phase with primary device.

8.3.9 Primary Switching Outputs (OUTA/OUTB)

The controllers in the TPS7H500x-SP series either have a single primary output (OUTA) or dual primary outputs (OUTA and OUTB). Table 8-2 below shows the primary switching outputs that are available for each of the devices. Due to the roughly 150-mA peak current capability of each primary switching output, an external gate drive solution is recommended. For those controllers that support buck and single ended isolated applications (TPS7H5001-SP, TPS7H5002-SP, and TPS7H5003-SP), OUTA provides the gate control signal for the main switch in the topology. For push-pull and full-bridge applications, OUTA and OUTB both provide control signals for the main primary switches. Note that OUTB is only active when the duty cycle limit is set to 50% by connecting DCL pin to AVSS, and this DCL option is only valid for TPS7H5001-SP and TPS7H5004-SP (see *Duty Cycle Programmability* for more details). For the two output controller options, OUTA and OUTB are not perfectly matched and will vary based on the COMP voltage in a given switching cycle.

Table 8-2. Available Primary Output(s) for TPS7H500x-SP

DEVICE	OUTA	OUTB
TPS7H5001-SP	Yes	Yes
TPS7H5002-SP	Yes	No
TPS7H5003-SP	Yes	No
TPS7H5004-SP	Yes	Yes

8.3.10 Synchronous Rectifier Outputs (SRA and SRB)

For applications in which synchronous rectification (SR) is desired in order to increase overall converter efficiency, there are TPS7H500x-SP controllers with a single SR output (SRA) or dual SR outputs (SRA and SRB). Table 8-3 below shows the synchronous rectifier outputs that are available for each of the devices. Similar to the primary switching outputs, the peak current capability is roughly 150 mA and an external gate drive solution is recommended. The TPS7H5001-SP is the only controller in the series that contains the SRB output, and this output is only active when the duty cycle limit is set to 50% by connecting the DCL pin to AVSS. The SRA/SRB outputs will be off during the soft-start period and start switching when the voltage on SS exceeds 1 V. A small voltage transient may appear on the converter output when SRA/SRB become active.

Table 8-3. Available Synchronous Rectifier Output(s) for TPS7H500x-SP

DEVICE	SRA	SRB
TPS7H5001-SP	Yes	Yes
TPS7H5002-SP	Yes	No
TPS7H5003-SP	Yes	No
TPS7H5004-SP	No	No

8.3.11 Dead Time and Leading Edge Blank Time Programmability (PS, SP, and LEB)

While the TPS7H5003-SP has a fixed dead time (50 ns typical), the TPS7H5001-SP and TPS7H5002-SP allow for the user to program two independent dead times, TD_{SP} and TD_{PS}, as shown in Figure 8-13. This allows for the dead times to be optimized by the user in order to prevent shoot-though between the primary and synchronous switches while attaining the best possible converter efficiency. The dead time TD_{PS} between primary output (OUTA/OUTB) turn-off to synchronous rectifier (SRA/SRB) turn-on, can be programmed using a resistor from PS to AVSS. Likewise, the dead time TD_{SP} between synchronous rectifier turn-off and primary output turn-on is set using a resistor from SP to AVSS. The equation for determining the values of R_{PS} and R_{SP} required for a desired dead time is shown in Equation 8.

$$R_{PS} = R_{SP} = 1.207 \times DT - 8.858 \quad (8)$$

where:

- DT is the desired dead time in ns

- R_{PS} and R_{SP} are in kΩ

If the PS and SP pins are left floating, the dead time will be set to a minimum value of 8 ns (typical). When these pins are populated, it is recommended to use a minimum resistor value of 10 kΩ for R_{PS} and R_{SP}. The maximum resistor value to be used is 300 kΩ. As mentioned in *Soft-Start (SS)* and *Synchronous Rectifier Outputs (SRA and SRB)*, the SR outputs will be disabled during soft start, so the dead time is observed only after this sequence is complete.

After OUTA or OUTB goes high, a leading edge blank time is implemented to remove any transient noise from the current sensing loop. While the leading edge blank time is fixed (50-ns typical) for TPS7H5003-SP, the leading edge blank time for all other devices in the TPS7H500x-SP series is programmable by placing an external resistor from LEB to AVSS. This pin cannot be left floating and a minimum resistor value of 10 kΩ is required from LEB to AVSS. The maximum resistor value that should be used is 300 kΩ. The equation for determining the value of R_{LEB} for a desired leading edge blank time is shown in Equation 9.

$$R_{LEB} = 1.212 \times LEB - 9.484 \quad (9)$$

where:

- LEB is the desired leading edge blank time in ns
- R_{LEB} is in kΩ

Table 8-4. Dead Time and Leading Edge Blank Time Configurations for TPS7H500x-SP

DEVICE	DEAD TIME	LEADING EDGE BLANK TIME
TPS7H5001-SP	Resistor programmable	Resistor programmable
TPS7H5002-SP	Resistor programmable	Resistor programmable
TPS7H5003-SP	Fixed (50-ns typical)	Fixed (50-ns typical)
TPS7H5004-SP	Not applicable	Resistor programmable

In Figure 8-13, the dead times and leading edge blank times are shown for the switching waveforms. This figure also illustrates the minimum on-time of the device, which is comprised of the programmed blank time T_{LEB} and an internal logic delay t_d. Note that the dead-time waveforms for OUTB/SRB are only applicable for TPS7H5001-SP.

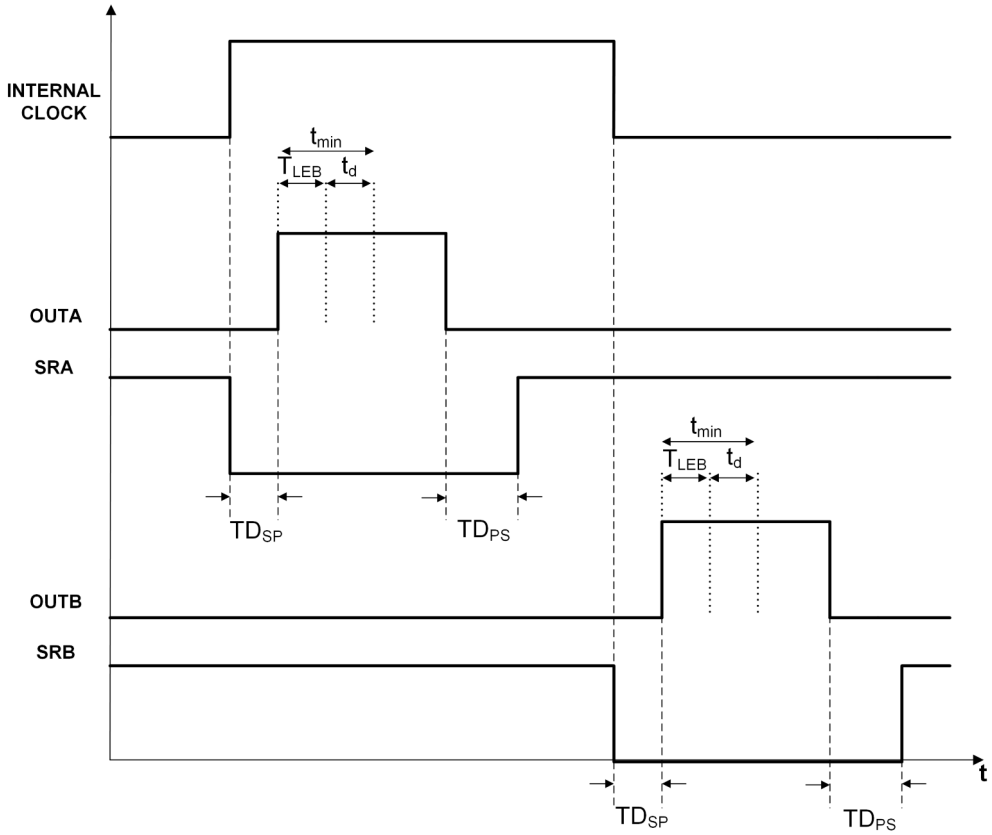


Figure 8-13. Outputs Timing Waveforms

8.3.12 Pulse Skipping

In order to prevent converter operational issues related to the minimum on-time of the controller, specifically during high frequency operation, a pulse skipping mode has been implemented for the TPS7H500x-SP controllers. During this mode, the primary outputs (OUTA/OUTB) will stop switching periodically. For the controllers with SR outputs, SRA/SRB remain on during pulse skipping if the soft-start period has ended. If the device enters into pulse skipping during the soft-start sequence, SRA/SRB remain off since the outputs are not yet active. Having a minimum on-time that is too long in duration during high frequency operation can lead to an issue such as inductor current runaway during the soft-start period. Pulse skipping allows for overcoming this issue by reducing the peak inductor current during the startup period. In high frequency converter designs where the V_{IN} to V_{OUT} ratio of the converter may lead to required duty cycles that are less than the minimum on-time, the controller outputs will skip pulses in order to maintain the required output voltage. Pulse skipping will occur when both of the following conditions are present:

- The voltage at the COMP pin is less than 0.3 V at the rising edge of the system clock
- The previous duty cycle was less than 25%

When the duty cycle limit of the controller is set to 50% and both OUTA and OUTB are active, the number of pulses skipped by each of the primary outputs will be equal. This will ensure the volt-second balance is maintained across the transformer and that flux-walking that leads to transformer saturation is avoided in isolated topologies such as the push-pull.

8.3.13 Duty Cycle Programmability

The TPS7H5001-SP, TPS75002-SP, and TPS7H5003-SP each have a configurable maximum duty cycle using the DCL pin. The TPS7H5004-SP only supports 50% maximum duty cycle and the DCL pin must be connected to AVSS. Table 8-5 shows the allowable maximum duty cycle limits for each device.

Table 8-5. Allowable Duty Cycle Limits for TPS7H500x-SP

DEVICE	DUTY CYCLE LIMIT OPTIONS
TPS7H5001-SP	50%, 75%, 100%
TPS7H5002-SP	75%, 100%
TPS7H5003-SP	75%, 100%
TPS7H5004-SP	50%

For applications in which 100% duty cycle is needed, the user should select one of the three compatible devices and connect DCL to VLDO. For other applications which require a duty cycle limit restriction, the DCL pin could be connected to AVSS for 50% duty cycle limit or left floating for 75% maximum duty cycle. Note that only TPS7H5001-SP and TPS7H5004-SP support the 50% duty cycle limit (DCL = AVSS), and OUTB/SRB are only active in this configuration. The 50% duty cycle limit case is intended to support applications such as the push-pull that require two primary switching outputs, and in the case of the TPS7H5001-SP, two synchronous rectification outputs. If the controller is being operated in external synchronization mode, the most precise duty cycle limiting results are obtained when the applied system clock has a 50% duty cycle. Specifically, for the case when the duty cycle limit is set to 75% (DCL = floating) in the supported devices, there may be some variation of the duty cycle limit that is dependent on the duty cycle of the external clock applied at SYNC.

Table 8-6. DCL Pin Configurations

MAXIMUM DUTY CYCLE (NOMINAL)	DCL CONNECTION
100%	VLDO
75%	Floating
50%	AVSS

8.3.14 Current Sense and PWM Generation (CS_ILIM)

The CS_ILIM pin is driven by a signal representative of the transformer primary-side current. The current signal has to have compatible input range of the COMP pin. As shown in Figure 8-14, the COMP pin voltage is used as the reference for the peak current. Note that the OUTB waveform is only applicable for TPS7H5001-SP and TPS7H5004-SP. The primary side signals, OUTA/OUTB, are turned on by the internal clock signal and turned off when sensed peak current reaches the COMP/2 pin voltage. The CS_ILIM pin is also used to configure the current limit for the controller.

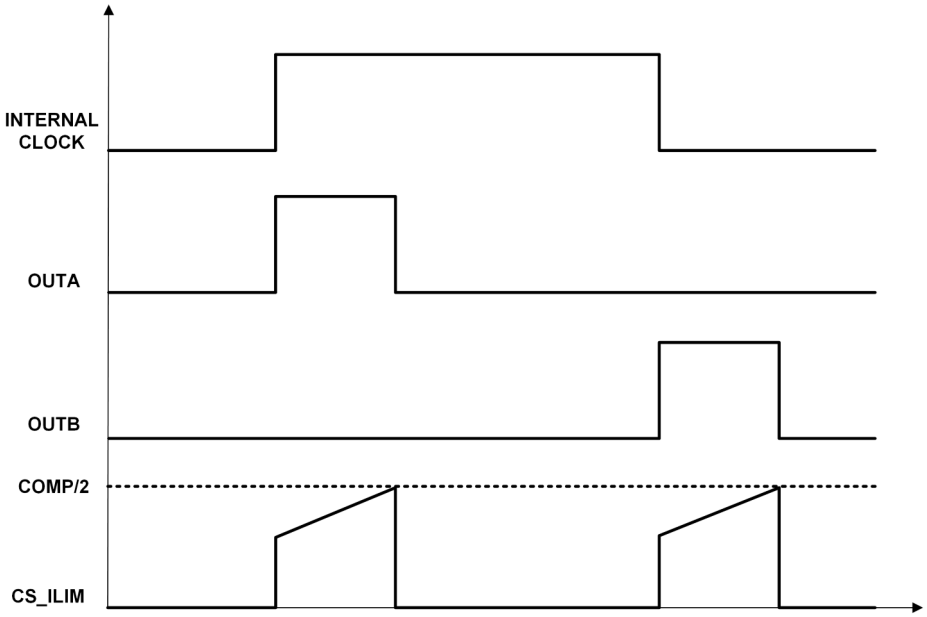


Figure 8-14. Peak Current Mode Control and PWM Generation

A resistor is needed from CS_ILIM to AVSS is used to detect current for both proper PWM operation and overcurrent protection. The current limit threshold V_{CS_ILIM}, is specified as 1.05 V (nominal) in the electrical specifications. This indicates that when the voltage on this pin reaches this threshold, the device will go into hiccup mode. Equation 10 shows the calculation for determining the value of the sense resistor for a selected current limit.

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \tag{10}$$

Note that the value of I_{LIM} has to account for where and how the current is being sensed. For a forward converter with sense resistor between source of primary FET to AVSS, I_{LIM} will be referred to the primary side of the converter.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_S}{N_P} \tag{11}$$

Equation 11 shows the calculation for determining I_{LIM} in the design of a forward converter, where:

- $I_{L,PEAK}$ is the peak output inductor current desired to activate the overcurrent protection
- N_S is the number of secondary turns for the power transformer
- N_P is the number of primary turns for the power transformer

In the design of a buck converter which senses the high side current via a current sense transformer, Equation 12 can be used for determining I_{LIM} for this instance.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_{CSP}}{N_{CSS}} \tag{12}$$

In this equation:

- $I_{L,PEAK}$ is the peak output inductor current desired to activate the overcurrent protection
- N_{CSP} is the number of primary turns of the current sense transformer
- N_{CSS} is the number of secondary turns of the current sense transformer

Regardless of the topology, the user should ensure that there is sufficient margin between the peak current during normal operation and the overcurrent trip point when determining the value of R_{CS}.

8.3.15 Hiccup Mode Operation (HICC)

Once the voltage at CS_ILIM exceeds 1.05 V, the device will execute cycle-by-cycle current limiting. The controller output is turned on at the beginning of each cycle until such point that CS_ILIM voltage reaches the current sense threshold V_{CS_ILIM}, when the output is turned off. At the same time, each time the voltage at CS_ILIM reaches 1.05 V, the capacitor at C_{HICC} is charged via a 80-µA current (hiccup delay current). This hiccup delay current is terminated at the end of the clock cycle. As long as there is still an overcurrent being detected, the cycle-by-cycle limiting will continue until the voltage on C_{HICC} reaches 0.6 V. This cycle-by-cycle limiting period is referred to as the delay mode. As such, the capacitor C_{HICC} can be chosen to dictate the amount of time that the controller will spend in delay mode.

$$C_{HICC} = \frac{t_{delay} \times 80\ \mu A}{0.6\ V} \tag{13}$$

Note that this equation is an approximation since:

- depending on the system behavior and if C_{HICC} has been charged previously, C_{HICC} may not start at 0 V as assumed by the equation
- the 80-µA charging current is a pulsed current, the duration of which will be dictated by the nature of the overcurrent (that is,. when the current sense threshold is reached during each clock cycle)

After the voltage on HICC pin reaches 0.6 V, the SS pin of the controller is discharged and switching stops. The voltage on HICC is then quickly pulled up to 1 V with the pull-up current limited to approximately 1 mA. Once HICC voltage reaches 1 V, the 1-µA hiccup restart current begins to discharge C_{HICC}. The controller will not switch until HICC voltage falls to 0.3 V. Once the voltage falls to 0.3 V, the controller will initiate its soft-start sequence again. If the overcurrent has disappeared, normal operation will resume. The hiccup time, which is the entire non-switching period, can be calculated using Equation 14.

$$t_{HICC} = \frac{C_{HICC} \times (1\ V - 0.3\ V)}{1\ \mu A} \tag{14}$$

In summary, the capacitor C_{HICC} on the HICC pin controls the amount of time the controller spends performing cycle-by-cycle limiting before switching stops, and also controls the amount of time switching is disabled before re-start is attempted again. It is recommended to use a minimum of 3.3 nF for C_{HICC}. Figure 8-15 shows the typical behavior during hiccup mode. Note that the OUTB and corresponding CS_ILIM waveforms are only applicable for TPS7H5001-SP and TPS7H5004-SP.

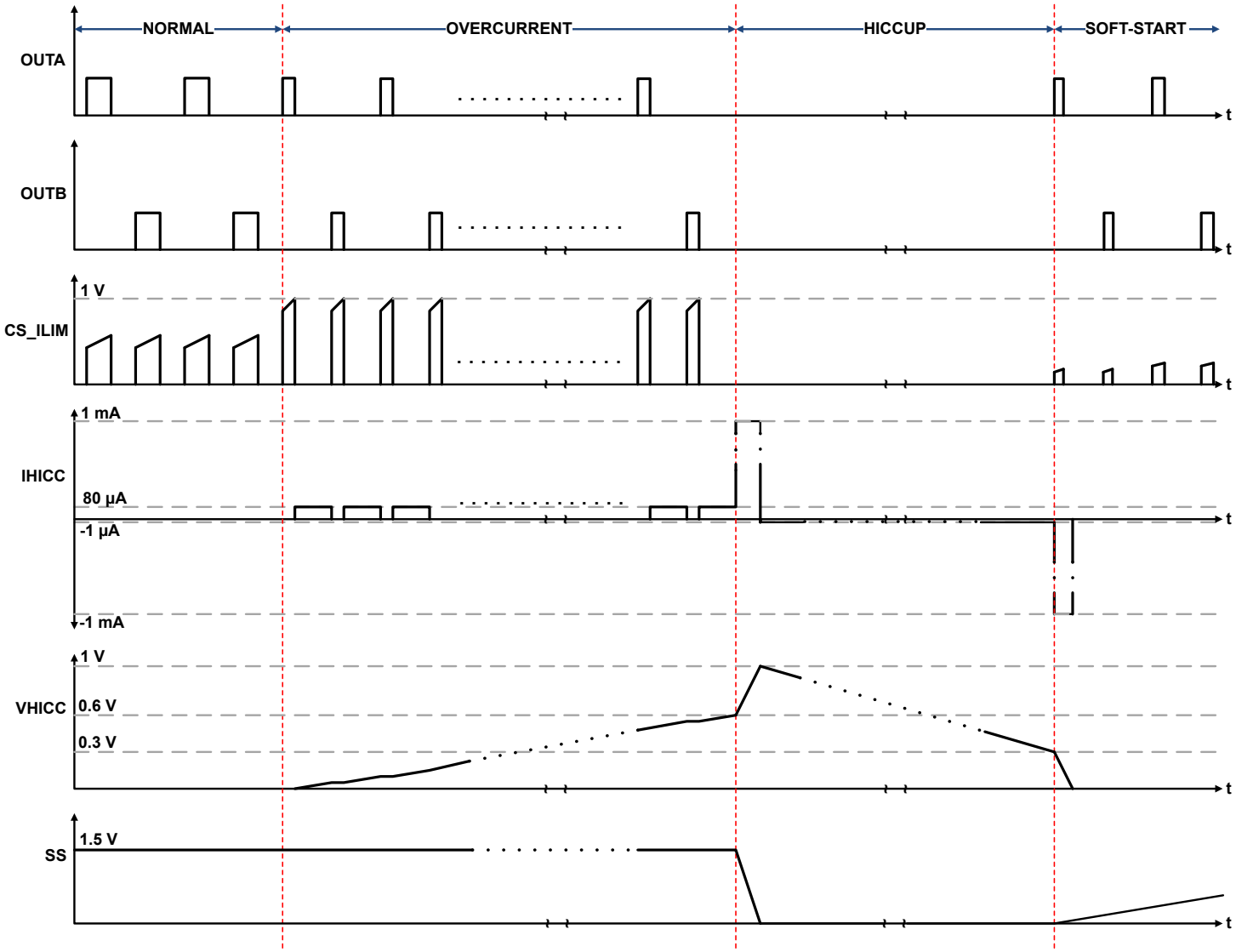


Figure 8-15. Cycle-by-Cycle Current Limit Delay Timer and Hiccup Restart Timer

8.3.16 External Fault Protection (FAULT)

The FAULT pin provides the user with flexibility to implement additional protections for the converter, such as input overcurrent protection or overvoltage protection, if desired. This pin can also be utilized in the event that the user desires more stringent protections than what is offered by the controller (i.e. thermal shutdown). The user can design external logic circuitry to generate the signal necessary to drive this pin based on the protection function. If the voltage on the FAULT pin exceeds 0.6 V (typical) for a duration specified by the FAULT minimum pulse width, a fault shutdown will occur. This FAULT minimum pulse width duration, which is between 0.4 µs and 1.4 µs, is intended to prevent any spurious triggering due to short-term transients. Since any short-term transient event detected on this pin that is less than 1.4 µs in duration may not activate the FAULT pin, these events should be properly evaluated by the user in order to determine the impact to the overall system. Once the fault is detected, the SS pin is discharged and the controller outputs stop switching and stay low as long as the rising threshold is exceeded on the pin. Once the fault has subsided and the voltage of FAULT falls below the falling threshold of 0.5 V (typical), the TPS7H500x-SP enters a delay period that is dependent on the switching frequency. This delay is appoximately equal to 15 switching frequency cycles in addition to an internal logic delay. The soft-start sequence is again initiated after the delay period has finished. Equation 15 can be used to determine the length of the fault delay.

$$t_{dFLT} = \frac{14700}{f_{sw}} + 2 \quad (15)$$

In this equation:

- t_{dFLT} is the fault delay duration in µs
- f_{sw} is the switching frequency in kHz

If the FAULT threshold is exceeded during the delay, the entire sequence is started again. Figure 8-16 shows the switching waveforms when the fault mode has been activated in the controller. Note that the OUTB waveforms are only applicable for TPS7H5001-SP and TPS7H5004-SP.

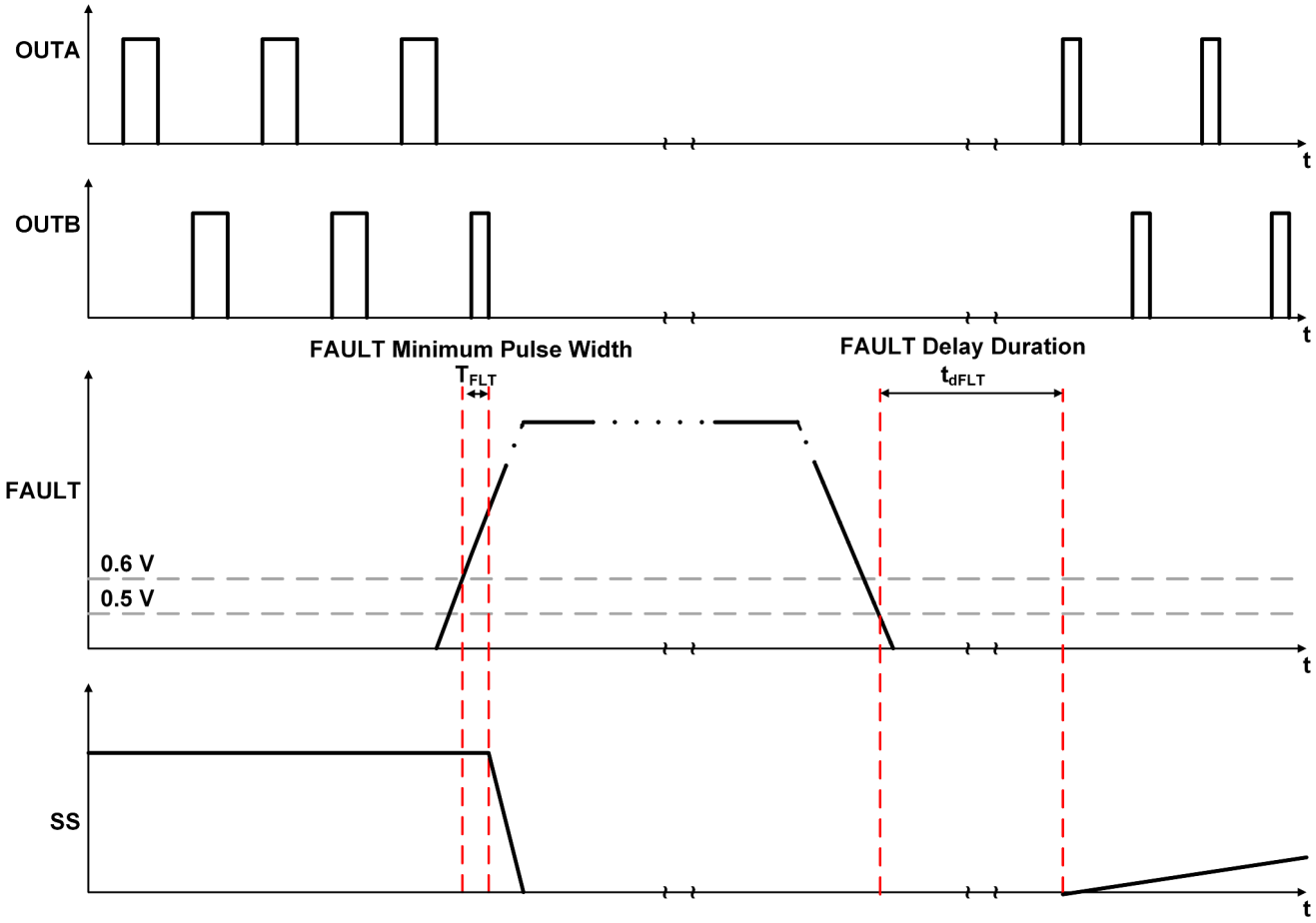


Figure 8-16. Switching Waveforms During Fault Mode

8.3.17 Slope Compensation (RSC)

When utilizing peak current mode control in switching power converter design, the converter can enter into an unstable state when the duty cycle for the main power switch rises above 50%. Essentially, the converter will be in a state where the error between the peak current and average current increases with each subsequent switching cycle. This instability, known as subharmonic oscillation, can be mitigated by adding slope compensation. For the TPS7H500x-SP, the slope compensation is in the form of a voltage ramp that is subtracted from the error amplifier output divided down by the parameter CCSR (COMP to CS_LIM ratio). The minimum slope compensation for stability over the entire duty cycle range is equal to 0.5 × *m*, where *m* is the inductor falling current slope. The recommended slope compensation is 1 × *m*, as any increase above this value will not improve stability.

For a typical buck converter, setting the slope compensation equal to the downward slope of the sensed current waveform yields the calculation in Equation 16.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \quad (16)$$

where:

- SC is the slope compensation value in V/µs
- L is the output inductor value in µH
- N_{CSP} is the number of primary turns of the current sense transformer
- N_{CSS} is the number of secondary turns on the current sense transformer
- R_{CS} is the value of the current sense resistor in Ω

If no current sense transformer is used, set N_{CSP} / N_{CSS} to 1.

The slope compensation for the forward converter will be similar with the note that the sensed current waveform would also need to take into account the turns ratio of the main power transformer.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \quad (17)$$

where:

- N_S is the number of secondary turns of the power transformer
- N_P is the number of primary turns of the power transformer

For the TPS7H500x-SP controllers, a resistor from the RSC pin to AVSS can be used to set the desired slope compensation. Equation 18 shows the calculation for determining the proper resistor value for RSC.

$$RSC = \frac{28.3}{SC^{1.1}} \quad (18)$$

where:

- SC is the desired slope compensation is V/µs
- RSC is in kΩ

8.3.18 Frequency Compensation

Since the TPS7H500x-SP uses a transconductance error amplifier (OTA), either Type 2A or Type 2B frequency compensation can be applied. The primary difference between the two compensation schemes is that Type 2A has an additional capacitor C_{HF} in parallel with R_{COMP} and C_{COMP} in order to provide high-frequency noise attenuation. These components will be connected between the COMP pin of the controller, which is the OTA output, and AVSS.

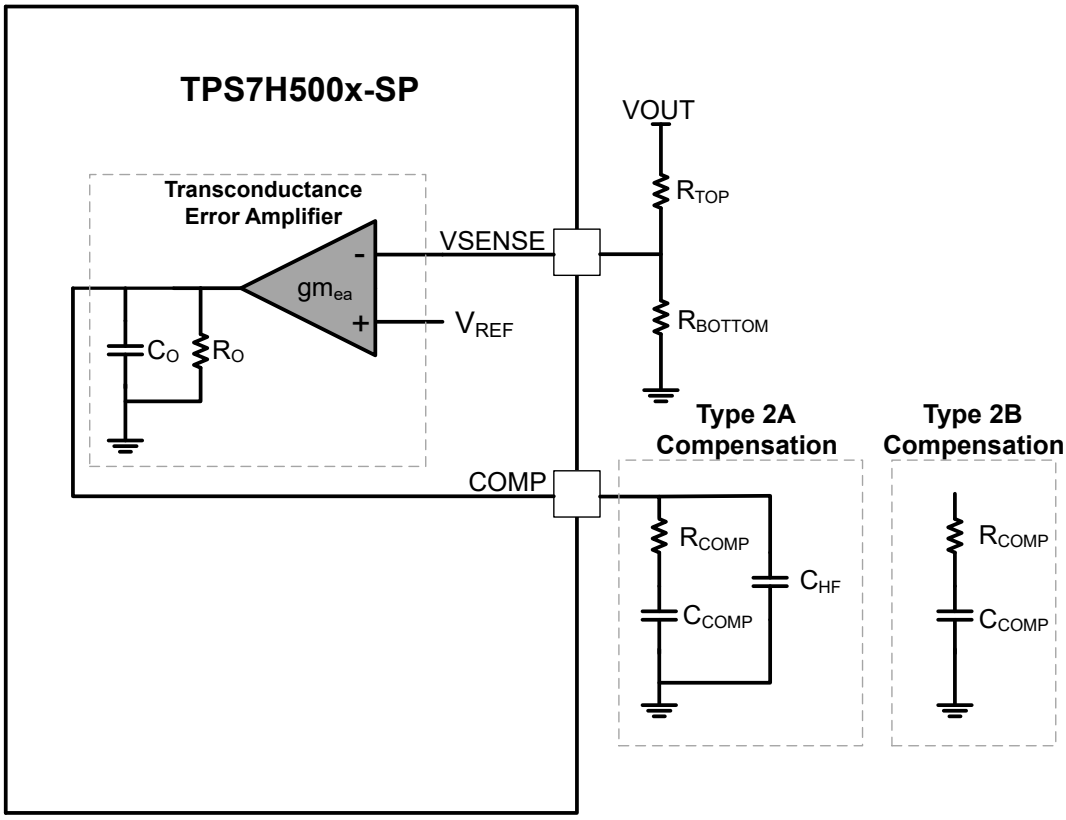


Figure 8-17. TPS7H500x-SP Frequency Compensation Options

For any of the topologies supported by the TPS7H500x-SP, the following procedure and equations can be used to select the compensation components. All parameters in the equations are in standard units unless otherwise indicated (that is, H for inductance, F for capacitance, Hz for frequency, and so on).

1. Select the desired crossover frequency (f_c) for the converter.
2. Calculate R_{COMP} based on the selected crossover frequency f_c.

1.
$$R_{COMP} = \frac{2\pi \times f_c \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{PS}} \quad (19)$$

where:

- gm_{ea} is the error amplifier transconductance of 1800 × 10^{-6} A/V (typical)
- V_{REF} is the 0.613 V reference voltage (typical)
- gm_{PS} is the power stage transconductance (see Equation 23)

2. Calculate C_{COMP} to place compensation zero at the location of the power stage dominant pole.

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}} \quad (20)$$

3. Determine the output capacitor ESR zero location (optional).

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (21)$$

4. Select the capacitor C_{HF} to provide a high frequency pole to compensate for the ESR zero (optional).

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{ESR}} \quad (22)$$

For different power converter topologies, the primary change to the compensation selection procedure will be the determination of the power stage transconductance gm_{PS}. The power stage transconductance can be calculated as shown in Equation 23.

$$gm_{PS} = \frac{N_P \times N_{CSS}}{CCSR \times R_{CS} \times N_S \times N_{CSP}} \quad (23)$$

where:

- N_P is the number of primary turns on the main power transformer (set to 1 if no transformer is used)
- N_S is the number of secondary turns on the main power transformer (set to 1 if no transformer is used)
- N_{CSP} is the number of primary turns on the current sense transformer (set to 1 if no transformer is used)
- N_{CSS} is the number of secondary turns of the current sense transformer (set to 1 if no transformer is used)
- R_{CS} is the selected value of the current sense resistor
- CCSR is the ratio to COMP of CS_ILIM

Note that for the TPS7H500x-SP controllers, the sensed current waveform is compared to the voltage at COMP divided down by the factor CCSR at the PWM comparator, which is accounted for in the denominator of the equation. For buck converters, all turns for the main power transformer can be set equal to 1 and the equation still applies.

8.3.19 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 160°C (typical).

8.4 Device Functional Modes

The TPS7H500x-SP series uses fixed frequency, peak current mode control. Each controller regulates the peak current and duty cycle of the converter. The internal oscillator initiates the turn-on of the primary output used as the gate driver input for the power switch. The external power switch current is sensed through an external resistor and compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors. When the sensed current reaches the stepped down COMP voltage, the power switch is then turned off.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H500x-SP series is a family of radiation-hardness-assured current mode PWM controllers that can be utilized for designing space-grade DC-DC converters. Each device should be paired with external gate drivers in order to provide control of the power semiconductor device(s) of the converter power stage. By allowing for switching frequencies up to 2 MHz, the controllers provide many advantages for GaN power semiconductor based designs. The TPS7H500x-SP family can be used for the design of a number of common DC-DC converter topologies, including but not limited to: buck, flyback, forward, active-clamp forward, push-pull, and full-bridge.

9.2 Typical Application

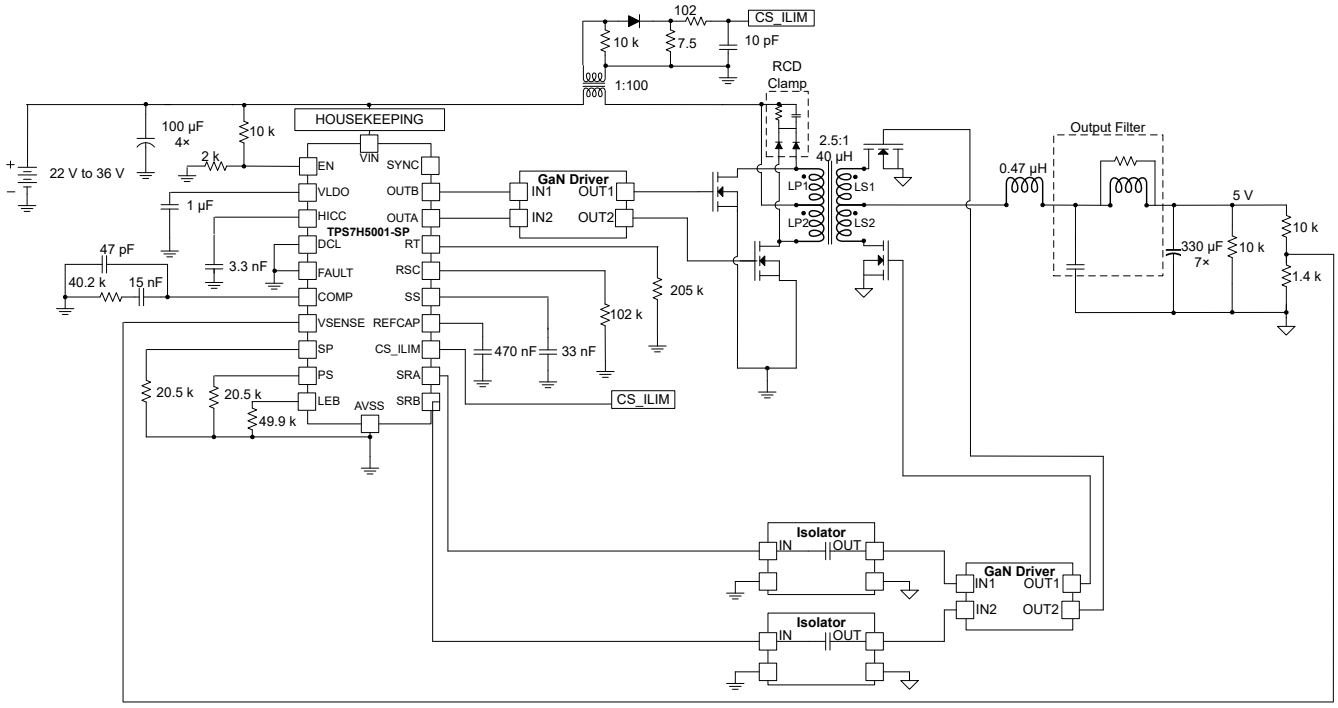


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The example provided here is to demonstrate how to design a synchronous push-pull converter using GaN power semiconductor devices. This design example is to show how to determine the component selection for the TPS7H5001-SP as well as key components of the converter power stage.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Output voltage	5 V
Maximum output current	20 A
Output current pre-load	0.5 mA
Operating temperature	25°C
Switching frequency	500 kHz
Peak input current limit	14 A
Target bandwidth	~10 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Switching Frequency

The synchronous push-pull converter was designed to operate at a switching frequency of 500 kHz. For space-grade converter designs, the benefits of GaN power devices over silicon counterparts are readily apparent at this switching frequency. Using Equation 7, the required RT resistor for the desired frequency can be determined as shown in Equation 24.

$$\mathrm{RT} = \frac{112000}{500} - 19.7 = 204.3\ \mathrm{k} \tag{24}$$

A standard resistor value of 205 kΩ is selected for the design.

9.2.2.2 Output Voltage Programming Resistors

The converter has an output voltage of 5 V. The feedback resistor divider connected to VSENSE should be selected to correspond to the selected V_{OUT}. With a resistor of 10 kΩ selected for R_{TOP}, the value of the bottom resistor in the divider can be calculated.

$$\mathrm{R_{BOTTOM}} = \frac{\mathrm{V_{REF}}}{\mathrm{V_{OUT}} - \mathrm{V_{REF}}} \times \mathrm{R_{TOP}} \tag{25}$$

$$\mathrm{R_{BOTTOM}} = \frac{0.613\ \mathrm{V}}{5\ \mathrm{V} - 0.613\ \mathrm{V}} \times 10\ \mathrm{k\Omega} = 1.397\ \mathrm{k\Omega} \tag{26}$$

The values for R_{TOP} and R_{BOT} needed are 10 kΩ and 1.4 kΩ, respectively.

9.2.2.3 Dead Time

For GaN power semiconductor devices, a key characteristic that has to be taken into consideration is the voltage drop of the GaN FET while it is operating in reverse conduction mode. While the GaN FET does not have a body diode that is inherent in the silicon FET, it does still have the ability to conduct current in the reverse direction with behavior that is similar to a diode. When conducting in the reverse direction, the source-drain voltage of the GaN FET can be quite large. Thus, to reduce the dead-time losses and maximize efficiency, the dead time was set to a value of approximately 25 ns. Based on the selected value, Equation 8 can be used to calculate the resistors needed to attain the desired dead time.

$$\mathrm{R_{PS}} = \mathrm{R_{SP}} = 1.207 \times 25 - 8.858 = 21.3\ \mathrm{k} \tag{27}$$

The standard resistor value of 20.5 kΩ was selected for both R_{PS} and R_{SP}.

9.2.2.4 Leading Edge Blank Time

The leading edge blank time was initially chosen to be roughly 50 ns. This value was the initial approximation based on any ringing or transient spikes that were expected to be seen on the sensed current waveform at the CS_ILIM pin. Using Equation 9 , the value of R_{LEB} was calculated from this desired value.

$$R_{LEB} = 1.212 \times 50 - 9.484 = 51.1\ k \tag{28}$$

The value of R_{LEB} selected was 49.9 kΩ. Note that the ringing and transient spikes on the sensed current waveform will depend heavily on component placement and parastics in the PCB layout. The leading edge blank time should also account for any propagation delay that is inherent to the gate driver being used in the application. As such, the value of R_{LEB} may need to be optimized as the design is tested in accommodate for these factors. Recall that the leading edge blank time is also correlated to the minimum on-time of the device, and extending this value significantly may become a limiting factor for the maximum switching frequency that can be achieved in the design.

9.2.2.5 Soft-Start Capacitor

For this design, the soft-start time is arbitrary. The value of the soft-start capacitor selected was 33 nF. Based on this value, the soft-start time can be calculated.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \tag{29}$$

$$t_{SS} = \frac{33\ nF \times 0.613\ V}{2.7\ \mu A} = 7.49\ ms \tag{30}$$

The soft-start time is ~7.5 ms for the design.

9.2.2.6 Transformer

The turns ratio and primary inductance of the transformer will be determined based on the target specifications of the converter. In order to calculate the maximum allowable turns ratio, a duty cycle limit must be selected for the design. Even though DCL will be connected to AVSS to impose a 50% duty cycle limit from the controller to ensure there is no overlap of the primary switching outputs, a maximum duty cycle of approximately 35% is targeted for the design in order to provide sufficient margin to the controller limit. This is due to the fact that the actual duty cycle is greater than calculated duty cycle when accounting for the converter efficiency, and to allow for duty cycle increases during load transient events. Equation 31 provides the formulate needed to calculate the maximum turns ratio for this design.

$$N_{PS\_MAX} = \frac{2 \times V_{IN\_MIN} \times D_{LIM}}{V_{OUT} + V_{SR}} \tag{31}$$

V_{SR} is estimated to be 0.5 V for the application and D_{LIM} is 35% duty cycle limit that was selected. N_{PS_MAX} is calculated using the values in Equation 32.

$$N_{PS\_MAX} = \frac{2 \times 22\ V \times 0.35}{5\ V + 0.5\ V} = 2.8 \tag{32}$$

A value of 2.5 is selected for the turns ratio for the design.

In order to design for the primary inductance of the transformer, the magnetizing current must be selected. The value of the magnetizing current is a trade-off between transformer size and efficiency, with larger magnetizing current leading to a smaller size due to lower required inductance, but also leading to lower efficiency. A magnetizing current equal to 6% of the output current was initially targeted for this design. With this value, the primary inductance can be calculated using Equation 36. The minimum duty cycle expected is needed for this

calculation can be determined using Equation 34, where the estimated efficiency η for the converter used in the calculation is 85%.

$$D_{MIN} = \frac{V_{OUT} + V_{SR}}{2 \times V_{IN\_MAX} \times N_{SP} \times} \quad (33)$$

$$D_{MIN} = \frac{5\ V + 0.5\ V}{2 \times 36\ V \times 0.4 \times 0.85} = 0.22 \quad (34)$$

$$L_P = \frac{N_{PS} \times V_{IN\_MAX} \times D_{MIN}}{f_{sw} \times I_{MAG}} \quad (35)$$

$$L_P = \frac{2.5 \times 36\ V \times 0.22}{500\ kHz \times 0.06 \times 20\ A} = 33\ \ H \quad (36)$$

Though the calculated value of L_P is 33 µH, it may often be challenging to find the exact primary inductance value needed for the transformer design. As such, an inductance of 40 µH was used in the actual design.

The following equations detail the how to calculate transformer primary and secondary currents that are critical for proper design of the transformer. These equations are useful for defining the physical structure of the transformer. Note that these are ideal equations, and the final design should be optimized depending on the application.

$$I_{SEC\_MAX} = I_{OUT} + \frac{\Delta I_L}{2} \quad (37)$$

$$I_{SEC\_MAX} = 20 + \frac{8.51\ A}{2} = 24.25\ A \quad (38)$$

$$I_{PRI\_MAX} = \frac{I_{SEC\_MAX} + (0.5 \times I_{MAG})}{N_{PS}} \quad (39)$$

$$I_{PRI\_MAX} = \frac{24.25\ A + (0.5 \times 0.06 \times 20\ A)}{2.5} = 9.94\ A \quad (40)$$

$$I_{SEC\_MAX\ (VIN\_MIN)} = \frac{I_{OUT} + \left(D_{MAX} \times \left(\frac{V_{IN\_MIN}}{N_{PS}} - V_{OUT} - V_{SR}\right)\right)}{2 \times f_{sw} \times L_{OUT}} \quad (41)$$

$$I_{SEC\_MAX\ (VIN\_MIN)} = \frac{20\ A + \left(0.37 \times \left(\frac{22\ V}{2.5} - 5\ V - 0.5\ V\right)\right)}{2 \times 500\ kHz \times 0.47\ \mu H} = 22.58\ A \quad (42)$$

$$I_{PRI\_MAX\ (VIN\_MIN)} = \frac{I_{SEC\_MIN\ (VIN\_MIN)} + (0.5 \times I_{MAG})}{N_{PS}} \quad (43)$$

$$I_{PRI\_MAX\,(VIN\_MIN)} = \frac{17.42\ A + (0.5 \times 0.06 \times 20\ A)}{2.5} = 9.27\ A \tag{44}$$

$$I_{SEC\_MIN\,(VIN\_MIN)} = \frac{I_{OUT} - \left(D_{MAX} \times \left(\frac{V_{IN\_MIN}}{N_{PS}} - V_{OUT} - V_{SR}\right)\right)}{2 \times f_{sw} \times L_{OUT}} \tag{45}$$

$$I_{SEC\_MAX\,(VIN\_MIN)} = \frac{20\ A - \left(0.37 \times \left(\frac{22\ V}{2.5} - 5\ V - 0.5\ V\right)\right)}{2 \times 500\ kHz \times 0.47\ \mu H} = 17.42\ A \tag{46}$$

$$I_{PRI\_MIN\,(VIN\_MIN)} = \frac{I_{SEC\_MIN\,(VIN\_MIN)} - (0.5 \times I_{MAG})}{N_{PS}} \tag{47}$$

$$I_{PRI\_MIN\,(VIN\_MIN)} = \frac{17.42\ A - (0.5 \times 0.06 \times 20\ A)}{2.5} = 6.73\ A \tag{48}$$

$$t_{ON\_MAX} = \frac{(V_{OUT} + V_{SR}) \times N_{PS}}{2 \times f_{sw} \times V_{IN\_MIN}} \tag{49}$$

$$t_{ON\_MAX} = \frac{(5\ V + 0.5\ V) \times 2.5}{2 \times 500\ kHz \times 22\ V} = 0.63\ \mu s \tag{50}$$

& ( ) #) – #) ( ) #)
,) # & (51)

$$m_{PRI} = \frac{9.27\ A - 6.73\ A}{0.63\ \mu s} = 4072130.16\ \frac{A}{s} = 4.07\ \frac{A}{\mu s} \tag{52}$$

$$I_{PRI\_RMS} = \sqrt{D_{MIN} \times \left(\frac{\left(m_{PRI} \times t_{ON\_MAX}\right)^2}{3} + \left(\frac{m_{PRI}}{2} \times I_{PRI\_MIN\,(VIN\_MIN)} \times t_{ON\_MAX}\right) + I_{PRI\_MIN\,(VIN\_MIN)}{}^2\right)} \tag{53}$$

$$I_{PRI\_RMS} = \sqrt{0.22 \times \left(\frac{\left(4072130.16\frac{A}{s} \times 0.63\ \mu s\right)^2}{3} + \left(\frac{4072130.16\frac{A}{s}}{2} \times 6.73\ A \times 0.63\ \mu s\right) + 6.73\ A^2\right)} = 3.55\ A \tag{54}$$

9.2.2.7 Main Switching FETs

In the push-pull topology, the switching devices on the primary side will see a voltage that is equal to twice that of the input when the devices are off. As such, the GaN FETs selected should have a voltage rating that 3 times higher than the input voltage. The voltage rating for the GaN FETs was conservatively chosen for the primary side as 170 V for this application based on maximum input voltage of 36 V. This was to account for any transient spikes that were seen during operation. Also ensure that the GaN FETs are properly sized based on the primary current calculations in Section 9.2.2.6.

9.2.2.8 Synchronous Rectificier FETs

The maximum voltage stress that will be seen by the synchronous rectifier switch on the secondary side can be calculated using Equation 55.

$$\text{"} \quad \text{"} \; ' \; \frac{()\quad ,}{)\ -} \tag{55}$$

$$V_{SR\_STRESS} = 5\ V + \frac{36\ V}{2.5} = 19.4\ V \tag{56}$$

Note that the maximum expected voltage is approximately 20 V, but a higher rating should be selected to allow for transient spikes. For the design, an 80-V rated GaN FET was conservatively chosen for the synchronous rectifier. The current rating should be sufficient to handle the maximum secondary current as calculated in Section 9.2.2.6. In order to reduce the current through GaN FET during the soft-start period, when the controller SRA and SRB signals are off, a Schottky diode can be used in parallel with the synchronous rectifier GaN FETs. This diode would also mitigate the reverse conduction losses attributed to the GaN FET during the dead time and boost the overall efficiency of the system.

9.2.2.9 RCD Clamp

A resistor-capacitor-diode clamp circuit can be used to limit the voltage at the switch node. The equations below can be used to determine initial values for the resistor and capacitor, but the circuit will need to be optimized through testing. First, calculate the clamp voltage by determining how much overshoot is allowable at the switch node.

$$V_{CLAMP} = K_{CLAMP} \times N_{PS} \times (V_{OUT} + V_{SR}) \tag{57}$$

The parameter K_{CLAMP} defines the target overshoot value. For example, set K_{CLAMP} to 1.5 for 50% allowable overshoot.

Next, the leakage inductance L_L and peak primary current I_{PRI_MAX} of the transformer can be used to approximate the clamp resistor. The clamp capacitor value can be determined thereafter. Note that ΔV_{CLAMP} defines the allowable ripple for the clamp capacitor.

$$R_{CLAMP} = \frac{{V_{CLAMP}}^2}{0.5 \times L_L \times {I_{PRI\_MAX}}^2 \times \frac{V_{CLAMP}}{V_{CLAMP} - (N_{PS} \times (V_{OUT} + V_{SR}))} \times f_{sw}} \tag{58}$$

$$C_{CLAMP} = \frac{V_{CLAMP}}{\Delta V_{CLAMP} \times V_{CLA\,MP} \times R_{CLAMP} \times f_{sw}} \tag{59}$$

9.2.2.10 Output Inductor

For the output inductor, a ripple current of 40% was targeted for the design. Based on the selected ripple current, Equation 60 can be used to determine the output inductor value. K_L is the current ripple factor, which will be set to 0.4 in this instance.

$$L_{OUT} = \frac{\left(\frac{V_{IN\_MAX}}{N_{PS}} - V_{OUT} - V_{SR}\right) \times D_{MIN}}{f_{sw} \times K_L \times I_{OUT}} \tag{60}$$

$$L_{OUT} = \frac{\left(\frac{36\ V}{2.5} - 5\ V - 0.5\ V\right) \times 0.22}{500\ kHz \times 0.4 \times 20\ A} = 0.5\ \mu H \tag{61}$$

The value of the inductor selected for the design is 0.47 µH.

9.2.2.11 Output Capacitance and Filter

Generally, there are two different calculations that can be used to determine the output capacitance required for the converter. The first calculates the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient as shown in Equation 62. The second, shown in Equation 64, determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design. Once the two different calculations are performed, the maximum of these should be chosen as the output capacitance for the design. The calculations are shown for target voltage ripple of 2% of the output voltage and maximum allowable voltage deviation of 2.5% of the output voltage.

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \times \Delta V_{OUT} \times f_c} \tag{62}$$

$$C_{OUT} > \frac{10\ A}{2\pi \times 0.025 \times 5\ V \times 10\ kHz} = 1.27\ mF \tag{63}$$

$$C_{OUT} > \frac{I_{OUT} \times 2 \times D_{MAX}}{V_{RIPPLE} \times f_{sw}} \tag{64}$$

$$C_{OUT} > \frac{I_{OUT} \times 2 \times 0.37}{0.02 \times 5\ V \times 500\ kHz} = 294.12\ \mu F \tag{65}$$

Based on the calculations, at least 1.3 mF of output capacitance is required. When selecting capacitors, consider any derating of capacitance that is needed to account for aging, temperature, and DC bias.

For space-grade converter designs, there is another consideration when selecting the output capacitance. This is the impact of radiation induced single event transients (SET). Single energetic particle strikes can lead to momentary variation in the PWM variation of the controller, which in turn can lead to output voltage transients in the converter. Thus, even though the value above provides a minimum value to account for voltage ripple and/or load transients, additional capacitance is likely needed to for adequate SET mitigation. For the design example, approximately 2.3 mF of total output capacitance was used.

An additional output filter can be used to further reduce the noise of the output stage if deemed necessary. This output filter consists of an additional inductor and a small amount of ceramic capacitance. This ceramic capacitance is placed immediately downstream of the main output inductor that was determined in Section 9.2.2.10. The filter inductance is then located between the added ceramic capacitance and the bulk output capacitance that was determined to be required for the design. This approach can drastically reduce the output voltage ripple without significantly increasing the size and/or number of components required. The key for the

secondary filter design is to choose the resonant frequency such that it is higher than the targeted crossover frequency yet well below the switching frequency and ESR zero of the bulk output capacitance. Equation 66, Equation 67, and Equation 68 can be used to determine the ESR zero as well as the resonant frequency and attenuation of the additional output filter.

$$f_{zero} = \frac{1}{2\pi \times C_{OUT\_BULK} \times ESR_{BULK}} \tag{66}$$

$$f_{resonant} = \frac{1}{2\pi \times L_f \times C_{OUT\_BULK}} \tag{67}$$

$$Att_{fsw} = 40\log_{10}\left(\frac{f_{sw}}{f_{resonant}}\right) - 20\log 10\left(\frac{f_{sw}}{f_{zero}}\right) \tag{68}$$

In the event that there is peaking at high frequencies due to the output filter, a resistor can be used to dampen this peaking effect. Equation 69 and Equation 70 can be used to determine the frequency of the peaking and the value of the resistor needed to provide adequate damping.

$$\omega_o = \frac{2 \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{L_f \times C_{OUT\_CER} \times C_{OUT\_BULK}} \tag{69}$$

$$R_f = \frac{R_{OUT} \times L_f \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right) - \frac{L_f}{\omega_o}}{\frac{R_{OUT} \times \left(C_{OUT\_CER} + C_{OUT\_BULK}\right)}{\omega_o} - \left(L_f \times C_{OUT\_CER}\right)} \tag{70}$$

9.2.2.12 Sense Resistor

The converter was designed such that the cycle-by-cycle limiting will begin once the output current reaches roughly 35 A. Given that the peak inductor current at maximum load current is 24.25 A, this provides about 45% margin before an overcurrent event is detected by the controller. The primary side current is being sensed at CS_ILIM, so the turns ratio must be accounted for when calculating the necessary value of the sense resistor. Likewise, a current sense transformer with turns ratio of 1:100 is used to step down the primary current. The following calcuations are used to arrive at the value of R_{CS} that translates to the desired output overcurrent level.

$$I_{LIM} = I_{L,PEAK} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \tag{71}$$

$$I_{LIM} = 35\ A \times \frac{1}{2.5} \times \frac{1}{100} = 0.14\ A \tag{72}$$

$$R_{CS} = \frac{V_{CS\_ILIM}}{I_{LIM}} \tag{73}$$

$$R_{CS} = \frac{1.05\ V}{0.14\ A} = 7.73 \tag{74}$$

Based on the calculation, a 7.5-Ω resistor was selected for R_{CS}.

9.2.2.13 Hiccup Capacitor

For the design, the value of the hiccup capacitor used is the minimum recommended value of 3.3 nF. Based on this value, the delay and hiccup times of the converter after an overcurrent are detected can be calculated.

$$t_{delay} = \frac{C_{HICC} \times 0.6\ V}{80\ \mu A} \tag{75}$$

$$t_{delay} = \frac{3.3\ nF \times 0.6\ V}{80\ \mu A} = 24.75\ \mu s \tag{76}$$

$$t_{HICC} = \frac{C_{HICC} \times (1\ V - 0.3\ V)}{1\ \mu A} \tag{77}$$

$$t_{HICC} = \frac{3.3\ nF \times (1\ V - 0.3\ V)}{1\ \mu A} = 2.31\ ms \tag{78}$$

Note that as mentioned in Section 8.3.15, the delay time calculation is an approximation and the actual time depends on the nature of the overcurrent.

9.2.2.14 Frequency Compensation Components

For this design, Type 2A compensation was used. With a target crossover frequency of 10 kHz, the guidelines shown in Section 8.3.18 are used here to determine the compensation values needed for the compensation network. The power stage transconductance is first needed in order to calculate the frequency compensation component values.

$$gm_{PS} = \frac{N_P \times N_{CSS}}{CCSR \times R_{CS} \times N_S \times N_{CSP}} \tag{79}$$

$$gm_{PS} = \frac{2.5 \times 100}{2.06 \times 7.5\ \Omega \times 1 \times 1} = 16.2\ \frac{A}{V} \tag{80}$$

With the power stage transconductance calculated as 16.2 A/V, the values of the external components needed at the COMP pin can be resolved.

$$R_{COMP} = \frac{2\pi \times f_c \times V_{OUT} \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{PS}} \tag{81}$$

$$R_{COMP} = \frac{2\pi \times 10\ kHz \times 5\ V \times 2.3\ mF}{1800 \times 10^{-6}\ \frac{A}{V} \times 0.613\ V \times 16.2\ \frac{A}{V}} = 40.4\ k \tag{82}$$

$$C_{COMP} = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_{COMP}} \tag{83}$$

$$C_{COMP} = \frac{5\ V \times 2.3\ mF}{20\ A \times 40.2\ k\Omega} = 14.3\ nF \tag{84}$$

For the output capacitance 7 × 330-µF polymer tantalum capacitors were used to meet the 2.3-mF value that was needed for the design. At the selected switching frequency and output voltage, each of these capacitors had an ESR of roughly 6 mΩ. As such, the equivalent ESR used to determine the frequency of the ESR zero in the

frequency response is equivalent the parallel resistance of these seven capacitors, which is 0.86 mΩ. The ESR zero frequency is then used in the calculation of C_{HF}.

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \tag{85}$$

$$f_{ESR} = \frac{1}{2\pi \times 2.3\ mF \times 0.86\ m\Omega} = 80.73\ kHz \tag{86}$$

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{ESR}} \tag{87}$$

$$C_{HF} = \frac{1}{2\pi \times 40.2\ k\Omega \times 80.73\ kHz} = 49.04\ pF \tag{88}$$

The values of R_{COMP}, C_{COMP}, and C_{HF} selected were 40.2 kΩ, 15 nF, and 47 pF, respectively. Note that like many other aspects of the design, the frequency compensation is often tuned during testing in order to obtain the best possible performance.

9.2.2.15 Slope Compensation Resistor

The slope compensation for the converter should be tailored by using the RSC pin of the TPS7H5001-SP. As recommended in Section 8.3.17, the slope compensation should be set to be equal to the falling slope of the output inductor in order to optimize sub-harmonic damping. The slope compensation that is calculated is dependent on the transformer turns ratio, current sense turns ratio, output inductor and current sense resistor that have been selected for the push-pull design.

$$SC = \frac{V_{OUT}}{L} \times \frac{N_S}{N_P} \times \frac{N_{CSP}}{N_{CSS}} \times R_{CS} \tag{89}$$

$$SC = \frac{5\ V}{0.47\ \mu H} \times \frac{1}{2.5} \times \frac{1}{100} \times 7.5\ \Omega = 319148.94 \frac{V}{s} = 0.319 \frac{V}{\mu s} \tag{90}$$

$$RSC = \frac{28.3}{SC^{1.1}} \tag{91}$$

$$RSC = \frac{28.3}{0.319^{1.1}} = 99.4\ k \tag{92}$$

A resistor value of 102 kΩ is connected between RSC and AVSS for the design.

9.2.3 Application Curves

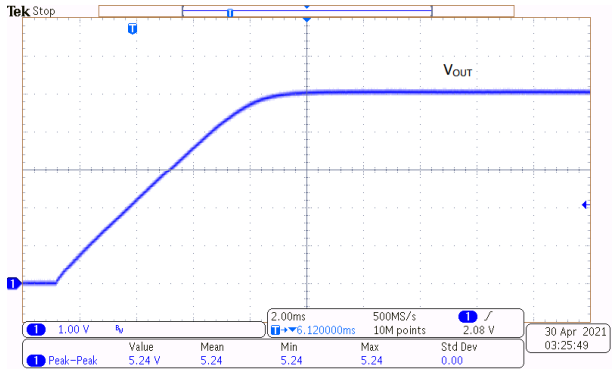


Figure 9-2. V_{OUT} Soft-Start of Push-Pull Converter With I_{OUT} = 10 A

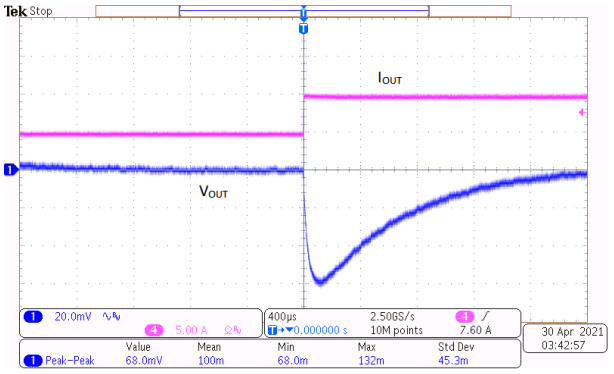


Figure 9-3. 5-A Load Step Response for Push Pull Converter

10 Power Supply Recommendations

The TPS7H500x-SP controllers are designed to operate from an input voltage supply range between 4 V and 14 V. The input voltage supply for the controller should be well regulated and properly bypassed for best electrical performance. A minimum input bypass capacitor of 0.1 µF is required from VIN to AVSS, but additional capacitance can be used to help improve the noise and radiation performance of the controller. It is recommended to use ceramic capacitors (X5R or better) for bypassing, and these capacitors should be placed as close as possible to the controller with a low impedance path to AVSS. Additional bulk capacitors should be used if the input supply is more than a few inches from TPS7H500x-SP controller.

11 Layout

11.1 Layout Guidelines

In order to increase the reliability of the converter design using the TPS7H500x-SP series, the following layout guidelines should be followed.

- Route the feedback trace as far away as possible from power magnetics components (inductor and/or power transformer) and other noise inducting traces on the printed circuit board (PCB) such as the switch node. If the feedback trace is routed beneath the power magnetic component, ensure that this trace is on another layer of the PCB with at least one ground layer separating the trace from the inductor or transformer.
- Minimize the copper area of the converter switch node for the best noise performance and reduction of parasitic capacitance to reduce switching losses. Ensure that any noise sensitive signals, such as the feedback trace, are routed away from this node as it contains a high dv/dt switching signal.
- All high di/dt and dv/dt switching loops in the power stage should have the paths minimized. This will help to reduce EMI, lower stresses on the power devices, and reduce any noise coupling into the control loop.
- Keep the analog ground of the controller (AVSS) separate from the power ground of the power stage that contains high frequency, high di/dt currents. These two grounds should be connected at a single point in the PCB layout. The sources of power semiconductor switches, the returns for bulk input capacitors of the power stage, and the ouput capacitor return should all be connected to the PCB power ground.
- All high current traces on the PCB should be short, direct, and as wide as possible. A good rule is to make the traces a minimum of 15 mils (0.381 mm) per ampere.
- Place all filtering and bypass capacitors for VIN, REFCAP, and VLDO as close as possible to the controller. Surface mount ceramic capacitors with lower ESR and ESL are recommended as these reduce the potential for noise coupling compared to through-hole capacitors. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the respective pin, and AVSS. Each bypass capacitor should have a good, low impedance connection to AVSS.
- External compensation components should be placed near the COMP pin of the controller. Surface mount components are recommended here as well.
- Attempt to keep the resistor divider used to generate the voltage at VSENSE close to the device in order to reduce noise coupling. Minimize stray capacitance to the VSENSE pin.
- OUTA, OUTB, SRA, and SRB are used to drive the inputs of a gate driver, isolator, or gate drive transformer. The PCB traces connected to these pins carry high dv/dt signals. Reduce noise coupling by routing these these PCB traces away from any traces connected to VSENSE, COMP, RT, CS_ILIM, HICC, LEB, RSC, PS, and SP.
- In addition to utilizing the leading edge blank time programmability of the controller, RC filtering may be required for the sensed current signal input to CS_ILIM. Keep the resistor and capacitor in close vicinity to CS_LIM to filter any ringing and/or spikes that may be present on the sensed current signal.
- When operating in internal oscillator mode with SYNC as an output, route the SYNC signal away from noise sensitive signals/pins such as VSENSE, COMP, RT, CS_ILIM, LEB, RSC, PS, and SP. Special care should be taken to eliminate noise from SYNC to HICC since these pins are adjacent to one another. It is recommended that the capacitor from HICC to AVSS be at least 3.3 nF to help with the reduction of the noise.
- Connect the backside metallization of the TPS7H500x-SP to the AVSS plane of the PCB using multiple vias. It is recommended to avoid putting solder paste directly on top of the vias unless these vias are tented or filled.

11.2 Layout Example

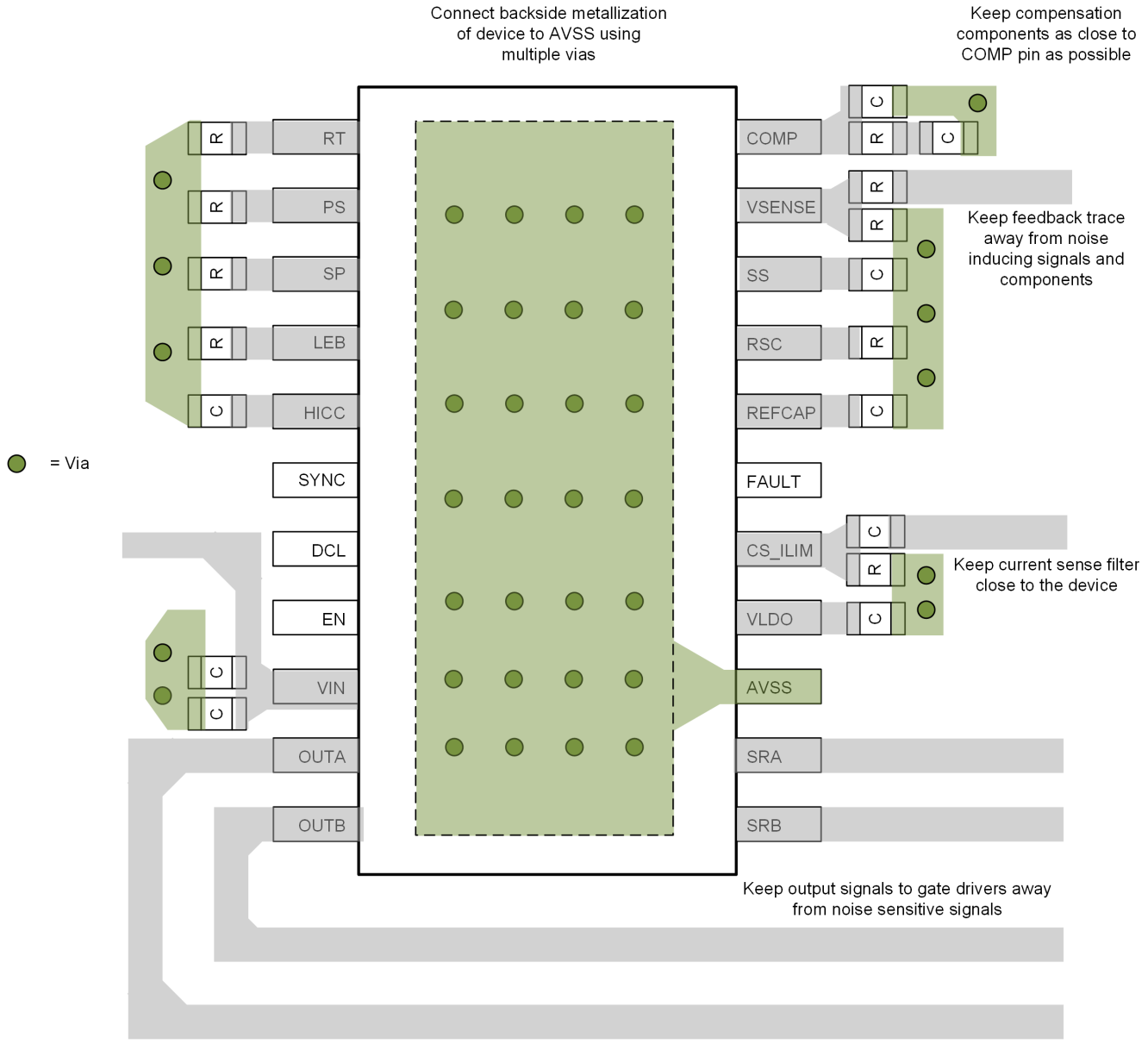


Figure 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H5001-SP Evaluation Module* user's guide
- Texas Instruments, *TPS7H5001-SP Total Ionizing Dose (TID)* radiation report
- Texas Instruments, *TPS7H5001-SP Single-Event Effects (SEE)* radiation report
- Texas Instruments, *TPS7H5001-SP Neutron Displacement Characterization* test report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R1822201V9A	ACTIVE	XCEPT	KGD	0	10	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R1822201VXC	ACTIVE	CFP	HFT	22	1	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1822201VXC TPS7H5001MHFTV	Samples
PTPS7H5002HFT/EM	ACTIVE	CFP	HFT	22	1	TBD	Call TI	Call TI	25 to 25		Samples
PTPS7H5003HFT/EM	ACTIVE	CFP	HFT	22	1	TBD	Call TI	Call TI	25 to 25		Samples
PTPS7H5004HFT/EM	ACTIVE	CFP	HFT	22	1	TBD	Call TI	Call TI	25 to 25		Samples
TPS7H5001HFT/EM	ACTIVE	CFP	HFT	22	1	RoHS & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H5001HFT EVAL ONLY	Samples
TPS7H5001Y/EM	ACTIVE	XCEPT	KGD	0	10	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

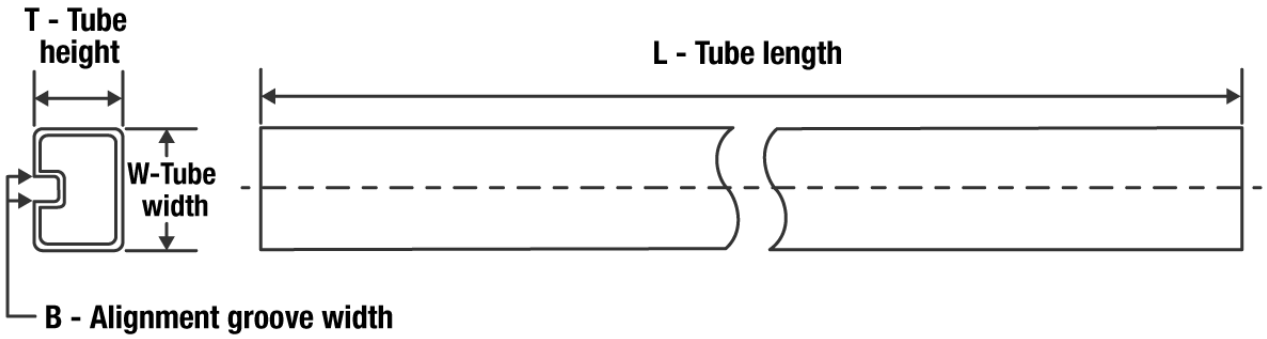
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

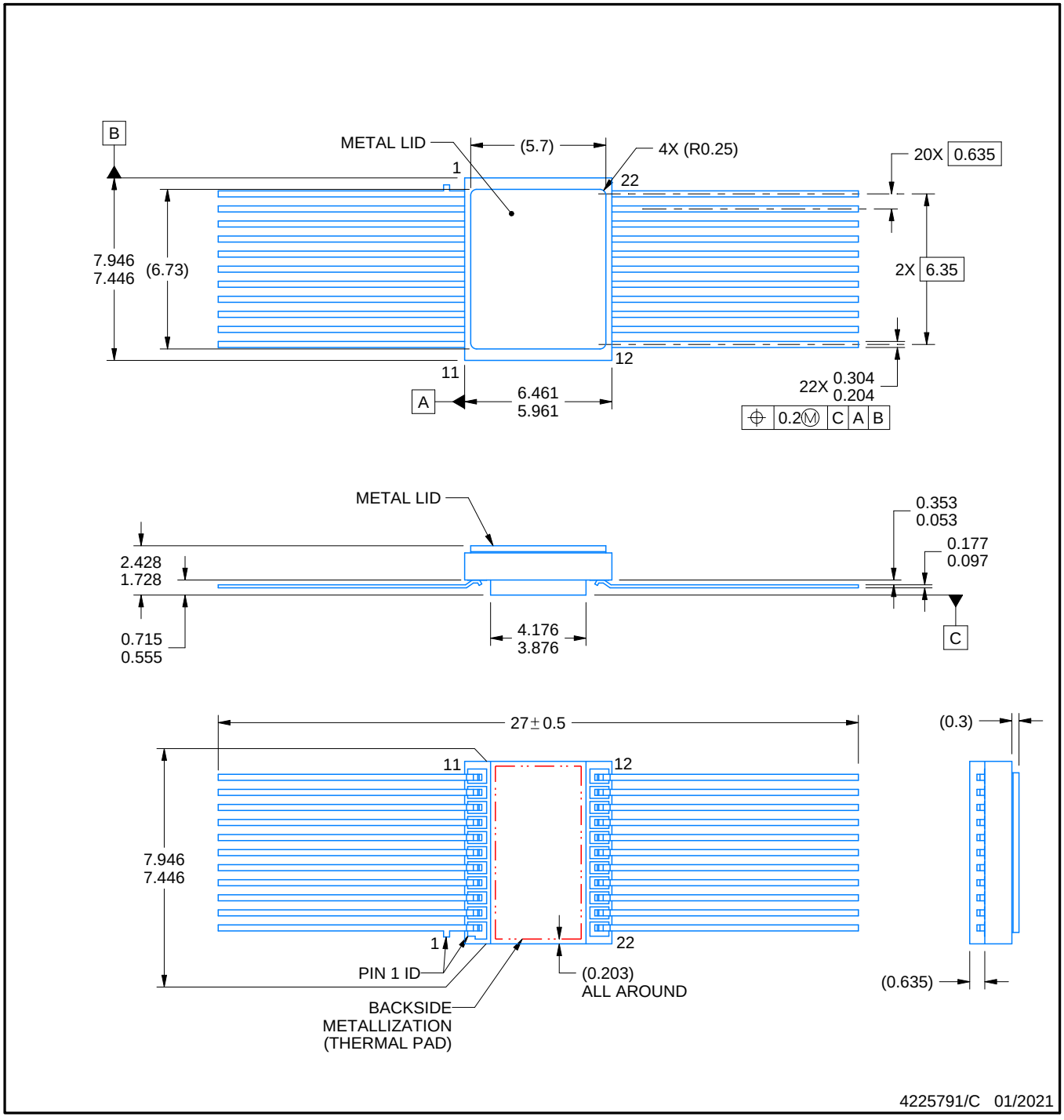
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1822201VXC	HFT	CFP	22	1	506.98	32.77	9910	NA
TPS7H5001HFT/EM	HFT	CFP	22	1	506.98	32.77	9910	NA

PACKAGE OUTLINE

HFT0022A

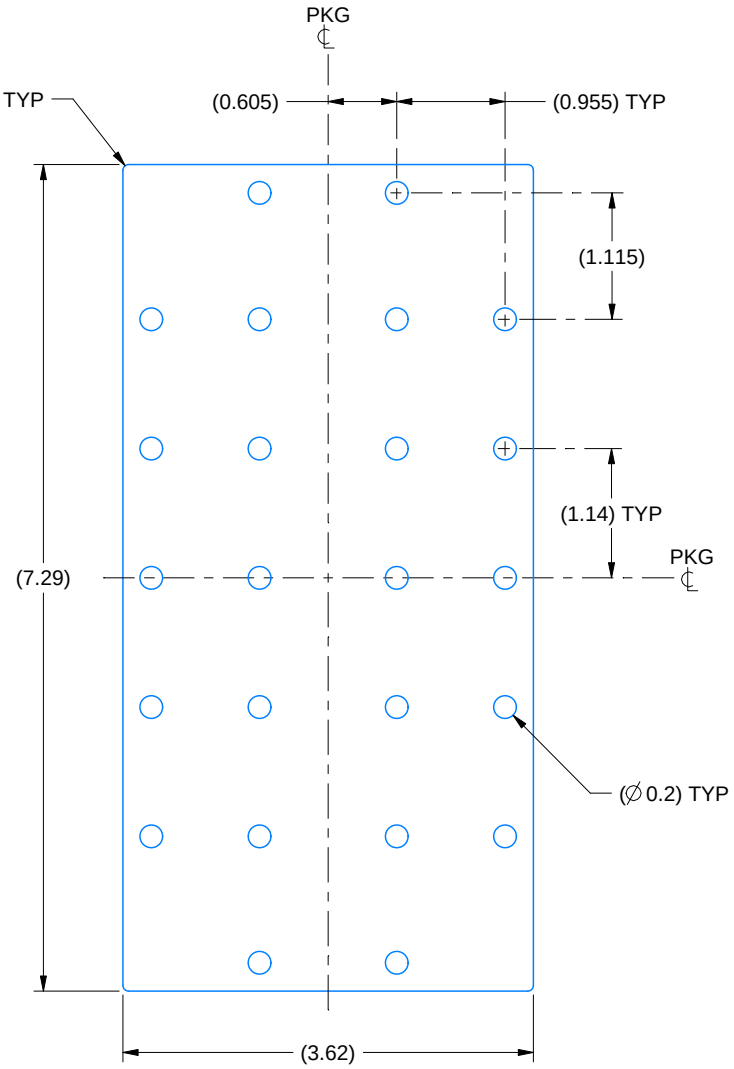
CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27 ± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

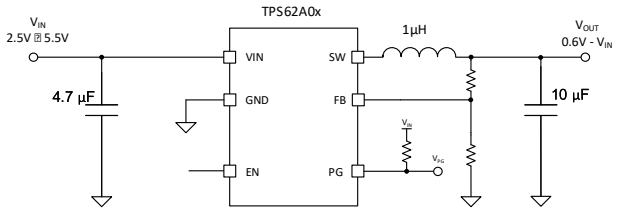
TPS62A01/TPS62A01A, 1-A High-Efficiency Synchronous Buck Converter in a SOT-5X3 Package

1 Features

- 2.5-V to 5.5-V input voltage range
- 0.6-V to V_{IN} adjustable output voltage range
- 180-mΩ / 120-mΩ low R_{DSON} switches (1 A)
- 20-µA quiescent current
- 1% feedback accuracy (0°C to 125°C)
- 100% mode operation
- 2.4-MHz switching frequency
- Power save mode or PWM option available
- Power-good output pin
- Short circuit protection (HICCUP)
- Internal soft start-up
- Output discharge
- Thermal shutdown protection
- Available in a 1.6-mm × 1.6-mm SOT563 package
- Pin-to-pin compatible with the TLV62585

2 Applications

- Multi-function printer
- Set top box
- TV applications
- IP network camera
- Wireless router, solid state drive
- Battery-powered applications
- General purpose point-of-load supply



Typical Application

3 Description

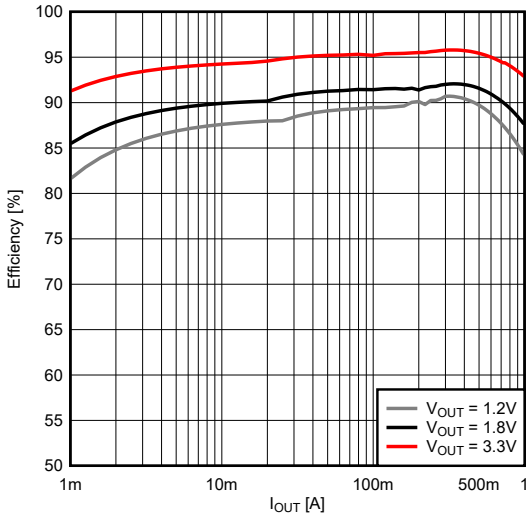
The TPS62A01 family of devices are synchronous step-down buck DC-DC converters optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 1 A. At medium to heavy loads, the device operates in pulse width modulation (PWM) mode with 2.4-MHz switching frequency. At light load, the device automatically enters power save mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is minimal as well. The TPS62A01A variants of this device family operate in forced PWM across the whole load current range.

The TPS62A01 provides an adjustable output voltage through an external resistor divider. An internal soft-start circuit limits the inrush current during start-up. Other features like overcurrent protection, thermal shutdown protection, and power good are built-in. The device is available in a SOT-5X3 package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS62A01	SOT-5X3	1.6 mm × 1.6 mm
TPS62A01A		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency Versus Output Current at 5 V_{IN}

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (March 2022)	Page
• Changed document status from Advance Information to Production Data	1

5 Device Comparison Table

Device Number	Output Current	Operation Mode
TPS62A01	1 A	PSM/ PWM
TPS62A01A	1 A	FPWM

6 Pin Configuration and Functions

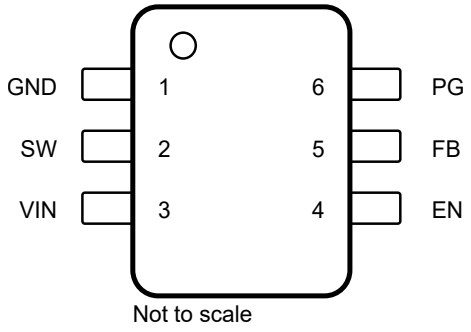


Figure 6-1. 6-Pin DRL SOT-5X3 Package (Top View)

Table 6-1. Pin Functions

Pin		I/O(1)	Description
Name	NO.		
EN	4	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns it into shutdown. Do not leave the pin floating.
FB	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	G	Ground pin
PG	6	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5 V. If unused, leave the pin open or connect to GND.
SW	2	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	I	Power supply voltage pin

(1) I = Input, O = Output, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6	V
	SW, DC	–0.3	V_{IN} + 0.3	
	SW, transient < 10 ns	–3.0	10	
	FB	–0.3	3	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
I_{OUT}	Output current range		0		1	A
L	Effective inductance			1.0		µH
C_{OUT}	Output capacitance	V_{OUT} < 1.2 V		44		µF
		1.2 V ≤ V_{OUT} < 1.8 V		22		µF
		V_{OUT} ≥ 1.8 V		10		µF
I_{PG}	Power-good input current capability		0		1	mA
T_J	Operating junction temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DRL	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610 mV		20		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = Low		0.01	2	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.2			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5 V			100	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 0°C to 125°C, PWM mode	594	600	606	mV
V_{FB}	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6 V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5 V, V_{OUT} = 1.8 V		2400		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56 V			1	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	TPS62A01, V_{IN} = 5V		180		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	TPS62A01, V_{IN} = 5V		120		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS62A01	1.3	1.8		A
$I_{LS(OC)}$	Low-side valley current limit	TPS62A01		1.8		A
$IL_{PEAK(min)}$	Min peak inductor current in PSM			0.4		A
POWER GOOD						
V_{PGTH}	Power-good threshold	PG low, FB falling		93.5%		
V_{PGTH}	Power-good threshold	PG high, FB rising		96%		
	PG delay falling			35		µs
	PG delay rising			10		µs
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 5 V			100	nA
	PG pin output low-level voltage	I_{PG} = 1 mA			400	mV
OUTPUT DISCHARGE						
	Output discharge current on the SW pin	V_{IN} = 3 V, V_{OUT} = 2.0 V		60		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

7.6 Typical Characteristics

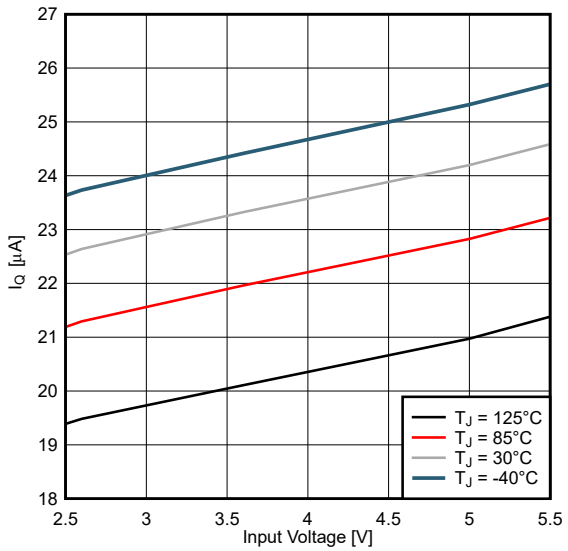


Figure 7-1. Quiescent Current Versus Input Voltage

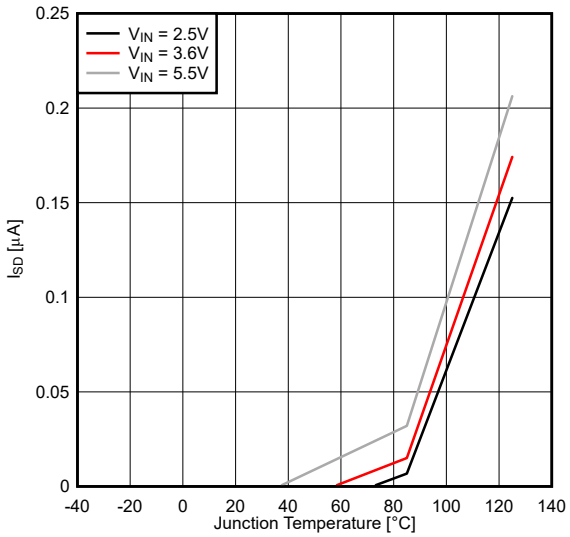


Figure 7-2. Shutdown Current Versus Junction Temperature

8 Detailed Description

8.1 Overview

The TPS62A01x is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.4-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

8.2 Functional Block Diagram

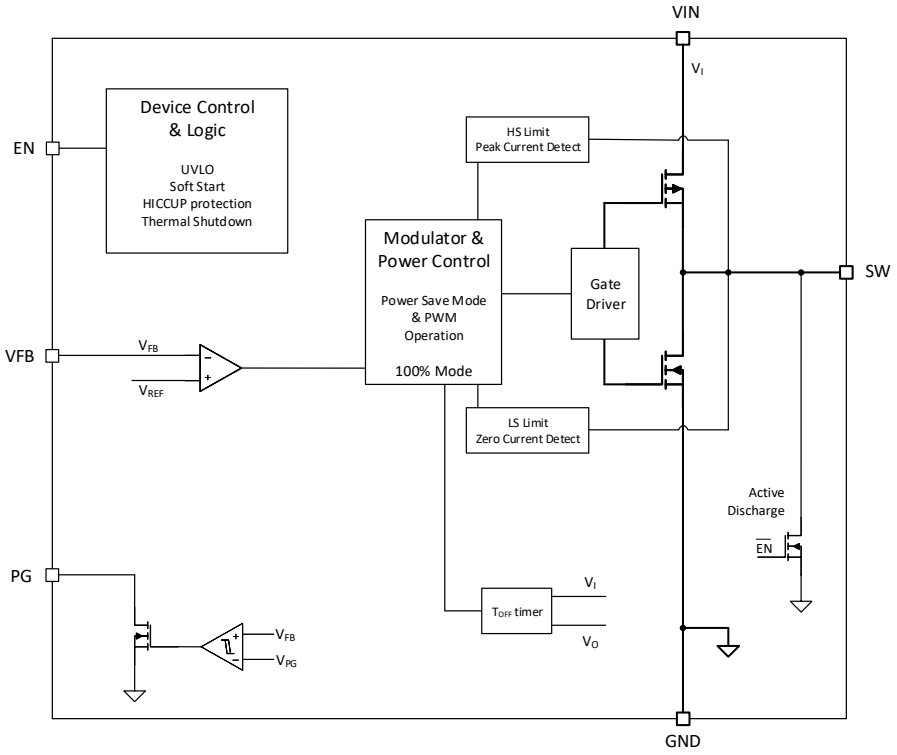


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

8.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

8.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A01x is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

8.3.4 Switch Current Limit and Short Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100 µs has passed. This is named HICCUP short circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

8.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO}.

8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Functional Modes

8.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

8.4.2 Power Good

The TPS62A01x has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power-good can be tie to GND or left open. The PG indicator has a de-glitch to avoid the signal indicating glitches or transient responses from the loop.

Table 8-1. Power Good indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_I > UVLO	HIGH	NO	V_O on target	High Impedance
			V_O < target	LOW
			YES	LOW
		YES	x	LOW
	UVLO < V_I < 1.8 V	x	x	LOW
V_I < 1.8 V	x	x	x	Undefined

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

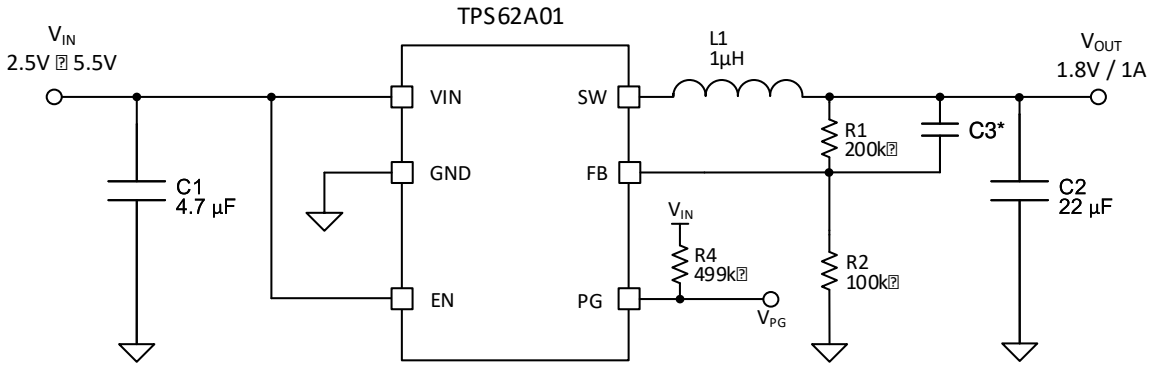


Figure 9-1. TPS62A01 Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters

Table 9-1. Design Parameters

Design Parameter	Example Value
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	1.0 A

Table 9-2 lists the components used for the example.

Table 9-2. List of Components

Reference	Description	Manufacturer(1)
C1	4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1 µH, Power Inductor, DFE252012F-1R0M	Murata
R1, R2	Chip resistor, 1%, size 0603	Std.
C3	Optional, 120 pF if it is needed	Std.

(1) See the *Third-Party Products Disclaimer*.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation 2.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (2)$$

R2 must not be higher than 100 kΩ to provide acceptable noise sensitivity.

9.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 9-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 9-3. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)				
		4.7	10	22	2 × 22	100
0.6 ≤ V_{OUT} < 1.2	1				++(3)	
1.2 ≤ V_{OUT} < 1.8	1			++(3)	+	
1.8 ≤ V_{OUT}	1		+(4)	++(3)	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) This LC combination is the standard value and recommended for most applications.
(4) The minimum C_{OUT} of 10 µF does not support an additional feedforward capacitor.

9.2.2.3 Input and Output Capacitor Selection

The architecture of the TPS62A01x allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, a 4.7-µF input capacitor is sufficient; a larger value reduces input voltage ripple.

The TPS62A01x is designed to operate with an output capacitor of 10 µF to 47 µF, depending on the selected output voltage, as outlined in Table 9-3.

A feedforward capacitor reduces the output ripple in PSM and improves the load transient response. A 120-pF capacitor is good for the 1.8-V output typical application.

9.2.3 Application Curves

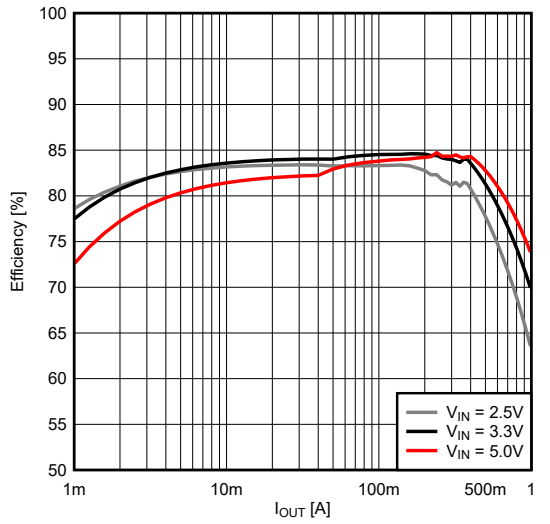


Figure 9-2. 0.6-V Output Efficiency (TPS62A01)

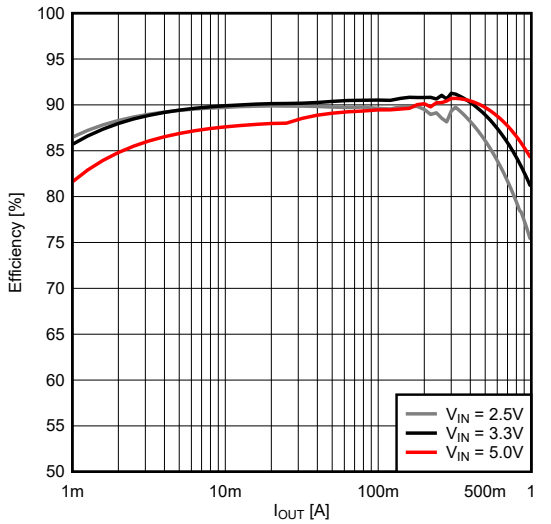


Figure 9-3. 1.2-V Output Efficiency (TPS62A01)

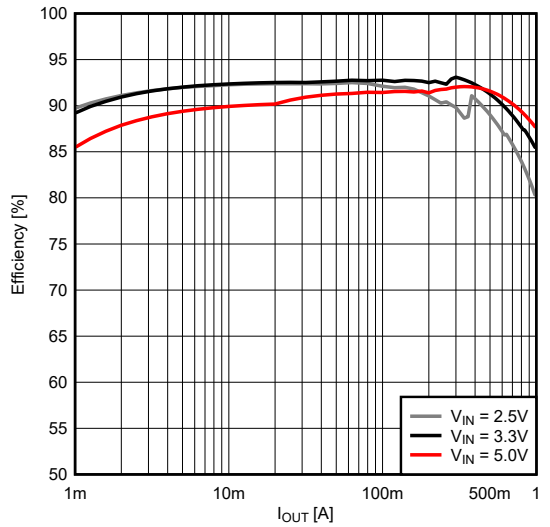


Figure 9-4. 1.8-V Output Efficiency (TPS62A01)

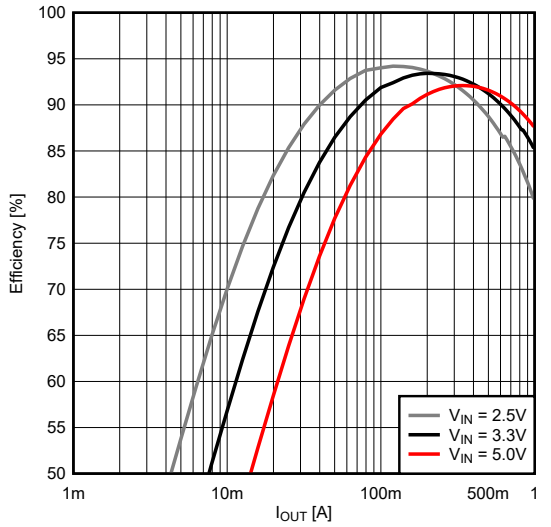
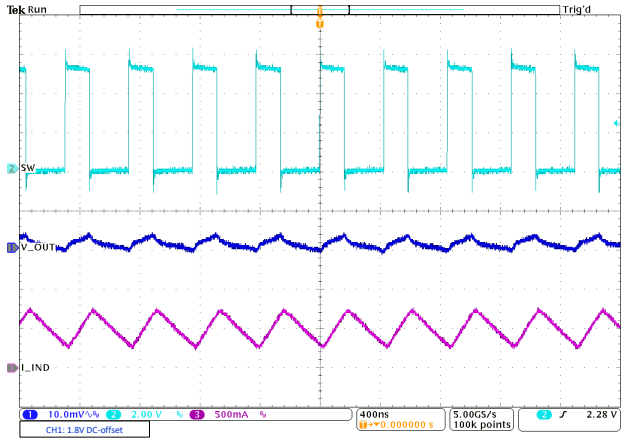
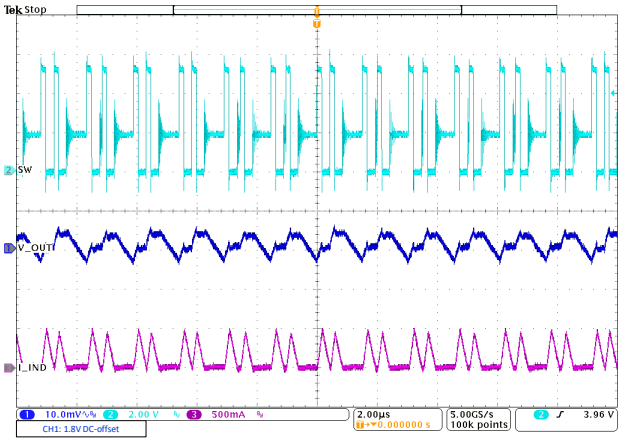


Figure 9-5. 1.8-V Output Efficiency (TPS62A01A)



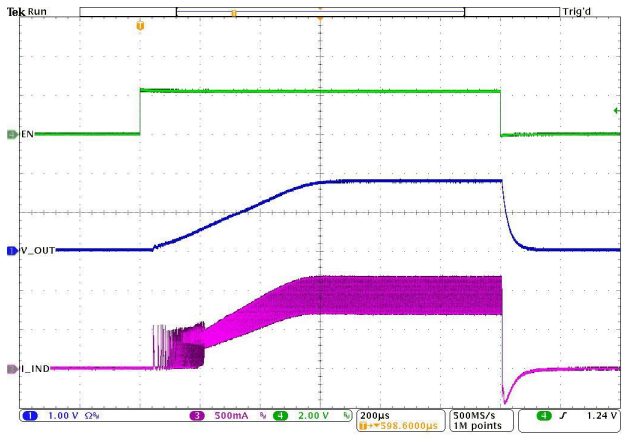
I_{OUT} = 100 mA

Figure 9-6. PWM Operation (TPS62A01)



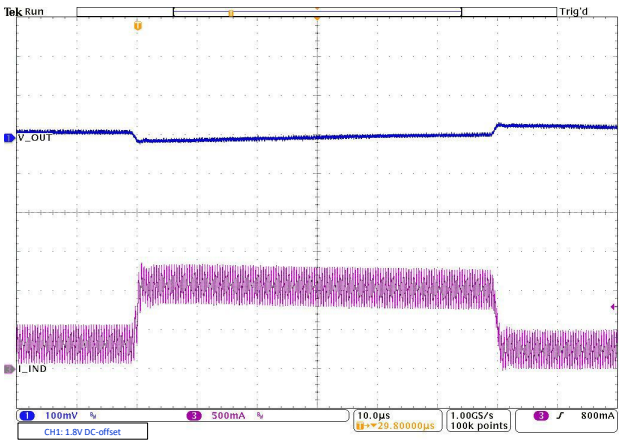
I_{OUT} = 500 mA

Figure 9-7. Power Save Mode Operation



I_{OUT} = 1 A

Figure 9-8. Start-Up with Load (TPS62A01)



Load step: 0.3 A to 1 A

Figure 9-9. Load Transient

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A01x device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- A common ground should be used. GND layers might be used for shielding.

See Figure 11-1 for the recommended PCB layout.

11.2 Layout Example

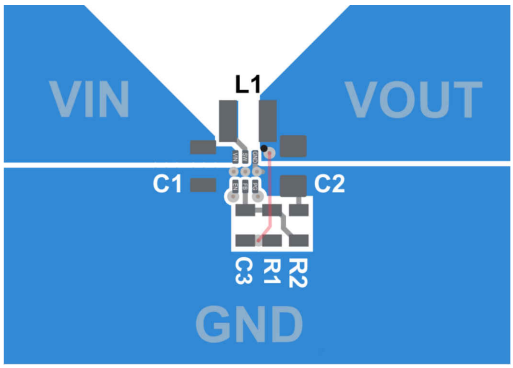


Figure 11-1. TPS62A01x PCB Layout Recommendation

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62A01ADRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1J8	Samples
TPS62A01DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1J7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

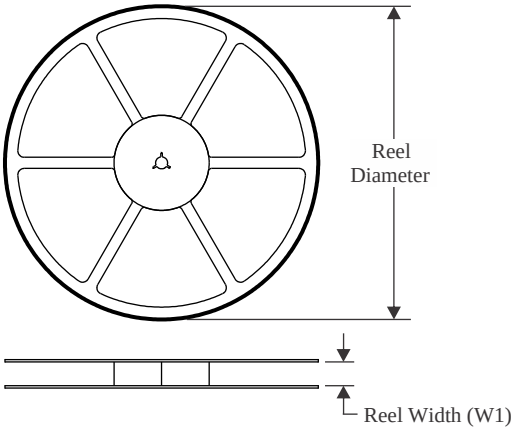
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

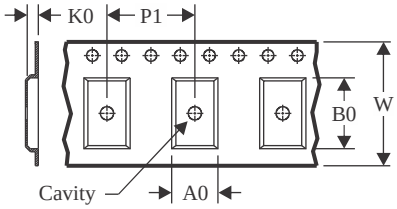
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

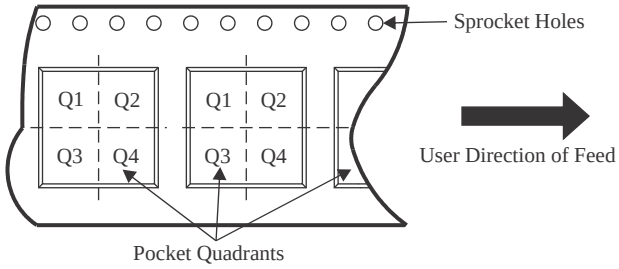


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

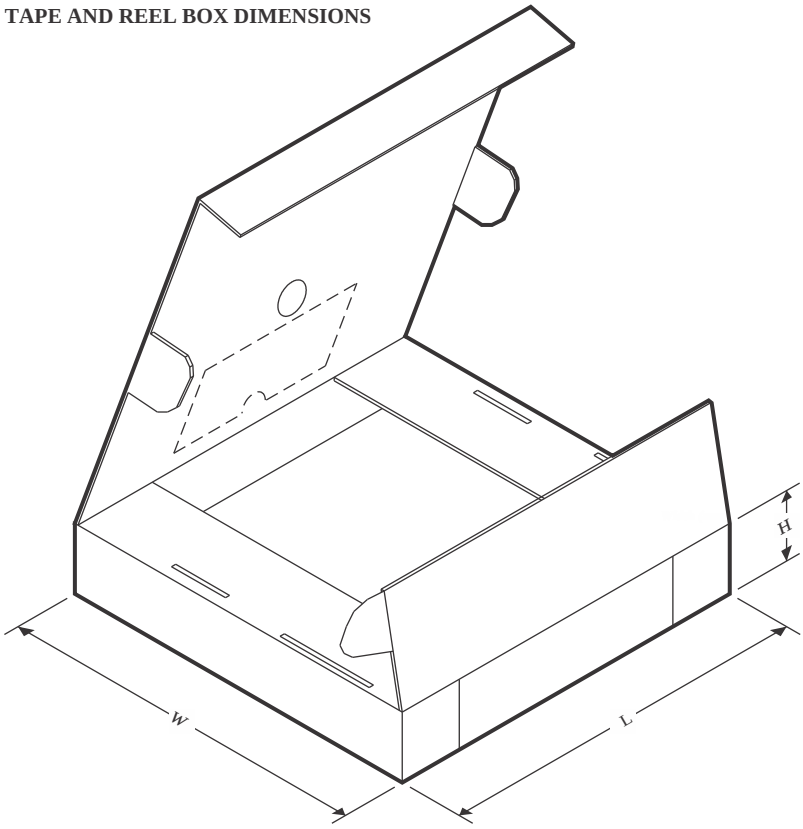
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

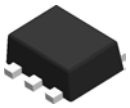
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS62A01DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A01ADRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS62A01DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

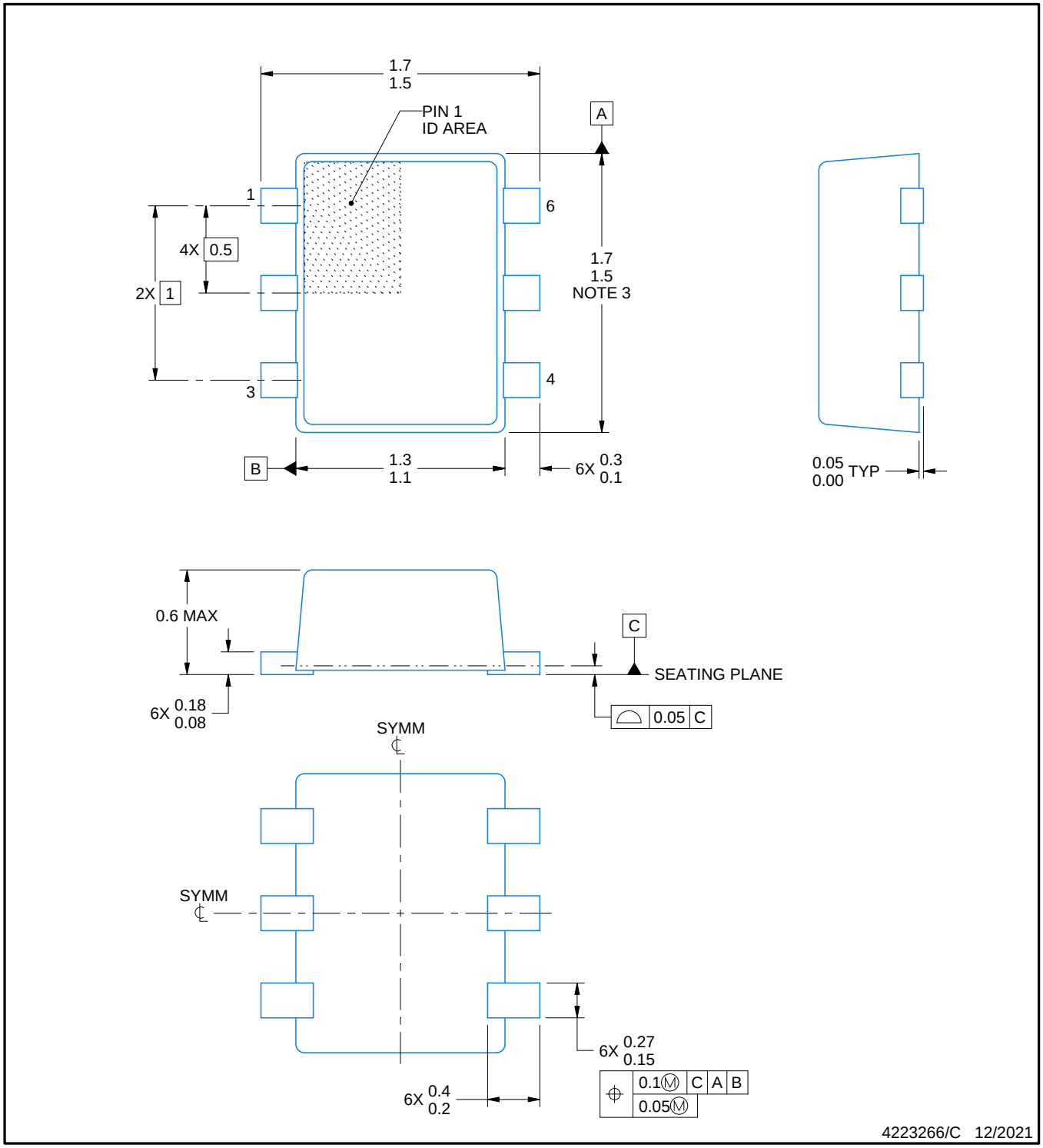


PACKAGE OUTLINE

DRL0006A

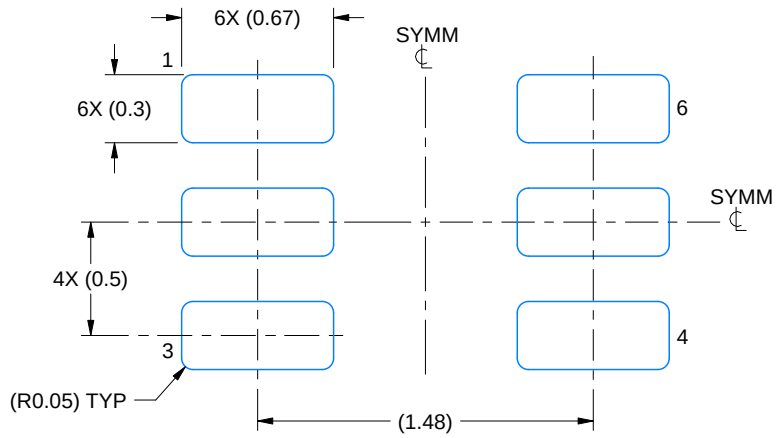
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

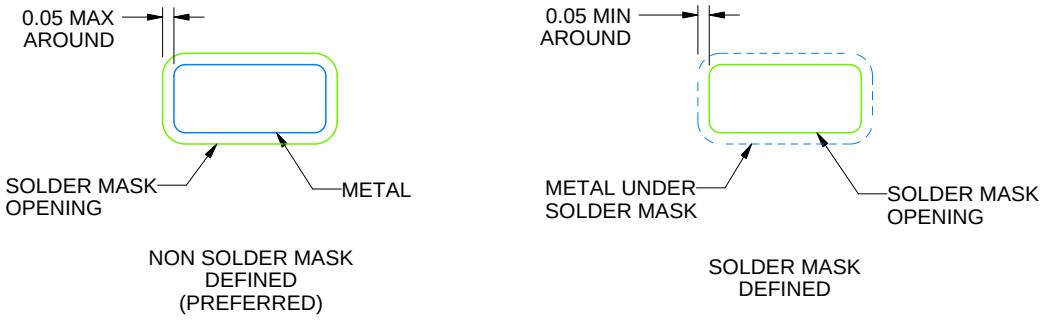


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

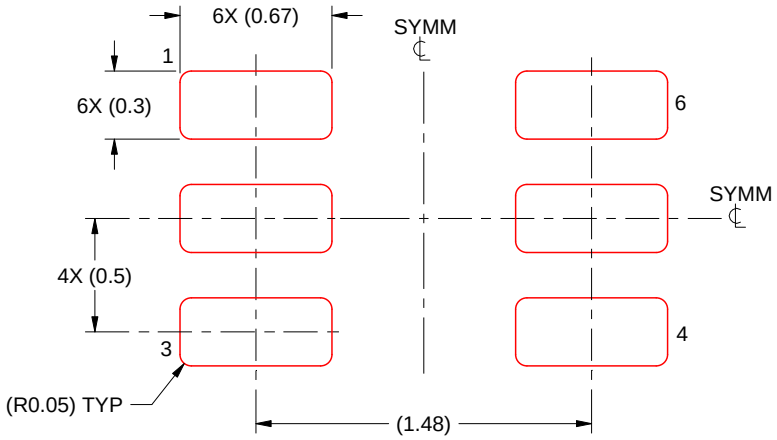
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS4811-Q1
SLUSEE5A – JANUARY 2022 – REVISED JUNE 2022

TPS4811-Q1 100-V Automotive Smart High Side Driver with Protection and Diagnostics

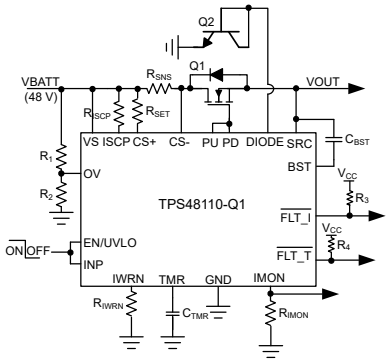
ADVANCE INFORMATION

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3.5-V to 80-V input range (100-V absolute maximum)
- Integrated 12-V charge pump with 100-µA capacity
- Low 1.7-µA shutdown current (EN/UVLO = Low)
- Strong pull up and pull down gate driver: 4 A
- Drives external back-to-back N-Channel MOSFETs
- Variant with Integrated pre-charge switch driver (TPS48111-Q1) to drive capacitive loads
- Two-level adjustable overcurrent protection (IWRN, ISCP) with adjustable circuit breaker timer (TMR) and fault flag output ($\overline{FLT\_I}$)
- Fast short-circuit protection: 1.2 µs (TPS48111-Q1), 5 µs (TPS48110-Q1)
- Accurate analog current monitor output (IMON) – < ±2% at 30 mV VSNS
- Adjustable undervoltage lockout (UVLO) and overvoltage protection (OV)
- Remote overtemperature sensing (DIODE) and protection with fault flag output ($\overline{FLT\_T}$)

2 Applications

- Power distribution box
- Body control module
- DC/DC converter
- Battery management system



Smart High Side Driver for Heater Loads

3 Description

The TPS4811x-Q1 family is a 100-V smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V–80 V, the device is suitable for 12-V, 24-V and 48-V system designs.

It has a strong 4-A sink (PD) and source (PU) GATE driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input.

The device has accurate current sensing (< ±2%) output (IMON) enabling systems for energy management. The device has integrated two-level overcurrent protection with $\overline{FLT\_I}$ output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured. The device features remote overtemperature protection with $\overline{FLT\_T}$ output.

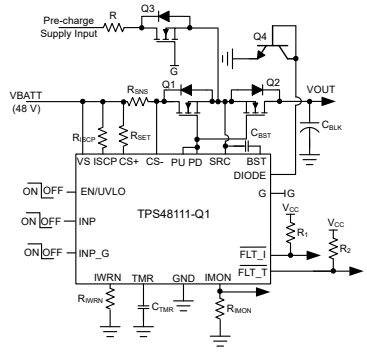
The TPS48111-Q1 integrates a pre-charge driver (G) with control input (INP_G). This features enables designs that must drive large capacitive loads. In shutdown mode, the controller draws a total IQ of 1.7 µA at 48-V supply input.

The TPS4811x-Q1 is available in a 19-pin VSSOP package with a pin removed between adjacent high voltage and low voltage pins, providing 0.8-mm clearance.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS48110-Q1(2), TPS48111-Q1	VSSOP (19)	5.1 mm × 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) PRODUCT PREVIEW.



Circuit Breaker for DC-DC Converter

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2022) to Revision A (June 2022)	Page
• Added functional safety bullets to the *Features* section	1
• Corrected pin number for TPS48111-Q1 VS pin	3

5 Device Comparison Table

	TPS48110-Q1[1]	TPS48111-Q1
Overvoltage protection	Yes	No
Pre-charge driver	No	Yes
Overtemperature fault response	Auto-retry with fixed 512-ms timer	Latch-off

(1) PRODUCT PREVIEW.

6 Pin Configuration and Functions

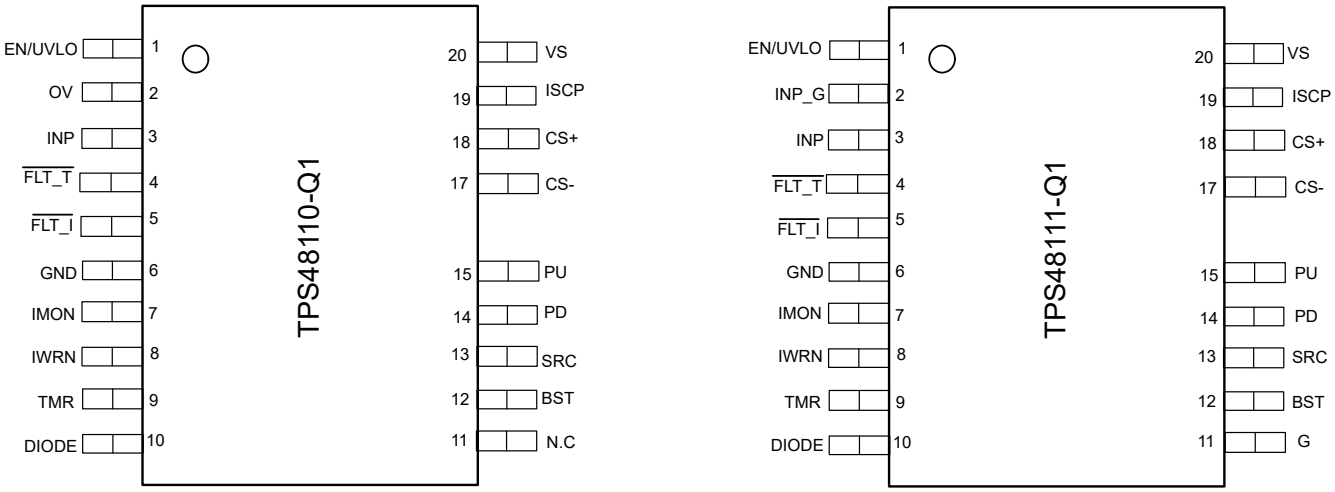


Figure 6-1. VSSOP 19-Pin DGX Top View

Table 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS48110-Q1	TPS48111-Q1		
	DGX-19 (VSSOP)			
EN/UVLO	1	1	I	EN/UVLO input. A voltage on this pin above 1.21 V enables normal operation. Forcing this pin below 0.3 V shuts down the TPS4811x-Q1, reducing quiescent current to approximately 1.7 µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 100 nA pulls EN/UVLO low and keeps the device in OFF state.
OV	2	—	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OVP exceeds the overvoltage cut-off threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pull down of 100 nA pulls OV low and keeps PU pulled up to BST.
INP_G	—	2	I	Input Signal. CMOS compatible input reference to GND that sets the state of G pin. INP_G has an internal pull-down to GND to keep G pulled to SRC when INP_G is left floating. Connect INP_G to GND if the G drive functionality is unused.
INP	3	3	I	Input Signal. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal pull-down to GND to keep PD pulled to SRC when INP is left floating
$\overline{\text{FLT\_T}}$	4	4	O	Open Drain Fault Output. This pin asserts low when overtemperature fault is detected.

ADVANCE INFORMATION

Table 6-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	TPS48110-Q1	TPS48111-Q1		
	DGX-19 (VSSOP)			
$\overline{FLT\_I}$	5	5	O	Open Drain Fault Output. This pin asserts low after the voltage on the TMR pin has reached the fault threshold of 1.1 V. This pin indicates the pass transistor is about to turn off due to an overcurrent condition. The $\overline{FLT\_I}$ pin does not go to a high-impedance state until the overcurrent condition and the auto-retry time expire.
GND	6	6	G	Connect GND to system ground
IMON	7	7	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor RSNS. A resistor from this pin to GND converts current to proportional voltage. If unused, connect the pin to GND.
IWRN	8	8	I	Overcurrent detection setting. A resistor across IWRN to GND sets the over current comparator threshold. Connect IWRN to GND if overcurrent protection feature is not desired.
TMR	9	9	I	Fault Timer Input. A capacitor across TMR pin to GND sets the times for fault warning, fault turn-off ($\overline{FLT\_I}$) and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
DIODE	10	10	I	Diode connection for temperature sensing. Connect this pin to base and collector of an MMBT3904 NPN BJT. Connect DIODE to GND, if remote overtemperature protection feature is not desired.
G	—	11	O	GATE of external pre-charge FET. Connect to the GATE of the external FET. Leave the G pin floating if the G drive functionality is unused.
N.C	11	—	—	No connect
BST	12	12	O	High Side Bootstrapped Supply. An external capacitor with a minimum value of > Qg(tot) of the external FET must be connected between this pin and SRC.
SRC	13	13	O	Source connection of the external FET
PD	14	14	O	High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	15	O	High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS-	17	17	I	Current sense negative input
CS+	18	18	I	Current sense positive input. Connect a 100-Ω resistor across CS+ to the external current sense resistor.
ISCP	19	19	I	Short circuit detection threshold setting. Connect ISCP to CS– if short-circuit protection is not desired.
VS	20	20	Power	Supply pin of the controller

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS–, ISCP to GND	–1	100	V
Input Pins	VS, CS+, CS– to SRC	–60	100	
Input Pins	SRC to GND	–30	100	
Input Pins	PU, PD, G, BST to SRC	–0.3	16	
Input Pins	TMR, IWRN, DIODE to GND	–0.3	5.5	
Input Pins	OV, EN/UVLO, INP, INP_G, $\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	–1	20	
Input Pins	CS+ to CS–	–0.3	0.3	
Sink current	$I_{(\overline{FLT\_I})}$, $I_{(\overline{FLT\_T})}$		10	mA
	$I_{(CS+)}$ to $I_{(CS–)}$, 1 msec	–100	100	
Source current	$I_{(IMON)}$	Internally limited		
Output Pins	PU, PD, G, BST to GND	–30	112	V
	IMON to GND	–1	7.5	
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, DIODE, G, VS)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS, CS+, CS- to GND	0		80	V
	EN/UVLO, OV to GND	0		15	
Output Pins	$\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	0		15	
	IMON to GND	0		5.5	
External Capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

ADVANCE INFORMATION

7.4 Thermal Information

THERMAL METRIC[1]		TPS4811-Q1 DGX 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.5 Electrical Characteristics

T_J = –40 °C to +125°C. $V_{(VS)} = V_{(CS+)} = V_{(CS-)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VS	Operating input voltage		3.5		80	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(VS)}$ = 48 V, $V_{(EN/UVLO)}$ = 2 V		510		µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		1.7		µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.18	1.2	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.11	1.12	1.15	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V
OVER VOLTAGE PROTECTION (OV) INPUT – TPS48110-Q1 Only						
$V_{(OVR)}$	Overvoltage threshold input, risIng	TPS48110-Q1[1] Only	1.16	1.18	1.2	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.11	1.12	1.15	V
CHARGE PUMP (BST–SRC)						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST-SRC)}$ = 10 V		100		µA
$V_{(BST-SRC)}$	Charge Pump Turn ON voltage		11			V
	Charge Pump Turnoff voltage				13	V
$V_{(BST\ UVLO)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising				8.2	V
	$V_{(BST-SRC)}$ UVLO voltage threshold, falling		6			V
$V_{(BST-SRC)}$	Charge Pump Voltage at $V_{(VS)}$ = 3.5 V		8			V
GATE DRIVER OUTPUTS (PU, PD, G)						
$I_{(PU)}$	Peak Source Current			3.7		A
$I_{(PD)}$	Peak Sink Current			4		A
$I_{(G)}$	Gate charge (sourcing) current, on state	TPS48111-Q1 Only		100		µA
	Gate discharge (sinking) current, off state			135		mA
CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS–, IMON, ISCP, IWRN)						
$V_{(OS\_SET)}$	Input referred offset (V_{SNS} to V_{IMON} scaling)	R_{SET} = 100 Ω, R_{IMON} = 5 kΩ, 10 kΩ (corresponds to V_{SNS} = 6 mV to 30 mV) and Gain of 45 and 90 respectively.	–350		350	µV

7.5 Electrical Characteristics (continued)

T_J = –40 °C to +125°C. $V_{(VS)}$ = $V_{(CS+)}$ = $V_{(CS-)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SNS\_WRN)}$	OCP threshold threshold	R_{SET} = 100 Ω, $R_{(IWRN)}$ = 41.2 kΩ	28	30	32	mV
	OCP threshold threshold	R_{SET} = 100 Ω, $R_{(IWRN)}$ = 123 kΩ		10		mV
I_{SCP}	SCP Input Bias current			14.5		µA
$V_{(SNS\_SCP)}$	SCP threshold	$R_{(ISCP)}$ = 2.1 kΩ	35	40	45	mV
		$R_{(ISCP)}$ = 750 Ω		20		mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current			77		µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current			2.5		µA
$I_{(TMR\_SNK)}$	TMR sink current			2.5		µA
INPUT CONTROLS (INP, INP_G), FAULT FLAG ($\overline{FLT\_I}$, $\overline{FLT\_T}$)						
$V_{(INP\_H)}$, $V_{(INP\_G\_H)}$		$V_{(INP\_G\_H)}$ for TPS48111-Q1 Only			2	V
$V_{(INP\_L)}$, $V_{(INP\_G\_L)}$		$V_{(INP\_G\_L)}$ for TPS48111-Q1 Only	0.8			V
$R_{(\overline{FLT\_I})}$, $R_{(\overline{FLT\_T})}$	$\overline{FLT\_x}$ Pull-down resistance			70		Ω
TEMPERATURE SENSING AND PROTECTION (DIODE)						
$I_{(DIODE)}$	External diode current source	High level		160		µA
		Low level		10		µA
$T_{(DIODE\_TSD\_rising)}$	DIODE sense TSD rising threshold			155		°C
$T_{(TSD\_INT)}$	Internal TSD rising threshold		165			°C
	Internal TSD falling threshold		150			°C

(1) PRODUCT PREVIEW

7.6 Switching Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = $V_{(CS+)}$ = $V_{(CS-)}$ = 48 V, $V_{(BST-SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propogation Delay	INP ↑ to PU ↑, C_L = 47 nF		2		µs
$t_{PD(INP\_L)}$	INP Turn OFF propogation Delay	INP ↓ to PD ↓, C_L = 47 nF		1		µs
$t_{G(INP\_G\_H)}$	INP_G Turn ON propogation Delay	INP_G ↑ to G ↑, C_L = 1 nF		25		µs
$t_{G(INP\_G\_L)}$	INP_G Turn OFF propogation Delay	INP_G ↓ to G ↓, C_L = 1 nF		1		µs
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to PD ↓, C_L = 47 nF		3		µs
$t_{PU(UVLO\_ON)}$	UVLO to PU Turn ON Propogation Delay with CBT pre-biased > VPORF and INP kept high	EN/UVLO ↑ to PU ↑, C_L = 47 nF, INP = 2 V		3		µs
$t_{PD(OV\_OFF)}$	OV Turn Off progopation Delay	OV ↑ to PD ↓, C_L = 47 nF		3		µs
$t_{PD(IFLT\_OFF)}$	Short Circuit Protection propogation Delay	(V_{CS+} – V_{CS-}) ↑ $I_{(SCP)}$ to PD ↓, C_L = 47 nF, TPS48110–Q1 Only		5		µs
		(V_{CS+} – V_{CS-}) ↑ to $I_{(SCP)}$ PD ↓, C_L = 47 nF, TPS48111-Q1 Only		1.2		µs
$t_{FLT\_I(IFLT\_ASSERT)}$	FLT_I assertion delay			290		µs
$t_{FLT\_I(IFLT\_DEASSERT)}$	FLT_I de-assertion delay			260		µs
$t_{FLT\_T(AR)}$	TSD Auto-retry	TPS48110-Q1(1) Only		512		msec

(1) PRODUCT PREVIEW.

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS4811x-Q1 family is a 100-V smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V – 80 V, the device is suitable for 12-V, 24-V, and 48-V system designs.

The device has a strong 4-A sink (PD) and source (PU) GATE driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing (<±2 % at 30-mV VSNS) output (IMON) enabling systems for energy management. The device has integrated two-level overcurrent protection with $\overline{\text{FLT\_I}}$ output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

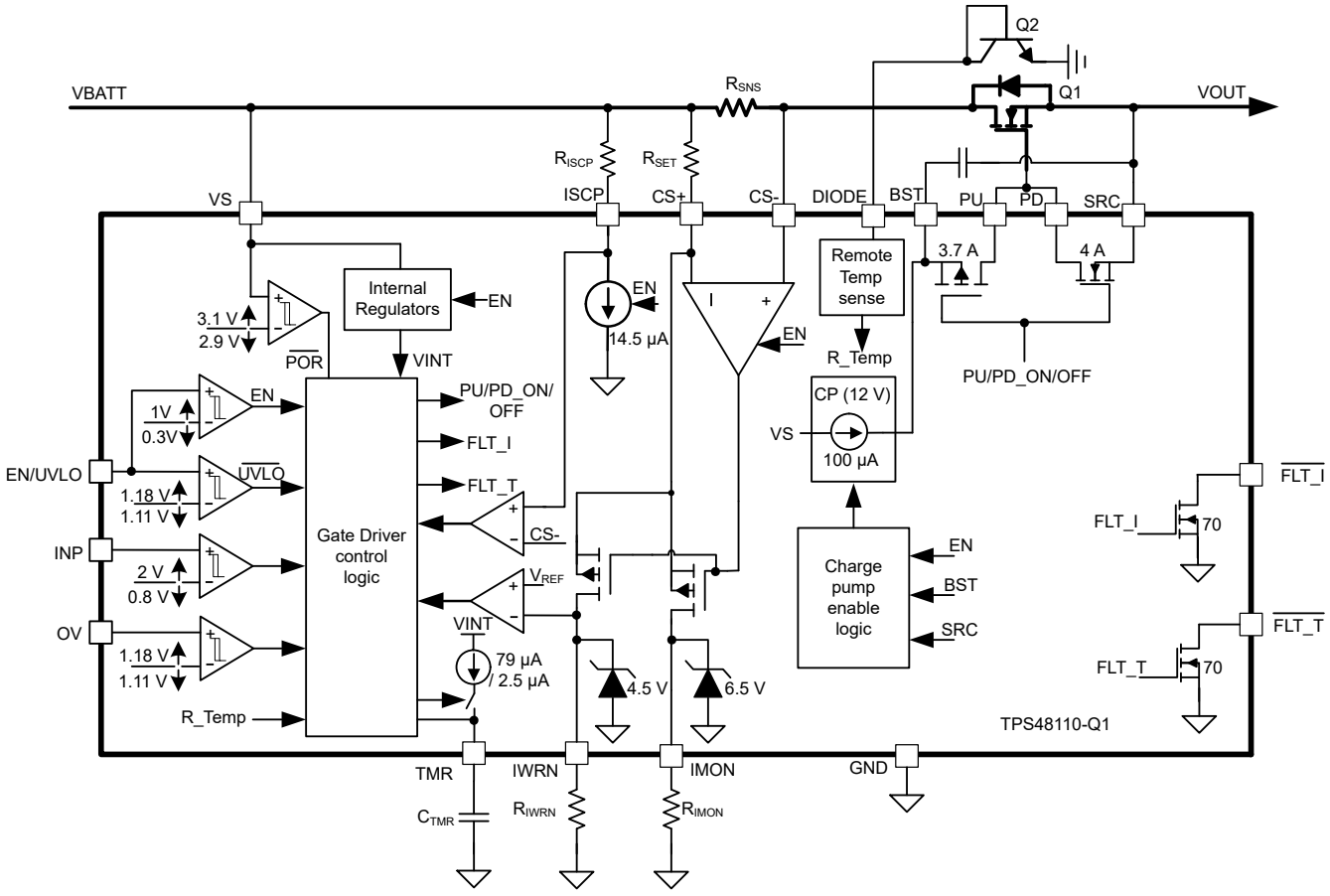
The device features remote overtemperature protection with $\overline{\text{FLT\_T}}$ output enabling robust system protection.

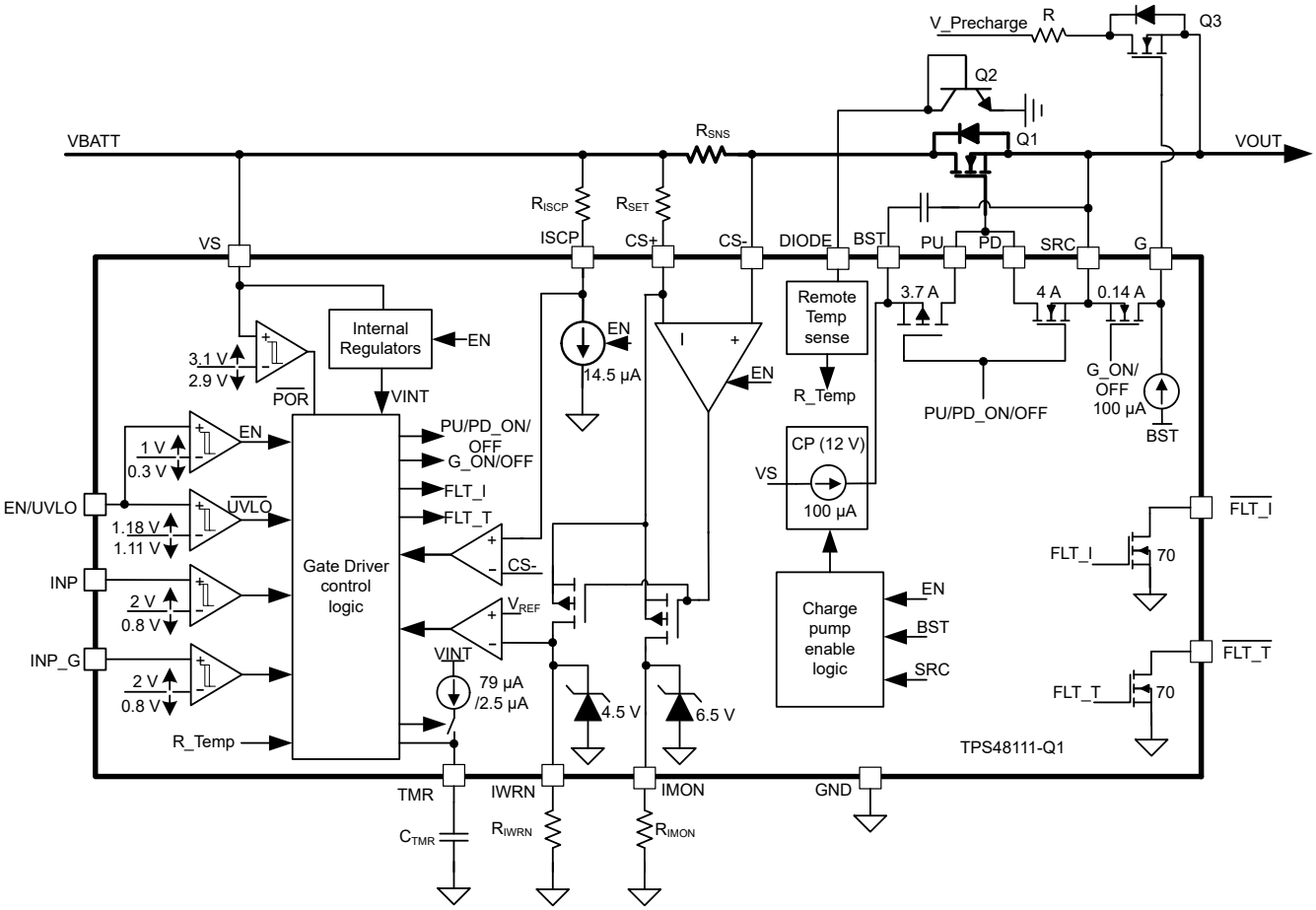
TPS48110-Q1 has an accurate overvoltage protection (<±2 %), providing robust load protection.

The TPS48111-Q1 integrates a pre-charge driver (G) with control input (INP_G). This feature enables system designs that need to drive large capacitive loads by pre-charging first and then turning ON the main power FETs.

TPS4811x-Q1 has an accurate undervoltage protection (±3 %) using EN/UVLO pin. Pull EN/UVLO low (< 0.3 V) to turn OFF the device and enter into shutdown state. In shutdown mode, the controller draws a total IQ of 1.7 µA at 48-V supply input.

8.2 Functional Block Diagram





8.3 Feature Description

8.3.1 Charge Pump and Gate Driver output (VS, PU, PD, BST, SRC)

Figure 8-1 shows simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7-A source and 4-A sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12-V, 100-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the GATE driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100 µA, then supply BST externally using a low leakage diode and 12-V supply as shown in the Figure 8-1.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET's QG and allowed dip during FET turn ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 12.3 V and 11.7 V as shown in the Figure 8-2.

ADVANCE INFORMATION

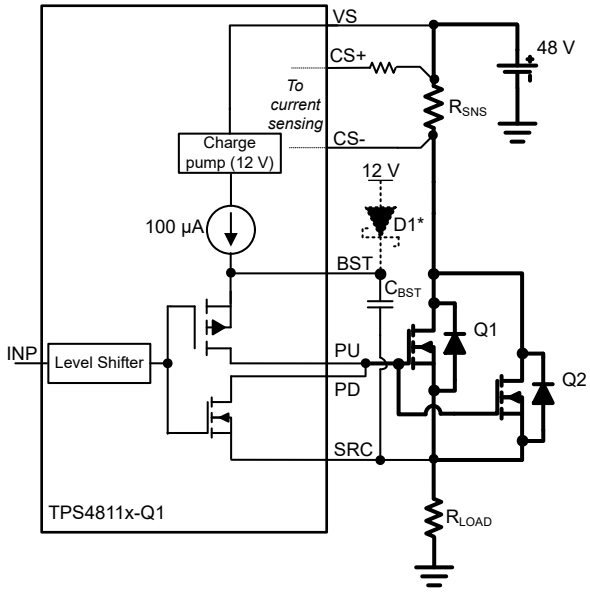


Figure 8-1. Gate Driver

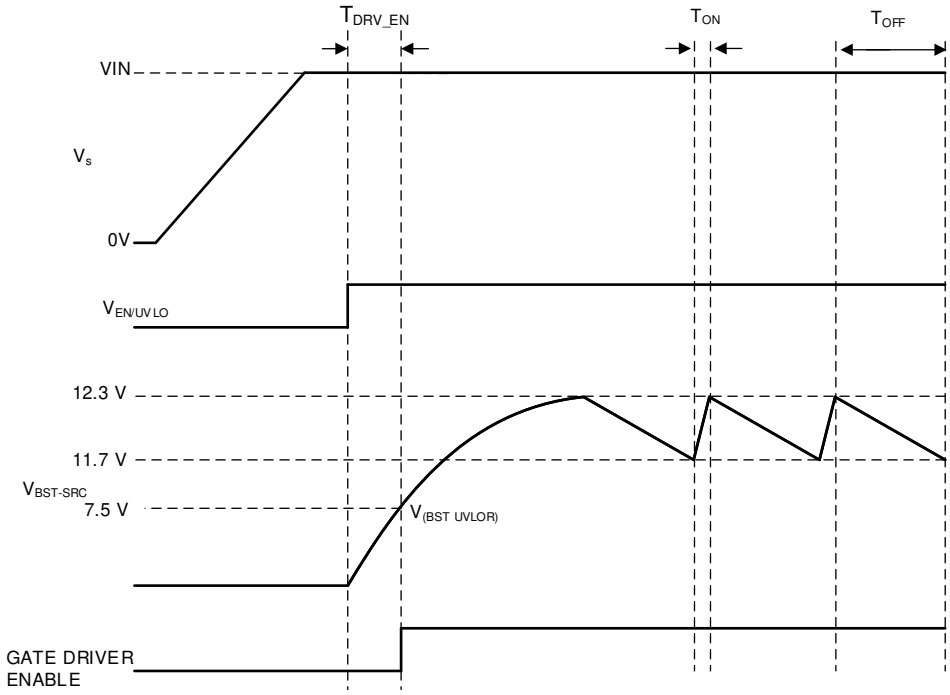


Figure 8-2. Charge Pump Operation

Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{100\ \mu A} \quad (1)$$

Where,

$C_{(BST)}$ is the charge pump capacitance connected across BST and SRC pins,

$V_{(BST\_UVLOR)}$ = 7.5 V (typical).

If T_{DRV_EN} needs to be reduced then pre-bias BST terminal externally using an external 12-V supply through a low leakage diode D1 as shown in Figure 8-1. With this connection T_{DRV_EN} reduces to 350 µs.

8.3.1.1 Inrush Current limiting

For limiting inrush current during turn ON of the FET with capacitive loads, use R_1, R_2, C_1 as shown in Figure 8-3. The R_1 and C_1 components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors. The inrush current during turn ON of the FET can be calculated using Equation 2.

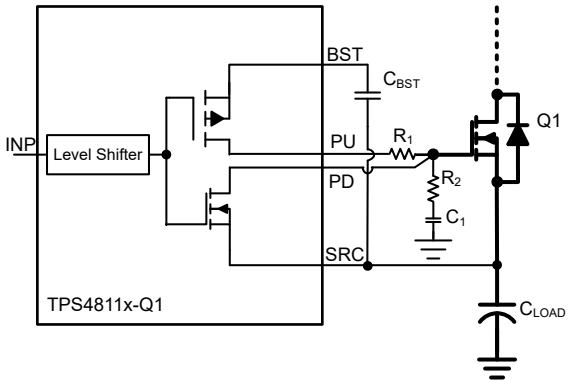


Figure 8-3. Inrush Current limiting

$$I_{INRUSH} = \frac{0.63 \times V_{(BST-SRC)} \times C_{LOAD}}{R_1 \times C_1} \quad (2)$$

Where,

$V_{(BST-SRC)}$ is the charge pump voltage (12 V),

C_{LOAD} is the load capacitance.

Use a damping resistor R_2 (~ 10 Ω) in series with C_1. Equation 2 can be used to compute required C_1 value for a target inrush current. A 100 kΩ resistor for R_1 can be a good starting point for calculations.

Connecting PD pin of TPS4811x-Q1 directly to the gate of the external FET ensures fast turn OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn ON. Use Equation 3 to calculate the required C_{BST} value.

$$C_{BST} > Q_{g(total)} + 10 \times C_1 \quad (3)$$

Where, $Q_{g(total)}$ is the total gate charge of the FET.

8.3.2 Precharge Gate Driver (G) and Control Input (INP_G) – TPS48111-Q1 Only

The TPS48111-Q1 integrates pre-charge gate driver. Use this feature to drive large bulk capacitors during power-up before turning ON the main FETs. INP_G control is active when EN/UVLO is high and $C_{(BST)}$ voltage isabove $V_{(BST\_UVLOR)}$. With INP_G high, G is pulled up to BST with a 100 µA. When INP_G is pulled low then G is pulled low to SRC with a 135-mA pull down.

ADVANCE INFORMATION

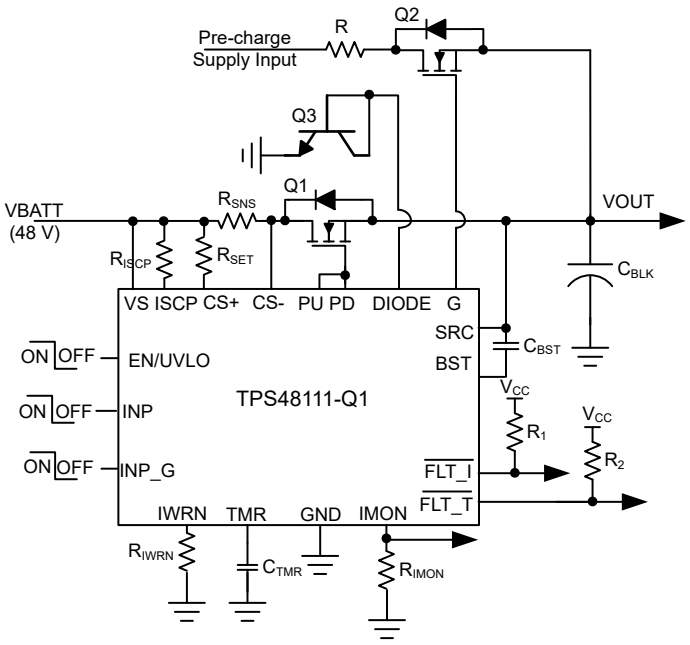


Figure 8-4. TPS48111-Q1 Typical Application Circuit

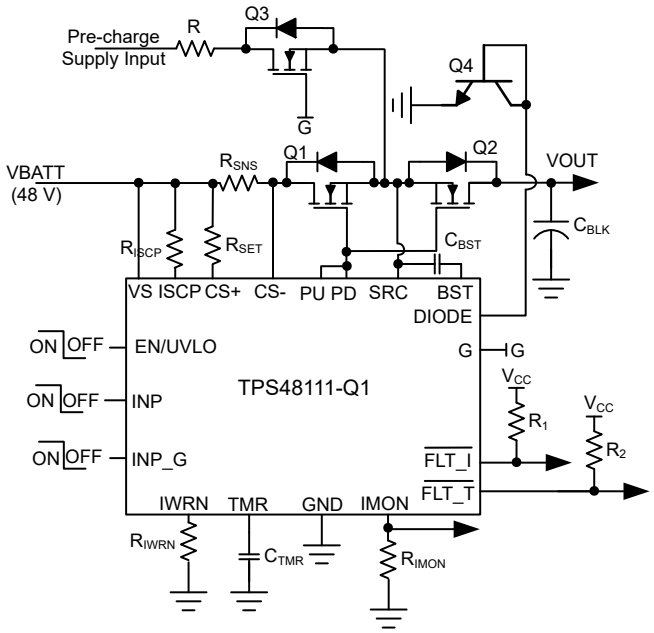


Figure 8-5. TPS48111-Q1 Typical Application Circuit With B2B FET Driving

8.3.3 Overcurrent Protection

TPS4811x-Q1 has two-level overcurrent protection. The device senses the voltage across the external current sense resistor through CS+ and CS–.

Set the circuit breaker detection threshold using an external resistor R_{IWRN} across IWRN and GND. Use Equation 4 to calculate the required R_{IWRN} value.

$$R_{IWRN}(\ \ ) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{WRN}} \tag{4}$$

Where, R_{SET} is the resistor connected across CS+ and VS,R_{SNS} is the current sense resistor, I_{WRN} is the overcurrent level

8.3.3.1 Overcurrent Protection With Auto-Retry

The $C_{(TMR)}$ programs the circuit breaker and auto-retry time. After the voltage across CS+ and CS– exceeds the set point, the $C_{(TMR)}$ starts charging with 77-µA pull-up current. After the $C_{(TMR)}$ charges up to $V_{(TMR\_FLT)}$, $\overline{FLT\_I}$ asserts low providing warning on impending FET turn OFF. After $C_{(TMR)}$ charges to $V_{(TMR\_OC)}$, PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The $C_{(TMR)}$ capacitor starts discharging with 2.5-µA pull-down current. After the voltage reaches $V_{(TMR\_Low)}$ level, the capacitor starts charging with 2.5-µA pull up. After 32 charging/discharging cycles of $C_{(TMR)}$ the FET turns ON back and $\overline{FLT\_I}$ de-asserts after de-assertion delay of 260 µs.

Use Equation 5 to calculate the T_{OC} duration.

$$T_{OC} = \frac{1.2 \times C_{TMR}}{77.5\ \mu} \quad (5)$$

Where, T_{OC} is the delay to turn OFF the FET, C_{TMR} is the capacitance across TMR to GND.

Use Equation 6 to calculate the T_{FLT} duration.

$$T_{FLT} = \frac{1.1 \times C_{TMR}}{77.5\ \mu} \quad (6)$$

Where, T_{FLT} is the $\overline{FLT\_I}$ assertion delay.

The auto-retry time can be computed as, $T_{RETRY} = 22.7 \times 10^6 \times C_{TMR}$

If the overcurrent pulse duration is below $T_{(OC)}$ then the FET remains ON and $C_{(TMR)}$ gets discharged using internal pull down switch.

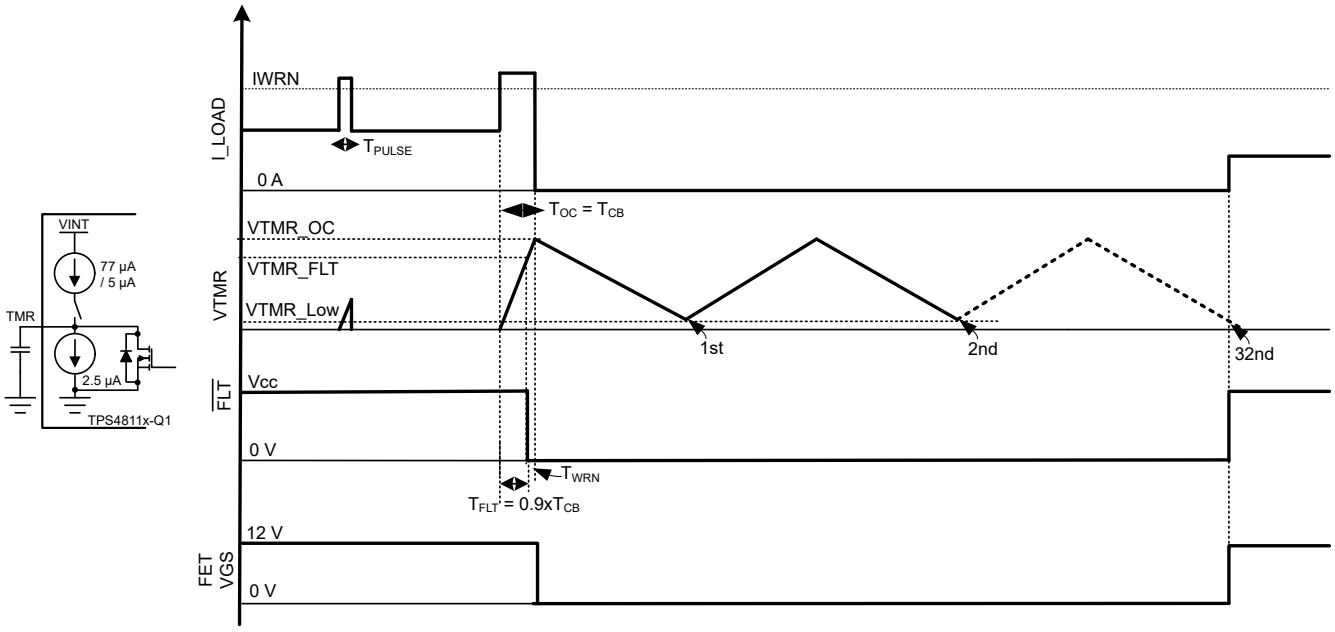


Figure 8-6. *Overcurrent Protection With Auto-Retry*

8.3.3.2 Overcurrent Protection With Latch-Off

Connect an approximately 100-kΩ resistor across $C_{(TMR)}$ as shown Figure 8-7. With this resistor, during the charging cycle, the voltage across $C_{(TMR)}$ gets clamped to a level below $V_{(TMR\_OC)}$ resulting in a latch-off behavior.

Toggle INP or EN/UVLO (below ENF) or power cycle VS below V_{SPORF} to reset the latch. At low edge, the timer counter is reset and $C_{(TMR)}$ is discharged. PU pulls up to BST when INP is pulled high.

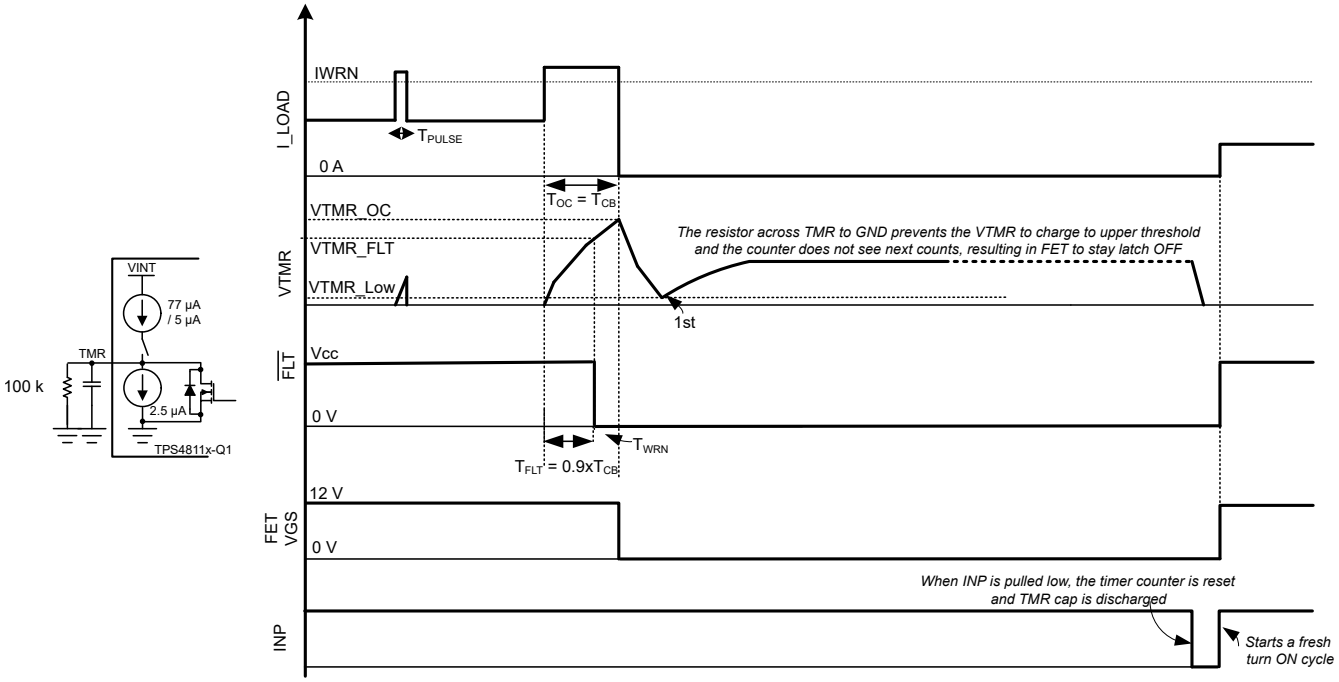


Figure 8-7. *Overcurrent Protection With Latch-Off*

8.3.4 Short-Circuit Protection

Connect a resistor, R_{ISCP} as shown in Figure 8-8.

Use Equation 7 to calculate the required R_{ISCP} value.

$$R_{ISCP}(\ \ ) = \frac{I_{SCP} \times R_{SNS}}{14.5\ \mu} - 600 \tag{7}$$

Once the sensed voltage across CS+ and CS– exceeds the ISCP set point, PD pulls low to SRC within 1.2µs in TPS48111-Q1 and 5 µs in TPS48110-Q1, protecting the FET. $\overline{FLT\_I}$ asserts low at the same time. Subsequent to this event, the charge and discharge cycles of $C_{(TMR)}$ starts similar to the behavior post FET OFF event in circuit breaker operation.

Latch-off can also achieved in the similar way as explained in the circuit breaker section.

8.3.5 Analog Current Monitor Output (IMON)

TPS4811x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain.

Use Equation 8 to calculate the V_{IMON}.

$$V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \text{Gain} \tag{8}$$

Where V_{SNS} = ILOAD × R_{SNS} and V_{OS_SET} is the input referred offset (± 350 µV) of the current sense amplifier (V_{SNS} to V_{IMON} scaling). Gain can be calculated using Equation 9

$$\text{Gain} = \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (9)$$

Where 0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

For linear performance ensure that V_{IMON} is set < 5.5 V at maximum system load condition. IMON pin has an internal clamp of 6.5 V (typ).

Accuracy of the current mirror factor is < ± 1%. The overall accuracy of IMON can be computed approximately using Equation 10

$$\%\ V_{IMON} = \frac{V_{OS\_SET}}{V_{SNS}} \times 100 \quad (10)$$

Figure 8-8 shows external connections and simplified block diagram of current sensing and over current protection (IWRN, ISCP) implementation.

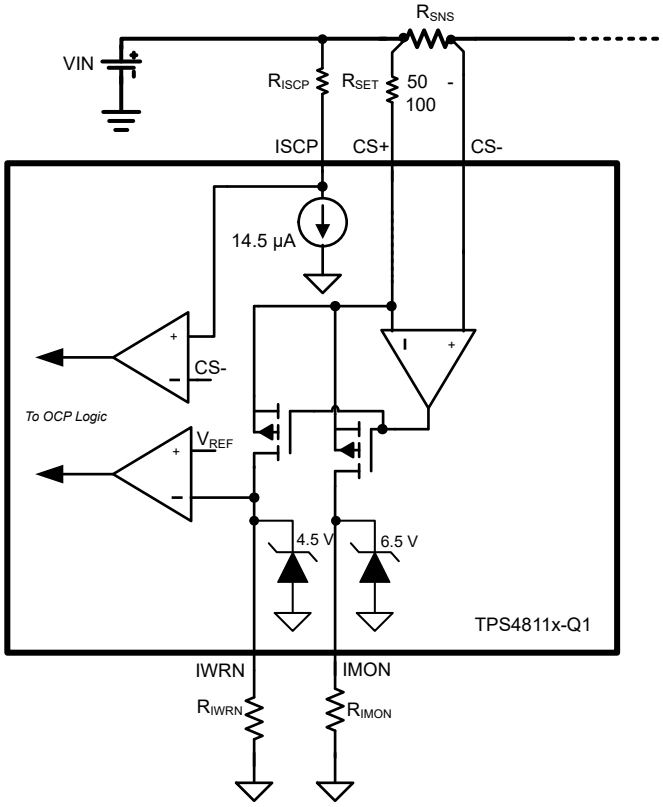


Figure 8-8. Current sensing and over current protection

ADVANCE INFORMATION

8.3.6 Overvoltage (OV) and Undervoltage Protection (UVLO)

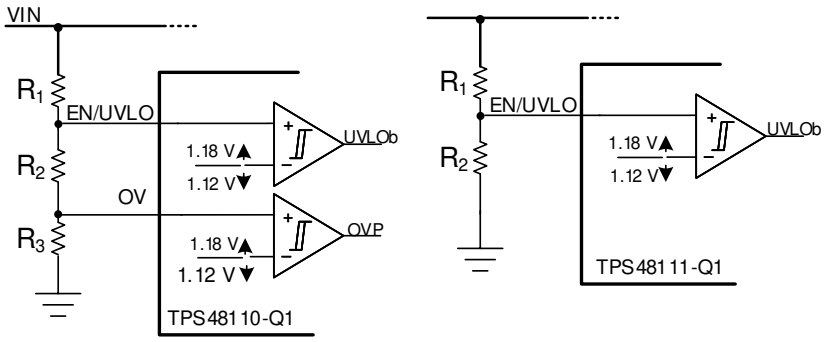


Figure 8-9. Programming Overvoltage and Undervoltage Protection Threshold

8.3.7 Remote Temperature sensing and Protection (DIODE)

The device features an integrated remote temperature sensing, protection and dedicated fault output. With a companion BJT, MMBT3904 as a remote temperature sense element, the controller gets the temperature information of the sense point. Connect the DIODE pin of TPS4811x-Q1 to the collector, base of a MMBT3904 BJT. After the sensed temperature reaches approximately 155ºC, the device pulls PD low to SRC, turning off the external FET and also asserts $\overline{FLT\_T}$ low. After the temperature reduces to 125ºC (minimum), an internally fixed auto-retry cycle of 512 ms commences. $\overline{FLT\_T}$ de-asserts and the external FET turns ON after the retry duration of 512 ms is lapsed.

In TPS48111-Q1, after the sensed temperature crosses 155°C, PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. Latch gets reset by toggling EN/UVLO below $V_{(ENF)}$ or by power cycling VS below V_{SPORF}.

8.3.8 TPS4811x-Q1 as a Simple Gate Driver

Figure 8-10 shows application schematics of TPS4811x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features like two- level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.

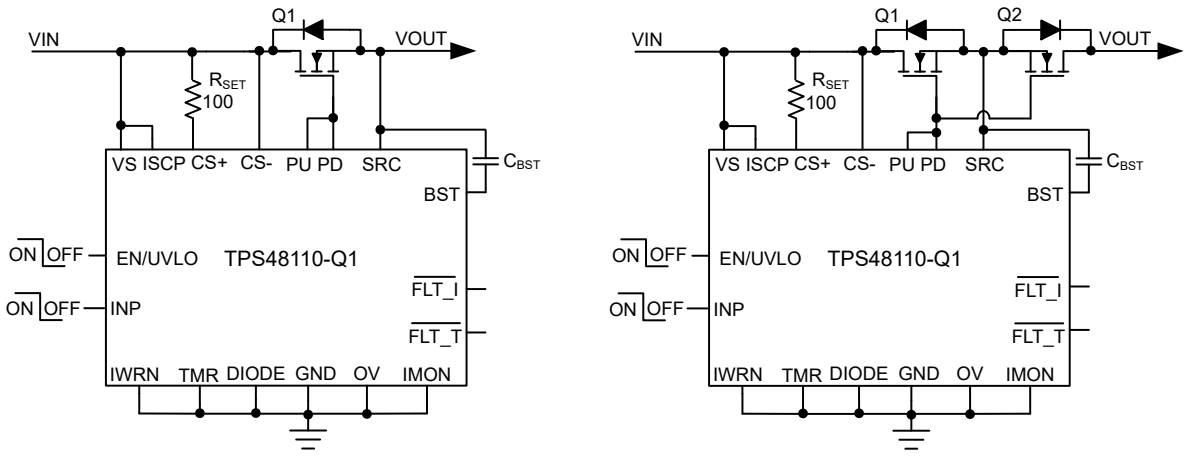


Figure 8-10. Connection Diagram of TPS48110-Q1 for Simple Gate Driver Design

8.4 Device Functional Mode (Shutdown Mode)

The TPS4811x-Q1 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold, $V_{(ENF)}$. The gate drivers and the charge pump are disabled in shutdown mode. During shutdown mode, the TPS4811x-Q1 enters low IQ operation with a total input quiescent consumption of 1.7 µA (typical).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS4811x-Q1 family is a 100-V smart high side driver with protection and diagnostics. The TPS4811x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 4-A source and sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in Powertrain (DC/DC converter), Battery Management System, Electric Power Steering, and driving PTC heater loads etc. The TPS4811x-Q1 device provides two-level adjustable overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS48111-Q1 features a separate pre-charge driver (G) with independent control input (INP_G). This feature enables system designs that need to pre-charge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool *TPS4811-Q1 Design Calculator* is available in the web product folder.

9.2 Typical Application: Driving HVAC PTC Heater Load on KL40 Line in Power Distribution Unit

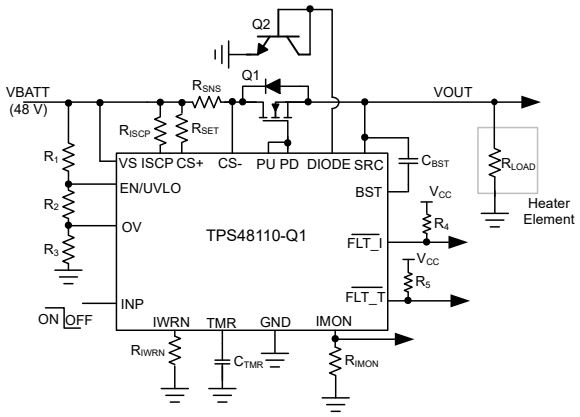


Figure 9-1. Typical Application Schematic: Driving HVAC PTC Heater

ADVANCE INFORMATION

9.2.1 Design Requirements

Table 9-1 shows the design parameters for this application example.

Table 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	48 V
Undervoltage lockout set point, VIN_{UVLO}	24 V
OV set point, VIN_{OVP}	58 V
Maximum load current, I_{OUT}	12 A
Overcurrent protection threshold, I_{WRN}	15 A
Short-circuit protection threshold, I_{SCP}	20 A
Fault timer period (T_{OC})	1 ms
Fault response	Auto-retry
Load resistance, R_{LOAD}	4 ± 0.2 Ω
Load switching frequency, F_{SW}	100 Hz

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$, extends from 10 mV to 30 mV. Values near the low threshold of 10 mV can be affected by the system noise. Values near the upper threshold of 30 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25 mV is selected as the overcurrent protection threshold voltage. The current sense resistor, R_{SNS} can be calculated using Equation 11.

$$R_{SNS} = \frac{V_{(SNS\text{-}WRN)}}{I_{WRN}} = \frac{25\ mV}{15\ A} = 1.66\ m \quad (11)$$

The next smaller available sense resistor 1.5 mΩ, 1% is chosen.

Selection of Scaling Resistor, R_{SET}

R_{SET} is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with R_{IWRN} and R_{IMON} to determine the overcurrent protection threshold and current monitoring output. The recommended range of R_{SET} is 50 Ω–100 Ω.

R_{SET} is selected as 100 Ω, 1% for this design example.

Programming the Overcurrent Protection Threshold – R_{IWRN} Selection

The R_{IWRN} sets the overcurrent protection (circuit breaker detection) threshold, whose value can be calculated using Equation 12.

$$R_{IWRN}(\ ) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{WRN}} \quad (12)$$

To set 15 A as overcurrent protection threshold, R_{IWRN} value is calculated to be 52.88 Ω.

Choose the closest available standard value: 54 Ω, 1%

.

Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold, whose value can be calculated using Equation 13.

$$R_{ISCP}\ (\ \ ) = \frac{I_{SCP} \times R_{SNS}}{14.5\ \mu} - 600 \tag{13}$$

To set 20 A as overcurrent protection threshold, R_{ISCP} value is calculated to be 1.4 kΩ.

Choose the closest available standard value: 1.43 kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between I_{SCP} and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF across I_{SCP} and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

Programming the Fault timer Period – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, T_{OC} (or circuit breaker interval, T_{CB}) can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. The value of C_{TMR} to set 1 ms for T_{OC} can be calculated using Equation 14.

$$C_{TMR} = \frac{T_{OC} \times 77.5\ \mu A}{1.2} = 64.58\ nF \tag{14}$$

Choose closest available standard value: 68 nF, 10%.

Selection of MOSFET, Q_1

For selecting the MOSFET Q_1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 60 V as the maximum application voltage, MOSFETs with V_{DS} voltage rating of 80 V is suitable for this application.

The maximum V_{GS} TPS4811-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, IPB160N08S4-03ATMA1 is selected and its ratings are:

- 80-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.6-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 86 nC

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100 µA. In case of switching applications, the BST must be powered externally from 12-V supply through a low-leakage silicon diode such as CMHD3595 to avoid collapsing the BST-SRC supply. This need is determined by the value of the switching frequency and MOSFET gate charge.

The maximum possible frequency without external supply is given by Equation 15.

ADVANCE INFORMATION

$$F_{SW,max} = \frac{I_{(BST)}}{2 \times Q_{g(total)}} = 581\ Hz \quad (15)$$

As the present application is switched at 100 Hz, external supply is not required. The minimum value of the bootstrap capacitor can be calculated using Equation 16.

$$C_{BST} = \frac{Q_{g(total)}}{1\ V} = 86\ nF \quad (16)$$

Choose closest available standard value: 100 nF, 10 %.

Setting the Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage set point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between VS, EN/UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 17 and Equation 18.

$$V_{(OVR)} = \frac{R_3}{(R_1 + R_2 + R_3)} \times VIN_{OVP} \quad (17)$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times VIN_{UVLO} \quad (18)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1, R_2 and R_3. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVR)}$ = 1.18 V and $V_{(UVLOR)}$ = 1.18 V. From the design requirements, VIN_{OVP} is 58 V and VIN_{UVLO} is 24 V. To solve the equation, first choose the value of R_1 = 470 kΩ and use Equation 18 to solve for $(R_2 + R_3)$ = 24.3 kΩ. Use Equation 17 and value of $(R_2 + R_3)$ to solve for R_3 = 10.1 kΩ and finally R_2 = 14.2 kΩ. Choose the closest standard 1 % resistor values: R_1 = 470 kΩ, R_2 = 14.3 kΩ, and R_3 = 10.2 kΩ.

Choosing the Current Monitoring Resistor, R_{IMON}

Voltage at IMON pin V_{IMON} is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the input voltage range of the ADC used. R_{IMON} is set using Equation 19.

$$V_{IMON} = (V_{SNS} + V_{OS\_SET}) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (19)$$

Where $V_{SNS} = I_{WRN} \times R_{SNS}$ and V_{OS_SET} is the input referred offset (± 350 µV) of the current sense amplifier.

For I_{WRN} = 15 A and considering the operating range of ADC to be 0 V to 3.3 V (for example, V_{IMON} = 3.3 V), R_{IMON} can be calculated as

$$R_{IMON} = \frac{V_{IMON} \times R_{SET}}{(V_{SNS} + V_{OS\_SET}) \times 0.9} = 16.52\ k \quad (20)$$

Selecting R_{IMON} value less than shown in Equation 20 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5 kΩ, 1%.

ADVANCE INFORMATION

9.2.3 Application Curves

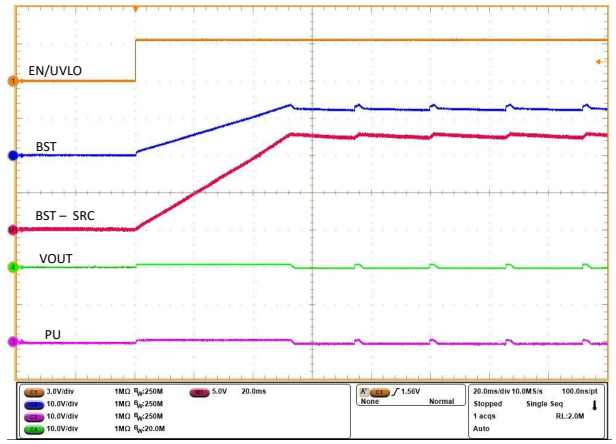


Figure 9-2. Start-Up Profile of Bootstrap Voltage for INP = GND

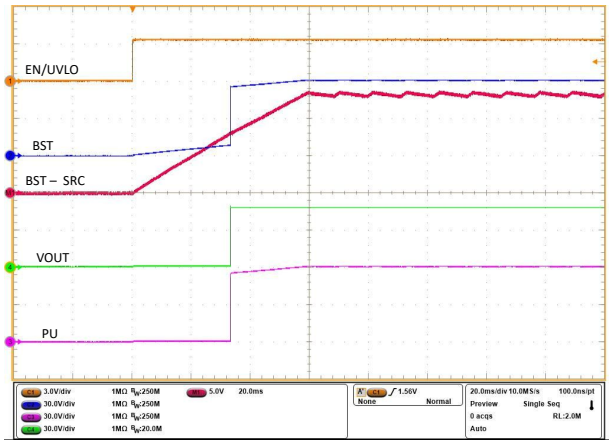


Figure 9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH

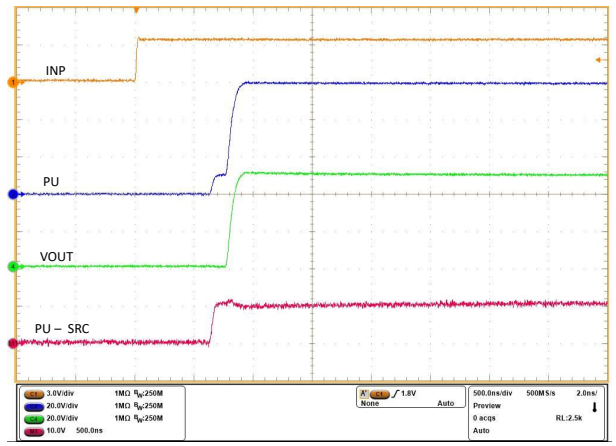


Figure 9-4. Turn-ON Response of TPS48110-Q1 for INP -> LOW to HIGH

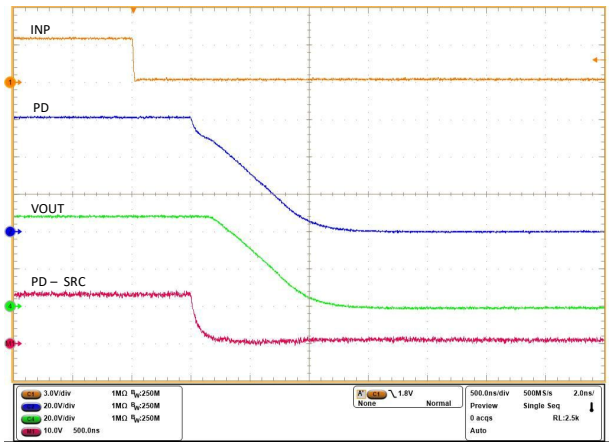


Figure 9-5. Turn-OFF Response of TPS48110-Q1 for INP -> HIGH to LOW

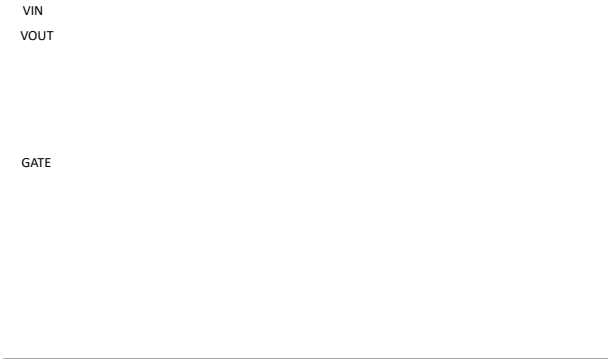


Figure 9-6. Overvoltage Cut-off Response at 58-V Level of TPS48110-Q1

Figure 9-7. Load Switching at 100 Hz With TPS48110-Q1

ADVANCE INFORMATION

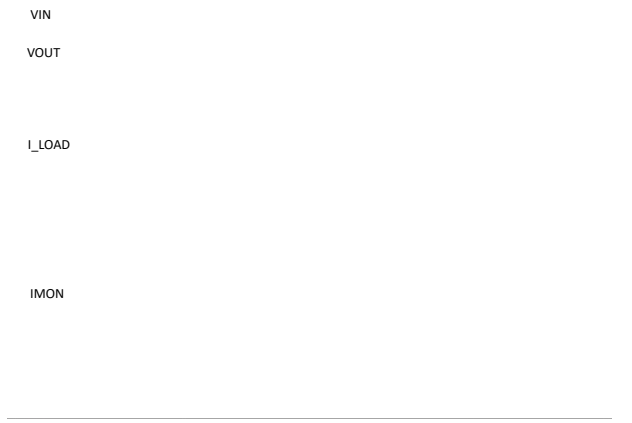


Figure 9-8. IMON Response During 10-A Load Step

Figure 9-9. Overcurrent Response of TPS48110-Q1 for a Load Step from 5 A to 18 A With 15-A Overcurrent Protection Setting

Figure 9-10. Auto-Retry Response of TPS48110-Q1 for an Overcurrent Fault

Figure 9-11. Latch-off Response of TPS48110-Q1 for an Overcurrent Fault

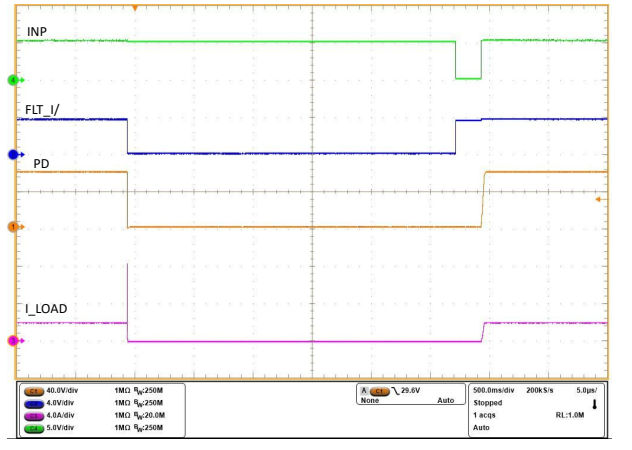


Figure 9-12. Response During Coming Out of Overload Fault With INP Reset

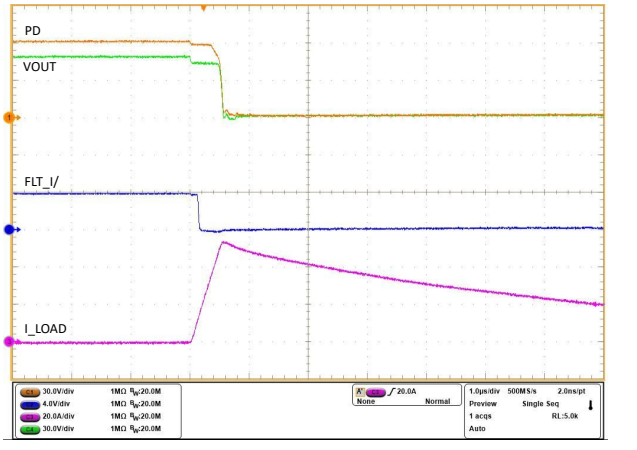


Figure 9-13. Output Hot-Short Response of the TPS48110-Q1 Device

9.3 Tpyical Application: Driving B2B FETs With Pre-Charging the Output Capacitance

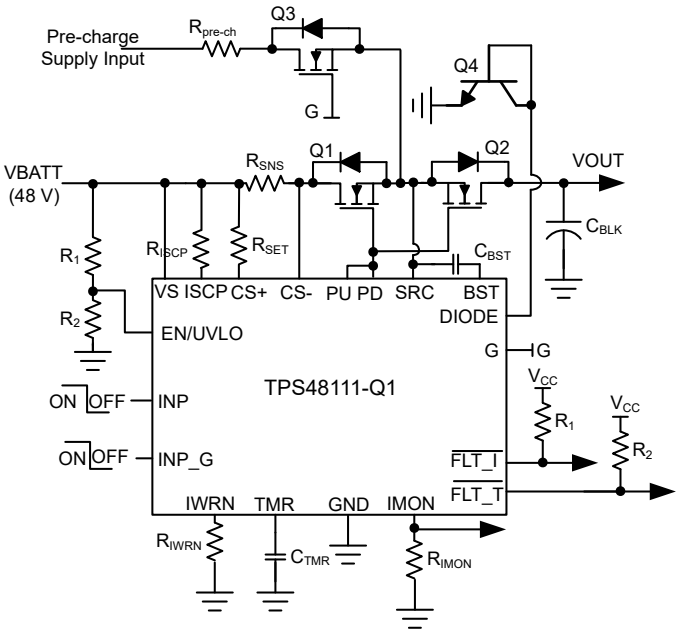


Figure 9-14. Typical Application Schematic: Driving DC-DC Converter Loads in Powertrain

9.3.1 Design Requirements

Table 9-2 shows the design parameters for this application example.

Table 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	48 V
Undervoltage lockout set point, VIN_{UVLO}	24 V
Maximum load current, I_{OUT}	40 A
Overcurrent protection threshold, I_{WRN}	50 A
Short-circuit protection threshold, I_{SCP}	60 A
Fault timer period (T_{OC})	1 ms
Fault response	Latch-off
Load capacitance, C_{OUT}	400 µF
Inrush current limit, I_{inrush}	500 mA

9.3.2 External Component Selection

By following similar design procedure as outlined in *Detailed Design Procedure*, the external component values are calculated as below:

- R_{SNS} = 500 µΩ
- R_{SET} = 100 Ω
- R_{IWRN} = 47 kΩ to set 50 A as overcurrent protection threshold
- R_{ISCP} = 1.4 kΩ to set 60 A as short-circuit protection threshold
- C_{TMR} = 68 nF to set 1 ms circuit breaker time
- R_1 and R_2 are selected as 470 kΩ and 24.9 kΩ respectively to set VIN undervoltage lockout threshold at 24 V
- R_{IMON} = 15 kΩ to limit maximum $V_{(IMON)}$ voltage to 3.3 V at full-load current of 50 A
- To reduce conduction losses, IAUS300N08S5N012 MOSFET is selected. Two FETs are used in parallel for control and another two FETs are used in parallel for reverse current blocking

ADVANCE INFORMATION

  - 80-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
  - $R_{DS(ON)}$ is 1-mΩ typical at 10-V V_{GS}
  - Q_g of each MOSFET is 231 nC
- $C_{BST} = (4 \times Q_g) / 1\ V = 1\ \mu F$

Selection of Pre-Charge Resistor

The value of pre-charge resistor must be selected to limit the inrush current to I_{inrush} as per Equation 21.

$$R_{pre\text{-}ch} = \frac{V_{IN}}{I_{inrush}} = 96 \tag{21}$$

The power rating of the pre-charge resistor is decided by the average power dissipation given by Equation 22.

$$P_{avg} = \frac{E_{pre\text{-}ch}}{T_{pre\text{-}ch}} = \frac{0.5 \times C_{OUT} \times V_{IN}^2}{5 \times R_{pre\text{-}ch} \times C_{OUT}} = 2.4\ W \tag{22}$$

The peak power dissipation in the pre-charge resistor is given by Equation 23.

$$P_{peak} = \frac{V_{IN}^2}{R_{pre\text{-}ch}} = 24\ W \tag{23}$$

Two 220-Ω, 1.5-W, 5% CRCW2512220RJNEGHP resistors are used in parallel to support both average and peak power dissipation.

TI suggests the designer to share the entire power dissipation profile of pre-charge resistor with the resistor manufacturer and get their recommendation.

ADVANCE INFORMATION

9.3.3 Application Curves

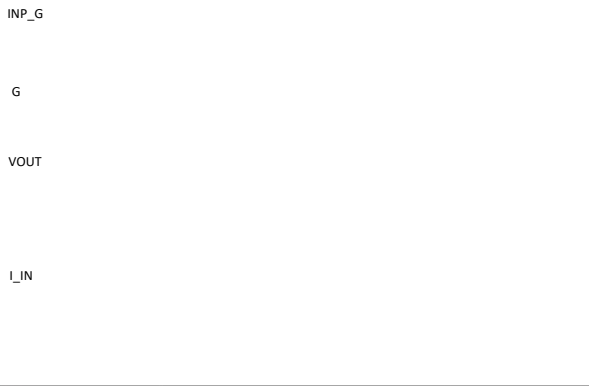


Figure 9-15. Pre-charge Profile of the Output Capacitance (VIN = 48 V, C_{OUT} = 440 µF, No Load)

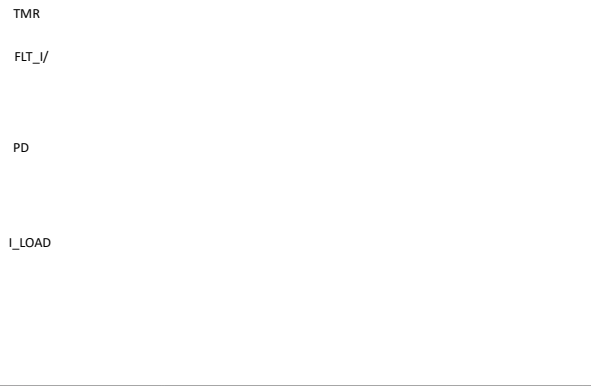


Figure 9-16. Overcurrent Response of TPS48111-Q1 for a Load Step from 24 A to 54 A With 50-A Overcurrent Protection Setting

Figure 9-17. IMON Response During 40-A Load Step

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

- The sense resistor (R_{SNS}) must be placed close to the TPS4811x-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high current path from the board's input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS4811x-Q1 must be connected directly to each other, and to the TPS4811x-Q1's GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000 pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.

10.2 Layout Example

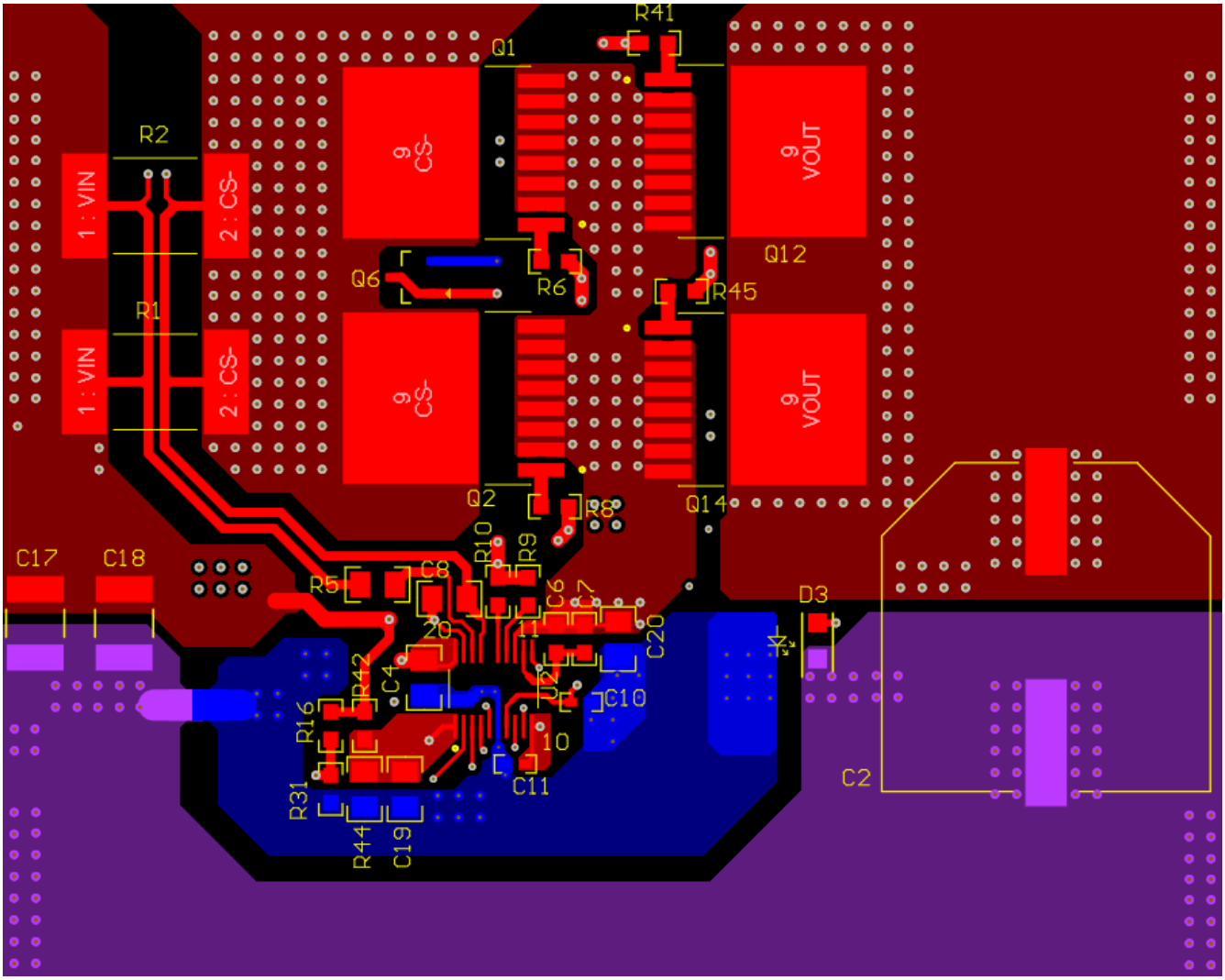


Figure 10-1. Typical PCB Layout Example With TPS4811-Q1 With Two Parallel B2B MOSFETs

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

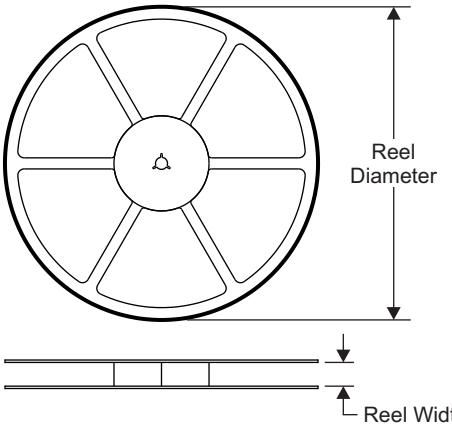
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

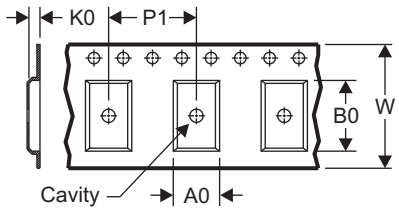
ADVANCE INFORMATION

12.1 Tape and Reel Information

REEL DIMENSIONS

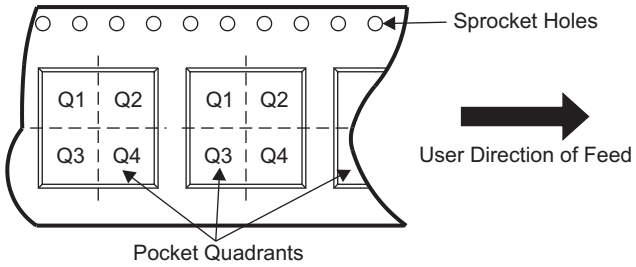


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

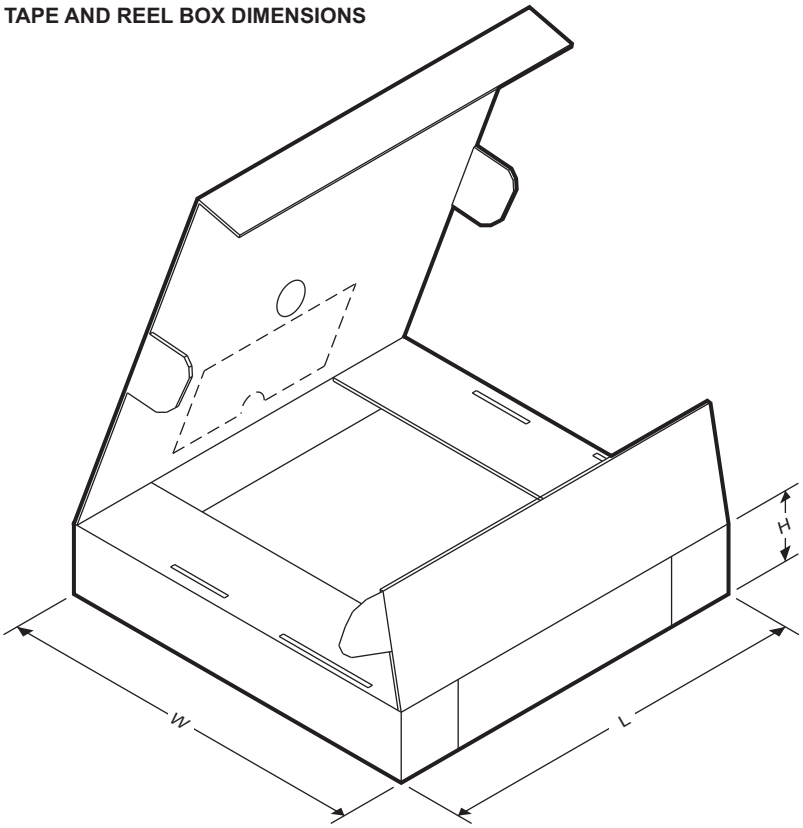


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS48110AQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.0	5.40	5.40	1.45	8.0	12.0	Q1
PTPS48111LQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.0	5.40	5.40	1.45	8.0	12.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



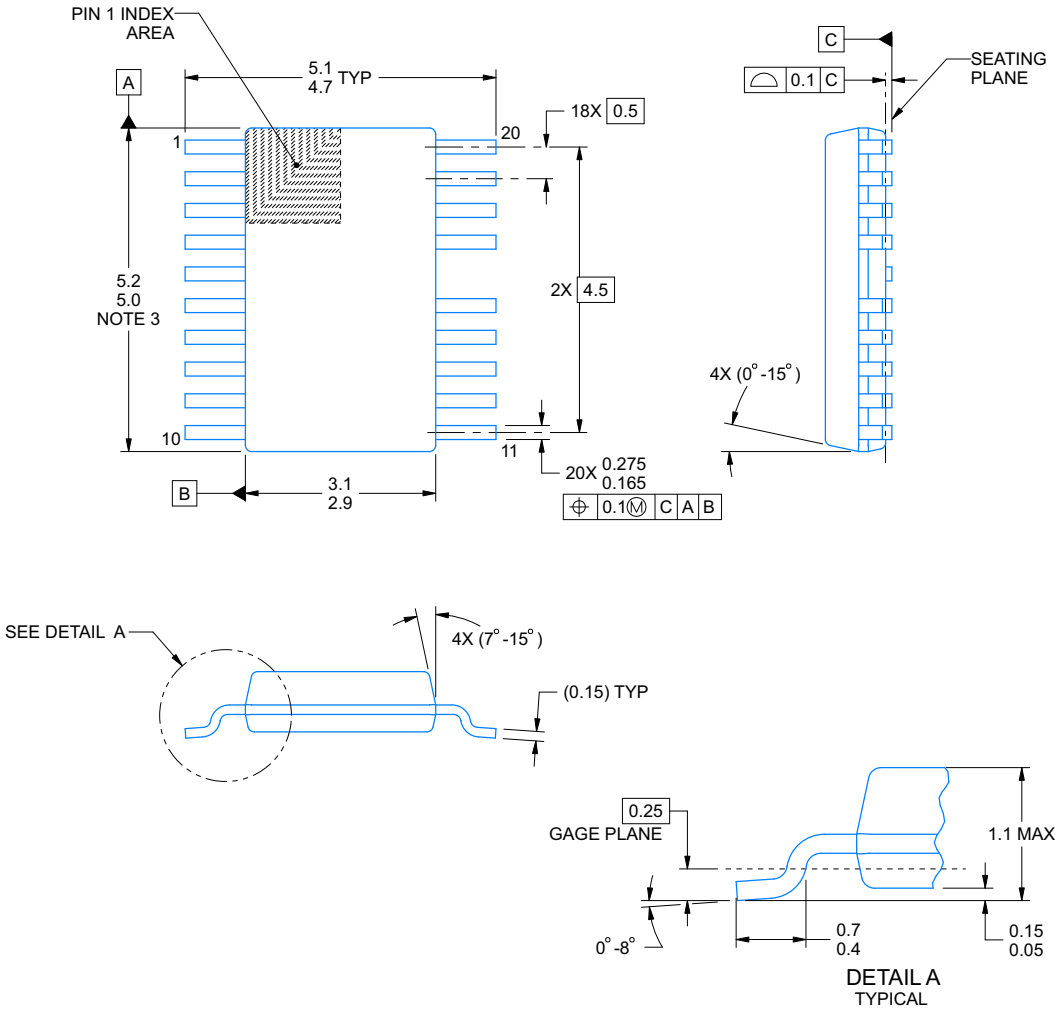
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS48110AQDGXRQ1	VSSOP	DGX	19	5000	853.0	449.0	35.0
PTPS48111LQDGXRQ1	VSSOP	DGX	19	5000	853.0	449.0	35.0

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.

www.ti.com

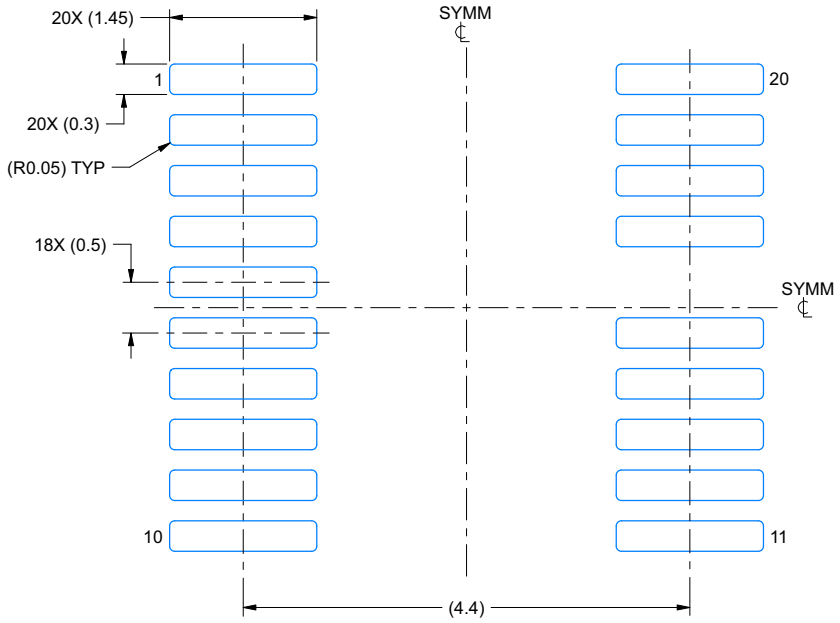
ADVANCE INFORMATION

ADVANCE INFORMATION

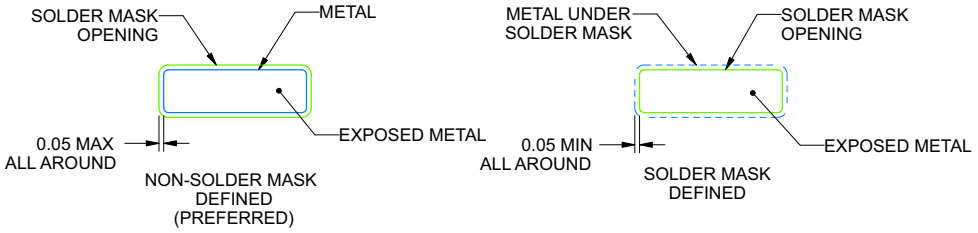
EXAMPLE BOARD LAYOUT

DGX0019A — VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

4226944/A 07/2021

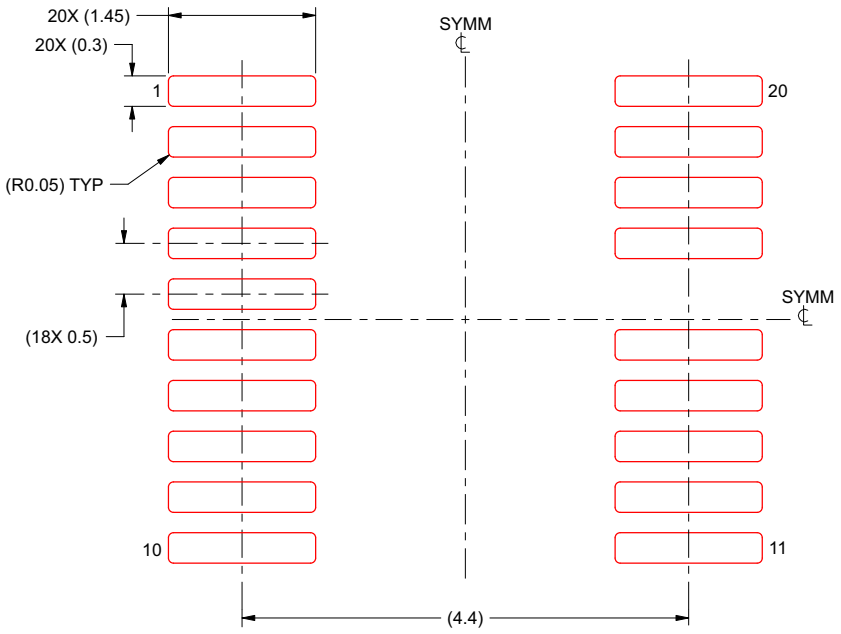
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGX0019A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS48111LQDGXRQ1	ACTIVE	VSSOP	DGX	19	4500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS22811
SLVSGU5 – APRIL 2022

TPS22811x 2.7 V–16 V, 10-A, 6-mΩ Load Switch with Adjustable Overvoltage Protection and Current Monitoring

ADVANCE INFORMATION

1 Features

- Wide operating input voltage range: 2.7 V to 16 V
  - 20-V absolute maximum
- Integrated FET with low On-resistance: R_{ON} = 6 mΩ (typ.)
- Adjustable output slew rate control (dVdt)
- Active high enable input with adjustable undervoltage lockout threshold (UVLO)
- Active low enable input with adjustable undervoltage lockout threshold (OVLO)
- Fast overvoltage protection
  - Adjustable overvoltage lockout (OVLO) with 1.2-µs (typ.) response time
- Analog load current monitor output (IMON)
  - • ±10 % accuracy for I_{OUT} > 2 A
- Fast-trip response for short-circuit protection
  - 640-ns (typ.) response time
  - Fixed threshold
- Overtemperature protection
- Power Good (PG) indication with adjustable threshold (PGTH)
- Quick output discharge
- Small footprint: QFN 2 mm × 2 mm, 0.45-mm pitch

2 Applications

- Optical modules
- Server/PC motherboard/add-on cards
- Enterprise routers/data center switches
- Industrial PC
- UHDTV

3 Description

The TPS22811x is a highly integrated power distribution solution in a small package. The device allows control and monitoring of power supply rails using minimum number of external components.

Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions by cutting off the output if input exceeds an adjustable overvoltage threshold. The device integrates a fast-trip response to provide protection against severe faults at the output during steady-state.

The devices provide an accurate analog sense of the output load current as well as a digital power good indication to help with system monitoring and diagnostics.

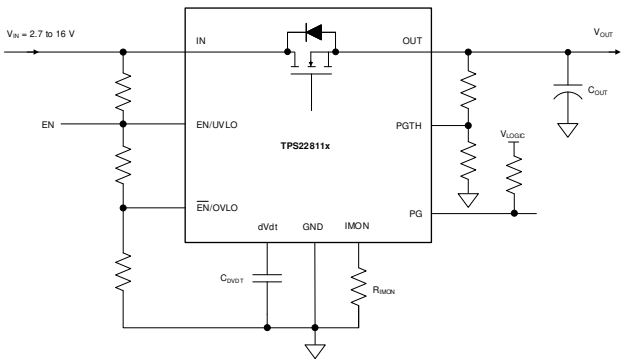
The devices are available in a 2-mm × 2-mm, 10-pin HotRod™ QFN package for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS22811LRPW	QFN (10)	2 mm × 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2022	*	Initial release.

5 Pin Configuration and Functions

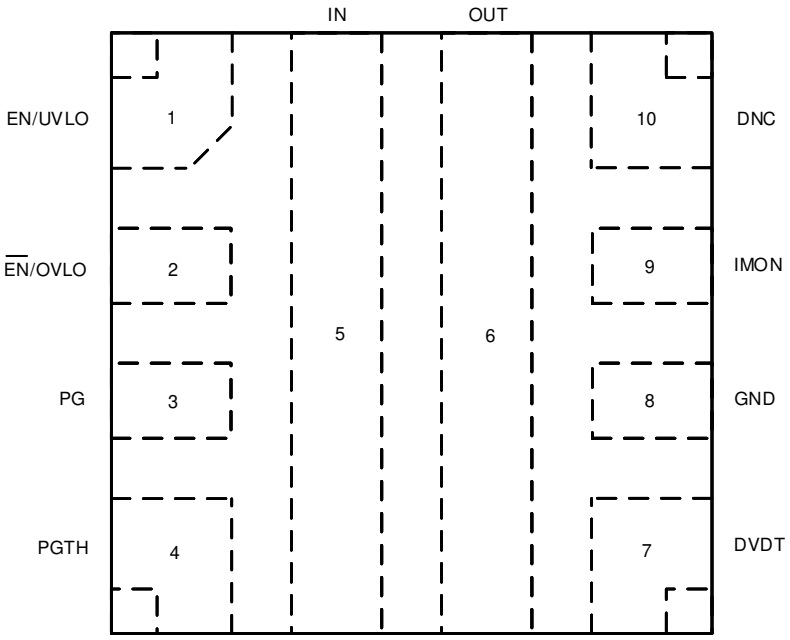


Figure 5-1. TPS22811x RPW Package 10-Pin QFN Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. *Do not leave floating.* Refer to *Undervoltage Lockout (UVLO and UVP)* for details.
$\overline{EN}$/OVLO	2	Analog Input	A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an active low enable for the device. *Do not leave floating.* Refer to *Overvoltage Lockout (OVLO)* for more details.
PG	3	Digital Output	Power Good indication. This pin is an open drain signal which is asserted high when the internal power path is fully turned ON and PGTH input exceeds a certain threshold. Refer to *Power Good Indication (PG)* for more details.
PGTH	4	Analog Input	Power Good threshold. Refer to *Power Good Indication (PG)* for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to *Slew Rate (dVdt) and Inrush Current Control* for more details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
IMON	9	Analog Output	Analog load current monitor output. An external resistor from this pin to GND sets the gain for the current monitor. This pin also provides a secondary function of setting the current limit during start-up. Connect to GND if neither of these features are used. *Do not leave floating.* Refer to *Analog Load Current Monitor* and *Active Current Limiting During Start-Up* for more details.
DNC	10	X	Do not connect anything to this pin.

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40°C ≤ T_J ≤ 125°C	IN	–0.3	20	V
V_{OUT}	Maximum output voltage range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	V_{IN} + 0.3	
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable pin voltage range	EN/UVLO	–0.3	6.5	V
V_{OV}	Maximum $\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT pin voltage range	dVdt	Internally limited		V
V_{PG}	Maximum PG pin voltage range	PG	–0.3	6.5	V
VPGTH	Maximum PGTH pin voltage range	PGTH	–0.3	6.5	V
V_{IMON}	Maximum IMON pin voltage range	IMON	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	10		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	16	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	$\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	0.5	1.5	V
V_{dVdT}	dVdT pin capacitor voltage rating	dVdt	V_{IN} + 5 V		V
V_{PGTH}	PGTH pin voltage range	PGTH		5	V
V_{PG}	PG pin voltage range	PG		5	V
I_{MAX}	Continuous switch current, T_J ≤ 125°C	IN to OUT		10	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

6.4 Thermal Information

THERMAL METRIC (1)		TPS25981xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7(2)	°C/W
		71.8(3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1(2)	°C/W
	Junction-to-top characterization parameter	1.3(3)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23 (2)	°C/W
		14.5 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

ADVANCE INFORMATION

ADVANCE INFORMATION

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{IMON} = 600 Ω , dVdT = Open, PGTH = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		384		µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		68		µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		2		µA
$V_{UVP(R)}$	IN supply UVP rising threshold		2.53		V
$V_{UVP(F)}$	IN supply UVP falling threshold		2.42		V
OUTPUT LOAD CURRENT MONITOR (IMON)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), 1.5 A ≤ I_{OUT} ≤ 11 A, I_{OUT} < I_{LIM}		95		µA/A
SHORT-CIRCUIT PROTECTION (OUT)					
I_{FT}	Fixed fast-trip current threshold		37		A
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} ≤ 4 V, I_{OUT} = 3 A, T_J = 25℃		6		mΩ
	4 < V_{IN} ≤ 16 V, I_{OUT} = 3 A, T_J = 25℃		5.8		mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold		1.2		V
$V_{UVLO(F)}$	EN/UVLO falling threshold		1.1		V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current		0.75		V
I_{ENLKG}	EN/UVLO pin leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT ($\overline{EN}$/OVLO)					
$V_{OV(R)}$	OVLO rising threshold		1.2		V
$V_{OV(F)}$	OVLO falling threshold		1.1		V
I_{OVLKG}	OVLO pin leakage current (0.5 V < V_{OVLO} < 1.5 V)	–0.1		0.1	µA
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pull-up (I_{PG} = 26 µA)			1000	mV
	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pull-up (I_{PG} = 242 µA)			1000	mV
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0	600	mV
I_{PGLKG}	PG pin leakage current, PG asserted			3	µA
POWER GOOD THRESHOLD (PGTH)					
$V_{PGTH(R)}$	PGTH rising threshold		1.2		V
$V_{PGTH(F)}$	PGTH falling threshold		1.09		V
$I_{PGTHLKG}$	PGTH leakage current	–1		1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J↑		154		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J↓		10		°C
DVDT					
I_{dVdt}	dVdt pin internal charging current		3.49		µA
QUICK OUTPUT DISCHARGE (OUT)					
R_{QOD}	Quick Output Discharge Resistance, V_{EN} < $V_{UVLO(F)}$		488		Ω

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT}↓		1.2		µs
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT}↓		640		ns
t_{PGA}	PG assertion de-glitch time			14		µs
t_{PGD}	PG de-assertion de-glitch time			14		µs

ADVANCE INFORMATION

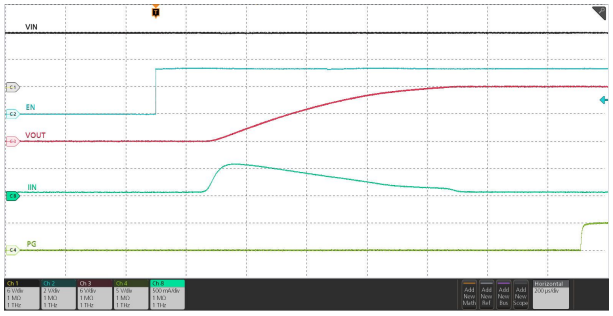
6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNITS
SR_{ON}	Output rising slew rate	2.7 V	8.19	1.30	0.78	V/ms
		5 V	11.28	1.42	0.84	
		12 V	19.71	1.68	0.98	
$t_{D,ON}$	Turn on delay	2.7 V	0.14	0.46	0.70	ms
		5 V	0.14	0.60	0.96	
		12 V	0.14	0.93	1.57	
t_R	Rise time	2.7 V	0.26	1.66	2.77	ms
		5 V	0.36	2.82	4.78	
		12 V	0.49	5.74	9.84	
t_{ON}	Turn on time	2.7 V	0.40	2.11	3.47	ms
		5 V	0.50	3.42	5.74	
		12 V	0.63	6.67	11.41	
$t_{D,OFF}$	Turn off delay	2.7 V	24.90	24.90	24.90	µs
		5 V	21.10	21.10	21.10	
		12 V	18.80	18.80	18.80	

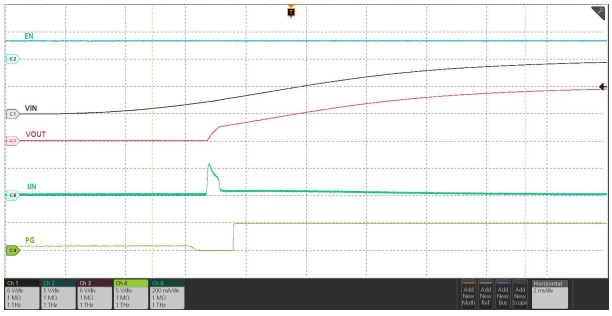
ADVANCE INFORMATION

6.8 Typical Characteristics



V_{IN} = 12 V, C_{OUT} = 10 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 3.3 V

Figure 6-1. Start-Up with Enable

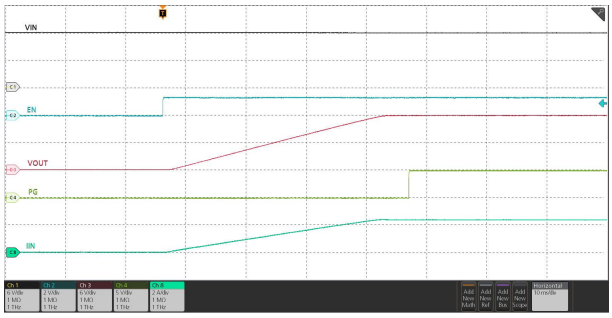


$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 10 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

Figure 6-2. Star- Up with Supply

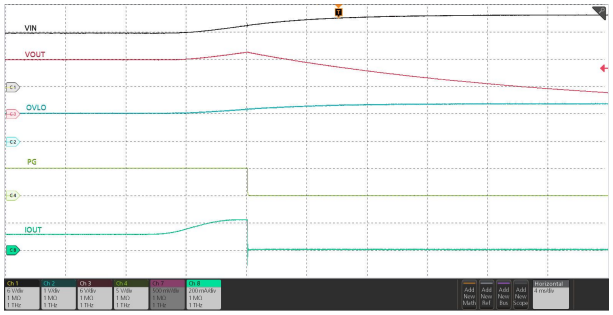
V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 6-3. Inrush Current with Capacitive Load



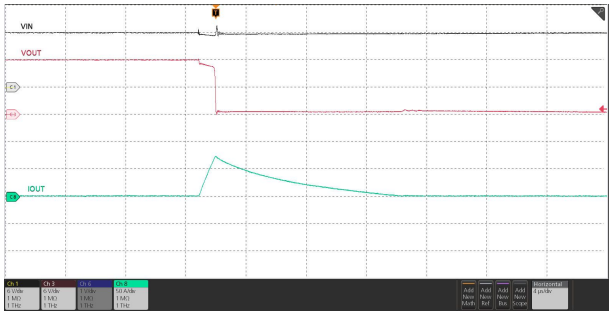
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 6-4. Inrush Current with Resistive and Capacitive Load



V_{IN} Overvoltage threshold set to 13.6 V using resistor ladder connected on OVLO pin, V_{IN} ramped up from 12 V to 16 V

Figure 6-5. Overvoltage Lockout Response

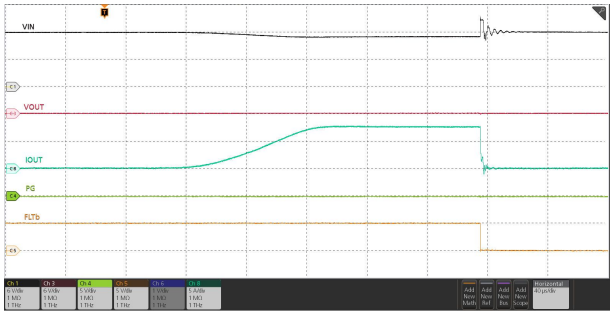


V_{IN} = 12 V, OUT stepped from open → short-circuit to GND

Figure 6-6. Output Short-Circuit During Steady State (Zoomed In)

ADVANCE INFORMATION

6.8 Typical Characteristics (continued)



V_{IN} = 12 V, C_{OUT} = Open, OUT short-circuit to GND, R_{IMON} = 649 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

Figure 6-7. Power Up into Short-Circuit

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

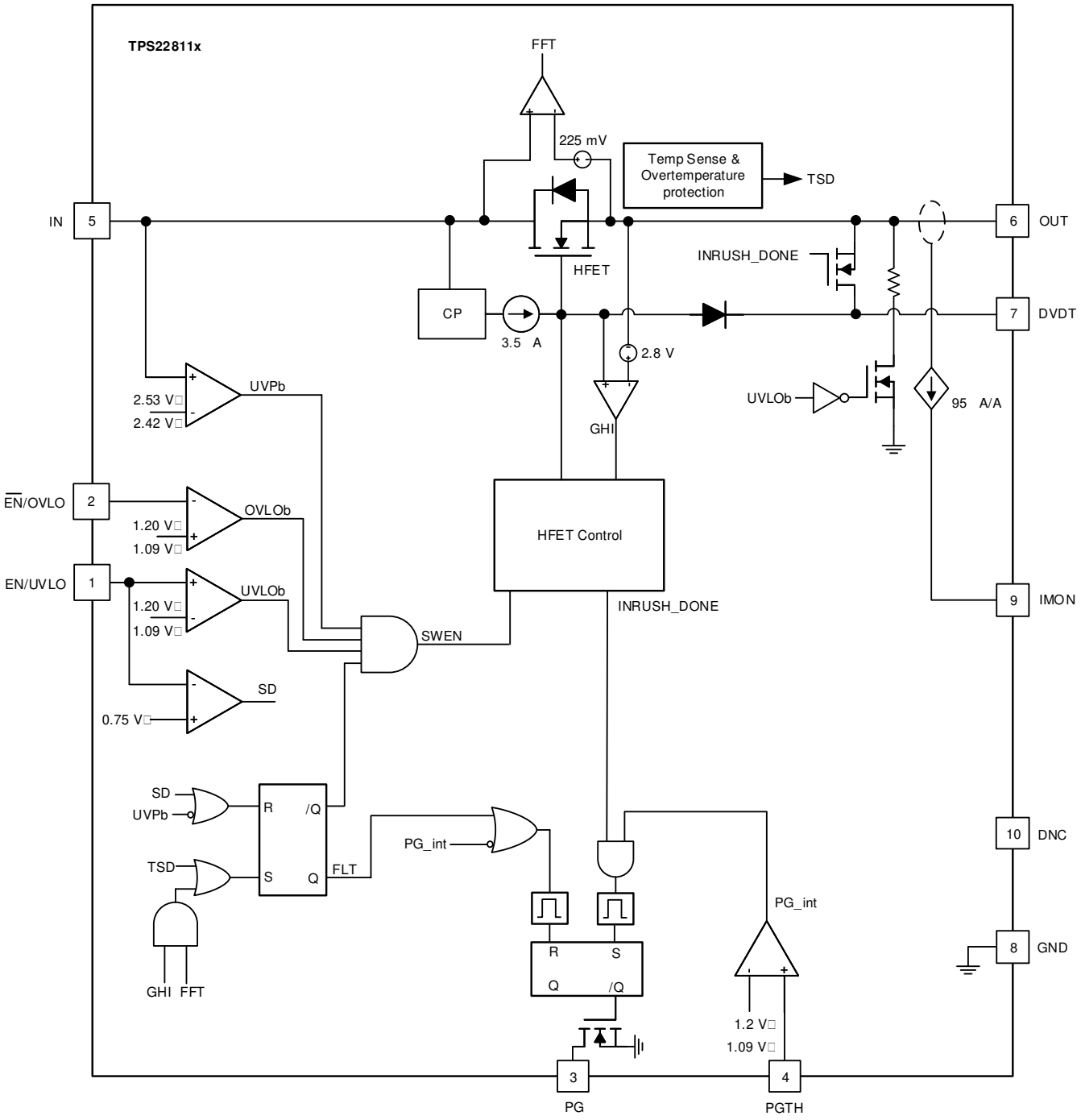
TPS22811x is an integrated load switch with protection and monitoring. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the undervoltage protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the fast-trip current threshold is not exceeded and overvoltage spikes are cut-off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). This feature keeps the system safe from harmful levels of voltage and current.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

ADVANCE INFORMATION

7.2 Functional Block Diagram



7.3 Feature Description

The TPS22811x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS22811x implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 7-1 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

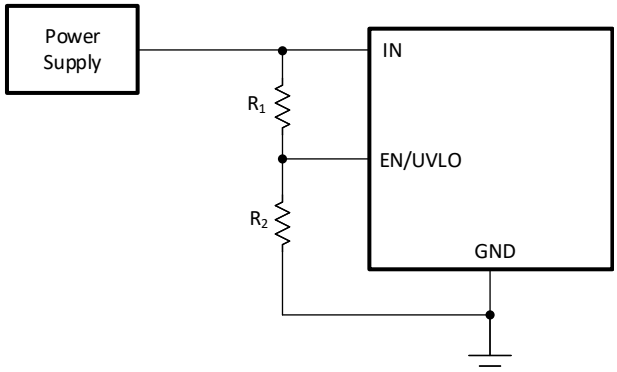


Figure 7-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

7.3.2 Overvoltage Lockout (OVLO)

The TPS22811x allows the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the $\overline{EN}$/OVLO pin allows the overvoltage protection threshold to be adjusted to a user defined value. After the voltage at the $\overline{EN}$/OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the $\overline{EN}$/OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. Figure 7-2 and Equation 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

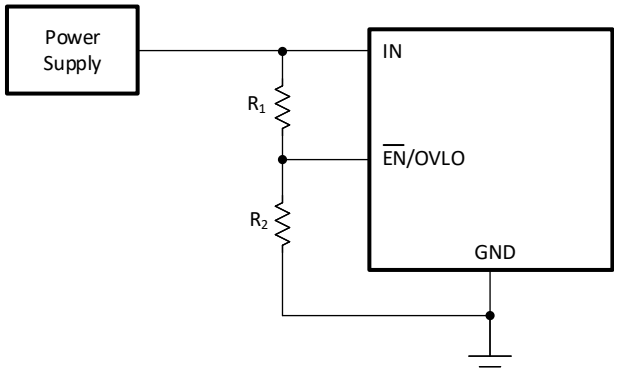


Figure 7-2. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

ADVANCE INFORMATION

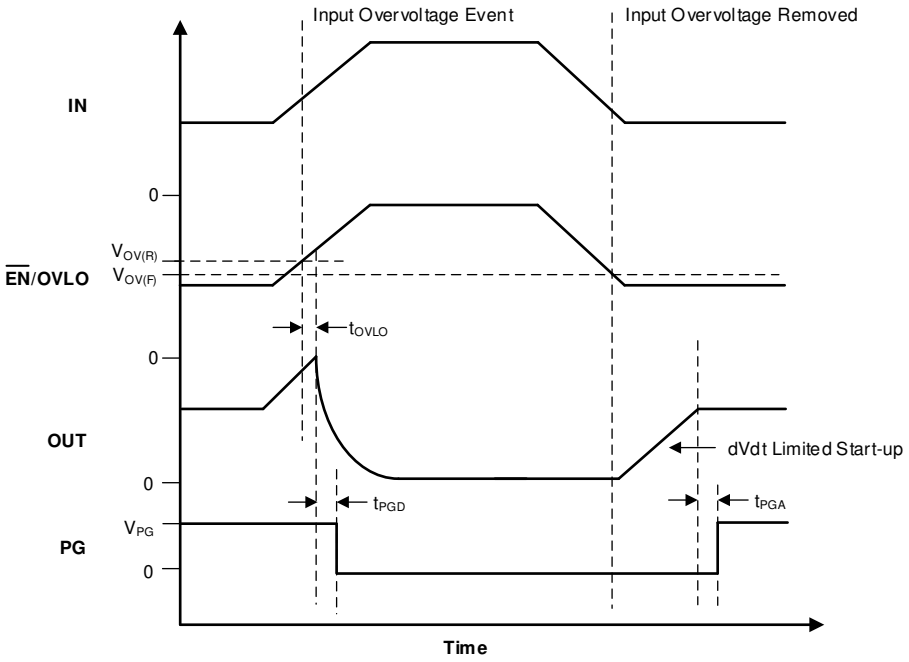


Figure 7-3. TPS22811x Overvoltage Lockout and Recovery

While recovering from a OVLO event, the TPS22811x starts up with inrush control (dVdt).

7.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS22811x incorporates three levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state
3. Adjustable current limit (I_{LIM}) for protection against overcurrent or short-circuit during start-up

7.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. Equation 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using Equation 4.

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

7.3.3.2 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the TPS22811x triggers a fast-trip response to cut off the power path. The device employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short-circuits during steady state. Once the current exceeds I_{FT}, the FET is turned off completely within t_{FT}. Thereafter, the device remains off till the device is power cycled or re-enabled using EN/UVLO pin.

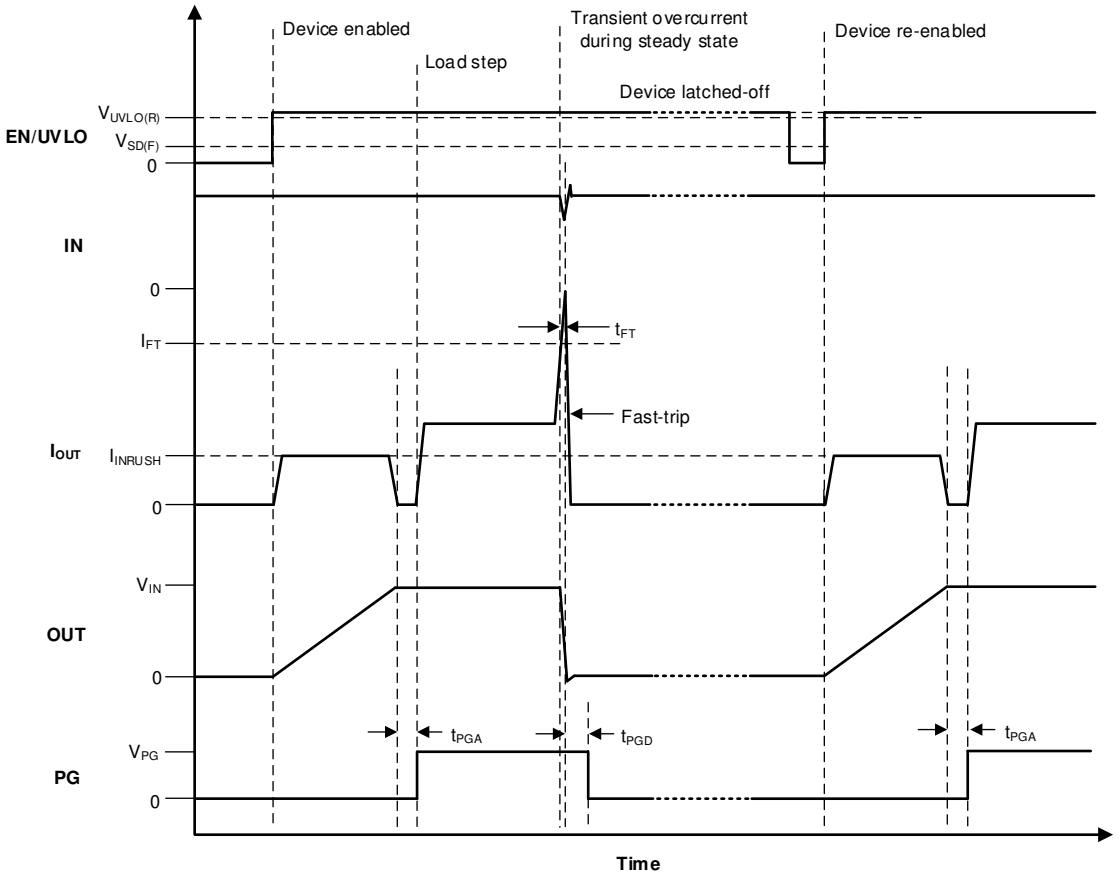


Figure 7-4. TPS22811x Short-Circuit Response

7.3.3.3 Active Current Limiting During Start-Up

The TPS22811x devices respond to output overcurrent conditions during start-up by actively limiting the current. If the load current exceeds the set overcurrent threshold (I_{LIM}) set by the IMON pin resistor (R_{IMON}), but stays lower than the fast-trip threshold (I_{FT}), the current limit loop starts regulating the FET to actively limit the current to the set overcurrent threshold (I_{LIM}). Equation 5 can be used to calculate the R_{IMON} value for a desired overcurrent threshold.

$$R_{IMON}\,(\Omega) = \frac{6595}{I_{LIM}\,(A)} \tag{5}$$

Note

1. Leaving the IMON pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the target current limit threshold (I_{LIM}).
3. Connecting the IMON pin to GND disables the active current limit protection during start-up.

ADVANCE INFORMATION

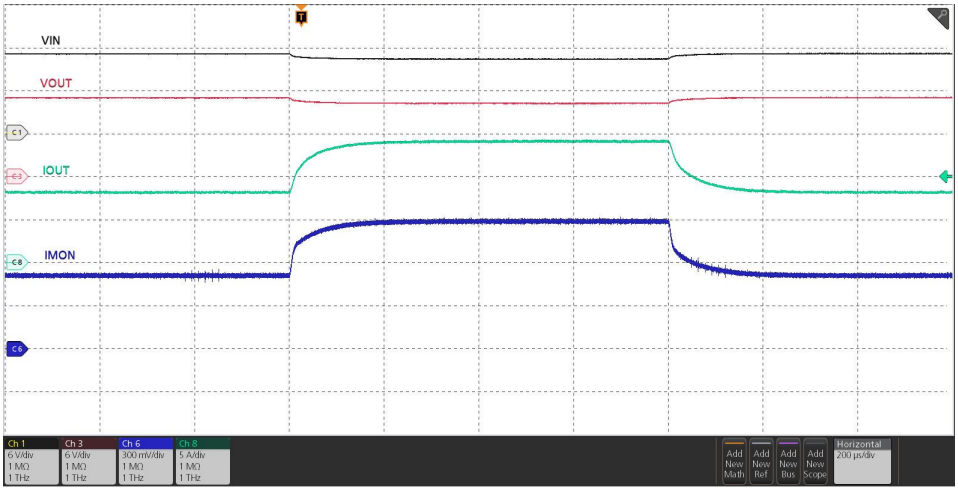
During active current limit, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to TSD fault, it stays latched off. See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

7.3.4 Analog Load Current Monitor

The TPS22811x allows the system to accurately monitor the output load current by providing an analog current sense output on the IMON pin which is proportional to the current through the FET. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current.

$$I_{LOAD}\,(A) = \frac{V_{IMON}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times R_{IMON}\,(\Omega)} \tag{6}$$

The waveform below shows the IMON signal response to a load step at the output.



V_{IN} = 12 V, R_{IMON} = 649 Ω, I_{OUT} varied dynamically between 8 A and 14 A

Figure 7-5. Analog Load Current Monitor Response

7.3.5 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device does turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS22811x detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled.

Table 7-1. Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

7.3.6 Fault Response

The following table summarizes the device response to various fault conditions.

Table 7-2. Fault Summary

Event	Protection Response	Fault Latched Internally
Overtemperature	Shutdown	Y
Undervoltage (UVP or UVLO)	Shutdown	N
Input overvoltage	Shutdown	N
Output short-circuit to GND	Fast-trip	Y

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device.

7.3.7 Power Good Indication (PG)

The TPS22811x provides an active high digital output (PG) which serves as a power good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.

ADVANCE INFORMATION

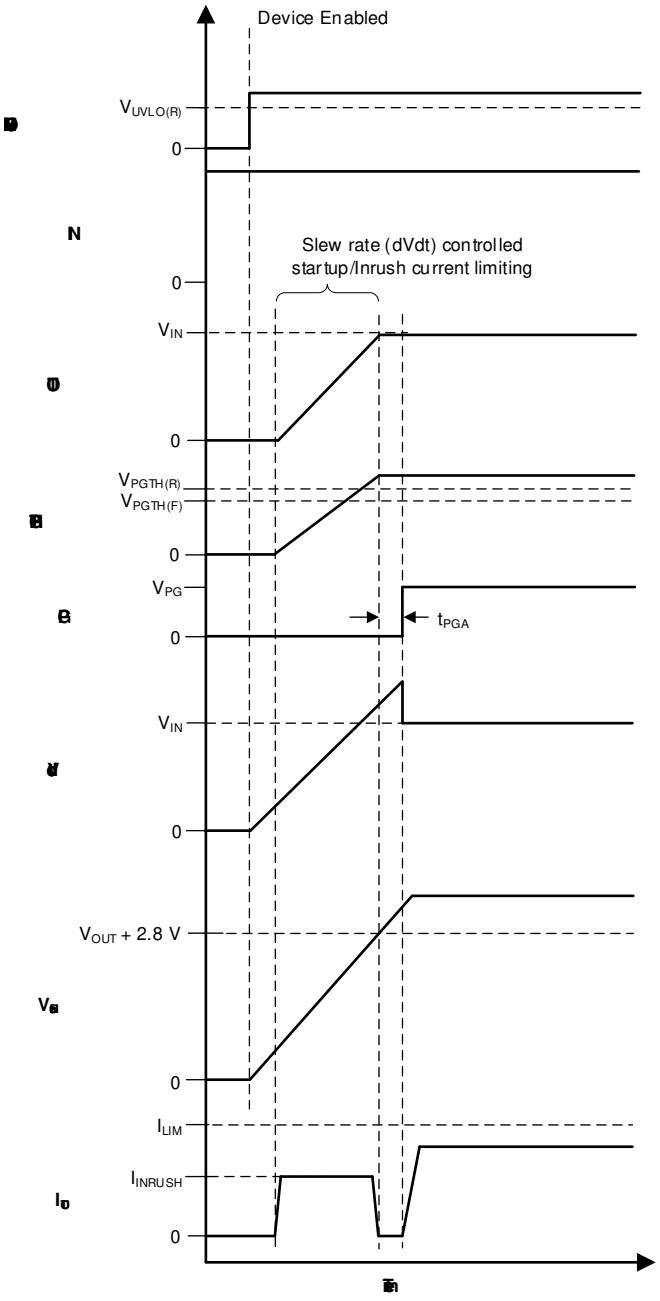


Figure 7-6. TPS22811xx PG Timing Diagram

Table 7-3. TPS22811x PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
Steady state	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Output short-circuit to GND	Fast-trip followed by Current Limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Overtemperature	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.3.8 Quick Output Discharge (QOD)

The TPS22811x has an integrated output discharge function which can be helpful in quickly removing residual charge left on the large output capacitors and avoids bus floating at some undefined voltage. The internal QOD pulldown FET on the OUT pin is activated when the EN/UVLO is held low ($V_{EN} < V_{UVLO(F)}$). The output discharge function can result in excess power dissipation inside the device leading to increase in junction temperature. The output discharge is disabled if the junction temperature (T_J) crosses the thermal shutdown threshold (TSD) to avoid long term degradation of the part.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS22811x is a 2.7-V to 16-V, 10-A load switch that is typically used for power rail protection applications. The device operates from 2.7 V to 16 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current. The device can be used in a variety of systems such as server motherboard/add-on cards/NIC, optical modules, enterprise switches/routers, Industrial PC, UHDTV. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS22811xx Design Calculator*, is available in the web product folder.

8.2 Single Device, Self-Controlled

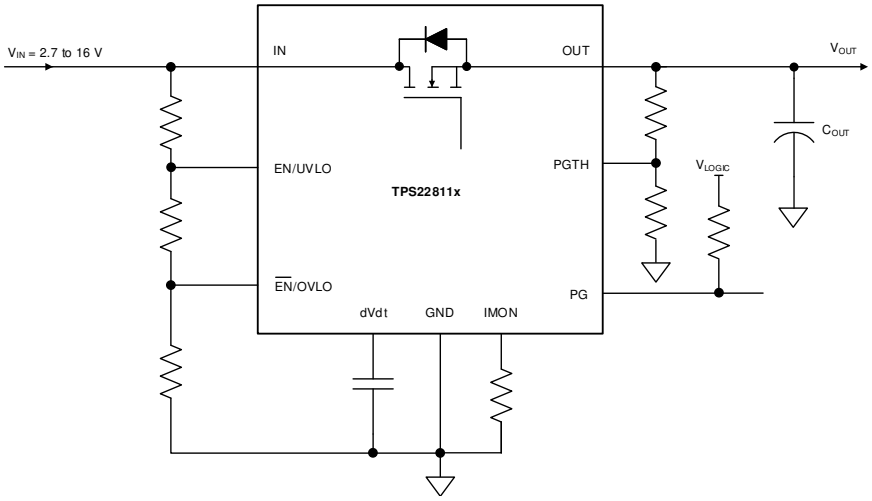


Figure 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

IMON pin can be connected to the MCU ADC input for current monitoring purpose.

8.3 Typical Application

The TPS22811 device can be used in an industrial PC for input power protection of PCIe card. Industrial PCs provide flexible PCIe expansion slots with different combination of PCIe x16, PCIe x4 and PCI. PCIe x16 slot draws maximum current of up to 5.5 A from on board a 12-V rail. Load switch device like TPS22811 can support the power requirements of these PCIe expansion slots and can be used for switching 12-V supply to PCIe card. During plugging or unplugging PCIe card power pin of PCIe slot can short to ground that can cause the 12-V rail to droop or even damage the power tree due to very high current draw. The TPS22811 device can quickly respond to fault events like short-circuit and isolate supply from load side thus preventing supply from drooping. The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop.

The TPS22811 device can also be used for switching the 12-V bulk power rail of DDR5 DIMM. PG pin of TPS22811 device can be used to enable downstream DC-DC converters after the 12-V rail is fully up.

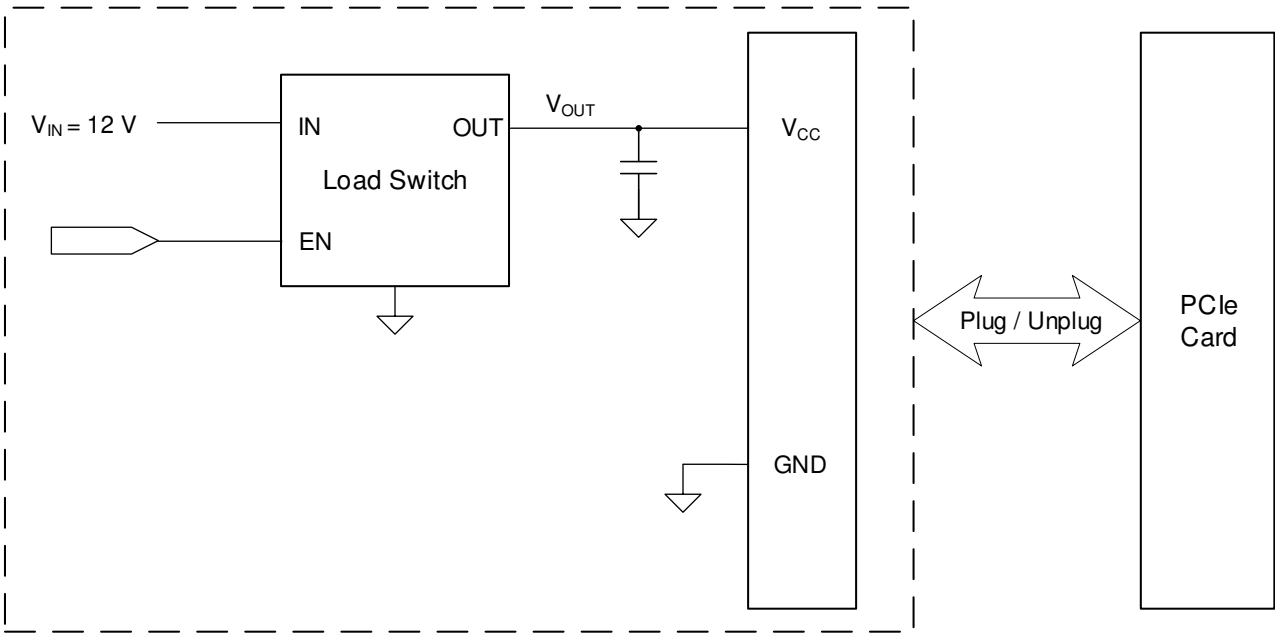
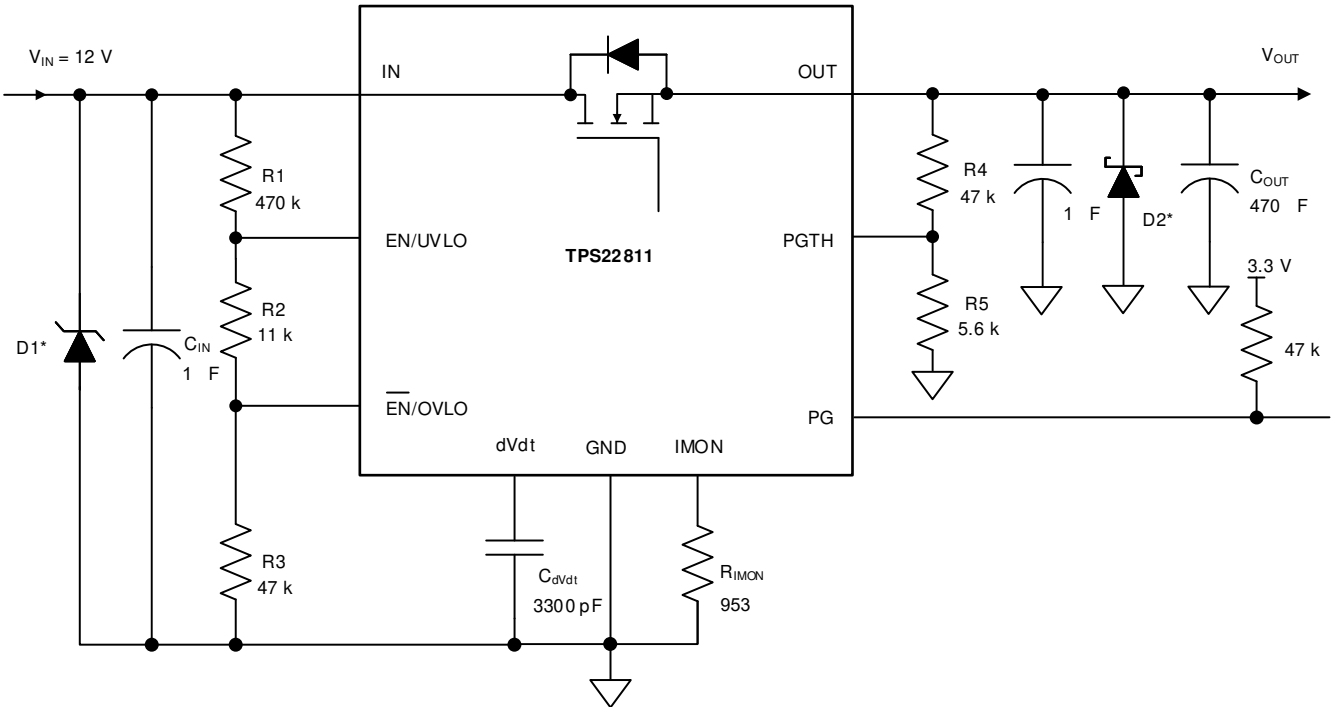


Figure 8-2. Power path protection block diagram of a typical PCIe slot



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

Figure 8-3. PCIe expansion slot protection

ADVANCE INFORMATION

8.3.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	12 V
Undervoltage threshold ($V_{IN(UV)}$)	10.8 V
Overvoltage threshold ($V_{IN(OV)}$)	13.2 V
Output power good threshold (V_{PG})	11.4 V
Maximum continuous current	5.5 A
Analog load current monitor voltage range ($V_{IMONmax}$)	0.5 V
Output capacitance (C_{OUT})	470 µF
Output rise time (t_R)	12 ms

8.3.2 Detailed Design Procedure

8.3.2.1 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2 and R3 whose values can be calculated using Equation 7 and Equation 8:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \times \left(R_1 + R_2 + R_3\right)}{R_2 + R_3} \quad (7)$$

$$V_{IN(OV)} = \frac{V_{OV(R)} \times \left(R_1 + R_2 + R_3\right)}{R_3} \quad (8)$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold and $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 and R3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 and R3 from the power supply is IR123 = V_{IN} / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins.

From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (maximum), $V_{OV(R)}$ = 1.2 V and $V_{UVLO(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 13.2 V and $V_{IN(UV)}$ = 10.8 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 10.7 kΩ and R3 = 48 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 11 kΩ, and R3 = 47 kΩ.

8.3.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\left(\frac{V}{ms}\right) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{12\,V}{12\,ms} = 1\,\frac{V}{ms} \quad (9)$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} = \frac{3300}{1\,\frac{V}{ms}} = 3300\,pF \quad (10)$$

Choose the nearest standard capacitor value as 3300 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = C_{OUT}\,(\mu F) \times SR\left(\frac{V}{ms}\right) = 470\,\mu F \times 1\,\frac{V}{ms} = 470\,mA \quad (11)$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH} = 0.5 \times V_{IN}\,(V) \times I_{INRUSH}\,(mA) = 0.5 \times 12\,V \times 470\,mA = 2.82\,W \quad (12)$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. Figure 8-4 shows the thermal shutdown limit, for 2.82 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 12 ms. Therefore, it is safe to use 12 ms as the start-up time for this application.

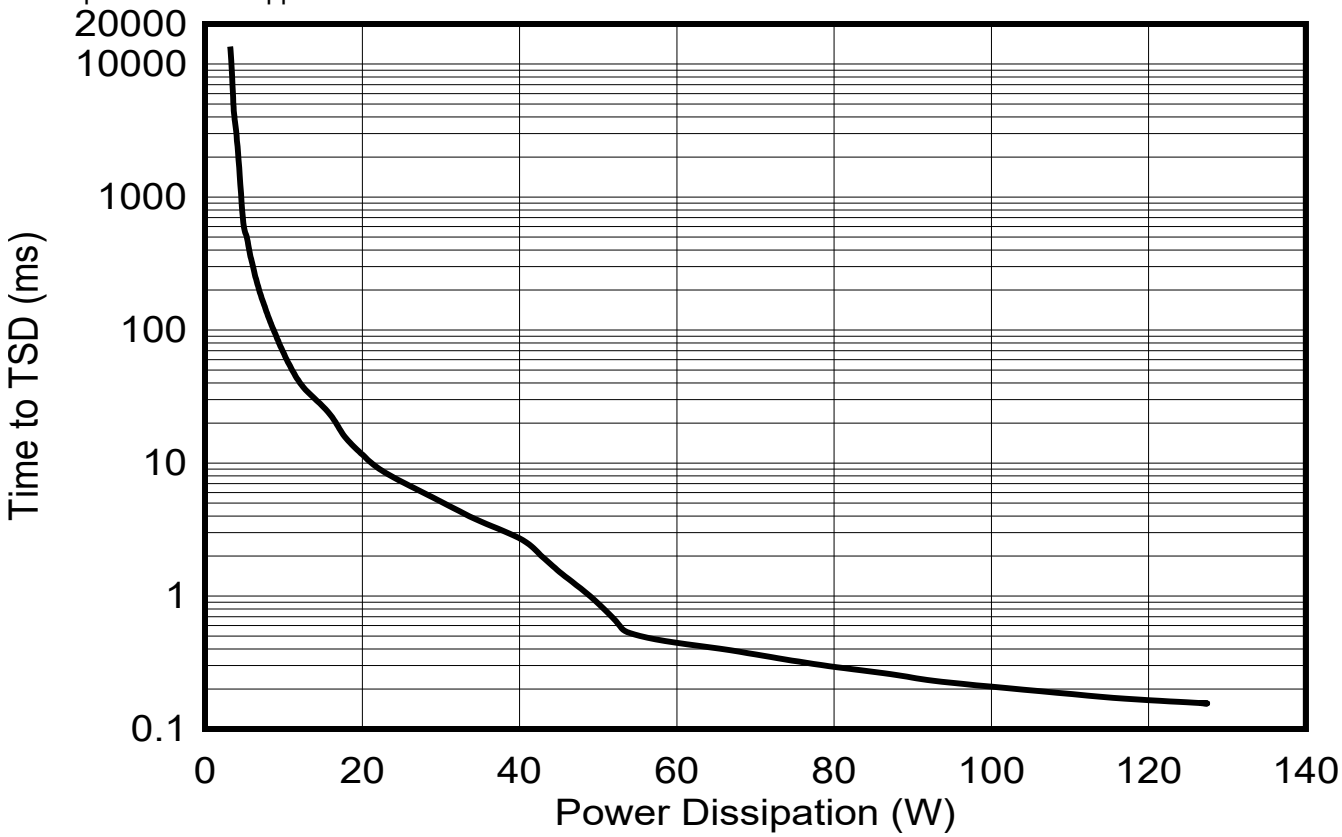


Figure 8-4. Thermal Shut-Down Plot During Inrush

8.3.2.3 Setting Power Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R4 & R5 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \times \left(R_4 + R_5\right)}{R_5} \quad (13)$$

Because R4 and R5 leak the current from the output rail VOUT, these resistors must be selected to minimize the leakage current. The current drawn by R4 and R5 from the power supply is IR45 = VOUT / (R4 + R5). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the PGTH leakage current expected. From the device electrical specifications, PGTH leakage current is 1 µA (max), $VPGTH_{(R)}$ = 1.2 V and from design requirements, VPG = 11.4 V. To solve the equation, first choose the value of R4 = 47 kΩ and calculate R5 = 5.52 kΩ. Choose nearest 1% standard resistor value as R5 = 5.6 kΩ.

8.3.2.4 Setting Analog Current Monitor Voltage (IMON) Range

The analog current monitor voltage range can be set using the RIMON resistor whose value can be calculated as:

$$R_{IMON}\,(\Omega) = \frac{V_{IMON}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times I_{OUTmax}\,(A)} = \frac{0.5 \times 10^6}{95 \times 5.5} = 957\ \Omega \quad (14)$$

Choose nearest 1% standard resistor value as 953 Ω.

8.3.3 Application Curves

Figure 8-5. Power Up

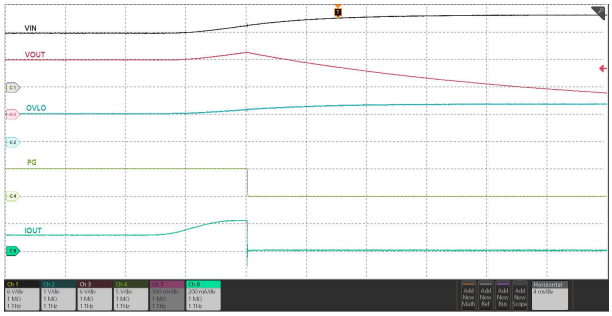


Figure 8-6. Overvoltage response

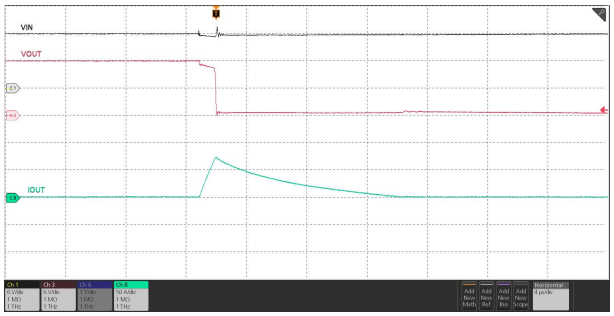


Figure 8-7. Output Short-Circuit During Steady State

8.4 Parallel Operation

Applications which need higher steady current can use two TPS22811x devices connected in parallel as shown in Figure 8-8 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the PG signal of the first device. After the inrush sequence is complete, the first device asserts its PG pin high and turns on the second device. The second device asserts its PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

After in steady state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

ADVANCE INFORMATION

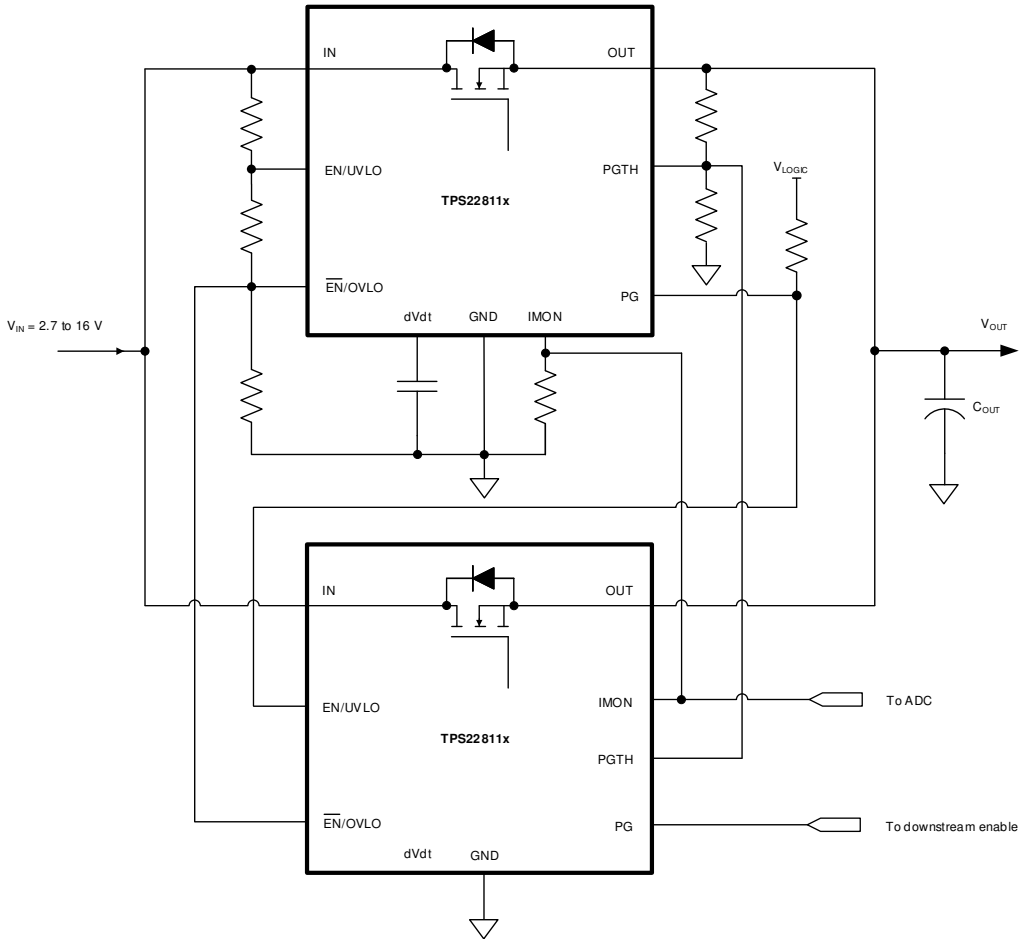


Figure 8-8. Two Devices Connected in Parallel for Higher Steady State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady state.

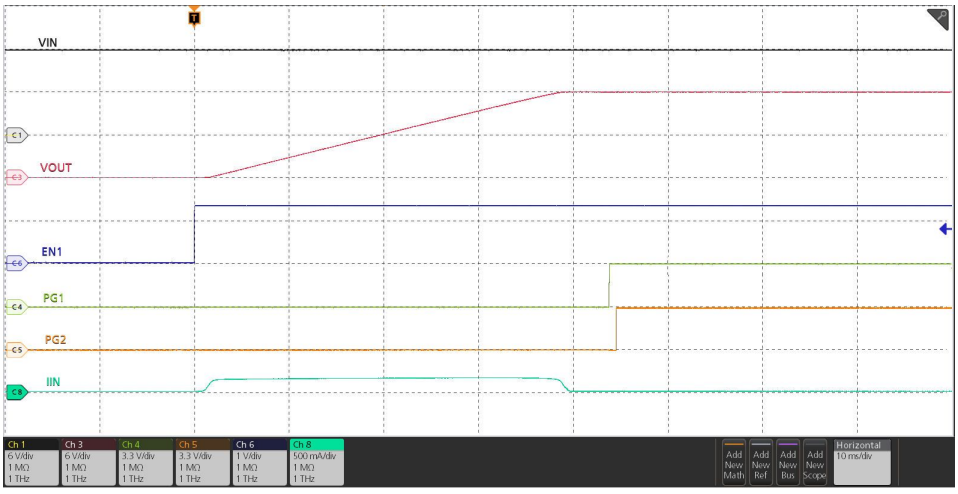


Figure 8-9. Parallel Devices Sequencing During Start-Up

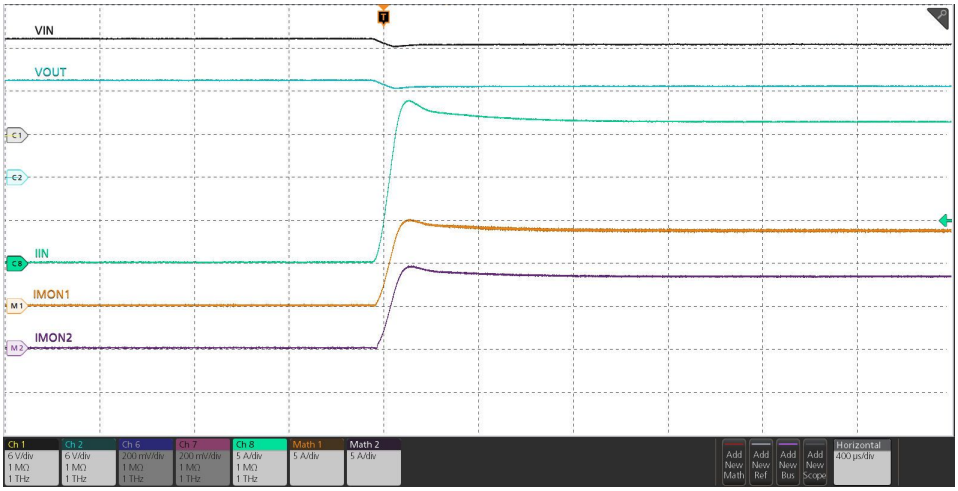


Figure 8-10. Parallel Devices Load Current During Steady State

ADVANCE INFORMATION

9 Power Supply Recommendations

The TPS22811x devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 16 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

9.1 Transient Protection

In the case of a short-circuit or device turn off during steady state when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  The approximate value of input capacitance can be estimated with Equation 15:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

  where

  – V_{IN} is the nominal supply voltage.
  – I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 9-1.

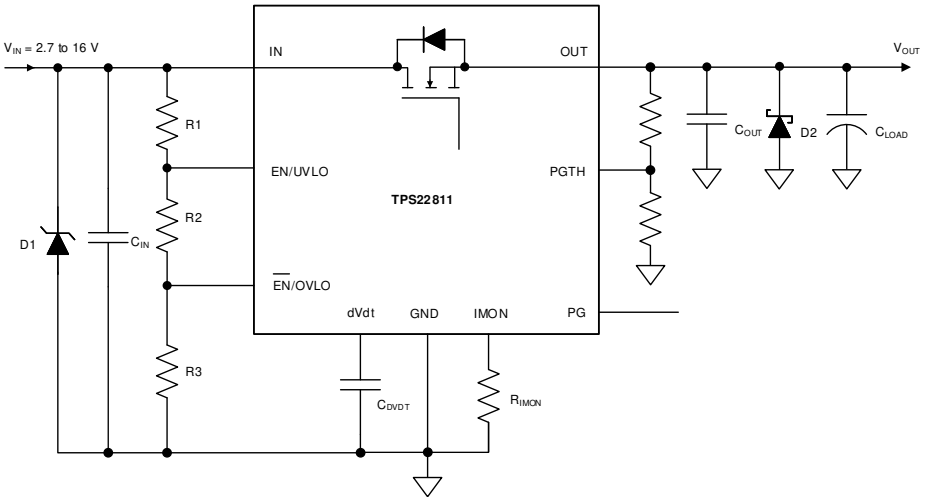


Figure 9-1. Circuit Implementation with Optional Protection Components

9.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

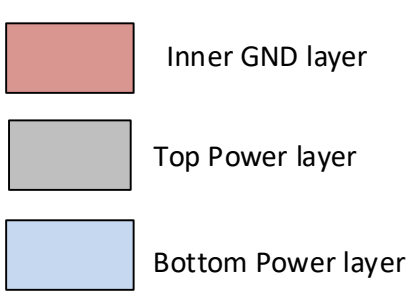
ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{IMON}
  - C_{dVdT}
  - Resistors for the EN/UVLO, $\overline{EN}$/OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{IMON} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current monitor and soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

10.2 Layout Example



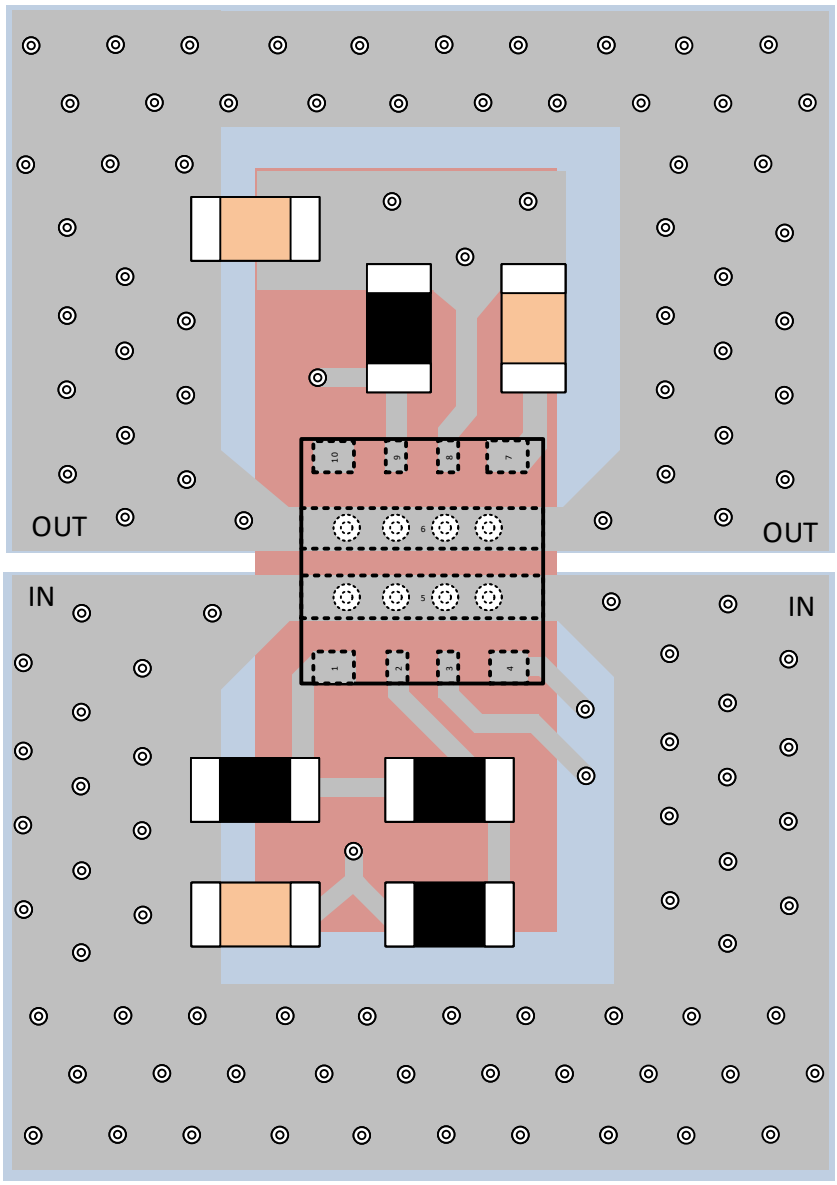


Figure 10-1. Layout Example

ADVANCE INFORMATION

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS22811EVM eFuse Evaluation Board*
- Texas Instruments, *TPS22811x Design Calculator*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

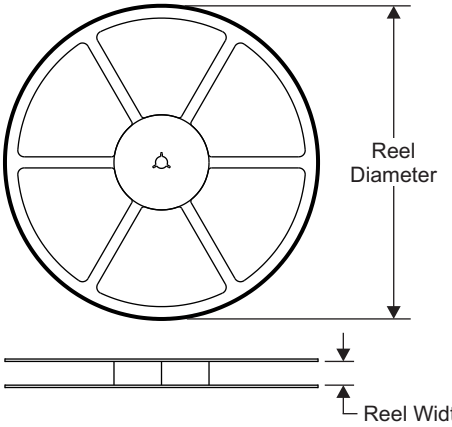
ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

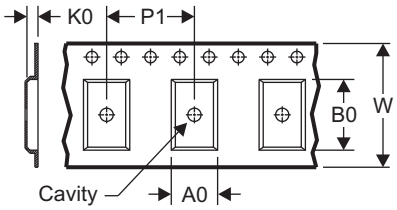
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

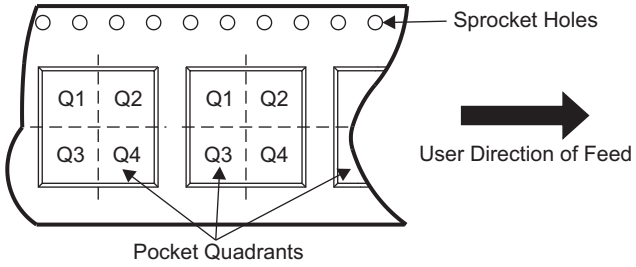


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

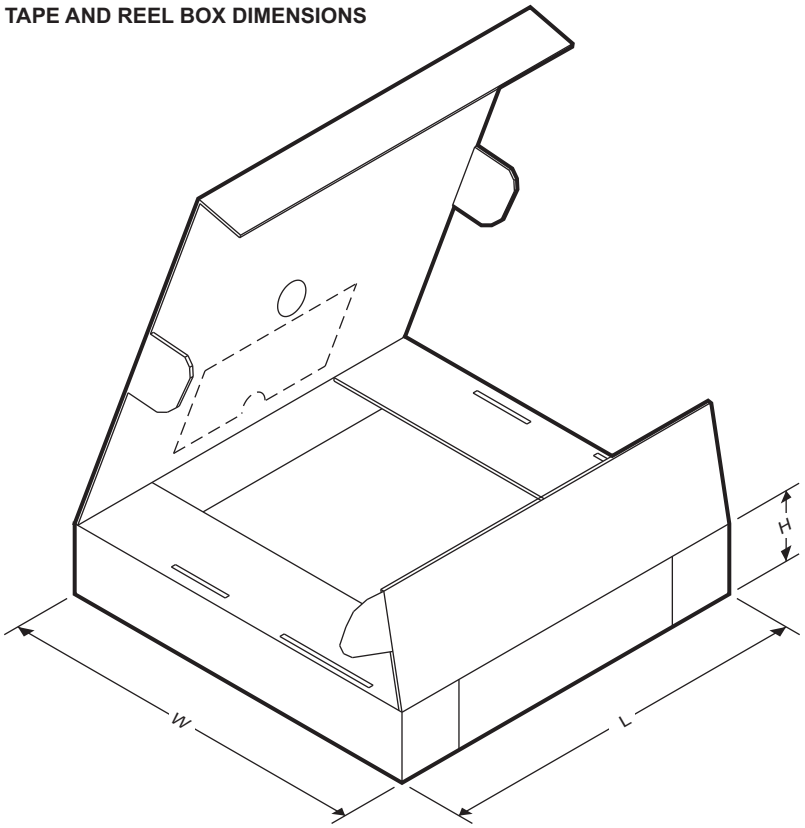


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS228114ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
PTPS22811LARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS228114ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS228114LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



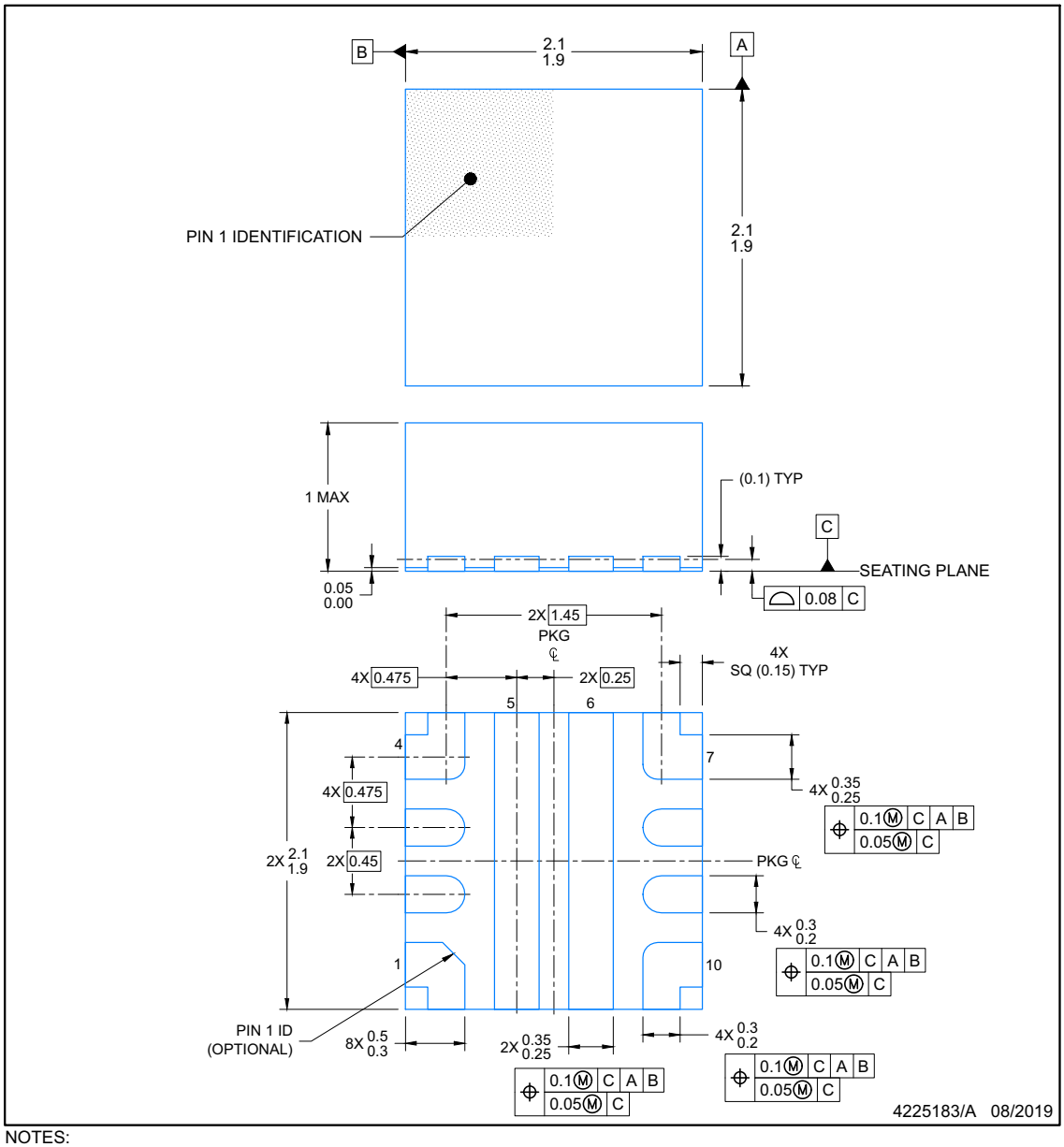
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS228114ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
PTPS228114LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS228114ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS228114LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

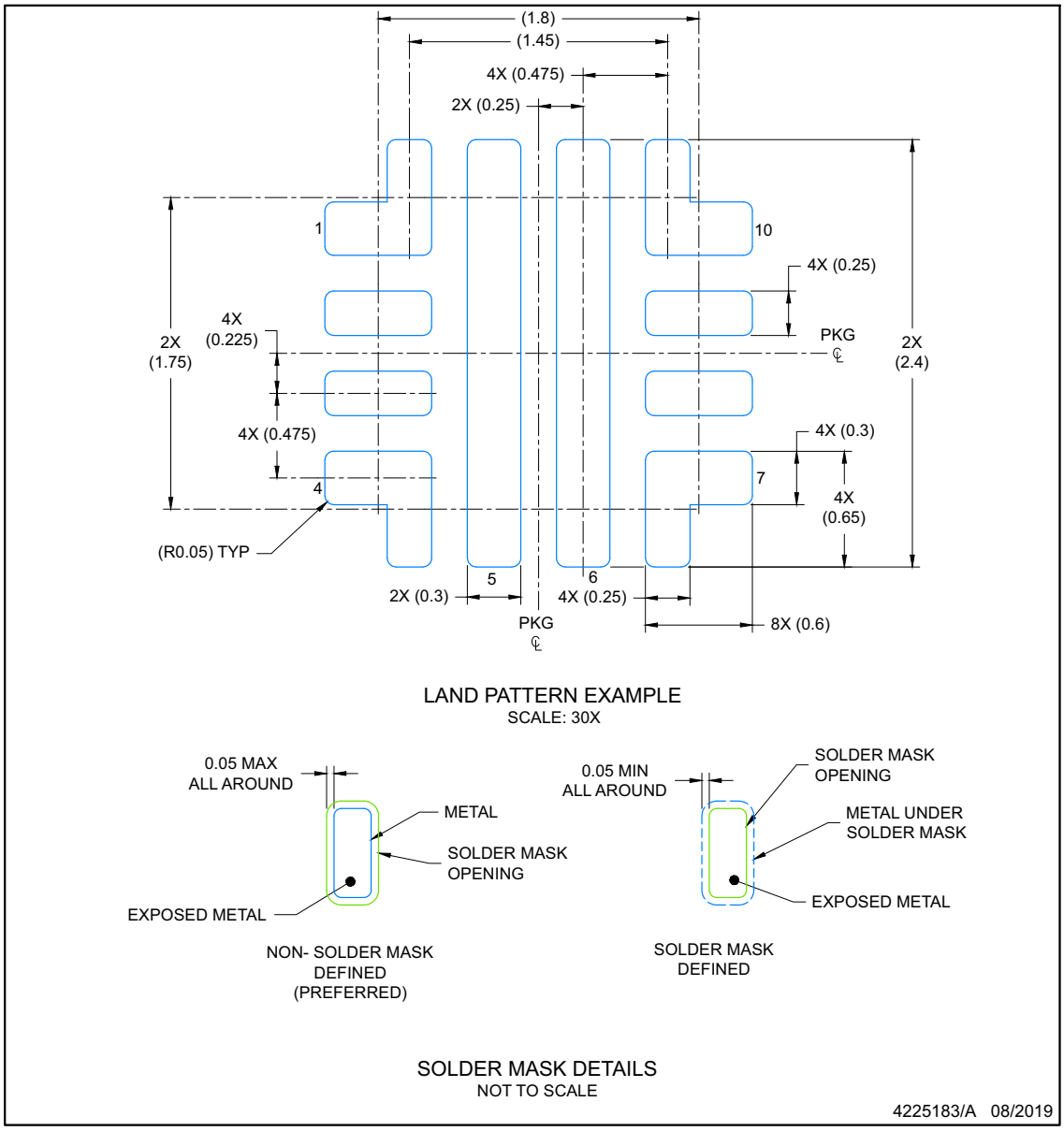
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RPW0010A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

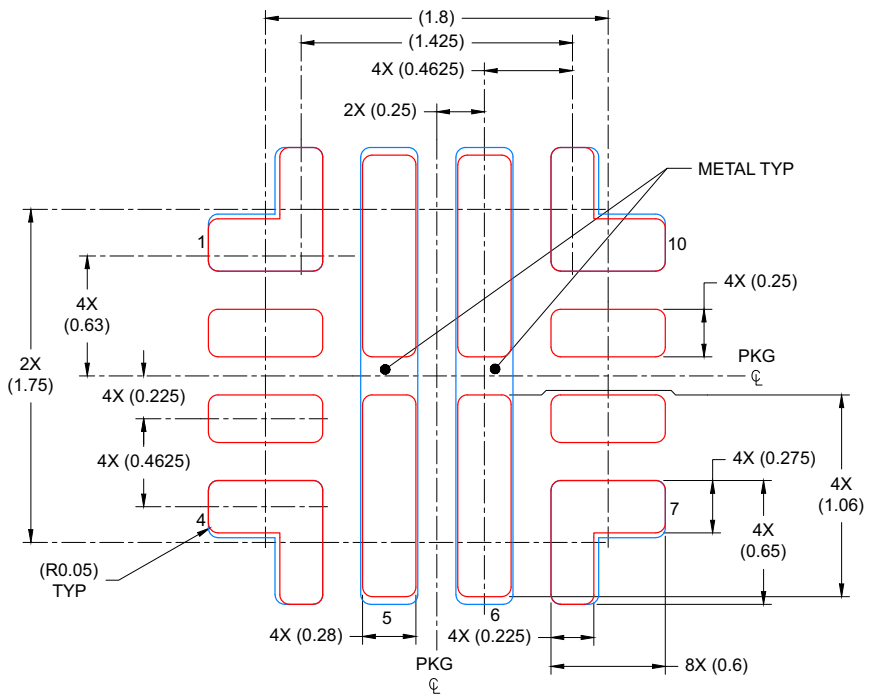
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RPW0010A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22811LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

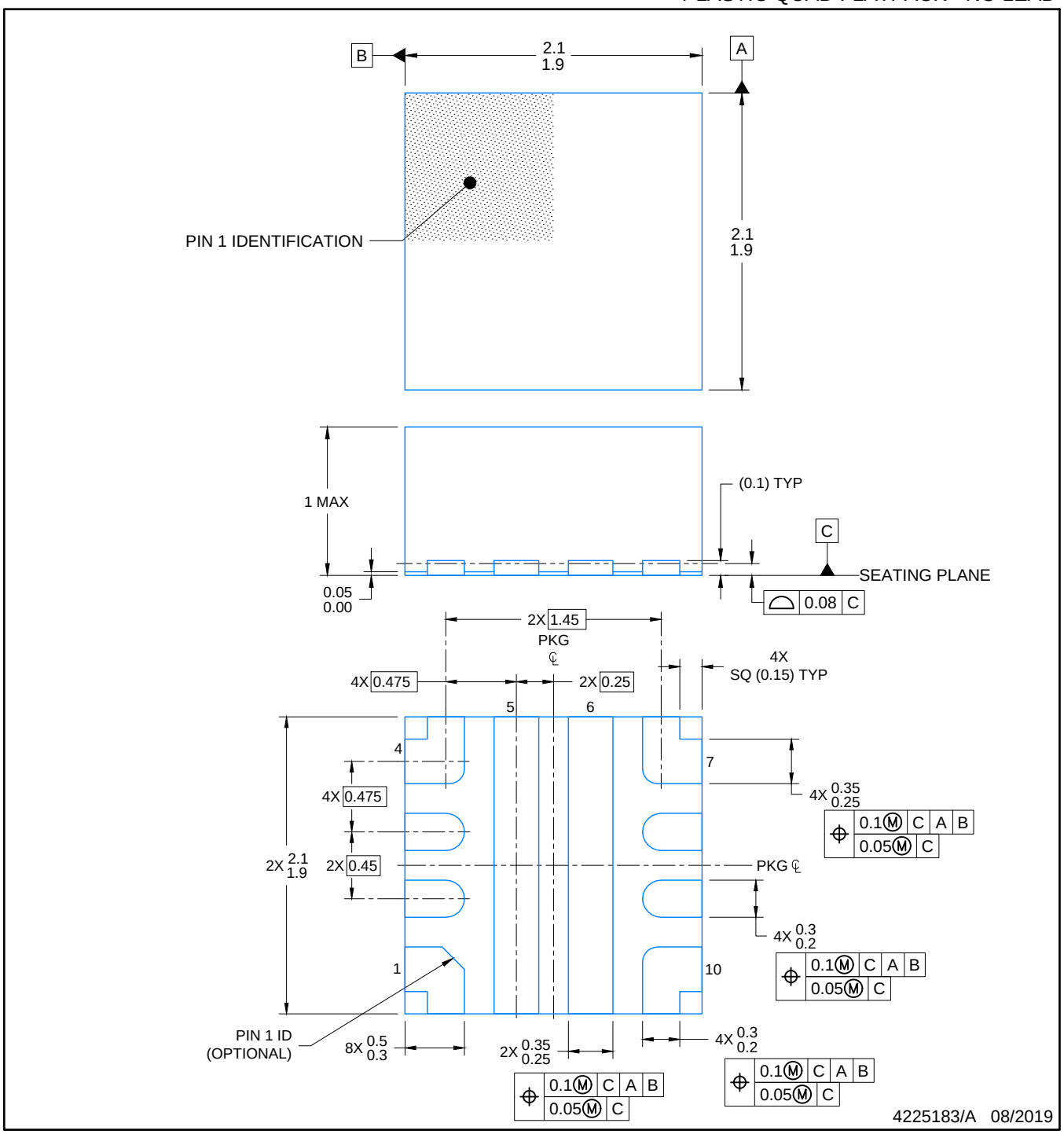
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RPW0010A

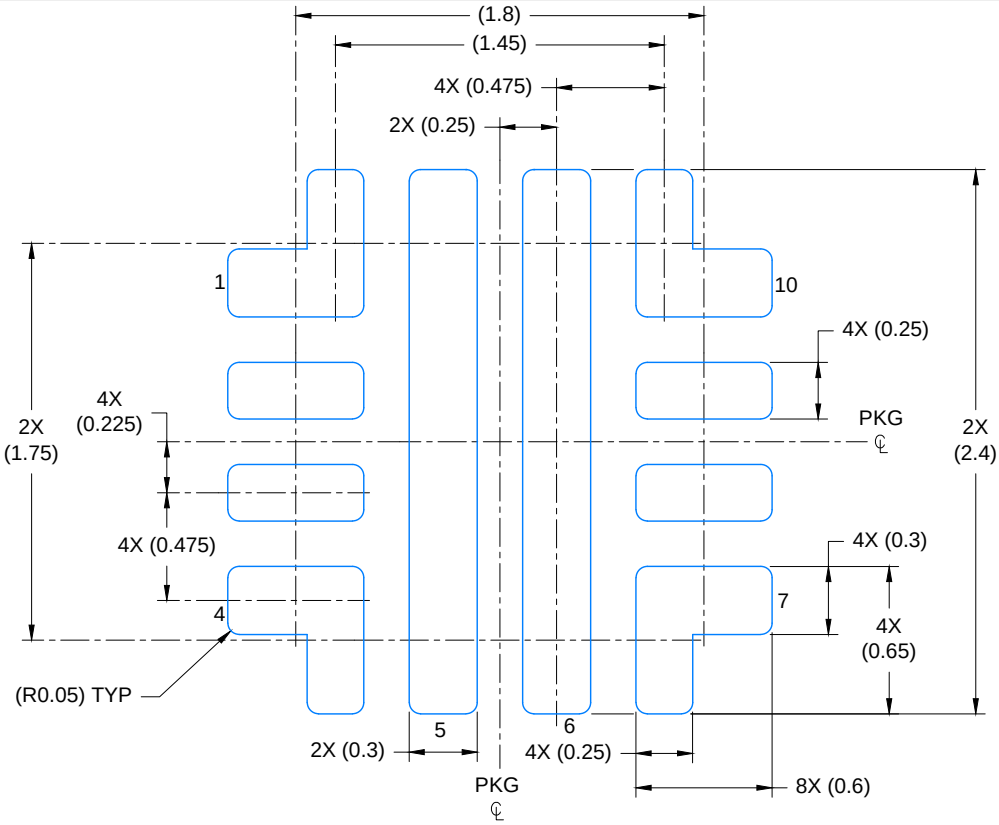
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



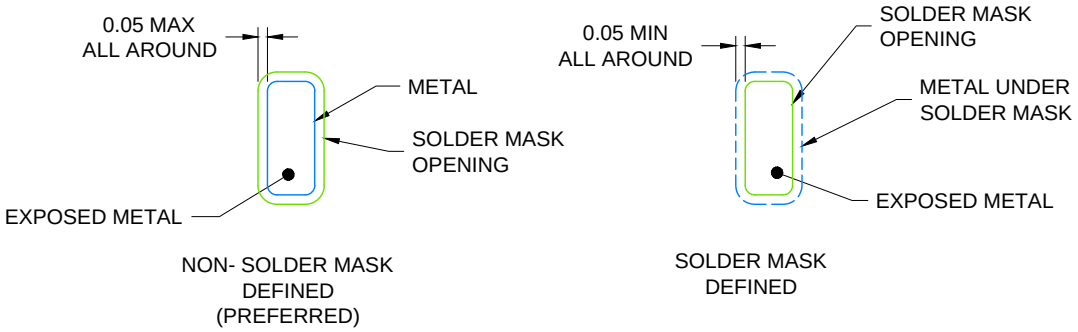
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



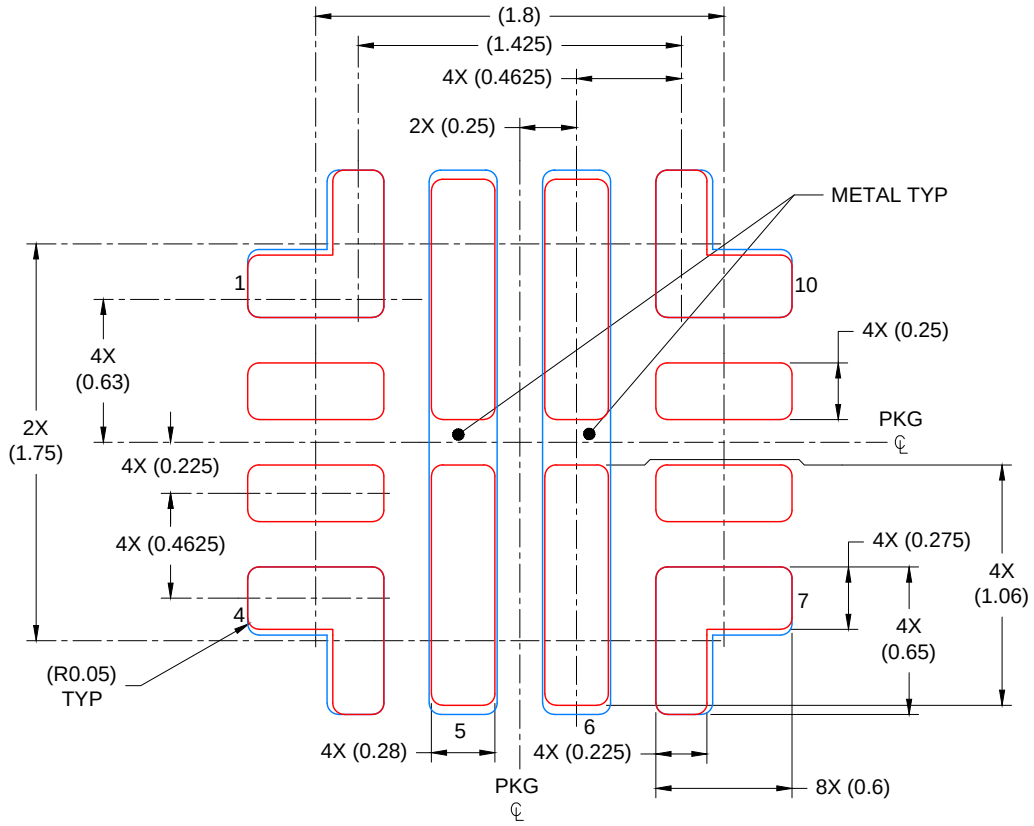
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS22953-Q1, TPS22954-Q1
SLVSGK4A – NOVEMBER 2021 – REVISED JUNE 2022

TPS2295x-Q1 5.7-V, 5-A, 14-mΩ On-Resistance, Automotive Load Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Integrated single channel load switch
- Input voltage range: 0.7 V to 5.7 V
- R_{ON} resistance
  - R_{ON} = 14 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
- 5-A maximum continuous switch current
- Adjustable Undervoltage Lockout Threshold (UVLO)
- Adjustable voltage supervisor with Power Good (PG) indicator
- Adjustable output slew rate control
- Enhanced quick output discharge remains active after power is removed (TPS22954-Q1 only)
  - 15 Ω (typ.) discharges 100 µF within 10 ms
- Reverse current blocking when disabled (TPS22953-Q1 only)
- Automatic restart after supervisor fault detection when enabled
- Thermal shutdown
- Low quiescent current ≤ 50 µA
- SON 10-pin package with thermal pad
- ESD performance tested per JESD 22
  - 2-kV HBM and 750-V CDM

2 Applications

- Infotainment and cluster head unit
- Automotive cluster display
- ADAS surround view system ECU
- Body control module and gateway

3 Description

The TPS2295x-Q1 are small, single channel load switches with controlled turn-on. The devices contain an N-channel MOSFET that can operate over an input voltage range of 0.7 V to 5.7 V and can support a maximum continuous current of 5 A.

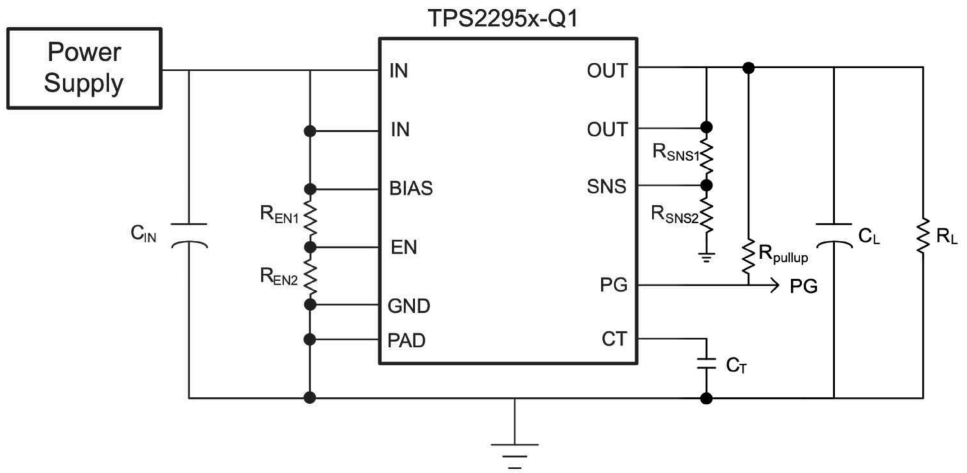
The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing. The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω on-chip load is integrated into the device for a quick discharge of the output when the switch is disabled. The enhanced Quick Output Discharge (QOD) remains active for a short time after power is removed from the device to finish discharging the output.

The TPS2295x-Q1 are available in small, space-saving 10-SON packages with integrated thermal pad, allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TPS2295x-Q1	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (June 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

Device	Quick Output Discharge	Reverse Current Blocking	Package (Pin)	Body Size	Pin Pitch
TPS22954-Q1	Yes	No	DQC (10)	2.00 mm × 3.00 mm	0.5 mm
TPS22953-Q1	No	Yes	DQC (10)	2.00 mm × 3.00 mm	0.5 mm

6 Pin Configuration and Functions

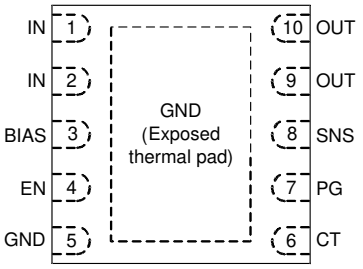


Figure 6-1. DQC/DSQ Package 10-Pin WSON Top View

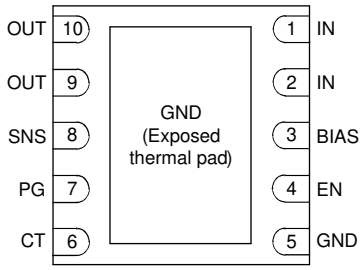


Figure 6-2. DQC/DSQ Package 10-Pin WSON Bottom View

Table 6-1. Pin Functions

PIN[1]		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input. Bypass this input with a ceramic capacitor to GND.
2			
3	BIAS	I	Bias pin and power supply to the device
4	EN	I	Active high switch to enable and disable the output. Also acts as the input UVLO pin. Use external resistor divider to adjust the UVLO level. Do not leave floating.
5	GND	—	Device ground
6	CT	O	V_{OUT} slew rate control. Place ceramic cap from CT to GND to change the V_{OUT} slew rate of the device and limit the inrush current. Rate the CT Capacitor to 25 V or higher.
7	PG	O	Power Good. This pin is open drain which pulls low when the voltage on EN or SNS is below their respective VIL levels.
8	SNS	I	Sense pin. Use external resistor divider to adjust the power good level. Do not leave floating.
9	OUT	O	Switch output
10			
—	Thermal Pad	—	Exposed thermal pad. Tie to GND.

(1) Pinout applies to all package versions.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current, T_A = 70°C		5	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		7	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100- 002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100- 011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.7	V_{BIAS}	V
V_{BIAS}	Bias voltage	2.5	5.7	V
V_{OUT}	Output voltage	0.9	5.7	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	0	5.7	V
TA	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

7.3 Thermal Information

THERMAL METRIC (1)		TPS2295x-Q1 DQC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and the recommended VBIAS voltage range of 2.5 V to 5.7 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{EN}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	650	700	750	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	560	600	640	mV
V_{SNS}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	465	515	565	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	410	455	500	mV
t_{BLANK}	Blanking time for EN and SNS	EN or SNS rising	–40°C to +125°C		100		µs
$t_{DEGLITCH}$	Deglitch time for EN and SNS	EN or SNS falling	–40°C to +125°C		5		µs
t_{DIS}	Output discharge time (TPS22954 only)	C_L = 100µF	–40°C to +125°C			10	ms
$t_{RESTART}$	Output restart time	SNS falling	–40°C to +125°C		2		ms
t_{RCB}	Response time for reverse current blocking (TPS22953 only)	V_{OUT} = V_{BIAS} EN falling	–40°C to +125°C		10		µs
T_{SD}	Thermal shutdown	Junction temperature rising	-	130	150	170	°C
TSD_{HYS}	Thermal shutdown hysteresis	Junction temperature falling	-		20		°C
$I_{RCB,IN}$	Input reverse blocking current (TPS22953 only)	V_{OUT} = 5V, V_{IN} = V_{EN} = 0V, V_{BIAS} = 0V to 5.7V	25°C		0.01	2	mΩ
			–40°C to +85°C			5	mΩ
			–40°C to +125°C			11	mΩ

7.5 Electrical Characteristics – VBIAS = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 5 V		–40°C to +85°C		34	45	µA
				–40°C to +125°C			50	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		5	7	µA
				–40°C to +125°C			8	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.02	4	µA
				–40°C to +125°C			13	
			V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.5 Electrical Characteristics – VBIAS = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		14	20	mΩ
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 3.3 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		15	28	Ω
				–40°C to +125°C			30	Ω

7.6 Electrical Characteristics – VBIAS = 3.3 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 3.3 V		–40°C to +85°C		19	35	µA
				–40°C to +125°C			37	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	6	µA
				–40°C to +125°C			7	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.6 Electrical Characteristics – VBIAS = 3.3 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 3.3 V	25°C		15	21	mΩ
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		13	28	Ω
				–40°C to +125°C			30	Ω

7.7 Electrical Characteristics – VBIAS = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 2.5 V		–40°C to +85°C		16	25	µA
				–40°C to +125°C			27	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	5	µA
				–40°C to +125°C			6	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.7 Electrical Characteristics – VBIAS = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		16	23	mΩ
				–40°C to +85°C			26	
				–40°C to +125°C			27	
			V_{IN} = 1.8 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.5 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.2 V	25°C		15	22	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 0.7 V	25°C		14	21	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		12	28	Ω
				–40°C to +125°C			30	Ω

7.8 Switching Characteristics – CT = 1000 pF

All typical values are at 25°C unless otherwise noted

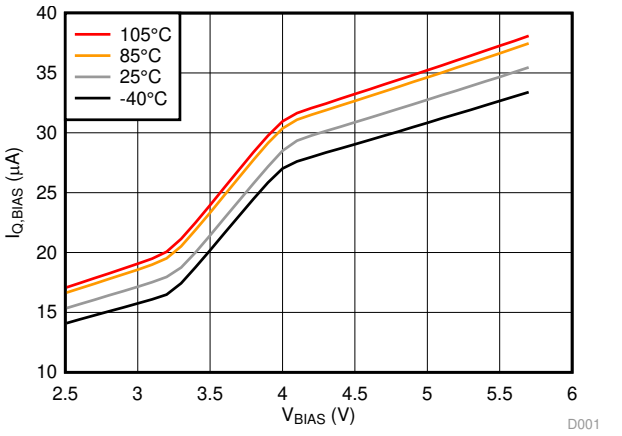
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1265		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1492		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		519		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.2		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		4.9		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs

7.9 Switching Characteristics – CT = 0 pF

All typical values are at 25°C unless otherwise noted

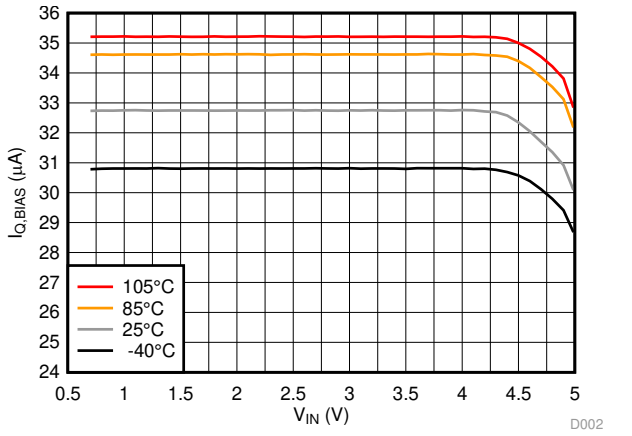
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		235		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		140		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		165		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs

7.10 Typical DC Characteristics



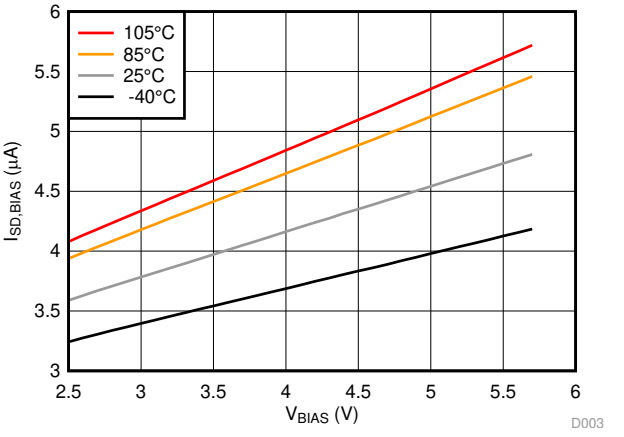
V_{IN} = 1.8 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-1. $I_{Q,BIAS}$ vs V_{BIAS}



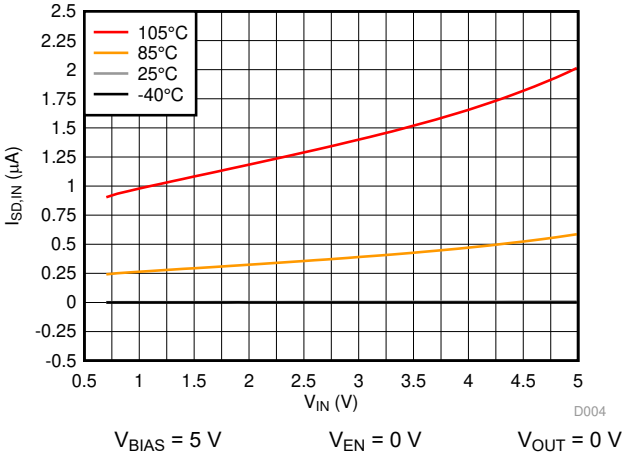
V_{BIAS} = 5 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-2. $I_{Q,BIAS}$ vs V_{IN}



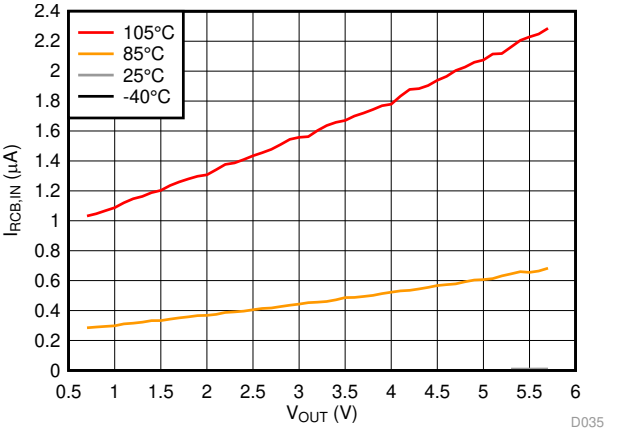
V_{IN} = 1.8 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-3. $I_{SD,BIAS}$ vs V_{BIAS}



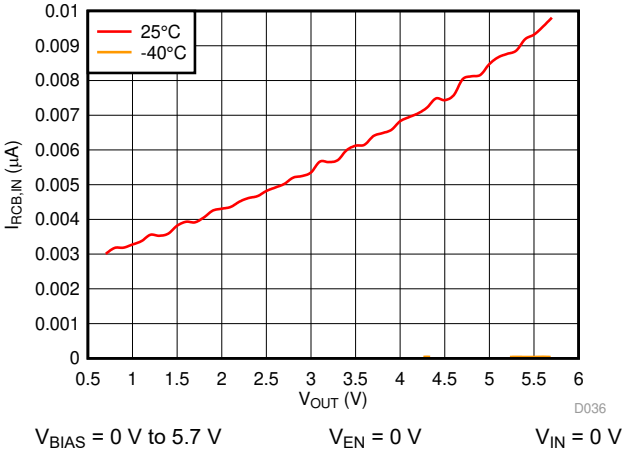
V_{BIAS} = 5 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-4. $I_{SD,IN}$ vs V_{IN}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

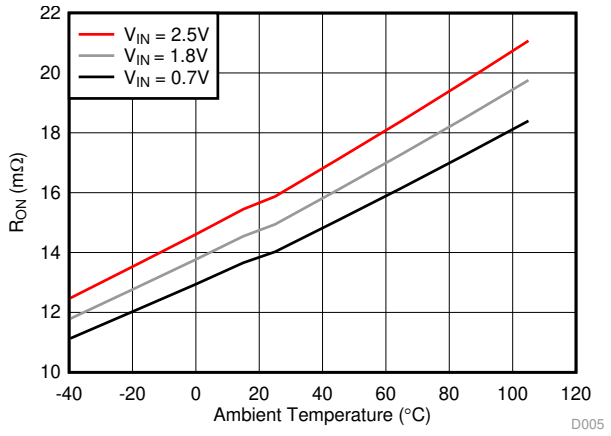
Figure 7-5. $I_{RCB,IN}$ vs V_{OUT}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

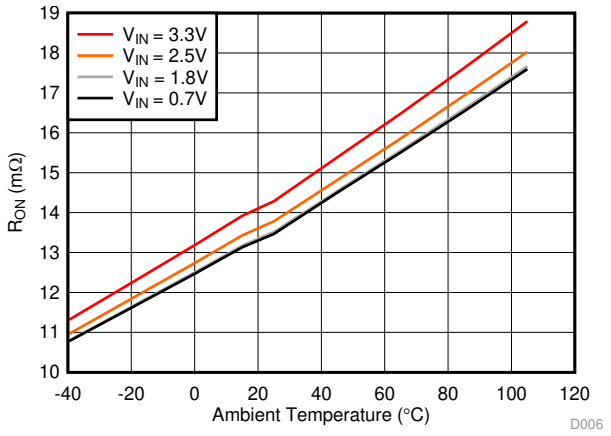
Figure 7-6. $I_{RCB,IN}$ vs V_{OUT}

7.10 Typical DC Characteristics (continued)



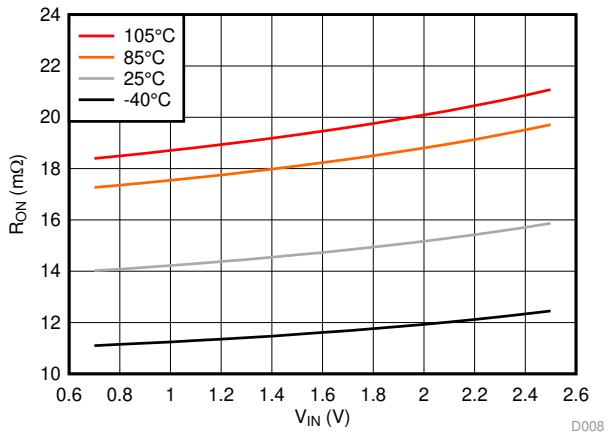
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-7. R_{ON} vs Temperature, V_{BIAS} = 2.5 V



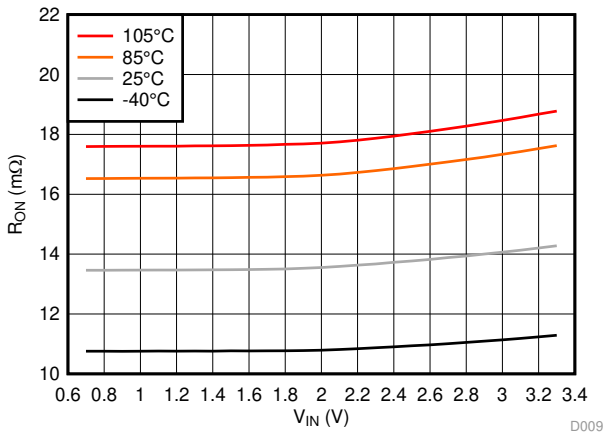
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-8. R_{ON} vs Temperature, V_{BIAS} = 3.3 V



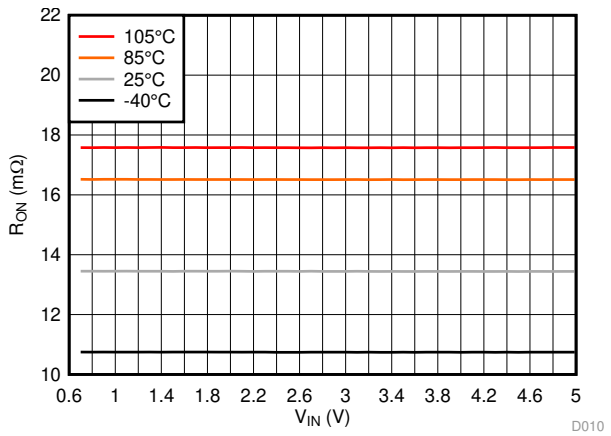
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-9. R_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



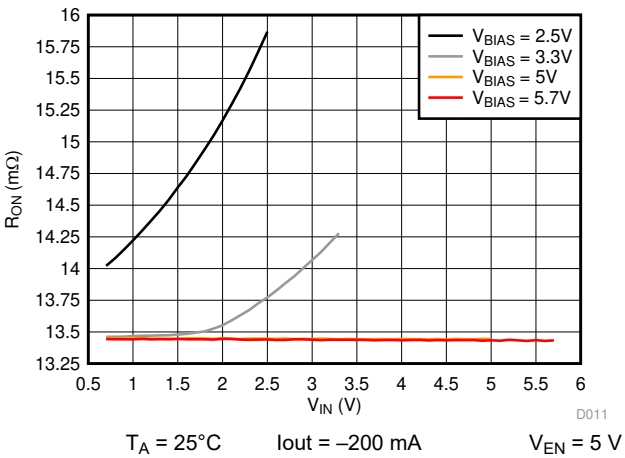
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-10. R_{ON} vs V_{IN}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V Iout = –200 mA V_{EN} = 5 V

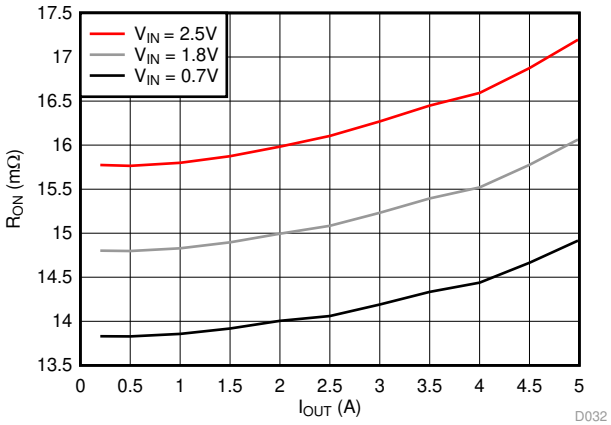
Figure 7-11. R_{ON} vs V_{IN}, V_{BIAS} = 5 V



T_A = 25°C Iout = –200 mA V_{EN} = 5 V

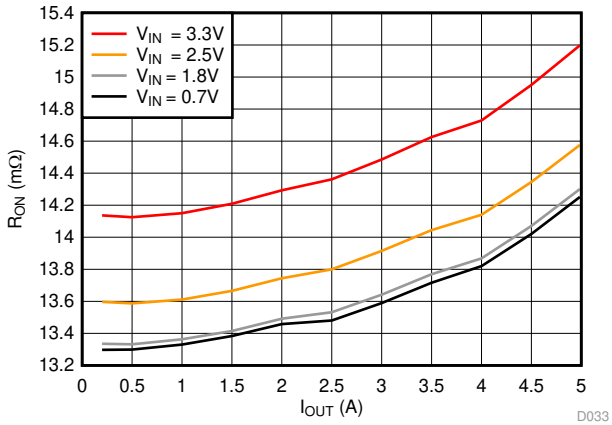
Figure 7-12. R_{ON} vs V_{IN}

7.10 Typical DC Characteristics (continued)



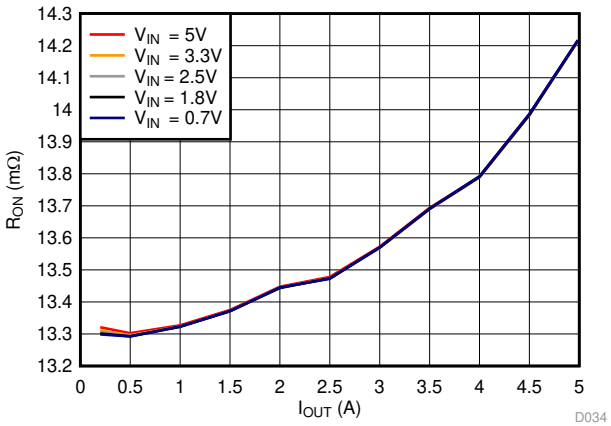
V_{BIAS} = 2.5 V V_{EN} = 5 V

Figure 7-13. R_{ON} vs I_{OUT}, V_{BIAS} = 2.5 V



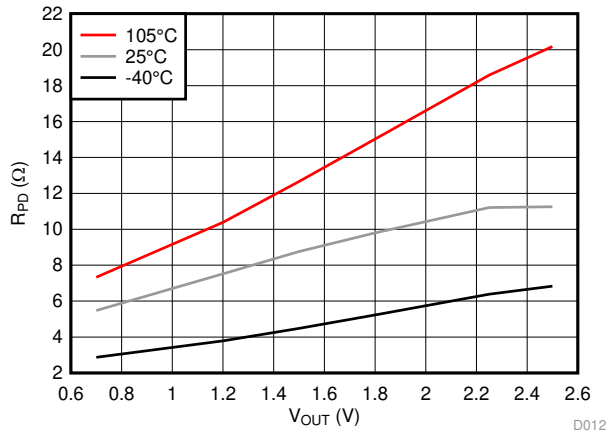
V_{BIAS} = 3.3 V V_{EN} = 5 V

Figure 7-14. R_{ON} vs I_{OUT}, V_{BIAS} = 3.3 V



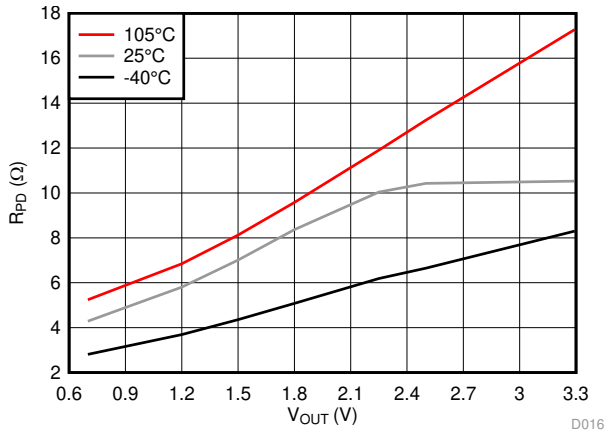
V_{BIAS} = 5 V V_{EN} = 5 V

Figure 7-15. R_{ON} vs I_{OUT}, V_{BIAS} = 5 V



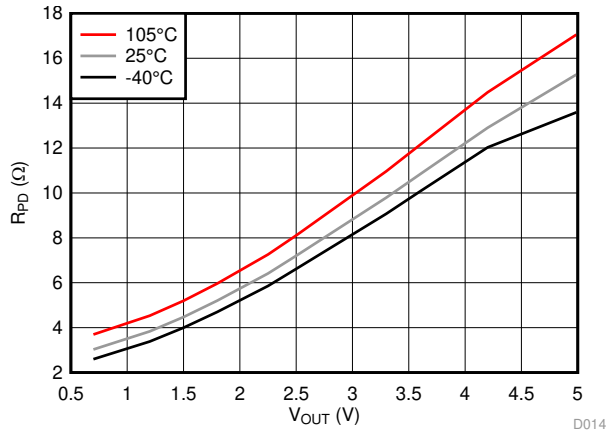
V_{BIAS} = 2.5 V V_{IN} = V_{OUT} V_{EN} = 0 V

Figure 7-16. R_{PD} vs V_{OUT}, V_{BIAS} = 2.5 V



V_{BIAS} = 3.3 V V_{IN} = V_{OUT} V_{EN} = 0 V

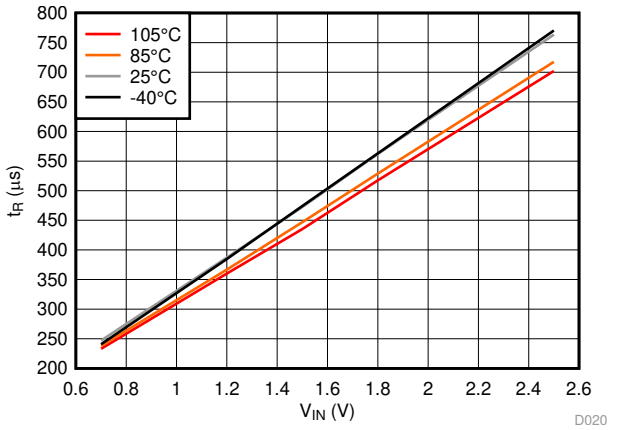
Figure 7-17. R_{PD} vs V_{OUT}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V V_{IN} = V_{OUT} V_{EN} = 0 V

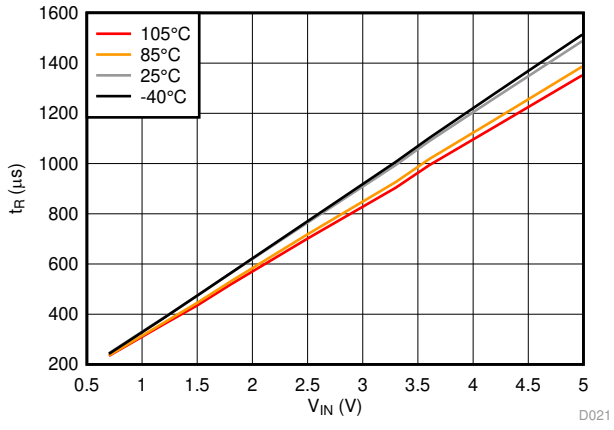
Figure 7-18. R_{PD} vs V_{OUT}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



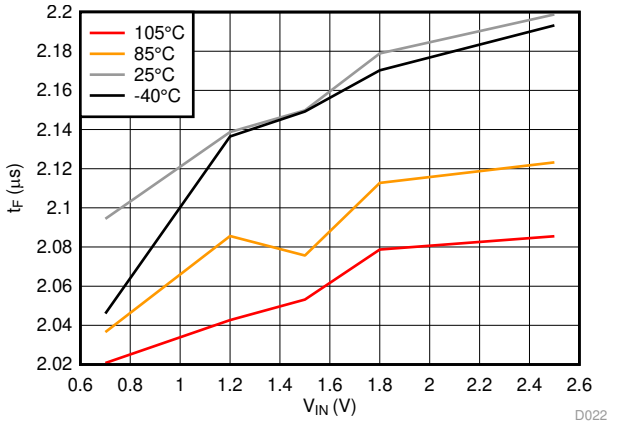
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-19. t_R vs V_{IN}, V_{BIAS} = 2.5 V



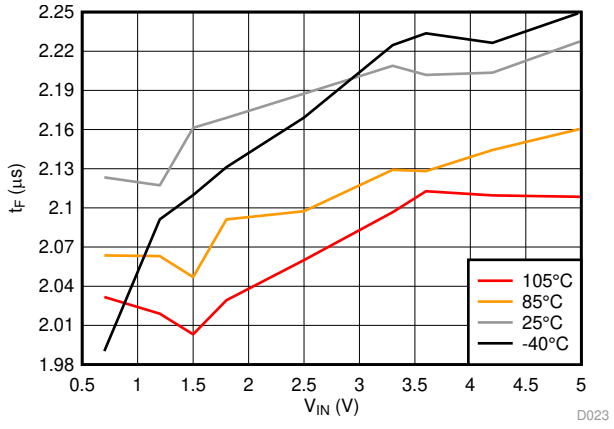
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-20. t_R vs V_{IN}, V_{BIAS} = 5 V



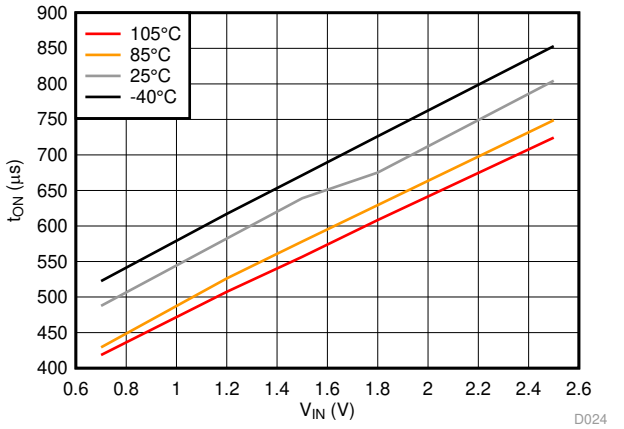
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-21. t_F vs V_{IN}, V_{BIAS} = 2.5 V



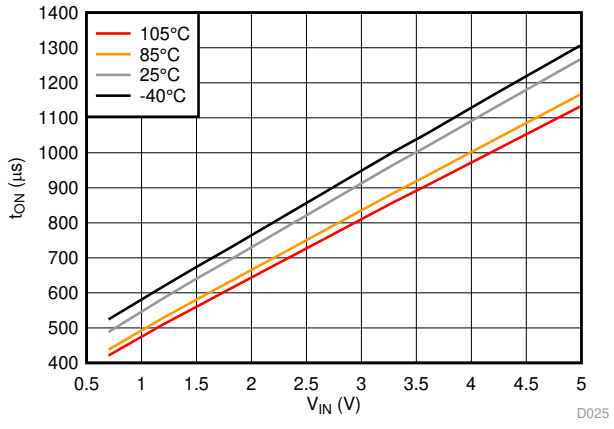
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-22. t_F vs V_{IN}, V_{BIAS} = 5 V



V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

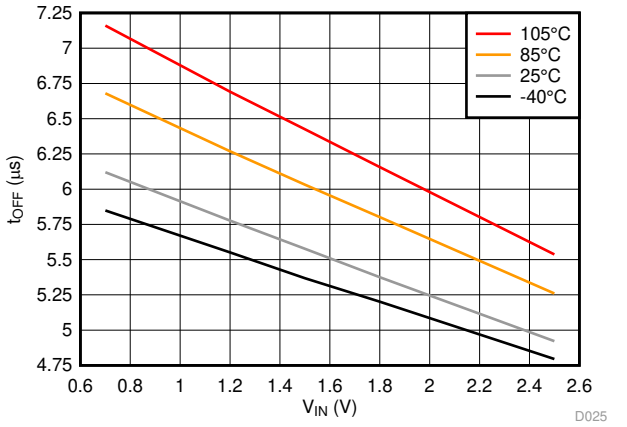
Figure 7-23. t_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

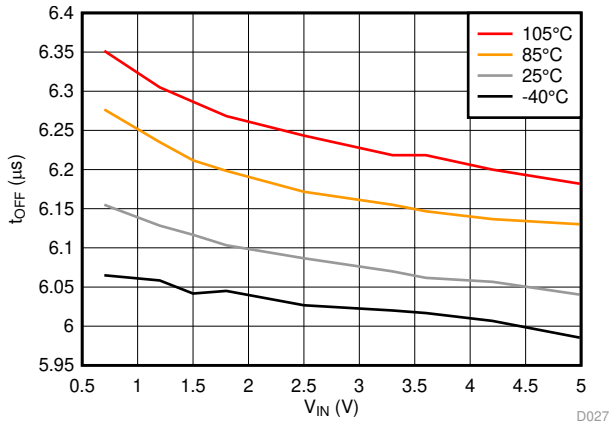
Figure 7-24. t_{ON} vs V_{IN}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



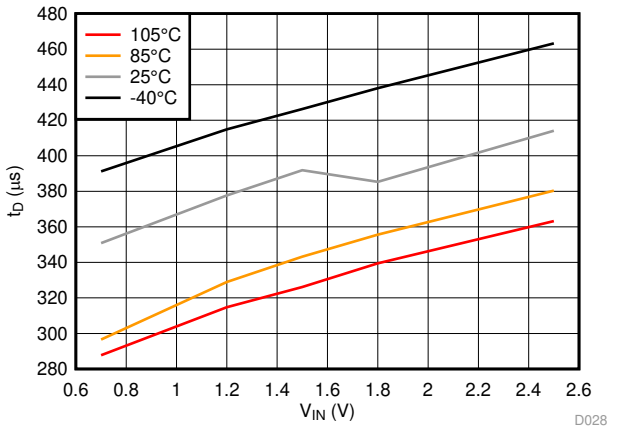
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-25. t_{OFF} vs V_{IN}, V_{BIAS} = 2.5 V



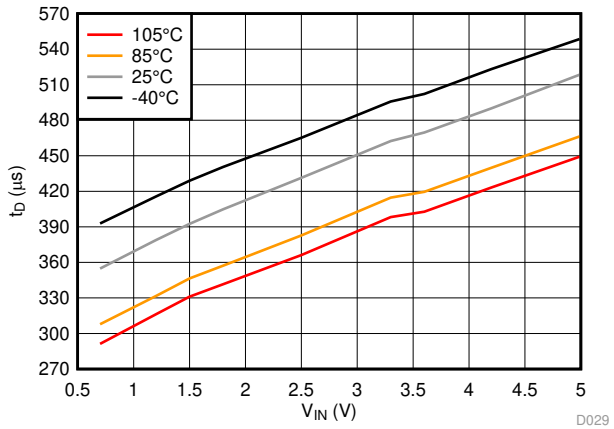
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-26. t_{OFF} vs V_{IN}, V_{BIAS} = 5 V



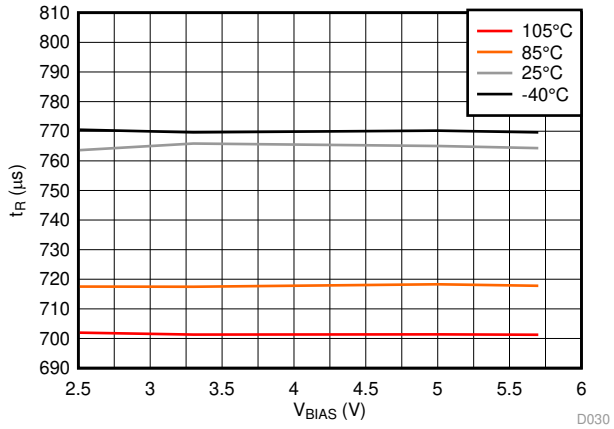
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-27. t_D vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} =Low to High

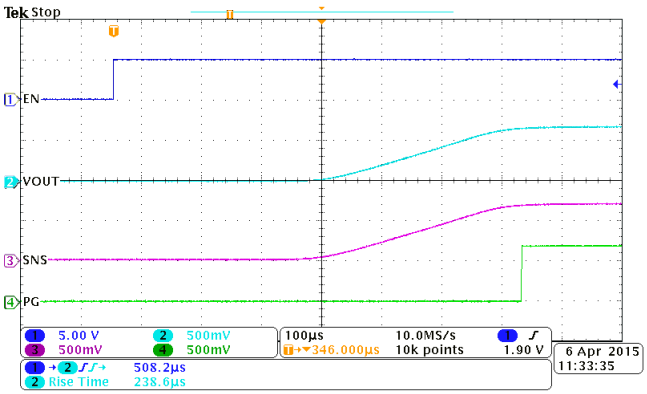
Figure 7-28. t_D vs V_{IN}, V_{BIAS}= 5 V



V_{IN} = 2.5 V CT = 1000 pF V_{EN} = Low to High

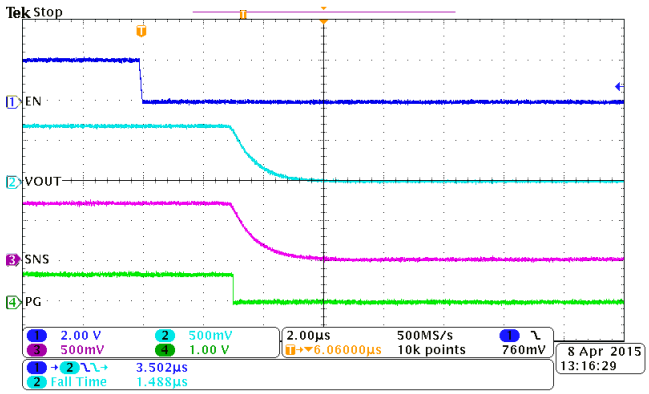
Figure 7-29. t_R vs V_{BIAS}

7.11 Typical Switching Characteristics (continued)



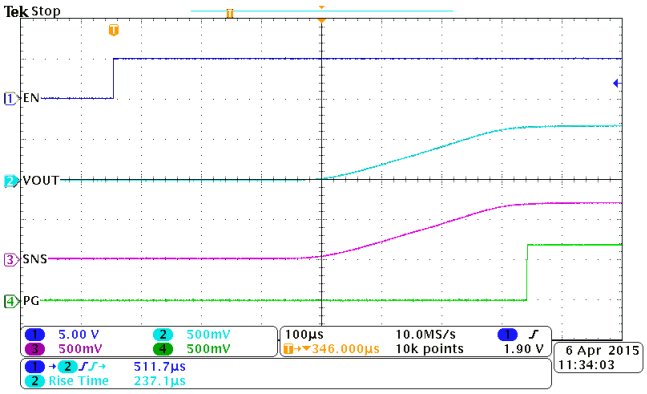
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-30. Turn-on Waveform, V_{BIAS} = 2.5 V



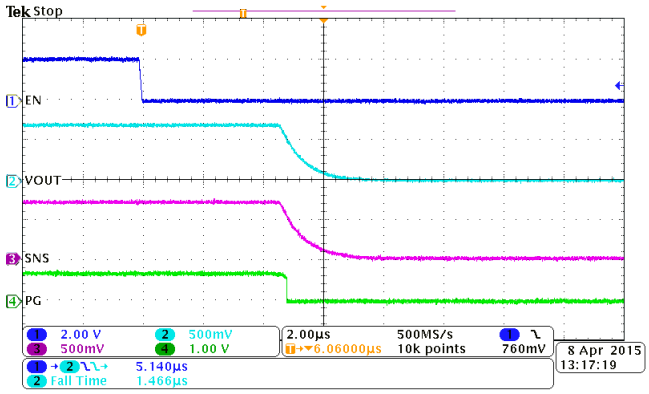
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-31. Turn-off Waveform, V_{BIAS} = 2.5 V



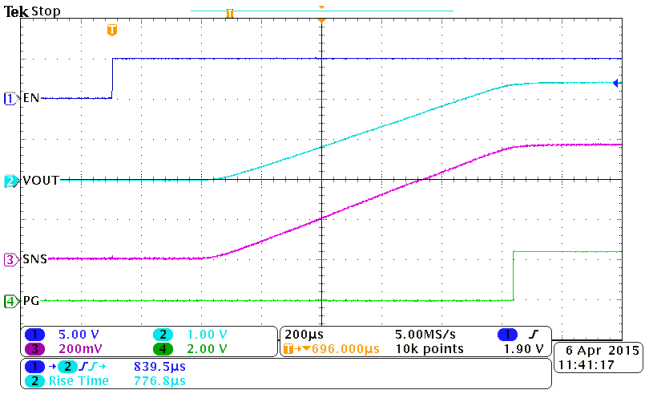
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-32. Turn-on Waveform, V_{BIAS} = 5 V



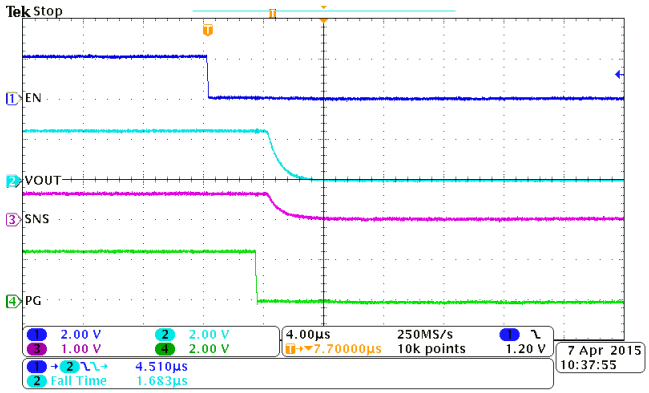
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-33. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

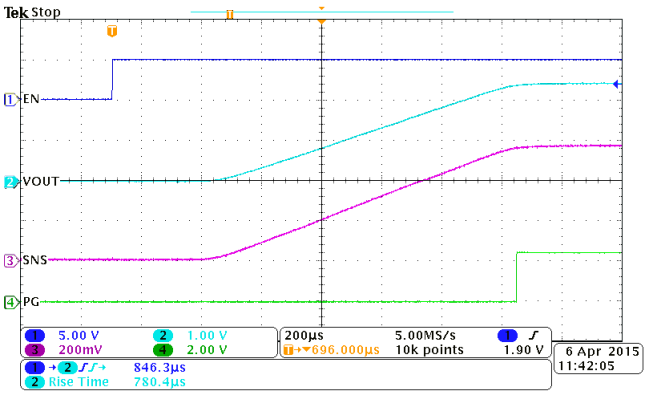
Figure 7-34. Turn-on Waveform, V_{BIAS} = 2.5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

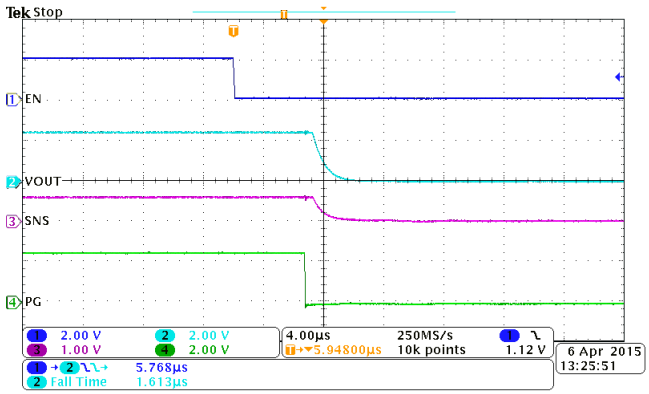
Figure 7-35. Turn-off Waveform, V_{BIAS} = 2.5 V

7.11 Typical Switching Characteristics (continued)



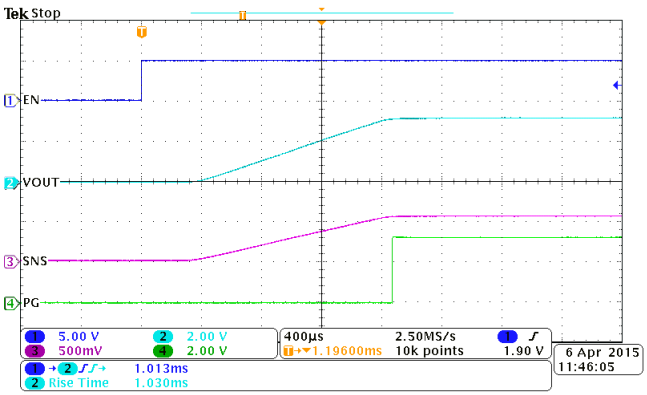
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-36. Turn-on Waveform, V_{BIAS} = 5 V



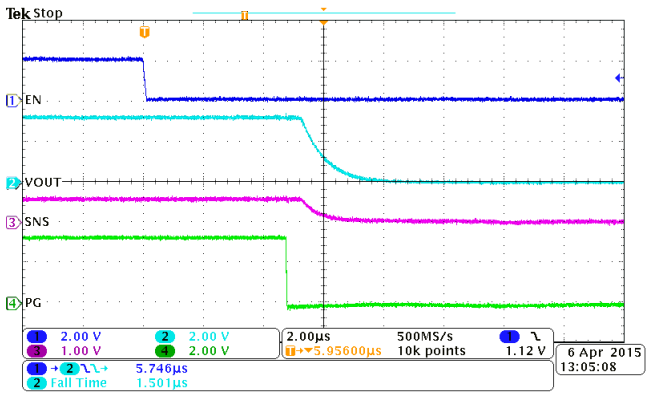
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-37. Turn-off Waveform, V_{BIAS} = 5 V



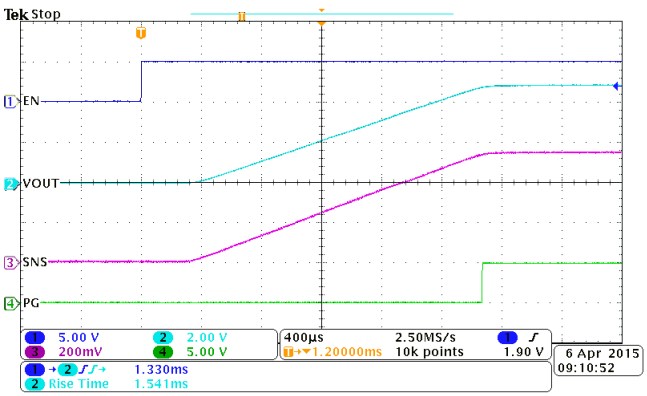
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-38. Turn-on Waveform, V_{BIAS} = 5 V



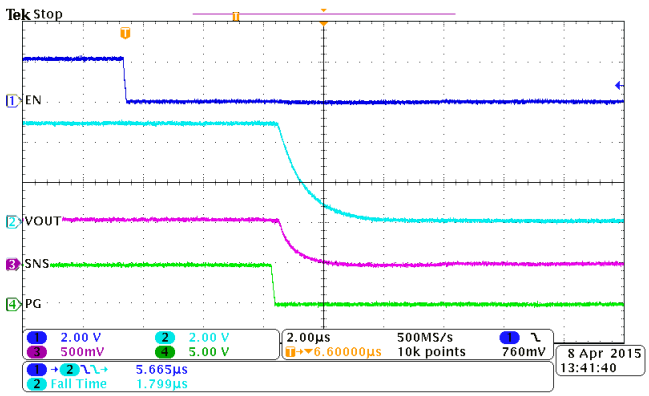
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-39. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

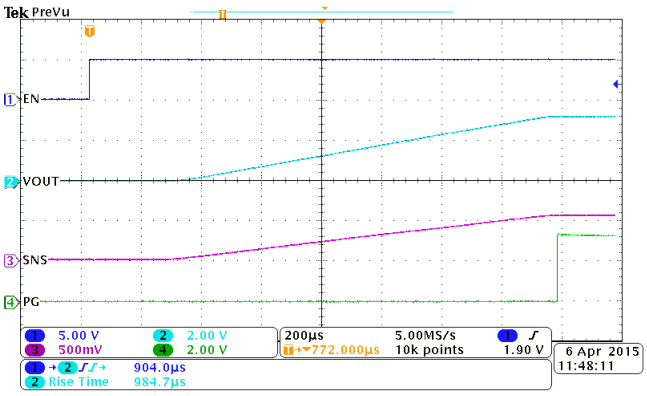
Figure 7-40. Turn-on Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

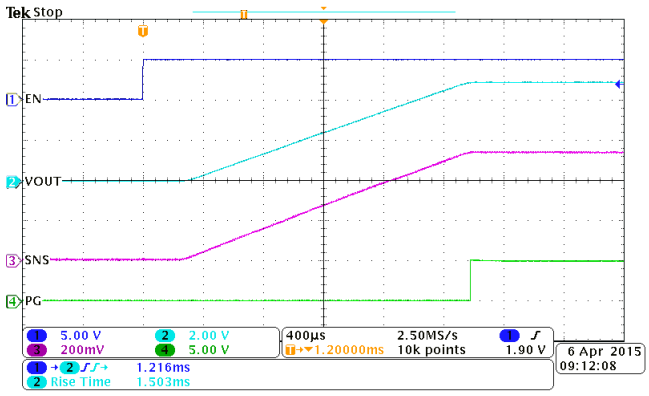
Figure 7-41. Turn-off Waveform, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics (continued)



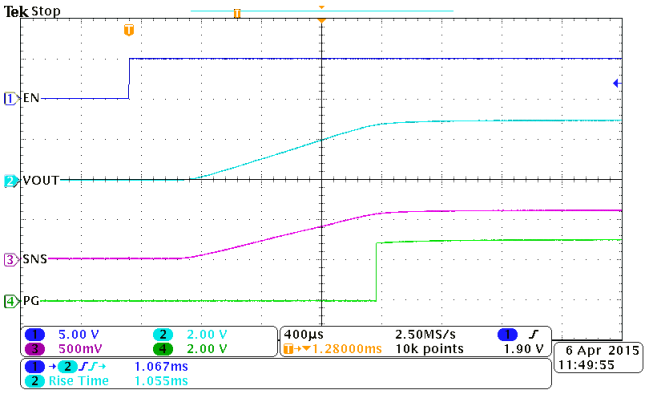
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-42. Turn-on Waveform, No Load



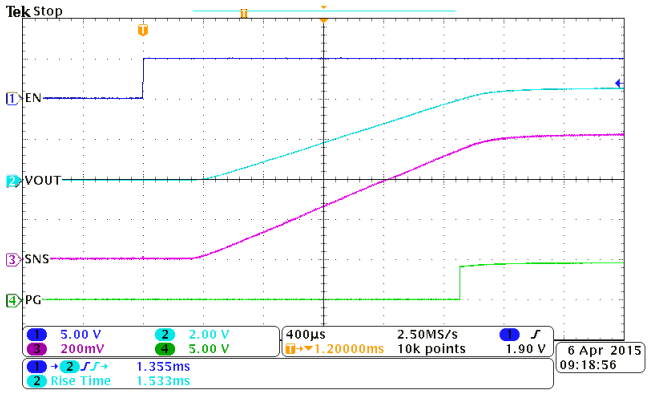
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-43. Turn-on Waveform, No Load



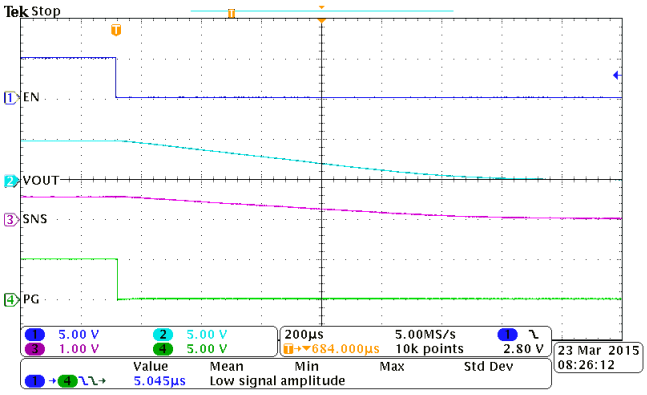
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-44. Turn-on Waveform, Heavy Load



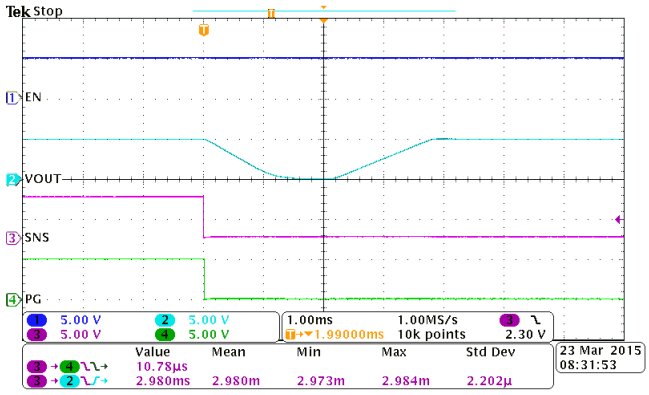
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-45. Turn-on Waveform, Heavy Load



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

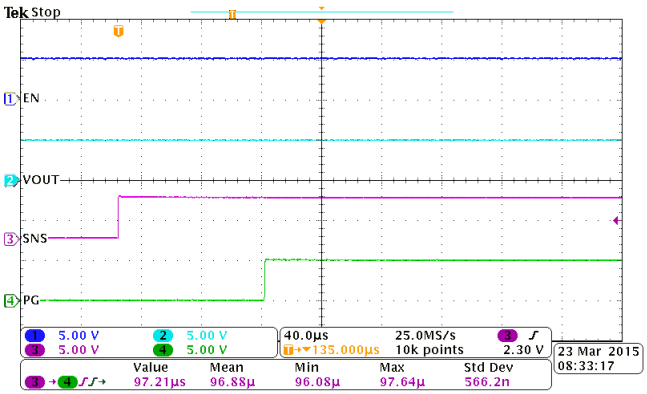
Figure 7-46. PG Response to EN Falling ($t_{DEGLITCH}$)



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

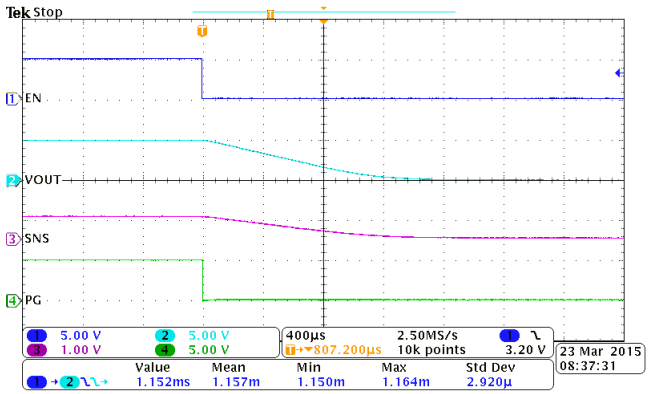
Figure 7-47. PG Response to SNS Falling With Auto-Restart ($t_{DEGLITCH}$ and $t_{RESTART}$)

7.11 Typical Switching Characteristics (continued)



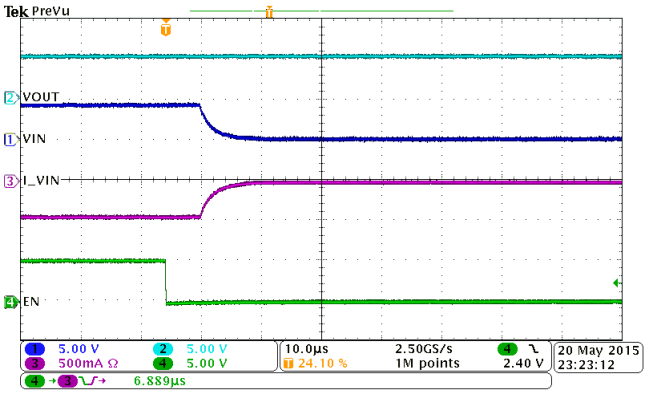
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

Figure 7-48. PG Response to SNS Rising (t_{BLANK})



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = None

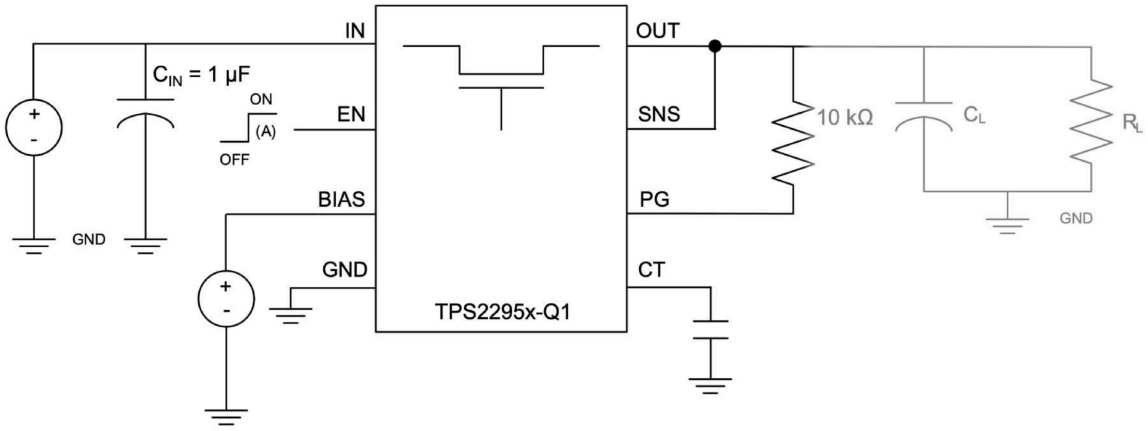
Figure 7-49. Quick Output Discharge of 100-µF Load (t_{DIS})



V_{IN} = 10 Ω to GND V_{BIAS} = 5 V
C_{IN} = 0.2 µF V_{OUT} = 5 V

Figure 7-50. Reverse Current Blocking Response Time (t_{RCB})

8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100 ns.

Figure 8-1. Timing Test Circuit

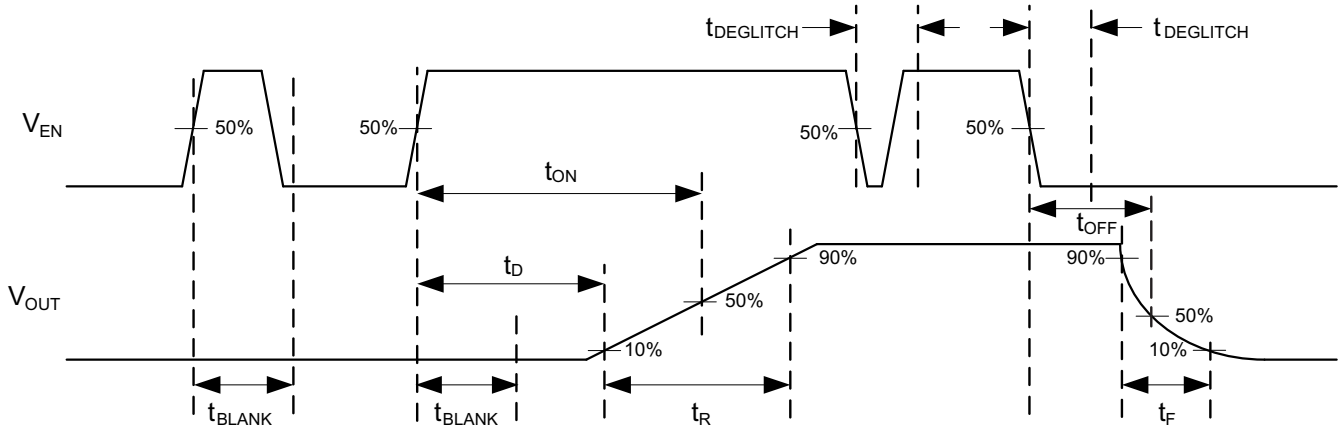


Figure 8-2. Timing Waveforms

9 Detailed Description

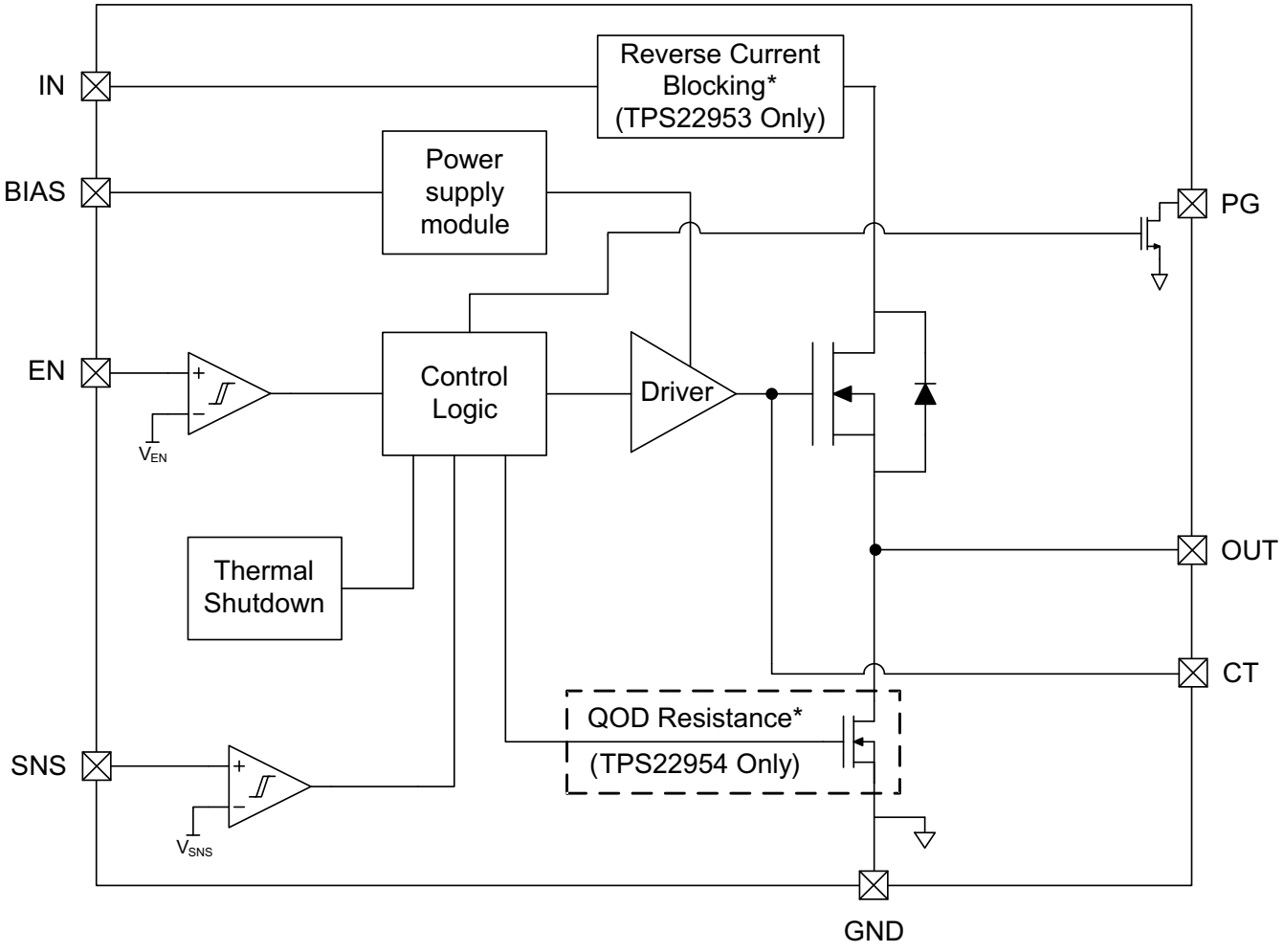
9.1 Overview

The TPS2295x-Q1 are 5.7-V, 5-A load switches in 10-pin SON packages. To reduce voltage drop for low voltage, high current rails the device implements a low-resistance N-channel MOSFET, which reduces the drop out voltage through the device at high currents. The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing.

The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω, on-chip load resistor integrates into the device for output quick discharge when the switch turns off.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated power monitoring functionality, control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



(*) Only active when the switch is disabled.

9.3 Feature Description

9.3.1 On and Off Control (EN Pin)

The EN pin controls the state of the switch. When the voltage on EN exceeds $V_{IH,EN}$ the switch enables. When EN goes below $V_{IL,EN}$ the switch disables.

The EN pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,EN}$ threshold has been exceeded. The EN pin also has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,EN}$.

The EN pin can also be configured through an external resistor divider to monitor a voltage signal for input UVLO. See Equation 1 and Figure 9-1 on how to configure the EN pin for input UVLO.

$$V_{IH,EN} = V_{IN} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \quad (1)$$

where

- $V_{IH,EN}$ is the rising threshold of the EN pin (see the *Electrical Characteristics* table)
- V_{IN} is the input voltage being monitored (this can be V_{IN}, V_{BIAS}, or an external power supply)
- R_{EN1}, R_{EN2} are the resistor divider values

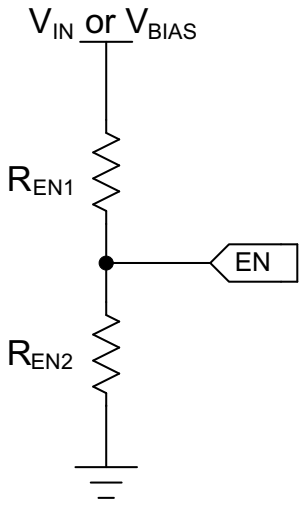


Figure 9-1. Resistor Divider (EN Pin)

9.3.2 Voltage Monitoring (SNS Pin)

The SNS pin of the device can be used to monitor the output voltage of the device or another voltage rail. The pin can be configured with an external resistor divider to set the desired trip point for the voltage being monitored or be tied to OUT directly. If the voltage on the SNS pin exceeds $V_{IH,SNS}$, the voltage being monitored on the SNS pin is considered to be valid high. The voltage on the SNS pin must be greater than $V_{IH,SNS}$ for at least t_{BLANK} before PG is asserted high. If the voltage on the SNS pin goes below $V_{IL,SNS}$, then the switch powers cycle (that is, the switch is disabled and re-enabled). For proper functionality of the device, this pin must not be left floating. If a resistor divider is not being used for voltage sensing, this pin can be tied directly to V_{OUT}.

The SNS pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,SNS}$ threshold has been exceeded. The SNS pin has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,SNS}$.

See Equation 2 and Figure 9-2 on how to configure the SNS pin for voltage monitoring.

$$V_{IH,SNS} = V_{OUT} \times \frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}} \tag{2}$$

where

- $V_{IH,SNS}$ is the the rising threshold of the SNS pin (see *Electrical Characteristics* table)
- V_{OUT} is the voltage on the OUTpin
- R_{SNS1}, R_{SNS2} are the resistor divider values

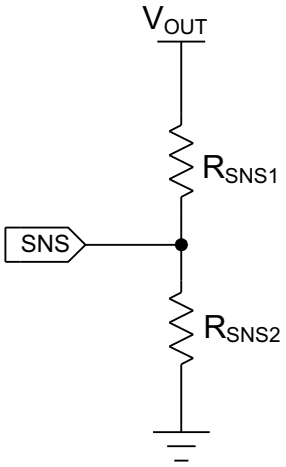


Figure 9-2. Voltage Divdier (SNS Pin)

9.3.3 Power Good (PG Pin)

The PG pin is only asserted high when the voltage on EN exceeds $V_{IH,EN}$ and the voltage on SNS exceeds $V_{IH,SNS}$. There is a t_{BLANK} time, typically 100 µs, between the SNS voltage exceeding $V_{IH,SNS}$ and PG being asserted high. If the voltage on EN goes below $V_{IL,EN}$ or the voltage on SNS goes below $V_{IL,SNS}$, PG is de-asserted. There is a $t_{DEGLITCH}$ time, typically 5 µs, between the EN voltage or SNS voltage going below their respective V_{IL} levels and PG being pulled low.

PG is an open drain pin and must be pulled up with a pullup resistor. Be sure to never exceed the maximum operating voltage on this pin. If PG is not being used in the application, tie it to GND for proper device functionality.

For proper PG operation, the BIAS voltage must be within the recommended operating range. In systems that are very sensitive to noise or have long PG traces, TI recommends to add a small capacitance from PG to GND for decoupling.

9.3.4 Supervisor Fault Detection and Automatic Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$. In the case, the SNS pin is being used to monitor V_{OUT} or a downstream voltage. The restart helps to protect against excessive overcurrent if there is a quick short to GND. See Figure 9-3.

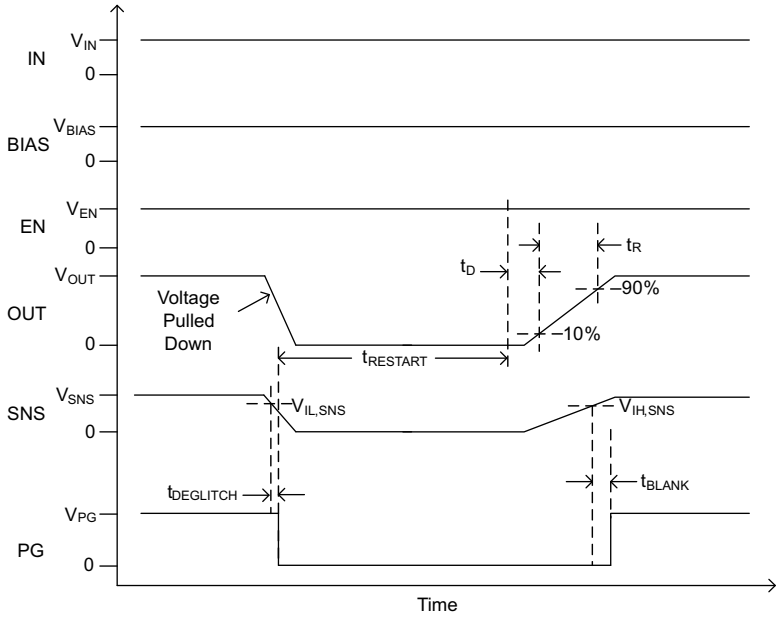


Figure 9-3. Automatic Restart After Quick Short to GND

9.3.5 Manual Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). The SNS pin can be driven by an MCU to manually reset the load switch. After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$, even is SNS is held low. The PG pin stays low until the switch is re-enabled and the SNS pin rises above $V_{IH,SNS}$. See Figure 9-4.

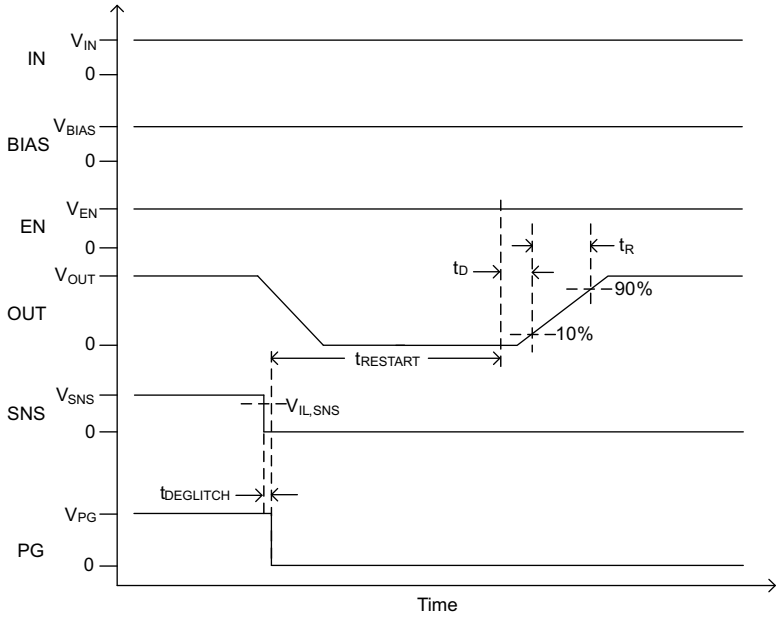


Figure 9-4. Manual Restart (SNS Held Low)

If the SNS pin is brought above $V_{IH,SNS}$ within the $t_{RESTART}$ time, the switch still waits to re-enable. The PG pin also stays low until t_{BLANK} after switch is re-enabled. In this case, PG indicates when the switch is enabled and capable of being reset again. See Figure 9-5.

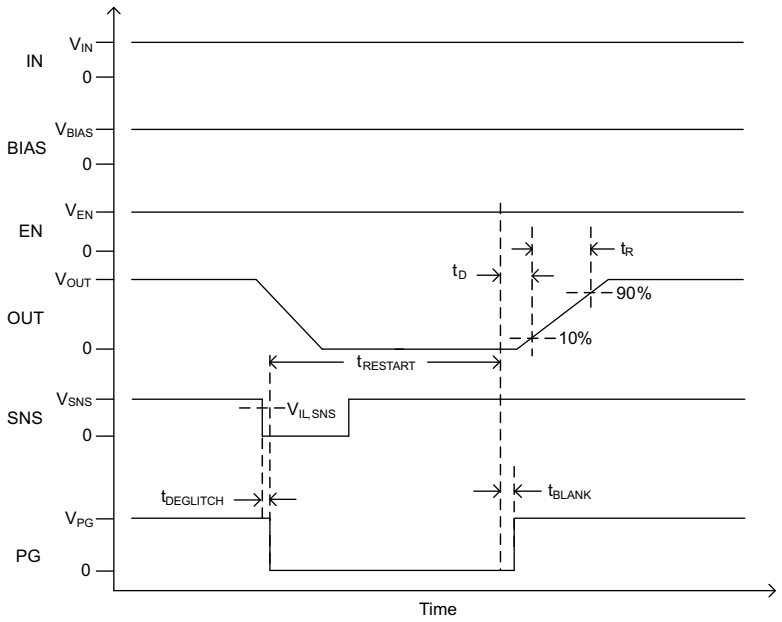


Figure 9-5. Manual Restart (SNS Toggled Low to High)

9.3.6 Thermal Shutdown

If the junction temperature of the device exceeds T_{SD}, the switch disables. The device enables after the junction temperature drops by TSD_{HYS} as long as EN is still greater than $V_{IH,EN}$.

9.3.7 Reverse Current Blocking (TPS22953-Q1 Only)

When the switch disables (either by de-asserting EN or SNS, triggering thermal shutdown, or losing power), the reverse current blocking (RCB) feature of the device engages within t_{RCB}, typically 10 µs. After the RCB engages, the reverse current from the OUT pin to the IN pin is limited to $I_{RCB,IN}$, typically 0.01 µA.

9.3.8 Quick Output Discharge (QOD) (TPS22954-Q1 Only)

The Quick Output Discharge (QOD) transistor is engaged indefinitely whenever the switch is disabled and the recommended V_{BIAS} voltage is met. During this state, the QOD resistance (R_{PD}) discharges V_{OUT} to GND. TI does not recommend to apply a continuous DC voltage to OUT when the device is disabled.

The QOD transistor can remain active for a short period of time even after V_{BIAS} loses power. This brief period of time is defined as t_{DIS}. For best results, TI recommends the device get disabled before V_{BIAS} goes below the minimum recommended voltage. The waveform in Figure 9-6 shows the behavior when power is applied and then removed in a typical application.

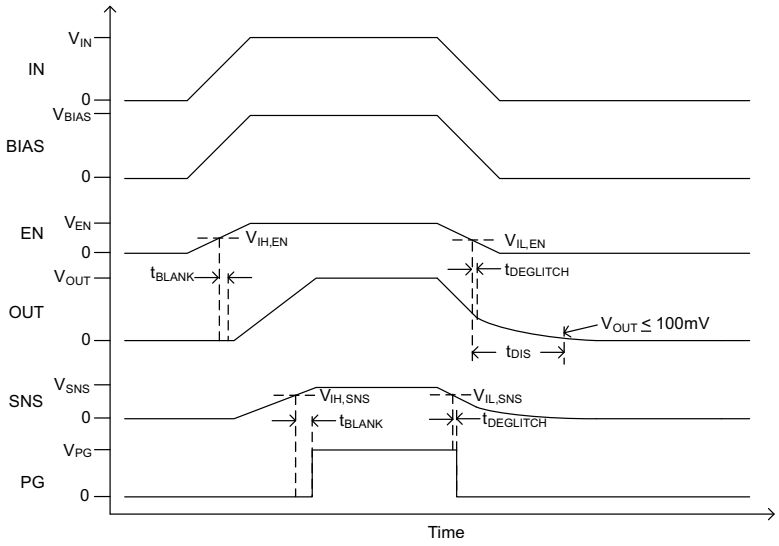


Figure 9-6. Power Applied and Then Removed in a Typical Application

At the end of the t_{DIS} time, it is not assured that V_{OUT} is 0 V because the final voltage is dependent upon the initial voltage and the C_L capacitor. The final V_{OUT} can be calculated with Equation 3 for a given initial voltage and C_L capacitor.

$$V_f = V_o \times e^{\frac{-t}{RC}} \tag{3}$$

where

- V_f is the final V_{OUT} voltage
- V_o is the initial V_{OUT} voltage
- R is the the value of the output discharge resistor, R_{PD} (see the *Electrical Characteristics* table)
- C is the output bulk capacitance on OUT

9.3.9 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics* table. See Figure 9-7 for an example of a typical

device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

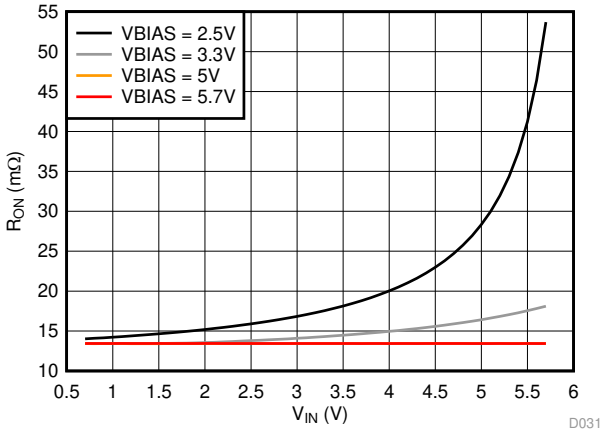


Figure 9-7. R_{ON} When V_{IN} > V_{BIAS}

9.3.10 Adjustable Rise Time (CT Pin)

A capacitor to GND on the CT pin sets the slew rate for V_{OUT}. An appropriate capacitance value must be placed on CT such that the I_{MAX} and I_{PLS} specifications of the device are not violated. The capacitor to GND on the CT pin must be rated for 25 V or higher. Equation 4 shows an approximate formula for the relationship between CT (except for CT = open) and the slew rate for any V_{BIAS}.

$$SR = 0.35 \times CT + 20 \quad (4)$$

where

- SR is the slew rate (in µs/V).
- CT is the capacitance value on the CT terminal (in pF).
- The units for the constant 20 are µs/V.
- The units for the constant 0.35 are µs/(V*pF).

Rise time can be calculated by multiplying the input voltage (typically 10% to 90%) by the slew rate. Table 9-1 contains rise time values measured on a typical device.

Table 9-1. Rise Time

CTx (pF)	RISE TIME (µs) 10% – 90%, C_L = 0.1 µF, V_{BIAS} = 2.5 V to 5.7 V, R_L = 10-Ω LOAD. TYPICAL VALUES AT 25°C, 25-V X7R 10% CERAMIC CAP					
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	0.7 V
Open	140	98	62	54	46	32
220	444	301	175	150	124	81
470	767	518	299	255	210	133
1000	1492	994	562	474	387	245
2200	3105	2050	1151	961	787	490
4700	6420	4246	2365	1980	1612	998
10000	14059	9339	5183	4331	3533	2197

9.3.11 Power Sequencing

The TPS2295x-Q1 operates regardless of power-on and power-off sequencing order. The order in which voltages are applied to IN, BIAS, and EN does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions. If voltage is applied to EN before IN and BIAS, the slew rate of VOUT is not controlled. Also, turning off IN or BIAS while EN is high does not damage the device.

9.4 Device Functional Modes

Table 9-2 describes what the OUT pin is connected to for a particular device as determined by the EN pin.

Table 9-2. Function Table

EN	TPS22953-Q1	TPS22954-Q1
L	OPEN	R_{PD} to GND
H	IN	IN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available on www.ti.com for further aid.

10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this data sheet. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} voltage conditions, use Equation 5 to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{5}$$

where

- ΔV is the voltage drop from IN to OUT
- I_{LOAD} is the load current
- R_{ON} is the On-Resistance of the device for a specific V_{IN} and V_{BIAS}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 Thermal Considerations

The maximum IC junction temperature must be restricted to just under the thermal shutdown (T_{SD}) limit of the device. Use Equation 6 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{6}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.
- $T_{J(max)}$ is the maximum allowable junction temperature before hitting thermal shutdown (see the *Electrical Characteristics* table).
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

10.1.3 Automatic Power Sequencing

The PG pin of the TPS2295x-Q1 allows for automatic sequencing of multiple system rails or loads. The accurate SNS voltage monitoring ensures the first rail is up before the next starts to turn on. This approach provides robust system sequencing and reduces the total inrush current by preventing overlap. Figure 10-1 shows how two rails can be sequenced. There is no limit to the number of rails that can be sequenced in this way.

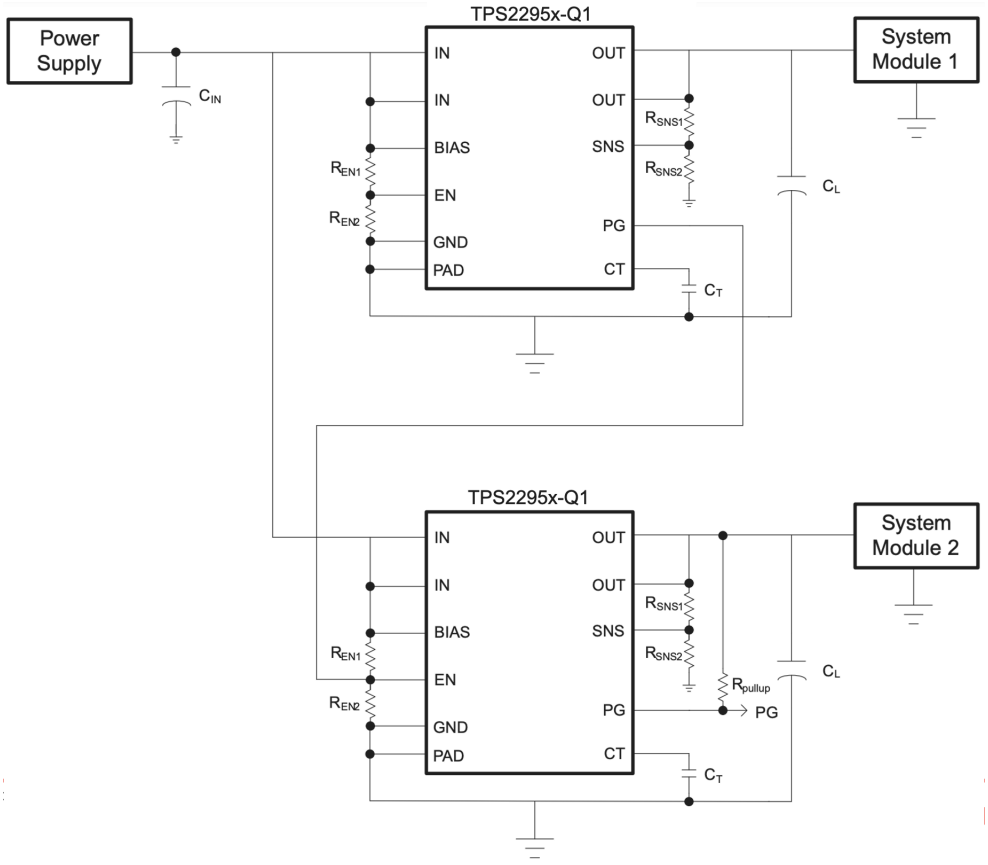


Figure 10-1. Power Sequencing with PG Control Schematic

10.1.4 Monitoring a Downstream Voltage

The SNS pin can be used to monitor other system voltages in addition to V_{OUT}. The status of the monitored voltage are indicated by the PG pin which can be pulled up to V_{OUT} or another voltage. Figure 10-2 shows an example of the TPS2295x-Q1 monitoring the output of a downstream DC/DC regulator. In this case, the switch turns on when the power supply is above the UVLO, but the PG is not asserted until the DC/DC regulator has started up.

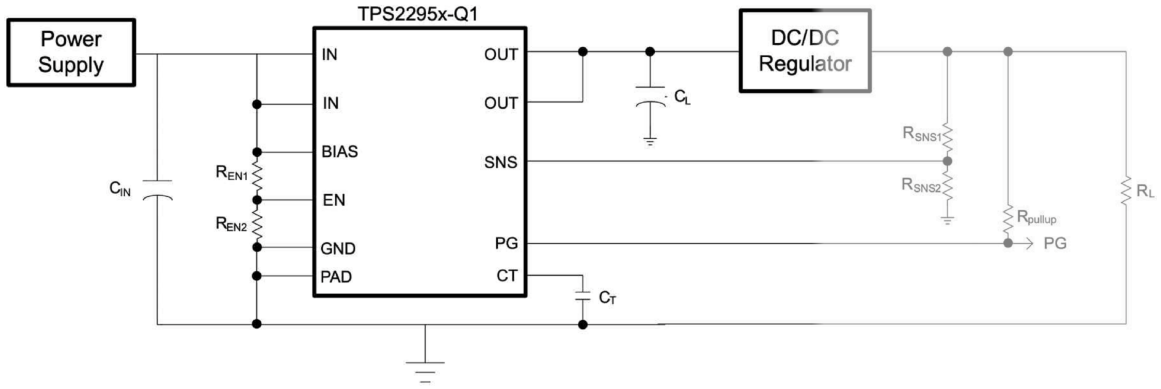


Figure 10-2. Monitoring a Downstream Voltage Schematic

In this application, if the DC/DC Regulator is shut down, the supervisor registers this as a fault case and resets the load switch.

10.1.5 Monitoring the Input Voltage

The SNS pin can also be used to monitor V_{IN} in the case a MCU GPIO is being used to control the EN. This event allows PG to report on the status of the input voltage when the switch is enabled. See Figure 10-3.

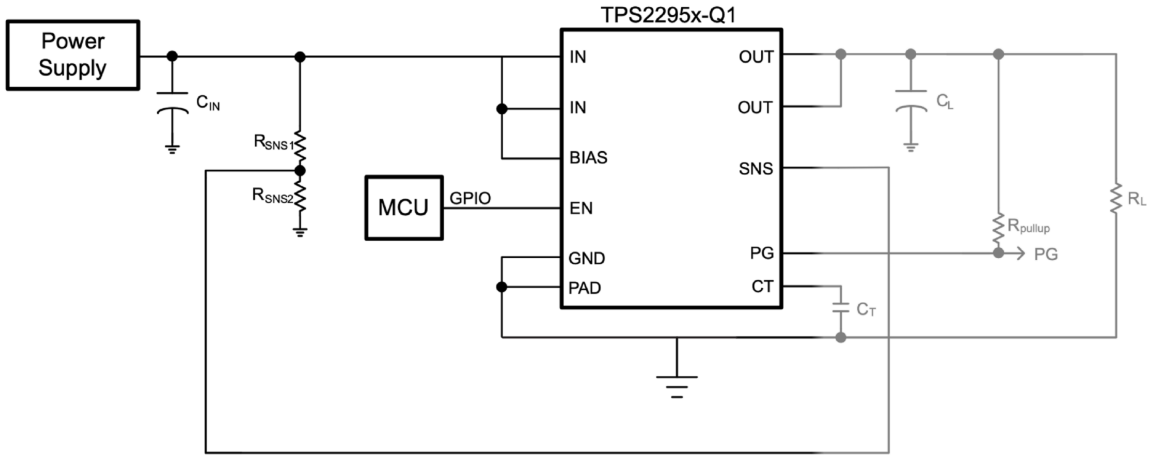


Figure 10-3. Monitoring the Input Voltage Schematic

10.1.6 Break-Before-Make Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement break-before-make logic. The circuit in Figure 10-4 shows how the detection of power supply 1 can be used to disable the load switch for power supply 2. By tying the SNS of Load Switch 1 directly to the input, its PG pin is pulled up as soon as the device is enabled.

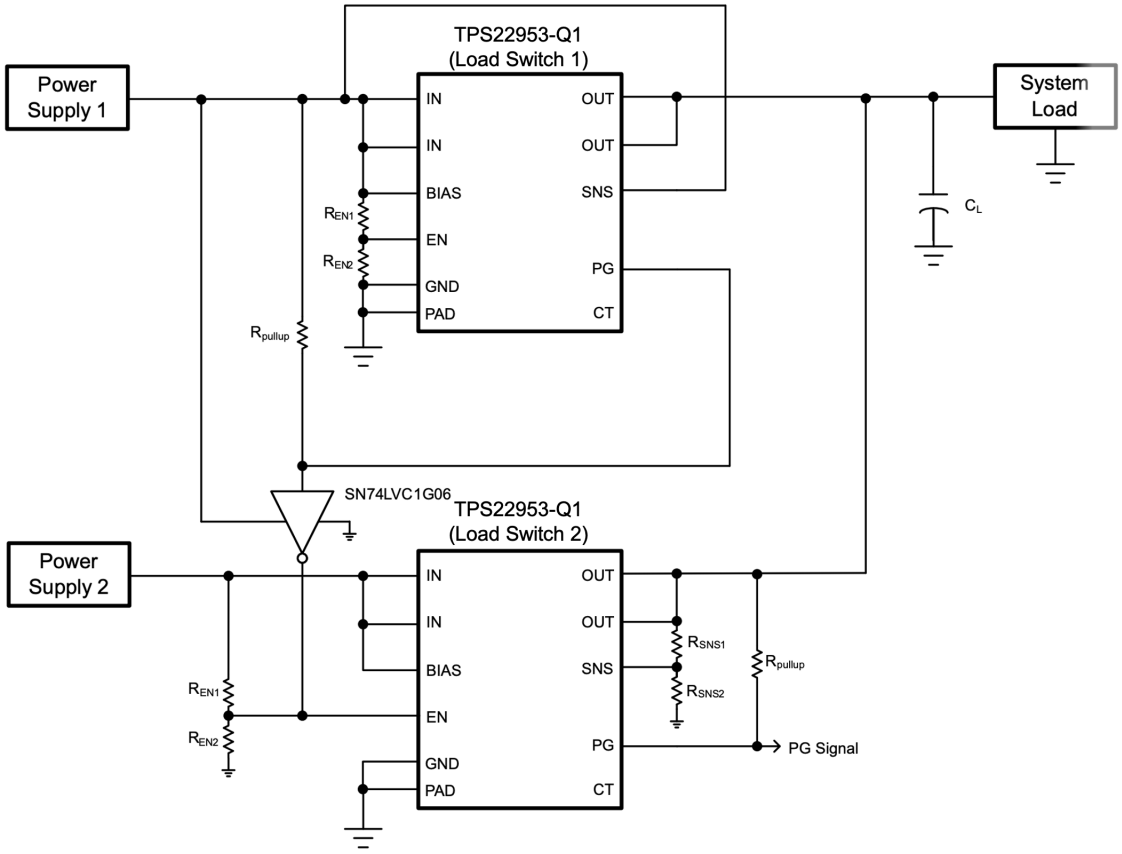


Figure 10-4. Break-Before-Make Power MUX Schematic

The break-before-make logic ensures that power supply 2 is completely disconnected before power supply 1 is connected. This approach provides very robust reverse current blocking. However, in most cases, this aproach also results in a dip in the output voltage when switching between supplies.

The amount of voltage dip depends on the loading, the output capacitance, and the turn-on delay of the load switch. In this application, leaving the CT pin open results in the shortest turn-on delay and minimizes the output voltage dip.

Table 10-1 summarizes the logic of the PG Signal for Figure 10-4.

Table 10-1. Break-Before-Make PG Signal

PG Signal	Indication
H	Power supply 1 not present. System powered from power supply 2.
L	Power supply 1 present. System powered from power supply 1.

10.1.7 Make-Before-Break Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement make-before-break logic. The circuit in Figure 10-5 shows how the detection of Load Switch 1 turning on can be used to disable the load switch for power supply 2. By tying SNS to the Load, the PG is pulled up when the output voltage starts to rise. This event disables an active low load switch such as the TPS22910A.

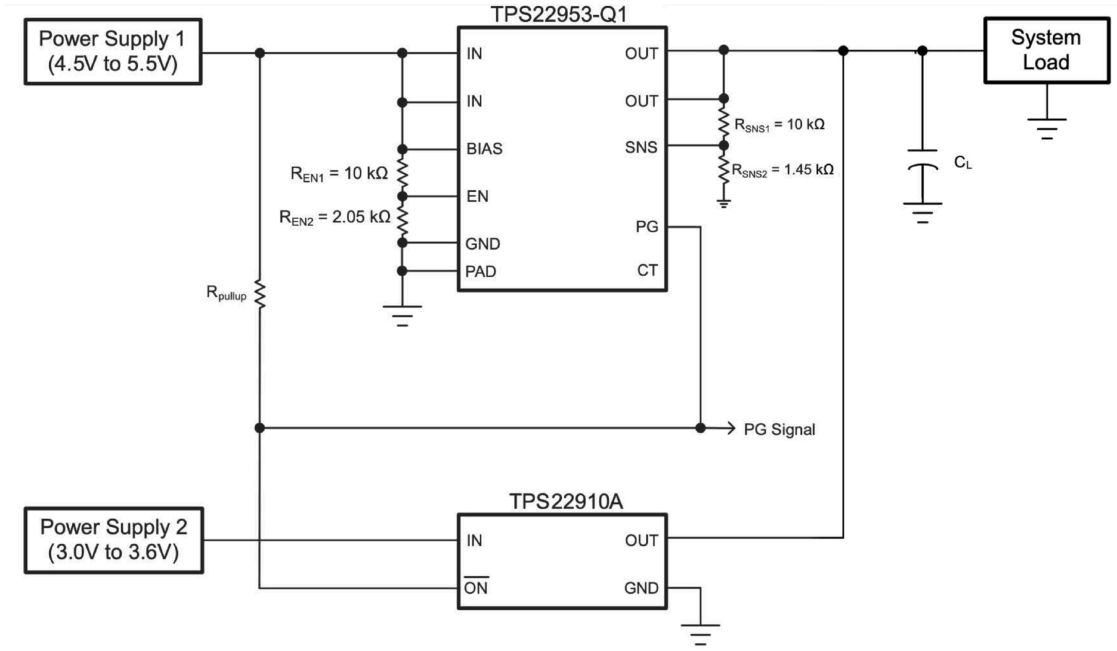


Figure 10-5. Make-Before-Break Power MUX Schematic

The make-before-break logic ensures that power supply 2 is not disconnected until power supply 1 is connected. Unlike break-before-make logic, this approach is ideal for preventing voltage dip on the output when switching between supplies. However, in most cases, this approach also results in temporary reverse current flow.

The TPS22910A is well suited for this application because it can detect and block reverse current even before it is disabled by the TPS22953-Q1 PG signal. Also, the active low enable of the TPS22910A eliminates the need for an inverter as shown in the previous example.

To ensure correct logic, the SNS pin must be configured to toggle PG when the load voltage is between the two supply voltages (3.6 V to 4.5 V). The SNS resistor values in Figure 10-5 are assuming a tolerance of ±1% or better.

Table 10-2 summarizes the logic of the PG Signal for Figure 10-5.

Table 10-2. Make-Before-Break PG Signal

PG Signal	Indication
H	Power supply 1 present. System powered from power supply 1.
L	Power supply 1 not present. System powered from power supply 2.

10.2 Typical Application

This application demonstrates how the TPS2295x-Q1 can be used to limit inrush current to output capacitance.

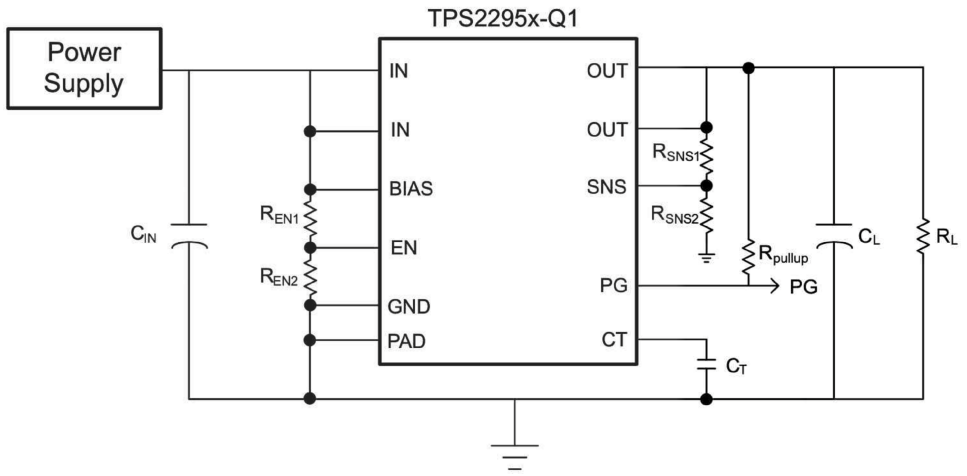


Figure 10-6. Powering a Downstream Module Schematic

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-3.

Table 10-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	47 µF
Maximum acceptable inrush current	150 mA
R_L	None

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- Input voltage
- BIAS voltage
- Load current
- Load capacitance
- Maximum acceptable inrush current

10.2.2.1 Inrush Current

Use Equation 7 to determine how much inrush current is caused by the C_L capacitor.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \tag{7}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the load capacitance on V_{OUT}
- dt is the V_{OUT} rise time (typically 10% to 90%)
- dV_{OUT} is the change in V_{OUT} Voltage (typically 10% to 90%)

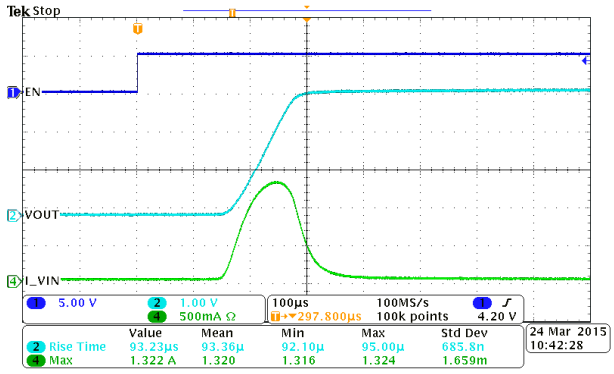
In this case, a Slew Rate slower than 314 µs/V is required to meet the maximum acceptable inrush requirement. Equation 4 can be used to estimate the CT capacitance (as shown in Equation 8 and Equation 9) required for this slew rate.

$$314\ \mu s/V = 0.35 \times CT + 20 \quad (8)$$

$$CT = 840\ pF \quad (9)$$

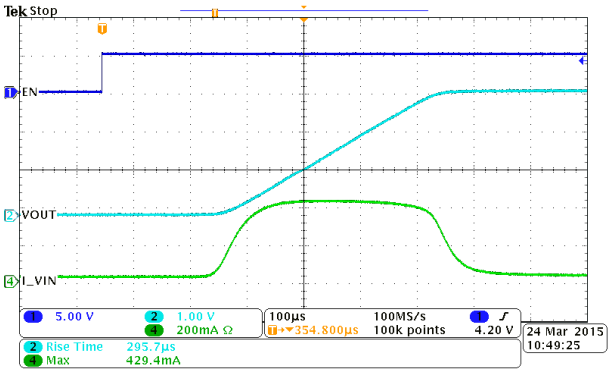
10.2.3 Application Curves

The following Application Curves show the inrush with multiple different CT values. These curves show only a CT capacitance greater than 840 pF results in the acceptable inrush current of 150 mA.



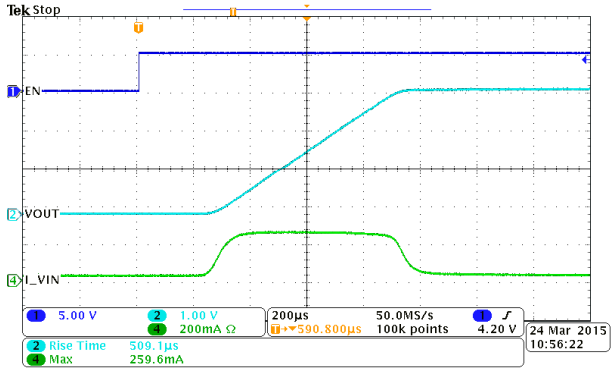
CT = 0 pF

Figure 10-7. Inrush with CT = 0 pF



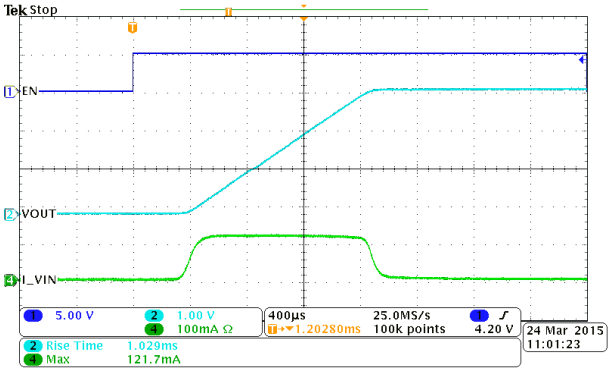
CT = 220 pF

Figure 10-8. Inrush with CT = 220 pF



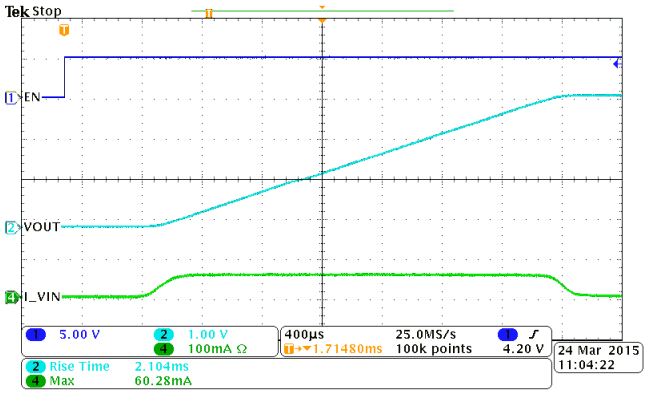
CT = 470 pF

Figure 10-9. Inrush with CT = 470 pF



CT = 1000 pF

Figure 10-10. Inrush with CT = 1000 pF



CT = 2200 pF

Figure 10-11. Inrush with CT = 2200 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.7 V and a V_{IN} range of 0.7 V to 5.7 V. The power supply must be well regulated and placed as close to the device terminals as possible. The power supply must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This action causes the load switch to turn on more slowly. Not only does this event reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

12 Layout

12.1 Layout Guidelines

- Input and Output traces must be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The CT Capacitor must be placed as close as possible to the device to minimize parasitic trace capacitance. TI recommends to cutout copper on other layers directly below CT to minimize parasitic capacitance.
- The IN terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The OUT terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The BIAS terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric.

12.2 Layout Example

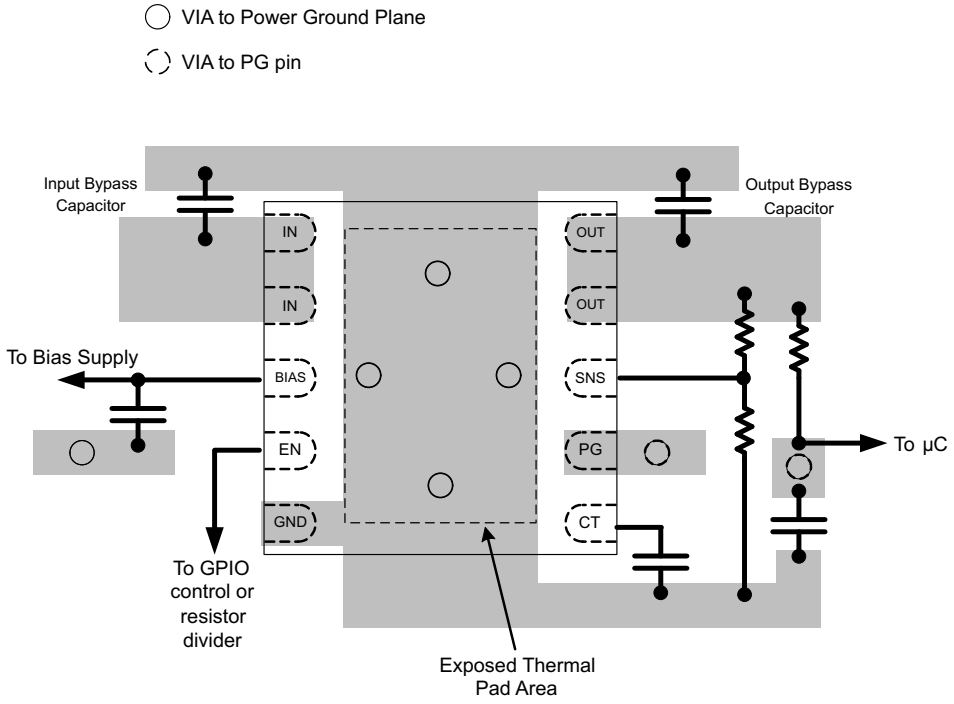


Figure 12-1. Recommended Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS22953/54 5.7-V, 5-A, 14-mΩ On-Resistance Load Switch* user's guide
- Texas Instruments, *Basics of Load Switches* application note
- Texas Instruments, *Managing Inrush Current* application note
- Texas Instruments, *Reverse Current Protection in Load Switches* application note
- Texas Instruments, *Quiescent Current vs Shutdown Current for Load Switch Power Consumption* application note
- Texas Instruments, *Load Switch Thermal Considerations* application note

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22953QDQCRQ1	ACTIVE	WSON	DQC	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS22954QDQCRQ1	ACTIVE	WSON	DQC	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS22953QDQCRQ1	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	953Q1	Samples
TPS22954QDQCRQ1	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	954Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22953-Q1, TPS22954-Q1 :

- Catalog : TPS22953, TPS22954

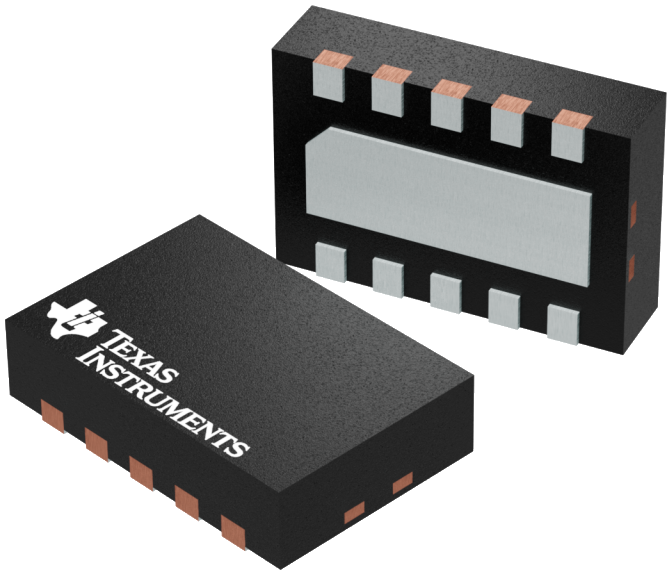
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4209674/B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS22953-Q1, TPS22954-Q1
SLVSGK4A – NOVEMBER 2021 – REVISED JUNE 2022

TPS2295x-Q1 5.7-V, 5-A, 14-mΩ On-Resistance, Automotive Load Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Integrated single channel load switch
- Input voltage range: 0.7 V to 5.7 V
- R_{ON} resistance
  - R_{ON} = 14 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
- 5-A maximum continuous switch current
- Adjustable Undervoltage Lockout Threshold (UVLO)
- Adjustable voltage supervisor with Power Good (PG) indicator
- Adjustable output slew rate control
- Enhanced quick output discharge remains active after power is removed (TPS22954-Q1 only)
  - 15 Ω (typ.) discharges 100 µF within 10 ms
- Reverse current blocking when disabled (TPS22953-Q1 only)
- Automatic restart after supervisor fault detection when enabled
- Thermal shutdown
- Low quiescent current ≤ 50 µA
- SON 10-pin package with thermal pad
- ESD performance tested per JESD 22
  - 2-kV HBM and 750-V CDM

2 Applications

- Infotainment and cluster head unit
- Automotive cluster display
- ADAS surround view system ECU
- Body control module and gateway

3 Description

The TPS2295x-Q1 are small, single channel load switches with controlled turn-on. The devices contain an N-channel MOSFET that can operate over an input voltage range of 0.7 V to 5.7 V and can support a maximum continuous current of 5 A.

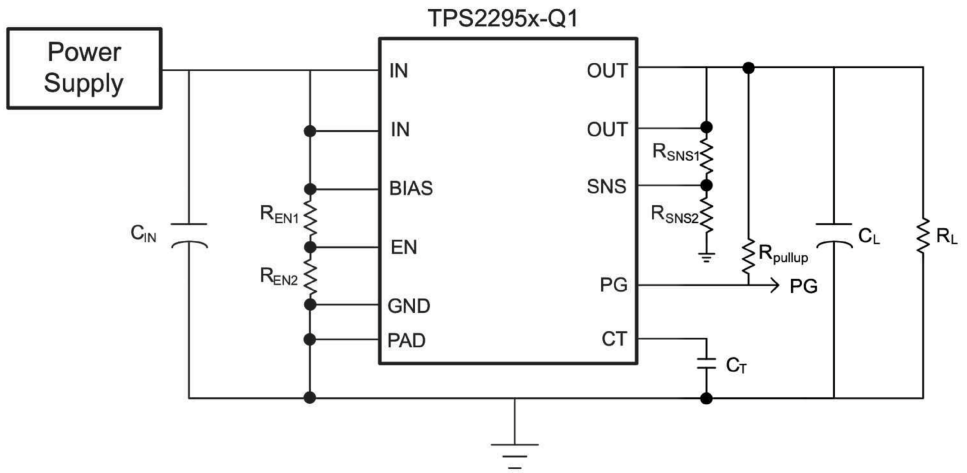
The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing. The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω on-chip load is integrated into the device for a quick discharge of the output when the switch is disabled. The enhanced Quick Output Discharge (QOD) remains active for a short time after power is removed from the device to finish discharging the output.

The TPS2295x-Q1 are available in small, space-saving 10-SON packages with integrated thermal pad, allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TPS2295x-Q1	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (June 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

Device	Quick Output Discharge	Reverse Current Blocking	Package (Pin)	Body Size	Pin Pitch
TPS22954-Q1	Yes	No	DQC (10)	2.00 mm × 3.00 mm	0.5 mm
TPS22953-Q1	No	Yes	DQC (10)	2.00 mm × 3.00 mm	0.5 mm

6 Pin Configuration and Functions

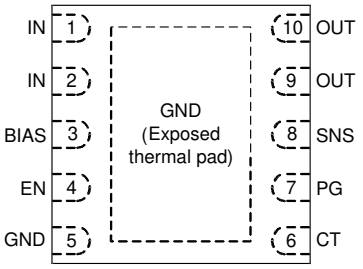


Figure 6-1. DQC/DSQ Package 10-Pin WSON Top View

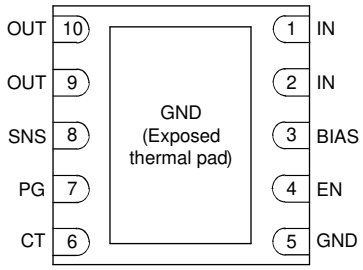


Figure 6-2. DQC/DSQ Package 10-Pin WSON Bottom View

Table 6-1. Pin Functions

PIN[1]		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input. Bypass this input with a ceramic capacitor to GND.
2			
3	BIAS	I	Bias pin and power supply to the device
4	EN	I	Active high switch to enable and disable the output. Also acts as the input UVLO pin. Use external resistor divider to adjust the UVLO level. Do not leave floating.
5	GND	—	Device ground
6	CT	O	V_{OUT} slew rate control. Place ceramic cap from CT to GND to change the V_{OUT} slew rate of the device and limit the inrush current. Rate the CT Capacitor to 25 V or higher.
7	PG	O	Power Good. This pin is open drain which pulls low when the voltage on EN or SNS is below their respective VIL levels.
8	SNS	I	Sense pin. Use external resistor divider to adjust the power good level. Do not leave floating.
9	OUT	O	Switch output
10			
—	Thermal Pad	—	Exposed thermal pad. Tie to GND.

(1) Pinout applies to all package versions.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current, T_A = 70°C		5	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		7	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100- 002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100- 011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.7	V_{BIAS}	V
V_{BIAS}	Bias voltage	2.5	5.7	V
V_{OUT}	Output voltage	0.9	5.7	V
V_{EN}, V_{SNS}, V_{PG}	EN, SNS, and PG voltage	0	5.7	V
TA	Operating free-air temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

7.3 Thermal Information

THERMAL METRIC (1)		TPS2295x-Q1 DQC (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and the recommended VBIAS voltage range of 2.5 V to 5.7 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{EN}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	650	700	750	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	560	600	640	mV
V_{SNS}	V_{IH}, Rising threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	465	515	565	mV
	V_{IL}, Falling threshold	VIN = 0.7V to V_{BIAS}	–40°C to +125°C	410	455	500	mV
t_{BLANK}	Blanking time for EN and SNS	EN or SNS rising	–40°C to +125°C		100		µs
$t_{DEGLITCH}$	Deglitch time for EN and SNS	EN or SNS falling	–40°C to +125°C		5		µs
t_{DIS}	Output discharge time (TPS22954 only)	C_L = 100µF	–40°C to +125°C			10	ms
$t_{RESTART}$	Output restart time	SNS falling	–40°C to +125°C		2		ms
t_{RCB}	Response time for reverse current blocking (TPS22953 only)	V_{OUT} = V_{BIAS} EN falling	–40°C to +125°C		10		µs
T_{SD}	Thermal shutdown	Junction temperature rising	-	130	150	170	°C
TSD_{HYS}	Thermal shutdown hysteresis	Junction temperature falling	-		20		°C
$I_{RCB,IN}$	Input reverse blocking current (TPS22953 only)	V_{OUT} = 5V, V_{IN} = V_{EN} = 0V, V_{BIAS} = 0V to 5.7V	25°C		0.01	2	mΩ
			–40°C to +85°C			5	mΩ
			–40°C to +125°C			11	mΩ

7.5 Electrical Characteristics – VBIAS = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 5 V		–40°C to +85°C		34	45	µA
				–40°C to +125°C			50	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		5	7	µA
				–40°C to +125°C			8	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.02	4	µA
				–40°C to +125°C			13	
			V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.5 Electrical Characteristics – VBIAS = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		14	20	mΩ
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 3.3 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		15	28	Ω
				–40°C to +125°C			30	Ω

7.6 Electrical Characteristics – VBIAS = 3.3 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 3.3 V		–40°C to +85°C		19	35	µA
				–40°C to +125°C			37	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	6	µA
				–40°C to +125°C			7	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 3.3 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7 V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.6 Electrical Characteristics – VBIAS = 3.3 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 3.3 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 3.3 V	25°C		15	21	mΩ
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 1.8 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.5 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 1.2 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
			V_{IN} = 0.7 V	25°C		14	20	
				–40°C to +85°C			23	
				–40°C to +125°C			24	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		13	28	Ω
				–40°C to +125°C			30	Ω

7.7 Electrical Characteristics – VBIAS = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q, BIAS}$	BIAS quiescent current	I_{OUT} = 0, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 2.5 V		–40°C to +85°C		16	25	µA
				–40°C to +125°C			27	
$I_{SD,BIAS}$	BIAS shutdown current	V_{OUT} = 0 V, V_{IN} = 0.7 V to V_{BIAS}, V_{EN} = 0 V to V_{IL}		–40°C to +85°C		4	5	µA
				–40°C to +125°C			6	
$I_{SD, IN}$	Input shutdown current	V_{EN} = 0 V to V_{IL}, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		0.01	3	µA
				–40°C to +125°C			10	
			V_{IN} = 1.8 V	–40°C to +85°C		0.01	3	
				–40°C to +125°C			10	
			V_{IN} = 1.2 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
			V_{IN} = 0.7 V	–40°C to +85°C		0.01	2	
				–40°C to +125°C			8	
I_{EN}	EN pin leakage current	V_{EN} = 0 V to 5.7V		–40°C to +125°C			0.1	µA
I_{SNS}	SNS pin leakage current	VSNS ≤ V_{BIAS}		–40°C to +125°C			0.1	µA

7.7 Electrical Characteristics – VBIAS = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40 °C ≤ TA ≤ +125 °C and VBIAS = 2.5 V. Typical values are for TA = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		16	23	mΩ
				–40°C to +85°C			26	
				–40°C to +125°C			27	
			V_{IN} = 1.8 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.5 V	25°C		15	22	
				–40°C to +85°C			25	
				–40°C to +125°C			26	
			V_{IN} = 1.2 V	25°C		15	22	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
			V_{IN} = 0.7 V	25°C		14	21	
				–40°C to +85°C			24	
				–40°C to +125°C			25	
R_{PD}	Output pull down resistance (TPS22954 only)	V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0 V		25°C		12	28	Ω
				–40°C to +125°C			30	Ω

7.8 Switching Characteristics – CT = 1000 pF

All typical values are at 25°C unless otherwise noted

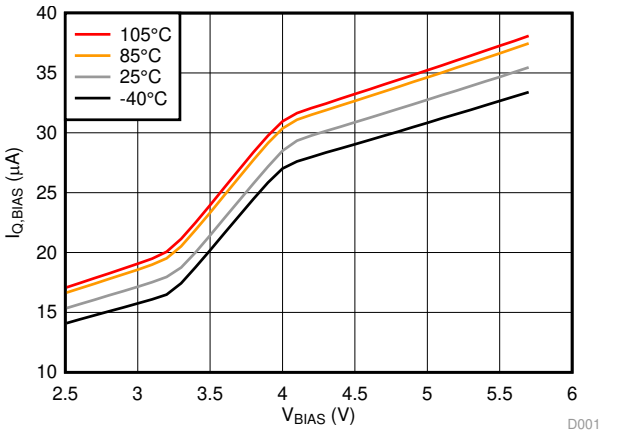
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1265		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1492		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		519		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.2		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		813		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		4.9		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		765		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		430		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		476		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6.1		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		245		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		353		µs

7.9 Switching Characteristics – CT = 0 pF

All typical values are at 25°C unless otherwise noted

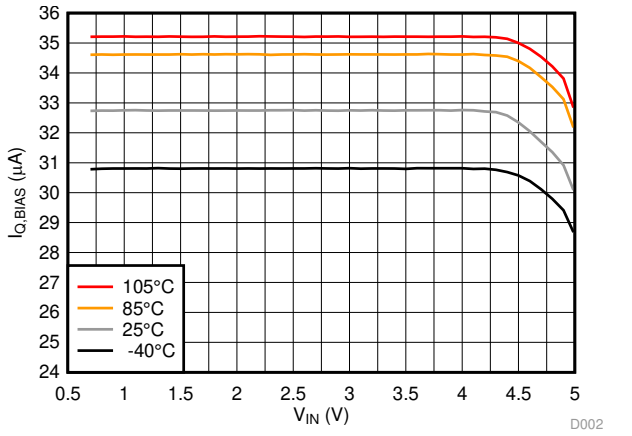
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5 V, V_{EN} = V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		235		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		140		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		165		µs
V_{IN} = 2.5 V, V_{EN} = V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs
V_{IN} = 2.5 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		200		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		79		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2.1		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		160		µs
V_{IN} = 0.7 V, V_{EN} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C						
t_{ON}	Turn-On time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		170		µs
t_{OFF}	Turn-Off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		6		µs
t_R	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		32		µs
t_F	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		2		µs
t_D	Delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 0 pF		154		µs

7.10 Typical DC Characteristics



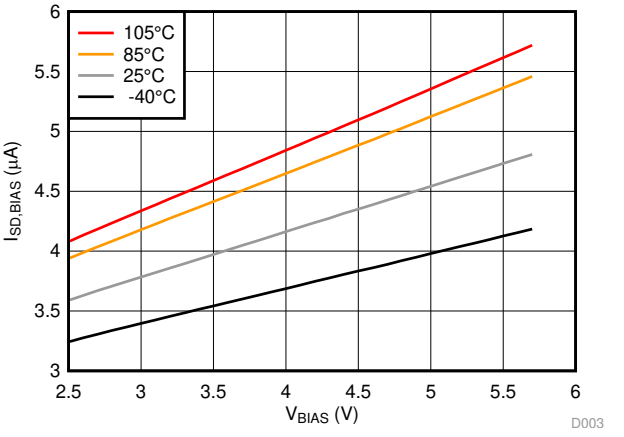
V_{IN} = 1.8 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-1. $I_{Q,BIAS}$ vs V_{BIAS}



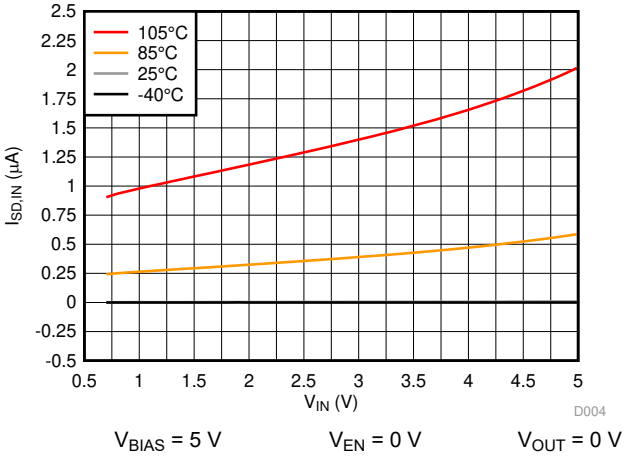
V_{BIAS} = 5 V V_{EN} = 5.7 V V_{OUT} = 0 V

Figure 7-2. $I_{Q,BIAS}$ vs V_{IN}



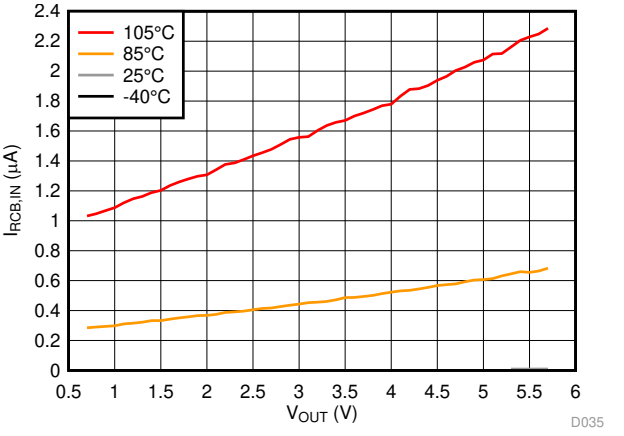
V_{IN} = 1.8 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-3. $I_{SD,BIAS}$ vs V_{BIAS}



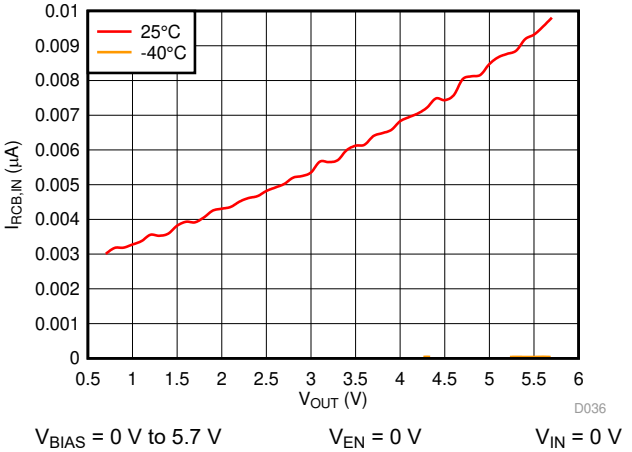
V_{BIAS} = 5 V V_{EN} = 0 V V_{OUT} = 0 V

Figure 7-4. $I_{SD,IN}$ vs V_{IN}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

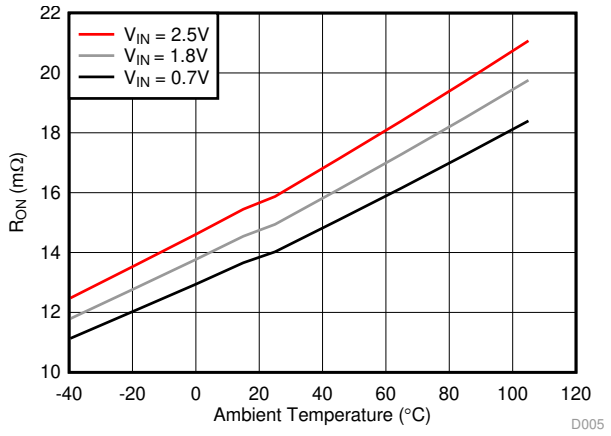
Figure 7-5. $I_{RCB,IN}$ vs V_{OUT}



V_{BIAS} = 0 V to 5.7 V V_{EN} = 0 V V_{IN} = 0 V

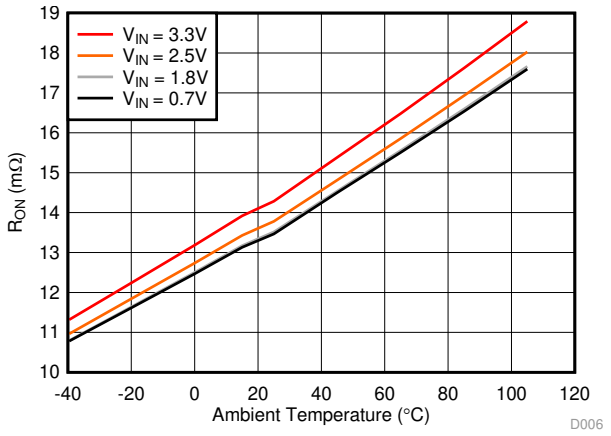
Figure 7-6. $I_{RCB,IN}$ vs V_{OUT}

7.10 Typical DC Characteristics (continued)



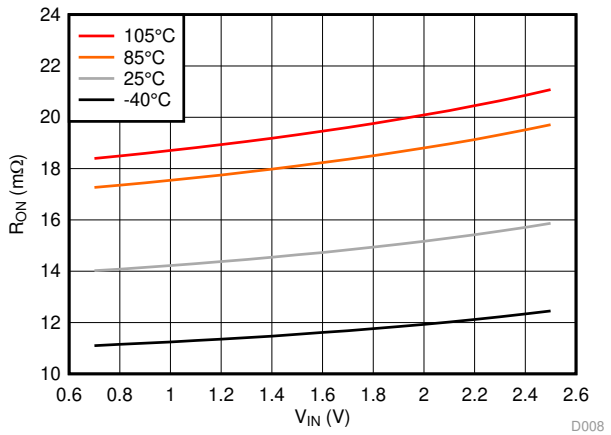
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-7. R_{ON} vs Temperature, V_{BIAS} = 2.5 V



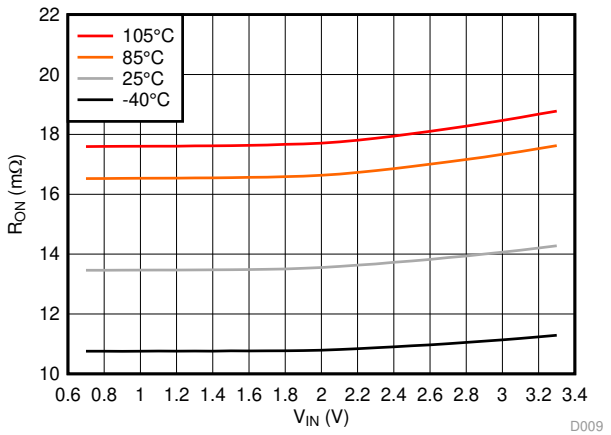
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-8. R_{ON} vs Temperature, V_{BIAS} = 3.3 V



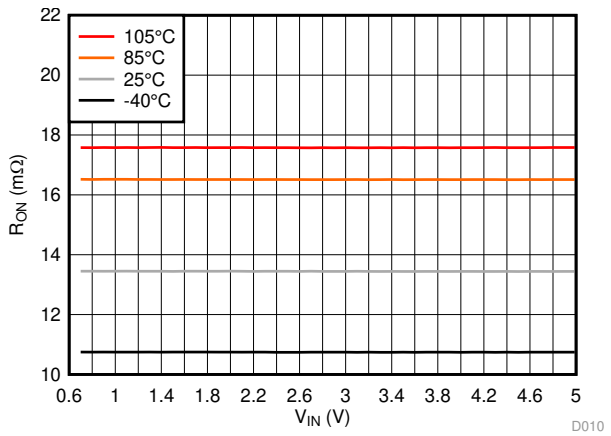
V_{BIAS} = 2.5 V Iout = –200 mA V_{EN} = 5 V

Figure 7-9. R_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



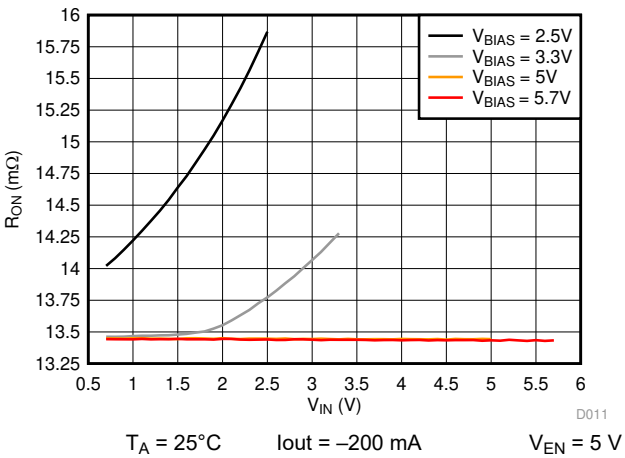
V_{BIAS} = 3.3 V Iout = –200 mA V_{EN} = 5 V

Figure 7-10. R_{ON} vs V_{IN}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V Iout = –200 mA V_{EN} = 5 V

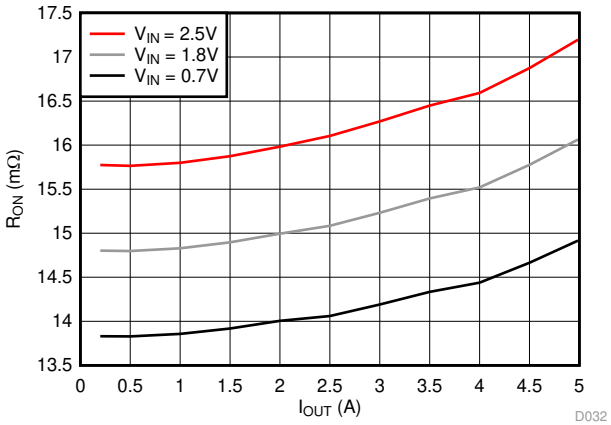
Figure 7-11. R_{ON} vs V_{IN}, V_{BIAS} = 5 V



T_A = 25°C Iout = –200 mA V_{EN} = 5 V

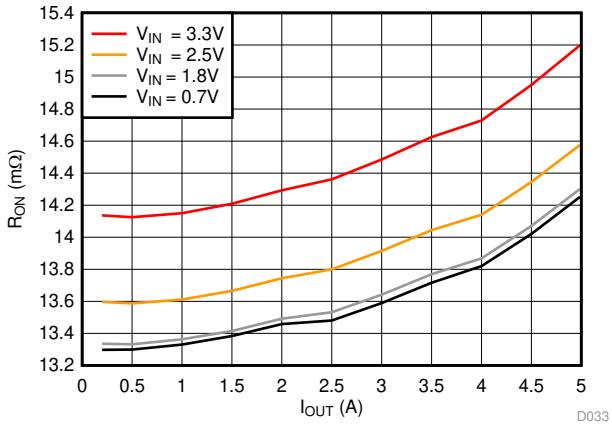
Figure 7-12. R_{ON} vs V_{IN}

7.10 Typical DC Characteristics (continued)



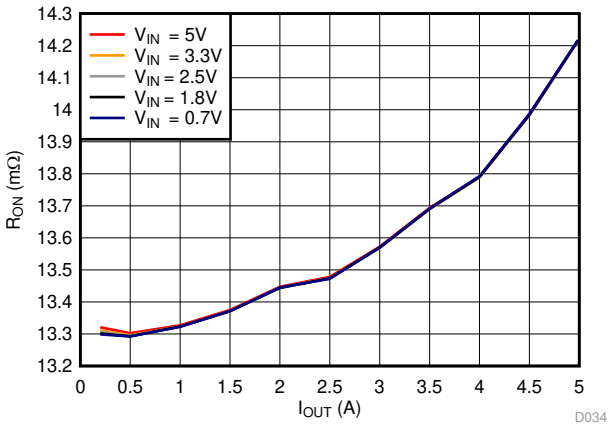
V_{BIAS} = 2.5 V V_{EN} = 5 V

Figure 7-13. R_{ON} vs I_{OUT}, V_{BIAS} = 2.5 V



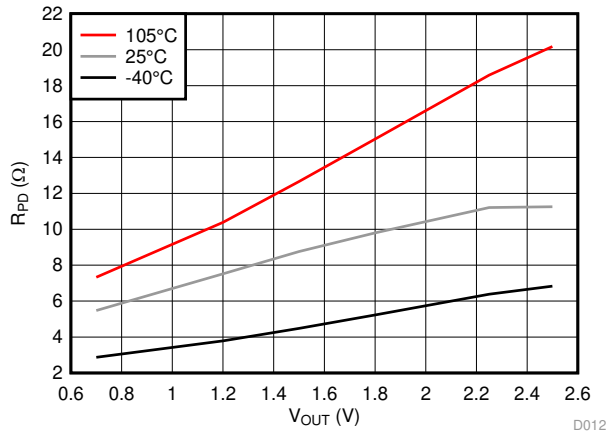
V_{BIAS} = 3.3 V V_{EN} = 5 V

Figure 7-14. R_{ON} vs I_{OUT}, V_{BIAS} = 3.3 V



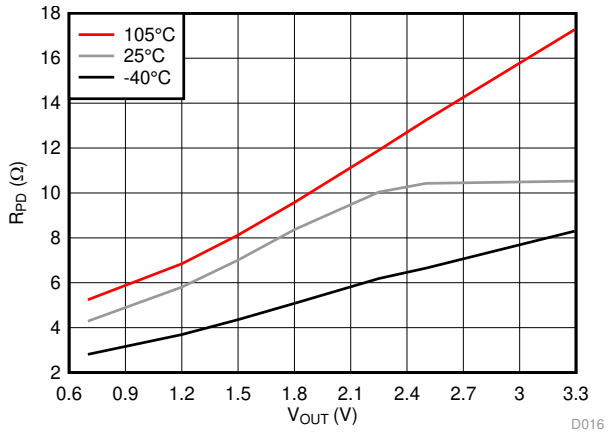
V_{BIAS} = 5 V V_{EN} = 5 V

Figure 7-15. R_{ON} vs I_{OUT}, V_{BIAS} = 5 V



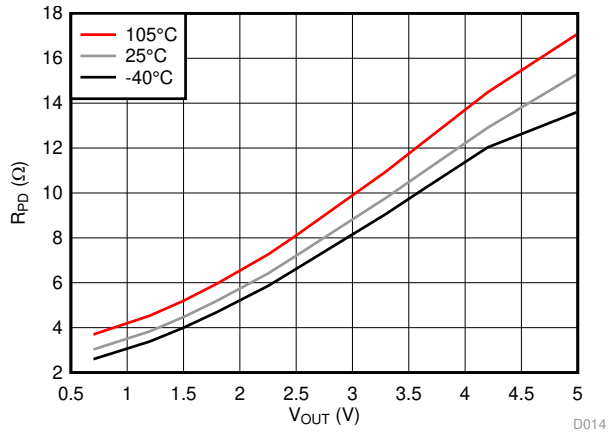
V_{BIAS} = 2.5 V V_{IN} = V_{OUT} V_{EN} = 0 V

Figure 7-16. R_{PD} vs V_{OUT}, V_{BIAS} = 2.5 V



V_{BIAS} = 3.3 V V_{IN} = V_{OUT} V_{EN} = 0 V

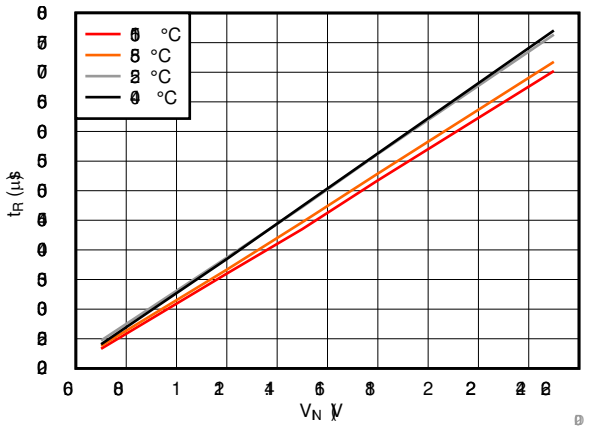
Figure 7-17. R_{PD} vs V_{OUT}, V_{BIAS} = 3.3 V



V_{BIAS} = 5 V V_{IN} = V_{OUT} V_{EN} = 0 V

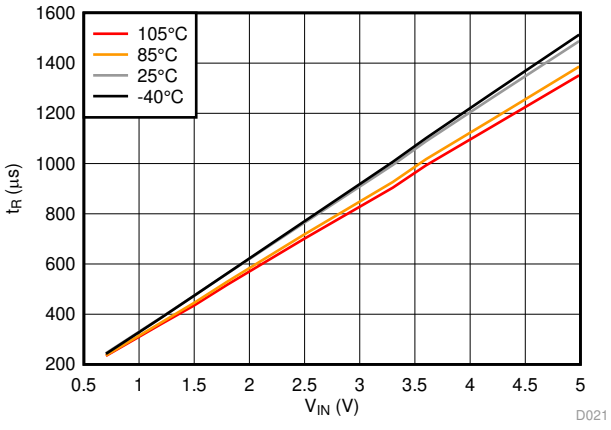
Figure 7-18. R_{PD} vs V_{OUT}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



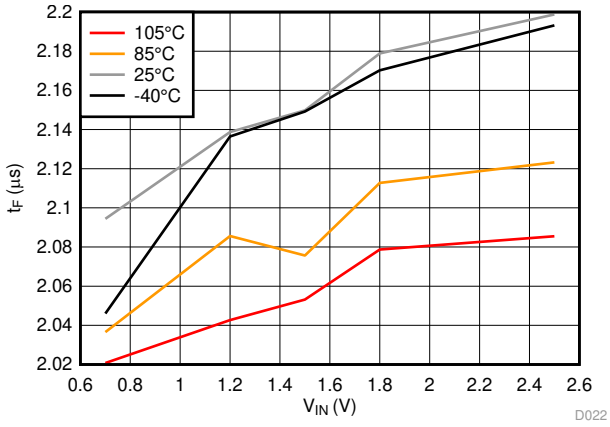
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-19. t_R vs V_{IN}, V_{BIAS} = 2.5 V



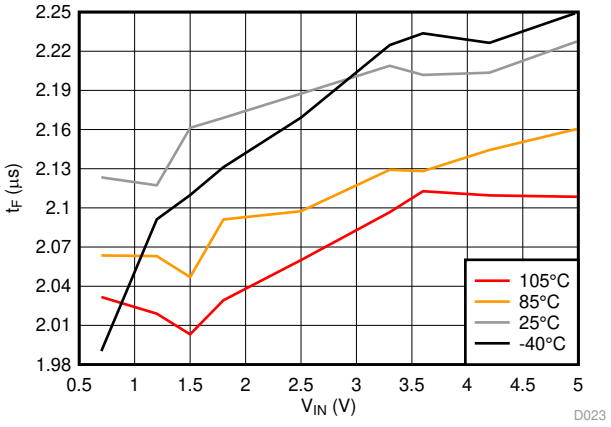
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-20. t_R vs V_{IN}, V_{BIAS} = 5 V



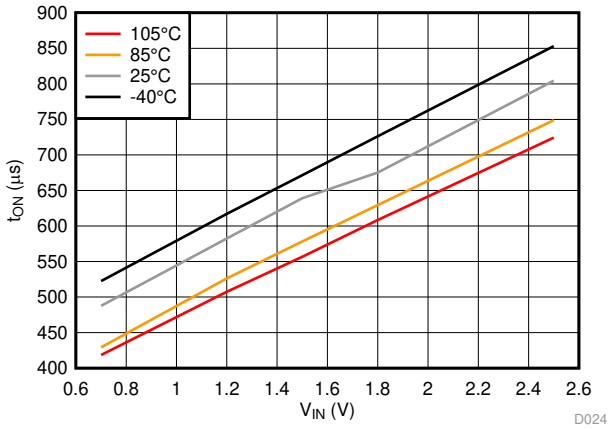
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-21. t_F vs V_{IN}, V_{BIAS} = 2.5 V



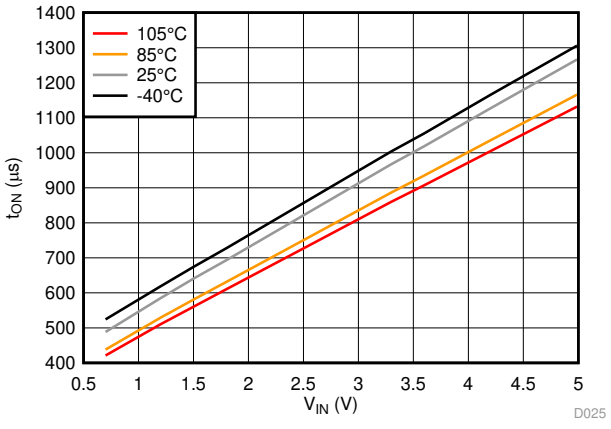
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-22. t_F vs V_{IN}, V_{BIAS} = 5 V



V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

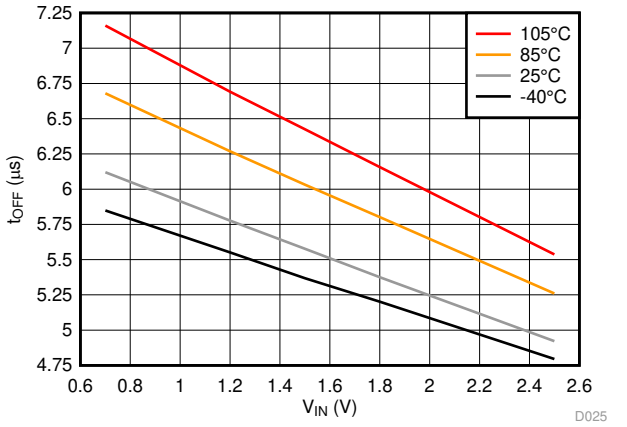
Figure 7-23. t_{ON} vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} = Low to High

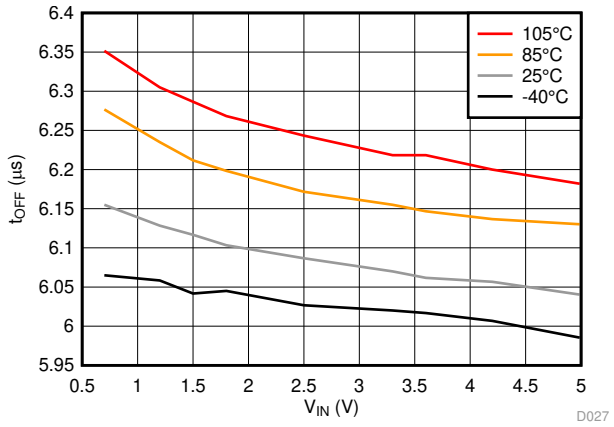
Figure 7-24. t_{ON} vs V_{IN}, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics



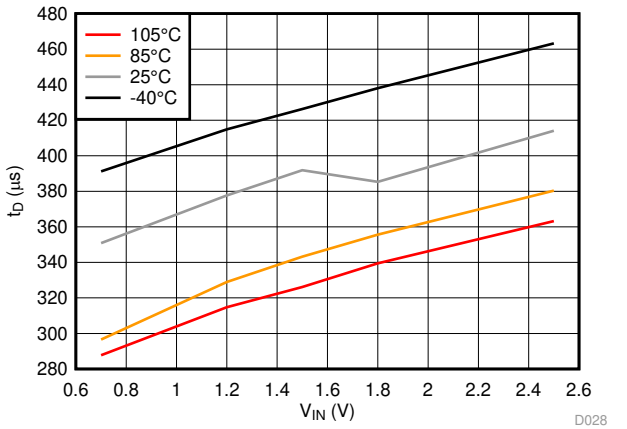
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-25. t_{OFF} vs V_{IN}, V_{BIAS} = 2.5 V



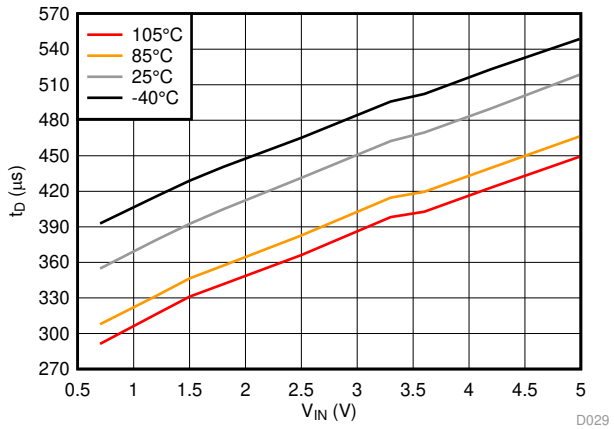
V_{BIAS} = 5 V CT = 1000 pF V_{EN} = High to Low

Figure 7-26. t_{OFF} vs V_{IN}, V_{BIAS} = 5 V



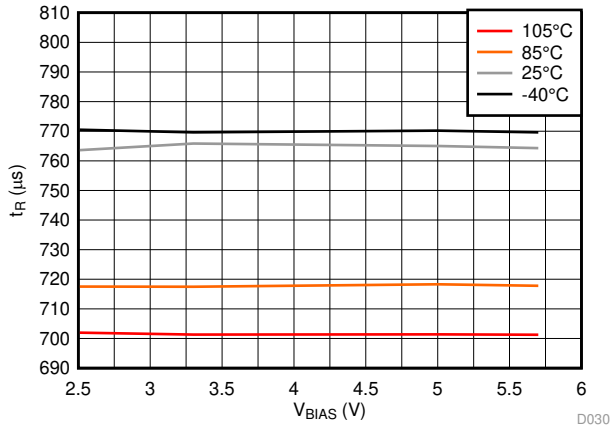
V_{BIAS} = 2.5 V CT = 1000 pF V_{EN} = Low to High

Figure 7-27. t_D vs V_{IN}, V_{BIAS} = 2.5 V



V_{BIAS} = 5 V CT = 1000 pF V_{EN} =Low to High

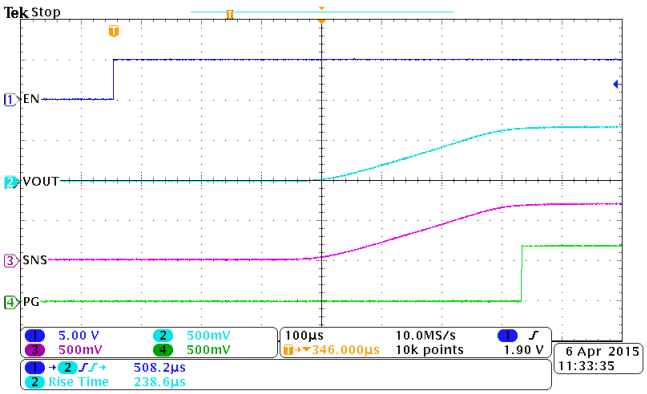
Figure 7-28. t_D vs V_{IN}, V_{BIAS}= 5 V



V_{IN} = 2.5 V CT = 1000 pF V_{EN} = Low to High

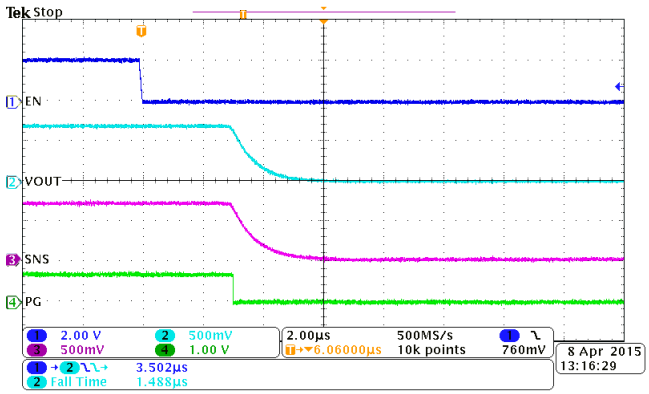
Figure 7-29. t_R vs V_{BIAS}

7.11 Typical Switching Characteristics (continued)



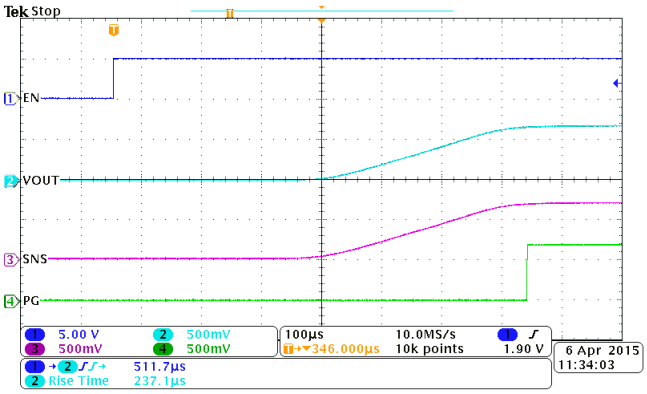
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-30. Turn-on Waveform, V_{BIAS} = 2.5 V



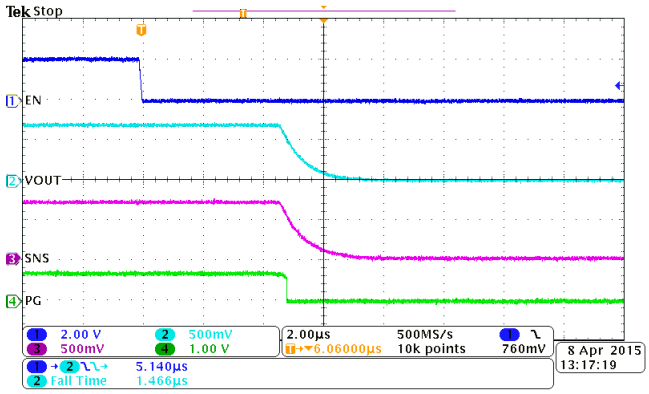
V_{IN} = 0.7 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-31. Turn-off Waveform, V_{BIAS} = 2.5 V



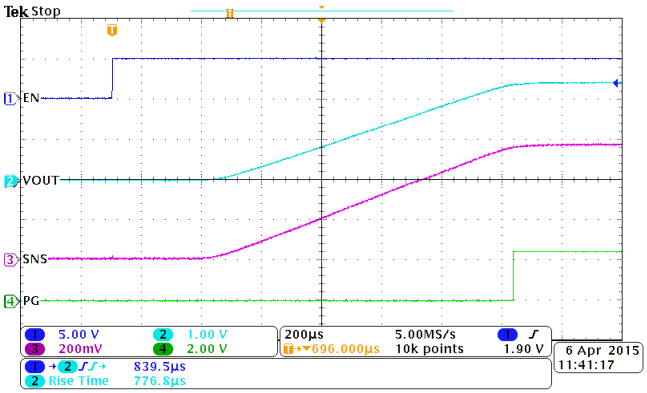
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-32. Turn-on Waveform, V_{BIAS} = 5 V



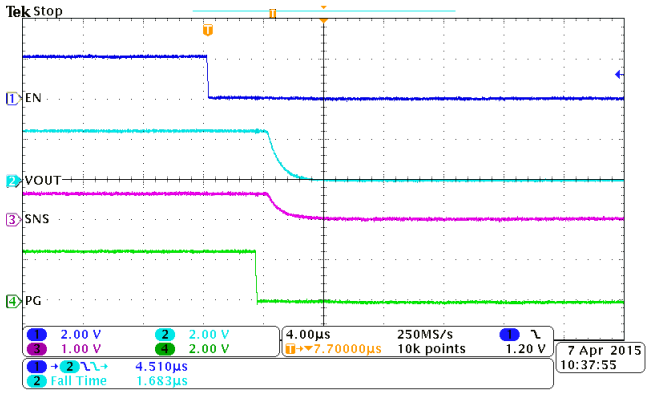
V_{IN} = 0.7 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-33. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

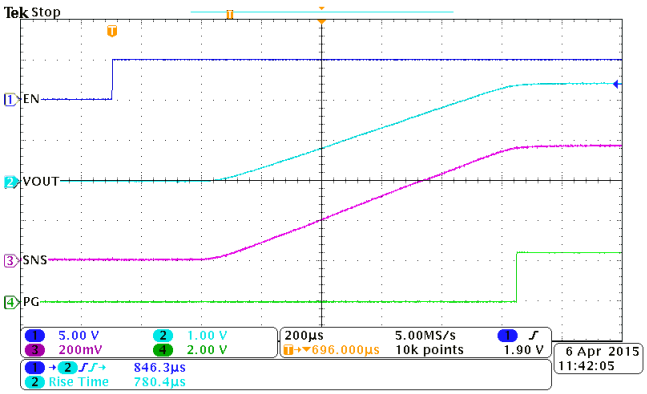
Figure 7-34. Turn-on Waveform, V_{BIAS} = 2.5 V



V_{IN} = 2.5 V V_{BIAS} = 2.5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

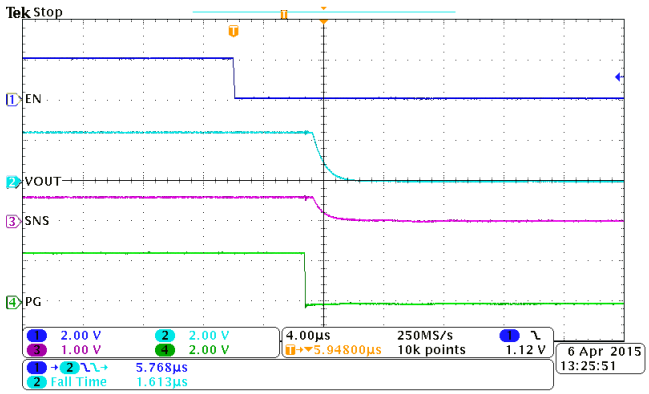
Figure 7-35. Turn-off Waveform, V_{BIAS} = 2.5 V

7.11 Typical Switching Characteristics (continued)



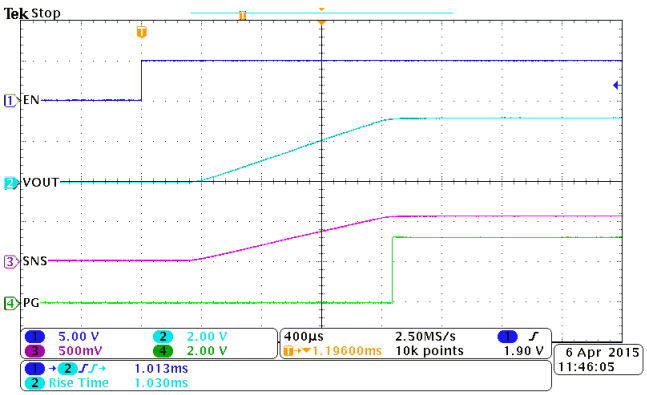
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-36. Turn-on Waveform, V_{BIAS} = 5 V



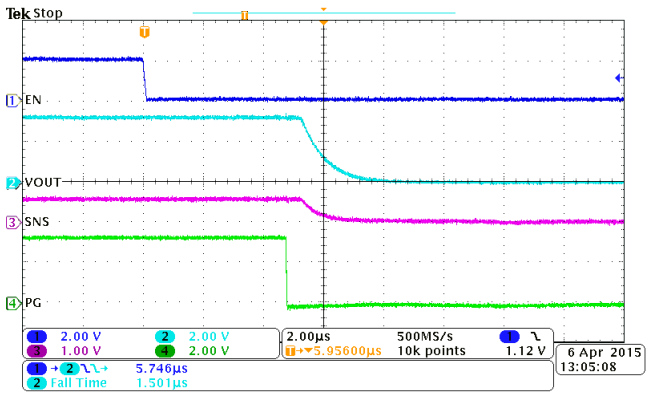
V_{IN} = 2.5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-37. Turn-off Waveform, V_{BIAS} = 5 V



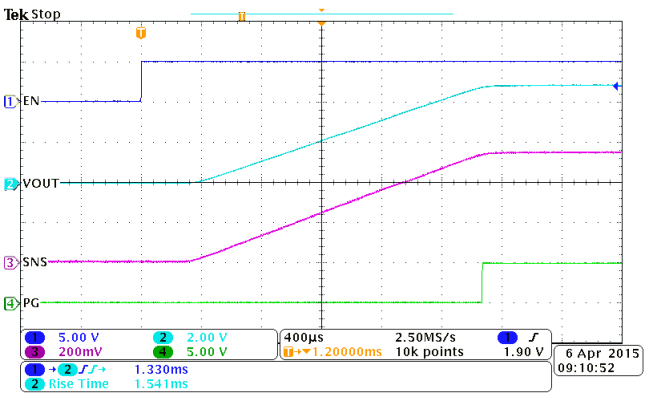
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-38. Turn-on Waveform, V_{BIAS} = 5 V



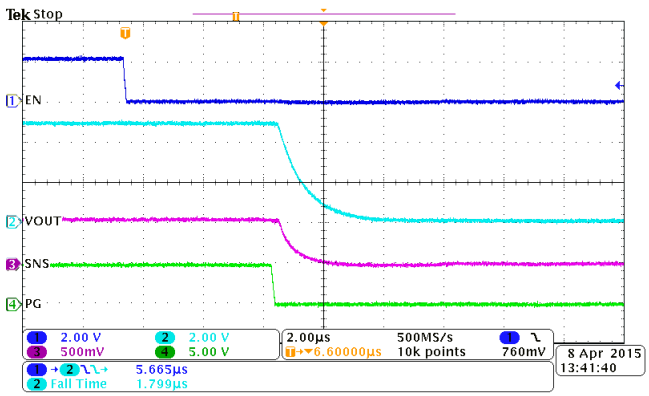
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

Figure 7-39. Turn-off Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

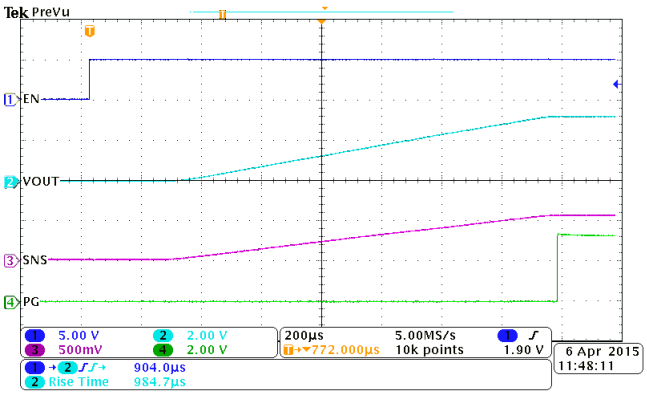
Figure 7-40. Turn-on Waveform, V_{BIAS} = 5 V



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 10 Ω

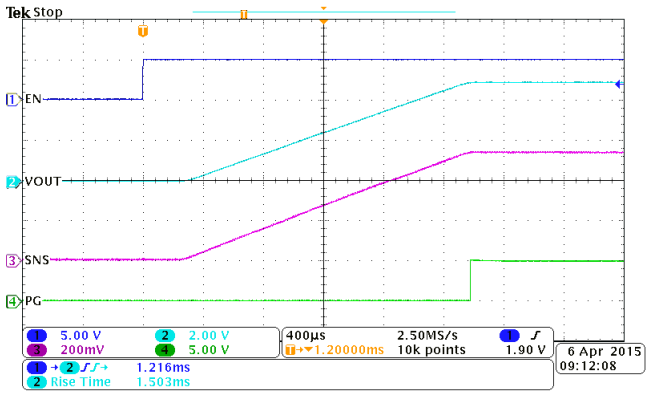
Figure 7-41. Turn-off Waveform, V_{BIAS} = 5 V

7.11 Typical Switching Characteristics (continued)



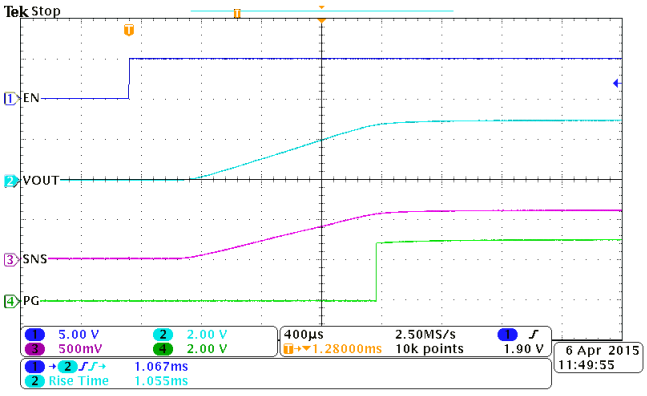
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-42. Turn-on Waveform, No Load



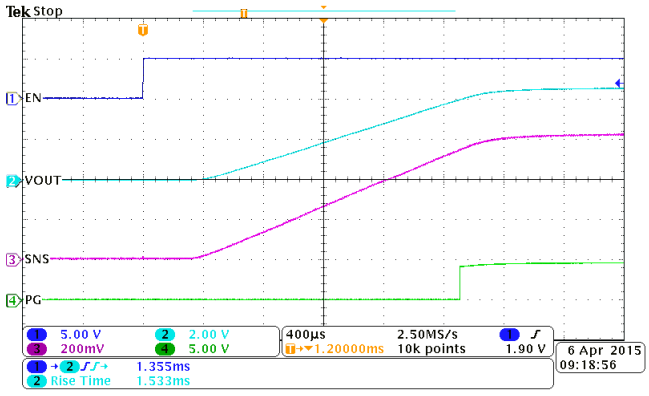
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = Open

Figure 7-43. Turn-on Waveform, No Load



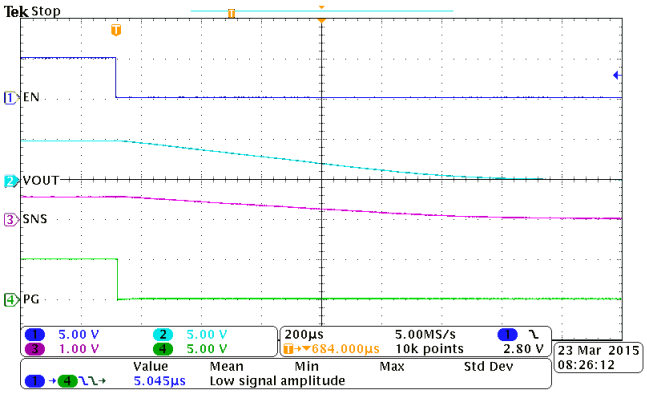
V_{IN} = 3.3 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-44. Turn-on Waveform, Heavy Load



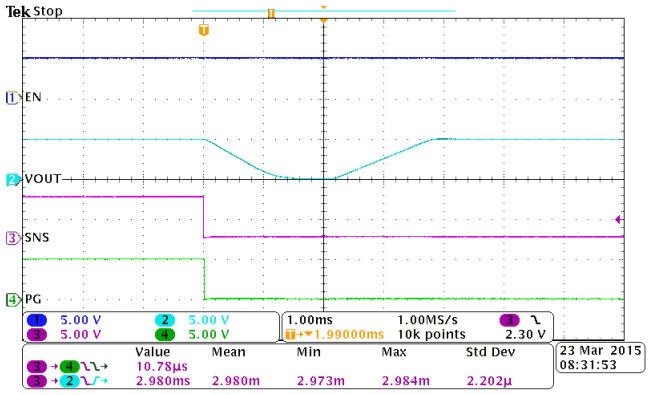
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 0.1 µF R_L = 1 Ω

Figure 7-45. Turn-on Waveform, Heavy Load



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

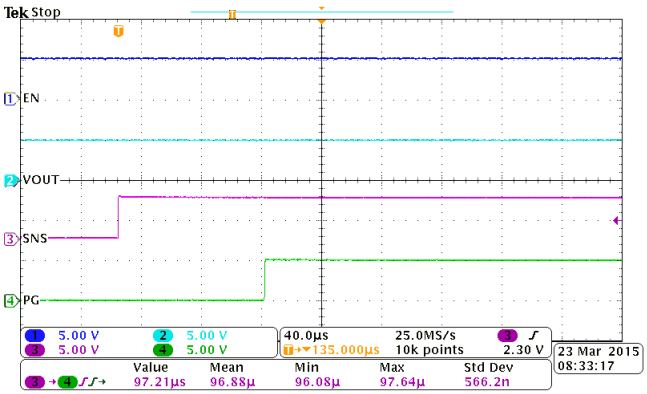
Figure 7-46. PG Response to EN Falling ($t_{DEGLITCH}$)



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

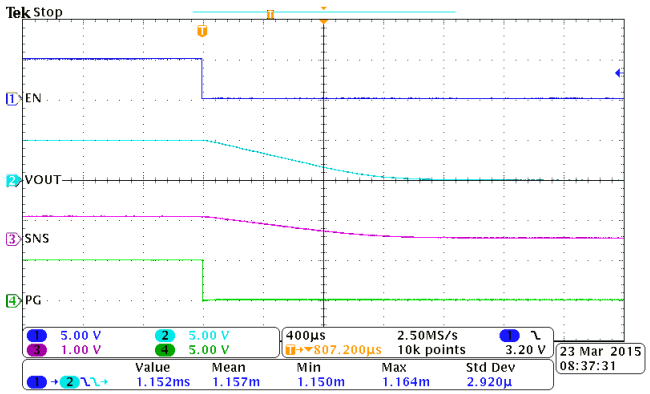
Figure 7-47. PG Response to SNS Falling With Auto-Restart ($t_{DEGLITCH}$ and $t_{RESTART}$)

7.11 Typical Switching Characteristics (continued)



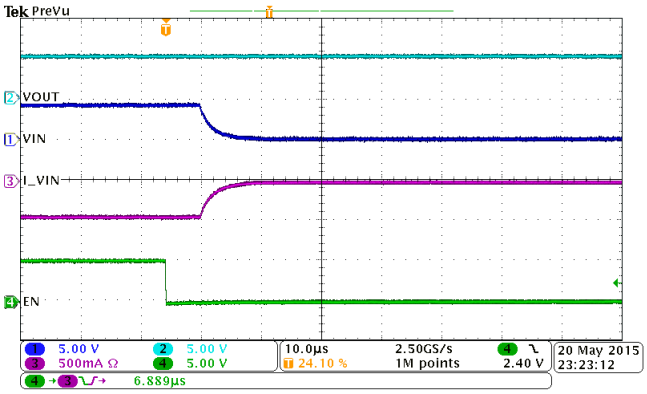
V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = 10 Ω

Figure 7-48. PG Response to SNS Rising (t_{BLANK})



V_{IN} = 5 V V_{BIAS} = 5 V CT = 1000 pF
C_{IN} = 1 µF C_L = 100 µF R_L = None

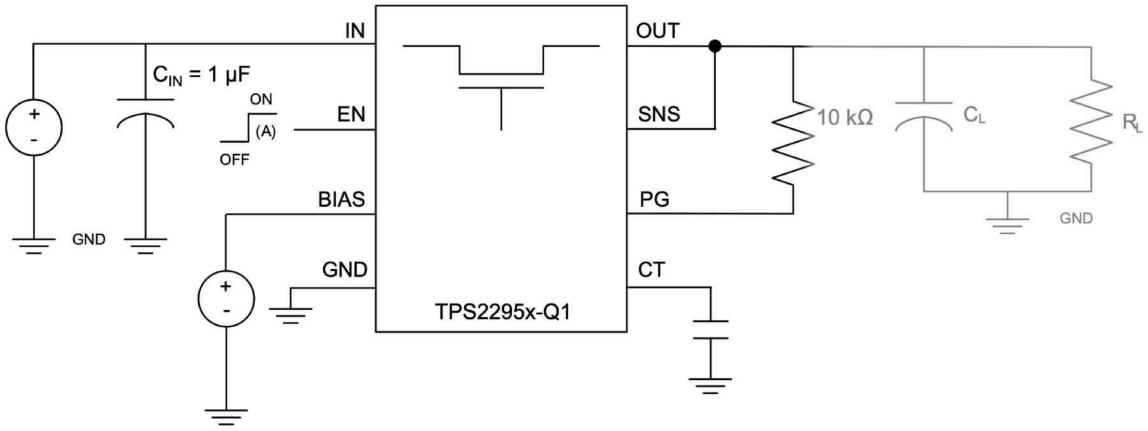
Figure 7-49. Quick Output Discharge of 100-µF Load (t_{DIS})



V_{IN} = 10 Ω to GND V_{BIAS} = 5 V
C_{IN} = 0.2 µF V_{OUT} = 5 V

Figure 7-50. Reverse Current Blocking Response Time (t_{RCB})

8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100 ns.

Figure 8-1. Timing Test Circuit

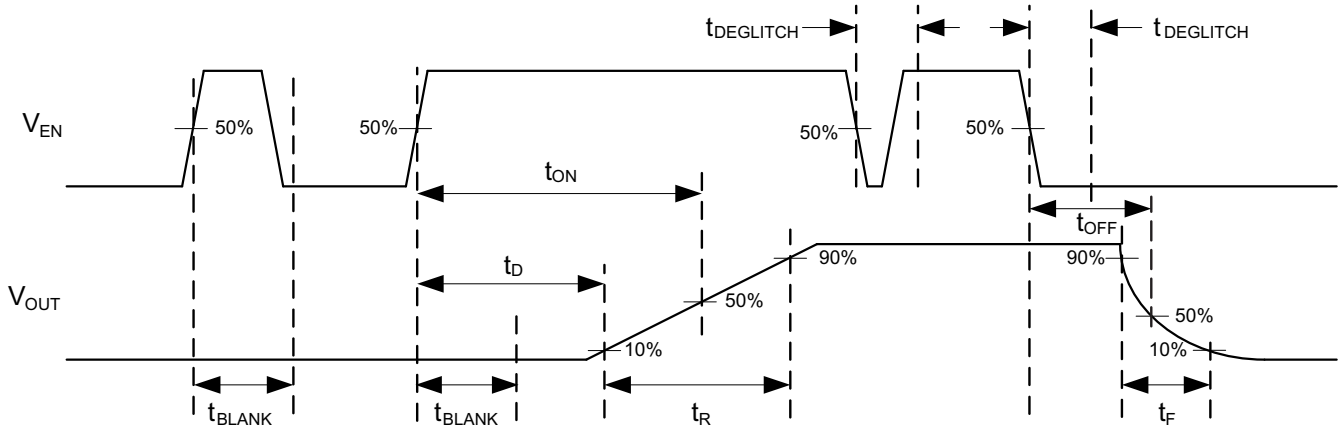


Figure 8-2. Timing Waveforms

9 Detailed Description

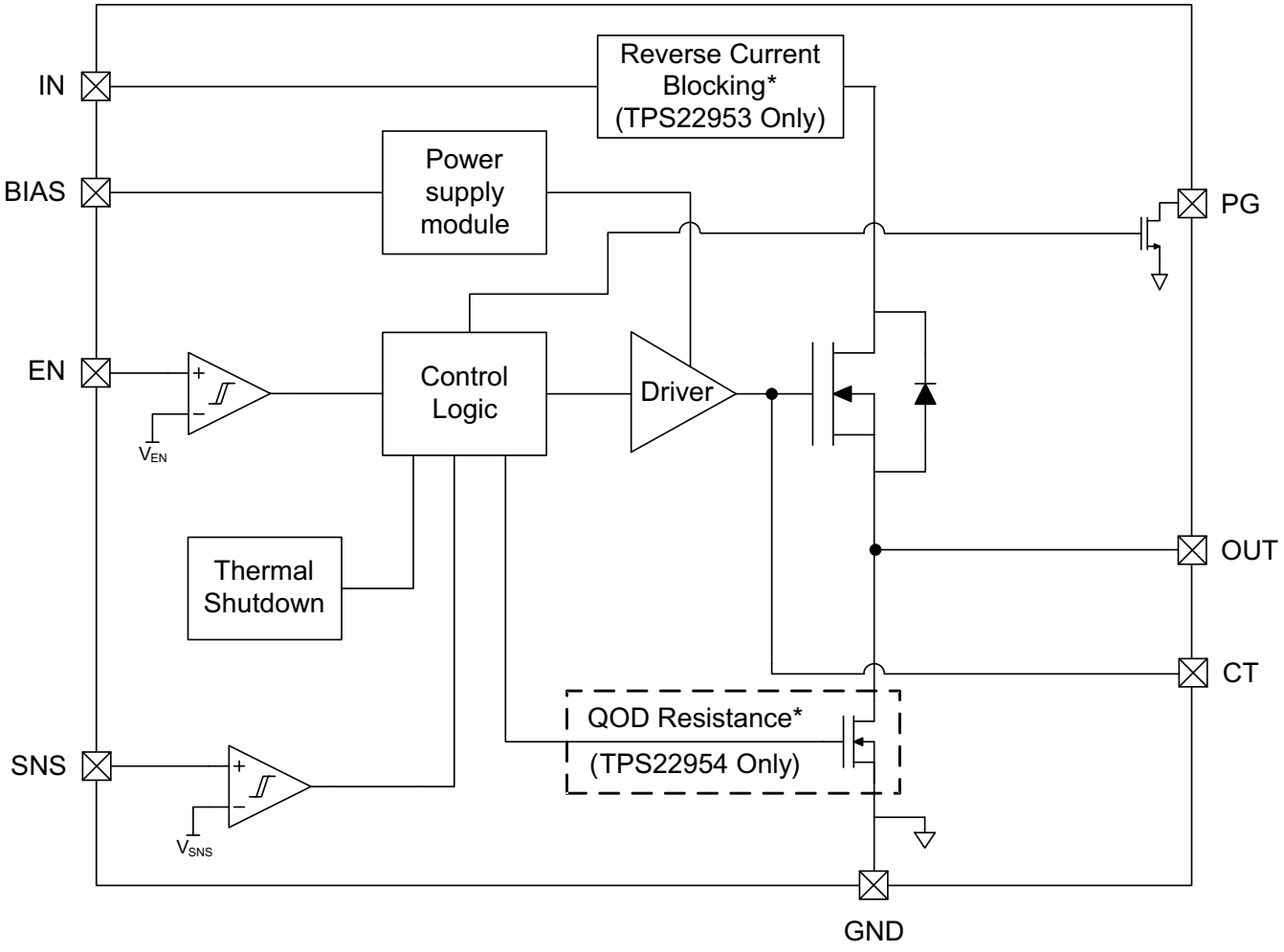
9.1 Overview

The TPS2295x-Q1 are 5.7-V, 5-A load switches in 10-pin SON packages. To reduce voltage drop for low voltage, high current rails the device implements a low-resistance N-channel MOSFET, which reduces the drop out voltage through the device at high currents. The integrated adjustable Undervoltage Lockout (UVLO) and adjustable Power Good (PG) threshold provides voltage monitoring as well as robust power sequencing.

The adjustable rise-time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on and off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15-Ω, on-chip load resistor integrates into the device for output quick discharge when the switch turns off.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated power monitoring functionality, control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



(*) Only active when the switch is disabled.

9.3 Feature Description

9.3.1 On and Off Control (EN Pin)

The EN pin controls the state of the switch. When the voltage on EN exceeds $V_{IH,EN}$ the switch enables. When EN goes below $V_{IL,EN}$ the switch disables.

The EN pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,EN}$ threshold has been exceeded. The EN pin also has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,EN}$.

The EN pin can also be configured through an external resistor divider to monitor a voltage signal for input UVLO. See Equation 1 and Figure 9-1 on how to configure the EN pin for input UVLO.

$$V_{IH,EN} = V_{IN} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \quad (1)$$

where

- $V_{IH,EN}$ is the rising threshold of the EN pin (see the *Electrical Characteristics* table)
- V_{IN} is the input voltage being monitored (this can be V_{IN}, V_{BIAS}, or an external power supply)
- R_{EN1}, R_{EN2} are the resistor divider values

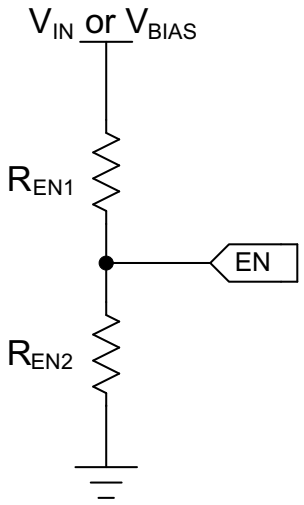


Figure 9-1. Resistor Divider (EN Pin)

9.3.2 Voltage Monitoring (SNS Pin)

The SNS pin of the device can be used to monitor the output voltage of the device or another voltage rail. The pin can be configured with an external resistor divider to set the desired trip point for the voltage being monitored or be tied to OUT directly. If the voltage on the SNS pin exceeds $V_{IH,SNS}$, the voltage being monitored on the SNS pin is considered to be valid high. The voltage on the SNS pin must be greater than $V_{IH,SNS}$ for at least t_{BLANK} before PG is asserted high. If the voltage on the SNS pin goes below $V_{IL,SNS}$, then the switch powers cycle (that is, the switch is disabled and re-enabled). For proper functionality of the device, this pin must not be left floating. If a resistor divider is not being used for voltage sensing, this pin can be tied directly to V_{OUT}.

The SNS pin has a blanking time of t_{BLANK} on the rising edge after the $V_{IH,SNS}$ threshold has been exceeded. The SNS pin has a de-glitch time of $t_{DEGLITCH}$ when the voltage has gone below $V_{IL,SNS}$.

See Equation 2 and Figure 9-2 on how to configure the SNS pin for voltage monitoring.

$$V_{IH,SNS} = V_{OUT} \times \frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}} \tag{2}$$

where

- $V_{IH,SNS}$ is the the rising threshold of the SNS pin (see *Electrical Characteristics* table)
- V_{OUT} is the voltage on the OUTpin
- R_{SNS1}, R_{SNS2} are the resistor divider values

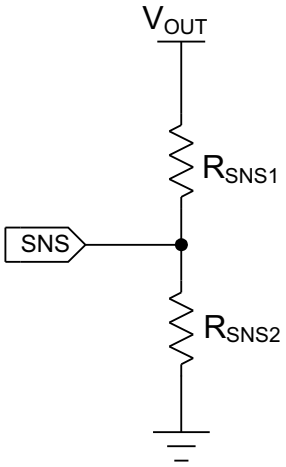


Figure 9-2. Voltage Divdier (SNS Pin)

9.3.3 Power Good (PG Pin)

The PG pin is only asserted high when the voltage on EN exceeds $V_{IH,EN}$ and the voltage on SNS exceeds $V_{IH,SNS}$. There is a t_{BLANK} time, typically 100 µs, between the SNS voltage exceeding $V_{IH,SNS}$ and PG being asserted high. If the voltage on EN goes below $V_{IL,EN}$ or the voltage on SNS goes below $V_{IL,SNS}$, PG is de-asserted. There is a $t_{DEGLITCH}$ time, typically 5 µs, between the EN voltage or SNS voltage going below their respective V_{IL} levels and PG being pulled low.

PG is an open drain pin and must be pulled up with a pullup resistor. Be sure to never exceed the maximum operating voltage on this pin. If PG is not being used in the application, tie it to GND for proper device functionality.

For proper PG operation, the BIAS voltage must be within the recommended operating range. In systems that are very sensitive to noise or have long PG traces, TI recommends to add a small capacitance from PG to GND for decoupling.

9.3.4 Supervisor Fault Detection and Automatic Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$. In the case, the SNS pin is being used to monitor V_{OUT} or a downstream voltage. The restart helps to protect against excessive overcurrent if there is a quick short to GND. See Figure 9-3.

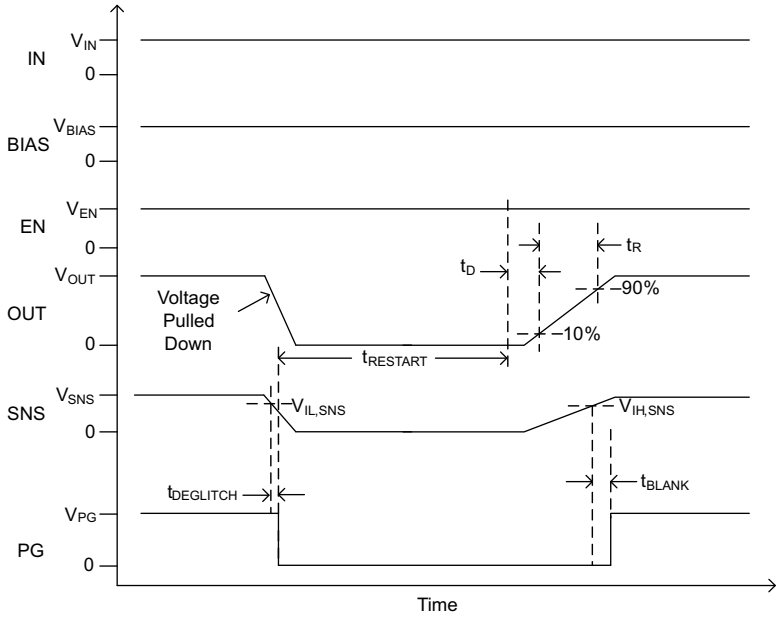


Figure 9-3. Automatic Restart After Quick Short to GND

9.3.5 Manual Restart

The falling edge of the SNS pin below $V_{IL,SNS}$ is considered a fault case and causes the load switch to be disabled for $t_{RESTART}$ (typically 2 ms). The SNS pin can be driven by an MCU to manually reset the load switch. After the $t_{RESTART}$ time, the switch is automatically re-enabled as long as EN is still above $V_{IH,EN}$, even is SNS is held low. The PG pin stays low until the switch is re-enabled and the SNS pin rises above $V_{IH,SNS}$. See Figure 9-4.

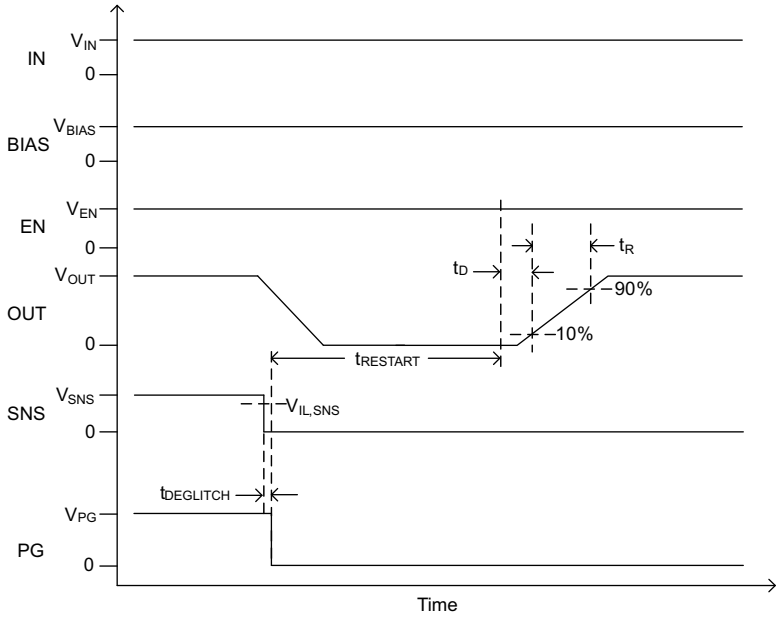


Figure 9-4. Manual Restart (SNS Held Low)

If the SNS pin is brought above $V_{IH,SNS}$ within the $t_{RESTART}$ time, the switch still waits to re-enable. The PG pin also stays low until t_{BLANK} after switch is re-enabled. In this case, PG indicates when the switch is enabled and capable of being reset again. See Figure 9-5.

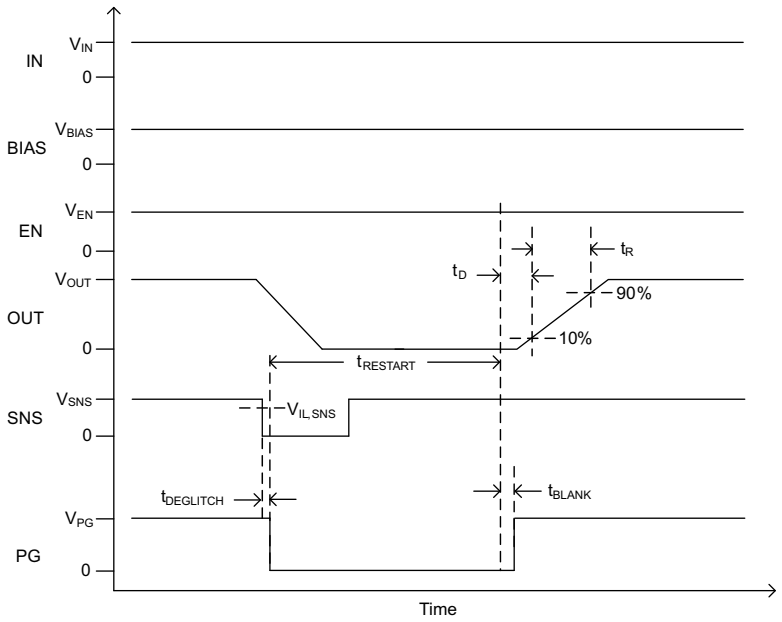


Figure 9-5. Manual Restart (SNS Toggled Low to High)

9.3.6 Thermal Shutdown

If the junction temperature of the device exceeds T_{SD}, the switch disables. The device enables after the junction temperature drops by TSD_{HYS} as long as EN is still greater than $V_{IH,EN}$.

9.3.7 Reverse Current Blocking (TPS22953-Q1 Only)

When the switch disables (either by de-asserting EN or SNS, triggering thermal shutdown, or losing power), the reverse current blocking (RCB) feature of the device engages within t_{RCB}, typically 10 µs. After the RCB engages, the reverse current from the OUT pin to the IN pin is limited to $I_{RCB,IN}$, typically 0.01 µA.

9.3.8 Quick Output Discharge (QOD) (TPS22954-Q1 Only)

The Quick Output Discharge (QOD) transistor is engaged indefinitely whenever the switch is disabled and the recommended V_{BIAS} voltage is met. During this state, the QOD resistance (R_{PD}) discharges V_{OUT} to GND. TI does not recommend to apply a continuous DC voltage to OUT when the device is disabled.

The QOD transistor can remain active for a short period of time even after V_{BIAS} loses power. This brief period of time is defined as t_{DIS}. For best results, TI recommends the device get disabled before V_{BIAS} goes below the minimum recommended voltage. The waveform in Figure 9-6 shows the behavior when power is applied and then removed in a typical application.

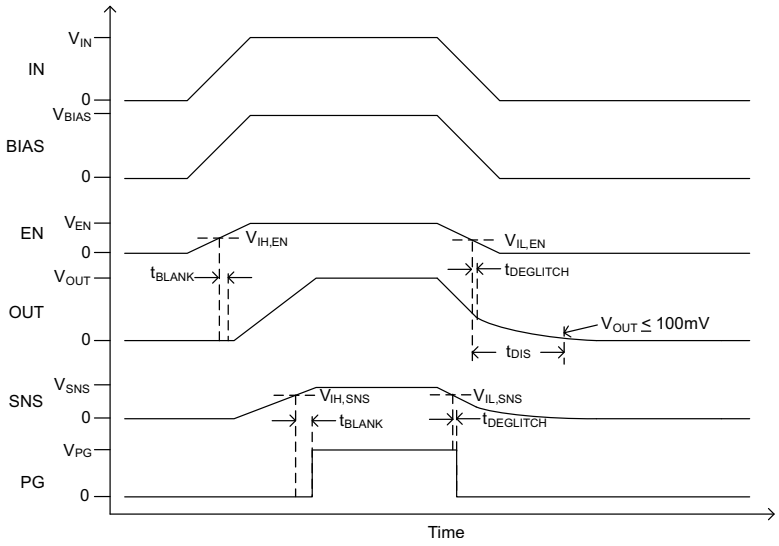


Figure 9-6. Power Applied and Then Removed in a Typical Application

At the end of the t_{DIS} time, it is not assured that V_{OUT} is 0 V because the final voltage is dependent upon the initial voltage and the C_L capacitor. The final V_{OUT} can be calculated with Equation 3 for a given initial voltage and C_L capacitor.

$$V_f = V_o \times e^{\frac{-t}{RC}} \tag{3}$$

where

- V_f is the final V_{OUT} voltage
- V_o is the initial V_{OUT} voltage
- R is the the value of the output discharge resistor, R_{PD} (see the *Electrical Characteristics* table)
- C is the output bulk capacitance on OUT

9.3.9 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics* table. See Figure 9-7 for an example of a typical

device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

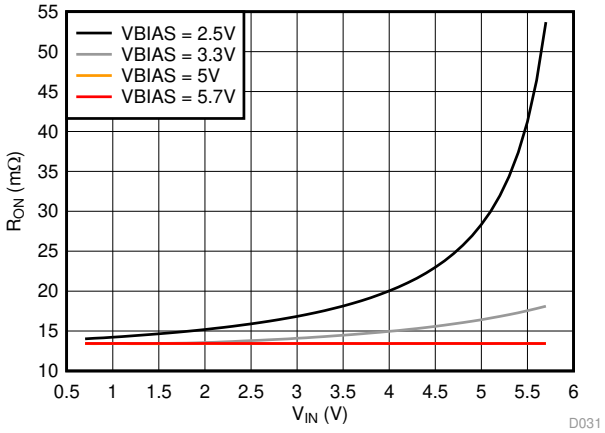


Figure 9-7. R_{ON} When V_{IN} > V_{BIAS}

9.3.10 Adjustable Rise Time (CT Pin)

A capacitor to GND on the CT pin sets the slew rate for V_{OUT}. An appropriate capacitance value must be placed on CT such that the I_{MAX} and I_{PLS} specifications of the device are not violated. The capacitor to GND on the CT pin must be rated for 25 V or higher. Equation 4 shows an approximate formula for the relationship between CT (except for CT = open) and the slew rate for any V_{BIAS}.

$$SR = 0.35 \times CT + 20 \quad (4)$$

where

- SR is the slew rate (in µs/V).
- CT is the capacitance value on the CT terminal (in pF).
- The units for the constant 20 are µs/V.
- The units for the constant 0.35 are µs/(V*pF).

Rise time can be calculated by multiplying the input voltage (typically 10% to 90%) by the slew rate. Table 9-1 contains rise time values measured on a typical device.

Table 9-1. Rise Time

CTx (pF)	RISE TIME (µs) 10% – 90%, C_L = 0.1 µF, V_{BIAS} = 2.5 V to 5.7 V, R_L = 10-Ω LOAD. TYPICAL VALUES AT 25°C, 25-V X7R 10% CERAMIC CAP					
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	0.7 V
Open	140	98	62	54	46	32
220	444	301	175	150	124	81
470	767	518	299	255	210	133
1000	1492	994	562	474	387	245
2200	3105	2050	1151	961	787	490
4700	6420	4246	2365	1980	1612	998
10000	14059	9339	5183	4331	3533	2197

9.3.11 Power Sequencing

The TPS2295x-Q1 operates regardless of power-on and power-off sequencing order. The order in which voltages are applied to IN, BIAS, and EN does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions. If voltage is applied to EN before IN and BIAS, the slew rate of VOUT is not controlled. Also, turning off IN or BIAS while EN is high does not damage the device.

9.4 Device Functional Modes

Table 9-2 describes what the OUT pin is connected to for a particular device as determined by the EN pin.

Table 9-2. Function Table

EN	TPS22953-Q1	TPS22954-Q1
L	OPEN	R_{PD} to GND
H	IN	IN

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available on www.ti.com for further aid.

10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics* table of this data sheet. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} voltage conditions, use Equation 5 to calculate the input to output voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{5}$$

where

- ΔV is the voltage drop from IN to OUT
- I_{LOAD} is the load current
- R_{ON} is the On-Resistance of the device for a specific V_{IN} and V_{BIAS}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 Thermal Considerations

The maximum IC junction temperature must be restricted to just under the thermal shutdown (T_{SD}) limit of the device. Use Equation 6 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{6}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.
- $T_{J(max)}$ is the maximum allowable junction temperature before hitting thermal shutdown (see the *Electrical Characteristics* table).
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

10.1.3 Automatic Power Sequencing

The PG pin of the TPS2295x-Q1 allows for automatic sequencing of multiple system rails or loads. The accurate SNS voltage monitoring ensures the first rail is up before the next starts to turn on. This approach provides robust system sequencing and reduces the total inrush current by preventing overlap. Figure 10-1 shows how two rails can be sequenced. There is no limit to the number of rails that can be sequenced in this way.

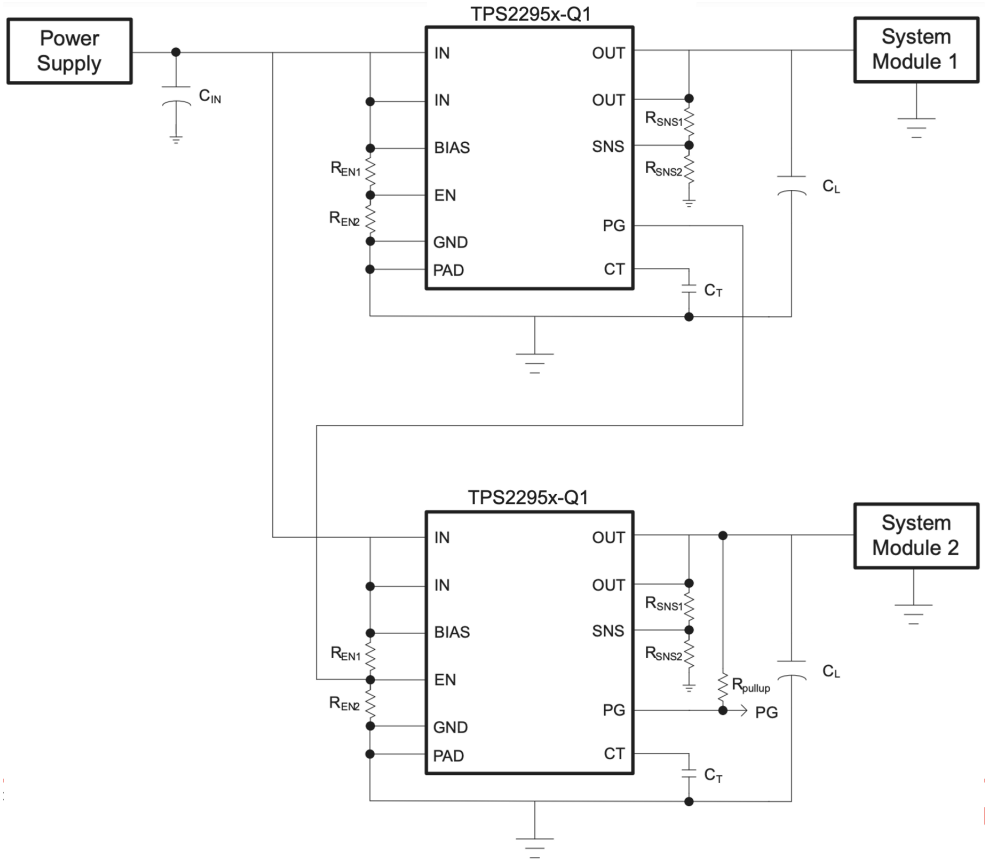


Figure 10-1. Power Sequencing with PG Control Schematic

10.1.4 Monitoring a Downstream Voltage

The SNS pin can be used to monitor other system voltages in addition to V_{OUT}. The status of the monitored voltage are indicated by the PG pin which can be pulled up to V_{OUT} or another voltage. Figure 10-2 shows an example of the TPS2295x-Q1 monitoring the output of a downstream DC/DC regulator. In this case, the switch turns on when the power supply is above the UVLO, but the PG is not asserted until the DC/DC regulator has started up.

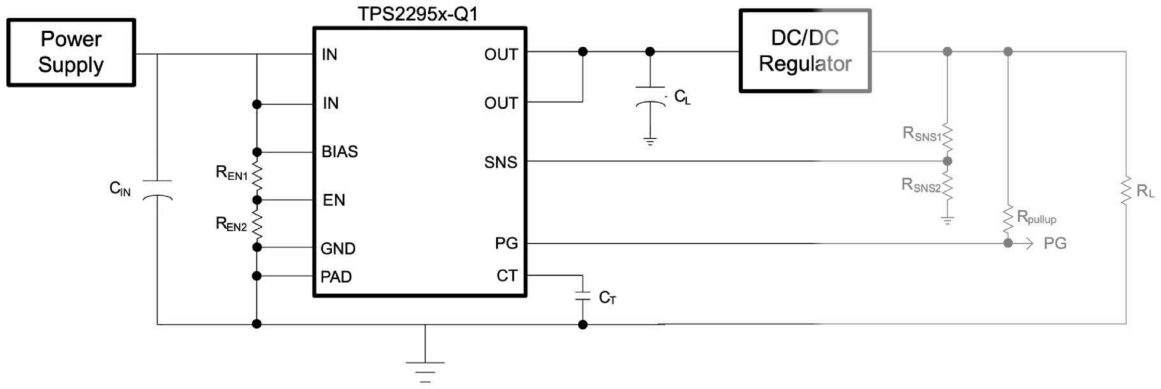


Figure 10-2. Monitoring a Downstream Voltage Schematic

In this application, if the DC/DC Regulator is shut down, the supervisor registers this as a fault case and resets the load switch.

10.1.5 Monitoring the Input Voltage

The SNS pin can also be used to monitor V_{IN} in the case a MCU GPIO is being used to control the EN. This event allows PG to report on the status of the input voltage when the switch is enabled. See Figure 10-3.

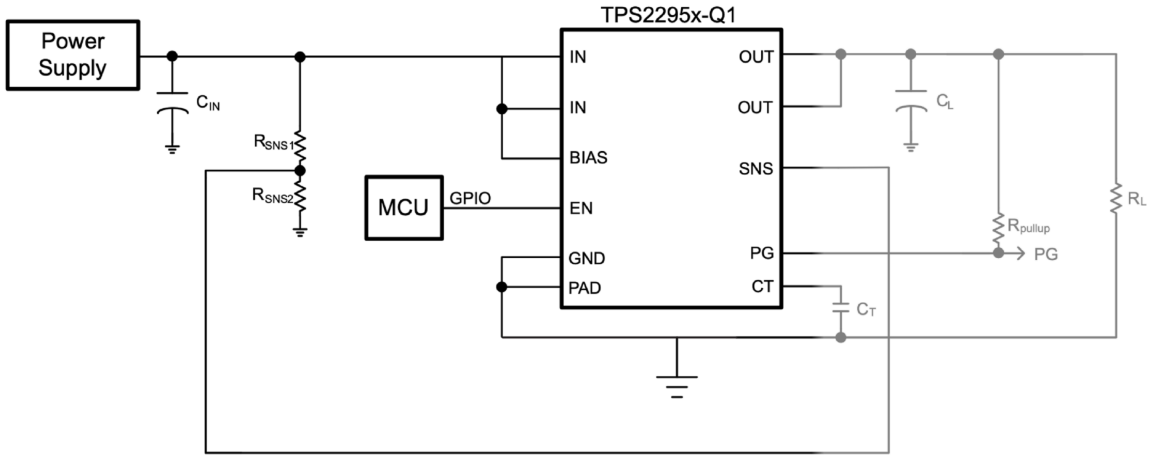


Figure 10-3. Monitoring the Input Voltage Schematic

10.1.6 Break-Before-Make Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement break-before-make logic. The circuit in Figure 10-4 shows how the detection of power supply 1 can be used to disable the load switch for power supply 2. By tying the SNS of Load Switch 1 directly to the input, its PG pin is pulled up as soon as the device is enabled.

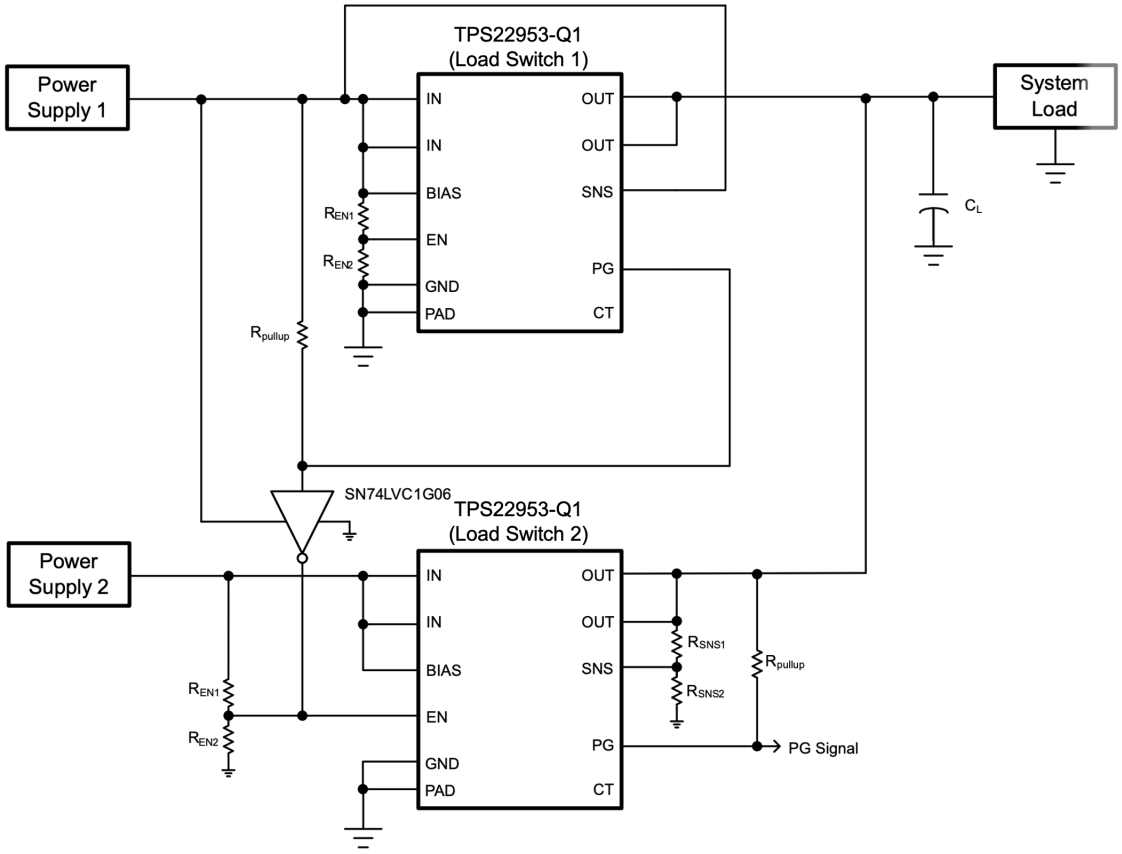


Figure 10-4. Break-Before-Make Power MUX Schematic

The break-before-make logic ensures that power supply 2 is completely disconnected before power supply 1 is connected. This approach provides very robust reverse current blocking. However, in most cases, this aproach also results in a dip in the output voltage when switching between supplies.

The amount of voltage dip depends on the loading, the output capacitance, and the turn-on delay of the load switch. In this application, leaving the CT pin open results in the shortest turn-on delay and minimizes the output voltage dip.

Table 10-1 summarizes the logic of the PG Signal for Figure 10-4.

Table 10-1. Break-Before-Make PG Signal

PG Signal	Indication
H	Power supply 1 not present. System powered from power supply 2.
L	Power supply 1 present. System powered from power supply 1.

10.1.7 Make-Before-Break Power MUX (TPS22953-Q1 Only)

The reverse current blocking feature of the TPS22953-Q1 makes it suitable for power multiplexing (MUXing) between two power supplies with different voltages. The SNS and PG pin can be configured to implement make-before-break logic. The circuit in Figure 10-5 shows how the detection of Load Switch 1 turning on can be used to disable the load switch for power supply 2. By tying SNS to the Load, the PG is pulled up when the output voltage starts to rise. This event disables an active low load switch such as the TPS22910A.

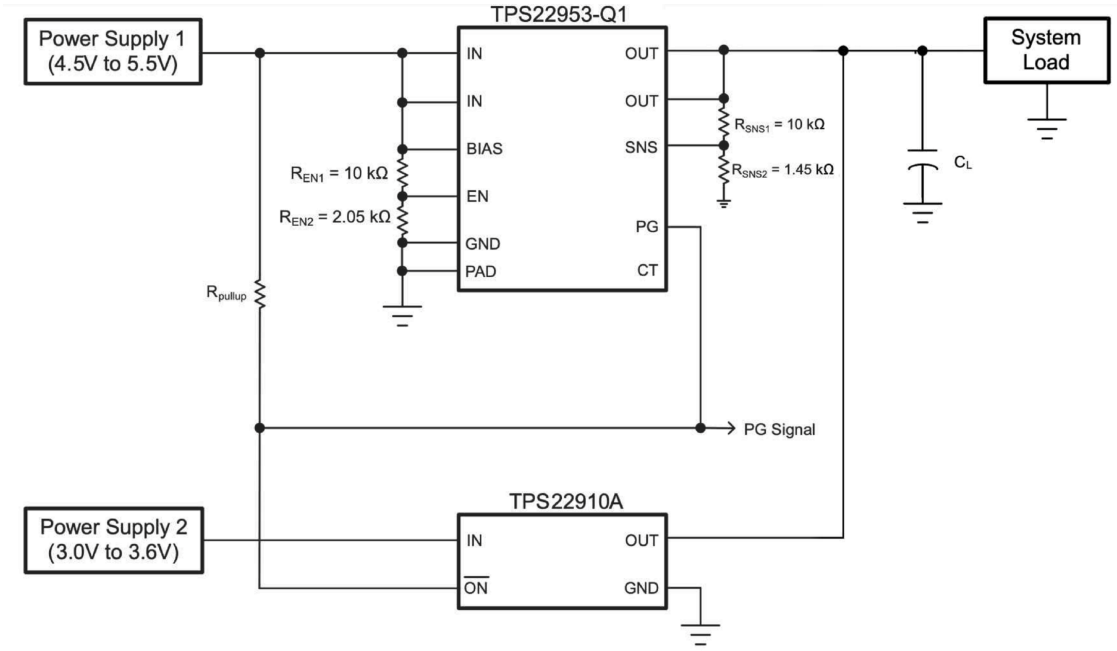


Figure 10-5. Make-Before-Break Power MUX Schematic

The make-before-break logic ensures that power supply 2 is not disconnected until power supply 1 is connected. Unlike break-before-make logic, this approach is ideal for preventing voltage dip on the output when switching between supplies. However, in most cases, this approach also results in temporary reverse current flow.

The TPS22910A is well suited for this application because it can detect and block reverse current even before it is disabled by the TPS22953-Q1 PG signal. Also, the active low enable of the TPS22910A eliminates the need for an inverter as shown in the previous example.

To ensure correct logic, the SNS pin must be configured to toggle PG when the load voltage is between the two supply voltages (3.6 V to 4.5 V). The SNS resistor values in Figure 10-5 are assuming a tolerance of ±1% or better.

Table 10-2 summarizes the logic of the PG Signal for Figure 10-5.

Table 10-2. Make-Before-Break PG Signal

PG Signal	Indication
H	Power supply 1 present. System powered from power supply 1.
L	Power supply 1 not present. System powered from power supply 2.

10.2 Typical Application

This application demonstrates how the TPS2295x-Q1 can be used to limit inrush current to output capacitance.

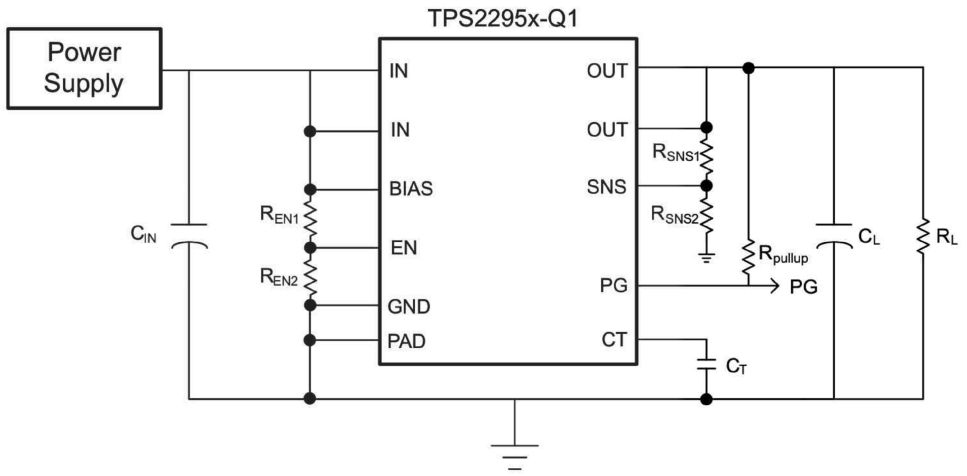


Figure 10-6. Powering a Downstream Module Schematic

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-3.

Table 10-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	47 µF
Maximum acceptable inrush current	150 mA
R_L	None

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- Input voltage
- BIAS voltage
- Load current
- Load capacitance
- Maximum acceptable inrush current

10.2.2.1 Inrush Current

Use Equation 7 to determine how much inrush current is caused by the C_L capacitor.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \tag{7}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the load capacitance on V_{OUT}
- dt is the V_{OUT} rise time (typically 10% to 90%)
- dV_{OUT} is the change in V_{OUT} Voltage (typically 10% to 90%)

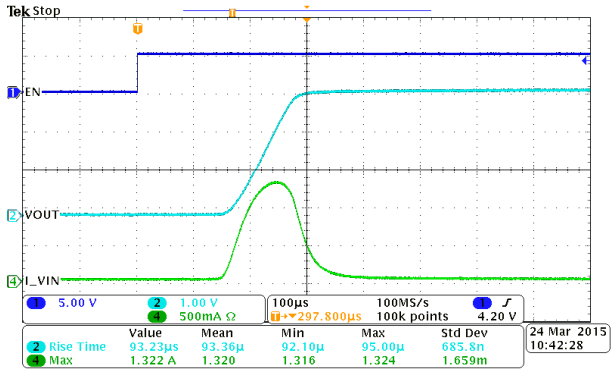
In this case, a Slew Rate slower than 314 µs/V is required to meet the maximum acceptable inrush requirement. Equation 4 can be used to estimate the CT capacitance (as shown in Equation 8 and Equation 9) required for this slew rate.

$$314\ \mu s/V = 0.35 \times CT + 20 \quad (8)$$

$$CT = 840\ pF \quad (9)$$

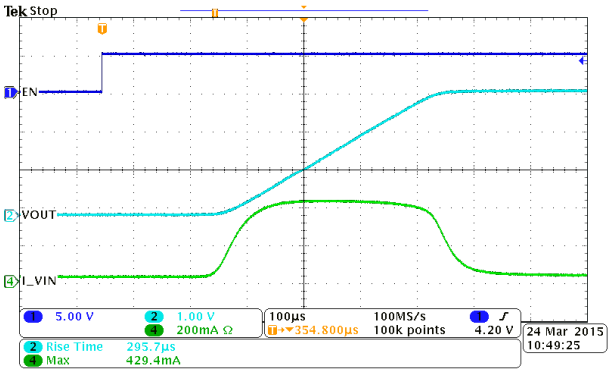
10.2.3 Application Curves

The following Application Curves show the inrush with multiple different CT values. These curves show only a CT capacitance greater than 840 pF results in the acceptable inrush current of 150 mA.



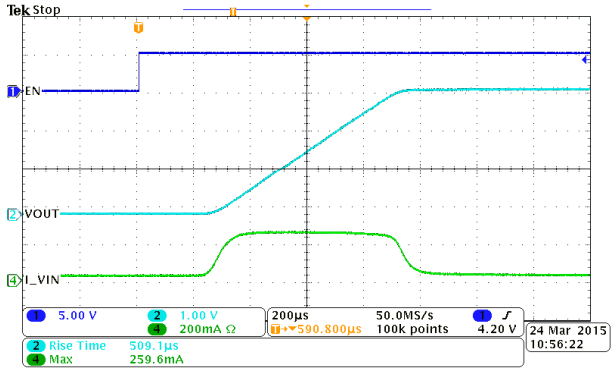
CT = 0 pF

Figure 10-7. Inrush with CT = 0 pF



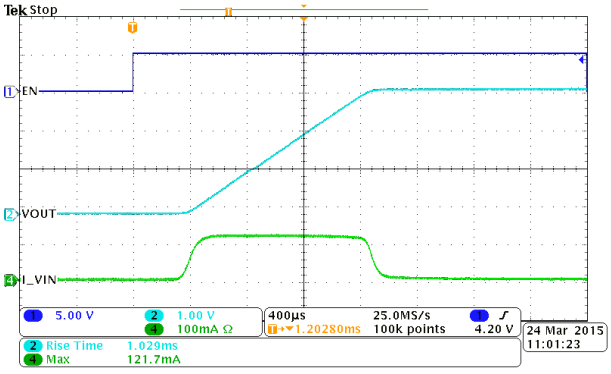
CT = 220 pF

Figure 10-8. Inrush with CT = 220 pF



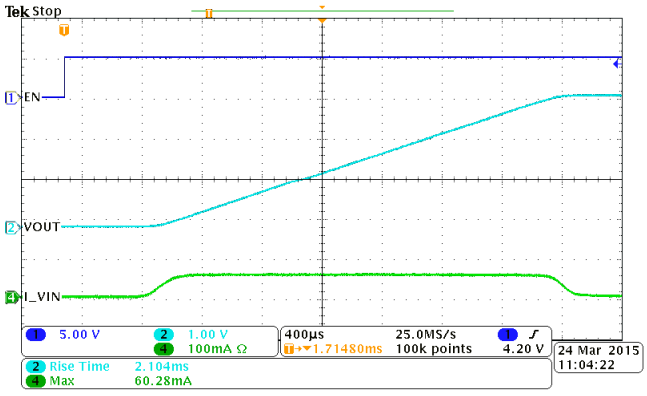
CT = 470 pF

Figure 10-9. Inrush with CT = 470 pF



CT = 1000 pF

Figure 10-10. Inrush with CT = 1000 pF



CT = 2200 pF

Figure 10-11. Inrush with CT = 2200 pF

11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.7 V and a V_{IN} range of 0.7 V to 5.7 V. The power supply must be well regulated and placed as close to the device terminals as possible. The power supply must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This action causes the load switch to turn on more slowly. Not only does this event reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

12 Layout

12.1 Layout Guidelines

- Input and Output traces must be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The CT Capacitor must be placed as close as possible to the device to minimize parasitic trace capacitance. TI recommends to cutout copper on other layers directly below CT to minimize parasitic capacitance.
- The IN terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The OUT terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The BIAS terminal must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric.

12.2 Layout Example

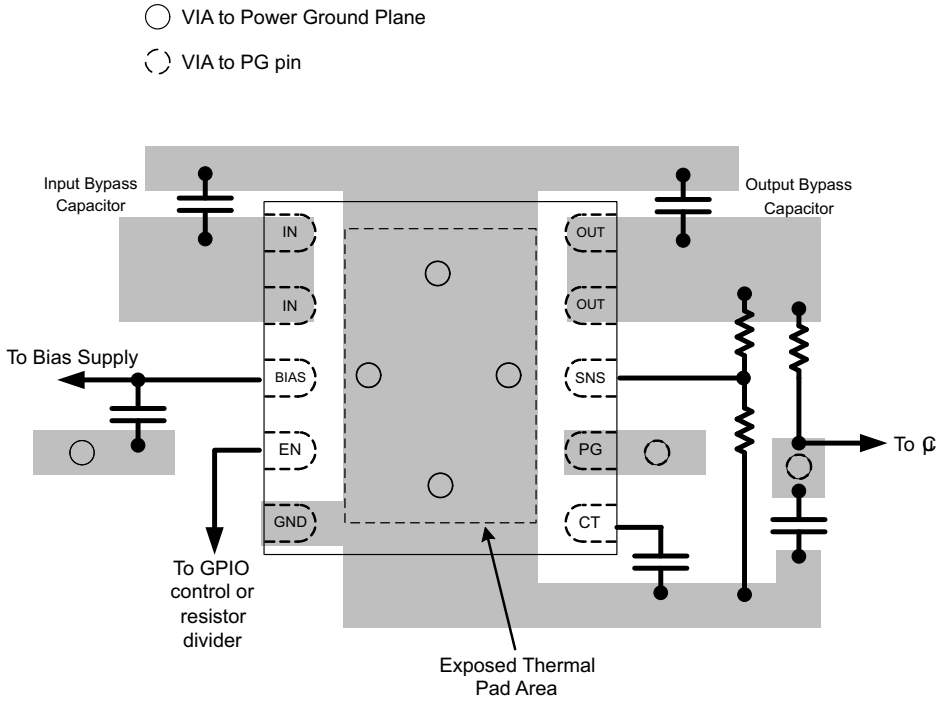


Figure 12-1. Recommended Board Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS22953/54 5.7-V, 5-A, 14-mΩ On-Resistance Load Switch* user's guide
- Texas Instruments, *Basics of Load Switches* application note
- Texas Instruments, *Managing Inrush Current* application note
- Texas Instruments, *Reverse Current Protection in Load Switches* application note
- Texas Instruments, *Quiescent Current vs Shutdown Current for Load Switch Power Consumption* application note
- Texas Instruments, *Load Switch Thermal Considerations* application note

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22953QDQCRQ1	ACTIVE	WSON	DQC	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS22954QDQCRQ1	ACTIVE	WSON	DQC	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS22953QDQCRQ1	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	953Q1	Samples
TPS22954QDQCRQ1	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	954Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22953-Q1, TPS22954-Q1 :

- Catalog : TPS22953, TPS22954

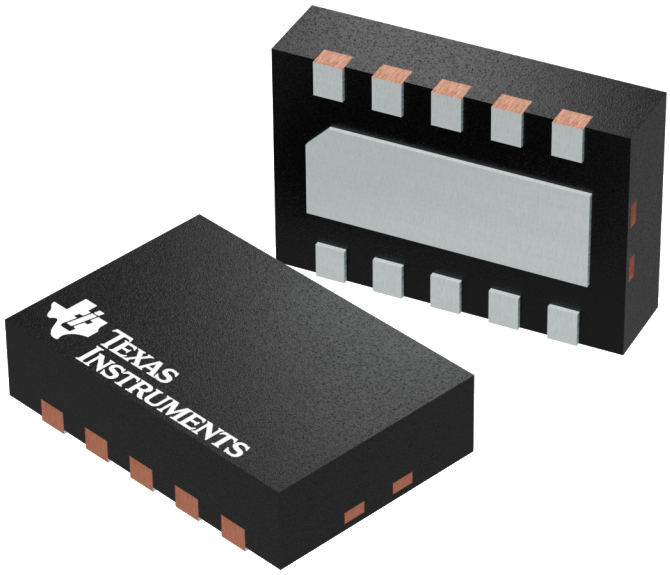
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4209674/B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPS25981x 2.7 V – 16 V, 10-A, 6-mΩ eFuse with Transient Overcurrent Blanking Timer

1 Features

- Wide operating input voltage range: 2.7 V to 16 V
  - 20-V absolute maximum
- Integrated FET with low on-resistance: R_{ON} = 6 mΩ (typ.)
- Fast overvoltage protection
  - Adjustable overvoltage lockout (OVLO) with 1.2-µs (typ.) response time
- Overcurrent protection with load current monitor output (ILM)
  - Circuit-breaker response
  - Adjustable threshold (I_{LIM}) 1.5 A – 11 A
    - ±10% accuracy for I_{LIM} > 5 A
  - Adjustable transient blanking timer (ITIMER) to allow peak currents up to 2 × I_{LIM}
  - Output load current monitor accuracy: ±10% (I_{OUT} ≥ 3 A)
- Fast-trip response for short-circuit protection
  - 640-ns (typ.) response time
  - Adjustable (2 × I_{LIM}) and fixed thresholds
- Active high enable input with adjustable undervoltage lockout threshold (UVLO)
- Active low enable input with adjustable undervoltage lockout threshold (OVLO)
- Adjustable output slew rate control (dVdt)
- Overtemperature protection
- Quick Output Discharge
- Digital outputs
  - Power Good (PG) and fault indication ($\overline{FLT}$)
- UL 2367 recognition (pending)
- IEC 62368 CB certification (pending)
- Small footprint: QFN 2-mm × 2-mm, 0.45-mm pitch

2 Applications

- Optical modules
- Server/PC motherboard/add-on cards
- Enterprise routers/data center switches
- Industrial PC
- UHDTV

3 Description

The TPS25981xx family of eFuses is a highly integrated circuit protection and power management solution in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short circuits, voltage surges and excessive inrush current.

Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions by cutting off the output if input exceeds an adjustable overvoltage threshold. The devices respond to output overload by actively limiting the current (during start-up) or breaking the circuit (during steady-state). The overcurrent protection threshold as well as the transient overcurrent blanking timer are user-adjustable. The current limit control pin also functions as an analog load current monitor.

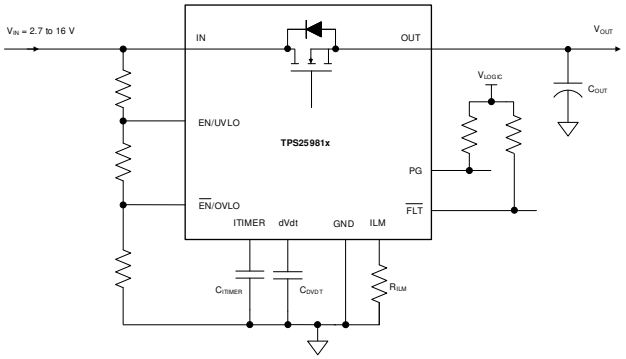
The devices are available in a 2-mm × 2-mm, 10-pin HotRod™ QFN package for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS25981	RPW (VQFN-HR, 10)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (July 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

Part Number	Overvoltage Response	Overcurrent Response	Response to Fault
TPS259814ARPW	Adjustable OVLO	Circuit-Breaker	Auto-Retry
TPS259814LRPW			Latch-Off

6 Pin Configuration and Functions

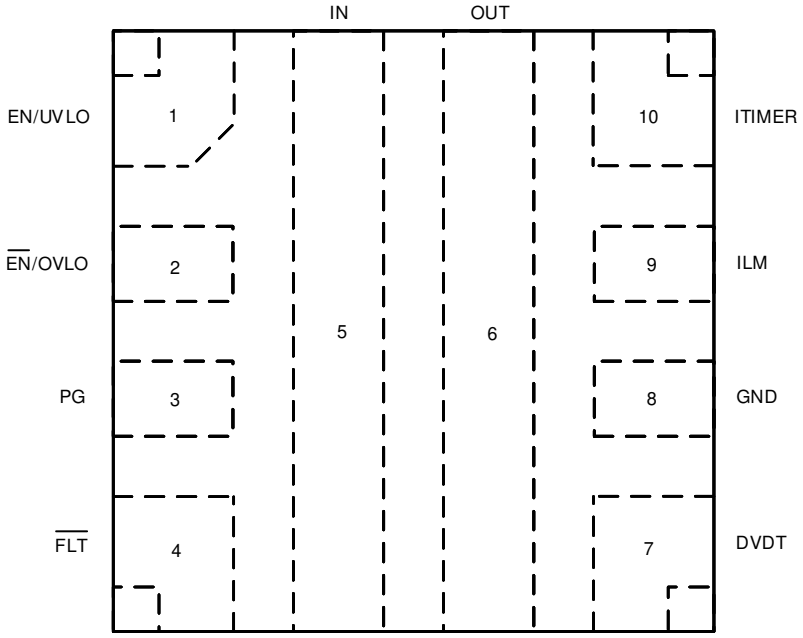


Figure 6-1. TPS25981xx RPW Package 10-Pin QFN Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the undervoltage lockout threshold. *Do not leave floating.* Refer to *Undervoltage Lockout (UVLO and UVP)* for details.
$\overline{EN}$/OVLO	2	Analog Input	A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an Active low enable for the device. *Do not leave floating.* Refer to *Overvoltage Lockout (OVLO)* for details.
PG	3	Digital Output	Power Good indication. This pin is an open-drain signal which is asserted high when the power FET has fully turned ON and is ready to deliver power. Refer to *Power Good (PG)* for more details.
$\overline{FLT}$	4	Digital Output	Active low fault event indicator. This pin is an open-drain signal which is pulled low when a fault is detected. Refer to *Fault Response and Indication ($\overline{FLT}$)* for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn-on slew rate. Refer to *Slew Rate (dVdt) and Inrush Current Control* for details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog Output	This pin is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the overcurrent protection threshold during start-up as well as steady-state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to *Circuit-Breaker During Steady-state* or *Active Current Limiting During Start-up* for more details.
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) during steady-state before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to *Circuit-Breaker During Steady-state* for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40°C ≤ T_J ≤ 125°C	IN	–0.3	20	V
V_{OUT}	Maximum output voltage range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	V_{IN} + 0.3	
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable pin voltage range	EN/UVLO	–0.3	6.5	V
V_{OV}	Maximum $\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT pin voltage range	dVdt	Internally limited		V
V_{ITIMER}	Maximum ITIMER pin voltage range	ITIMER	Internally limited		V
V_{PG}	Maximum PG pin voltage range	PG	–0.3	6.5	V
V_{FLTB}	Maximum $\overline{FLT}$ pin voltage range	$\overline{FLT}$	–0.3	6.5	V
V_{ILM}	Maximum ILM pin voltage range	ILM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	16	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	$\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	0.5	1.5	V
V_{dVdT}	dVdT pin capacitor voltage rating	dVdt	V_{IN} + 5 V		V
V_{FLTB}	$\overline{FLT}$ pin voltage range	$\overline{FLT}$		5	V
V_{PG}	PG pin voltage range	PG		5	V
V_{ITIMER}	ITIMER pin capacitor voltage rating	ITIMER	4		V
R_{ILM}	ILM pin resistance to GND	ILM	600	4400	Ω
I_{MAX}	Continuous switch current, T_J ≤ 125°C	IN to OUT		10	A

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

7.4 Thermal Information

THERMAL METRIC (1)		TPS25981xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7(2)	°C/W
		71.8(3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1(2)	°C/W
	Junction-to-top characterization parameter	1.3(3)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23 (2)	°C/W
		14.5 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 611 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		417	610	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		68	90	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		3	25	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.35	2.42	2.55	V
OUTPUT LOAD CURRENT MONITOR (ILM)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 1.5 A, I_{OUT} < I_{LIM}	82.9	95.3	107.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 3 A, I_{OUT} < I_{LIM}	87	95.3	104.5	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 4.5 A, I_{OUT} < I_{LIM}	87.6	95.3	103.1	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 8 A, I_{OUT} < I_{LIM}	87.7	95.3	102.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 10 A, I_{OUT} < I_{LIM}	87.8	95.3	102.4	µA/A
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, R_{ILM} = 3320 Ω	1.72	1.99	2.26	A
	Overcurrent threshold, R_{ILM} = 2212 Ω	2.64	2.98	3.32	A
	Overcurrent threshold, R_{ILM} = 1102 kΩ	5.43	5.98	6.52	A
	Overcurrent threshold, R_{ILM} = 750 Ω	7.95	8.73	9.52	A
	Overcurrent threshold, R_{ILM} = 611 Ω	9.8	10.76	11.73	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin open (Single point failure)			0.1	A
I_{SPFLT}	Circuit-Breaker threshold, ILM pin shorted to GND (Single point failure)		2.24	3.3	A
I_{FT}	Fixed fast-trip current threshold		39.5		A
I_{SCGain}	Scalable fast-trip threshold (I_{SC}) : I_{LIM} ratio	170	193	242	%
V_{FB}	V_{OUT} threshold to exit current limit foldback	1.55	1.91	2.23	V
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} ≤ 4 V, I_{OUT} = 3 A, T_J = 25°C		6.07		mΩ
	4 < V_{IN} ≤ 16 V, I_{OUT} = 3 A, T_J = 25°C		5.81		mΩ
	2.7 ≤ V_{IN} ≤ 16 V, I_{OUT} = 3 A, –40°C ≤ T_J ≤ 125°C			8.4	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.176	1.20	1.224	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.073	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.45	0.75		V
I_{ENLKG}	EN/UVLO pin leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT ($\overline{EN}$/OVLO)					
$V_{OV(R)}$	OVLO rising threshold	1.176	1.20	1.224	V
$V_{OV(F)}$	OVLO falling threshold	1.074	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current (0.5 V < V_{OVLO} < 1.5 V)	–0.1		0.1	µA
OVERCURRENT FAULT TIMER (ITIMER)					
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.25	2	2.72	µA

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 611 Ω , dVdT = Open, ITIMER = Open, $\overline{FLT}$ = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
R_{ITIMER}	ITIMER pin internal pullup resistance		15.4		kΩ
V_{INT}	ITIMER pin internal pullup voltage	2.1	2.57	2.74	V
$V_{ITIMER(F)}$	ITIMER comparator threshold, I_{OUT} > I_{LIM}	0.6	1.06	1.37	V
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold, I_{OUT} > I_{LIM}	1.28	1.51	1.74	V
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pullup (I_{PG} = 26 µA)		0.66	0.80	V
	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pullup (I_{PG} = 242 µA)		0.78	0.90	V
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0	0.60	V
I_{PGLKG}	PG pin leakage current, PG asserted			3	µA
R_{FLTB}	$\overline{FLT}$ pin internal pulldown resistance		12.57		Ω
FAULT INDICATION ($\overline{FLT}$)					
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	–1		1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J↑		154		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J↓		10		°C
DVDT					
I_{dVdt}	dVdt pin internal charging current	1.4	3.45	5.7	µA
QUICK OUTPUT DISCHARGE (OUT)					
R_{QOD}	Quick Output Discharge Resistance, V_{EN} < $V_{UVLO(F)}$	455	488	530	Ω

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT}↓		1.2		µs
t_{CB}	Circuit-Breaker response time	ITIMER = Open, I_{OUT} > I_{LIM} + 30% to V_{OUT}↓		1.8		µs
t_{SC}	Short-circuit response time	I_{OUT} > 3 × I_{LIM} to output current cut off		640		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT}↓		640		ns
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD – TSD_{HYS}		105		ms
t_{PGA}	PG assertion de-glitch time			14		µs
t_{PGD}	PG de-assertion de-glitch time			14		µs

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it slows the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady-state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNITS
SR_{ON}	Output rising slew rate	2.7 V	8.19	1.30	0.78	V/ms
		5 V	11.28	1.42	0.84	
		12 V	19.71	1.68	0.98	
$t_{D,ON}$	Turn-on delay	2.7 V	0.14	0.46	0.70	ms
		5 V	0.14	0.60	0.96	
		12 V	0.14	0.93	1.57	
t_R	Rise time	2.7 V	0.26	1.66	2.77	ms
		5 V	0.36	2.82	4.78	
		12 V	0.49	5.74	9.84	
t_{ON}	Turn-on time	2.7 V	0.40	2.11	3.47	ms
		5 V	0.50	3.42	5.74	
		12 V	0.63	6.67	11.41	
$t_{D,OFF}$	Turn-off delay	2.7 V	24.90	24.90	24.90	µs
		5 V	21.10	21.10	21.10	
		12 V	18.80	18.80	18.80	

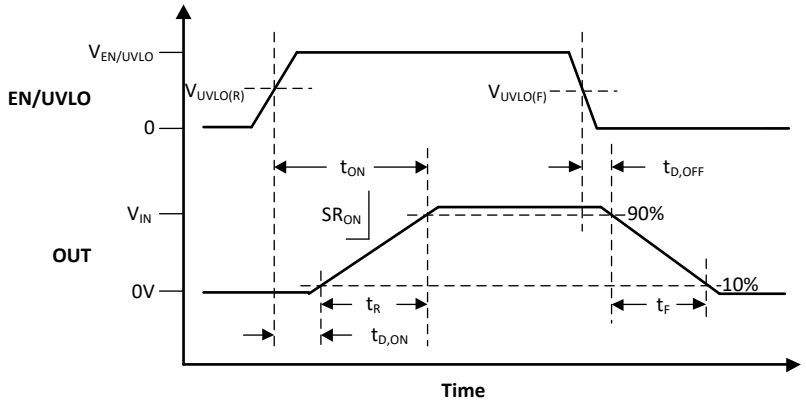


Figure 7-1. TPS25981xx Switching Times

7.8 Typical Characteristics

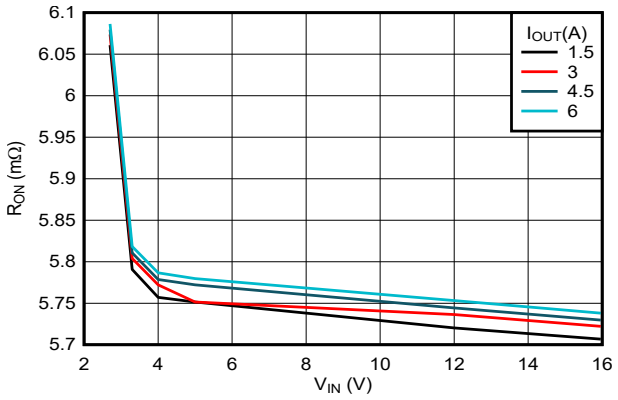


Figure 7-2. ON-Resistance vs Supply Voltage (T_A = 25°C)

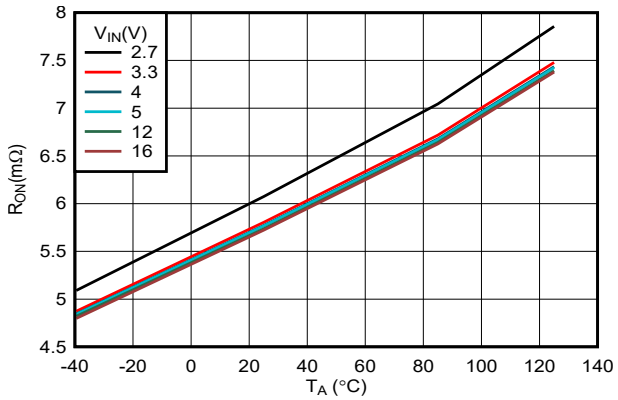


Figure 7-3. ON-Resistance vs Temperature (I_{OUT} = 3 A)

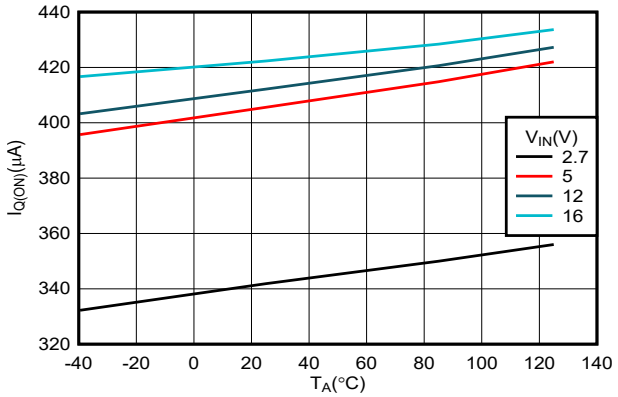


Figure 7-4. IN Quiescent Current vs Temperature

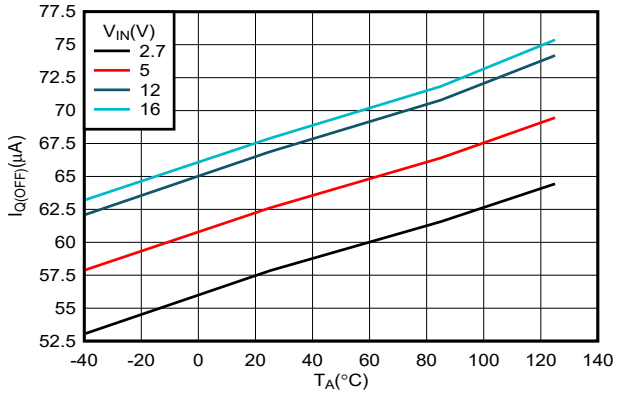


Figure 7-5. IN OFF State (UVLO) Current vs Temperature

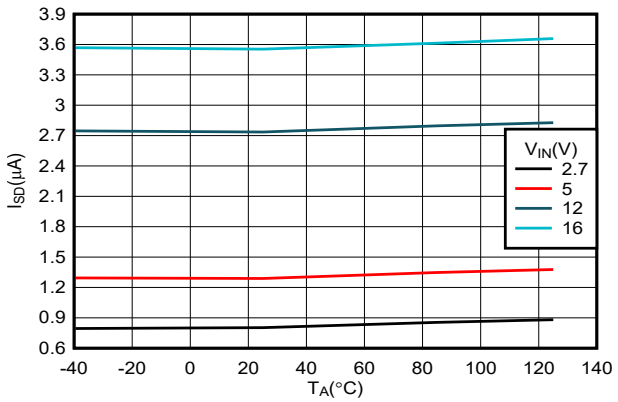


Figure 7-6. IN Shutdown Current vs Temperature

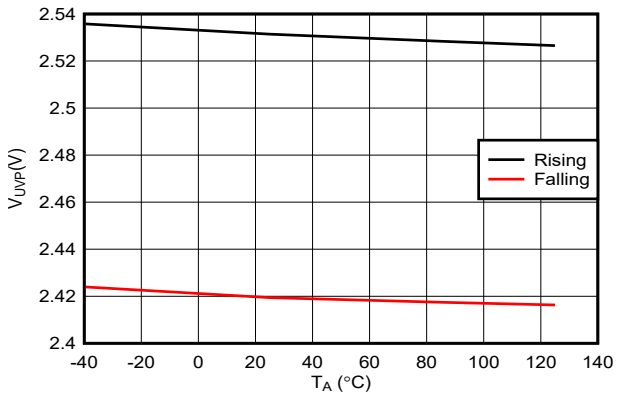


Figure 7-7. IN Undervoltage Threshold vs Temperature

7.8 Typical Characteristics (continued)

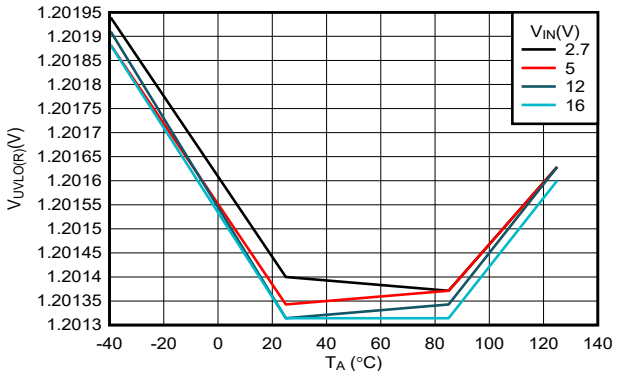


Figure 7-8. EN/UVLO Rising Threshold vs Temperature

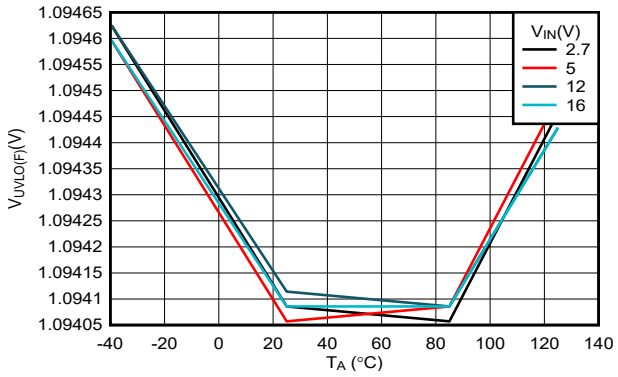


Figure 7-9. EN/UVLO Falling Threshold vs Temperature

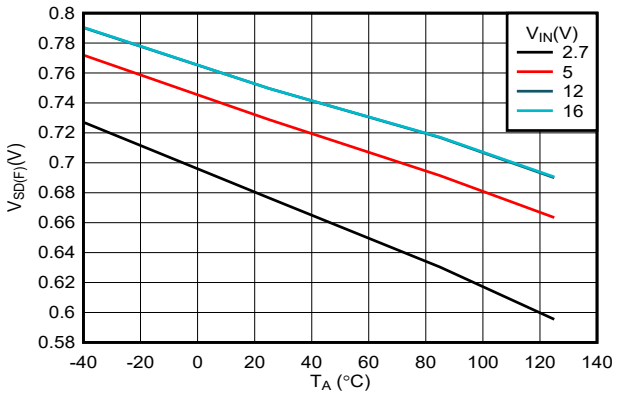


Figure 7-10. EN/UVLO Shutdown Falling Threshold vs Temperature

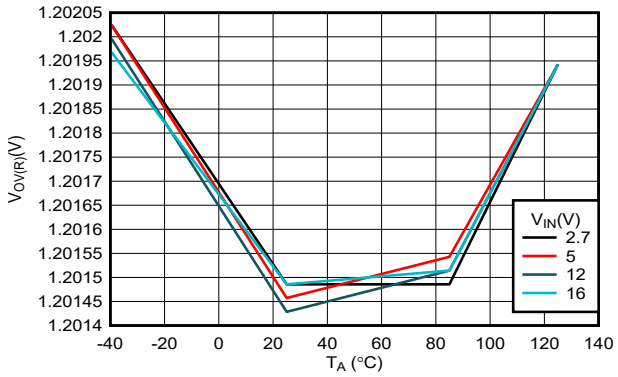


Figure 7-11. OVLO Rising Threshold vs Temperature

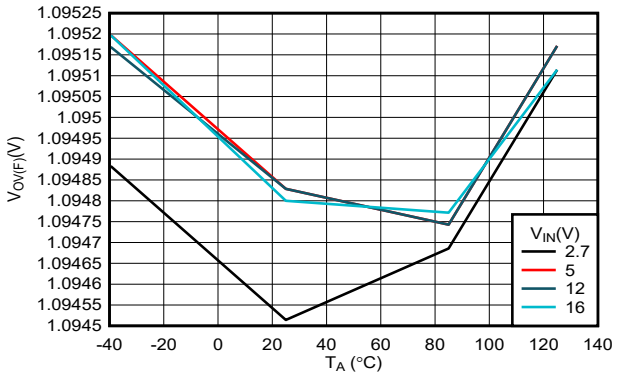


Figure 7-12. OVLO Falling Threshold vs Temperature

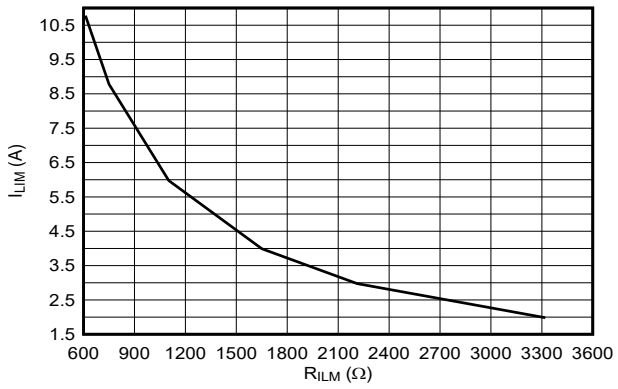


Figure 7-13. Overcurrent Threshold vs ILM Resistor

7.8 Typical Characteristics (continued)

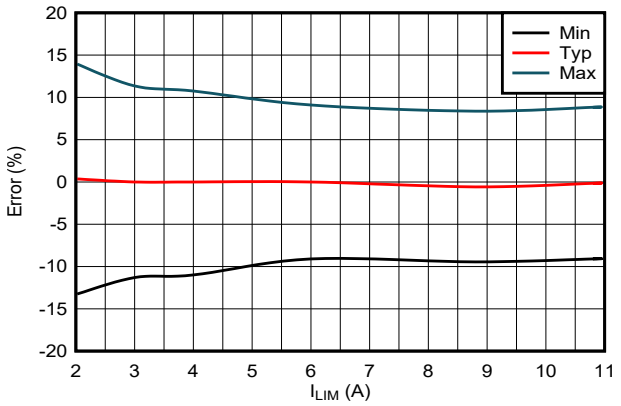


Figure 7-14. Overcurrent Threshold Accuracy (Across Process, Voltage and Temperature)

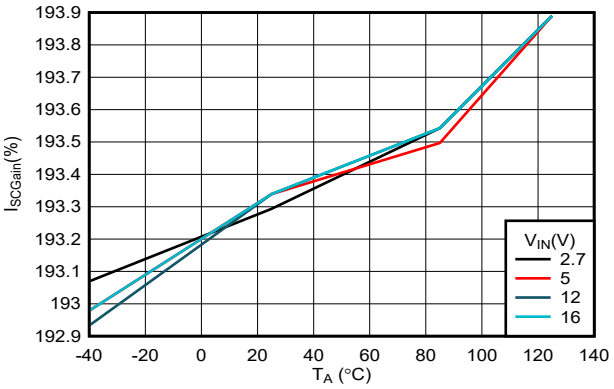


Figure 7-15. Scalable Fast-Trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature

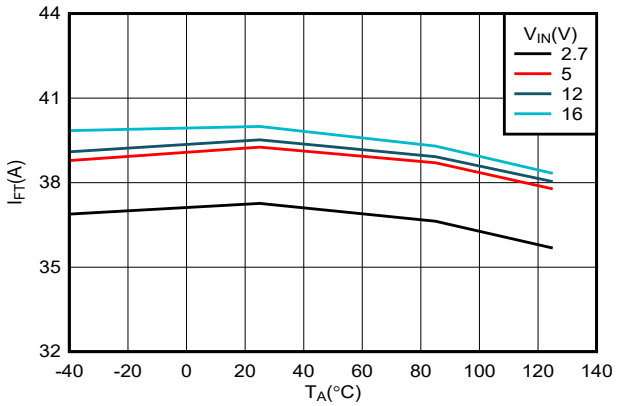


Figure 7-16. Fixed Fast-Trip Threshold vs Temperature

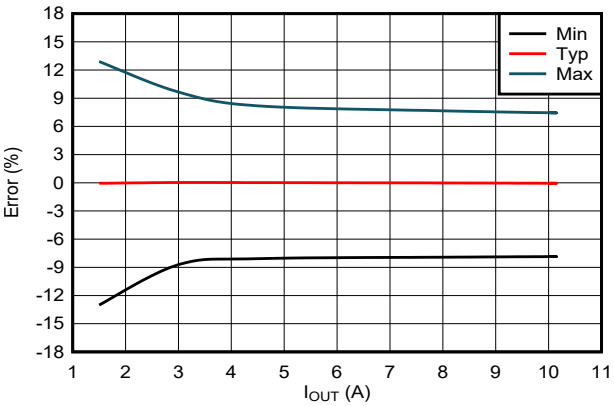


Figure 7-17. Analog Current Monitor Gain Accuracy

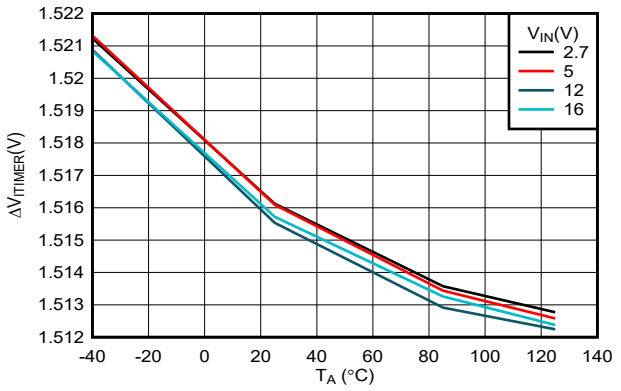


Figure 7-18. ITIMER Discharge Differential Voltage Threshold vs Temperature

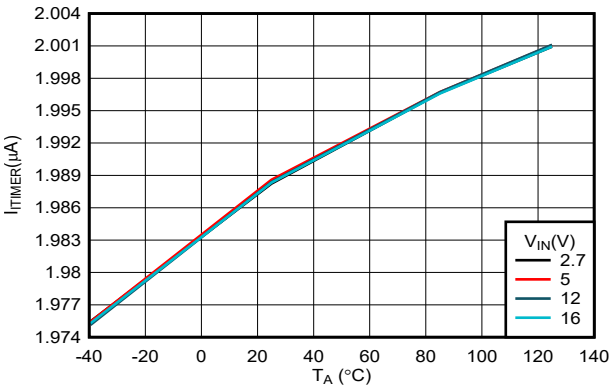


Figure 7-19. ITIMER Discharge Current vs Temperature

7.8 Typical Characteristics (continued)

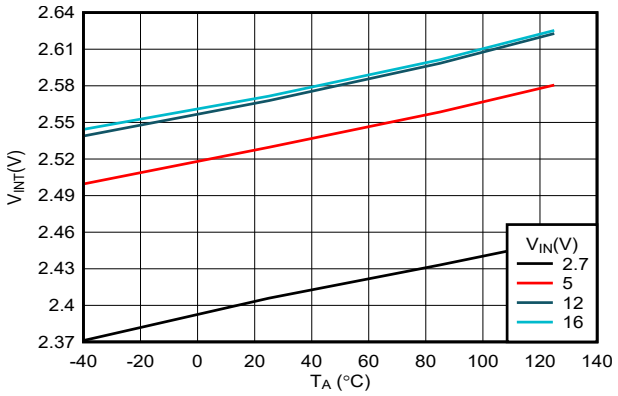


Figure 7-20. ITIMER Internal Pullup Voltage vs Temperature

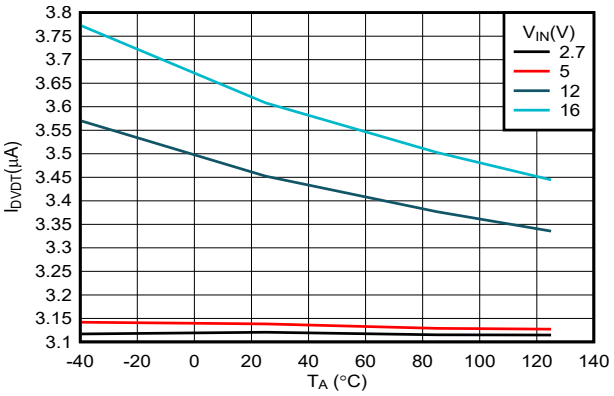


Figure 7-21. DVDT Charging Current vs Temperature

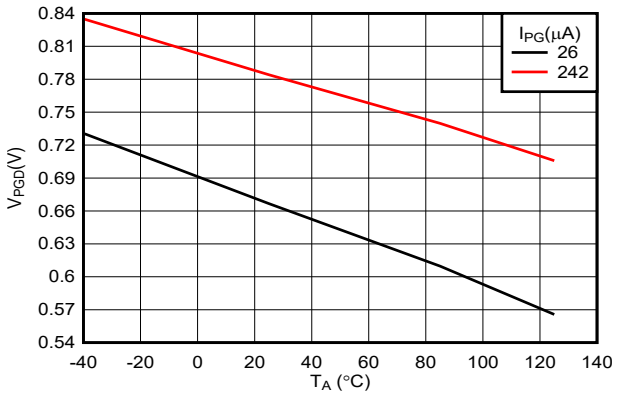


Figure 7-22. PG Pin Voltage vs Temperature (VIN = 0 V)

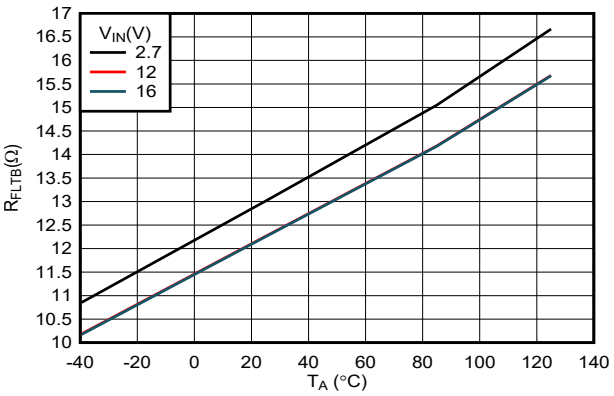


Figure 7-23. $\overline{\text{FLT}}$ Pin Pulldown Resistance vs Temperature

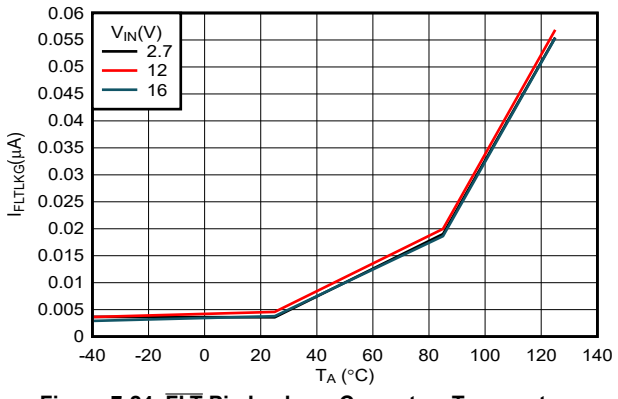


Figure 7-24. $\overline{\text{FLT}}$ Pin Leakage Current vs Temperature

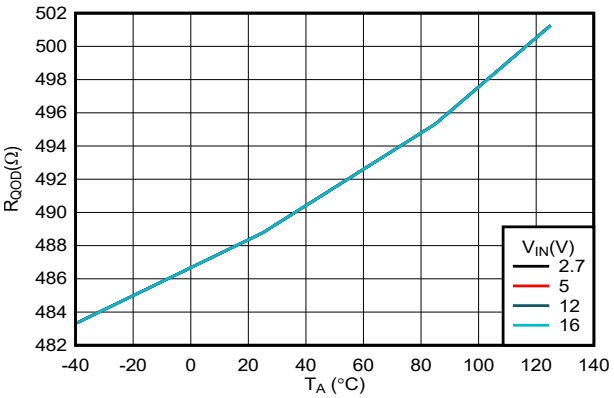


Figure 7-25. Quick Output Discharge Resistance vs Temperature

7.8 Typical Characteristics (continued)

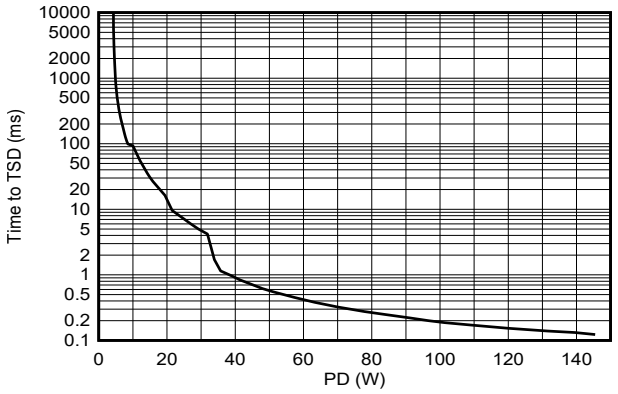


Figure 7-26. Time to Thermal Shutdown During Inrush State

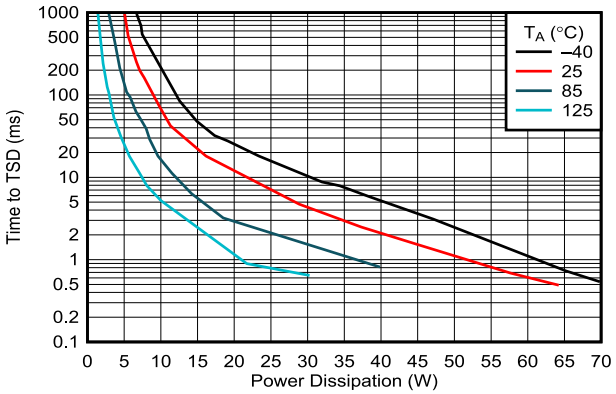
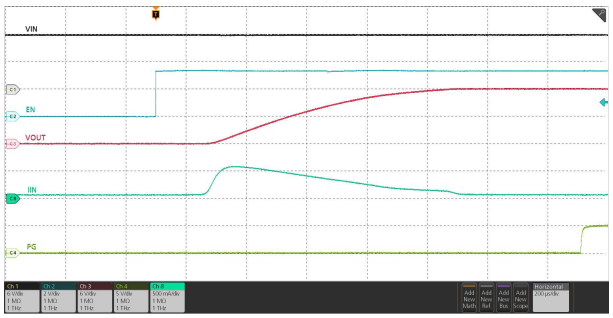
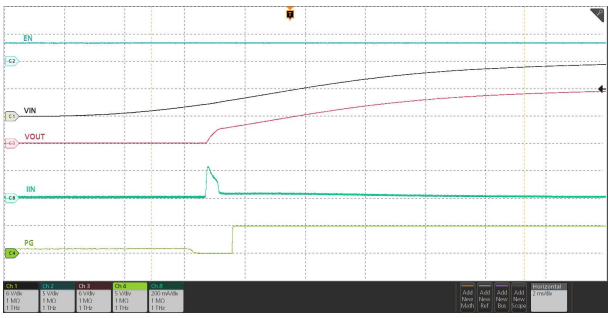


Figure 7-27. Time to Thermal Shutdown During Steady-State



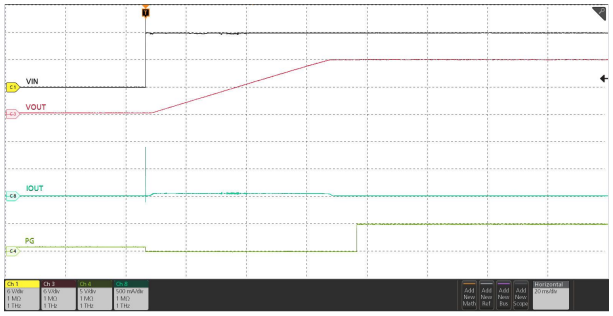
V_{IN} = 12 V, C_{OUT} = 10 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 3.3 V

Figure 7-28. Start-Up with Enable



$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 10 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

Figure 7-29. Start-Up with Supply



C_{OUT} = 220 µF, C_{dVdt} = 15 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

Figure 7-30. Input Hot-Plug

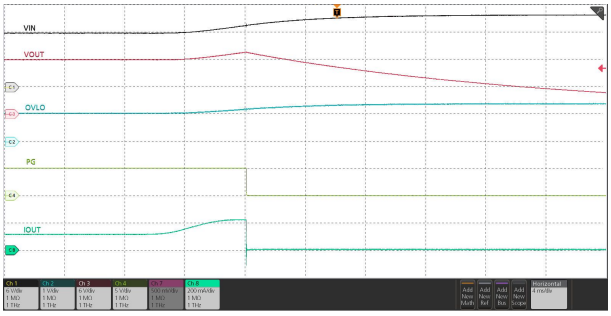
V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-31. Inrush Current with Capacitive Load

7.8 Typical Characteristics (continued)

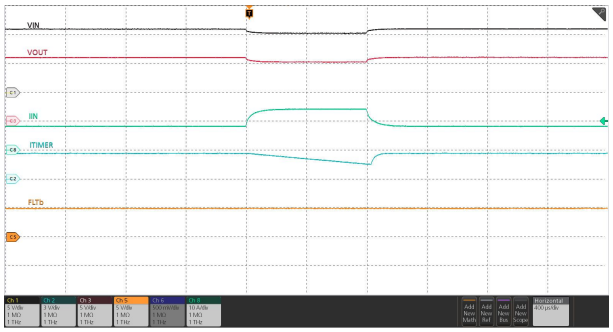
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-32. Inrush Current with Resistive and Capacitive Load



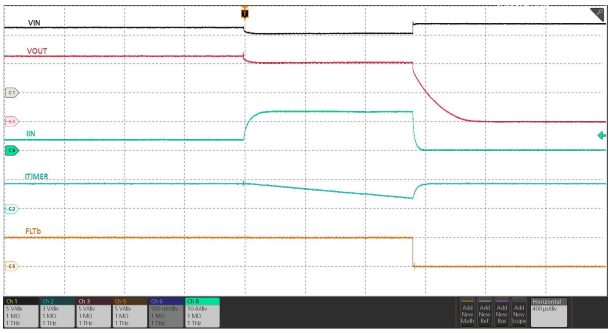
V_{IN} Overvoltage threshold set to 13.6 V using resistor ladder connected to OVLO pin, V_{IN} ramped up from 12 V to 16 V

Figure 7-33. Overvoltage Lockout Response



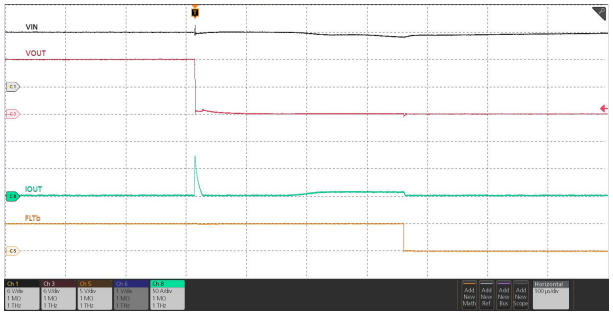
V_{IN} = 12 V, C_{ITIMER} = 1.5 nF, R_{ILM} = 649 Ω, I_{OUT} ramped from 8 A → 14 A→ 8 A within 1 ms

Figure 7-34. Transient Overcurrent Blanking Timer Response



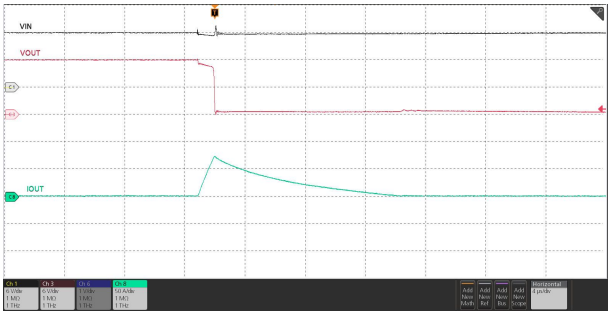
V_{IN} = 12 V, C_{ITIMER} = 1.5 nF, R_{ILM} = 649 Ω, I_{OUT} ramped from 4 A → 13 A

Figure 7-35. Circuit-Breaker Response



V_{IN} = 12 V, R_{ILM} = 649 Ω, OUT stepped from Open → Short-circuit to GND

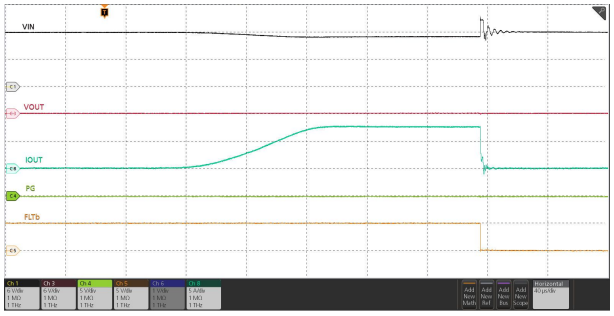
Figure 7-36. Output Short-Circuit During Steady-State



V_{IN} = 12 V, R_{ILM} = 649 Ω, OUT stepped from Open → Short-circuit to GND

Figure 7-37. Output Short-Circuit During Steady-State (Zoomed In)

7.8 Typical Characteristics (continued)



V_{IN} = 12 V, OUT short-circuit to GND, R_{ILM} = 649 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

Figure 7-38. Power Up into Short Circuit

8 Detailed Description

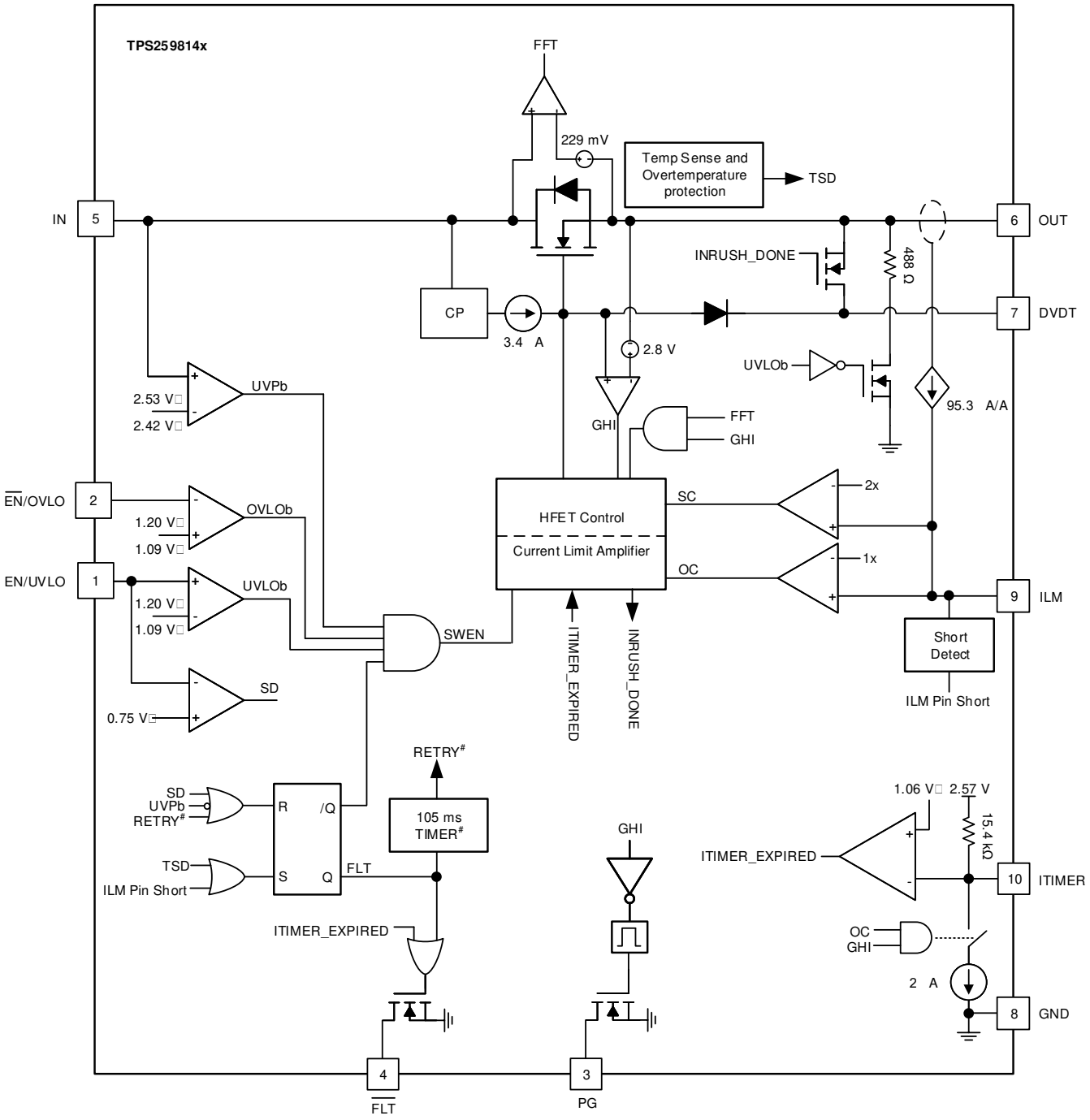
8.1 Overview

The TPS25981xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the Undervoltage Protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the user adjustable overcurrent protection threshold (I_{LIM}) is not exceeded and overvoltage spikes are cut-off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This feature keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This feature ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

8.2 Functional Block Diagram



Not applicable to Latch-off variants (TPS259814L)

8.3 Feature Description

The TPS25981xx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS25981xx implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 8-1 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

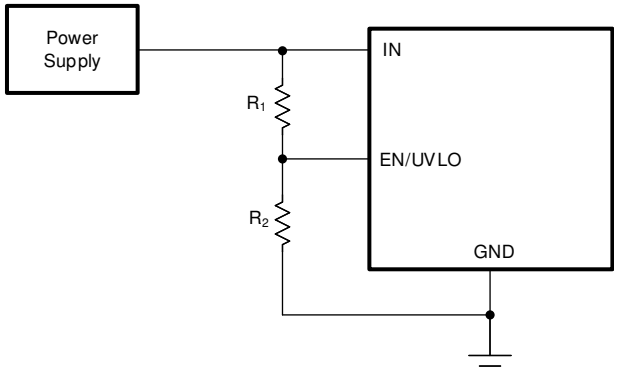


Figure 8-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

8.3.2 Overvoltage Lockout (OVLO)

The TPS259814x devices allow the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the $\overline{EN}$/OVLO pin allows the overvoltage protection threshold to be adjusted to a user defined value. After the voltage at the $\overline{EN}$/OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the $\overline{EN}$/OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. Figure 8-2 and Equation 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

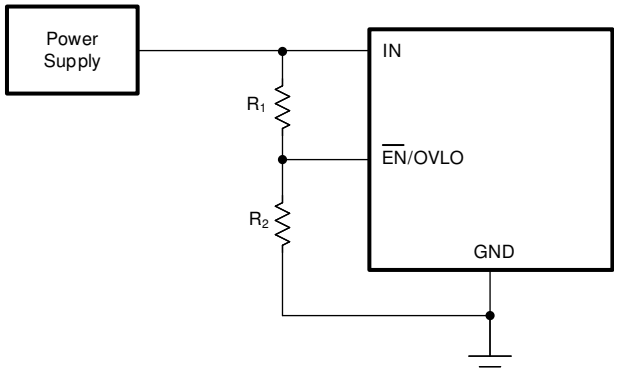


Figure 8-2. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

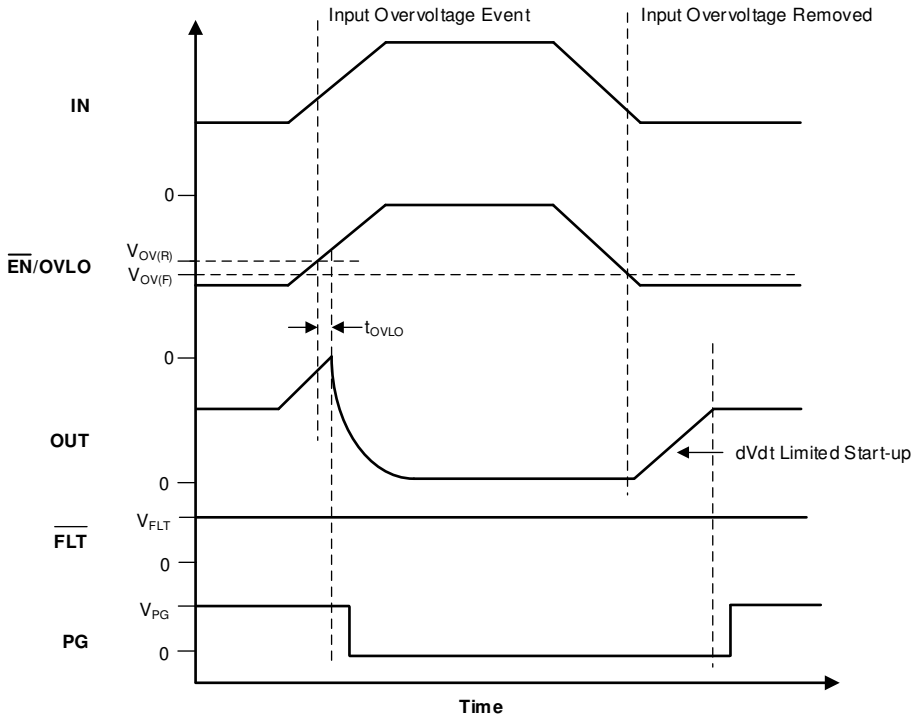


Figure 8-3. TPS259814x Overvoltage Lockout and Recovery

While recovering from a OVLO event, the TPS259814x variants start up with inrush control (dVdt).

8.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25981xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short circuits during steady-state

8.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. Use Equation 4 to calculate the required C_{dVdt} capacitance to produce a given slew rate.

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

8.3.3.2 Circuit-Breaker During Steady-State

The TPS259814x (circuit-breaker) variants respond to output overcurrent conditions by turning off the output after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the fast-trip threshold (2 × I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 2-µA pulldown current. If the load current drops below I_{LIM} before the ITIMER pin capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short load transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. Equation 5 can be used to calculate the R_{ILM} value for a overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} \tag{5}$$

Note

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part breaking the circuit with the slightest amount of loading at the output.
2. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There is a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. Use Equation 6 to calculate the C_{ITIMER} value needed to set the desired transient overcurrent blanking interval.

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} \tag{6}$$

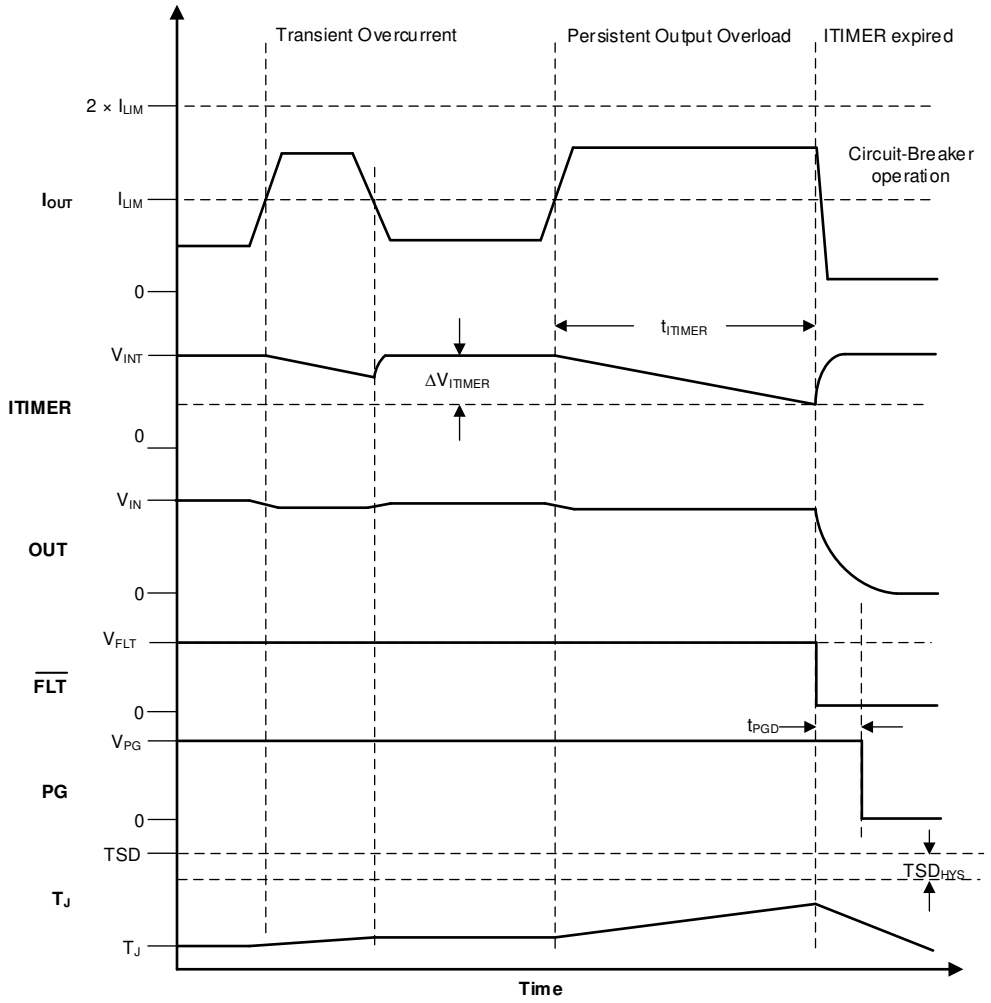


Figure 8-4. TPS259814x Overcurrent Response

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This action is not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it takes lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.
4. In low voltage applications, TI recommends adding a 30 kΩ resistor between the ITIMER pin and C_{ITIMER} for improved immunity to supply noise or fluctuations.

After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS259814L variant) or restarts automatically after a fixed delay (TPS259814A variant).

8.3.3.3 Active Current Limiting During Start-Up

The TPS259814x devices respond to output overcurrent conditions during start-up by actively limiting the current. If the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 × I_{LIM}), the current limit loop starts regulating the FET to actively

limit the current to the set overcurrent threshold (I_{LIM}). Equation 7 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} \tag{7}$$

Note

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the target steady-state overcurrent threshold (I_{LIM}).

During active current limit, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to TSD fault, it either stays latched off (TPS25981xL variants) or restarts automatically after a fixed delay (TPS25981xA variants). For more details on device response to overtemperature, see *Overtemperature Protection (OTP)*.

8.3.3.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This action enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short circuits during steady-state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. After the current exceeds I_{SC} or I_{FT}, the FET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the FET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This action ensures that the FET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. For details on the device response to overtemperature, see *Overtemperature Protection (OTP)*.

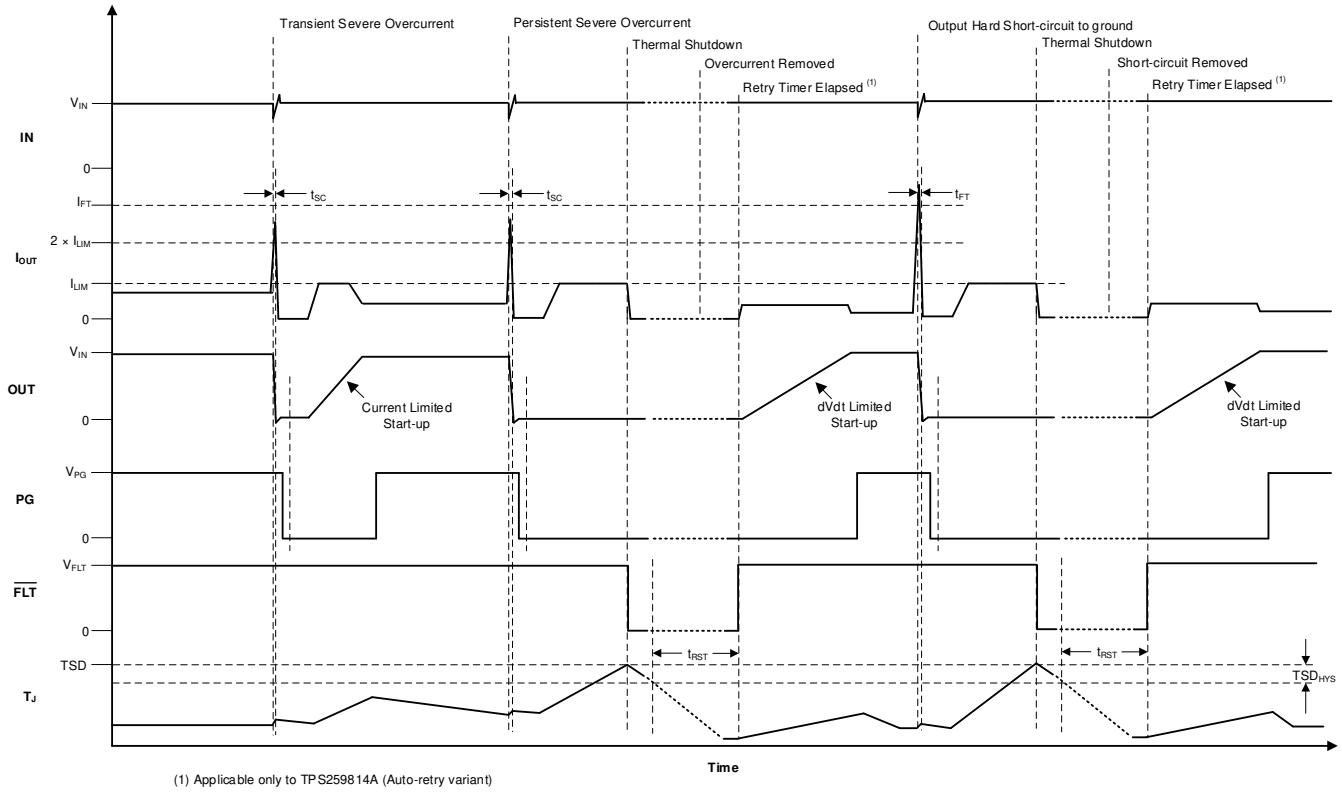


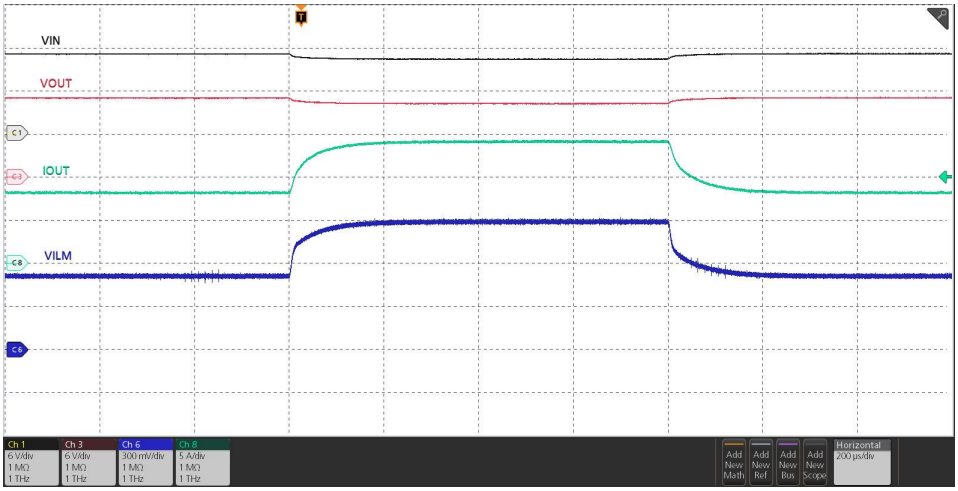
Figure 8-5. TPS25981xx Short-Circuit Response

8.3.4 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{LOAD}\,(A) = \frac{V_{ILM}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times R_{ILM}\,(\Omega)} \tag{8}$$

The waveform below shows the ILM signal response to a load step at the output.



V_{IN} = 12 V, R_{ILM} = 649 Ω, I_{OUT} varied dynamically between 8 A and 14 A

Figure 8-6. Analog Load Current Monitor Response

Note

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

8.3.5 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device does turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS25981xL (latch-off variant) detects thermal overload, it is shut down and remains latched-off until the device is power cycled or re-enabled. When the TPS25981xA (auto-retry variant) detects thermal overload, it remains off until it has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

Table 8-1. Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS25981xL (latch-off)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ *or* EN/UVLO toggled below $V_{SD(F)}$
TPS25981xA (auto-retry)	T_J ≥ TSD	T_J < TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ *or* EN/UVLO toggled below $V_{SD(F)}$ *or* t_{RST} timer expired

8.3.6 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available.

Table 8-2. Fault Summary

Event	Protection Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	$\overline{FLT}$ Assertion Delay
Overtemperature	Shutdown	Y	L	
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input overvoltage	Shutdown	N	H	
Transient overcurrent (I_{LIM} < I_{OUT} < 2 × I_{LIM})	None	N	N	
Persistent overcurrent	Circuit-breaker	Y	N/A	
Output short circuit to GND	Circuit-breaker followed by current limit	N	H	
ILM pin open (during steady-state)	Shutdown	N	L	t_{ITIMER}
ILM pin shorted to GND	Shutdown	Y	L	t_{ITIMER}

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This action also releases the $\overline{FLT}$ pin and resets the t_{RST} timer for the TPS25981xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This fact is true for both TPS25981xL (latch-off) and TPS25981xA (auto-retry) variants.

For TPS25981xA (auto-retry) variants, on expiry of the t_{RST}timer after a fault, the device restarts automatically and the $\overline{FLT}$ pin is de-asserted.

8.3.7 Power Good Indication (PG)

The TPS259814x provides an active high digital output (PG) which serves as a power good indication signal and is asserted high when the device is in steady-state and ready to deliver power. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the FET is turned on in a controlled manner. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time the FET is turned off. The PG de-assertion de-glitch time is t_{PGD}.

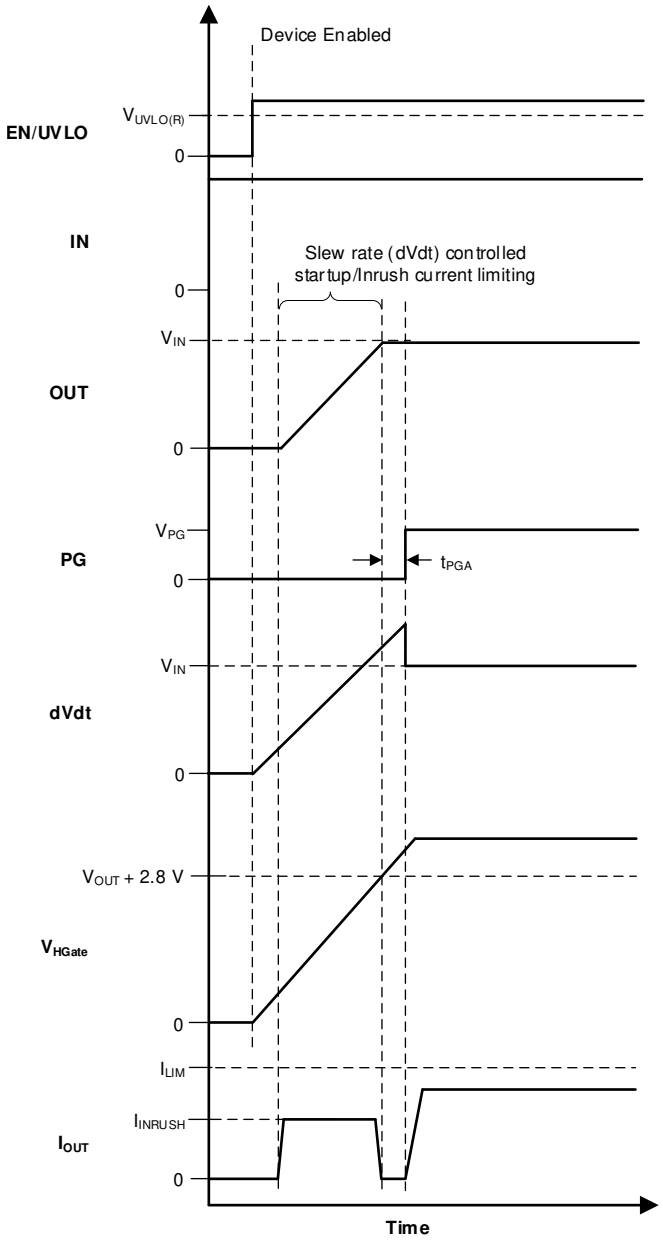


Figure 8-7. TPS25981xx PG Timing Diagram

Table 8-3. TPS25981xx PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L	t_{PGD}
Steady-state	NA	H	t_{PGA}
Transient overcurrent	NA	H	
Persistent overload	Circuit-breaker	L	t_{ITIMER} + t_{PGD}
Output short-circuit to GND	Fast-trip followed by current limit	L	t_{PGD}
ILM pin open	Shutdown	L	t_{ITIMER} + t_{PGD}
ILM pin shorted to GND	Shutdown	L	t_{PGD}
Overtemperature	Shutdown	L	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.3.8 Quick Output Discharge (QOD)

The TPS25981xx has an integrated output discharge function which can be helpful in quickly removing residual charge left on the large output capacitors and avoids bus floating at some undefined voltage. The internal QOD pulldown FET on the OUT pin is activated when the EN/UVLO is held low ($V_{EN} < V_{UVLO(F)}$). The output discharge function can result in excess power dissipation inside the device leading to increase in junction temperature. The output discharge is disabled if the junction temperature (T_J) crosses the thermal shutdown threshold (TSD) to avoid long term degradation of the part.

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25981xx is a 2.7-V to 16-V, 10-A eFuse that is typically used for power rail protection applications. The device operates from 2.7 V to 16 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current. The device can be used in a variety of systems such as server motherboard/add-on cards/NIC, optical modules, enterprise switches/routers, Industrial PC, UHDTV. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS25981xx Design Calculator*, is available in the web product folder.

9.1.1 Single Device, Self-Controlled

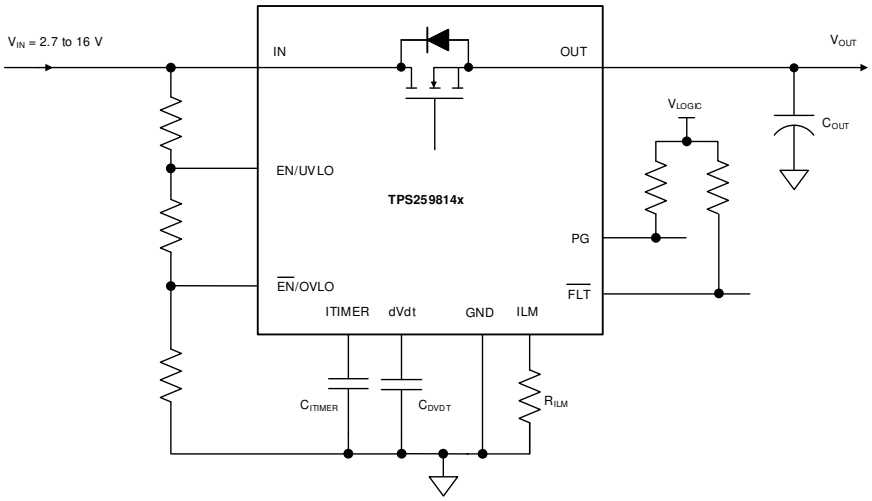


Figure 9-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

Note

TI recommends to keep parasitic capacitance on the ILM pin below 50 pF to ensure stable operation.

9.1.2 Parallel Operation

Applications which need higher steady current can use two TPS25981xx devices connected in parallel as shown in Figure 9-2 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the PG signal of the first device. After the inrush sequence is complete, the first device asserts its PG pin high and turns on the second device.

The second device asserts its PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady-state current.

Once in steady-state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

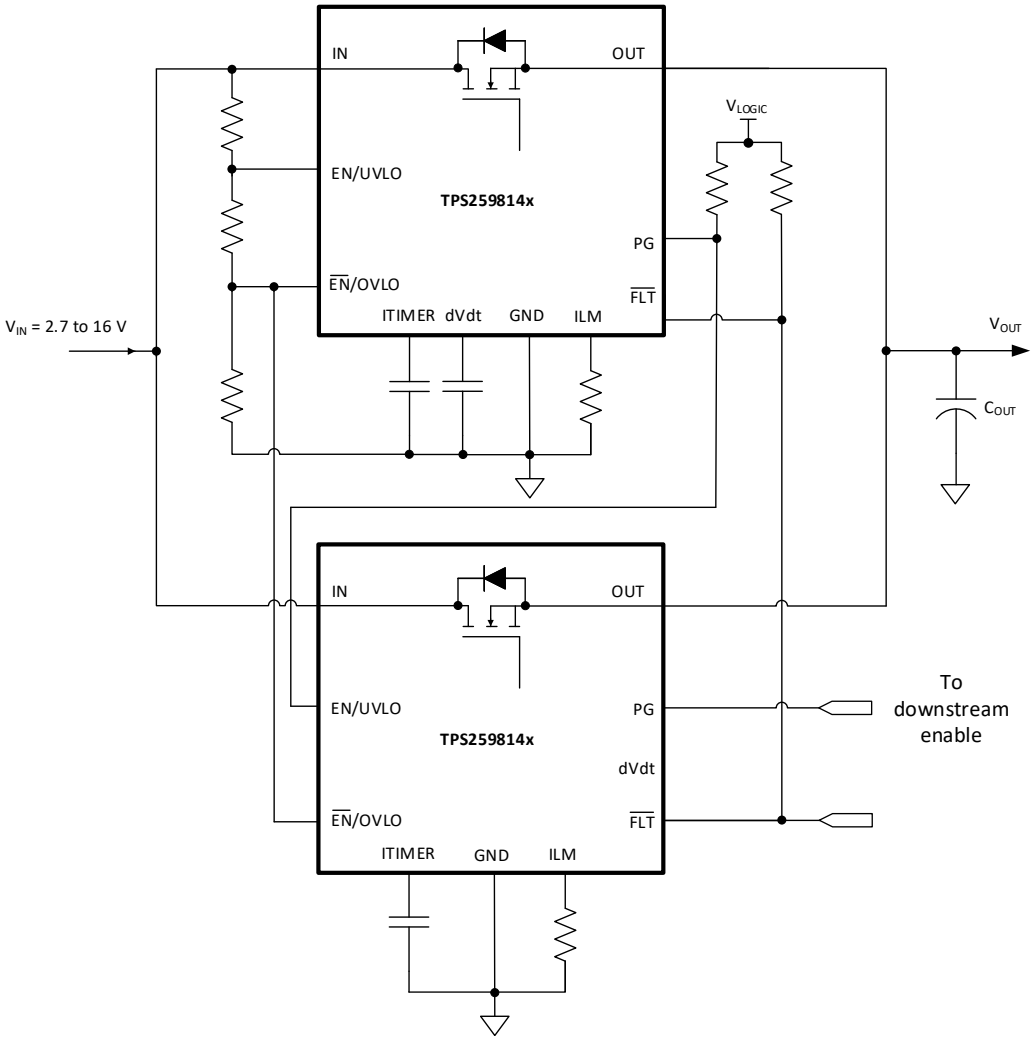


Figure 9-2. Two TPS259814x Devices Connected in Parallel for Higher Steady-State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady-state.

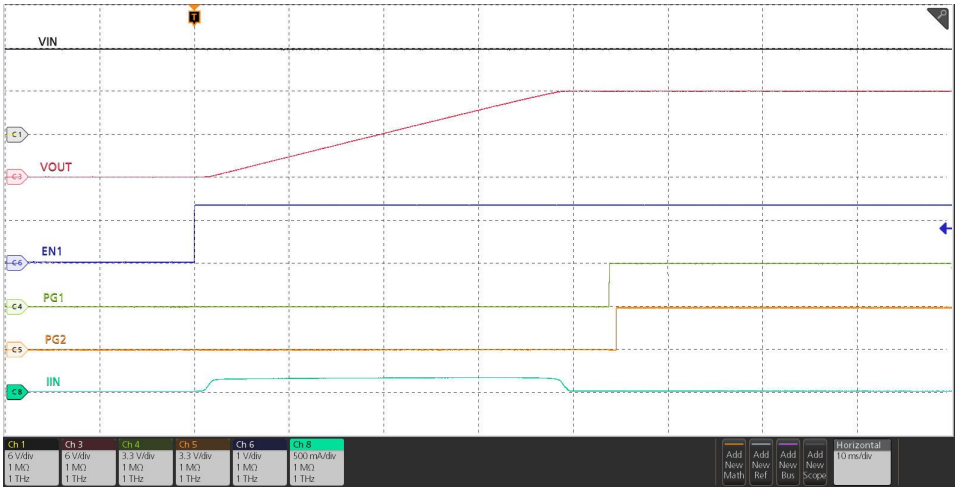


Figure 9-3. Parallel Devices Sequencing During Start-Up

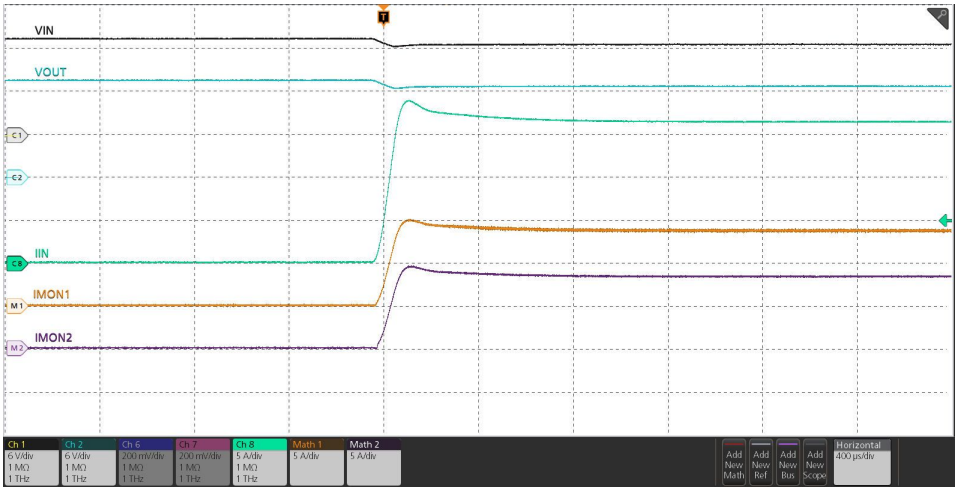


Figure 9-4. Parallel Devices Load Current During Steady-State

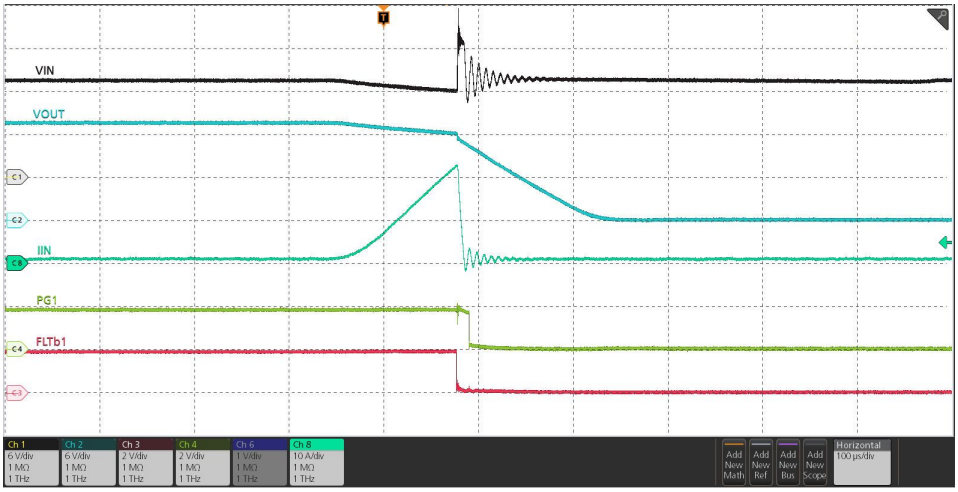


Figure 9-5. Parallel Devices Overcurrent Response

Another way to increase current handling capability of the eFuse in steady-state is by connecting a TPS25981xx eFuse in parallel with a TPS22811x load switch as shown in Figure 9-6.

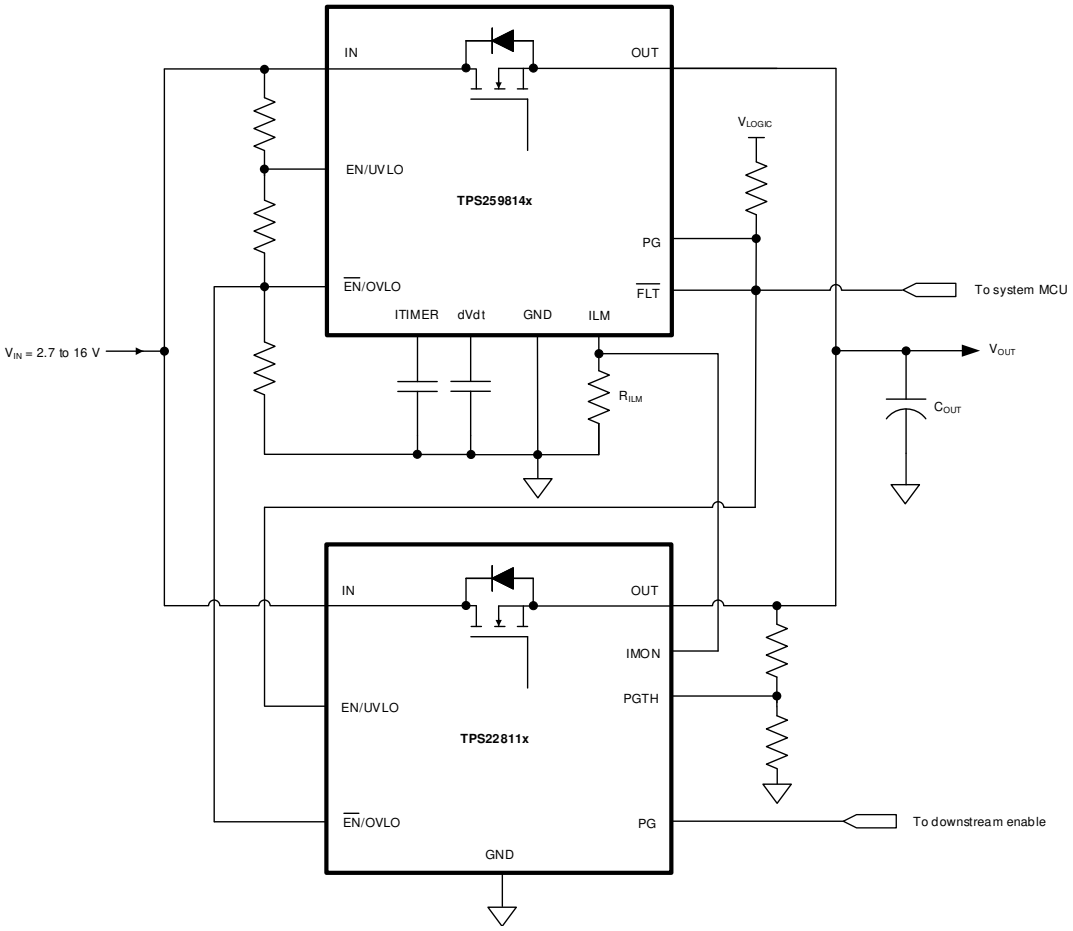


Figure 9-6. TPS259814x and TPS22811x Connected in Parallel for Higher Steady-State Current Capability

9.2 Typical Application

TPS259814x can be used for optical module power rail protection. Optical modules are commonly used in high-bandwidth data communication systems such as optical networking equipment, enterprise/data-center switches and routers. Several variants of optical modules are available in the market, which differ in the form-factor and the data speed support (Gbit/s). Of these, the popular variant double dense quad small form-factor pluggable (QSFP-DD) module supports speeds up to 400 Gbit/s. In addition to the system protection during hot-plug events, the other key requirement for optical module is the tight voltage regulation. The optical module uses 3.3-V supply and requires voltage regulation within ±5% for proper operation.

A typical power tree of such system is shown in Figure 9-7. The optical line card consists of DC-DC converter, protection device (eFuse) and power supply filters. The DC-DC converter steps-down the 12 V to 3.3 V and maintains the 3.3-V rail within ±2 %. The power supply filtering network uses ‘LC’ components to reduce high frequency noise injection into the optical module. The DC resistance of the inductor ‘L’ causes voltage drop of around 1.5% which leaves us with a voltage drop budget of just 1.5% (3.3 V × 1.5% = 50 mV) across the protection device. Considering a maximum load current of 5.5 A per module, the maximum ON-resistance of the protection device must be less than 9 mΩ. TPS259814x eFuse offers a very low ON-resistance of 6 mΩ (typical), thereby meeting the target specification with additional margin to spare and simplifying the overall system design.

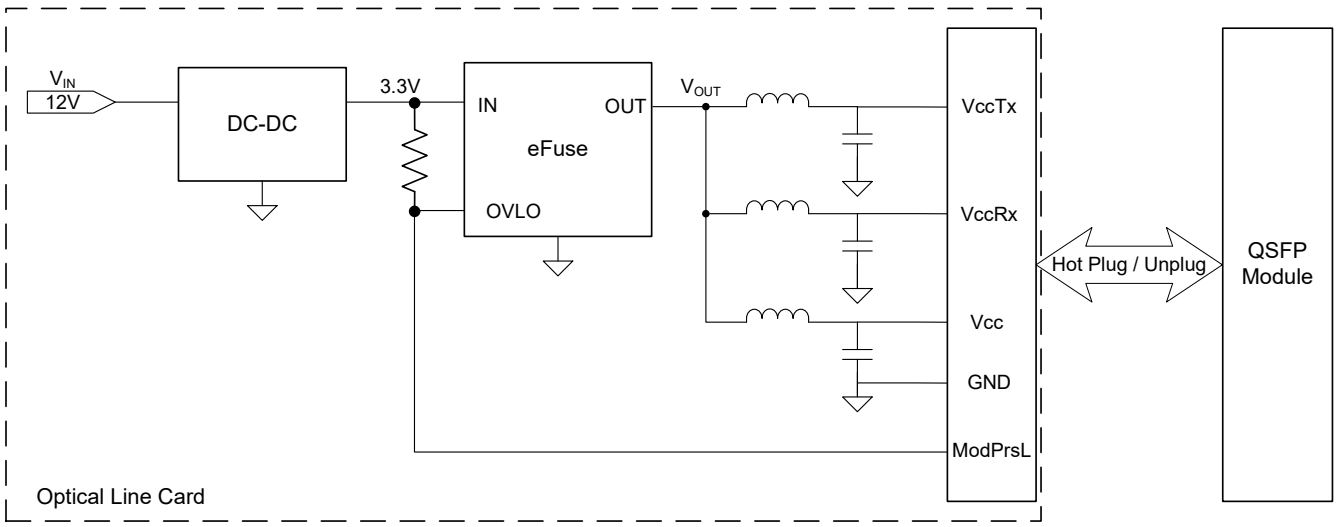
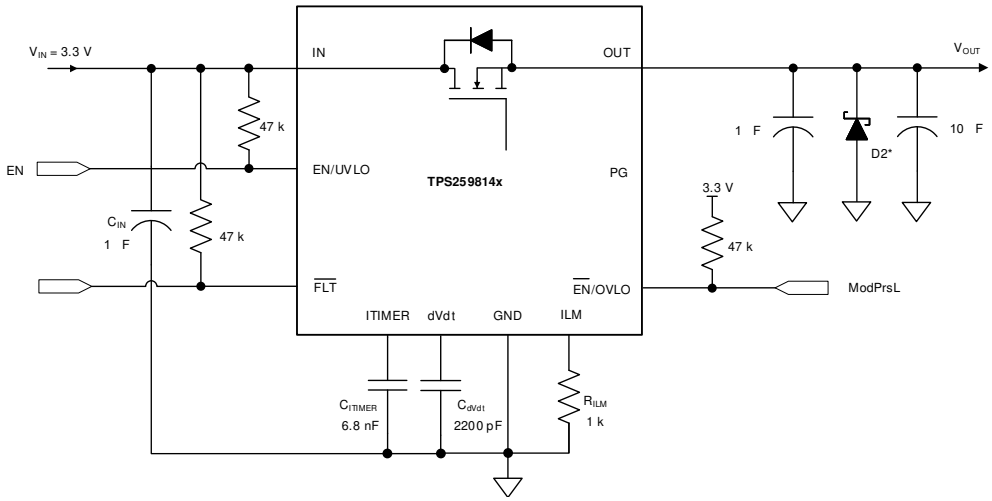


Figure 9-7. Power Tree Block Diagram of a Typical Optical Line Card

As shown in *Figure 9-7*, ModPrsL signal acts as a handshake signal between the line card and the optical module. ModPrsL is always pulled to ground inside the module. When the module is hot-plugged into the host "Optical Line Card" connector, the ModPrsL signal pulls down the OVLO pin and enables the TPS259814x eFuse to power the module. This action ensures that power is applied on the port only when a module is plugged in and disconnected when there is no module present.



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

Figure 9-8. Optical Module Port Protection

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	3.3 V
Maximum voltage drop in the path	± 5%
Maximum continuous current	5.5 A
Load transient blanking interval (t_{ITIMER})	5 ms
Output capacitance (C_{OUT})	10 µF

Table 9-1. Design Parameters (continued)

PARAMETER	VALUE
Output rise time (t_R)	2.2 ms
Overcurrent threshold (I_{LIM})	6.5 A
Fault response	Auto-retry

9.2.2 Detailed Design Procedure

9.2.2.1 Device Selection

Because the application requires retry response after a fault, the TPS259814A variant is selected after referring to the *Device Comparison Table*.

9.2.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\left(\frac{V}{ms}\right) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{3.3\,V}{2.2\,ms} = 1.5\,\frac{V}{ms} \tag{9}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} = \frac{3300}{1.5\,\frac{V}{ms}} = 2200\,pF \tag{10}$$

Choose the nearest standard capacitor value as 2200 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = C_{OUT}\,(\mu F) \times SR\left(\frac{V}{ms}\right) = 10\,\mu F \times 1.5\,\frac{V}{ms} = 15\,mA \tag{11}$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH}\,(mW) = 0.5 \times V_{IN}\,(V) \times I_{INRUSH}\,(mA) = 0.5 \times 3.3\,V \times 15\,mA = 25\,mW \tag{12}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. Figure 9-9 shows the thermal shutdown limit, for 0.025 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 2.2 ms. Therefore, it is safe to use 2.2 ms as the start-up time for this application.

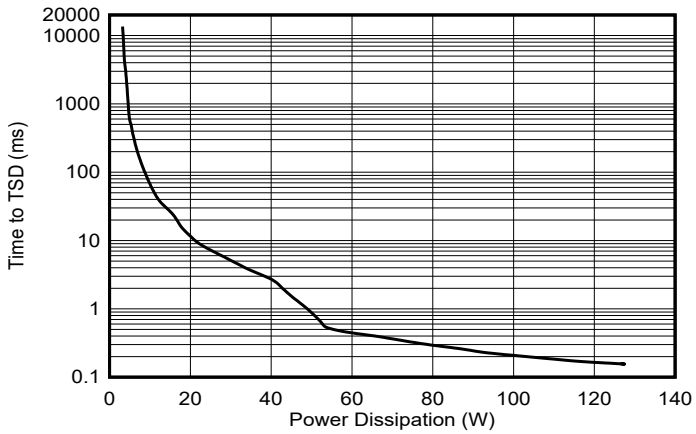


Figure 9-9. Thermal Shutdown Plot During Inrush

9.2.2.3 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (circuit-breaker) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$R_{ILM}\,(\Omega) = \frac{6585}{I_{LIM}\,(A)} = \frac{6585}{6.5\,A} = 1013\ \Omega \tag{13}$$

Choose the nearest 1% standard resistor value as 1 kΩ.

9.2.2.4 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} = \frac{5\,ms \times 2\,\mu A}{1.51\,V} = 6.62\,nF \tag{14}$$

Choose the nearest standard capacitor value as 6.8 nF.

9.2.2.5 Voltage Drop

Table 9-2 shows the power path voltage drop (%) due to the eFuse in QSFP modules of different power classes.

Table 9-2. Voltage Drop Across TPS25981 on QSFP Module Power Rail

POWER CLASS	MAXIMUM POWER CONSUMPTION PER MODULE (W)	MAXIMUM LOAD CURRENT (A)	TYPICAL VOLTAGE DROP (%)
1	1.5	0.454	0.082
2	3.5	1.06	0.192
3	7	2.12	0.385
4	8	2.42	0.440
5	10	3.03	0.551
6	12	3.63	0.660
7	14	4.24	0.771
8	18	5.45	0.991

9.2.3 Application Curves

Figure 9-10. Output Voltage Profile When Optical Module is Inserted

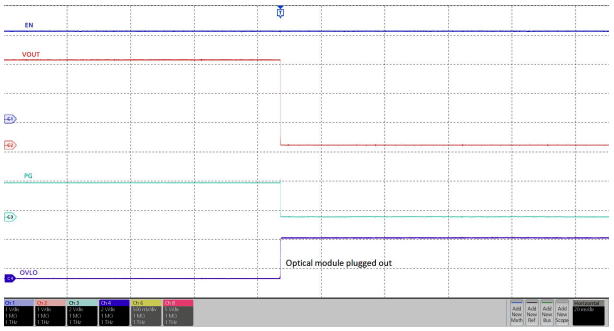


Figure 9-11. Output Voltage Profile When Optical Module is Plugged Out

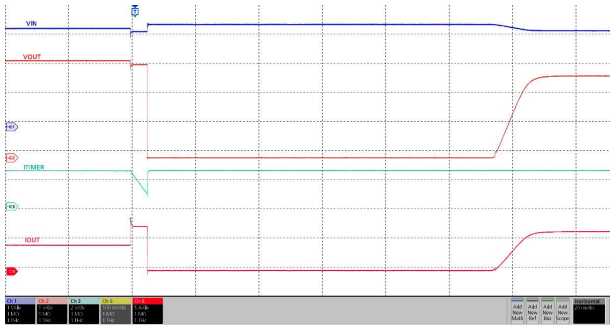


Figure 9-12. Circuit-Breaker with Transient Overcurrent Blanking Interval of 5 ms; Device Restarts in Current Limit Mode

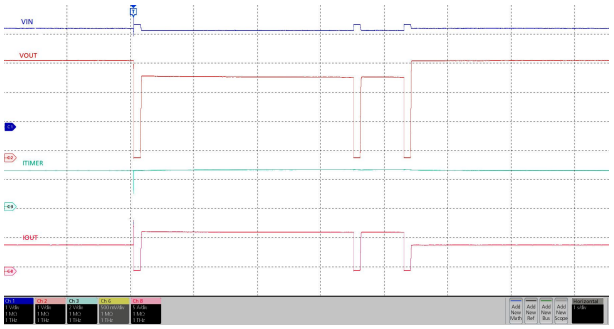


Figure 9-13. Overload Response and Recovery

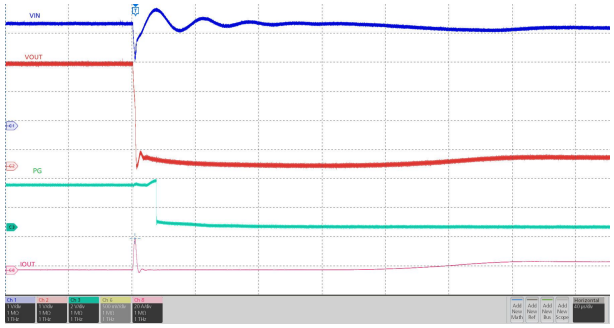


Figure 9-14. Output Hard Short Circuit While ON

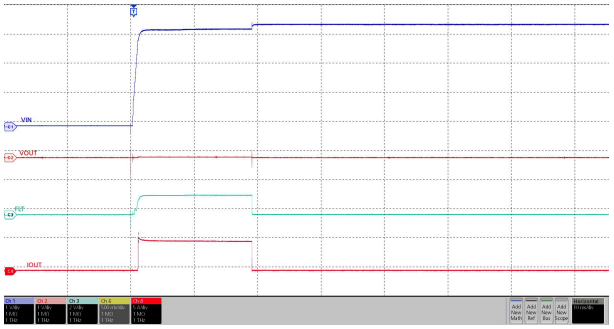


Figure 9-15. Power Up with Short Circuit on Output

10 Power Supply Recommendations

The TPS25981xx devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 16 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  Use Equation 15 to estiamte the approximate value of input capacitance:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

  where

  – V_{IN} is the nominal supply voltage.
  – I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

Figure 10-1 shows the circuit implementation with optional protection components.

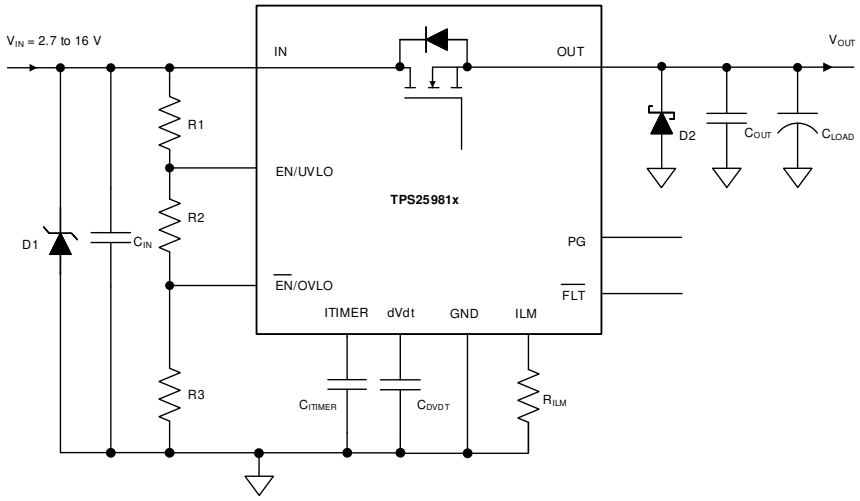


Figure 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, $\overline{EN}$/OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode, bypass-capacitor connection, the OUT pin, and the GND terminal of the IC.

11.2 Layout Example

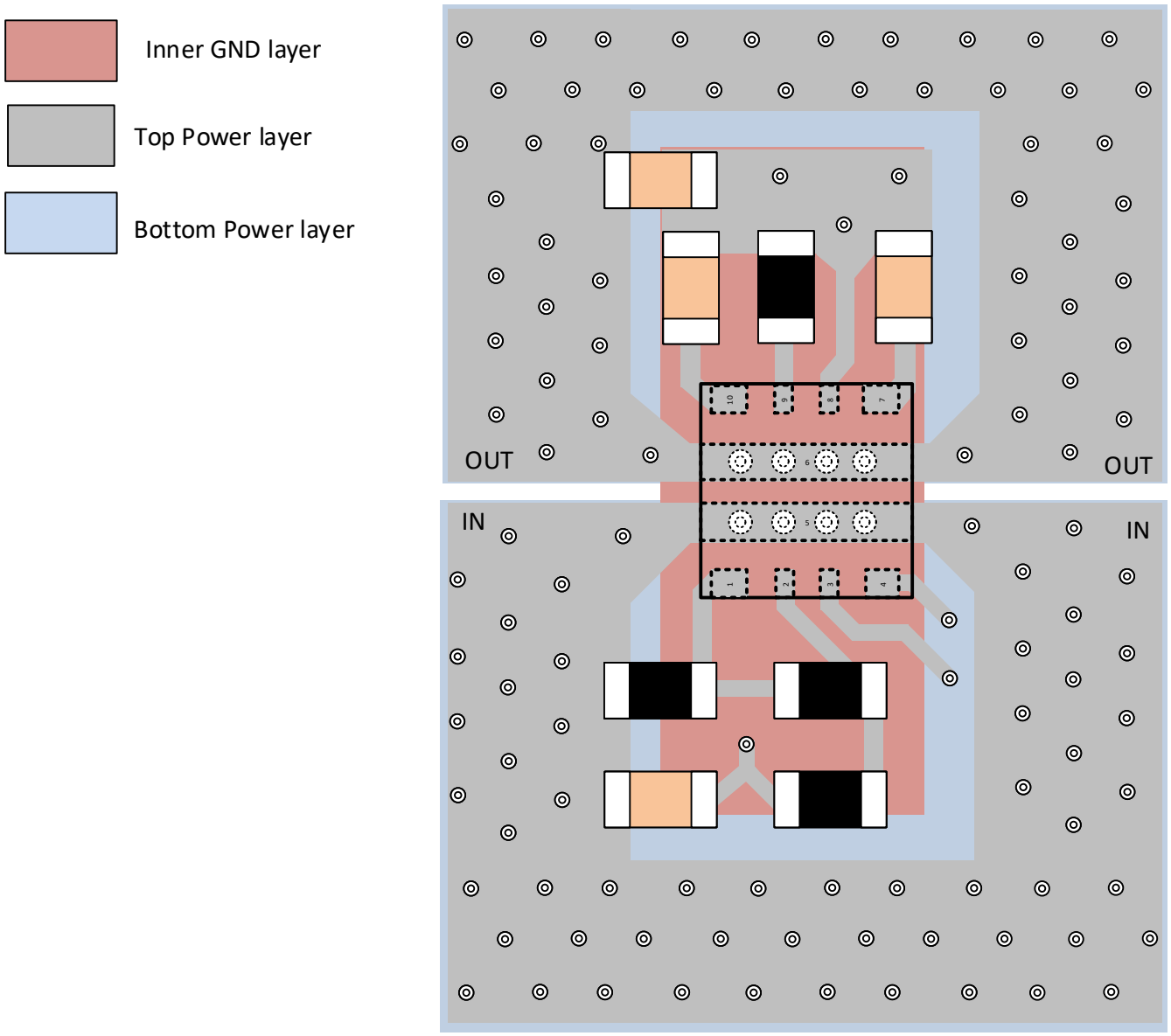


Figure 11-1. Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25981EVM eFuse Evaluation Board*
- Texas Instruments, *TPS25981xx Design Calculator*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259814ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2KWH	Samples
TPS259814LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2KXH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

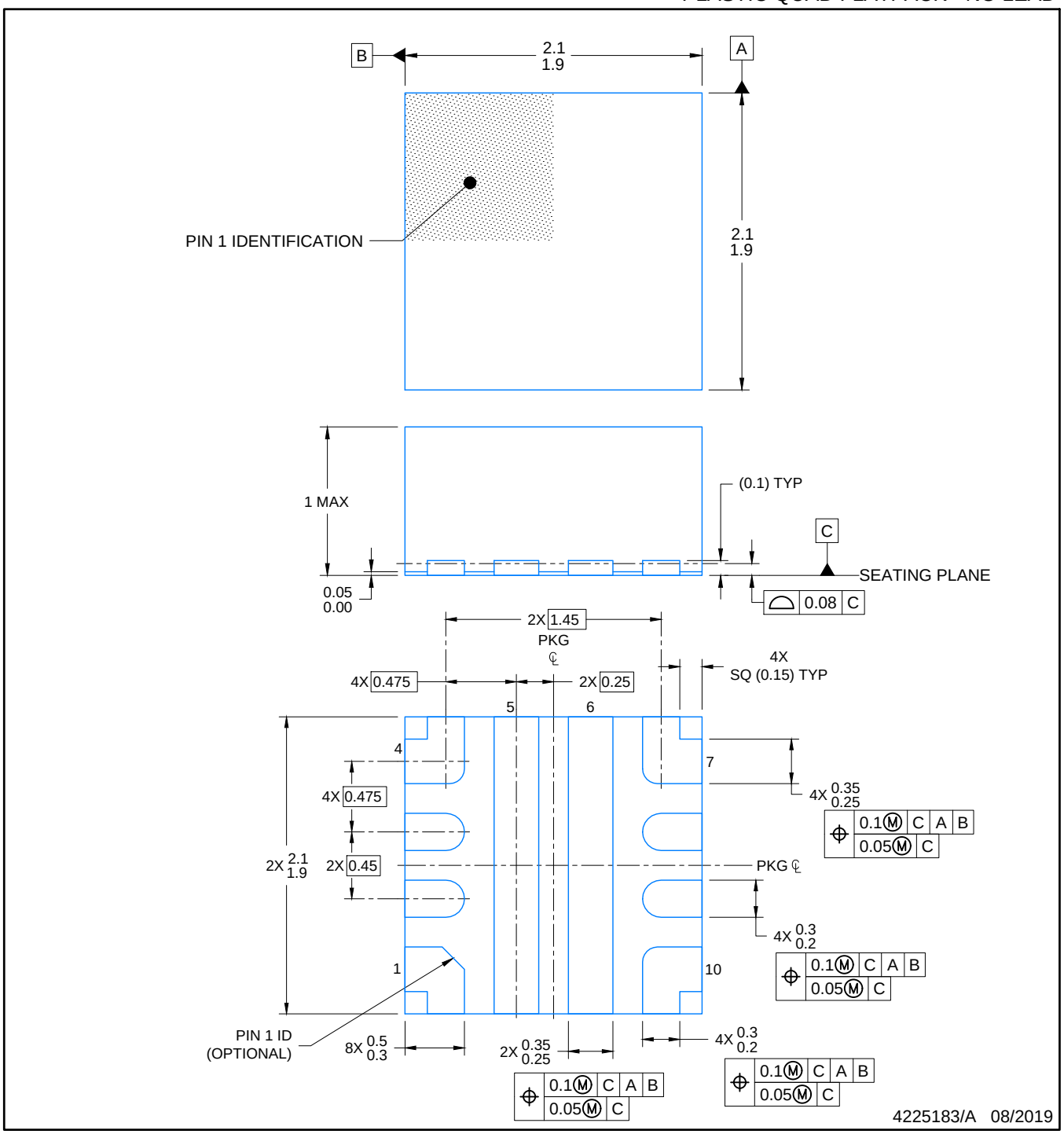
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RPW0010A

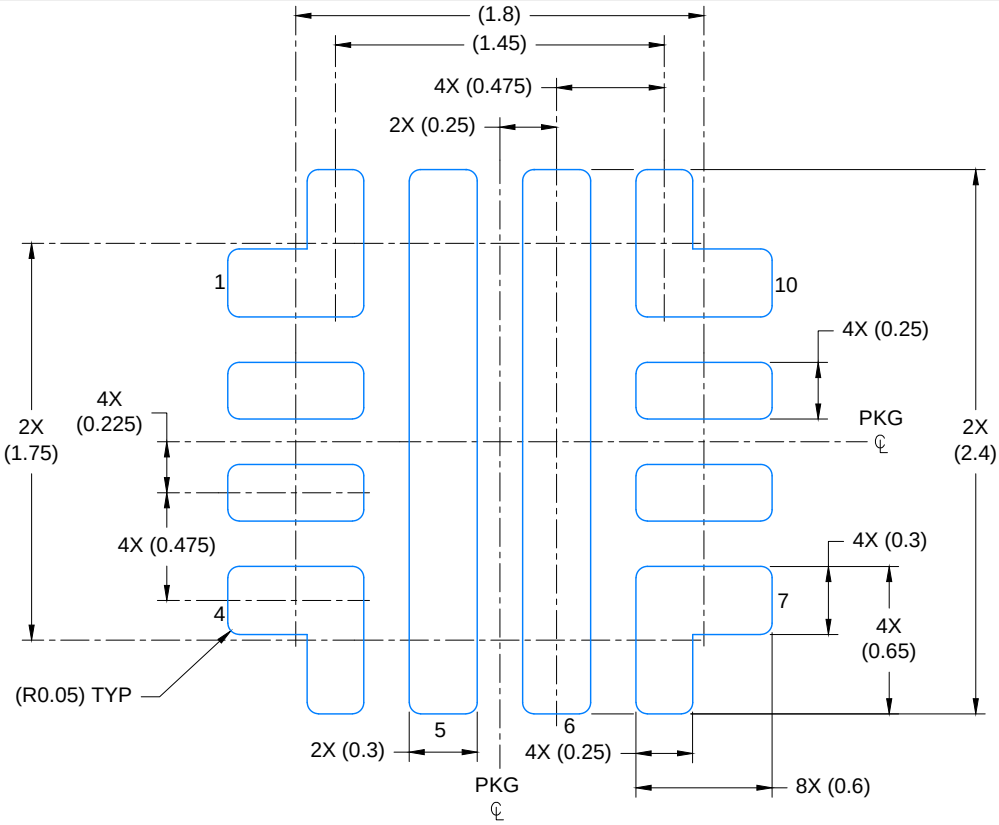
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



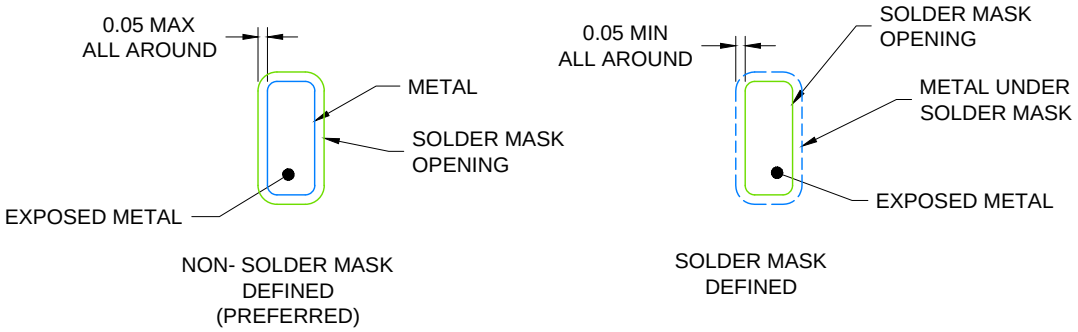
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



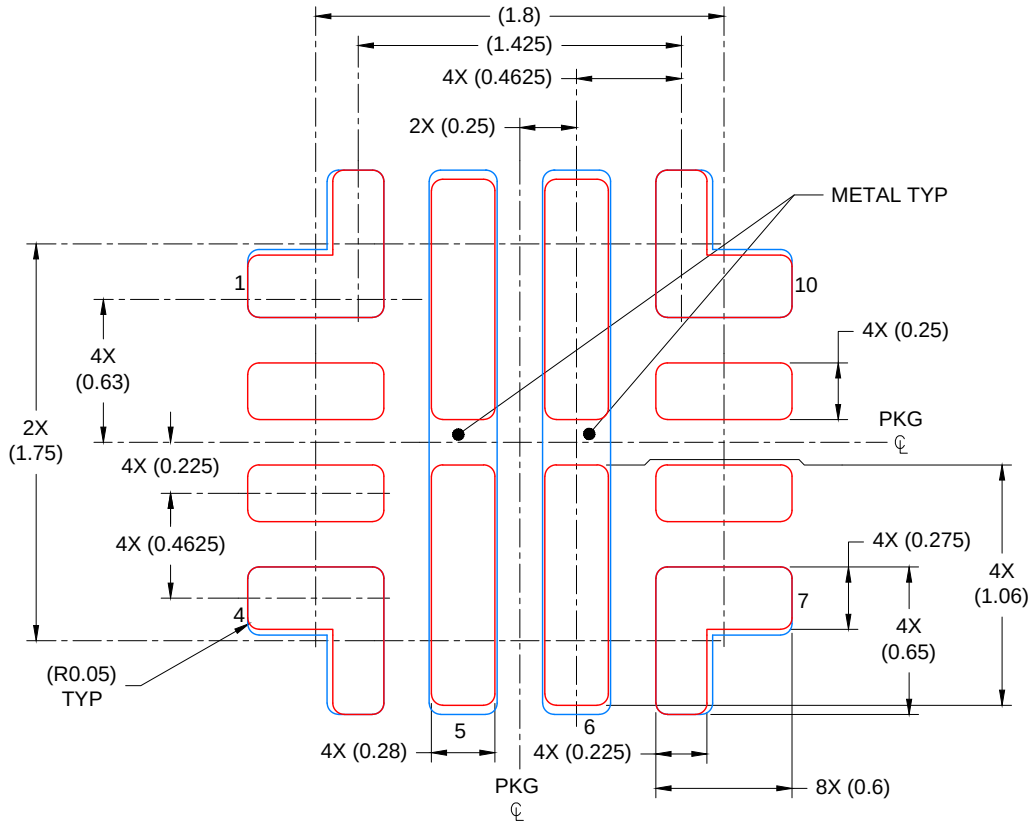
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS25985
SLVSGG3 – MAY 2022

TPS25985x 4.5 V–16 V, 0.59-mΩ, 70-A Stackable eFuse with Accurate and Fast Current Monitor

1 Features

- Input operating voltage range: 4.5 V to 16 V
  - 20-V absolute maximum
  - Withstands negative voltages up to –1 V at output
- Integrated FET with ultra-low on-resistance: 0.59 mΩ (typ.)
- Rated for continuous current of 55 A and peak current of 70 A
- Supports parallel connection of multiple eFuses for higher current support
  - Active device state synchronization and load sharing during start-up and steady-state
- Robust overcurrent protection
  - Adjustable overcurrent threshold (I_{OCP}): 10 A to 60 A with accuracy of ±5%
  - Circuit-breaker response during steady state operation with adjustable transient overcurrent timer (ITIMER) to support peak currents up to 2 × I_{OCP}
  - Adjustable active current limit during start-up (I_{LIM})
- Robust short-circuit protection
  - Fast-trip response (200 ns) to output short-circuit events
  - Adjustable threshold (2 × I_{OCP})
  - Immune to supply line transients — no nuisance tripping
- Precise load current monitoring
  - < 2.1% error over 50%–100% of maximum current
  - > 500-kHz bandwidth
- Fast overvoltage protection (fixed 16.6-V threshold)
- Adjustable output slew rate control (dVdt) for inrush current protection
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Overtemperature Protection (OTP) to ensure FET SOA
  - Guaranteed FET SOA: 12 W√s
- Integrated FET health monitoring and reporting
- Analog die temperature monitor output (TEMP)
- Dedicated fault indication pin ($\overline{FLT}$)
- Power Good indication pin (PG)
- Uncommitted general purpose fast comparator
- Small footprint: QFN 4.5-mm × 5-mm, 0.6-mm pitch
  - 29-mil clearance between power and GND pins

2 Applications

- Input hotswap and hotplug
- Server and High performance computing
- Network interface cards
- Graphics and Hardware accelerator cards
- Datacenter switches and Routers
- Fan trays

3 Description

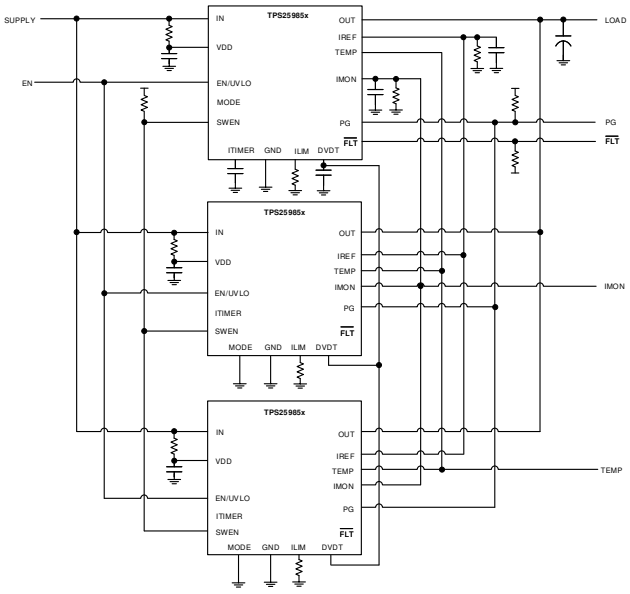
The TPS25985x is an integrated, high-current circuit protection and power management solution in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short-circuits, and excessive inrush current.

Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit level can be set by user as per system needs. A user adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS25985xRQP	QFN (26)	4.5 mm × 5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2022	*	Initial Release

5 Description (continued)

Multiple TPS25985x devices can be connected in parallel to increase the total current capacity for high power systems. All devices actively synchronize their operating state and share current during start-up as well as steady state to avoid over-stressing some of the devices which can result in premature or partial shutdown of the parallel chain.

An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management techniques such as Intel® PSYS™ and PROCHOT to maximize system throughput and power supply utilization.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

6 Pin Configuration and Functions

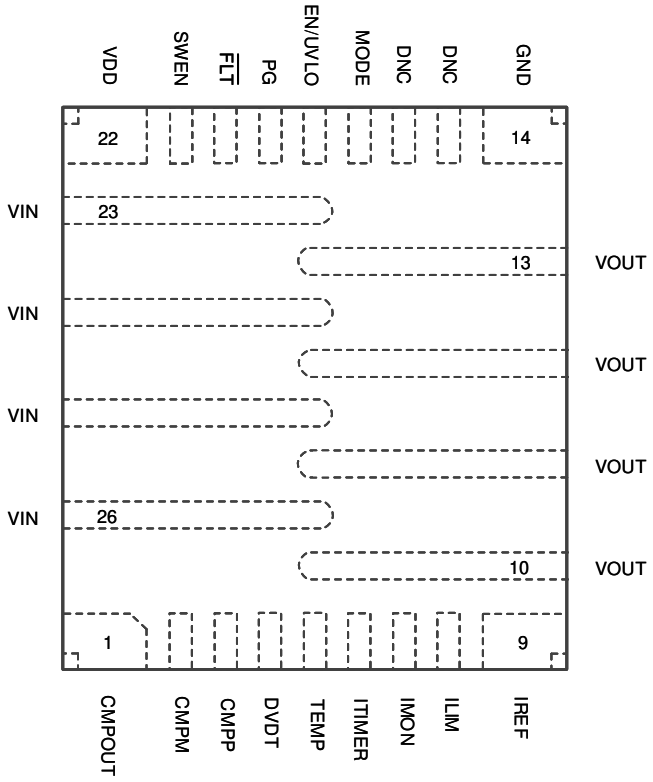


Figure 6-1. TPS25985x RQP Package 26-pin QFN Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CMPOUT	1	O	General purpose comparator open-drain output
CMPM	2	I	General purpose comparator negative input
CMPP	3	I	General purpose comparator positive input
DVDT	4	I/O	Start-up output slew rate control pin. Leave this pin open to allow fastest start-up. Connect capacitor to ground to slow down the slew rate to manage inrush current.
TEMP	5	O	Die junction temperature monitor analog voltage output. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to indicate the peak temperature of the chain.
ITIMER	6	I/O	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed the overcurrent threshold (but lower than fast-trip threshold) during steady-state operation before the device overcurrent response takes action.
IMON	7	O	An external resistor from this pin to GND sets the overcurrent protection threshold and fast-trip threshold during steady-state. This pin also acts as a fast and accurate analog output load current monitor signal during steady-state. *Do not leave floating.*
ILIM	8	O	An external resistor from this pin to GND sets the current limit threshold and fast-trip threshold during start-up. This also sets the active current sharing threshold during steady-state. *Do not leave floating.*

ADVANCE INFORMATION

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
IREF	9	I/O	Reference voltage for overcurrent, short-circuit protection and active current sharing blocks. Can be generated using internal current source and resistor on this pin, or can be driven from external voltage source. *Do not leave floating.*
OUT	10, 11, 12, 13	P	Power output. Must be soldered to output power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
GND	14	G	Device ground reference pin. Connect to system ground.
DNC	15	X	Do not connect anything to this pin.
DNC	16	X	Do not connect anything to this pin.
MODE	17	I	MODE selection pin. Leave the pin floating for standalone and primary mode of operation. Connect the pin to GND to configure device as a secondary device in a parallel chain.
EN/UVLO	18	I	Active high enable input. Connect resistor divider from input supply to set the undervoltage threshold. *Do not leave floating.*
PG	19	I/O	Open-drain active high Power Good indication
$\overline{\text{FLT}}$	20	O	Open-drain active low fault indication
SWEN	21	I/O	Open-drain signal to indicate and control power switch ON/OFF status. This pin facilitates active synchronization between multiple devices in a parallel chain.
VDD	22	P	Controller power input pin. Can be used to power the internal control circuitry with a filtered and stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.
IN	23, 24, 25, 26	P	Power input. Must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}	Maximum Input Voltage Range	IN	–0.3	20	V
V_{DDMAX}	Maximum Supply Voltage Range	VDD	–0.3	20	V
V_{OUTMAX}	Maximum Output Voltage Range	OUT	–1	Min(20 V, VIN + 0.3)	
$V_{IREFMAX}$	Maximum IREF Pin Voltage Range	IREF		5.5	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage Range	DVDT		5.5	V
$V_{MODEMAX}$	Maximum MODE Pin Voltage Range	MODE	Internally Limited		V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage Range	SWEN		5.5	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink Current	SWEN		10	mA
V_{ENMAX}	Maximum Enable Pin Voltage Range	EN/UVLO		20	V
$V_{FLTBMAX}$	Maximum $\overline{FLT}$ Pin Voltage Range	$\overline{FLT}$		5.5	V
$I_{FLTBMAX}$	Maximum $\overline{FLT}$ Pin Sink Current	$\overline{FLT}$		10	mA
V_{PGMAX}	Maximum PG Pin Voltage Range	PG		5.5	V
I_{PGMAX}	Maximum PG Pin Sink Current	PG		10	mA
$V_{CMPPMAX}$	Maximum CMPP Pin Voltage Range	CMPP		5.5	V
$V_{CMPMMAX}$	Maximum CMPM Pin Voltage Range	CMPM		5.5	V
$V_{CMPOUTMAX}$	Maximum CMPOUT Pin Voltage Range	CMPOUT		5.5	V
$I_{CMPOUTMAX}$	Maximum CMPOUT Pin Sink Current	CMPOUT		10	mA
$V_{TEMPMAX}$	Maximum TEMP Pin Voltage Range	TEMP		5.5	V
$V_{ILIMMAX}$	Maximum ILIM pin voltage	ILIM	Internally Limited		V
$V_{IMONMAX}$	Maximum IMON pin voltage	IMON	Internally Limited		V
$V_{ITIMERMAX}$	Maximum ITIMER pin voltage	ITIMER	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Soldering Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	4.5	16	V
V_{DD}	Supply Voltage Range	VDD	4.5	16	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5	V
V_{dVdT}	dVdT Pin Cap Voltage Rating	dVdT	4		V
V_{PG}	PG Pin Pull-up Voltage Range	PG		5	V
V_{FLTB}	$\overline{FLT}$ Pin Pull-up Voltage Range	$\overline{FLT}$		5	V
V_{CMPOUT}	CMPOUT Pin Pull-up Voltage Range	CMPOUT		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN	2.5	5	V
V_{ITIMER}	ITIMER Pin Cap Voltage Rating	ITIMER	4		V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
V_{CMPx}	CMPP, CMPM Common mode voltage rage	CMPP, CMPM	0.3	1.5	V
I_{MAX}	Continuous Switch Current	IN to OUT		55	A
$I_{MAX, PLS}$	Peak Output Current (2.5 ms with 10% duty cycle), $T_J \leq$ 125°C	IN to OUT		70	A
T_J	Junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1) (2)		TPS25985X RQP (QFN) 26 PINS	UNIT
$R_{\theta JA(eff)}$	Junction-to-ambient thermal resistance (effective)	19.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 8-layer PCB (4s4p)

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{DD}	VDD input operating voltage range		4.5		16	V
$I_{QON(VDD)}$	VDD ON state quiescent current	$V_{VDD} > V_{UVP(R)}$, $V_{EN} \geq V_{UVLO(R)}$		0.45		mA
$I_{QOFF(VDD)}$	VDD OFF state current	$V_{EN} < V_{UVLO(F)}$		87		µA
$V_{UVP(R)}$	VDD undervoltage protection threshold	VDD Rising		4.20		V
$V_{UVP(F)}$	VDD undervoltage protection threshold	VDD Falling		4.05		V
INPUT SUPPLY (IN)						

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	VIN input operating voltage range		4.5		16	V
$V_{UVPIN(R)}$	V_{IN} undervoltage protection threshold	V_{IN} Rising		4.24		V
$V_{UVPIN(F)}$	V_{IN} undervoltage protection threshold	V_{IN} Falling		4.09		V
$I_{QON(IN)}$	IN ON state quiescent current	$V_{EN} \geq V_{UVLO(R)}$		2.8		mA
$I_{QOFF(IN)}$	IN OFF state current	$V_{EN} < V_{UVLO(F)}$		2		µA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO pin voltage rising threshold for turning on	EN/UVLO Rising		1.2		V
$V_{UVLO(F)}$	EN/UVLO pin voltage falling threshold for turning off and engaging output discharge (primary device)	EN/UVLO Falling, MODE = Open		1.1		V
	EN/UVLO pin voltage threshold for turning off and engaging QOD (secondary device)	EN/UVLO Falling, MODE = GND		1.0		V
$V_{SD(F)}$	EN/UVLO pin voltage threshold for entering full shutdown	EN/UVLO Falling		0.8		V
I_{ENLKG}	EN/UVLO pin leakage current				0.1	µA
OVERVOLTAGE PROTECTION (IN)						
$V_{OVP(R)}$	Input overvoltage protection threshold (rising)	V_{IN} rising		16.6		V
$V_{OVP(F)}$	Input overvoltage protection threshold (falling)	V_{IN} falling		16.5		V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON resistance	T_J = 25℃		0.586		mΩ
		T_J = –40 to 125℃			1	mΩ
OVERCURRENT PROTECTION REFERENCE (IREF)						
I_{IREF}	IREF pin internal sourcing current			25		µA
CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	ILIM current monitor gain (ILIM:IOUT)			18.18		µA/A
$CL_{REF(SAT)\%}$	Ratio of start-up current limit threshold (ILIM) to steady-state overcurrent protection threshold reference (IREF)	$V_{OUT} > V_{FB}$, PG not asserted		23.7		%
I_{LIM}	Start-up current limit regulation threshold	R_{ILIM} = 385 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$		40.7		A
		R_{ILIM} = 440 Ω, V_{IREF} = 1..2 V, $V_{OUT} > V_{FB}$		35.6		A
		R_{ILIM} = 1100 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$		14.2		A
		R_{ILIM} = 1540 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$		10		A
		R_{ILIM} = 2200 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$		7		A
V_{FB}	Foldback voltage			2.0		V
OUTPUT CURRENT MONITOR AND OVERCURRENT PROTECTION (IMON)						
G_{IMON}	IMON current monitor gain (IMON:IOUT)	Device in steady state (PG asserted)		18.18		µA/A
I_{OCP}	Steady-state overcurrent protection (Circuit-Breaker) threshold	R_{IMON} = 1100 Ω, V_{IREF} = 1.2 V		60		A
		R_{IMON} = 1320 Ω, V_{IREF} = 1.2 V		50.05		A
		R_{IMON} = 2640 Ω, V_{IREF} = 1.2 V		25.06		A
		R_{IMON} = 6600 Ω, V_{IREF} = 1.2 V		10		A
TRANSIENT OVERCURRENT BLANKING TIMER (ITIMER)						

ADVANCE INFORMATION

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ITIMER}	ITIMER pin internal discharge current	I_{OUT} > I_{OCP}, ITIMER ↓		2.07		µA
R_{ITIMER}	ITIMER pin internal pull-up resistance			13.8		kΩ
V_{INT}	ITIMER pin internal pull-up voltage	I_{OUT} < I_{OCP}		3.66		V
$V_{ITIMERTHR}$	ITIMER comparator falling threshold	I_{OUT} > I_{OCP}, ITIMER ↓		2.16		V
ΔV_{ITIMER}	ITIMER discharge voltage threshold	I_{OUT} > I_{OCP}, ITIMER ↓		1.5		V
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast-trip threshold in steady-state	PG asserted High, Standalone/Primary mode, MODE = Open		151		A
		PG asserted High, Secondary mode, MODE = GND		227		A
$SFT_{REF(LIN)\%}$	Scalable fast-trip threshold (IMON) to overcurrent protection threshold reference (IREF) ratio during steady-state	Standalone/Primary mode, MODE = Open		200		%
		Secondary mode, MODE = GND		225		%
$SFT_{REF(SAT)\%}$	Scalable fast-trip threshold (ILIM) to overcurrent protection threshold reference (IREF) ratio during start-up	Standalone/Primary mode, MODE = Open		49.5		%
		Secondary mode, MODE = GND		49.6		%
$R_{ON(ACS)}$	Maximum R_{DSON} during active current sharing	V_{ILIM} > $CL_{REF(ACS)\%}$ × V_{IREF}		0.75		mΩ
$G_{IMON(ACS)}$	IMON:IOUT ratio during active current sharing	PG asserted High, V_{ILIM} > $CL_{REF(ACS)\%}$ × V_{IREF}		18.33		µA/A
$CL_{REF(ACS)\%}$	Ratio of active current sharing trigger threshold to steady state overcurrent protection threshold	PG asserted High		36.67		%
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	dVdt pin charging current	Primary/Standalone mode, MODE = Open		2.03		µA
G_{DVDT}	dVdt gain			20.53		V/V
R_{DVDT}	dVdt pin to GND discharge resistance			523		Ω
$R_{ON(GHI)}$	R_{DSON} when PG is asserted			0.72		mΩ
COMPARATOR INPUTS (CMPP, CMPM)						
$V_{CM(CMP)}$	CMPx common mode voltage range		0.3		1.5	
I_{CMPx}	CMPx pin leakage current	0.3 V < V_{CMPx} < 1.5 V			0.1	µA
QUICK OUTPUT DISCHARGE (QOD)						
I_{QOD}	Quick output discharge internal pull-down current	$V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$, –40 < T_J < 125°C		20.9		mA
TEMPERATURE SENSOR OUTPUT (TEMP)						
G_{TMP}	TEMP sensor gain			2.72		mV/°C
V_{TMP}	TEMP pin output voltage	T_J = 25°C		677.6		mV
I_{TMPSRC}	TEMP pin sourcing current			92.6		µA
I_{TMPSNK}	TEMP pin sinking current			10.1		µA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Thermal shutdown threshold	T_J Rising		150		°C
TSD_{HYS}	Thermal shutdown hysteresis	T_J Falling		12.5		°C
FET HEALTH MONITOR						

ADVANCE INFORMATION

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DSFLT}	FET D-S fault threshold	SWEN = L		0.49		V
SINGLE POINT FAILURE (ILIM, IMON, IREF, ITIMER)						
$I_{OC\_BKP(LIN)}$	Back-up overcurrent protection threshold (steady -steady)			93.8		A
$I_{OC\_BKP(SAT)}$	Back-up overcurrent protection threshold (start-up)			90.3		A

7.6 Logic Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWEN						
R_{SWEN}	SWEN pin pull-down resistance	SWEN de-asserted Low		9		Ω
$I_{SWENLKG}$	SWEN pin leakage current	SWEN asserted High			2	µA
V_{IH_SWEN}	SWEN input logic high				1.4	V
V_{IL_SWEN}	SWEN input logic low		0.4			V
FAULT INDICATION (FLTB)						
R_{FLTB}	$\overline{FLT}$ pin pull-down resistance	$\overline{FLT}$ asserted Low		9		Ω
$I_{FLTBLKG}$	$\overline{FLT}$ pin leakage current	$\overline{FLT}$ de-asserted High			2	µA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low		9		Ω
I_{PGKG}	PG pin leakage current	PG asserted High			2	µA
COMPARATOR OUTPUT (CMPOUT)						
R_{CMPOUT}	CMPOUT pin pull-down resistance	CMPOUT de-asserted Low		19		Ω
I_{CMPOUT}	CMPOUT pin leakage current	CMPOUT asserted High			2	µA

7.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{IN} > $V_{OVP(R)}$ to SWEN↓		1.5		µs
t_{INSDLY}	Insertion delay	V_{DD} > $V_{UVP(R)}$ to SWEN↑		13		ms
t_{FFT}	Fixed Fast-Trip response time	I_{OUT} > 1.5 × I_{FFT} to I_{OUT}↓		200		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 × I_{OCP} to I_{OUT}↓		400		ns
t_{CMP}	General purpose comparator response time			400		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 × I_{OCP}, C_{ITIMER} = Open		0		ms
		I_{OUT} = 1.5 × I_{OCP}, C_{ITIMER} = 4.7 nF		3.5		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant, Primary mode (MODE = Open)		100		ms
$t_{EN(DG)}$	EN/UVLO de-glitch time			10		µs
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		200		ms
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	$V_{SD(F)}$ < $V_{EN/UVLO}$ < $V_{UVLO(F)}$, C_{OUT} = 1 mF		550		ms
t_{QOD}	QOD enable timer	$V_{SD(F)}$ < $V_{EN/UVLO}$ < $V_{UVLO(F)}$		4.5		ms
t_{PGA}	PG assertion delay			20		us

ADVANCE INFORMATION

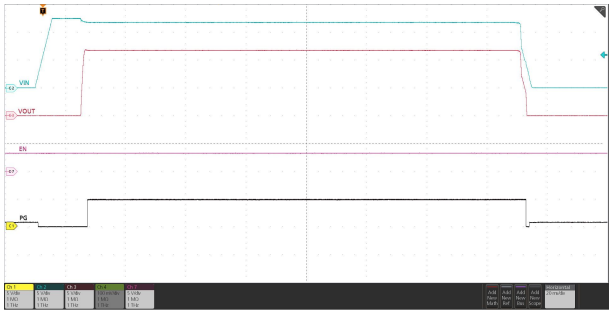
7.8 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. V_{IN} = 12 V, R_{OUT} = 500 Ω, C_{OUT} = 1 mF

PARAMETER		C_{dVdt} = 3.3 nF	C_{dVdt} = 33 nF	UNITS
SR_{ON}	Output rising slew rate	9.79	1.20	V/ms
$t_{D,ON}$	Turn-on delay	0.34	1.54	ms
t_R	Rise time	1.00	8.13	ms
t_{ON}	Turn-on time	1.38	10.35	ms
$t_{D,OFF}$	Turn-off delay	1081	1060	µs
t_F	Fall time	Depends on R_{OUT} and C_{OUT}		µs

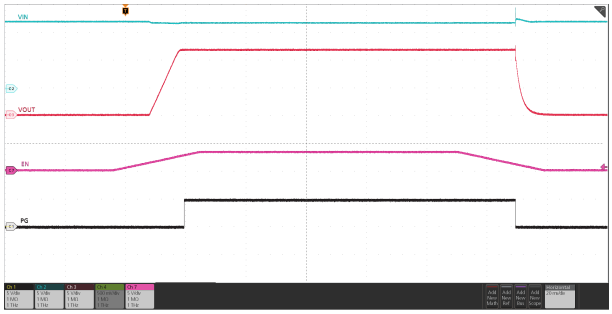
ADVANCE INFORMATION

7.9 Typical Characteristics



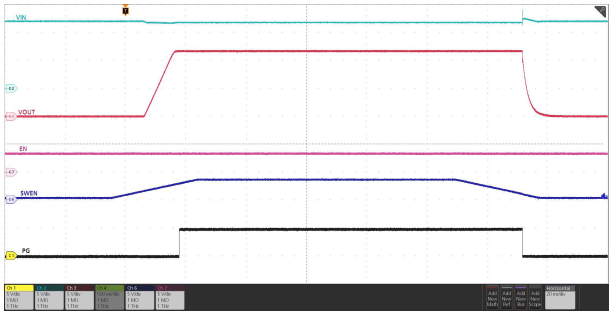
EN held high, input supply ramped up and down

Figure 7-1. Power Up and Down Sequencing Using Input Supply



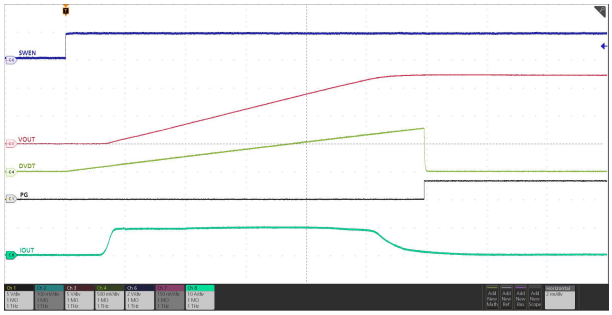
Input supply held steady, EN/UVLO pin toggled high and low

Figure 7-2. Power Up and Down Sequencing Using EN/UVLO Pin



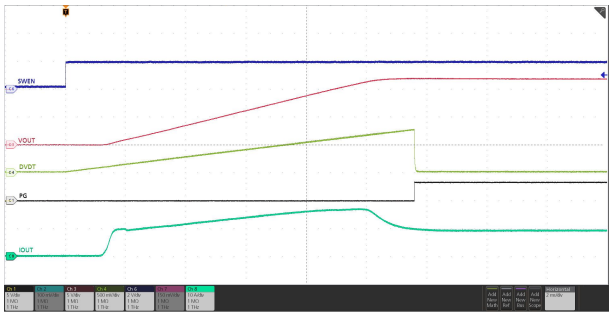
Input supply held steady, EN/UVLO pin held high, SWEN pin toggled high and low

Figure 7-3. Power Up and Down Sequencing Using SWEN Pin



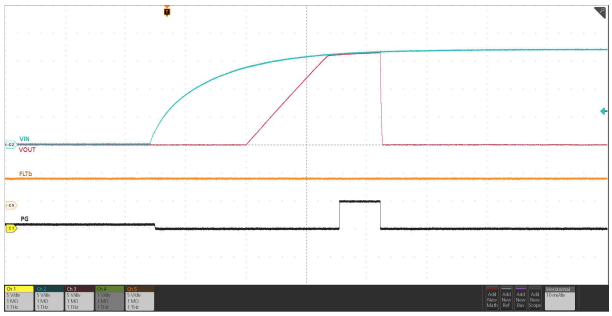
C_{OUT} = 6.8 mF, C_{dVdt} = 33 nF

Figure 7-4. Inrush Current Control with Capacitive Load



C_{OUT} = 6.8 mF, R_{OUT} = 1.2 Ω, C_{dVdt} = 33 nF

Figure 7-5. Inrush Current Control with Capacitive and Resistive Load

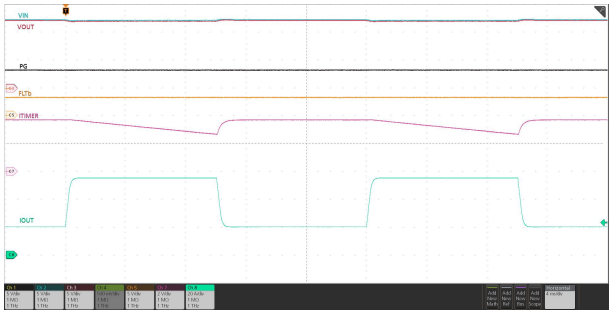


Input supply ramped up above 16.6 V

Figure 7-6. Input Overvoltage Protection Response

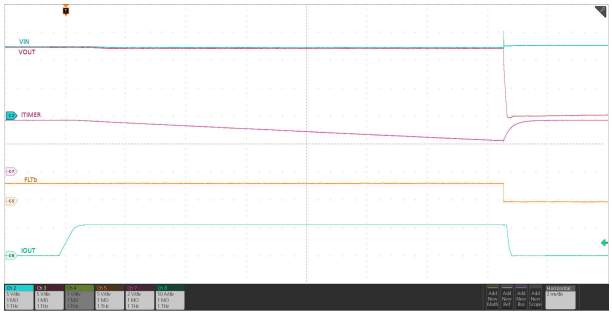
ADVANCE INFORMATION

7.9 Typical Characteristics (continued)



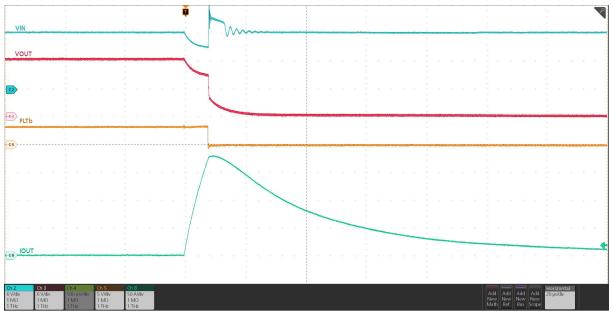
I_{OCP} = 50 A, t_{ITIMER} = 14 ms, I_{OUT} pulsed above the I_{OCP} threshold for short duration without triggering circuit-breaker response

Figure 7-7. Peak Current Support Using Transient Overcurrent Blanking



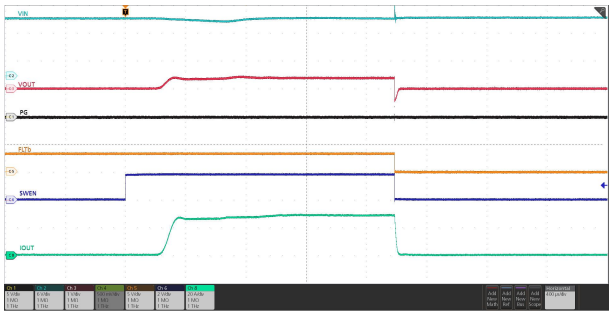
I_{OCP} = 50 A, t_{ITIMER} = 14 ms, I_{OUT} stays above the I_{OCP} threshold persistently to trigger circuit-breaker response

Figure 7-8. Overcurrent Protection Response (Circuit-Breaker)



I_{OCP} = 50 A, Output hard-short to GND while in steady. I_{OUT} rises above 2 × I_{OCP} triggers fast-trip response

Figure 7-9. Short-Circuit Protection Response



Device turned on using SWEN with output hard-short to GND. Device limits the current with foldback.

Figure 7-10. Power Up into Short-Circuit

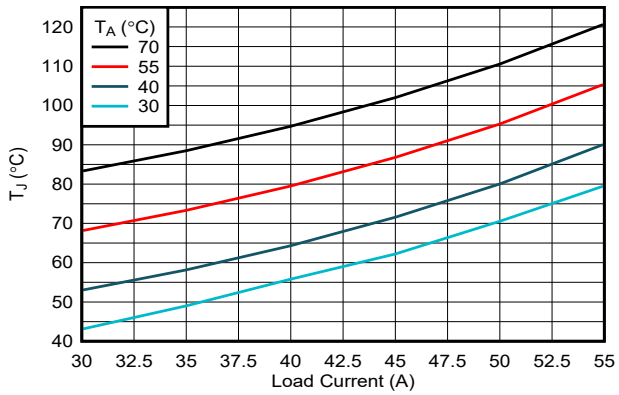


Figure 7-11. Junction Temperature vs Load Current (No Air-Flow)

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS25985x is an eFuse with integrated power switch that is used to manage load voltage and load current. The device starts its operation by monitoring the VDD and IN bus. When V_{DD} and V_{IN} exceed the respective Undervoltage Protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next the device samples the EN/UVLO pin and SWEN pins. A high level on both these pins enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When either EN/UVLO or SWEN is held low, the internal MOSFET is turned off.

After a successful start-up sequence, the TPS25985x device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the programmed overcurrent threshold is not exceeded and input overvoltage spikes are cut off. This action keeps the system safe from harmful levels of voltage and current. At the same time, a user-adjustable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This feature ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

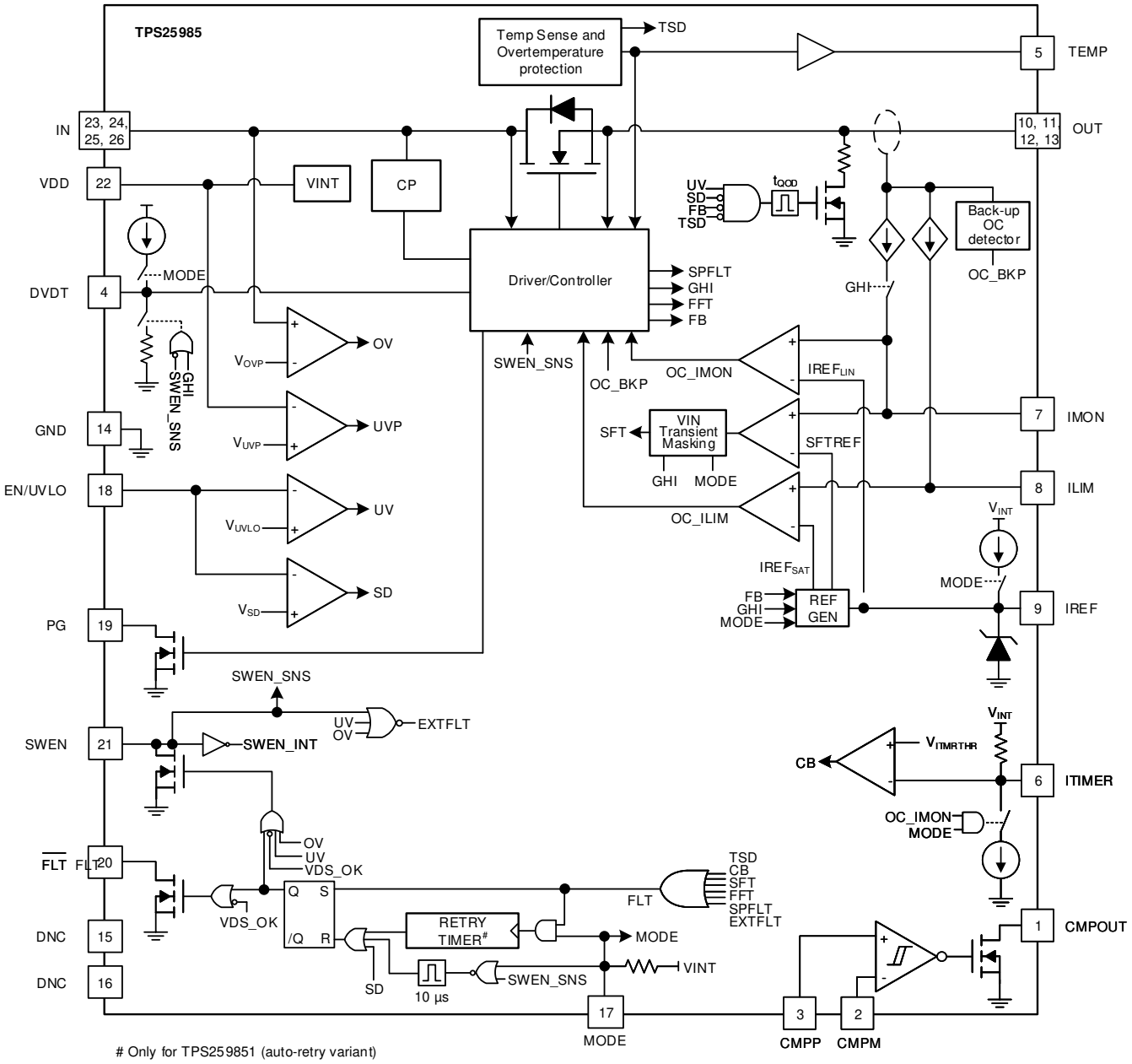
The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This feature facilitates the implementation of advanced dynamic platform power management techniques such as Intel® PSYS™ to maximize system power usage and throughput without sacrificing safety and reliability.

For systems needing higher load current support, multiple TPS25985x eFuses can be connected in parallel. All devices share current during start-up as well as steady-state to avoid over-stressing some of the devices more than others which can result in premature or partial shutdown of the parallel chain. The devices synchronize their operating states to ensure graceful startup, shutdown and response to faults. This makes the whole chain function as a single very high current eFuse rather than a bunch of independent eFuses operating asynchronously.

The device has integrated protection circuits to ensure device safety and reliability under recommended operating conditions. The internal FET SOA is protected at all times using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (T_J) becomes too high for the FET to operate safely.

ADVANCE INFORMATION

8.2 Functional Block Diagram



Only for TPS259851 (auto-retry variant)

8.3 Feature Description

The TPS25985x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Protection

The TPS25985x implements undervoltage lockout on VDD and VIN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage lockout has a default internal threshold of V_{UVP} on VDD and V_{UVPIN} on VIN. Alternatively, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 8-1 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

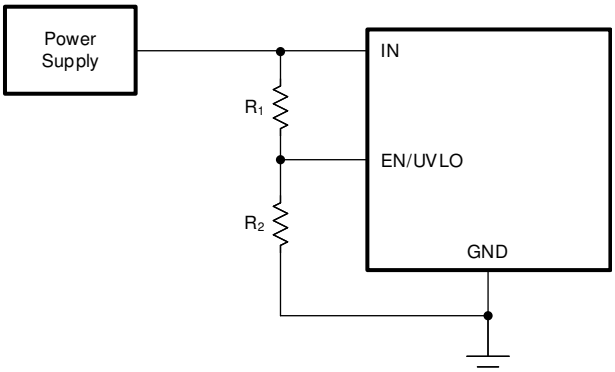


Figure 8-1. Adjustable Undervoltage Protection

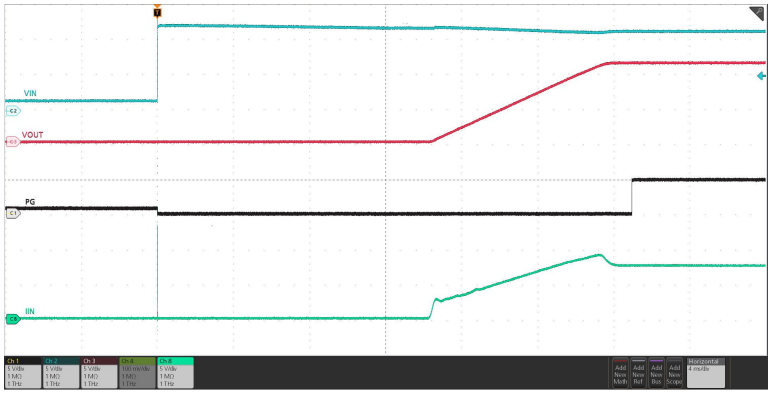
$$V_{IN(UV)} = V_{UVLO(R)}\frac{R_1 + R_2}{R_2} \quad (1)$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for > t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and it retains no digital state memory. It also resets any latched faults. In this condition, the device quiescent current consumption is minimal.

8.3.2 Insertion Delay

The TPS25985x implements insertion delay at start-up to ensure the supply has stabilized before the device tries to turn on the power to the load. The device initially waits for the VDD supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, the device remains off for an additional delay of t_{INSDLY} irrespective of the EN/UVLO pin condition. This action helps to prevent any unexpected behavior in the system if the device tries to turn on before the card has made firm contact with the backplane or if there is any supply ringing or noise during start-up.



Input supply stepped up from 0 V to 12 V. Device waits for t_{INSDLY} for input supply to stabilize before it turns on the output.

Figure 8-2. Insertion Delay

8.3.3 Overvoltage Protection

The TPS25985x implements overvoltage lockout to protect the load from input overvoltage conditions. The OVP comparator on the IN pin uses a fixed internal overvoltage protection threshold. If the input voltage on IN exceeds the OVP rising threshold ($V_{OVP(R)}$), the power FET is turned OFF within t_{OVP}. After the voltage on IN falls below the OVP falling threshold ($V_{OVP(F)}$), the FET is turned ON in a dVdt controlled manner.

ADVANCE INFORMATION

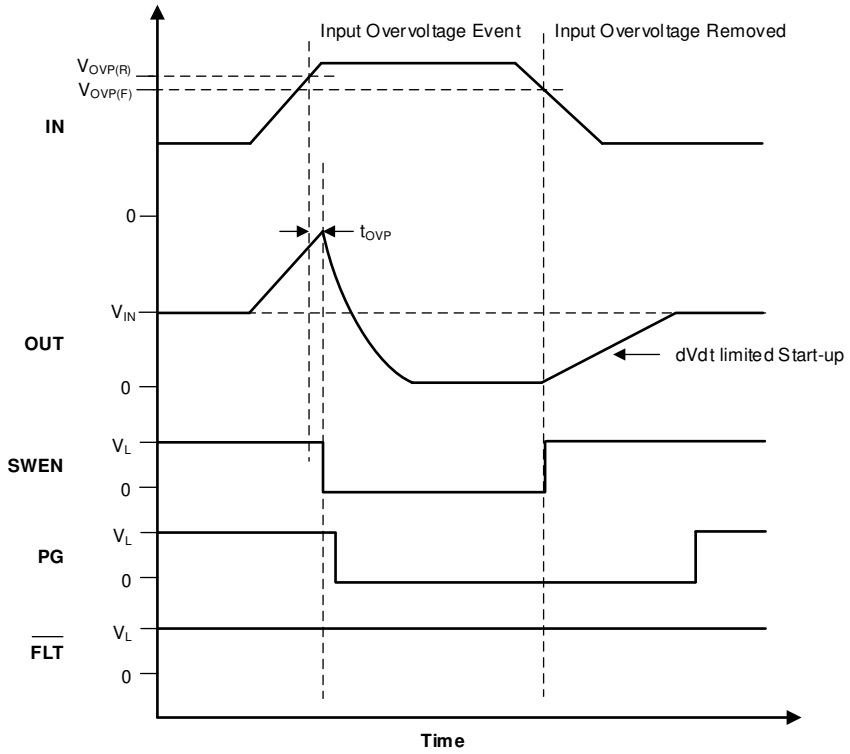


Figure 8-3. Input Overvoltage Protection Response

8.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25985x incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Active current limit with an adjustable threshold (I_{LIM}) for overcurrent protection during start-up
3. Circuit-breaker with an adjustable threshold (I_{OCP}) and blanking timer (t_{ITIMER}) for overcurrent protection during steady-state
4. Fast-trip response to severe overcurrent faults with an adjustable threshold (I_{SFT} = 2 × I_{OCP}) to quickly protect against severe short-circuits under all conditions, as well as a fixed threshold (I_{FFT}) during steady state

8.3.4.1 Slew rate (dVdt) and Inrush Current Control

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, the inrush current can damage the input connectors and cause the system power supply to droop. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (2)$$

A capacitor can be added to the dVdt pin to control the rising slew rate and lower the inrush current during turn-on. The required CdVdt capacitance to produce a given slew rate can be calculated using Equation 3.

$$C_{DVDT}(pF) = \frac{42000}{SR(V/ms)} \quad (3)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

1. High input slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:
   a. Reduce the input inductance.
   b. Increase the capacitance on VIN pin.
   c. Increase the dVdt pin capacitance to reduce the slew rate or increase the start-up time. TI recommends using a minimum start-up time of 5 ms.

8.3.4.1.1 Start-Up Time Out

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after SWEN is asserted, the device registers it as a fault. $\overline{FLT}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the device configuration.

8.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS25985x responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also ensures robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 4.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (4)$$

Where G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT})

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- In the standalone or primary mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage. It is also possible to drive the IREF pin from an external low impedance reference voltage source as shown in Equation 5.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (5)$$

- In a primary and secondary parallel configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}) for all the secondary devices in the chain.

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using Equation 6.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (6)$$

Note

Maintain V_{IREF} within the recommended voltage range to ensure proper operation of the overcurrent detection circuit.

TI recommends to add a 150-pF capacitor from IREF pin to GND for improved noise immunity.

After an overcurrent condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (2 × I_{OCP}), the device starts discharging the ITIMER pin capacitor using an internal 2-µA pulldown current. If the load current drops below the current limit threshold before the ITIMER capacitor discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor

ADVANCE INFORMATION

continues to discharge and once it falls by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the ITIMER cap is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. Equation 7 can be used to calculate the R_{IMON} value for the desired overcurrent threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \quad (7)$$

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculated using Equation 8.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (8)$$

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay. However, this makes the circuit-breaker response extremely sensitive to noise and may cause false tripping during load transients.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the quiescent current – not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval. However, it also extends the time needed for the ITIMER cap to recharge up to V_{INT} before the next overcurrent event. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it takes less time to discharge to the VITIMER threshold, thereby it provides a shorter blanking interval than intended.

Figure 8-4 illustrates the overcurrent response for TPS25985x eFuse. After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS259850 variant) or restarts automatically after a fixed delay (TPS259851 variant).

ADVANCE INFORMATION

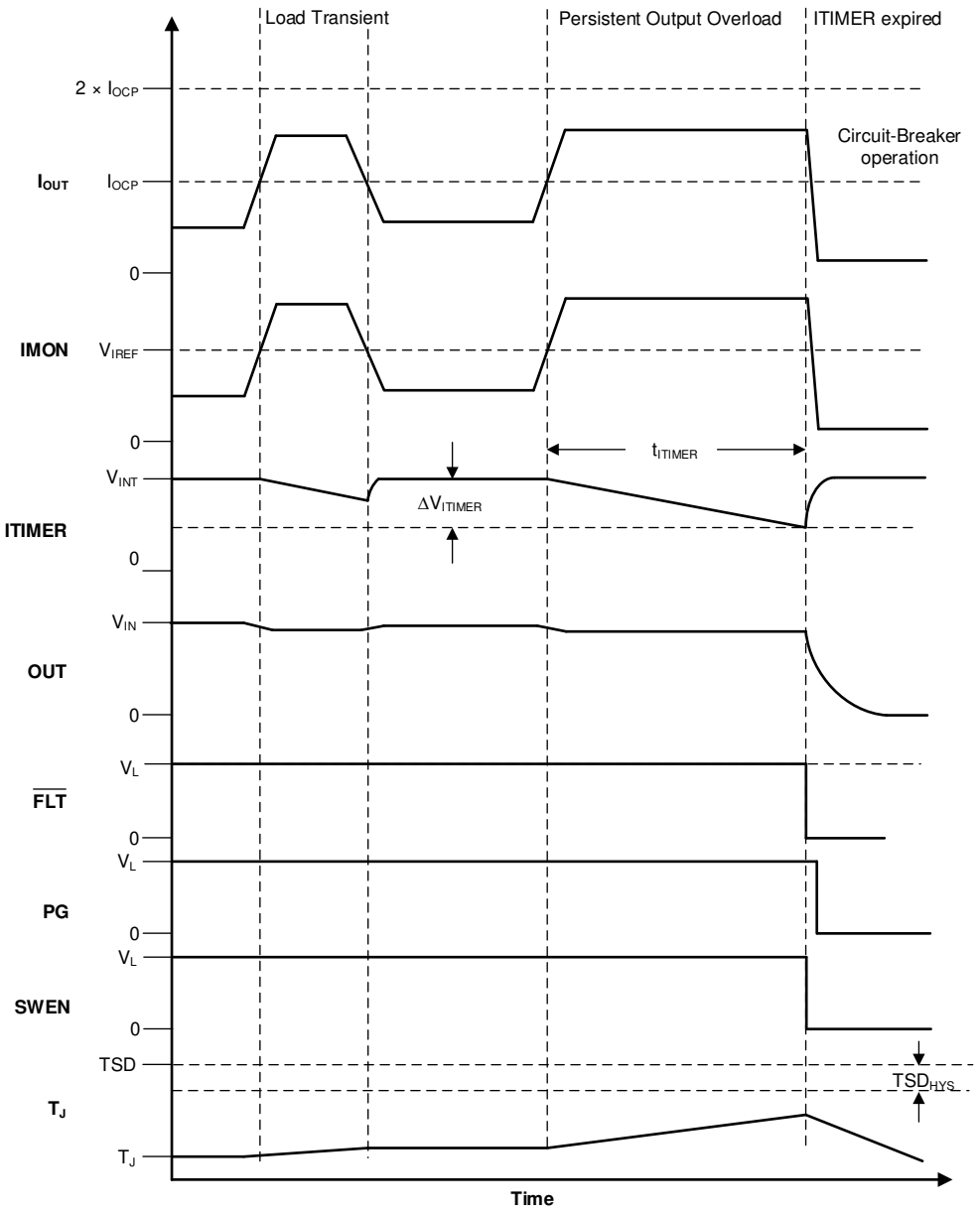


Figure 8-4. Steady-State Overcurrent (Circuit-Breaker) Response

8.3.4.3 Active Current Limiting During Start-Up

The TPS25985x responds to output overcurrent conditions during start-up by actively limiting the current. The device constantly senses the current flowing through each one (I_{DEVICE}) and provides an analog current output (I_{ILIM}) on the ILIM pin, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) as per Equation 9.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (9)$$

Where G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE})

The overcurrent condition is detected by comparing this voltage against a threshold which is a scaled voltage ($CLREF_{SAT}$) derived from the reference voltage (V_{IREF}) on the IREF pin as presented in Equation 10.

$$CLREF_{SAT} = \frac{0.7 \times V_{IREF}}{3} \quad (10)$$

ADVANCE INFORMATION

The reference voltage (V_{IREF}) can be controlled in two ways, which sets the start-up current limit threshold (I_{LIM}) accordingly.

1. In the standalone mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage as shown in Equation 11.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (11)$$

2. In a primary and secondary configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}).

The active current limit (I_{LIM}) threshold during start-up can be calculated using Equation 12.

$$I_{ILIM} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \quad (12)$$

When the load current during start-up exceeds I_{LIM}, the device tries to regulate and hold the load current at I_{LIM}.

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to a TSD fault, it either stays latched off (TPS259850 variants) or restarts automatically after a fixed delay (TPS259851 variants). See *Overtemperature protection* section for more details on device response to overtemperature.

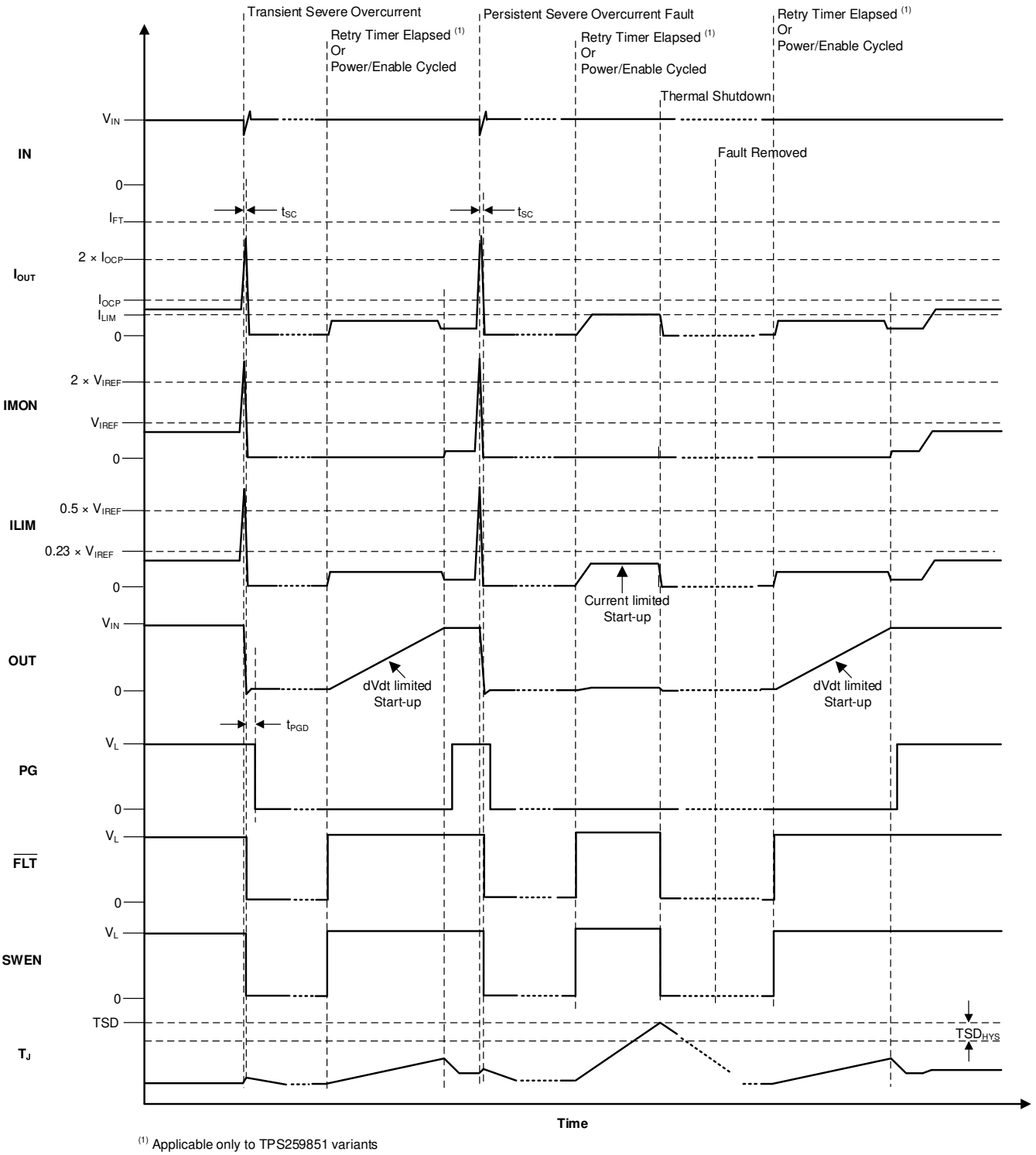
Note

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

8.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. The fast-trip comparator employs a scalable threshold (I_{SFT}) which is equal to 2 × I_{OCP} (primary device) or 2.25 × I_{OCP} (secondary device) during steady-state and 1.5 × I_{LIM} during inrush. This action enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which may not be suitable for all systems. After the current exceeds the fast-trip threshold, the TPS25985x turns off the FET within t_{SFT}. The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}. Figure 8-5 illustrates the short-circuit response for TPS25985x eFuse.

In some of the systems, for example blade servers and telecom equipment which house multiple hot-pluggable blades or line cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which could potentially be large enough to trigger the fast-trip comparator of the eFuse. The TPS25985x uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating uninterrupted system operation.



(1) Applicable only to TPS259851 variants

Figure 8-5. Short-Circuit Response

8.3.5 Analog Load Current Monitor (IMON)

The TPS25985x allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The current output also allows the IMON pins of multiple TPS25985x devices to be tied together to get the total current in a parallel configuration. The IMON signal can be converted to a voltage

ADVANCE INFORMATION

by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using Equation 13.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \quad (13)$$

The TPS25985x IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as PROCHOT™ or Intel PSYS™ to maximize system power usage and platform throughput without sacrificing safety or reliability.

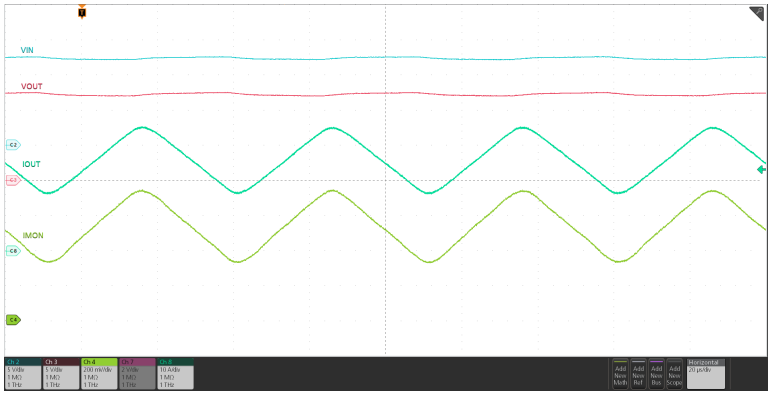


Figure 8-6. Analog Load Current Monitor Response

Note

1. The IMON pin provides load current monitoring information only during steady-state. During inrush, the IMON pin reports zero load current.
2. The ILIM pin reports the individual device load current at all times and can also be used as an analog load current monitor for each individual device.
3. Care must be taken to minimize parasitic capacitance on the IMON and ILIM pins to avoid any impact on the overcurrent and short-circuit protection timing.

8.3.6 Mode Selection (MODE)

This pin can be used to configure the TPS25985x as a primary device in a chain along with other TPS25985x eFuses, designated as secondary devices. This feature allows some of the TPS25985x pin functions to be changed to aid the primary + secondary parallel connection.

This pin is sampled at power up. Leaving the pin open configures it as a primary or standalone device. Connecting this pin to GND configures it as a secondary device.

The following functions are disabled in secondary mode and the device relies on the primary device to provide this functionality:

1. IREF internal current source
2. DVDT internal current source
3. Overcurrent detection in steady-state for circuit-breaker response
4. PG de-assertion (pulldown) after reaching steady-state
5. Latch-off after fault

In secondary mode, the following functions are still active:

1. Overtemperature protection
2. Start-up current limit based on ILIM
3. Active current sharing during inrush as well as steady-state
4. Analog current monitor (IMON) in steady state

ADVANCE INFORMATION

5. Steady-state overcurrent detection based on IMON. This is indicated by pulling ITIMER pin low internally, but does not trigger circuit-breaker action on ITIMER expiry. Rather, it relies on the primary device to start its own ITIMER and then trigger the circuit-breaker action for the whole chain by pulling SWEN low after the ITIMER expiry. However, the secondary devices use an internal overcurrent timer as a backup in case the primary device fails to initiate circuit-breaker action for an extended period of time. Refer to *Single Point Failure Mitigation* section for details.
6. Each device still has individual scalable and fixed fast-trip thresholds to protect itself. The individual short-circuit protection threshold is set to maximum, that is 2.25 × I_{OCP} (steady-state) or 2 × I_{LIM} (start-up) in secondary mode so that the primary device can lower it further for the whole system.
7. Individual OVP is set to maximum in secondary device so that the primary can lower it further for the whole system.
8. $\overline{FLT}$ assertion based on individual device fault detection (except circuit-breaker).
9. PG de-assertion control during inrush and assertion control after device reaches steady state. However, after that in steady state, the secondary device no longer controls the de-assertion of the PG in case of faults.
10. SWEN assertion or de-assertion based on internal events as well as FET ON and OFF control based on SWEN pin status.

In secondary mode, the device behavior during short-circuit and fast-trip is also altered. More details are available in the *Short-Circuit Protection* section.

8.3.7 Parallel Device Synchronization (SWEN)

The SWEN pin is a signal which is driven high when the FET must be turned ON. When the SWEN pin is driven low (internally or externally), it signals the driver circuit to turn OFF the FET. This pin serves both as a control and handshake signal and allows multiple devices in a parallel configuration to synchronize their FET ON and OFF transitions.

Table 8-1. SWEN Summary

Device State	FET Driver Status	SWEN
Steady-state	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Undervoltage (VIN UVP)	OFF	L
Insertion delay	OFF	L
Overvoltage lockout (VIN OVP)	OFF	L
Transient overcurrent	ON	H
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L
Fast-trip	OFF	L
Fault response mono-shot running (MODE = GND)	OFF	L
Fault response mono-shot expired (MODE = GND)	ON	H
ILM pin open (start-up)	OFF	L
ILM pin short (start-up)	OFF	L
ILM pin open (steady-state)	OFF	L
ILM pin short (steady-state)	OFF	L

ADVANCE INFORMATION

Table 8-1. SWEN Summary (continued)

Device State	FET Driver Status	SWEN
FET health fault	OFF	L

The SWEN is an open-drain pin and must be pulled up to an external supply.

Note

1. The SWEN pullup supply needs to be powered up before the eFuse can be turned on. TI recommends to use a system standby rail which is derived from the input of the eFuse.
2. In some cases, it may be possible to use the ITIMER pin as a pullup rail for SWEN pin. Usse a weak pullup to ensure that the loading on the ITIMER is not high enough to affect the ITIMER charging and discharging time.

In a primary + secondary parallel configuration, the SWEN pin is used by the primary device to control the on and off transitions of the secondary devices. At the same time, it allows the secondary devices to communicate any faults or other condition which might prevent it from turning on to the primary device. Refer to *Fault Response and Indication ($\overline{FLT}$)* for more details.

To maintain state machine synchronization, the devices rely on SWEN level transitions as well as timing for handshakes. This ensures all the devices turn ON and OFF synchronously and in the same manner (for example, DVDT controlled or current limited start-up). There are also fail-safe mechanisms in the SWEN control and handshake logic to ensure the entire chain is turned off safely even if the primary device is unable to take control in case of a fault.

Note

TI recommends to keep the parasitic loading on the SWEN pin to a minimum to avoid synchronization timing issues.

8.3.8 Stacking Multiple eFuses for Unlimited Scalability

For systems needing higher current than supported by a single TPS25985x, multiple TPS25985x devices can be connected in parallel to deliver the total system current. Conventional eFuses may not share current equally between themselves during steady-state due to mismatches in their path resistances (which includes the individual device R_{DSON} variation from part to part, as well as the parasitic PCB trace resistance). This fact can lead to multiple problems in the system:

1. Some devices always carry higher current as compared to other devices, which can result in accelerated failures in those devices and an overall reduction in system operational lifetime.
2. As a result, thermal hotspots form on the board, devices, traces, and vias carrying higher current, leading to reliability concerns for the PCB. In addition, this problem makes thermal modeling and board thermal management more challenging for designers.
3. The devices carrying higher current may hit their individual circuit-breaker threshold prematurely even while the total system load current is lower than the overall circuit-breaker threshold. This action may lead to false tripping of the eFuse during normal operation. This has the effect of lowering the current-carrying capability of the parallel chain. In other words, the current rating of the parallel eFuse chain needs to be de-rated as compared to the sum of the current ratings of the individual eFuses. This de-rating factor is a function of the path resistance mismatch, the number of devices in parallel, and the individual eFuse circuit-breaker accuracy.

The need for de-rating has an adverse impact on the system design. The designer is forced to make one of these trade-offs:

1. Limit the operating load current of the system to below the derated current threshold of the eFuse chain. Essentially, it means lower platform capabilities than are supported by the power supply (PSU).

ADVANCE INFORMATION

2. Increase the overall circuit-breaker threshold to allow the desired system load current to pass through without tripping. As a consequence, the power supply (PSU) must be oversized to deliver higher currents during faults to account for the de-grading of the overall circuit-breaker accuracy.

In either case, the system suffers from poor power supply utilization, which can mean sub-optimal system throughput or increased installation and operating costs, or both.

The TPS25985x uses a proprietary technique to address these problems and provide unlimited scalability of the solution by paralleling as many eFuses as needed. This is incorporated without unequal current sharing or any degradation in accuracy.

For this scheme to work correctly, the devices must be connected in the following manner:

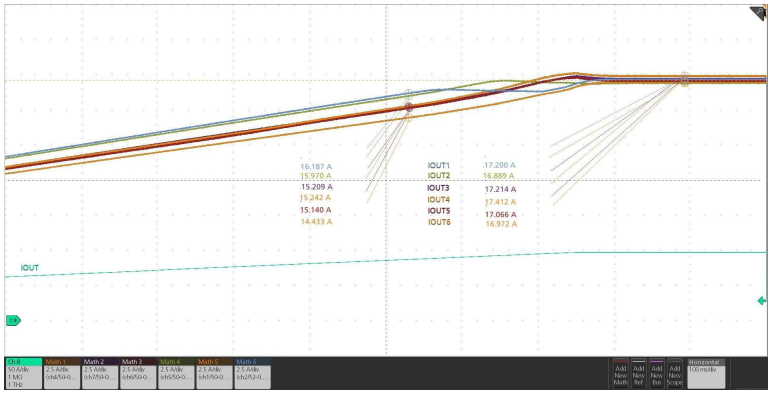
- The SWEN pins of all the devices are connected together.
- The IMON pins of all the devices need to be connected together. The R_{IMON} resistor value on the combined IMON pin can be calculated using Equation 14.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (14)$$

- The R_{ILIM} for each individual eFuse must be selected based on Equation 15.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (15)$$

Where N = number of devices in parallel chain. Figure 8-7 illustrates the response of the active current sharing block in TPS25985 eFuse during steady-state.



Intentional skew is introduced between the power path resistances for six devices and the load current is ramped up slowly. Equal current distribution is seen between all devices after the current through each device exceeds the active current sharing threshold.

Figure 8-7. Active Current Sharing During Steady-State with Six TPS25985x eFuses in Parallel

Note

The active current sharing scheme is engaged when the current through any eFuse while in steady-state exceeds the individual current sharing threshold set by the R_{ILIM} based on Equation 16.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (16)$$

The active current sharing scheme is disengaged when the total system current exceeds the system overcurrent (circuit-breaker) threshold ($I_{OCP(TOTAL)}$).

ADVANCE INFORMATION

8.3.8.1 Current Balancing During Start-Up

The TPS25985x implements a proprietary current balancing mechanism during start-up, which allows multiple TPS25985x devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance makes it possible to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

8.3.9 Analog Junction Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

Note

1. The TEMP pin voltage is used only for external monitoring and does not interfere with the overtemperature protection scheme of each individual device which is based purely on the internal temperature monitor.
2. TI recommends to add a capacitance of 22 pF on the TEMP pin to filter out glitches during system transients.

8.3.10 Overtemperature Protection

The TPS25985x employs an internal thermal shutdown mechanism to protect itself when the internal FET becomes too hot to operate safely. When the TPS259850 detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS259851 detects thermal overload, it remains off until it has cooled down sufficiently. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

Table 8-2. Overtemperature Protection Summary

Device	Enter TSD	Exit TSD
TPS259850 (Latch-Off)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$
TPS259851 (Auto-Retry)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ t_{RST} timer expired or VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

8.3.11 Fault Response and Indication ($\overline{FLT}$)

Table 8-3 summarizes the device response to various fault conditions.

Table 8-3. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Delay
Steady-state	None	N/A	H	
Inrush	None	N/A	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Undervoltage (VIN UVP)	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	H	
Transient overcurrent	None	N	H	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	L	
Short-circuit (primary mode)	Fast-trip	Y	L	t_{FT}
Short-circuit (secondary mode)	Fast-trip followed by current limited Start-up	N	H	
ILIM pin open (start-up)	Shutdown	Y	L	
ILIM pin short (start-up)	Shutdown (if $I_{OUT} > I_{OC\_BKP}$)	Y	L	
ILIM pin open (steady-state)	Active current sharing loop always active	N	H	
ILIM pin short (steady-state)	Active current sharing loop disabled	N	H	
IMON pin open (steady-state)	Shutdown	Y	L	
IMON pin short (steady-state)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	45 µs
IREF pin open (start-up)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	
IREF pin open (steady-state)	Shutdown (if $I_{OUT} > I_{OC\_BKP}$)	Y	L	t_{ITIMER}

ADVANCE INFORMATION

Table 8-3. Fault Summary (continued)

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Delay
IREF pin short (steady-state)	Shutdown	Y	L	
IREF pin short (start-up)	Shutdown	Y	L	
ITIMER pin forced to high voltage	Shutdown (if $I_{OUT} > I_{OCP}$ or $I_{OUT} > I_{OC\_BKP}$)	Y	L	t_{SPFAIL_TMR}
Start-up timeout	Shutdown	Y	L	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	10 us
FET health fault (G-D)	Shutdown	Y	L	
FET health fault (D-S)	Shutdown	N	L	t_{SU_TMR}
External fault (SWEN pulled low externally while device is not in UV or OV)	Shutdown	Y	L	

$\overline{FLT}$ is an open-drain pin and must be pulled up to an external supply.

The device response after a fault varies based on the mode of operation:

1. During standalone or primary mode of operation (MODE = OPEN), the device latches a fault and follows the auto-retry or latch-off response as per the device selection. When the device turns on again, it follows the usual DVDT limited start-up sequence.
2. During the secondary mode of operation (MODE = GND), if the device detects any fault, it pulls the SWEN pin low momentarily to signal the event to the primary device and thereafter relies on the primary to take control of the fault response. However, if the primary device fails to register the fault, there i a failsafe mechanism in the secondary device to turn off the entire chain and enter a latch-off condition. Thereafter, the device can be turned on again only by power cycling VDD below $V_{UVP(F)}$ or by cycling EN/UVLO pin below $V_{SD(F)}$.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the pin is de-asserted. This action also clears the t_{RST} timer (auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both latch-off and auto-retry variants.

8.3.12 Power Good Indication (PG)

Power Good indication is an active high output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

Table 8-4. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Undervoltage ($V_{EN} < V_{UVLO}$)	OFF	L	t_{PGD}
$V_{IN} < V_{UVP}$	OFF	L	
$V_{DD} < V_{UVP}$	OFF	L	
Overvoltage ($V_{IN} > V_{OVP}$)	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A

ADVANCE INFORMATION

Table 8-4. PG Indication Summary (continued)

Event or Condition	FET Status	PG Pin Status	PG Delay
Fast-trip	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A
ILM pin open	OFF	L (MODE = H) H (MODE = L)	t_{ITIMER} + t_{PGD} N/A
ILM pin short	OFF	L (MODE = H) H(MODE = L)	t_{PGD} N/A
Overtemperature	Shutdown	L (MODE = H) H (MODE = L)	t_{PGD} N/A

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted HIGH after a de-glitch time (t_{PGA}).

The PG is de-asserted if the FET is turned off at any time during normal operation. The PG de-assertion de-glitch time is t_{PGD}.

ADVANCE INFORMATION

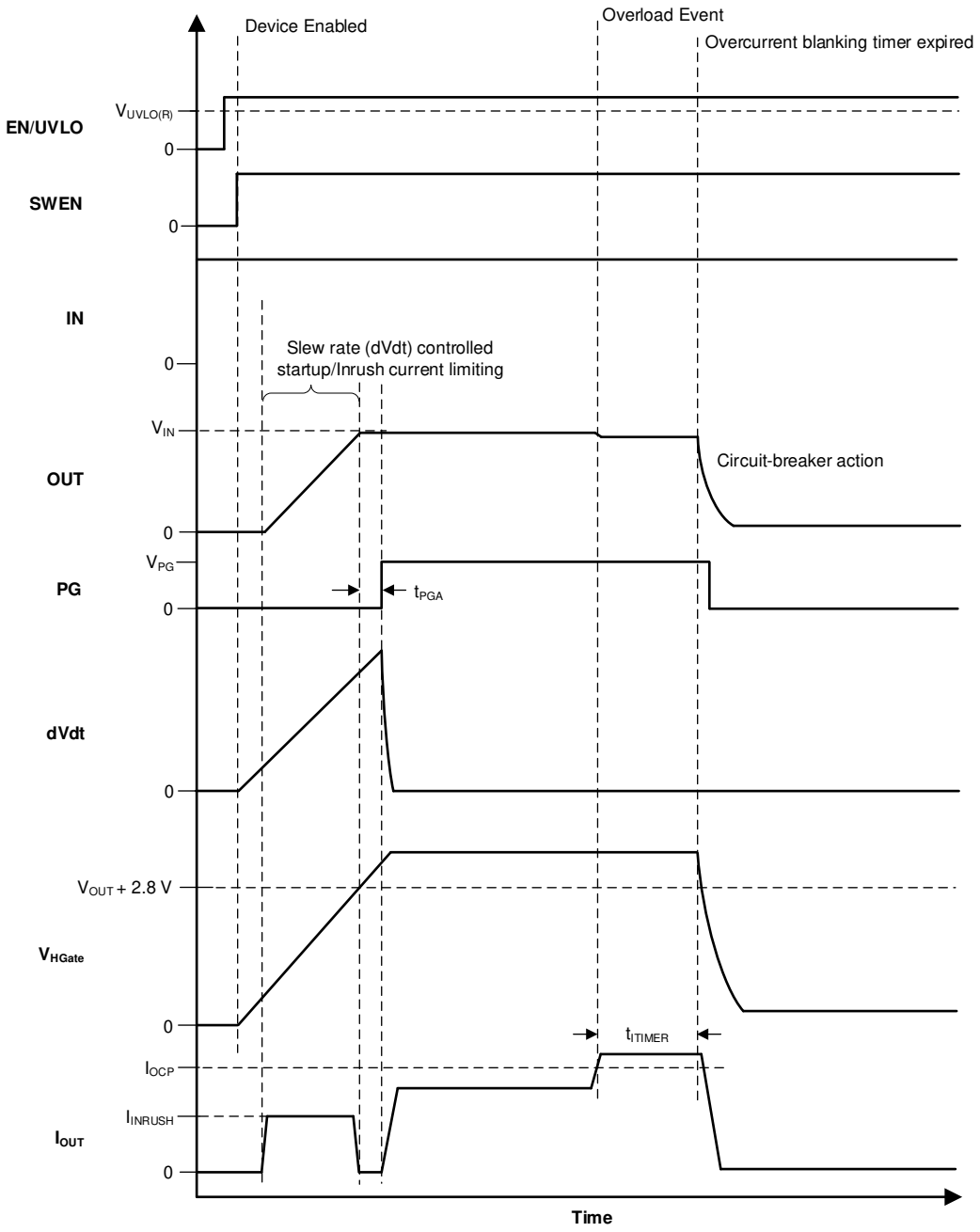


Figure 8-8. TPS25985x PG Timing Diagram

The PG is an open-drain pin and must be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

When the device is used in secondary mode (MODE = GND) in conjunction with another TPS25985 device as a primary device in a parallel chain, it controls the PG assertion during start-up, but after the device reaches steady-state, it no longer has control over the PG de-assertion. Refer to the *Mode Selection (MODE)* for more details.

8.3.13 Output Discharge

The device has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when V_{OUT} < V_{FB} or if the device detects a fault.

The output discharge function may result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long-term degradation of the part.

Note

In a primary+secondary parallel configuration, TI recommends to hold EN/UVLO voltage below the $V_{UVLO(F)}$ threshold of the secondary device to activate output discharge for all the devices in the chain.

8.3.14 General Purpose Comparator

The device has a spare general purpose comparator whose inputs (CMPP, CMPM) and output (CMPOUT) are not connected to any internal logic, thereby allowing the user complete flexibility to use this comparator as per the system needs.

The comparator can be used for various purposes. Here are a few examples:

- **Adjustable fast overcurrent detect (PROCHOT#):** IMON pin is connected to CMPM input and an appropriate reference voltage is connected to CMPP input. CMPOUT is connected to the PROCHOT# pin of the processor. When the load current crosses the set threshold, the CMPOUT goes low and signals the processor to throttle down immediately.

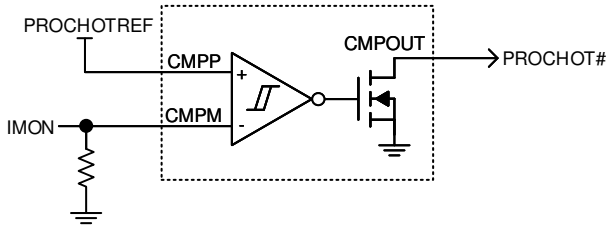


Figure 8-9. Adjustable Fast Overcurrent (PROCHOT#) Detect Using Internal Comparator

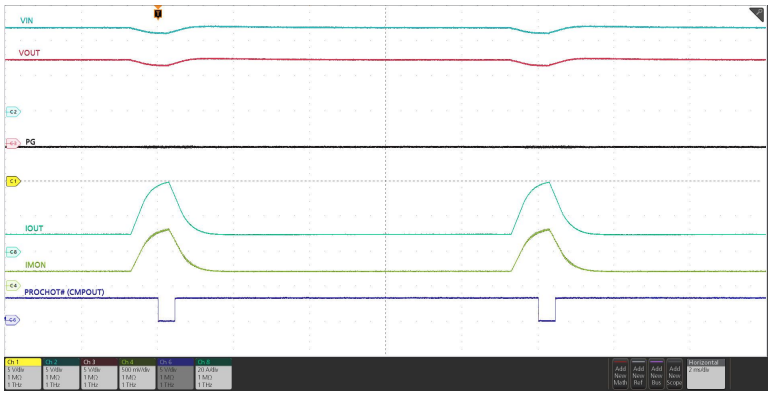


Figure 8-10. PROCHOT# Response Using Internal Comparator

- **Fast overvoltage protection with adjustable threshold:** Input supply is connected to CMPM input through a resistor divider and an appropriate reference voltage is connected to CMPP input. CMPOUT is connected

ADVANCE INFORMATION

to the EN/UVLO pin. When the input supply crosses the set threshold, the CMPOUT goes low and turns off the part.

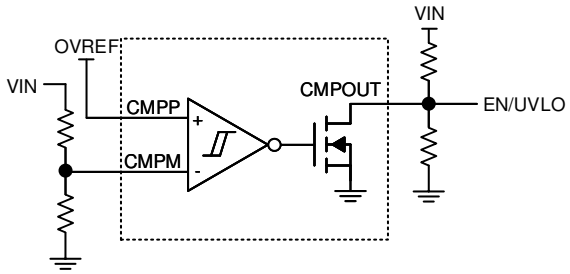


Figure 8-11. Fast Overvoltage Protection with Adjustable Threshold Using Internal Comparator

- **Load handshake or detect timer:** An R-C network from VOUT supply is connected to CMPM input through a resistor divider and an appropriate reference voltage is connected to the CMPP input. CMPOUT is connected to the EN/UVLO pin. After the device turns on, the R-C on VOUT starts charging and after it crosses the threshold, CMPOUT goes low to pull down the EN/UVLO and turn off the device, unless the downstream circuit indicates it has powered up successfully by driving the CMPM input low within the expected amount of time determined by the R-C time constant.

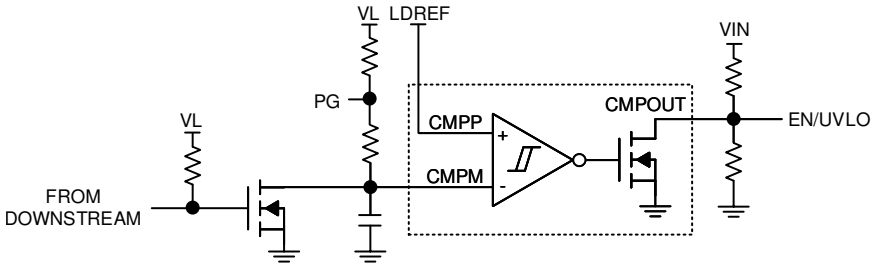


Figure 8-12. Load Handshake or Detect Timer Using Internal Comparator

8.3.15 FET Health Monitoring

The TPS25985x can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance by not providing power to the load correctly or by not providing the necessary level of protection. After a FET failure is detected, the TPS25985x tries to turn off the internal FET by pulling the gate low and asserts the $\overline{FLT}$ pin.

- **D-S short:** D-S short can result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at start-up by checking if $V_{IN-OUT} < V_{DSFLT}$ before the FET is turned ON. If yes, the device engages the internal output discharge to try and discharge the output. If the V_{OUT} doesn't discharge below V_{FB} within a certain allowed interval, the device asserts the $\overline{FLT}$ pin.
- **G-D short:** The TPS25985x detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition.
- **G-S short:** The TPS25985x detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, it is latched as a fault.

8.3.16 Single Point Failure Mitigation

The TPS25985x relies on the proper component connections and biasing on the IMON, ILIM, IREF, and ITIMER pins to provide overcurrent and short-circuit protection under all circumstances. As an added safety measure, the device uses the following mechanisms to ensure that the device provides some form of overcurrent protection even if any of these pins are not connected correctly in the system or the associated components have a failure in the field.

ADVANCE INFORMATION

8.3.16.1 IMON Pin Single Point Failure

- **IMON pin open:** In this case, the IMON pin voltage is internally pulled up to a higher voltage and exceeds the threshold (V_{IREF}), causing the part to perform a circuit-breaker action even if there is no significant current flowing through the device.
- **IMON pin shorted to GND directly or through a very low resistance:** In this case, the IMON pin voltage is held at a low voltage and is not allowed to exceed the threshold (V_{IREF}) even if there is significant current flowing through the device, thereby rendering the primary overcurrent protection mechanism ineffective. The device relies on an internal overcurrent sense mechanism to provide some protection as a backup. If the device detects that the backup current sense threshold (I_{OC_BKP}) is exceeded but at the same time the primary overcurrent detection on IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

8.3.16.2 ILIM Pin Single Point Failure

- **ILIM pin open:** In this case, the ILIM pin voltage is internally pulled up to a higher voltage and exceeds the V_{IREF} threshold, causing the part to engage the current limit even if there is no significant current flowing through the device.
- **ILIM pin shorted to GND directly or through a very low resistance:** In this case, the ILIM pin voltage is held at a low voltage and is not allowed to exceed the start-up current limit threshold even if there is significant current flowing through the device, thereby rendering the primary current limit mechanism ineffective during start-up. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold (IOC_BKP) is exceeded but at the same time the primary overcurrent detection on ILIM pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

8.3.16.3 IREF Pin Single Point Failure

- **IREF pin open or forced to higher voltage:** In this case, the IREF pin (V_{IREF}) is pulled up internally or externally to a voltage which is higher than the target value as per the recommended I_{OCP} or I_{LIM} calculations, preventing the primary circuit-breaker, active current limit, and short-circuit protection from getting triggered even if there is significant current flowing through the device. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold is exceeded but at the same the primary overcurrent or short-circuit detection on ILIM or IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.
- **IREF pin shorted to GND:** In this case, the V_{IREF} threshold is set to 0 V, causing the part to perform active current limit or circuit-breaker action even if there is no significant current flowing through the device.

8.3.16.4 ITIMER Pin Single Point Failure

- **ITIMER pin open or short to GND:** In this case, the ITIMER pin is already discharged below $V_{ITIMERTHR}$ and hence indicates overcurrent blanking timer expiry instantaneously after an overcurrent event and triggers a circuit-breaker action without any delay.
- **ITIMER pin forced to some voltage higher than $V_{ITIMERTHR}$:** In this case, the ITIMER pin is unable to discharge below $V_{ITIMERTHR}$ and hence fails to indicate overcurrent blanking timer expiry, thereby rendering the primary circuit-breaker mechanism ineffective. The device relies on a backup overcurrent timer mechanism to provide some protection as a backup. If the device detects an overcurrent event on either the IMON pin or the backup overcurrent detection circuit, the device engages the internal backup time and after the timer expires ($t_{SPFLTMR}$), it latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

ADVANCE INFORMATION

8.4 Device Functional Modes

The features of the device depend on the operating mode. Table 8-5 and Table 8-6 summarize the device functional modes.

Table 8-5. Device Functional Modes Based on EN/UVLO Pin

Pin: EN/UVLO	Device State	Output Discharge
> $V_{UVLO(R)}$	Fully ON	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (< t_{QOD})	FET OFF	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (> t_{QOD})	FET OFF	Enabled
< $V_{SD(F)}$	Shutdown	Disabled

Table 8-6. Device Functional Modes Based on MODE Pin

Pin: MODE	Device Configuration
Open	Primary or standalone
GND	Secondary

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25985x is a high-current eFuse that is typically used for power rail protection applications. The device operates from 4.5 V to 16 V with input overvoltage and adjustable undervoltage protection. The device provides ability to control inrush current and offers protection against overcurrent and short-circuit conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool, *TPS25985x Design Calculator* is available in the web product folder.

9.2 Single Device, Standalone Operation

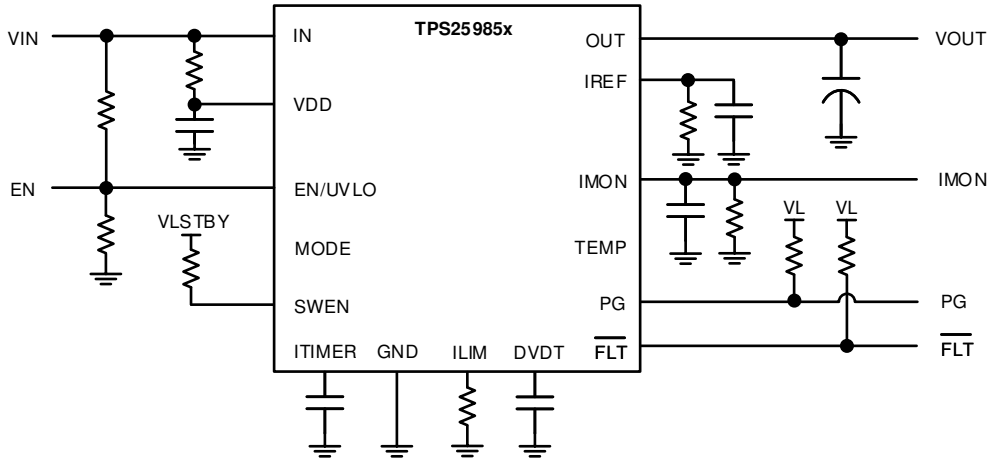


Figure 9-1. Single Device, Standalone Operation

Note

The MODE pin is left OPEN to configure for standalone operation.

Other variations:

1. The IREF pin can be driven from an external reference voltage source.
2. In a host MCU controlled system, EN/UVLO can be connected to a GPIO pin to control the device. IMON pin voltage can be monitored using an ADC. The host MCU can use a DAC to drive IREF to change the current limit threshold dynamically.
3. The device can be used as a simple high current load switch without adjustable overcurrent or fast-trip protection by tying the ILIM and IMON pins to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.
4. The CMPP, CMPM, and CMPOUT pins can be used to implement adjustable OVP or PG thresholds or PROCHOT or Load Handshake timer functionality as described in the *General Purpose Comparator* section.

ADVANCE INFORMATION

9.3 Multiple Devices, Parallel Connection

Applications which need higher current capability can use two or more TPS25985x devices connected in parallel as shown in Figure 9-2.

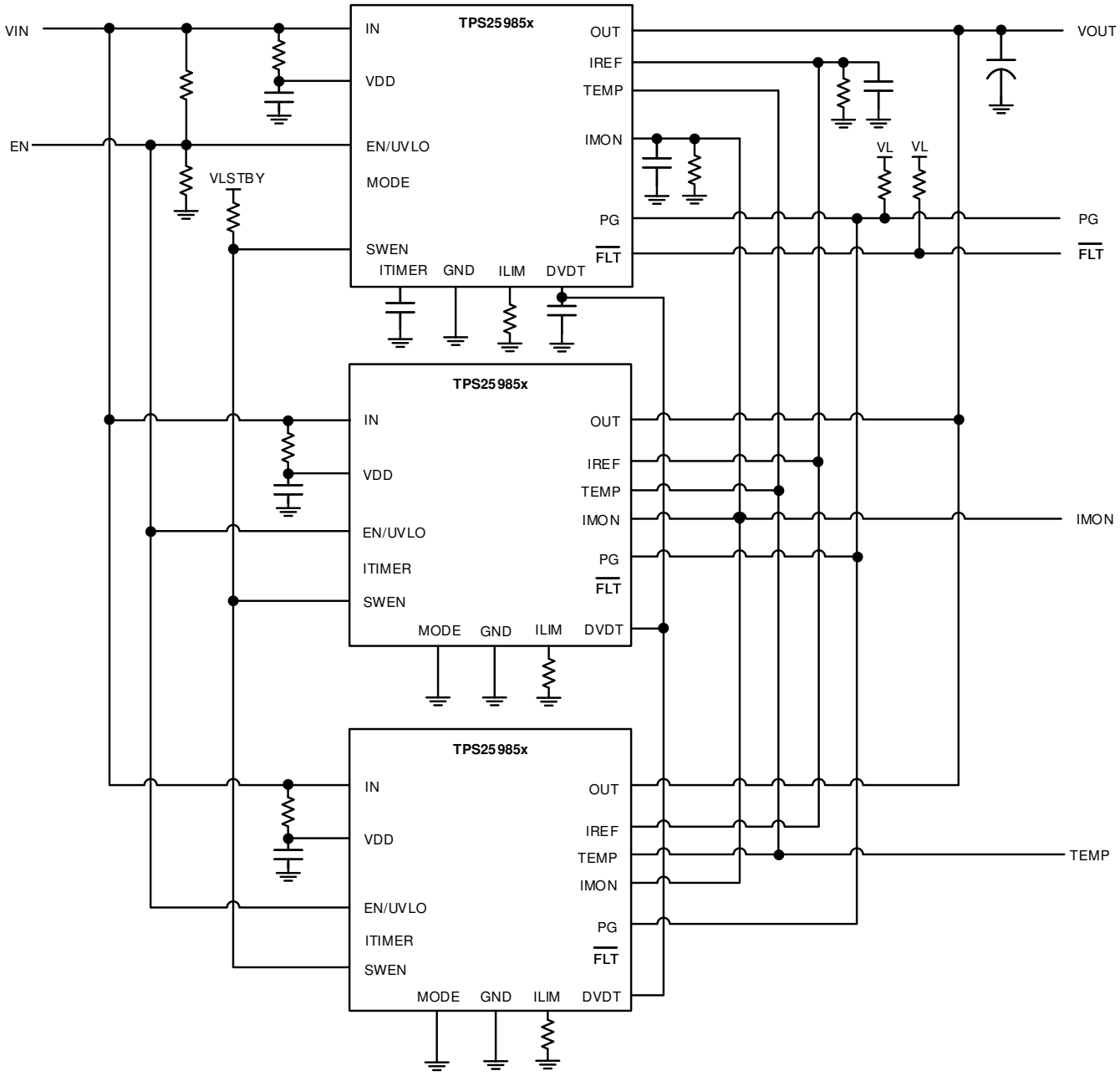


Figure 9-2. Devices Connected in Parallel for Higher Current Capability

In this configuration, one TPS25985x device is designated as the primary device and controls the other TPS25985x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through an R-C filter.
2. MODE pin is left OPEN.
3. ITIMER is connected through capacitor to GND.
4. DVDT is connected through capacitor to GND.
5. IREF is connected through resistor to GND.

6. IMON is connected through resistor to GND.
7. ILIM is connected through resistor to GND.
8. SWEN is pulled up to a 3.3-V to 5-V standby rail. This rail must be powered up independent of the eFuse.

The secondary devices must be connected in the following manner:

1. VDD is connected to IN through a R-C filter.
2. MODE pin is connected to GND.
3. ITIMER pin is left OPEN.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. SWEN
6. PG
7. IMON
8. IREF

In this configuration, all the devices are powered up and enabled simultaneously.

Power up: After power up or enable, all devices initially hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. After all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs at the same time.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per the following Equation 17 and Equation 18.

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (17)$$

$$C_{DVDT}(pF) = \frac{42000}{SR(V/ms)} \quad (18)$$

In this condition, the internal balancing circuit ensures that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This can potentially result in premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up.

All devices hold their respective PG signals low during start-up. After the output ramps up fully and reaches steady-state, each device releases its own PG pulldown. Because the DVDT pins of all devices are tied together, the internal gate high detection of all devices is synchronized. There can be some threshold or timing mismatches between devices leading to PG assertion in a staggered manner. However, since the PG pins of all devices are tied together, the combined PG signal becomes high only after all devices have released their PG pulldown. This signals the downstream load that it is okay to draw power.

Steady-state: During steady-state, all devices share current equally using the active current sharing mechanism which actively regulates the respective device R_{DSON} to evenly distribute current across all the devices in the parallel chain.

Overcurrent during steady-state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than the current flowing through individual devices. This is done by connecting the IMON pins of all the devices together. Similarly, the IREF pins of all devices are tied together and connected to a single R_{IREF} (or an external V_{IREF} source) to generate a common reference for the overcurrent protection

ADVANCE INFORMATION

block in all the devices. This action helps minimize the contribution of I_{IREF} variation and R_{IREF} tolerance to the overall mismatch in overcurrent threshold between devices. In this case, choose the combined R_{IMON} as per the following Equation 19:

$$R_{IMON} = \frac{I_{IREF} \times R_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (19)$$

The R_{ILIM} value for each individual eFuse must be selected based on the following Equation 20.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (20)$$

Where N = number of devices in parallel chain.

Other variations:

The IREF pin can be driven from an external voltage reference (V_{IREF}).

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (21)$$

During an overcurrent event, the overcurrent detection of all the devices is triggered simultaneously. This in turn triggers the overcurrent blanking timer (ITIMER) on each device. However, only the primary device uses the ITIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain. This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and ITIMER intervals among the devices do not degrade the accuracy of the circuit-breaker threshold of the complete parallel chain or the overcurrent blanking interval.

However, the secondary devices also start their backup overcurrent timer and can trigger the shutdown of the whole chain if the primary device fails to do so within a certain interval.

Severe overcurrent (short-circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path) during steady-state operation, the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold (I_{SFT} = 2 × I_{OCP} in steady-state or I_{SFT} = 2 × I_{LIM} during inrush) as well as a fixed threshold (I_{FFT} only during steady-state). After the fast-trip, the devices enter into a latch-off fault condition till the device is power cycled or re-enabled or expires the auto-retry timer (only for auto-retry variants).

9.4 Typical Application: 12-V, 300-A Power Path Protection in Datacenter Servers

9.4.1 Application

This design example considers a 12-V system operating voltage with a tolerance of ±10%. The maximum steady-state load current is 300 A. If the load current exceeds 330 A, the eFuse circuit must allow transient overload currents up to a 16-ms interval. For persistent overloads lasting longer than that, the eFuse circuit must break the circuit and then latch-off. The eFuse circuit must charge a bulk capacitance of 55 mF and support approximately 10% of the steady-state load during start-up. Figure 9-3 shows the application schematic for this design example.

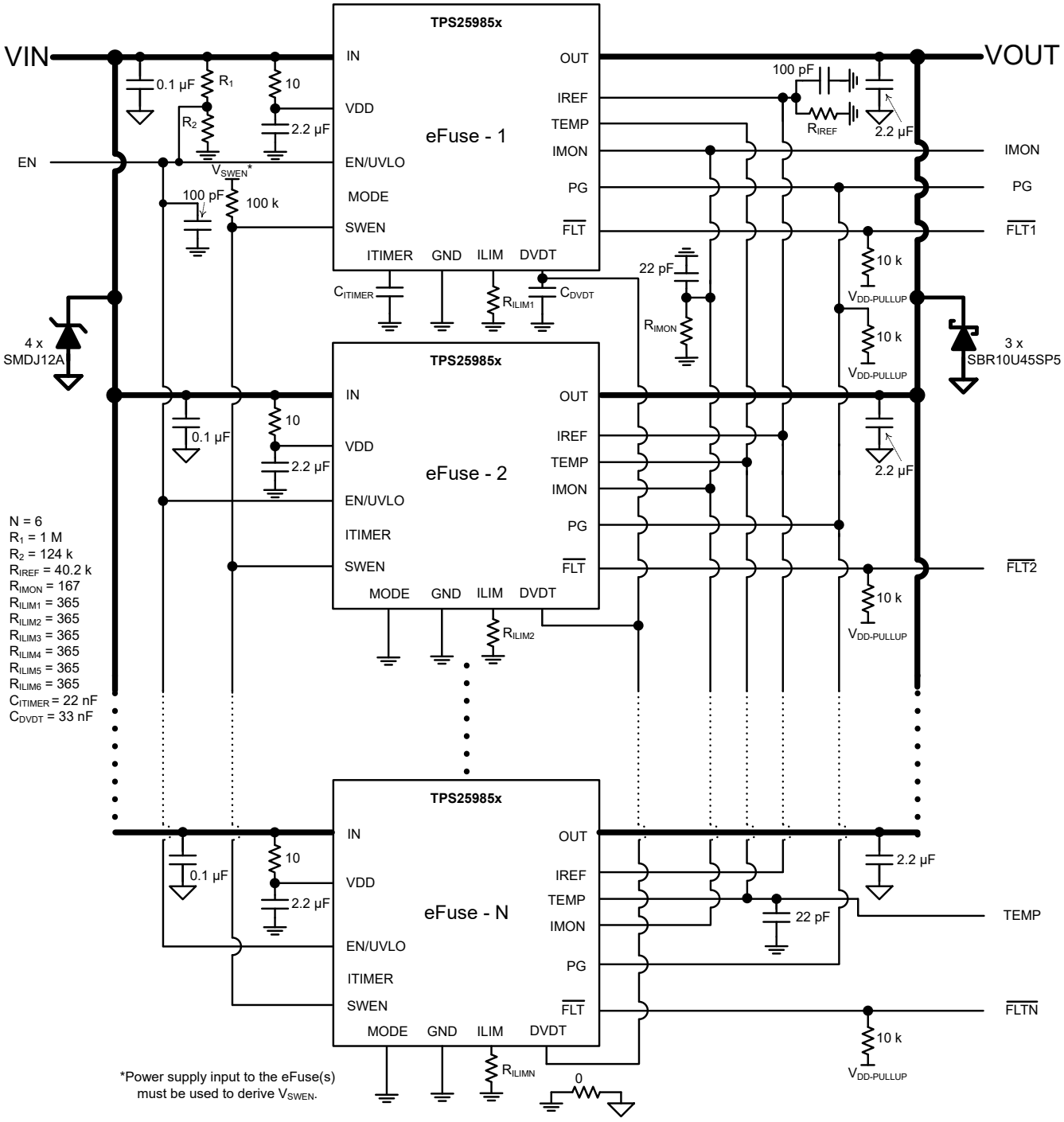


Figure 9-3. Application Schematic for a 12-V, 300-A Power Path Protection Circuit

ADVANCE INFORMATION

9.4.2 Design Requirements

Table 9-1 shows the design parameters for this application example.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	10.8 V–13.2 V
Maximum DC load current ($I_{OUT(max)}$)	300 A
Maximum output capacitance (C_{LOAD})	55 mF
Are all the loads off until the PG is asserted?	No
Load at start-up ($R_{LOAD(Startup)}$)	0.33 Ω (equivalent to approximately 10% of the maximum steady-state load)
Maximum ambient temperature	55°C
Transient overload blanking timer	16 ms
Output voltage slew rate	1.2 V/ms
Need to survive a “Hot-Short” on output condition ?	Yes
Need to survive a “power up into short” condition?	Yes
Can a board be hotplugged in or power cycled?	Yes
Load current monitoring needed?	Yes
Fault response	Latch-off

9.4.3 Detailed Design Procedure

- **Determining the number of eFuse devices to be used in parallel**

  By factoring in a small variation in the junction to ambient thermal resistance ($R_{\theta JA}$), a single TPS25985x eFuse is rated at a maximum steady state DC current of 50 A at an ambient temperature of 70°C. Therefore, Equation 22 can be used to calculate the number of devices (N) to be in parallel to support the maximum steady state DC load current ($I_{LOAD(max)}$), for which the solution must be designed.

$$N \geq \frac{I_{OUT(max)}\,(A)}{50\ A} \tag{22}$$

  According to Table 9-1, $I_{OUT(max)}$ is 300 A. Therefore, six (6) TPS25985 eFuses are connected in parallel.

- **Setting up the primary and secondary devices in a parallel configuration**

  The MODE pin is used to configure one TPS25985x eFuse as the primary device in a parallel chain along with the other TPS25985x eFuses as the secondary devices. As a result, some of the TPS25985 pin functionalities can be changed to facilitate primary+secondary configuration as described in *Multiple Devices, Parallel Connection*.

  Leaving the pin open configures the corresponding device as the primary one. For the secondary devices, this pin must be connected to GND.

- **Selecting the C_{DVDT} capacitor to control the output slew rate and start-up time**

  For a robust design, the junction temperature of the device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Typically, dynamic power stresses are orders of magnitude greater than static stresses, so it is crucial to establish the right start-up time and inrush current limit for the capacitance in the system and the associated loads to avoid thermal shutdown during start-up.

Table 9-2 summarizes the formulas for calculating the average inrush power loss on the eFuses in the presence of different loads during start-up if the power good (PG) signal is not used to turn on all the downstream loads.

Table 9-2. Calculation of Average Power Loss During Inrush

Type of Loads During Start-Up	Expressions to Calculate the Average Inrush Power Loss
Only output capacitor of C_{LOAD} (µF)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}}$ (23)
Output capacitor of C_{LOAD} (µF) and constant resistance of $R_{LOAD(Startup)}$ (Ω) with turn-ON threshold of V_{RTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + \frac{V_{IN}^2}{R_{LOAD(Startup)}}\left[\frac{1}{6} - \left\{\frac{1}{2}\left(\frac{V_{RTH}}{V_{IN}}\right)^2\right\} + \left\{\frac{1}{3}\left(\frac{V_{RTH}}{V_{IN}}\right)^3\right\}\right]$ (24)
Output capacitor of C_{LOAD} (µF) and constant current of $I_{LOAD(Startup)}$ (A) with turn-ON threshold of V_{CTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + V_{IN} I_{LOAD(Startup)}\left[\frac{1}{2} - \left(\frac{V_{CTH}}{V_{IN}}\right) + \left\{\frac{1}{2}\left(\frac{V_{CTH}}{V_{IN}}\right)^2\right\}\right]$ (25)
Output capacitor of C_{LOAD} (µF) and constant power of $P_{LOAD(Startup)}$ (W) with turn-ON threshold of V_{PTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{ss}} + P_{LOAD(Startup)}\left[\ln\left(\frac{V_{PTH}}{V_{IN}}\right) + \left(\frac{V_{PTH}}{V_{IN}}\right) - 1\right]$ (26)

Where V_{IN} is the input voltage and T_{ss} is the start-up time.

With the different combinations of loads during start-up, the total average inrush power loss (P_{INRUSH}) can be calculated using the formulas described in Table 9-2. For a successful start-up, the system must satisfy the condition stated in Equation 27.

$$P_{INRUSH}(W)\sqrt{T_{ss}(s)} < 12 \times N \quad (27)$$

Where N denotes the number of eFuses in parallel and 12 W√s is the SOA limit of a single TPS25985x eFuse. This equation can be used to obtain the maximum allowed T_{ss}.

Note

TI recommends to use a T_{ss} in the range of 5 ms to 120 ms to prevent start-up issues.

A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of T_{ss} as calculated above. Equation 28 is used to compute the value of C_{DVDT}. The DVDT pins of all the eFuses in a parallel chain must be connected together.

$$C_{DVDT}(pF) = \frac{42000}{V_{IN}(V)/T_{ss}(ms)} \quad (28)$$

In this design example, C_{LOAD} = 55 mF, $R_{LOAD(Startup)}$ = 0.33 Ω, V_{RTH} = 0 V, V_{IN} = 12 V, and T_{ss} = 10 ms. P_{INRUSH} is calculated to be 469 W using the equations provided in the Table 9-2. It can be verified that the system satisfies condition state in Equation 27 and therefore capable of a successful start-up. If Equation 27 does not hold true, start-up loads or T_{ss} must be tuned to prevent chances of thermal shutdown during start-up. Using V_{IN} = 12 V, T_{ss} = 10 ms and Equation 28, the required C_{DVDT} value can be calculated to be 35 nF. The closest standard value of C_{DVDT} is 33 nF with 10% tolerance and DC voltage rating of 25 V.

ADVANCE INFORMATION

Note

In some systems, there can be active load circuits (for example, DC-DC converters) with low turn-on threshold voltages which can start drawing power before the eFuse has completed the inrush sequence. This action can cause additional power dissipation inside the eFuse during start-up and can lead to thermal shutdown. TI recommends using the Power Good (PG) pin of the eFuse to enable and disable the load circuit. This action ensures that the load is turned on only when the eFuse has completed its start-up and is ready to deliver full power without the risk of hitting thermal shutdown.

- **Selecting the R_{IREF} resistor to set the reference voltage for overcurrent protection and active current sharing**

In this parallel configuration, the IREF internal current source (I_{IREF}) of the primary eFuse interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage (V_{IREF}) for the overcurrent protection and active current sharing blocks. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel® PSYS™) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the fast-trip threshold (2 × I_{OCP}). Equation 29 is used to calculate the value of R_{IREF}.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (29)$$

In this design example, V_{IREF} is set at 1 V. With I_{IREF} = 25 µA (typical), we can calculate the target R_{IREF} to be 40 kΩ. The closest standard value of R_{IREF} is 40.2 kΩ with 0.1% tolerance and power rating of 100 mW. For improved noise immunity, place a 100-pF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to ensure proper operation of overcurrent detection circuit.

- **Selecting the R_{IMON} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady-state**

TPS25985x eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 30.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (30)$$

G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.18 µA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 31.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (31)$$

In this design example, I_{OCP} is considered to be 1.1 times $I_{OUT(max)}$. Hence, I_{OCP} is set at 330 A, and R_{IMON} can be calculated to be 166.67 Ω with G_{IMON} as 18.18 µA/A and V_{IREF} as 1 V. The nearest value of R_{IMON} is 167 Ω with 0.1% tolerance and power rating of 100 mW. For noise reduction, place a 22-pF ceramic capacitor across the IMON pin and GND.

Note

A system output current (I_{OUT}) must be considered when selecting R_{IMON}, not the current carried by each device.

ADVANCE INFORMATION

- **Selecting the R_{ILIM} resistor to set the current limit and fast-trip thresholds during start-up and the active sharing threshold during steady-state**

  R_{ILIM} is used in setting up the active current sharing threshold during steady-state and the overcurrent limit during startup among the devices in a parallel chain. Each device continuously monitors the current flowing through it (I_{DEVICE}) and outputs a proportional analog output current on its own ILIM pin. This in turn produces a proportional voltage (V_{ILIM}) across the respective ILIM pin resistor (R_{ILIM}), which is expressed as Equation 32.

  $$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (32)$$

  G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE}), whose typical value is 18.18 µA/A.

  – ***Active current sharing during steady-state*:** This mechanism operates only after the device reaches steady-state and acts independently by comparing its own load current information (V_{ILIM}) with the Active Current Sharing reference ($CLREF_{LIN}$) threshold, defined as Equation 33.

  $$CLREF_{LIN} = \frac{1.1 \times V_{IREF}}{3} \quad (33)$$

  Therefore, R_{LIM} must be calculated using Equation 34 to define the active current sharing threshold as I_{OCP}/N, where N is the number of devices in parallel. Using N = 6, R_{IMON} = 167 Ω, and Equation 34, R_{ILIM} can be calculated to be 367.4 Ω. The closest standard value of 365 Ω with 0.1% tolerance and power rating of 100 mW resistances are selected as R_{ILIM} for each device.

  $$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (34)$$

  Note

  To determine the value of R_{ILIM}, Equation 35 must be used if a different threshold for active current sharing ($I_{LIM(ACS)}$) than I_{OCP}/N is desired.

  $$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (35)$$

  When computing the current limit threshold during start-up in the next sub-section, ensure to use this R_{ILIM} value.

  – ***Overcurrent limit during start-up*:** During inrush, the overcurrent condition for each device is detected by comparing its own load current information (V_{ILIM}) with a scaled reference voltage as depicted in Equation 36.

  $$CLREF_{SAT} = \frac{0.7 \times V_{IREF}}{3} \quad (36)$$

  The current limit threshold during start-up can be calculated using Equation 37.

  $$I_{ILIM(Startup)} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \quad (37)$$

  By using a R_{ILIM} value of 365 Ω for each device, the start-up current is limited to 35 A for each device.

  Note

  The active current limit block employs a foldback mechanism during start-up based on V_{OUT}. When V_{OUT} is below the foldback threshold (V_{FB}) of 2 V, the current limit threshold is further lowered.

- **Selecting the C_{ITIMER} capacitor to set the overcurrent blanking timer**

  An appropriate capacitor can be connected at the ITIMER pin to ground to adjust the duration for which the load transients above the circuit-breaker threshold are allowed. The transient overcurrent blanking interval can be calculated using Equation 38.

ADVANCE INFORMATION

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (38)$$

Where t_{ITIMER} is the transient overcurrent blanking timer and C_{ITIMER} is the capacitor connected between ITIMER pin of the primary device and GND. I_{ITIMER} = 2 µA and ΔV_{ITIMER} = 1.5 V. A 22-nF capacitor with 10% tolerance and DC voltage rating of 25 V is used as the C_{ITIMER} for the primary device in this design, which results in 16.5 ms of t_{ITIMER}. The ITIMER pin for all the secondary devices is left open.

- **Selecting the resistors to set the undervoltage lockout threshold**

  The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in Undervoltage protection section. The resistor values required for setting up the UVLO threshold are calculated using Equation 39.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (39)$$

  To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. The current drawn by R_1 and R_2 from the power supply is $I_{R12} = V_{IN} / (R_1 + R_2)$. However, the leakage currents due to external active components connected to the resistor string can add errors to these calculations. So, the resistor string current, I_{R12} must be 20 times greater than the leakage current at the EN/UVLO pin (I_{ENLKG}). From the device electrical specifications, I_{ENLKG} is 0.1 µA (maximum) and UVLO rising threshold $V_{UVLO(R)}$ = 1.2 V. From the design requirements, V_{INUVLO} = 10.8 V. First choose the value of R_1 = 1 MΩ and use Equation 13 to calculate R_2 = 125 kΩ. Use the closest standard 1 % resistor values: R_1 = 1 MΩ and R_2 = 124 kΩ. For noise reduction, place a 100-pF ceramic capacitor across the EN/UVLO pin and GND.

- **Selecting the R-C filter between VIN and VDD**

  VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (10 Ω) – C (2.2 µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short-circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

- **Selecting the pullup resistors and power supplies for SWEN, PG, $\overline{FLT}$, and CMPOUT pins**

  $\overline{FLT}$, PG, and CMPOUT are the open drain outputs. If these logic signals are used, the corresponding pins must be pulled up to the appropriate voltages (< 5 V) through 10-kΩ pullup resistances.

  Note

  SWEN pin must be pulled up to a voltage in the range of 2.5 V to 5 V through a 100-kΩ resistance. This pullup power supply must be generated from the input to the eFuse and available before the eFuse is enabled, without which the eFuse does not start up.

- **Selection of TVS diode at input and Schottky diode at output**

  In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

  1. Minimize lead length and inductance into and out of the device.
  2. Use a large PCB GND plane.
  3. Addition of the Transient Voltage Suppressor (TVS) diodes to clamp the positive transient spike at the input.
  4. Using Schottky diodes across the output to absorb negative spikes.

ADVANCE INFORMATION

Refer to *TVS Clamping in Hot-Swap Circuits* and *Selecting TVS Diodes in Hot-Swap and ORing Applications* for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (20 V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. Four (4) SMDJ12A are used in parallel in this design example.

Note

Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000 µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

Selection of the Schottky diodes must be based on the following criteria:

– The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 40 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

$$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \quad (40)$$

– Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. Ideally, the negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (–1 V).
– DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
– Leakage current (I_R) must be as small as possible.

Three (3) SBR10U45SP5 are used in parallel in this design example.

- **Selecting C_{IN} and C_{OUT}**

TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.1 µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 2.2 µF can be used at the OUT pin of each device.

ADVANCE INFORMATION

9.4.4 Application Performance Plots

All the waveforms below are captured on an evaluation setup with six (6) TPS25985 eFuses in parallel. All the pullup supplies are derived from a separate standby rail.

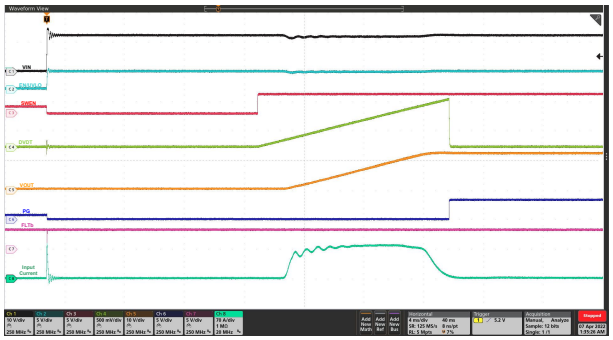


Figure 9-4. Input Hot Plug: V_{IN} Stepped Up from 0 V to 12 V, C_{LOAD} = 55 mF, C_{DVDT} = 33 nF, and R_{ILIM} on Each Device = 365 Ω

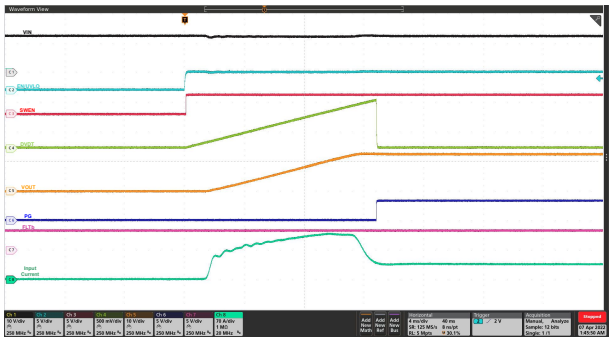


Figure 9-5. Start-up with EN/UVLO: V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, C_{LOAD} = 55 mF, $R_{LOAD(Start-up)}$ = 0.33 Ω, C_{DVDT} = 33 nF, and R_{ILIM} on Each Device = 365 Ω

Figure 9-6. Power Up into Short: V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, R_{IREF} = 40.2 kΩ, R_{ILIM} on Each Device = 365 Ω, and OUT Shorted to GND

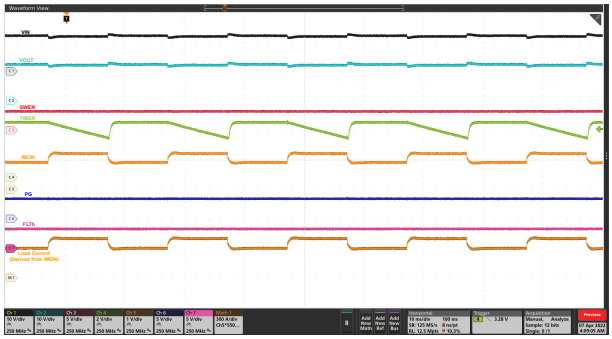


Figure 9-7. Transient Overload: V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped from 300 A to 400 A Then 300 A within 10 ms

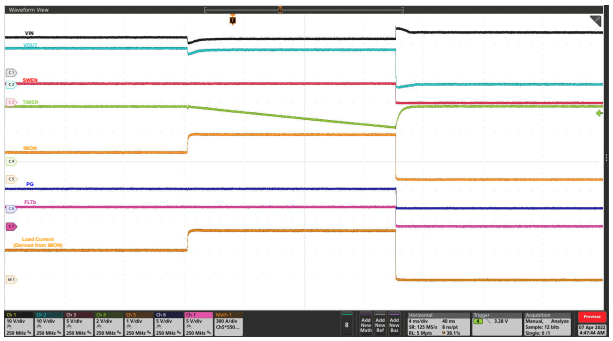


Figure 9-8. Circuit-Breaker Response: V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped up From 300 A to 500 A for > 20 ms

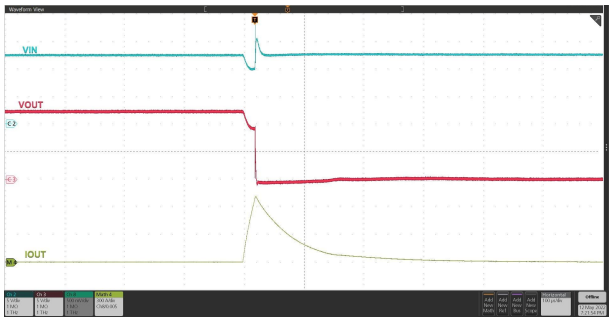


Figure 9-9. Output Hot-Short Response: V_{IN} = 12 V, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and OUT Shorted to GND

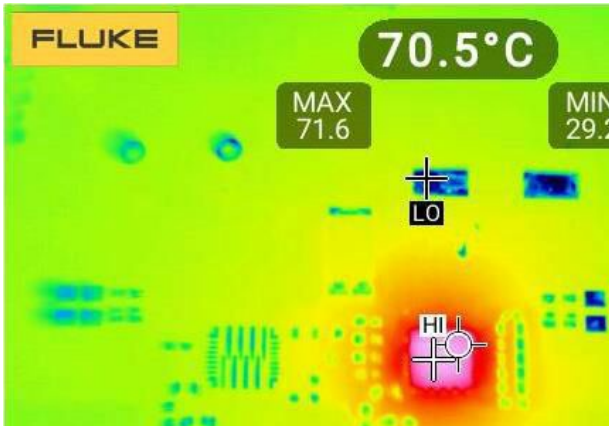


Figure 9-10. Single Device Temperature Rise with 50-A DC Current at Room Temperature (No Air-Flow)

9.5 What to Do and What Not to Do

TPS25985x needs the SWEN pin to be pulled up to a supply rail which is powered up before the device is enabled. Failing this, the device is not able to turn on the output. The SWEN pullup supply must not be derived from the output of the eFuse. Use one of the following options to derive the pullup supply rail for SWEN.

1. Use an existing standby rail in the system, which is derived from the main power input and comes up before the eFuse is turned on.
2. Use an LDO (3.3 V or 5 V) powered from the main power input.

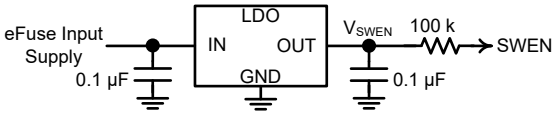


Figure 9-11. LDO Used as Pullup Supply for SWEN

3. Use a Zener regular powered from the main power input.

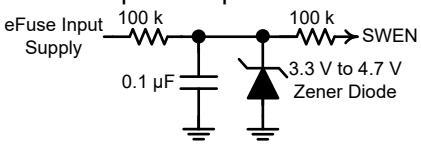


Figure 9-12. Zener Regulator Used as Pullup Supply for SWEN

4. Use the ITIMER pin of the primary eFuse. Ensure the ITIMER pin does not have excess loading which can interfere with the normal overcurrent blanking timer functionality.

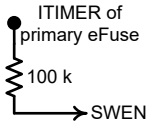


Figure 9-13. ITIMER Pin Used as Pullup Supply for SWEN

ADVANCE INFORMATION

9.6 Digital Telemetry Using External Microcontroller

Systems which need digital telemetry, control, and configurability along with high current eFuse functionality can use TPS25985x devices in conjunction with a microcontroller as shown in Figure 9-14.

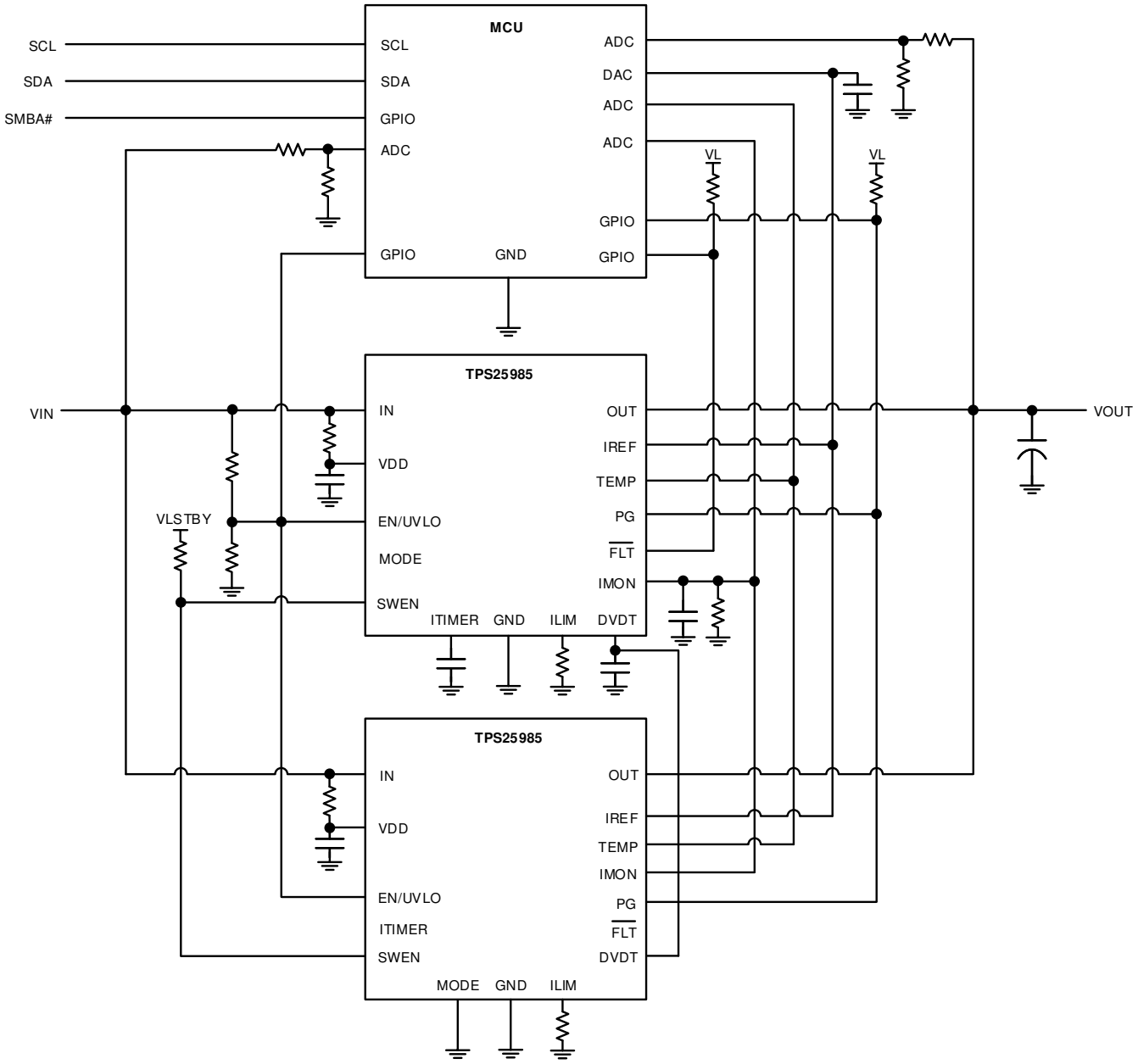


Figure 9-14. Digital Telemetry Using External Microcontroller

The basic circuit connections for the eFuses are the same for the single or multiple parallel device configuration. In addition, the following connections can be made to the microcontroller:

- IMON is connected to an ADC input of microcontroller for monitoring the load current.
- EN/UVLO is connected to GPIO of microcontroller to allow digital ON and OFF control of the eFuse.
- PG and $\overline{\text{FLT}}$ pins are connected to GPIO of microcontroller to allow digital monitoring of the eFuse status.
- VIN and VOUT rails are connected to the ADC inputs of microcontroller (through resistor ladder to appropriately step down the voltage) for monitoring the bus voltages.
- TEMP is connected to an ADC input of microcontroller for monitoring the eFuse die temperature.

- IREF can be optionally connected to a DAC output of the microcontroller to dynamically change the reference voltage for overcurrent and short-circuit current thresholds.

9.7 Application Limitations

This section highlights some limitations in the application which were identified during bench evaluation of the existing TPS25985x silicon on the evaluation module (EVM). A design fix is included in the final release of the IC.

- The Iq on VDD pin gradually increases over time after the device is powered up. System impact is minimum as the absolute Iq itself is very small.
- Higher values of capacitor from IREF pin to GND beyond 150 pF may incorrectly trigger overcurrent during start-up. TI recommends to keep the IREF pin capacitor value below 150 pF for proper operation.

10 Power Supply Recommendations

The TPS25985x devices are designed for a supply voltage in the range of 4.5 V to 16 V on the IN and VDD pins. TI recommends using a minimum capacitance of 0.1 µF on the IN pin of each device in parallel chain to avoid coupling of high slew rates during hot plug events. TI also recommends using an R-C filter from the input supply to the VDD pin on each device in parallel chain to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

10.1 Transient Protection

In the case of a short-circuit or circuit-breaker event when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 2.2 µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.1 µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 41.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (41)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 10-1.

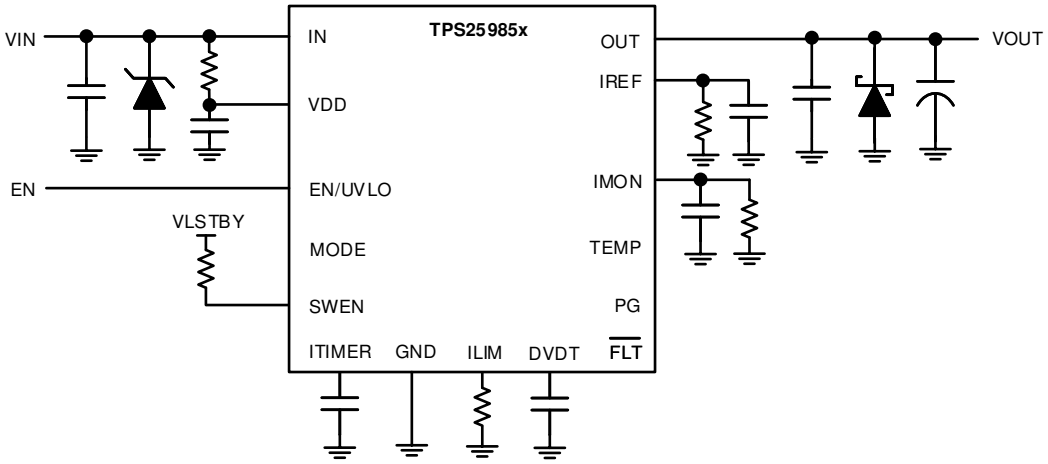


Figure 10-1. Circuit Implementation with Optional Protection Components

10.2 Output short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 2.2 µF or greater between the OUT terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - R_{IMON}
  - R_{IREF}
  - C_{dVdT}
  - C_{ITIMER}
  - C_{IN}
  - C_{OUT}
  - C_{VDD}
  - Resistors for the EN/UVLO pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{IN}, C_{OUT}, C_{VDD}, R_{IREF}, R_{ILIM}, R_{IMON}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the IMON, ILIM and IREF pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- TI recommends to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

11.2 Layout Example

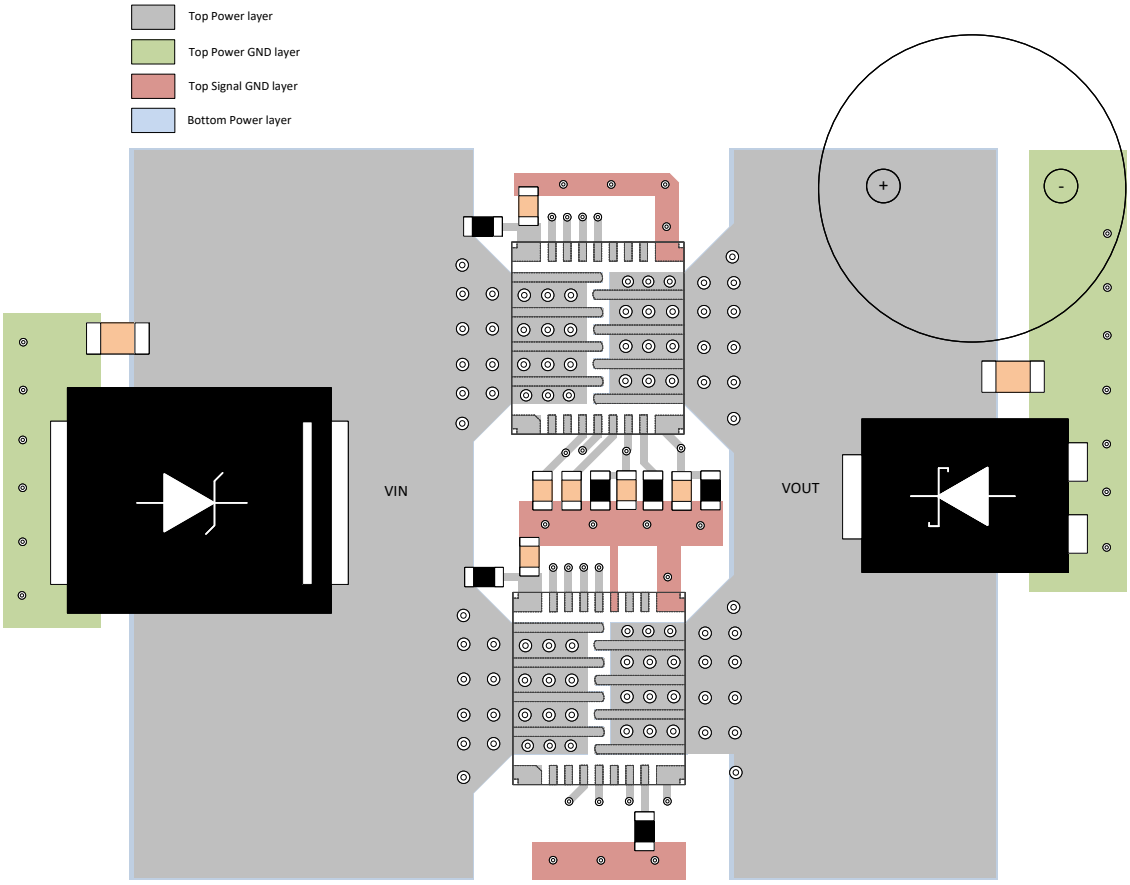


Figure 11-1. TPS25985x Two Parallel Devices Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25985EVM eFuse Evaluation Board*
- Texas Instruments, *TPS25985x Design Calculator*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

PSYS™ is a trademark of intel.
PROCHOT™ and Intel PSYS™ are trademarks of Intel.
TI E2E™ is a trademark of Texas Instruments.
Intel® is a registered trademark of Intel.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

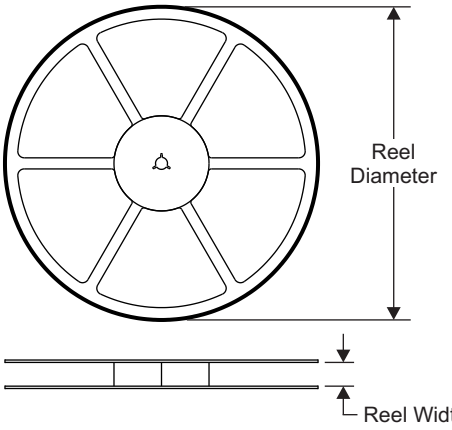
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

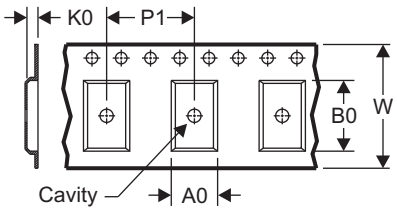
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

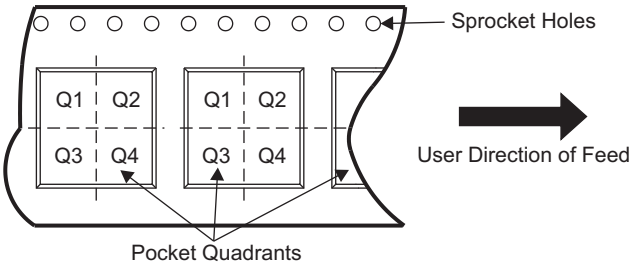


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

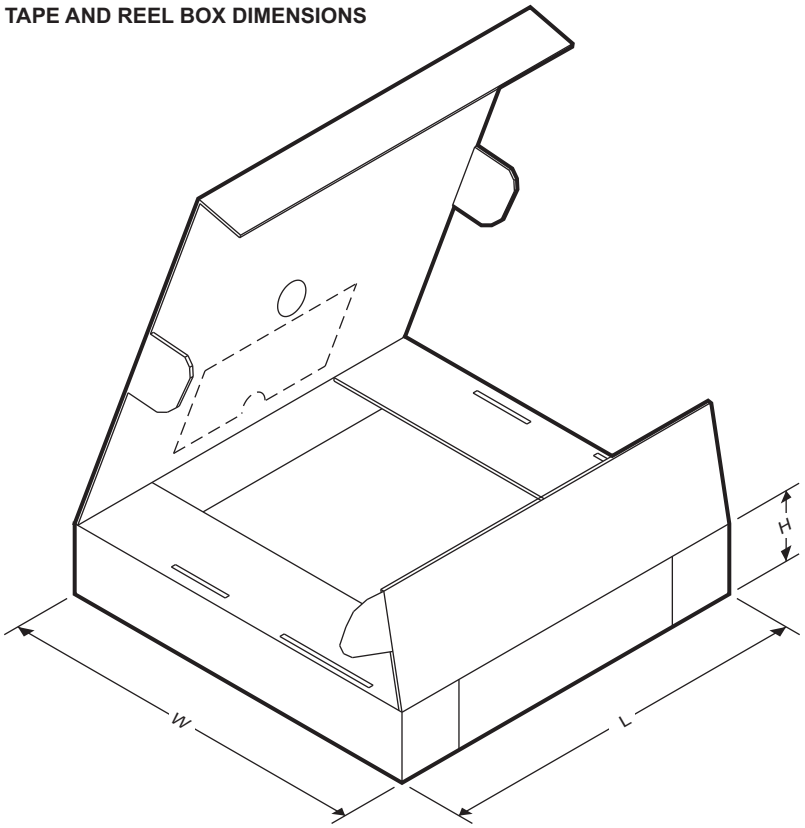


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS259850RQPR	VQFN	RQP	26	3000	330	12.4	4.5	5.3	1.15	8	9.1	Q2
TPS259850RQPR	VQFN	RQP	26	3000	330	12.4	4.5	5.3	1.15	8	9.1	Q2
TPS259851RQPR	VQFN	RQP	26	3000	330	12.4	4.5	5.3	1.15	8	9.1	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



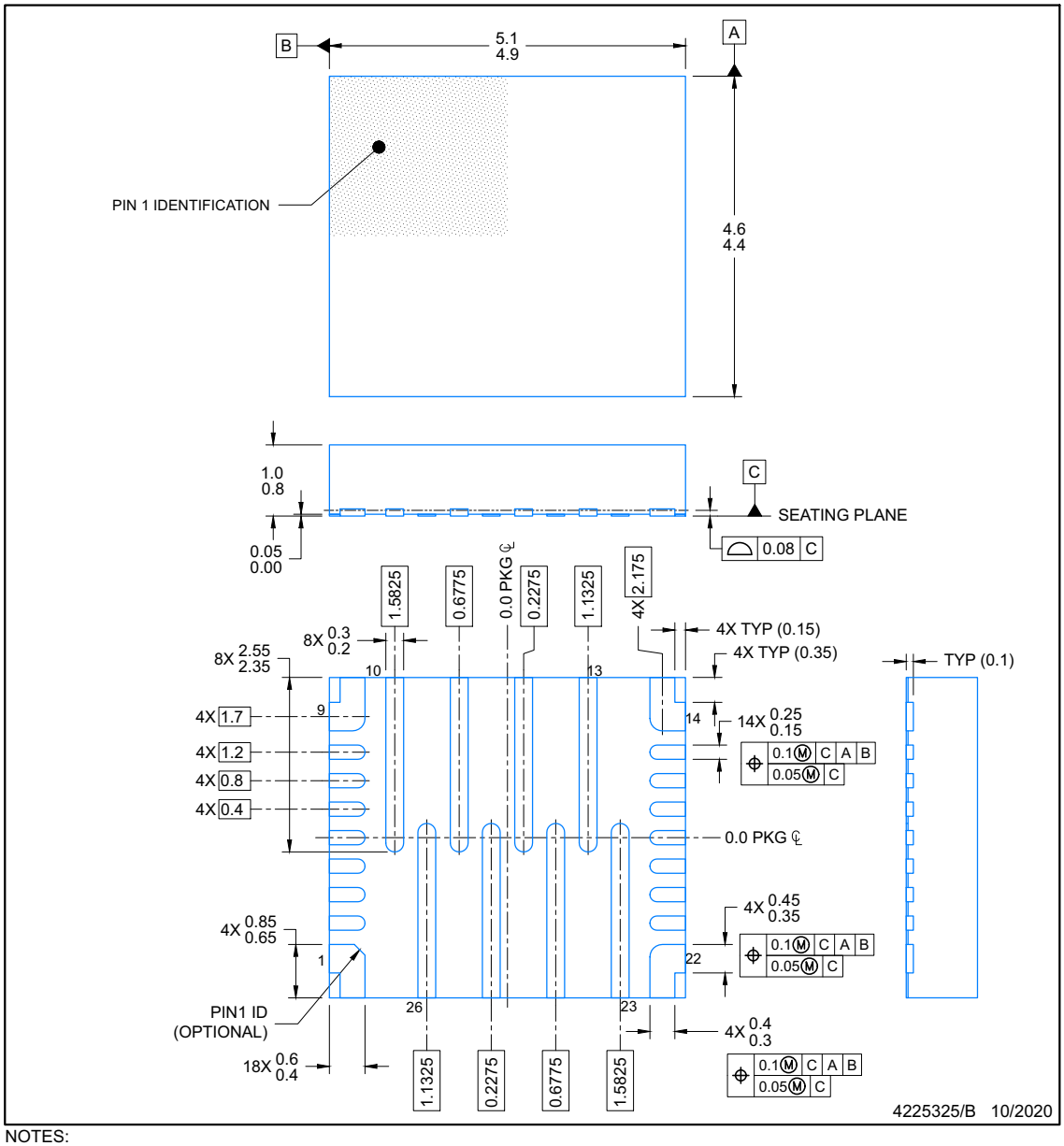
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS259850RQPR	VQFN	RQP	26	3000	210	185	35
TPS259850RQPR	VQFN	RQP	26	3000	210	185	35
TPS259851RQPR	VQFN	RQP	26	3000	210	185	35

PACKAGE OUTLINE

RQP0026A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

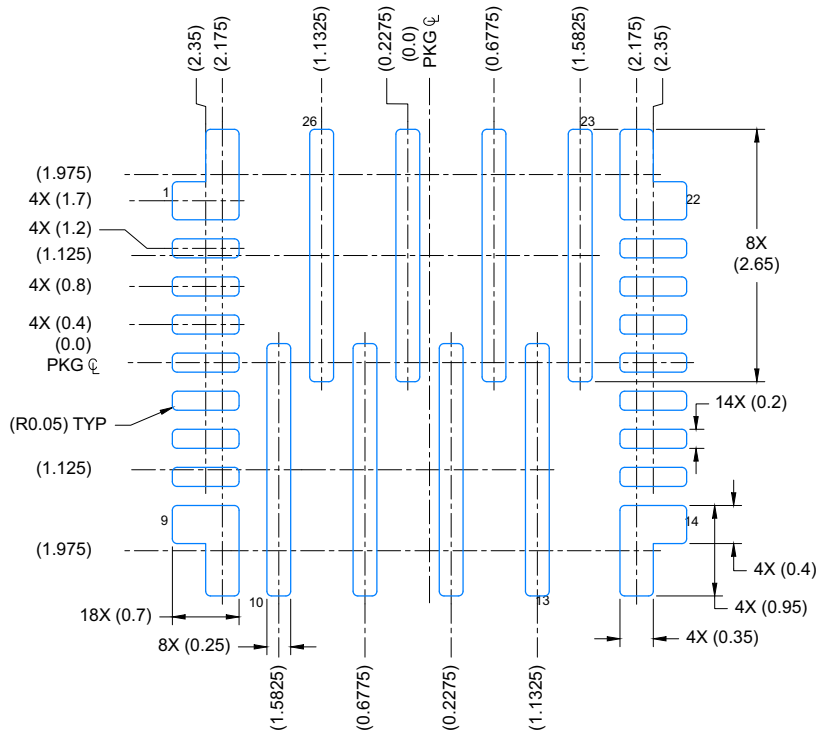
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

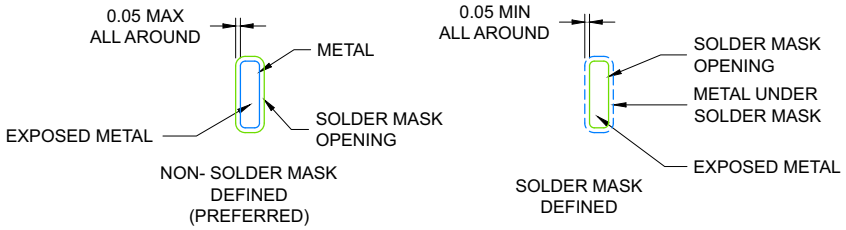
RQP0026A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

4225325/B 10/2020

NOTES: (continued)

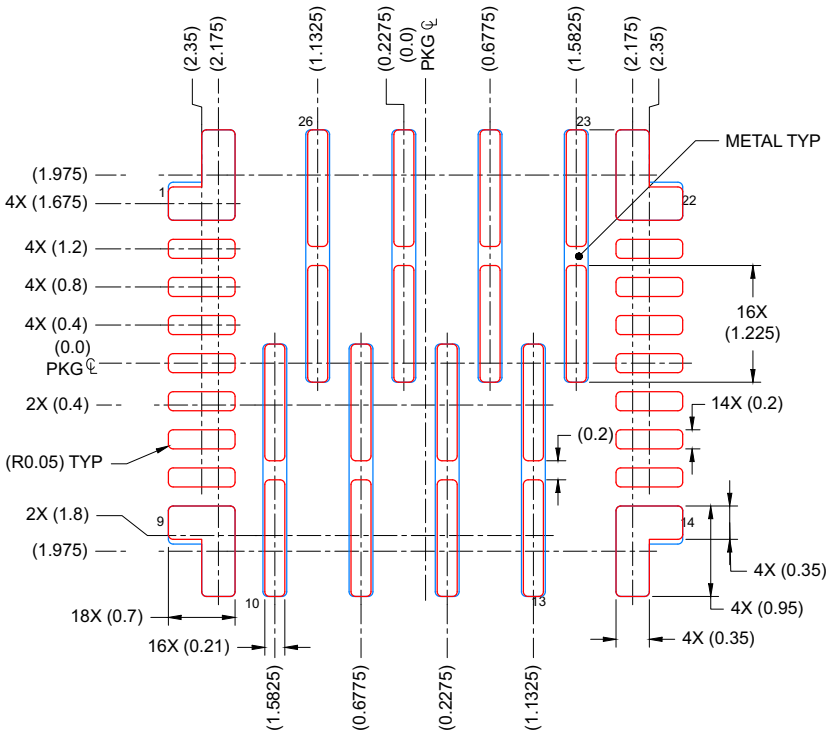
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RQP0026A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

PIN 1,9,14 & 22: 96%; PIN 10-13 & 23-26: 77%
SCALE: 15X

4225325/B 10/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS259850RQPR	ACTIVE	VQFN-HR	RQP	26	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS62843
SLVSFU8 – JANUARY 2022

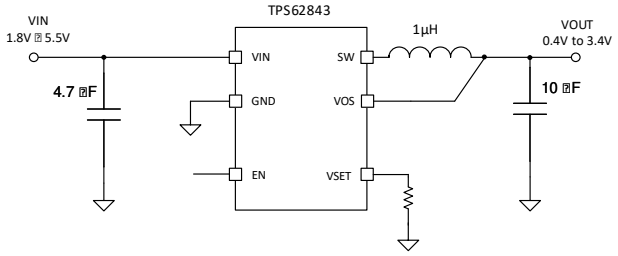
TPS62843 1.8-V to 5.5-V, 600-mA, 275-nA I_Q, Small Size Step-Down Converters

1 Features

- 1.8-V to 5.5-V input voltage range
- 0.4-V to 3.6-V output voltage range
- 275-nA typical quiescent current
- 600-mA output current
- 1% output voltage accuracy
- 20-nA typical shutdown current
- VSET pin-selectable output voltage though a single resistor
  - TPS628436: 0.4 V to 0.8 V
  - TPS628437: 0.8 V to 1.8 V
  - TPS628438: 1.8 V to 3.6 V
- Optimized for small passive components
  - 1-µH inductor
  - Down to 4.7-µF C_{OUT}
- Low output voltage ripple in power save mode
- RF-friendly and fast transient DCS-Control
- Automatic transition to no ripple 100% mode
- 0603-inductor and 0402-capacitor size supported
- Tiny 6-pin, 0.35-mm pitch WCSP package with 0.84mm² size
- Pin-to-pin compatible to the TPS6280x family (1 A)

2 Applications

- Wearable electronics
- Headsets/headphones and earbuds
- Mobile phones
- Medical sensor patches
- Hearing aid



Typical Application

3 Description

The TPS62843 is a high efficiency step-down converter family with ultra-low operating quiescent current of typically 275 nA. It features a 4-nA shutdown (typical) current when disabled.

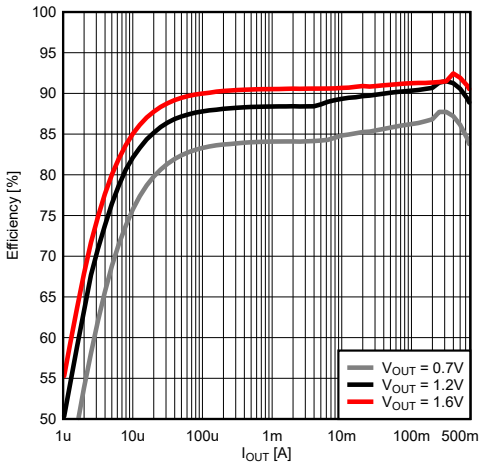
The device uses DCS-Control with a low and RF-friendly output voltage ripple to power radios.

The device operates with a typical switching frequency of 1.5 MHz and extends a high light-load efficiency down to 100-µA load current and below.

18 pre-defined output voltages can be selected by connecting a resistor to the VSET pin, making the family usable across various applications with a minimum set of passive components.

Device Information

Part Number	V_{OUT} Range	Body Size (NOM)
TPS628436	0.4 V–0.8 V	0.8 mm × 1.05 mm × 0.4 mm
TPS628437	0.8 V–1.8 V	0.8 mm × 1.05 mm × 0.4 mm
TPS628438	1.8 V–3.6 V	0.8 mm × 1.05 mm × 0.4 mm



Efficiency vs Output Current at 3.6 V_{IN}

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISON	NOTES
January 2022	*	Advance Information

5 Device Comparison Table

Device	Fixed V_{OUT} VSET = GND	Selectable Output Voltages	f_{SW} [MHz]	Soft Start t_{SS}	Inductor
TPS628436	Reserved	0.4V–0.8V in 25-mV steps	1.5	400 µs	1 µH
TPS628437	1.8 V	0.8V–1.6V in 50-mV steps	1.9	800 µs	1 µH
TPS628438	3.6 V	1.8V–3.4V in 100-mV steps	2.25	800 µs	1 µH

6 Pin Configuration and Functions

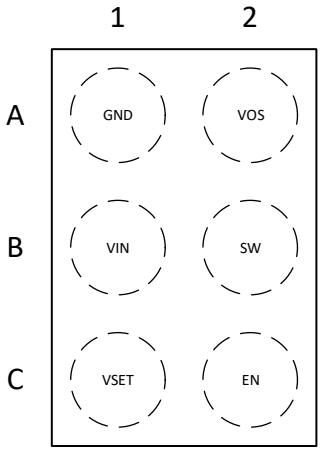


Figure 6-1. 6-Pin DSBGA YKA Package (Top View)

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VIN	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
VSET	C1	I	Connecting a resistor to GND selects a pre-defined output voltage.
VOS	A2	I	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
SW	B2	O	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
EN	C2	I	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	6	V
Pin voltage	SW, DC	–0.3	V_{IN} + 0.3 V	V
Pin voltage	SW, transient < 10 ns, while switching	–2.5	9	V
Pin voltage	VIN – SW, DC	—		V
Pin voltage	EN, VSET	–0.3	6	V
Pin voltage	VOS	–0.3	5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage, V_{IN}	1.8		5.5	V
I_{OUT}	Output current			0.6	A
L	Effective inductance	0.7	1.0	1.2	µH
C_{OUT}	Effective output capacitance	4		25	µF
C_{IN}	Effective input capacitance	0.5	4.7		µF
R_{SET}	Resistance range for external resistor at VSET pin (E96 1% resistor values)	4.87		124	kΩ
	External resistor tolerance E96 series at VSET pin			1%	
	E96 resistor series temperature coefficient (TCR)	–200		+200	ppm/°C
T_J	Operating junction temperature range	–40		125	°C

ADVANCE INFORMATION

7.3 Thermal Information

THERMAL METRIC		YKA (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

7.4 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 1.8 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current (power save mode)	Nonswitching, $V_{EN} = V_{IN}$, I_{OUT} = 0 µA, T_J = –40°C to 85°C		275	1500	nA
		Switching, $V_{EN} = V_{IN}$, I_{OUT} = 0 µA, V_{OUT} = 0.7 V		350		nA
I_{SD}	Shutdown current	V_{EN} = 0 V, VSET = GND, T_J = –40°C to 85°C		4	850	nA
UVLO						
$V_{UVLO(R)}$	Undervoltage lockout rising threshold	V_{IN} rising		1.75	1.8	V
$V_{UVLO(F)}$	Undervoltage lockout rising threshold	V_{IN} falling		1.65	1.7	V
$V_{UVLO(H)}$	Undervoltage lockout hysteresis			100		mV
VSET PIN						
$V_{SET(LKG)}$	VSET input leakage current	T_J = –40°C to 85°C		10	800	nA
$V_{SET(H)}$	VSET high-level detection	Voltage at VSET during start-up	1.0			V
R_{SET}	RSET accuracy		–4%		4%	
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	0.8			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN input leakage current	V_{EN} > 0.8 V, T_J = –40°C to 85°C		1	25	nA
$R_{EN;PD}$	EN internal pulldown resistance	EN pin to GND	425	500		kΩ
VOUT VOLTAGE						
V_{OUT}	DC output voltage accuracy	PWM operation	–1%		+1%	
V_{OUT}	TPS628436		0.4		0.8	V
	TPS628437		0.8		1.8	V
	TPS628438		1.8		3.6	V
$I_{VOS(LKG)}$	VOS input leakage current	TPS628436, $V_{EN} = V_{IN}$, V_{VOS} = 0.7 V, T_J = –40°C to 85°C				nA
		TPS628437, $V_{EN} = V_{IN}$, V_{VOS} = 1.2 V, T_J = –40°C to 85°C		100	400	nA
		TPS628438, $V_{EN} = V_{IN}$, V_{VOS} = 3.3 V, T_J = –40°C to 85°C				nA
f_{SW}	TPS628436	I_{OUT} = 400 mA		1.5		MHz
	TPS628437	I_{OUT} = 400 mA		1.9		MHz
	TPS628438	I_{OUT} = 400 mA		2.25		MHz
STARTUP						
t_{SS}	TPS628436 soft-start time	From V_{OUT}= 0% to V_{OUT}= 95% of V_{OUT} nominal		0.4	0.6	ms
	TPS628438 soft-start time			1.0	1.4	
	TPS628437 soft-start time			0.7	1.0	
	EN HIGH to start of switching delay	R2D = GND		250	460	µs
POWER STAGE						

ADVANCE INFORMATION

7.4 Electrical Characteristics (continued)

T_J = –40°C to +125°C, V_{IN} = 1.8 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V, I_{OUT} = 300 mA		170	260	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V, I_{OUT} = 300 mA		70	105	mΩ
	Leakage current into the SW pin	V_{SW} = 0.7 V, T_J = –40°C to 85°C		0	25	nA
	Leakage current into the SW pin	V_{SW} = 1.2 V, T_J = –40°C to 85°C		0	25	nA
	Leakage current into the SW pin	V_{VIN} > $V_{SW,}$, V_{SW} = 3.3 V, T_J = –40°C to 85°C		0	30	nA
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	Peak current limit on HS FET	0.9	1.1	1.3	A
$I_{LS(OC)}$	Low-side valley current limit	Valley current limit on LS FET	0.8	1.0	1.1	A
OUTPUT DISCHARGE						
	Output discharge resistor on the VOS pin	V_{EN} = GND, I(VOS) = –10 mA		7	17	Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		160		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS62843 is a high-frequency, synchronous step-down converter with ultra-low quiescent current of typically 275 nA in a 0.84-mm² chip size. The device operates with a tiny 1-µH inductor and 10-µF output capacitor over the entire recommended operation range to provide one of the industry's smallest chip and solution size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power save mode operation. TI's DCS-Control (Direct Control with Seamless Transition into power save mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

8.2 Functional Block Diagram

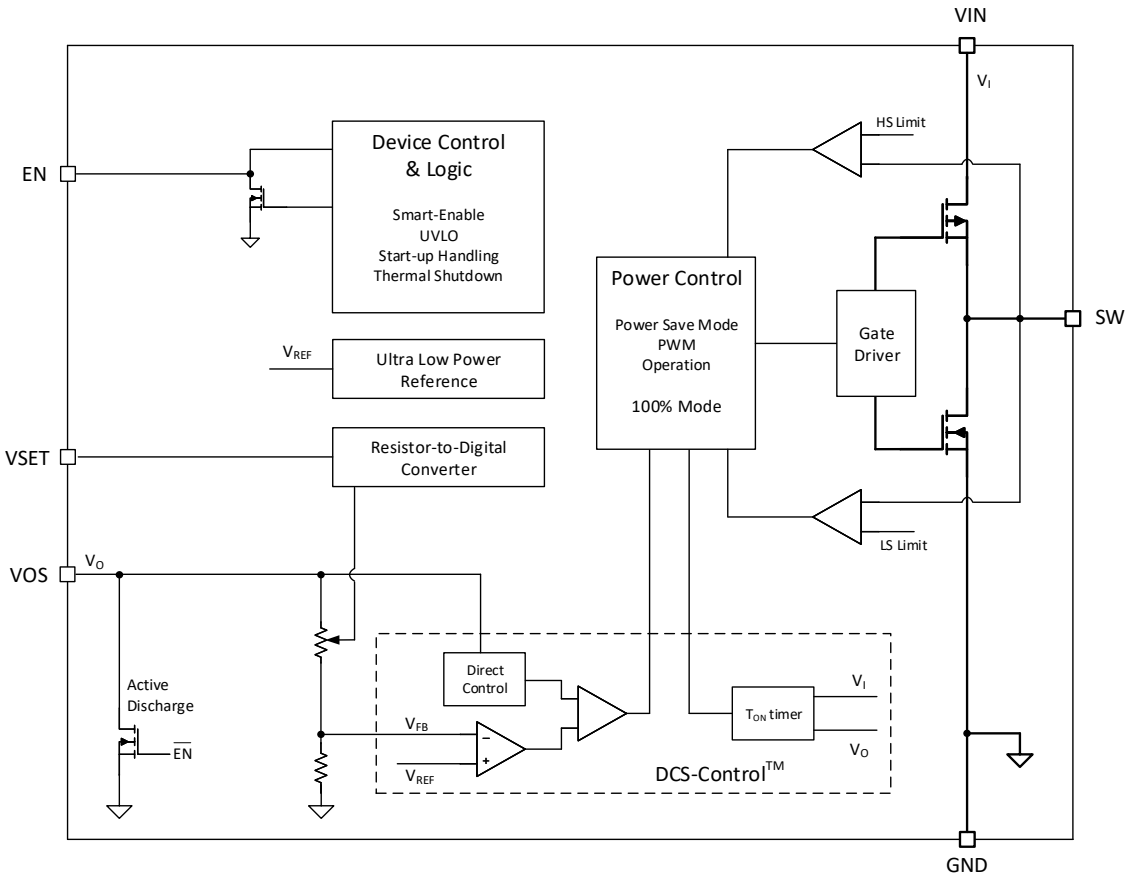


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Smart Enable and Shutdown (EN)

An internal 500-kΩ resistor pulls the EN pin to GND and avoids floating the pin. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

8.3.2 Soft Start

Once the device has been enabled with EN high, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time, $t_{Startup\_delay}$. Once $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, t_{ss}. See Figure 8-2.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSEL value. It is shortest with VSEL = 0 and longest with VSEL = 16.

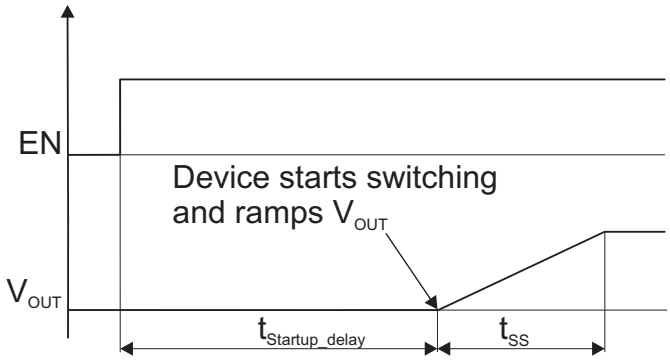


Figure 8-2. Device Start-Up

8.3.3 VSET Pin

This pin is used to define the output voltage selection during start-up of the converter. See Section 5.

8.3.4 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. Once the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor, R_{VSET}, within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. Once this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, ensure that there is no additional current path or capacitance greater than 30 pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. Table 8-1 lists the correct resistor values for R_{VSEL} to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor R_{SET} is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Ensure that there is no other leakage path than the R_{VSET} resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

Table 8-1. Output Voltage Setting

VSET	Output Voltage Setting [V]			R_{SET} [Ω]
	TPS628436	TPS628437	TPS628438	
1	0.400	0.80	1.8	10.0 k

Table 8-1. Output Voltage Setting (continued)

VSET	Output Voltage Setting [V]			R_{SET} [Ω]
	TPS628436	TPS628437	TPS628438	
2	0.425	0.85	1.9	12.1 k
3	0.450	0.90	2.0	15.4 k
4	0.475	0.95	2.1	18.7 k
5	0.500	1.00	2.2	23.7 k
6	0.525	1.05	2.3	28.7 k
7	0.550	1.10	2.4	36.5 k
8	0.575	1.15	2.5	44.2 k
9	0.600	1.20	2.6	56.2 k
10	0.625	1.25	2.7	68.1 k
11	0.650	1.30	2.8	86.6 k
12	0.675	1.35	2.9	105.0 k
13	0.700	1.40	3.0	133.0 k
14	0.725	1.45	3.1	162.0 k
15	0.750	1.50	3.2	205.0 k
16	0.775	1.55	3.3	249.0 k or larger
17	0.8	1.6	3.4	VIN
0	Reserved (contact TI)	1.8	3.6	GND

8.3.5 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (maximum) with falling V_{IN}. The device starts at an input voltage of 1.8 V (maximum) rising V_{IN}. Once the device re-enters operation out of an undervoltage lockout condition, it behaves like it does being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

8.3.6 Switch Current Limit/Short Circuit Protection

The TPS62843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, I_{LIMF} trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, I_{LIMF}, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature, T_{SD}, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set V_{OUT} (there is no R2D conversion of R_{VSEL}). The thermal shutdown is not active in power save mode.

8.3.8 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO-}$.

ADVANCE INFORMATION

8.4 Device Functional Modes

8.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275 nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency f_{sw} of typically 1.5 MHz (TPS628436), 1.9 MHz (TPS628437), or 2.25 MHz (TPS628438). The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

8.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

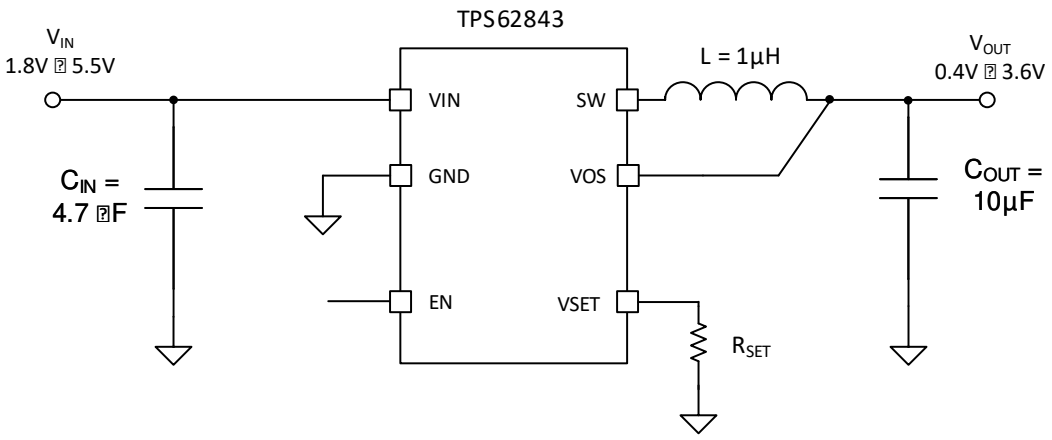


Figure 9-1. TPS62843 Typical Application Circuit

9.2.1 Design Requirements

Table 9-1 shows the list of components for the application circuit and the characteristic application curves.

Table 9-1. Components for Application Characteristic Curves

Reference	Description	Value	Size code Inch [metric L × W × T]	Manufacturer
TPS628436/ TPS628437/ TPS628438	275 nA-I_Q Buck Converter		[1.05 × 0.8 × 0.4 mm]	TI
C_{IN}	Ceramic CapacitorGRM155R60J475ME47D	4.7 µF	0402 [1.0 × 0.5 × 0.5 mm]	Murata
L	InductorDFE201610-1R0M	1 µH	0806 [2.0 × 1.6 × 1.0 mm]	Murata
C_{OUT}	Ceramic Capacitor GRM155R60J106ME15D	10 µF	0402 [1.0 × 0.5 × 0.5 mm]	Murata
R_{SET}	See voltage setting table		0402 [1.0 × 0.5 × 0.5 mm]	

9.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.

ADVANCE INFORMATION

9.2.3 Application Curves

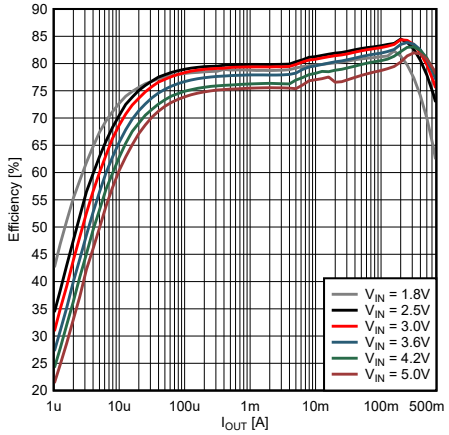


Figure 9-2. Efficiency at 0.4 V_{OUT}

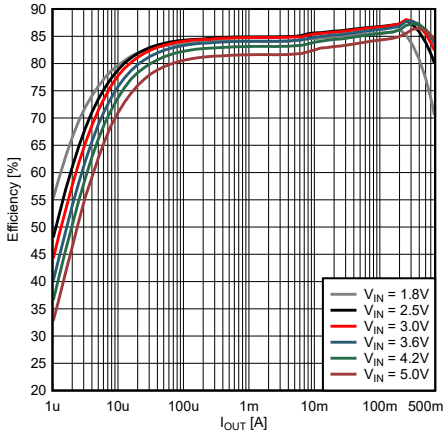


Figure 9-3. Efficiency at 0.7 V_{OUT}

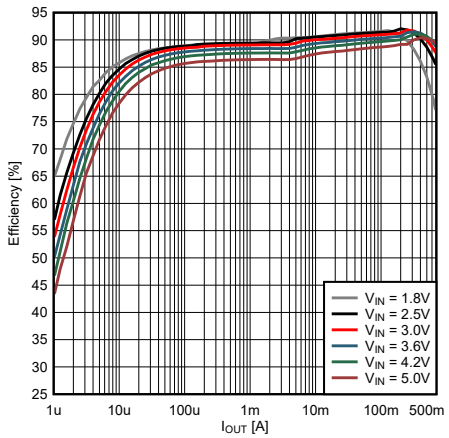


Figure 9-4. Efficiency at 1.2 V_{OUT}

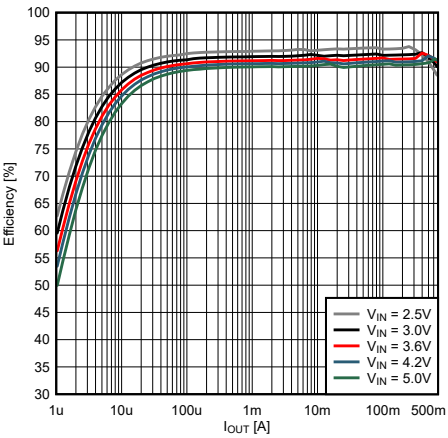


Figure 9-5. Efficiency at 1.8 V_{OUT}

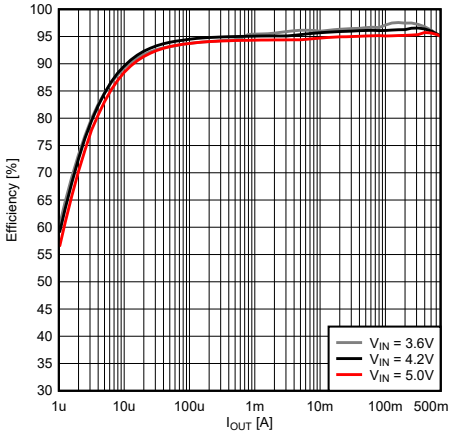


Figure 9-6. Efficiency at 3.3 V_{OUT}

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62843.

11 Layout

11.1 Layout Guidelines

The pinout of TPS62843 has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as CIN, COUT, and L. Furthermore, this pin out allows the user to connect tiny components such as 0201 (0603) size capacitors and 0402 (1005) size inductors. A solution size smaller than 5 mm^2 can be achieved with a fixed output voltage. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the VIN of the IC and GND pins. This is the most critical component placement. The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

11.2 Layout Example

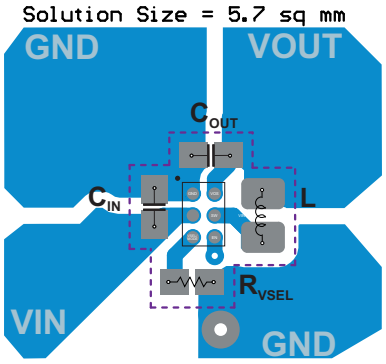


Figure 11-1. Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XPS628436YKAR	ACTIVE	DSBGA	YKA	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XPS628437YKAR	ACTIVE	DSBGA	YKA	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XPS628438YKAR	ACTIVE	DSBGA	YKA	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

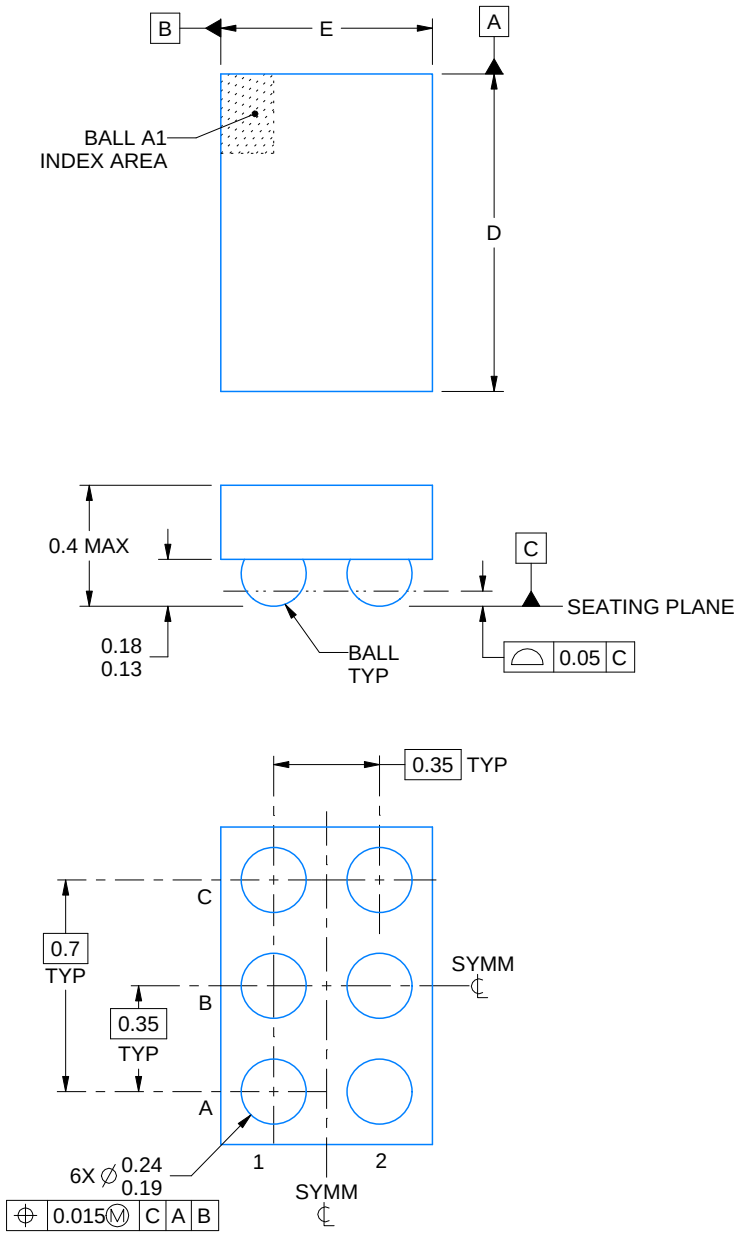
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY

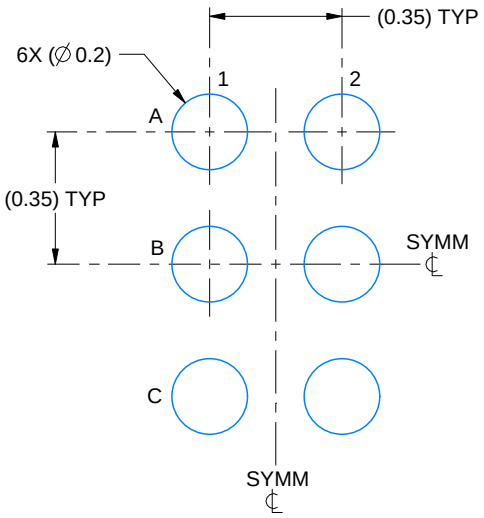


4223607/A 03/2017

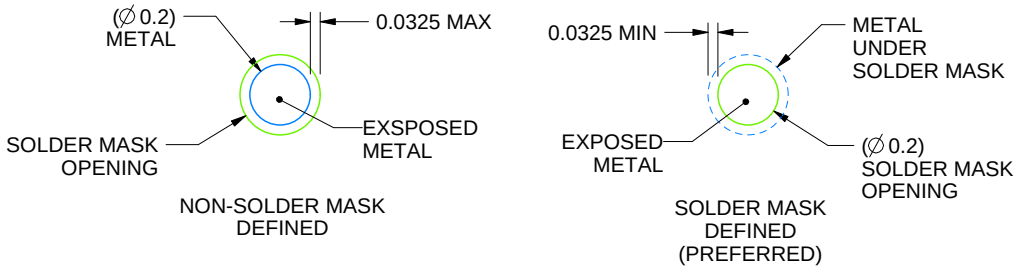
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223607/A 03/2017

NOTES: (continued)

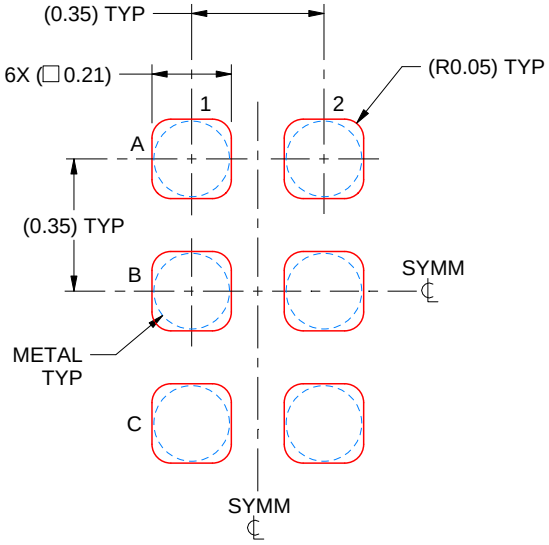
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

4223607/A 03/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

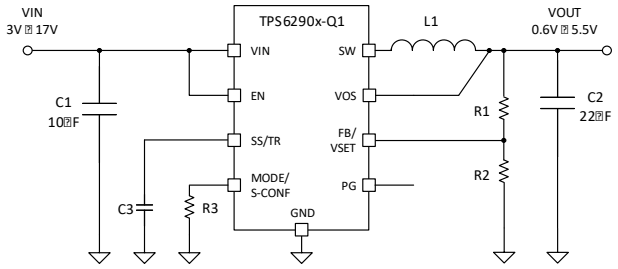
TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPS62903-Q1 3-V to 18-V, 3-A, Automotive Low I_Q Buck Converter with +165°C T_J

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Level 2 device HBM ESD classification
  - Level C4B CDM ESD classification
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Extended T_J range: up to 165°C
- High efficiency DCS-Control topology
  - $R_{DS(ON)}$: 62-mΩ high side, 22-mΩ low side
  - Seamless PWM/PFM transition
  - Internal compensation
- 4-µA low I_Q (typical)
- Up to 3-A continuous output current
- ±1% feedback voltage accuracy across temp
- Configurable output voltage options:
  - 0.6-V to 5.5-V V_{FB} external divider
  - V_{SET} internal divider
    - 16 options between 0.4 V and 5.5 V
- Flexibility through the MODE/S-CONF pin
  - 2.5-MHz or 1.0-MHz switching frequency
  - Forced PWM or auto PFM (power save mode) with dynamic mode change option
  - Output discharge on and off
- No external bootstrap capacitor required
- Overcurrent and overtemperature protection
- 100% duty cycle mode
- Precise enable input
- Adjustable soft start and tracking
- Power-good output
- Optimized pinout for single-layer routing
- Wettable 2.2-mm × 2.0-mm VQFN package with 0.5-mm pitch
- Create a custom design with the TPS62903-Q1 using the WEBENCH® Power Designer



Simplified Schematic

2 Applications

- ADAS
- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric, and powertrain systems

3 Description

The TPS62903-Q1 is a highly efficient, small, and flexible synchronous step-down DC-DC converter that is easy to use. A selectable switching frequency of 2.5 MHz or 1.0 MHz allows the use of small inductors and provides fast transient response. The device supports high V_{OUT} accuracy of ± 1% with the DCS-Control topology. The wide 3-V to 18-V input voltage range supports a variety of nominal inputs, like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

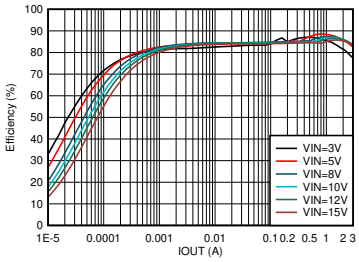
The TPS62903-Q1 can automatically enter power save mode (if auto PFM or PWM is selected) at light loads to maintain high efficiency. Additionally, to provide high efficiency at very small loads, the device has a low typical quiescent current of 4 µA. AEE, if enabled, provides high efficiency across V_{IN}, V_{OUT}, and load current. The device includes a MODE/Smart-CONF input to set the internal and external divider, switching frequency, output voltage discharge, and automatic power save mode or forced PWM operation.

The device is available in small 9-pin VQFN package measuring 2.20 mm × 2.00 mm with 0.5-mm pitch with wettable flank.

Device Information

Part Number	Package(1)	Body Size (NOM)
TPS62903-Q1	Wettable flank VQFN-HR	2.20 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency Versus Output Current (1.2 V_O at 2.5 MHz, 1 µH, Auto PFM or PWM)

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
May 2022	*	Advance Information

5 Device Comparison Table

Device Number	Output Current	Input Voltage	Operating Temperature Range	Switching Frequency	PWM Mode	V_O Adjust
TPS62903-Q1	0 A–3 A	3 V–18 V	–40°C to 165°C	Selectable 1-MHz or 2.5-MHz options	Selectable auto PWM/PFM or forced PWM	Externally programmable or 16 internal options
TPS62902-Q1	0 A–2 A					
TPS62901-Q1	0 A–1 A					
TPS62903	0 A–0.3 A	3 V–18 V	–40°C to 125°C	Selectable 1-MHz or 2.5-MHz options	Selectable auto PWM/PFM or forced PWM	Externally programmable or 16 internal options
TPS62902	0 A–2 A					
TPS62901	0 A–1 A					
TPS62903E	0 A–3 A		–55°C to 165°C			

ADVANCE INFORMATION

6 Pin Configuration and Functions

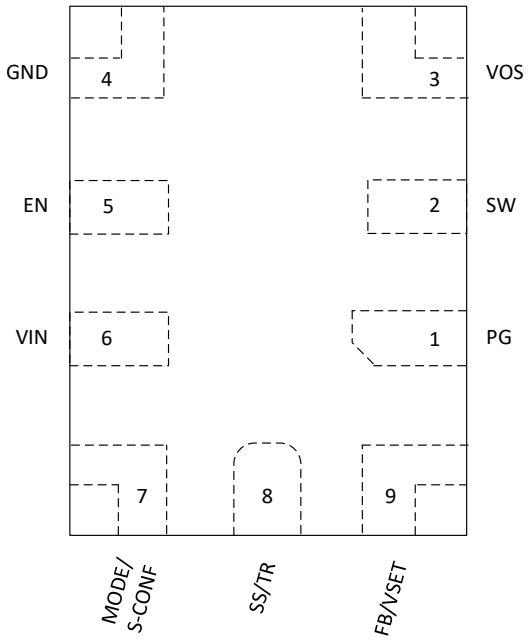


Figure 6-1. 9-Pin RPJ VQFN Package (Top View, Device Pins Face Down)

Table 6-1. Pin Functions

Pin		Type[1]	Description
Name	Number		
PG	1	O	Open-drain power good output. High = V_{OUT} is ready. Low = V_{OUT} is below nominal regulation. This pin requires a pullup resistor.
SW	2	—	Switch pin of the converter and is connected to the internal power switches. Connect the inductor between SW and the output capacitor.
VOS	3	I	Output voltage sense pin. Connect directly to the positive pin of the output capacitor.
GND	4	—	Ground pin. This pin must be connected directly to the common ground plane.
EN	5	I	Enable input pin. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
VIN	6	I	Power supply input pin. Ensure the input capacitor is connected as close as possible between the VIN and GND pins.
MODE/ S-CONF	7	I	Device mode selection (auto PFM/PWM or forced PWM operation) and SmartConfig™ pin. Connect high, low, or to a resistor to configure the device according to Table 8-1. Do not leave this pin unconnected.
SS/TR	8	I	Soft start and tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing. The pin can be left floating for the fastest ramp-up time.
FB/VSET	9	I	Depends on device configuration (see Section 8.3.1.) • FB: Voltage feedback input. Connect a resistive output voltage divider to this pin. • VSET: Output voltage setting pin. Connect a resistor to GND to choose the output voltage according to Table 8-2.

(1) O = output, I = input

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG, MODE/S-CONF	–0.3	19.5	V
Voltage(2)	SW (3)	–0.3	V_{IN} + 0.3	V
Voltage(2)	SW (AC, less than 10 ns)(3)	–3.0	23	V
Voltage(2)	FB/VSET, SS/TR, VOS	–0.3	6	V
T_J	Junction temperature	–55	165	°C
T_{stg}	Storage temperature	–65	165	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 HBM ESD Classification Level 2, all pins(1)		±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC-Q100-011 CDM ESD Classification level C4B	All pins	±500	V
			Corner pins (3, 4, 7, and 9)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3.0		18	V
V_O	Output voltage range	0.4		5.5	V
C_I	Effective input capacitance	3	10		µF
C_O	Effective output capacitance (2.5-MHz selection)(1)	10	22	100 (1)	µF
C_O	Effective output capacitance (1-MHz selection)(1)	10	22	100 (1)	µF
L	Output inductance(2)	1	2.2	4.7(3)	µH
I_{OUT}	Output current	0		3	A
I_{SINK_PG}	Sink current at the PG pin			1	mA
T_J	Junction temperature (4)	–40		165	°C

(1) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitor.
(2) Nominal inductance value
(3) Larger values of inductance can be used to reduce the ripple current, but they can have a negative impact on efficiency and the overall transient response.
(4) Operating lifetime is derated at junction temperatures greater than 165°C.

ADVANCE INFORMATION

7.4 Thermal Information

THERMAL METRIC(1)		SOT583 (8)		UNIT
		JEDEC PCB	TPS6290xEVM-xxx	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.2	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.4	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	28	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_I = 3 V to 18 V, T_J = –40°C to +165°C, typical values at V_I = 12 V and T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current (power save mode)	I_{OUT} = 0 mA, device not switching		4		µA
$I_{Q;PWM}$	Operating quiescent current (PWM mode)	V_{IN} = 12 V, V_{OUT} = 1.2 V; I_{OUT} = 0 mA, device switching		8		mA
I_{SD}	Shutdown current into the VIN pin	EN = 0 V, T_J = –40°C to 150°C		0.27	3.5	µA
V_{UVLO}	Undervoltage lockout	V_{IN} rising, T_J = –40°C to 150°C	2.85	2.925	3.0	V
	Undervoltage lockout	V_{IN} falling	2.7	2.775	2.85	V
V_{UVLO}	Undervoltage lockout hysteresis			130		mV
CONTROL AND INTERFACE						
I_{LKG}	EN input leakage current	EN = 5 V		10	310	nA
$V_{IH;MODE}$	High-level input voltage at the MODE/S-CONF pin		1.0			V
$V_{IL;MODE}$	Low-level input voltage at the MODE/S-CONF pin				0.15	V
T_{SD}	Thermal shutdown threshold	T_J rising	168	175	185	°C
	Thermal shutdown threshold	T_J falling		12.5		
V_{IH}	High-level input voltage at the EN pin		0.97	1.0	1.03	V
V_{IL}	Low-level input voltage at the EN pin		0.820	0.850	0.880	V
V_{PG}	Power-good threshold	V_{FB} rising, referenced to V_{FB} nominal	93.5%	96%	99%	
		V_{FB} falling, referenced to V_{FB} nominal	88.5%	92%	96%	
V_{PG_HYS}	Power-good threshold hysteresis		1.5%	3.5%	6%	
$V_{PG,OL}$	Low-level output voltage at the PG pin	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into the PG pin	V_{PG} = 5 V		25	550	nA
$t_{PG,DLY}$	Power-good delay time	V_{FB} rising and falling		32		µs
R_{SET}	VSET resistor tolerance		–4%		+4%	
C_{SET}	Maximum capacitance connected to the VSET pin				30	pF
POWER SWITCHES						
$I_{LKG;SW}$	Leakage current into the SW pin	EN = 0 V, V_{SW} = V_{OS} = 5.5 V		2	7	µA
$R_{DS;ON}$	High-side FET on resistance	V_{IN} > 4 V, I_{SW} = 500 mA		62	111	mΩ
	Low-side FET on resistance	V_{IN} > 4 V, I_{SW} = 500 mA		22	41	
I_{LIM}	High-side FET current limit		4	4.6	5.5	A
	Low-side FET current limit		4.0	4.4	5.0	A
$I_{LIM;SINK}$	Low-side FET sink current limit		1.3	1.7	2.5	A

ADVANCE INFORMATION

V_I = 3 V to 18 V, T_J = –40°C to +165°C, typical values at V_I = 12 V and T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	2.5-MHz selection		2.5		MHz
$T_{ON(MIN)}$	Minimum on time			30		ns
f_{SW}	Switching frequency	1.0-MHz selection		1.0		MHz
OUTPUT						
V_{O_Reg1}	Output voltage regulation	VSET configuration selected, T_J = 25°C	–0.9%		+0.9%	
V_{O_Reg4}	Output voltage regulation	VSET configuration selected	–1.5%		+1.5%	
V_{FB}	Feedback regulation voltage	Adjustable configuration selected		0.6		V
V_{FB_Reg1}	Feedback regulation voltage	FB option selected. T_J = 25°C	–0.6%		+0.6%	
V_{FB_Reg4}	Feedback regulation voltage	FB option selected	–1.25%		+1.25%	
I_{FB}	Input leakage current into the FB pin	Adjustable configuration, VFB = 0.6 V		1	70	nA
T_{delay}	Start-up delay time	I_O = 0 mA, time from EN = HIGH until start switching, adjustable configuration selected		600	1400	µs
	Start-up delay time	I_O = 0 mA, time from EN = HIGH until start switching, VSET configuration selected. The typical value is based on the first option of the VSET configuration.		650	1850	µs
T_{SS}	Soft-start time	I_O = 0 mA after T_{delay}, from first switching pulse until target V_O , C_{SS} = Open		150	200	µs
I_{SS}	SS/TR source current		2.3	2.5	2.7	µA
$V_{FB}/V_{SS/TR}$	Tracking gain, adjustable configuration			0.75		
$V_{FB}/V_{SS/TR}$	Tracking gain tolerance		–8		+8	mV
R_{DISCH}	Active discharge resistance	Discharge = ON option selected, EN = LOW		7.5	25	Ω

ADVANCE INFORMATION

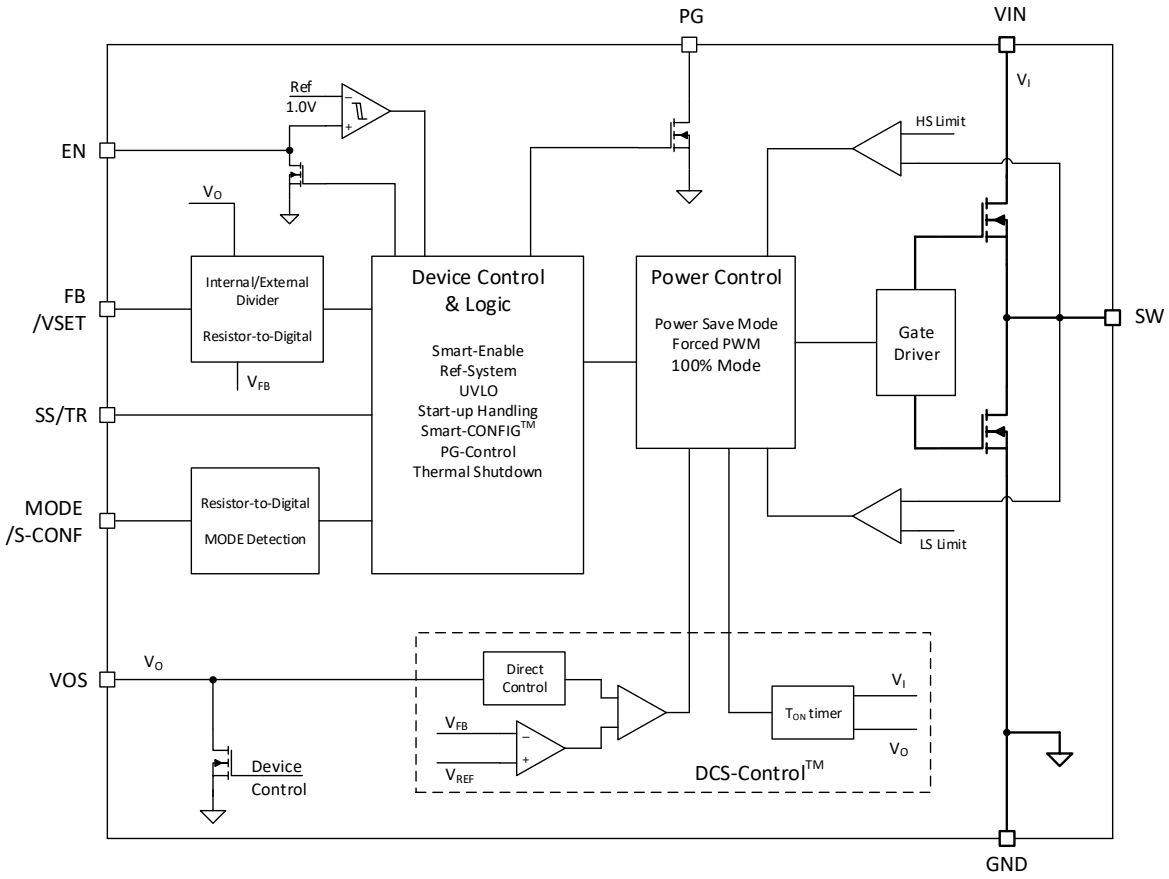
ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS62903-Q1 synchronous switched mode power converters are based on DCS-Control (Direct Control with Seamless Transition into power save mode). DCS-Control is an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control. This control loop takes information about output voltage changes and feeds the information directly to a fast comparator stage. DCS-Control sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Mode Selection and Device Configuration MODE/S-CONF

With MODE/S-CONF (SmartConfig), this device features an input with two functions. This pin can be used to customize the device behavior in two ways:

- Select the device mode (FPWM or auto PFM or PWM with AEE operation) traditionally with a HIGH-level or LOW-level.
- Select the device configuration (switching frequency, internal or external feedback, output discharge, and PFM/PWM mode) by connecting a single resistor to the MODE/S-CONF pin.

The device interprets this pin during the start-up sequence after the internal OTP readout and before the device starts switching in soft start. If the device reads a HIGH-level or LOW-level, dynamic mode change is active and PFM or PWM mode can be changed during operation. If the device reads a resistor value, there is no further interpretation during operation and device mode or other configurations cannot be changed afterward.

Note

The MODE/S-CONF pin must not be left floating. Connect the pin high, low, or to a resistor to configure the device according to Table 8-1.

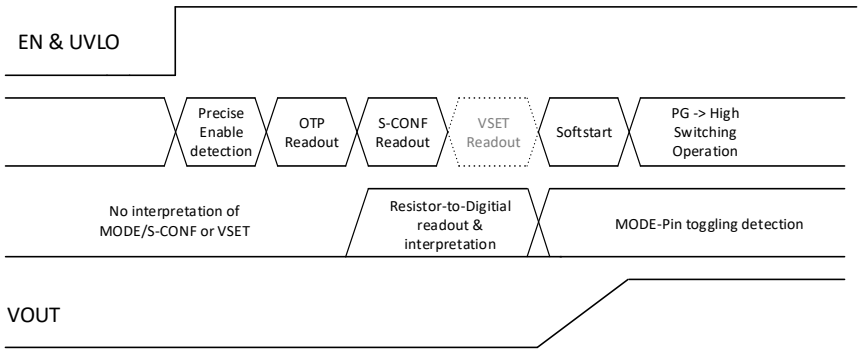


Figure 8-1. Interpretation of S-CONF and VSET Flow

ADVANCE INFORMATION

Table 8-1. SmartConfig Setting Table

#	Level Or Resistor Value [Ω] (1)	FB/VSET Pin	F_{SW} (MHz)	Output Discharge	Mode (Auto Or Forced PWM)	Dynamic Mode Change
	Setting Options by Level					
1	GND	External FB	2.5(1)	yes	Auto PFM/PWM with AEE	Active
2	HIGH (> V_{IH_MODE})	External FB	2.5	yes	Forced PWM	
	Setting Options by Resistor					
3	7.15 k	External FB	2.5(1)	no	Auto PFM/PWM with AEE	Not active
4	8.87 k	External FB	2.5	no	Forced PWM	
5	11.0 k	External FB	1	yes	Auto PFM/PWM	
6	13.7 k	External FB	1	yes	Forced PWM	
7	16.9 k	External FB	1	no	Auto PFM/PWM	
8	21.0 k	External FB	1	no	Forced PWM	
9	26.1 k	VSET	2.5(1)	yes	Auto PFM/PWM with AEE	
10	32.4 k	VSET	2.5	yes	Forced PWM	
11	40.2 k	VSET	2.5(1)	no	Auto PFM/PWM with AEE	
12	49.9 k	VSET	2.5	no	Forced PWM	
13	61.9 k	VSET	1	yes	Auto PFM/PWM	
14	76.8 k	VSET	1	yes	Forced PWM	
15	95.3 k	VSET	1	no	Auto PFM/PWM	
16	118 k	VSET	1	no	Forced PWM	

(1) E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C

8.3.2 Adjustable V_O Operation (External Voltage Divider)

The TPS62903-Q1 can be programmed by the MODE/S-CONF pin to either classical configuration where the FB/VSET pin is used as the feedback pin, sensing V_O through an external resistive divider. The TPS62903-Q1 can also be programmed to 16 different fixed output voltages. These are set through an external resistor between the FB/VSET pin and GND. In this configuration, V_O is directly sensed at the VOS pin of the device.

If the device is configured to operate in classical adjustable V_O operation, the FB/VSET pin is used as the feedback pin and needs to sense V_O through an external divider network. Figure 8-2 shows the typical schematic for this configuration.

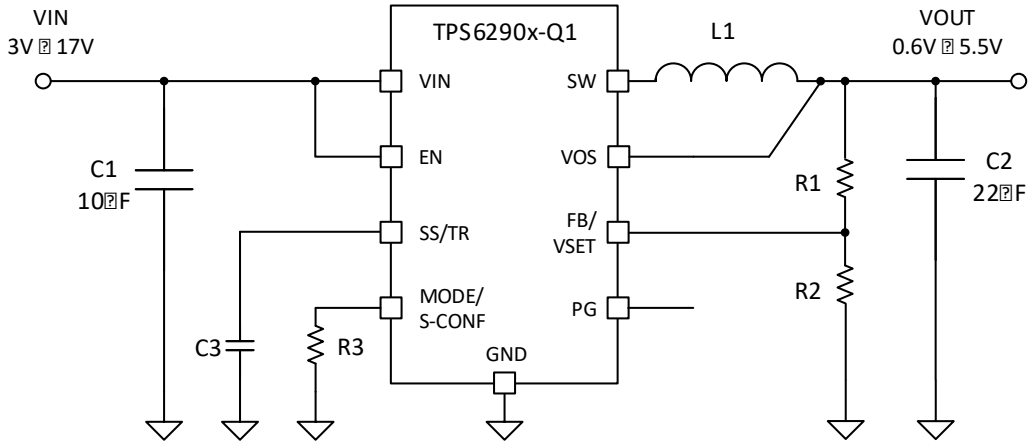


Figure 8-2. Adjustable V_O Operation Schematic

8.3.3 Selectable V_O Operation (VSET and Internal Voltage Divider)

If the device is configured to VSET operation, V_O is sensed only through the VOS pin by an internal resistor divider. The target V_O is programmed by an external resistor connected between the VSET pin and GND. Figure 8-3 shows the typical schematic for this configuration.

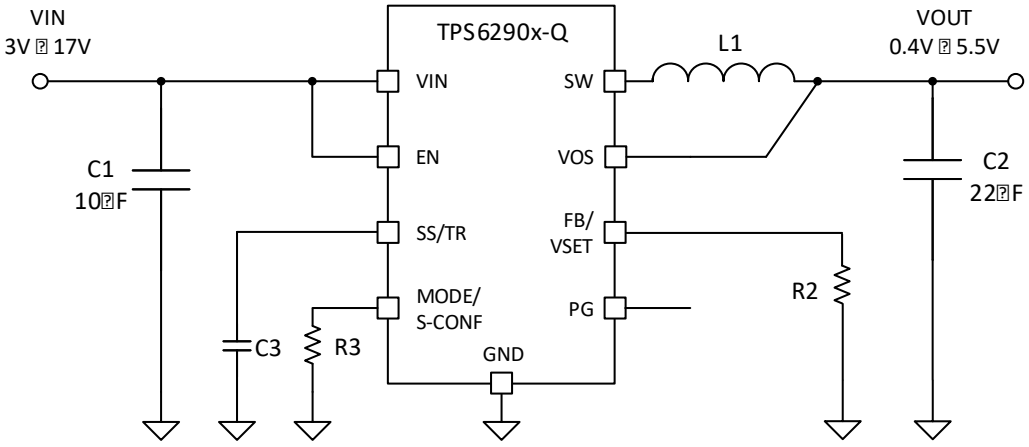


Figure 8-3. Selectable V_O Operation Schematic

Table 8-2. VSET Selection Table

#	Level Or Resistor Value [Ω] (1)	Target V_O [V]
1	GND	1.2
2	4.64 k	0.4
3	5.76 k	0.6
4	7.15 k	0.8
5	8.87 k	1.0
6	11.0 k	1.1
7	13.7 k	1.3
8	16.9 k	1.35
9	21.0 k	1.8
10	26.1 k	1.9
11	40.2 k	2.5
12	61.9 k	3.8
13	76.8 k	5.0
14	95.3 k	1.25
15	118.0 k	5.5
16	249.00 k or larger/Open	3.3

(1) E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C

8.3.4 Soft Start and Tracking (SS/TR)

With the SS/TR pin, the user can adjust the soft-start behavior and track an external voltage. See Section 9.2.2.6 for operation details.

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and makes sure there is a controlled output voltage rise time. The soft-start circuitry also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay, then the internal reference, and hence V_O, rises with a slope controlled by an external capacitor connected to the SS/TR pin.

ADVANCE INFORMATION

Leaving the SS/TR pin unconnected provides the fastest start-up, limited internally (the pin must not be pulled LOW externally).

If the device is set to shut down (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to make sure there is a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used to track another system voltage rail. The output voltage follows this voltage up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current.

8.3.5 Smart Enable with Precise Threshold

The voltage applied at the enable pin of the TPS62903-Q1 is compared to a fixed threshold rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input allows the user to program the undervoltage lockout by adding a resistor divider to the input of the EN pin.

The enable input threshold for a falling edge is lower than the rising edge threshold. The TPS62903-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

An internal resistor pulls the EN pin to GND when the device is disabled and avoids the pin to be floating (once the device is enabled, the pulldown is removed). This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to a low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

8.3.6 Power Good (PG)

The TPS62903-Q1 has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. V_{IN} must remain present for the PG pin to stay low.

If the power-good output is not used, it is recommended to tie to GND or leave it open.

Table 8-3. Power Good Indicator Functional Table

Logic Signals				PG Status
V_{IN}	EN Pin	Thermal Shutdown	V_{OUT}	
V_{IN} > UVLO	HIGH	No	V_{OUT} on target	High Impedance
			V_{OUT} < target	LOW
		Yes	×	LOW
	LOW	×	×	LOW
1.8 V< V_{IN} < UVLO	×	×	×	LOW
V_{IN} < 1.8 V	×	×	×	Undefined

Note

For prebiased V_{OUT} conditions (during start up) of 60% or more of the programmed output voltage, a minimum 250-µs external soft start (C_{SS} > 0.75 nF) is required. If the 250-µs soft start minimum is not ensured and V_{OUT} is prebiased above 60% of the programmed output voltage during start-up, PG can be seen asserted "early" before V_{OUT} reaches the PG rising threshold, a glitch on PG can be observed, or both.

ADVANCE INFORMATION

8.3.7 Output Discharge Function

The purpose of the discharge function is to make sure there is a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS62903-Q1 has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.

8.3.8 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

8.3.9 Current Limit And Short Circuit Protection

The TPS62903-Q1 is protected against overload and short circuit events. If the inductor current exceeds the high-side FET current limit (I_{LIMH}), the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side FET current limit threshold.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given as Equation 1:

$$I_{peak\ typ)} = (I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (1)$$

where

- I_{LIMH} is the static high-side FET current limit as specified in the *Electrical Characteristics*.
- L is the effective inductance at the peak current.
- V_L is the voltage across the inductor (V_{IN}–V_{OUT}).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductance is used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{VIN - VOUT}{L} \times 50ns \quad (2)$$

The TPS62903-Q1 also includes a low-side negative current limit ($I_{LIM:SINK}$) to protect against excessive negative currents that can occur in forced PMW mode under heavy to light load transient conditions. If the negative current in the low-side switch exceeds the $I_{LIM:SINK}$ threshold, the low-side switch is disabled. Both the low-side and high-side switches remain off until an internal timer re-enables the high-side switch based on the selected PWM switching frequency.

CAUTION

It is recommended that the inductor be sized such that the inductor ripple current, ΔI_L (see Section 8.4.3), does not exceed 2.6 A to avoid the potential for continuous operation of the negative current limit with no output load (I_O = 0 A).

8.3.10 High Temperature Specifications

The TPS62903-Q1 is capable of high operating junction temperatures up to 165°C. The AEC-Q100 Grade-1 maximum ambient temperature requirement (T_{A_max} = 125°C) combined with power dissipation on integrated chips often results in device operating temperatures well above 125 °C. Additionally, although Grade 1 with extended temperature does not exist as a standard by itself, the 165°C maximum operating junction temperature

ADVANCE INFORMATION

allows for the TPS62903-Q1 to be used in applications with ambient temperatures upwards of 150°C that require less device power dissipation.

Note

For more information on the different thermal metrics for semiconductor integrated circuits (ICs) including the relationship between the operating junction (T_J) and ambient (T_A) temperatures of a device, refer to the *Semiconductor and IC Package Thermal Metrics* application report.

The TPS62903-Q1 is designed to sustain these high temperatures while maintaining performance and reliability, which is accomplished by compliant electrical specifications up to T_J = 165°C. In addition, extra reliability testing has been performed that exceeds the AEC-Q100 Grade 1 requirements.

The TPS62903-Q1 passes the temperature profile displayed in Table 8-4.

Table 8-4. Power On Hours (POH) Profile

Junction Temperature (°C)(1)	Hours	%
–40°C to 0°C	720	6
0°C to 50°C	2400	20
50°C to 100°C	7800	65
100°C to 150°C	840	7
150°C to 155°C	120	1
155°C to 165°C	120	1

(1) Due to the variety of voltage and current levels used across different applications, the operating temperature ranges are provided as junction temperature instead of ambient temperature.

Table 8-4 shows an automotive profile of time and temperature for the TPS62903-Q1 converter application specified with 12,000 POH. Power-On Hours (POH) reliability for the TPS62903-Q1 is a function of power dissipation, temperature, and time. Increased usage at higher loads or temperatures results in a reduction in the total POH.

8.3.11 Thermal Shutdown

The junction temperature, T_J, of the device is monitored by an internal temperature sensor. If T_J rises and exceeds the thermal shutdown threshold, T_{SD}, the device shuts down. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis, the converter resumes normal operation, beginning with soft start. During a PFM skip pause, the thermal shutdown feature is not active. A shutdown or restart is only triggered during a switching cycle. See Section 8.4.2.

ADVANCE INFORMATION

8.4 Device Functional Modes

8.4.1 Forced Pulse Width Modulation (FPWM) Operation

The TPS62903-Q1 has two operating modes: forced PWM mode discussed in this section and PWM and PFM as discussed in Section 8.4.2.

With the MODE/S-CONF pin configured for FPWM mode, the TPS62903-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of either 2.5 MHz or 1.0 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT}, and the inductance. The on time in forced PWM mode is given by Equation 3:

$$TON = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{sw}} \tag{3}$$

For very small output voltages, a minimum on time of approximately 30 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high.

8.4.2 Power Save Mode Operation (Auto PFM and PWM)

When the MODE/S-CONF pin is configured for power save mode (auto PFM and PWM). The device operates in PWM mode as long the output current is higher than half of the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). PSM occurs if the output current becomes smaller than half of the ripple current of the inductor. Power save mode is entered seamlessly when the load current decreases, which makes sure there is a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition in and out of power save mode is seamless in both directions.

In addition to adjusting the switching, the TPS62903-Q1 adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain highest efficiency using the AEE function when 2.5 MHz is selected as described in Section 8.4.3.

In power save mode, the TON time can be estimated using Equation 3 for 1 MHz and Equation 7 for 2.5 MHz.

For very small output voltages, an absolute minimum on time of approximately 30 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Using TON, the typical peak inductor current in power save mode is approximated by Equation 4:

$$ILPSM_{(peak)} = \frac{(VIN - VOUT)}{L} \times TON \tag{4}$$

The output voltage ripple in power save mode is given by Equation 5:

$$\Delta V = \frac{L \times VIN^2}{200 \times C} \left(\frac{1}{VIN - VOUT} + \frac{1}{VOUT} \right) \tag{5}$$

where

- L is the effective inductance.
- C is the output effective capacitance.

Note

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS62903-Q1 does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

ADVANCE INFORMATION

8.4.3 AEE (Automatic Efficiency Enhancement)

When the MODE/S-CONF pin is configured for AEE mode, the TPS62903-Q1 provides the highest efficiency over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter. This adjustment is achieved by setting the predictive off time of the converter. The efficiency of a switched mode converter is determined by the power losses during the conversion. The efficiency decreases if V_{OUT} decreases, V_{IN} increases as shown in Equation 6, or both. To keep the efficiency high over the entire duty cycle range (V_{OUT} / V_{IN} ratio), the switching frequency is adjusted while maintaining the ripple current.

$$F_{sw}(MHz) = 10 \times V_{OUT} \times \frac{V_{IN} - V_{OUT}}{V_{IN}^{\ 2}} \tag{6}$$

The AEE function in the TPS62903-Q1 adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain highest efficiency. The on time in steady-state operation can be estimated as using Equation 7:

$$TON = 100 \times \frac{VIN}{VIN - VOUT}\,[ns] \tag{7}$$

Equation 8 shows the relation among the inductor ripple current, switching frequency, and duty cycle.

$$\Delta I_L = V_{OUT} \times \left(\frac{1-D}{L \times f_{SW}}\right) = V_{OUT} \times \left(\frac{1 - \left(\frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}}\right) \tag{8}$$

Efficiency increases by decreasing switching losses and preserving high efficiency for varying duty cycles, while the ripple current amplitude remains low enough to deliver the full output current without reaching current limit. The AEE feature provides an efficiency enhancement for various duty cycles, especially for lower V_{OUT} values where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversion, which limits the control range in other topologies.

8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter operating in PWM mode is given as D = V_{OUT} / V_{IN}. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of typically 80 ns is reached, the TPS62903-Q1 scales down its switching frequency while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point, allowing the conversion of small input to output voltage differences (for example, getting longest operation time of battery-powered applications). In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$VIN_{(\min)} = VOUT + IOUT\left(R_{DS\ on)} + R_L\right) \tag{9}$$

where

- IOUT is the output current.
- $R_{DS(on)}$ is the on-state resistance of the high-side FET.
- R_L is the DC resistance of the inductor used.

ADVANCE INFORMATION

8.4.5 Starting into a Prebiased Load

The TPS62903-Q1 is capable of starting into a prebiased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS62903-Q1 does not start switching unless the voltage at the feedback pin drops to the target. See the note in Section 8.3.6 regarding the soft-start requirement during prebiased conditions.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS62903-Q1 devices are highly efficient, small, and highly flexible synchronous step-down DC/DC converters that are easy to use. A wide input voltage range of 3 V to 18 V supports a wide variety of inputs like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

9.2 Typical Application with Adjustable Output Voltage

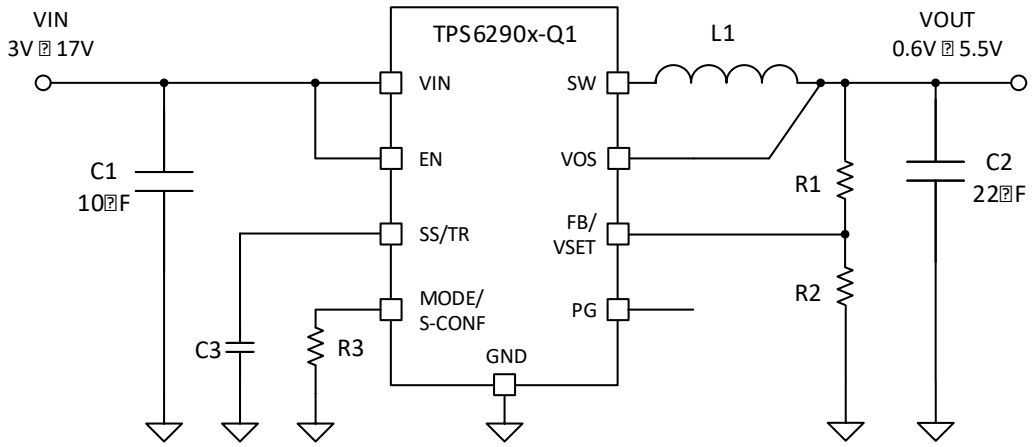


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

Table 9-1. List of Components

Reference	Description	Manufacturer
IC	18 V, 3-A step-down converter	TPS62903-Q1 series; Texas Instruments
L	1-µH inductor	XGL4020-102; Coilcraft
CIN	10 µF, 25 V, Ceramic, X8R	CGA6P1X8R1E106K250AE, TDK
COUT	22 µF, 16 V, Ceramic, X8L	CGA6P1X8L1C226M250AC, TDK
CSS	Depends on soft-start time; see Section 9.2.2.5.3.	AEC-Q200 qualified, 16 V, Ceramic, X8R
R1	Depending on V_{OUT}; see Section 9.2.2.2.	AEC-Q200 qualified, Standard 1% metal film
R2	Depending on V_{OUT}; see Section 9.2.2.2.	AEC-Q200 qualified, Standard 1% metal film
R3	Depending on device setting, see Section 8.3.1.	AEC-Q200 qualified, Standard 1% metal film

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62903-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

ADVANCE INFORMATION

3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Programming the Output Voltage

The output voltage of the TPS62903-Q1 is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from V_{OUT} to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 10. It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of R2 must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R1 = R2 \times \left(\frac{VOUT}{VFB} - 1 \right) \tag{10}$$

With typical VFB = 0.6 V:

Table 9-2. Setting the Output Voltage

Nominal Output Voltage	R1	R2	Exact Output Voltage
0.75 V	24.9 kΩ	100 kΩ	0.749 V
1.2 V	100 kΩ	100 kΩ	1.2 V
1.5 V	150 kΩ	100 kΩ	1.5 V
1.8 V	200 kΩ	100 kΩ	1.8 V
2.0 V	49.9 kΩ	21.5 kΩ	1.992 V
2.5 V	100 kΩ	31.6 kΩ	2.498 V
3.0 V	100 kΩ	24.9 kΩ	3.009 V
3.3 V	113 kΩ	24.9 kΩ	3.322 V
5.0V	182 kΩ	24.9 kΩ	4.985 V

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS62903-Q1 is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole responsible for the corner frequency of the converter (see Section 9.2.2.7). Table 9-3 can be used to simplify the output filter component selection. The values in Table 9-3 are nominal values. The effective capacitance was considered to vary by +20% and –50%.

Table 9-3. Recommended LC Output Filter Combinations

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF
1 µH		√	√(1)	√	√	√(3)
1.5 µH		√	√	√	√(3)	
2.2 µH		√	√(2)	√	√(3)	
3.3 µH	√	√	√	√		

(1) This LC combination is the standard value and recommended for most applications with 2.5-MHz switching frequency.
(2) This LC combination is the standard value and recommended for most applications with 1-MHz switching frequency.
(3) Output capacitance needs to have a ESR of ≥ 10 mΩ for stable operation, see Section 9.3.2.

ADVANCE INFORMATION

9.2.2.4 Inductor Selection

The TPS62903-Q1 is designed for a nominal 1-µH inductor. Larger values can be used to achieve a lower inductor current ripple, but they can have a negative impact on efficiency and transient response. Smaller values than 1 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. Therefore, they are not recommended at large voltages across the inductor as it is the case for high input voltages and low output voltages. Low-output current in forced PWM mode causes a larger negative inductor current peak, which can exceed the negative current limit. At low or no output current and small inductor values, the output voltage cannot be regulated any more. More detailed information on further LC combinations can be found in the *Optimizing the TPS62130/40/50/60 Output Filter* application report.

The inductor selection is affected by several factors like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 11 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{11}$$

$$\Delta I_{L(\max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \times f_{sw}} \right) \tag{12}$$

where

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the maximum peak-to-peak inductor ripple current.
- $L_{(min)}$ is the minimum effective inductor value.
- f_{sw} is the actual PWM switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum expected output voltage.

Calculating the maximum inductor current using the actual operating conditions gives the needed minimum saturation current of the inductor. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS62903-Q1 and are recommended for use:

Table 9-4. List of Inductors

Type	Inductance [µH]	Current [A](1)	Dimensions [L × B × H] mm	Manufacturer
XGL4020-102ME	1.0 µH, ±20%	8.8	4.0 × 4.0 × 2.1	Coilcraft
XGL4020-222ME	2.2 µH, ±20%	6.2	4.0 × 4.0 × 2.1	Coilcraft

(1) I_{SAT} at 30% drop

The inductor value also determines the load current at which power save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \tag{13}$$

9.2.2.5 Capacitor Selection

9.2.2.5.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS62903-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow

capacitance variation with temperature, it is recommended to use X8R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see the *Optimizing the TPS62130/40/50/60 Output Filter* application report).

In power save mode, the output voltage ripple depends on the following:

- Output capacitance
- ESR
- ESL
- Peak inductor current

. Using ceramic capacitors provides small ESR, ESL, and low ripple. The output capacitor needs to be as close as possible to the device.

For large output voltages, the DC bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

9.2.2.5.2 Input Capacitor

For most applications, 10 µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

Table 9-5. List of Capacitors

Type (1)	Nominal Capacitance [µF]	Voltage Rating [V]	Size	Manufacturer
CGA6P1X8R1E106K250AE	10	25	1210	TDK
CGA6P1X8L1C226M250AC	22	16	1210	TDK

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop

9.2.2.5.3 Soft-Start Capacitor

A capacitor connected between SS/TR pin and GND allows a user-programmable start-up slope of the output voltage.

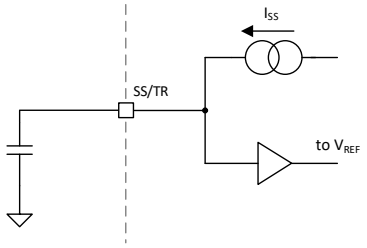


Figure 9-2. Soft-Start Operation Simplified Schematic

An internal constant current source is provided to charge the external capacitance. The capacitor required for a given soft-start ramp time is given by:

$$C_{SS} = T_{SS} \times \frac{I_{SS}}{V_{REF}} \tag{14}$$

where

- C_{SS} is the capacitance required at the SS/TR pin.
- T_{SS} is the desired soft-start ramp time.
- I_{SS} is the SS/TR source current, see the *Electrical Characteristics*.
- V_{REF} is the feedback regulation voltage divided by tracking gain (V_{FB} / 0.75); see the *Electrical Characteristics*.

ADVANCE INFORMATION

The fastest achievable typical ramp time is 150 µs, even if the external C_{ss} capacitance is lower than 680 pF or the pin is open.

9.2.2.6 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage with the typical gain and offset as specified in the *Electrical Characteristics*.

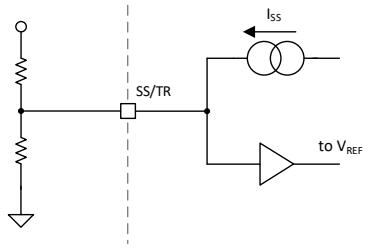


Figure 9-3. Tracking Operation Simplified Schematic

$$V_{FB} = 0.75 \times V_{SS/TR} \quad (15)$$

When the SS/TR pin voltage is above 0.8 V, the internal voltage is clamped and the device goes to normal regulation. This action works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing the SS/TR pin voltage in PFM mode, the device does not sink current from the output. The resulting decrease of the output voltage can therefore be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is 6 V. The SS/TR pin is internally connected with a resistor to GND when EN = 0.

If the input voltage drops below undervoltage lockout, the output voltage will go to zero, independent of the tracking voltage. Figure 9-4 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function. See Section 9.3.3 in the systems examples.

ADVANCE INFORMATION

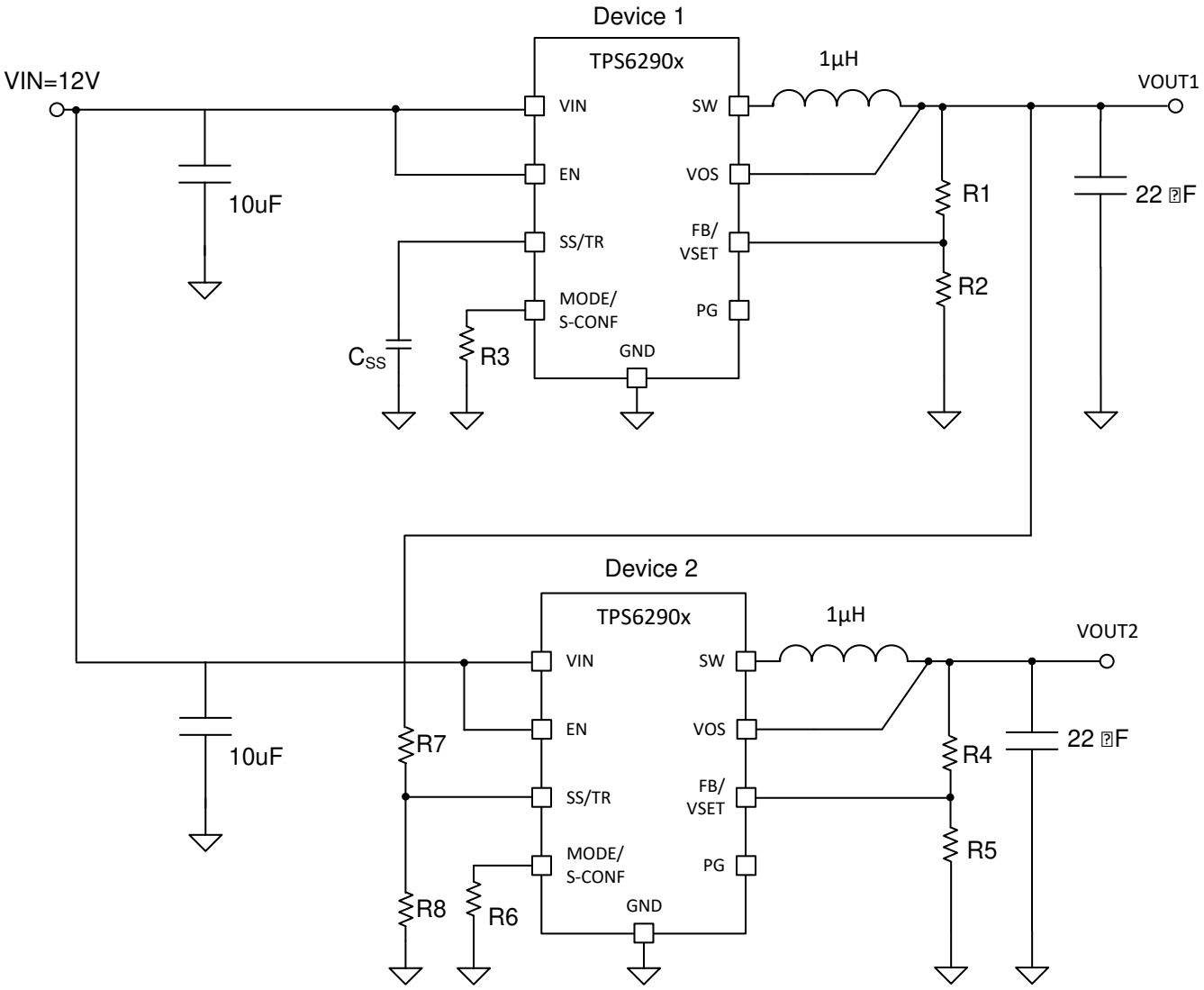


Figure 9-4. Schematic for Ratiometric and Simultaneous Start-Up

The resistive divider of R7 and R8 can be used to change the ramp rate of VOUT2 to be faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT of device 1 to the EN pin of device 2. PG requires a pullup resistor. Ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 14 gives the soft-start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in the *Sequencing and Tracking With the TPS621-Family and TPS821-Family* application report.

Note

If the voltage at the FB pin is below its typical value of 0.6 V, the output voltage accuracy can have a wider tolerance than specified. The current of 2.5 µA out of the SS/TR pin also has an influence on the tracking function, especially for high resistive external voltage dividers on the SS/TR pin.

9.2.2.7 Output Filter and Loop Stability

The devices of the TPS62903-Q1 family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 16:

ADVANCE INFORMATION

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (16)$$

Proven nominal values for inductance and ceramic capacitance are given in Section 9.2.2.3 and are recommended for use. Different values can work, but care has to be taken on the loop stability, which is affected. More information including a detailed LC stability matrix can be found in the *Optimizing the TPS62130/40/50/60 Output Filter* application report.

The TPS62903-Q1 devices include an internal 3-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 17 and Equation 18:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 3pF} \quad (17)$$

$$f_{pole} = \frac{1}{2\pi \times 3pF} \times \left(\frac{1}{R_1} \times \frac{1}{R_2} \right) \quad (18)$$

Though the TPS62903-Q1 devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power save mode, improved transient response, or both. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated DC-DC Converters* and *Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family* application reports.

9.3 System Examples

9.3.1 LED Power Supply

The TPS62903-Q1 can be used as a power supply for power LEDs. The FB pin can be easily set to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 19. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62903-Q1. Figure 9-5 shows an application circuit, tested with analog dimming.

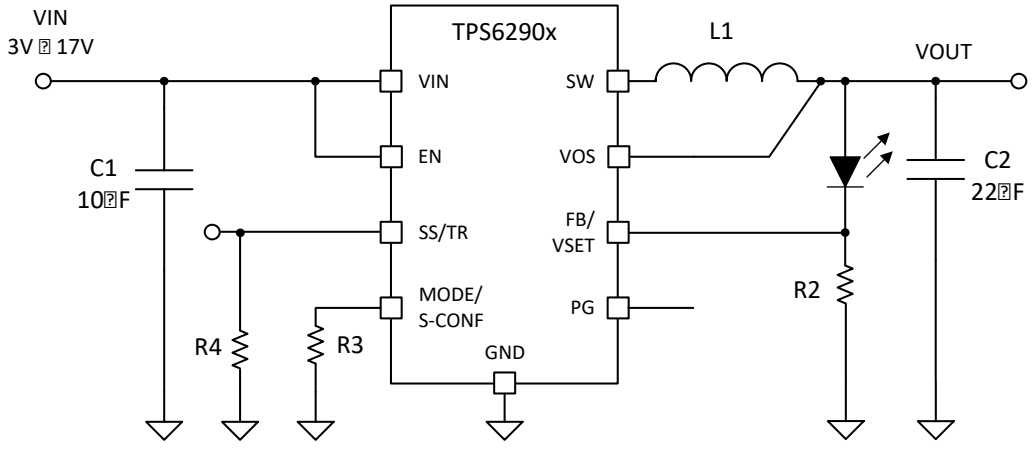


Figure 9-5. Single Power LED Supply

The resistor at SS/TR defines the FB voltage. It is set to 304 mV by $R_{SS/TR}$ = R4 = 162 kΩ using Equation 19. This cuts the losses on R4 to half from the nominal 0.6 V of feedback voltage while it still provides good accuracy.

$$V_{FB} = 0.75 \times 2.5uA \times R_{SS/TR} \quad (19)$$

The device now supplies a constant current set by resistor R2 from FB/VSET to GND. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the *Step-Down LED Driver With Dimming With the TPS621-Family and TPS821-Family* application report.

9.3.2 Powering Multiple Loads

In applications where the TPS62903-Q1 is used to power multiple load circuits, the total capacitance on the output can be very large. In order to properly regulate the output voltage, there needs to be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low-ESR ceramic capacitors, the output voltage ripple can get very low, so it is not recommended to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a PCB, these loads are typically distributed across the board. This adds enough trace resistance (R_{trace}) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is 10 mΩ. The total capacitance n × CIN in the use case below was 32 × 47 µF of ceramic X7R capacitors.

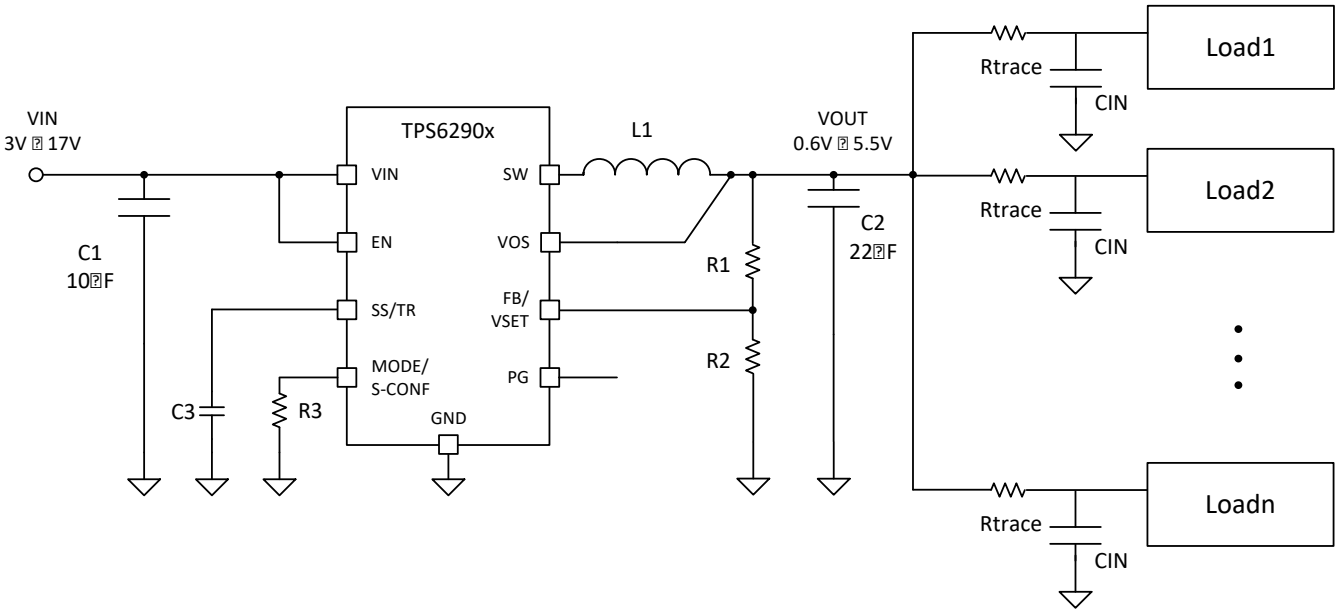


Figure 9-6. Multiple Loads

Note

Figure 9-6 shows an external feedback configuration, but the internal (VSET) configuration can also be used.

9.3.3 Voltage Tracking

Device 2 follows the voltage applied to the SS/TR pin. A ramp on SS/TR to 0.8 V ramps the output voltage according to the 0.6-V reference on V_{FB}.

Tracking the 3.8 V of device 1 requires a resistor divider on SS/TR of device 2 to output 0.8 V when the output voltage divider of device 1 is 0.6 V. The output current of 2.5 µA from the SS/TR pin causes an offset voltage on the resistor divider formed by R7 and R8. The equivalent resistance of R7 // R8 must therefore be kept below 15 kΩ.

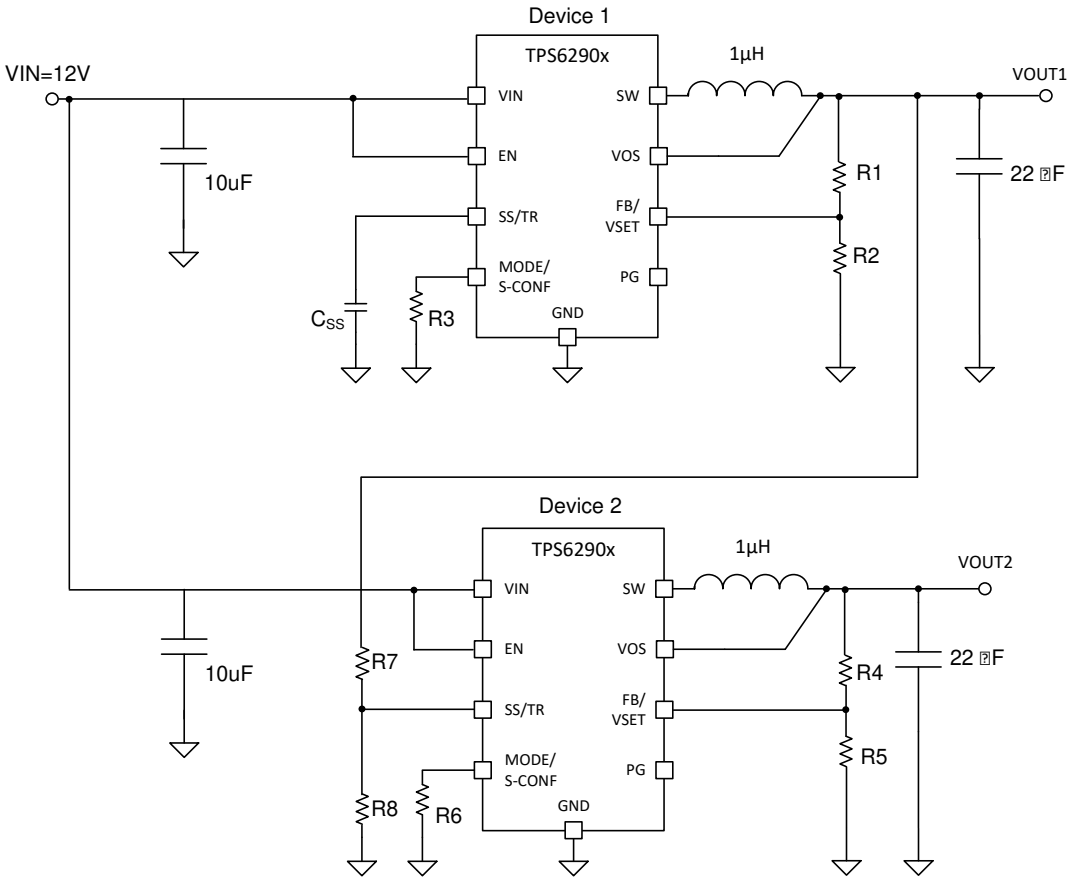


Figure 9-7. Tracking Example

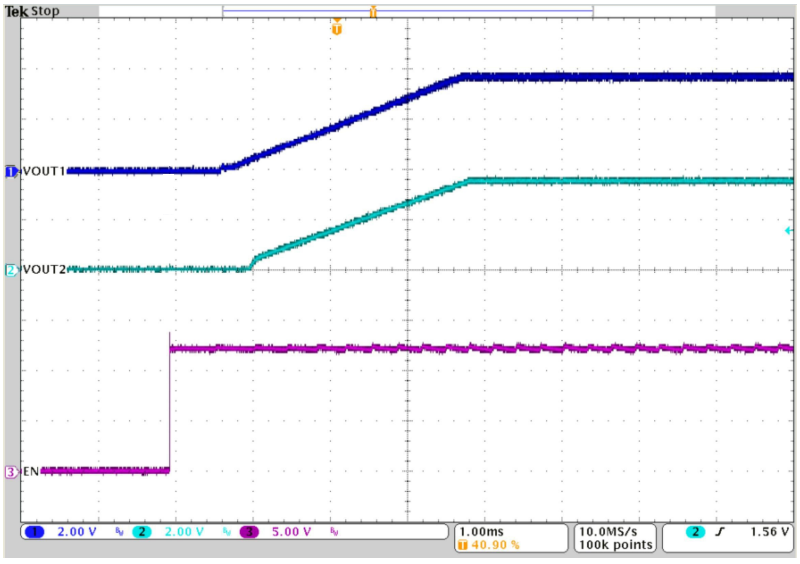


Figure 9-8. Tracking

9.3.4 Inverting Buck-Boost (IBB)

The need to generate negative voltage rails for electronic designs is a common challenge. The wide 3-V to 18-V input voltage range of the TPS62903-Q1 makes it ideal for an inverting buck-boost (IBB) circuit, where the output voltage is inverted or negative with respect to ground.

The circuit operation in the IBB topology differs from that in the traditional buck topology. Though the components are connected the same as with a traditional buck converter, thme output voltage terminals are reversed. See Figure 9-9.

The maximum input voltage that can be applied to an IBB converter is less than the maximum voltage that can be applied to the TPS62903-Q1 in a typical buck configuration. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, and not V_{IN} to ground. Thus, the input voltage range of the TPS62903-Q1 in an IBB configuration becomes 3 V to 18 V + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but only negative. Thus, the output voltage for a TPS62903-Q1 in an IBB configuration can be set between –0.4 V and –5.5 V.

The maximum output current for the TPS62903-Q1 in an IBB topology is normally lower than a traditional buck configuration due to the average inductor current being higher in an IBB configuration. Traditionally, lower input or (more negative) output voltages results in a lower maximum output current. However, using a larger inductor value or the higher 2.5-MHz frequency setting can be used to recover some or all of this lost maximum current capability.

When implementing an IBB design, it is important to understand that the IC ground is tied to the negative voltage rail, and in turn, the electrical characteristics of the TPS62903-Q1 device are referenced to this rail. During power up, as there is no charge in the output capacitor and the IC GND pin (and V_{OUT}) are effectively 0 V, thus parameters such as the V_{IN} UVLO and EN thresholds are the same as in a typical buck configuration. However, after the output voltage is in regulation, due to the negative voltage on the IC GND pin, the device traditionally continues to operate below what can appear to be the normal UVLO or EN falling thresholds relative to the system ground. Take care if the user is using the dynamic mode change feature on the MODE pin of the TPS62903-Q1 or driving the EN pin from an upstream microcontroller as the high and low thresholds are relative to the negative rail and not the system ground.

More information on using a DCS regulator in an IBB configuration can be found in the *Description Compensating the Current Mode Boost Control Loop*, *Using the TPS6215x in an Inverting Buck-Boost Topology*, and *Using the TPS629210 in an Inverting Buck-Boost Topology* application notes.

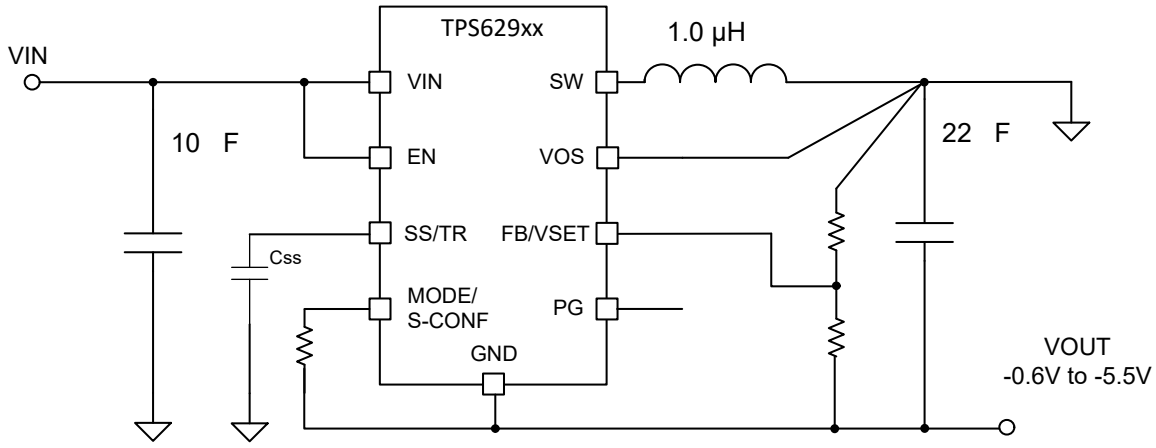


Figure 9-9. IBB Example with Adjustable Feedback

Note

Figure 9-9 shows an external feedback configuration, but the internal (VSET) configuration can also be used.

10 Power Supply Recommendations

The power supply to the TPS62903-Q1 needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS62903-Q1.

ADVANCE INFORMATION

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62903-Q1 demands careful attention to make sure the device works correctly and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See Figure 11-1 for the recommended layout of the TPS62903-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin of TPS62903-Q1. Also, connect the VOS pin in the shortest way to VOUT at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths, conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for traces with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R1 and R2, must be kept close to the IC and connected directly to those pins and the system ground plane. The same applies to the VSET resistor if VSET is used to scale the output voltage.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat through the PCB.

In case any of the digital inputs EN and MODE/S-CONF need to be tied to the input supply voltage at V_{IN}, the connection must be made directly at the input capacitor as indicated in the schematics.

The recommended layout is implemented on the EVM and shown in the *TPS6290x-Q1 Step-Down Converter Evaluation Module* user's guide.

11.2 Layout Example

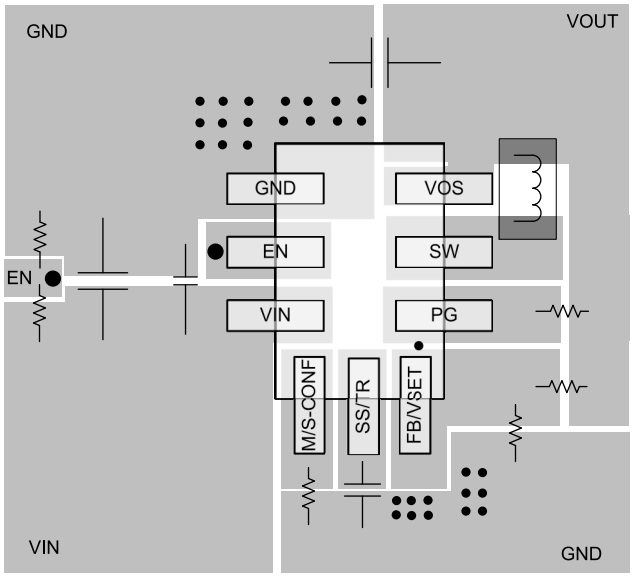


Figure 11-1. Layout

11.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design, for example, increasing copper thickness, thermal vias, number of layers
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics* application reports.

The TPS62903-Q1 is designed for a maximum operating junction temperature (T_J) of 165°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

The device is qualified for long term qualification with 165°C junction temperature. For more details about the derating and life time of the HotRod™ package, see the *Derating and Lifetime Calculations for FCOL Packages HotRod and FC-SOT* application note.

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62903-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Derating and Lifetime Calculations for FCOL Packages HotRod and FC-SOT* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report
- Texas Instruments, *TPS6290x-Q1 Step-Down Converter Evaluation Module* user's guide
- Texas Instruments, *Using the TPS629210 in an Inverting Buck-Boost Topology* application report
- Texas Instruments, *Description Compensating the Current Mode Boost Control Loop* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

SmartConfig™, HotRod™, and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

ADVANCE INFORMATION

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

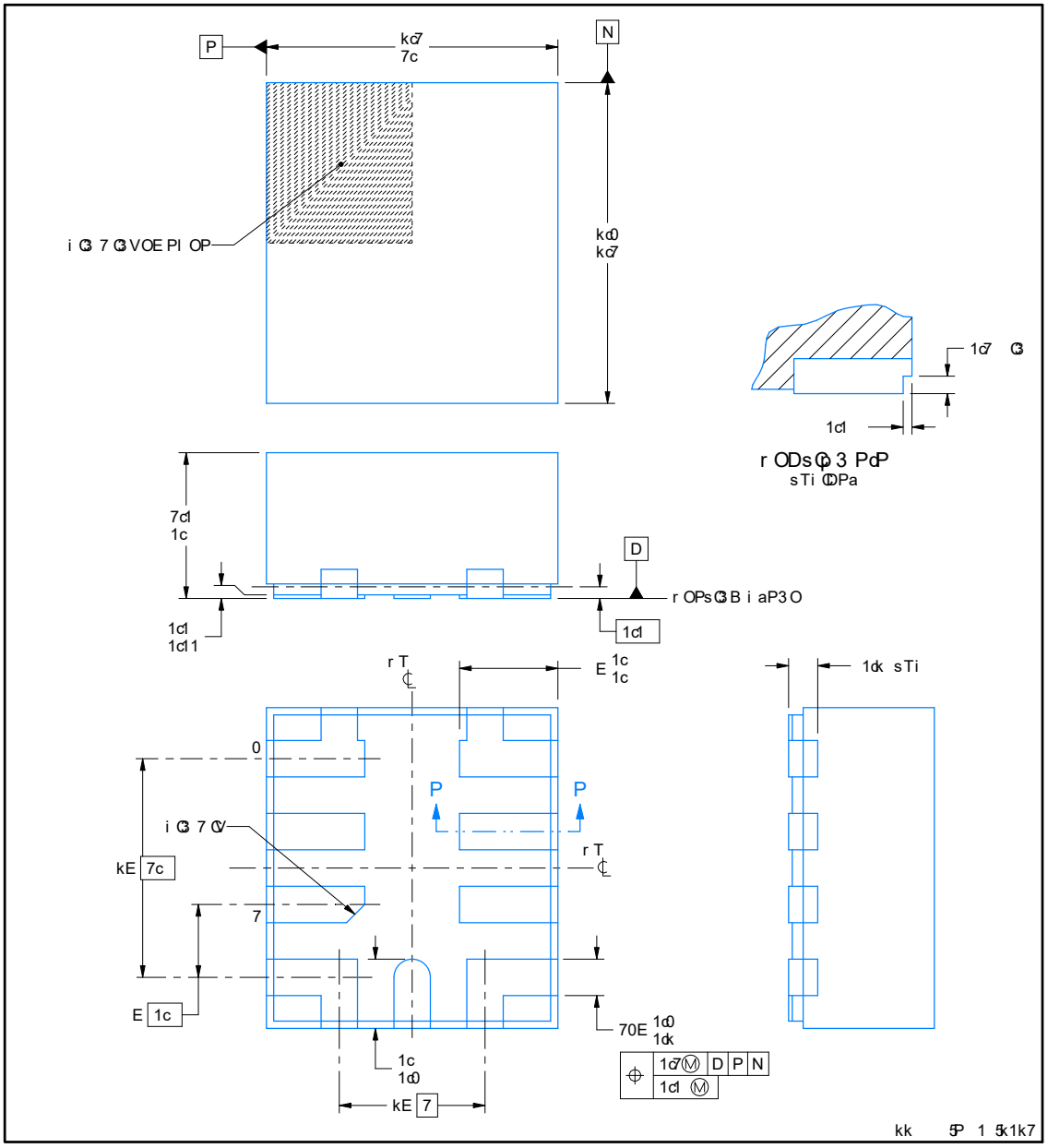
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

RYT0009A

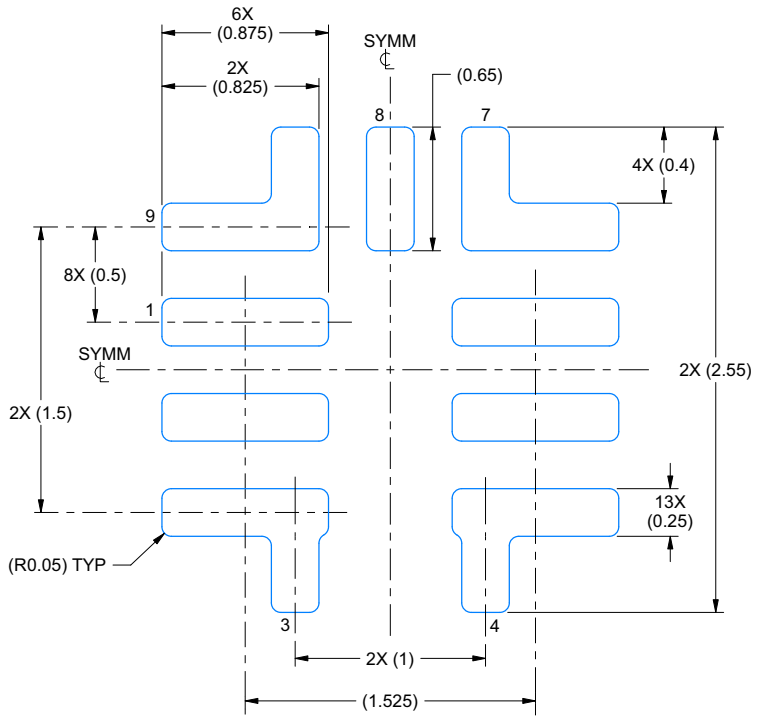
VQFN-HR - 1 mm max height



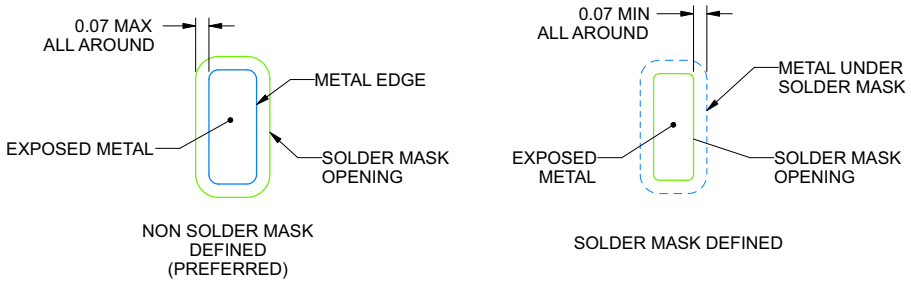
. - 2 - 54

2 4 60 2 77 7' 1,31

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4226765/A 04/2021

NOTES: (continued)

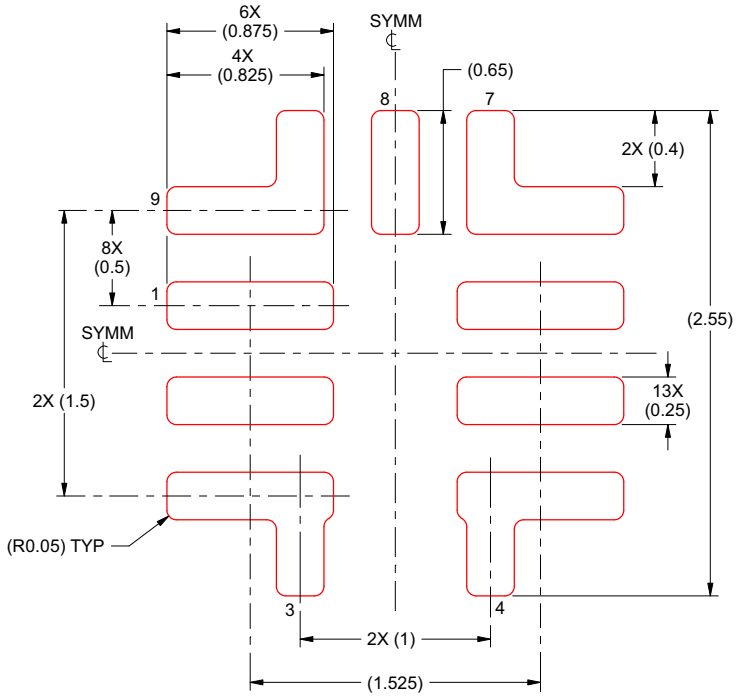
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RYT0009A — **VQFN-HR - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4226765/A 04/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PPS62903QRYTRQ1	ACTIVE	VQFN-HR	RYT	9	3000	TBD	Call TI	Call TI	-40 to 165		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62903-Q1 :

- Catalog : TPS62903

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPS92643-Q1 Automotive 3-A Synchronous Buck LED Driver

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C5
- Input voltage range: 5.5 V to 36 V
  - Operation down to 5.15 V after start-up
- Up to 3-A continuous with 4% accuracy
- Adaptive on-time current control
  - Low offset high-side current sense amplifier
  - Stable with any combination of ceramic, and aluminum capacitors
- Programmable switching frequency from 100 kHz to 2.2 MHz
- Advanced dimming operation
  - 1000:1 precision PWM dimming
  - 15:1 precision analog dimming
  - 1.4-kHz internal analog input to PWM duty cycle translation
- Cycle-by-cycle switch overcurrent protection
- Open-drain fault indicator output
  - LED short circuit, open circuit and cable harness fault indication
- Thermal shutdown protection

2 Applications

- Headlight
- Front fog light LED driver module

3 Description

The TPS92643-Q1 is a monolithic, synchronous Buck LED driver with a wide 5.5-V to 36-V operating input voltage range and 40-V tolerance that supports load dump for duration of 400 ms. The TPS92643-Q1 implements an adaptive on-time average current mode control based on inductor valley current detection. The adaptive on-time control provides near constant switching frequency that can be set between 100 kHz and 2.2 MHz. Inductor current sensing and closed-loop feedback enables better than ±4% accuracy over wide input, output and ambient temperature.

The high-performance LED driver can independently modulate LED current using both analog or PWM dimming techniques. Linear analog dimming range with over 15:1 range is obtained by setting the IADJ voltage. PWM dimming of LED current is achieved by directly modulating the UDIM input pin with desired duty cycle or setting the analog voltage at APWM to enable internal analog-to-PWM conversion. The internal PWM generator translates the external analog voltage by comparing it to an internal 1.4-kHz ramp signal.

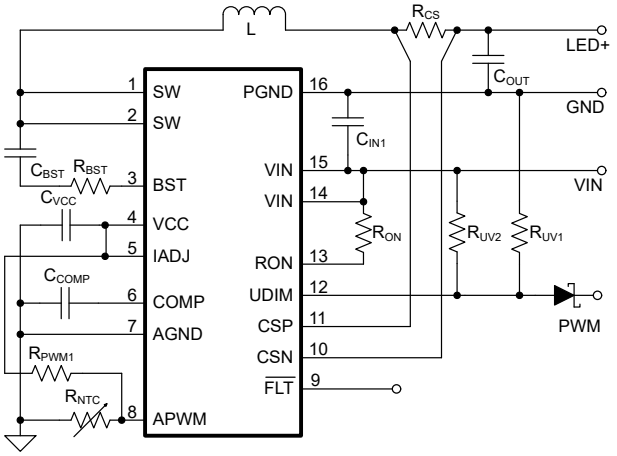
The TPS92643-Q1 incorporates advanced diagnostic and fault protection featuring: cycle-by-cycle switch current limit, bootstrap undervoltage, LED open, LED short and thermal shutdown.

The TPS92643-Q1 is available in a 6.6-mm × 5.1-mm thermally-enhanced 16-pin HTSSOP package with 0.65-mm lead pitch.

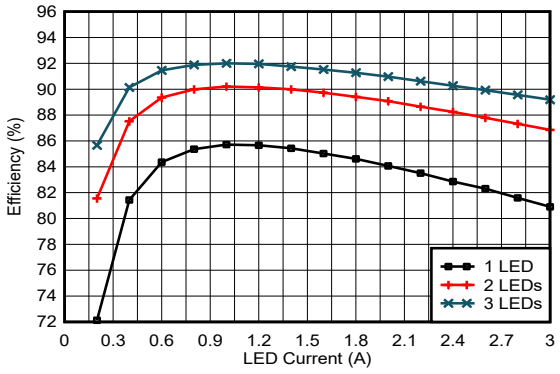
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS92643-Q1	HTSSOP (16)	6.60 mm × 5.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Buck LED Driver Application Schematic



Typical Efficiency

Table of Contents

4 Revision History

DATE	REVISION	NOTES
May 2022	*	Initial release.

5 Pin Configuration and Functions

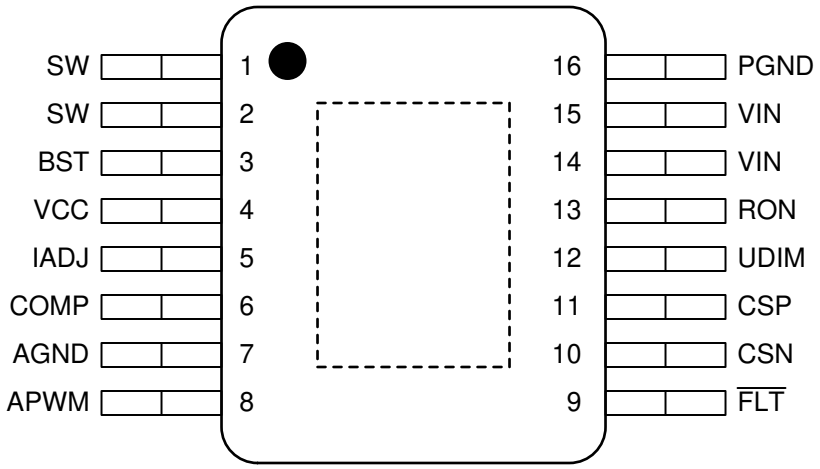


Figure 5-1. PWP Package, 16-Pin HTSSOP with PowerPAD, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
7	AGND	—	Analog ground. Return for the internal voltage reference and analog circuit. Connect to circuit ground, GND, to complete return path.
3	BST	I	Supply input for high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BST and SW pins. An internal diode is connected between VCC and BST pins.
6	COMP	O	Output of internal transconductance error amplifier. Connect an integral compensation network to ensure stability.
10	CSN	I	Negative input (–) of internal rail-to-rail transconductance error amplifier. Connect directly to the negative node of the LED current sense resistor, R_{CS}.
11	CSP	I	Positive input (+) of internal rail-to-rail transconductance error amplifier. Connect directly to the positive node of the LED current sense resistor, R_{CS}.
9	$\overline{FLT}$	O	Open-drain fault indicator. Connect to VCC with a resistor to create an active low fault signal output.
5	IADJ	I	Analog adjust input. Input below 100 mV disables the output. The analog input can be varied between 140 mV to 2.4 V to set current reference from 10 mV to 175 mV. Connect a 0.1-µF capacitor from pin to AGND.
16	PGND	—	Ground returns for low-side MOSFETs
8	APWM	I	External analog to PWM dimming command. The external analog dimming command between 1 V and 2.45 V is compared to the internal 1.5-kHz triangle waveform to set LED current duty cycle between 0% and 100%.
13	RON	I	On-time programming pin. Connect a resistor to VIN based on the desired pseudo-fixed switching frequency.
1,2	SW	I	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to the power inductor.
12	UDIM	I	Undervoltage lockout and external PWM dimming input. Connect to VIN through a resistor divider to implement input undervoltage protection. Diode couple external PWM signal to enable dimming. Do not float.
4	VCC	O	VCC bias supply pin. Locally decouple to AGND using a 2.2-µF to 4.7-µF ceramic capacitor located close to the controller.
14,15	VIN	I	Power input and connection to high-side MOSFET drain node. Connect to the power supply and bypass capacitors C_{IN}. The path from the VIN pin to the high frequency bypass capacitor and PGND must be as short as possible.
PowerPAD		—	The AGND and PGND pin must be connected to the exposed PowerPAD for proper operation. This PowerPAD must be connected to PCB ground plane using multiple vias for good thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	V_{IN}	–0.3	36	V
	V_{IN} (< 400 ms)		40	V
Bias supply voltage, VCC	V_{VCC}	–0.3	5.5	V
Boot voltage, BST	BST to SW	–0.3	5.5	V
	BST to GND	–0.3	41.5	V
Switch node voltage	V_{SW} to GND	–0.5	36	V
	V_{SW} to GND (< 400 ms)	–0.5	40	V
	V_{SW} to GND (< 10 ns)	–3.5	40	V
Inputs	CSP, CSN	–0.5	36	V
	RON	–0.1	36	V
	I_{RON}		500	µA
	$V_{(CSP-CSN)}$	–0.3	0.3	mV
	UDIM to GND	–0.3	V_{VIN}	V
	IADJ	–0.1	5.5	V
	COMP, APWM	–0.3	5.5	V
Outputs	$\overline{FLT}$	–0.3	20	V
Ground	PGND to AGND	–0.5	0.5	V
	PGND to AGND (< 10 ns)	–3.5	3.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (SW, APWM, $\overline{FLT}$ and PGND)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VIN}	Input Voltage	5.5		36	V
$V_{(CSP-CSN)}$	Sensed inductor current ripple voltage	8			mV
dV_{CSP}/dt	CSP slew-rate			10	V/µs
I_{LED}	LED Current (Continuous)			3	A
V_{APWM}	Analog PWM Input	–0.3		3	
V_{UDIM}	Digital PWM Input	–0.3		V_{VIN}	

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$\overline{FLT}$	Fault Output	–0.3		18	
f_{SW}	Switching Frequency	400		2200	kHz
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE PKG (HTSSOP) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

–40°C < T_J < 150°C, V_{IN} = 14V, V_{UDIM} = 5V, V_{IADJ} = 2.1V, C_{VCC} = 2.2µF, C_{BST} = 1nF, C_{COMP} = 1nF, R_{CS} = 100mΩ, R_{ON} = 401kΩ, V_{APWM} = 5V, f_{SW} = 200 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
V_{DO}	LDO dropout voltage	I_{VCC} = 20 mA, V_{VIN} = 5 V		315		mV
I_{SW}	Input switching current			10	17.6	mA
I_{OP}	Input operating current	Not switching, V_{IADJ} = V_{VCC}		2	4	mA
BIAS SUPPLY (VCC)						
$VCC_{(UVLO-RISE)}$	Rising threshold	VCC rising threshold, V_{VIN} = 8 V		4.40	4.58	V
$VCC_{(UVLO-FALL)}$	Falling threshold	VCC falling threshold, V_{VIN} = 8 V	3.9	4.2		V
$VCC_{(UVLO-HYS)}$		Hysteresis		200		mV
$VCC_{(REG)}$	Regulation voltage	No Load	4.75	5.00	5.25	V
$I_{CC(LIMIT)}$	Supply current Limit	V_{VCC} = 0 V	45	56	76	mA
HIGH-SIDE FET (SW, BOOT)						
$R_{DS(ON-HS)}$	High-side MOSFET on resistance	I_{LED} = 100 mA		65	130	mΩ
$V_{BST(UV)}$	Bootstrap gate drive UVLO	$V_{(BST-SW)}$ rising	2.95	3.2	3.47	V
$V_{BST(HYS)}$	Bootstrap gate drive UVLO hysteresis	Hysteresis	175	207	240	mV
$I_{Q(BST)}$	Bootstrap pin quiescent current	V_{SW} = 0V, V_{UDIM} = 0 V, V_{BOOT} = 5 V	197	265	325	µA
LOW-SIDE FET (SW)						
$R_{DS(ON-LS)}$	Low-side MOSFET on resistance	I_{LED} = 100 mA		67	130	mΩ
HIGH SIDE FET CURRENT LIMIT						
$I_{LIM(HS)}$	High-side current limit threshold		3.75	4.80	5.85	A
$t_{(HS-BLANK)}$	High-side current sense blanking period		35	60	80	ns
LOW SIDE FET CURRENT LIMIT						
$I_{SINK(LS)}$	Sinking current limit		2.0	3.2	4.3	A

6.5 Electrical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN} = 14V, V_{UDIM} = 5V, V_{IADJ} = 2.1V, C_{VCC} = 2.2µF, C_{BST} = 1nF, C_{COMP} = 1nF, R_{CS} = 100mΩ, R_{ON} = 401kΩ, V_{APWM} = 5V, f_{SW} = 200 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BLANK}	Blanking time			71		ns
ERROR AMPLIFIER (CSP, CSN, COMP)						
$V_{(CSP-CSN)}$	Current sense threshold	V_{IADJ} = V_{CC}, V_{CSP} = 3 V, I_{COMP} = 0 V	168	175	182	mV
		V_{IADJ} = 2.1 V, V_{CSP} = 3 V, I_{COMP} = 0 V		150		mV
g_M	Transconductance			450		µA/V
$I_{COMP(SRC)}$	COMP current source capacity	V_{IADJ} = 2.5 V, $V_{(CSP-CSN)}$ = 0 V		200		µA
$I_{COMP(SINK)}$	COMP current sink capacity	V_{IADJ} = 150 mV, $V_{(CSP-CSN)}$ = 300 mV		140		µA
$V_{COMP(RISE)}$	COMP startup threshold	Rising		2.45		V
$V_{COMP(HYS)}$	COMP startup comparator hysteresis			440		mV
$EA_{(BW)}$	Bandwidth	Unity gain bandwidth		3		MHz
$I_{COMP(LKG)}$	Comp leakage current	V_{UDIM} = 0 V		2.5		nA
$V_{COMP(RST)}$	COMP pin reset voltage	V_{VCC} dropping from 5 V to 0 V		100		mV
$R_{COMP(DCH)}$	COMP discharge FET resistance			230		Ω
$V_{COMP(OV)}$	COMP overvoltage protection threshold		2.9	3.2		V
$V_{COMP(OV-HYS)}$	COMP overvoltage protection hysteresis			60		mV
$V_{CSP(SHORT)}$	Output short circuit detection threshold	Falling		1.5		V
		Rising		1.6		V
ANALOG ADJUST INPUT (IADJ)						
$V_{IADJ(CLAMP)}$	IADJ internal clamp voltage			2.45		V
$V_{IADJ(DIS)}$	Disable threshold voltage	Rising		133		mV
$V_{IADJ(DIS)}$	Disable threshold voltage	Falling		100		mV
VALLEY CURRENT COMPARATOR						
$g_{M(LV)}$	Level shift amplifier transconductance			50		µA/V
t_{DEL}	$V_{(CSP-CSN)}$ falling to gate rising delay			65	80	ns
ON-TIME GENERATOR (RON)						
$t_{ON(MIN)}$	Minimum on-time		81	96	111	ns
t_{ON}	Programmed on-time	V_{VIN} = 14 V, V_{CSP} = 5 V, R_{ON} = 35 kΩ		150		ns
		V_{VIN} = 10 V, V_{CSP} = 8 V, R_{ON} = 35 kΩ		336		ns
		V_{VIN} = 14 V, V_{CSP} = 3 V, R_{ON} = 400 kΩ		0.95		µs
		V_{VIN} = 10 V, V_{CSP} = 8 V, R_{ON} = 400 kΩ		3.55		µs
MINIMUM OFF-TIME						
$t_{OFF(MIN)}$	Minimum off-time	$V_{(CSP-CSN)}$ = 0 V, VCOMP = 2.5 V	76	91	106	ns
PWM DIMMING and PROGRAMMABLE UVLO INPUT (UDIM)						
$I_{UDIM(DO)}$	UDIM source current (UVLO hysteresis)	V_{UDIM} > 2.45 V	6.5	10	13	µA
$V_{UDIM(DO,RISE)}$	Dropout detection rising threshold	V_{UDIM} rising		2.44	2.54	V
$V_{UDIM(DO,FALL)}$	Dropout detection falling threshold	V_{UDIM} falling	2.24	2.34		V
$V_{UDIM(EN,RISE)}$	Undervoltage lockout rising threshold	V_{UDIM} rising		1.22	1.27	V
$V_{UDIM(EN,FALL)}$	Undervoltage lockout falling threshold	V_{UDIM} falling	1.075	1.120		V
$t_{UDIM(RISE)}$	UDIM to SW pin rising delay			245		ns
$t_{UDIM(FALL)}$	UDIM pin SW pin falling delay			105		ns
ANALOG TO PWM GENERATOR (APWM)						
f_{RAMP}	Internal ramp generator frequency	V_{UDIM} = 5 V	1.0	1.5	1.9	kHz
$V_{RAMP(HIGH)}$	Internal ramp high threshold	V_{UDIM} = 5 V		2.45	2.60	V

6.5 Electrical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN} = 14V, V_{UDIM} = 5V, V_{IADJ} = 2.1V, C_{VCC} = 2.2µF, C_{BST} = 1nF, C_{COMP} = 1nF, R_{CS} = 100mΩ, R_{ON} = 401kΩ, V_{APWM} = 5V, f_{SW} = 200 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{RAMP(LOW)}$	Internal ramp low threshold	V_{UDIM} = 5 V	0.95	1.00		V
$V_{RAMP(CLAMP)}$	Internal ramp clamp	V_{UDIM} = 0 V		1		V
$t_{APWM(RISE)}$	APWM to SW pin rising delay			200		ns
$t_{APWM(FALL)}$	APWM to SW pin falling delay			80		ns
$V_{APWM(HYS)}$	Analog to PWM comparator hysteresis			5		mV
FAULT INDICATION (nFLT)						
$R_{(\overline{FLT})}$	Fault pin pull-down resistance	I_{FLT} = 20 mA		2.5	7	Ω
T_{OC}	Hiccup retry delay time			5.5		ms
$T_{UC(BLANK)}$	Undercurrent reporting blanking period			20		µs
$I_{\overline{FLT}(LKG)}$	Fault pin leakage current				100	nA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			15		°C

6.6 Typical Characteristics

–40°C < T_J < 150°C, V_{IN} = 14 V, V_{UDIM} = 5 V, V_{IADJ} = 2.1V , C_{VCC} = 2.2 µF, C_{BST} = 1 nF, C_{COMP} = 1 nF, R_{CS} = 100 mΩ, R_{ON} = 401 kΩ, V_{APWM} = 5 V, f_{SW} = 200 kHz

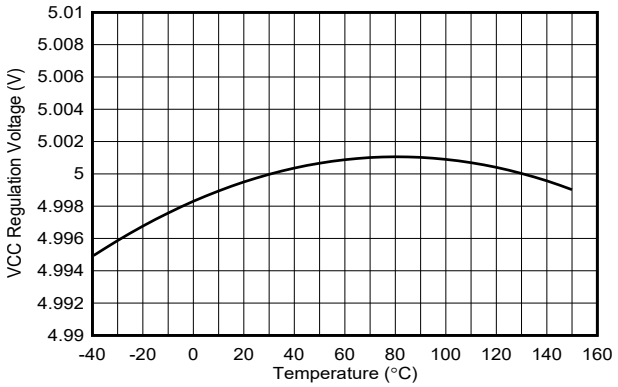


Figure 6-1. VCC Regulation Voltage vs Temperature

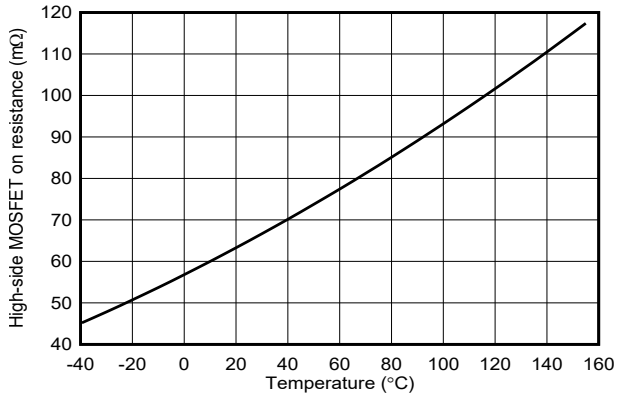


Figure 6-2. High-Side MOSFET On Resistance vs Temperature

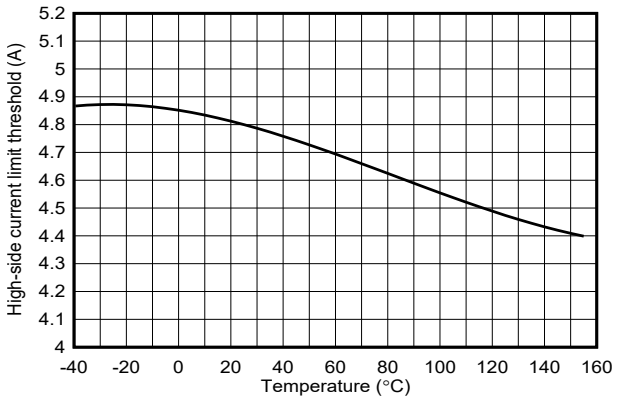


Figure 6-3. High-Side Current Limit Threshold vs Temperature

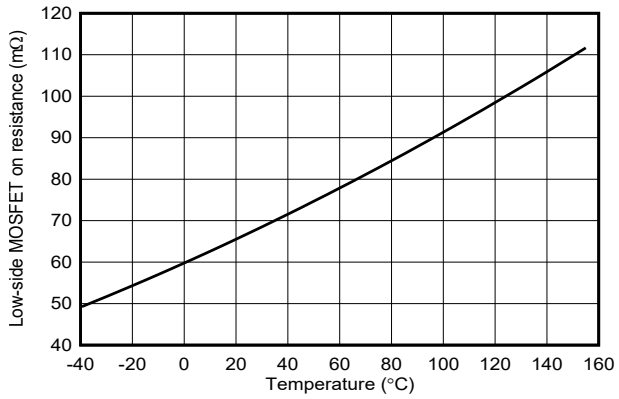


Figure 6-4. Low-Side MOSFET On Resistance vs Temperature

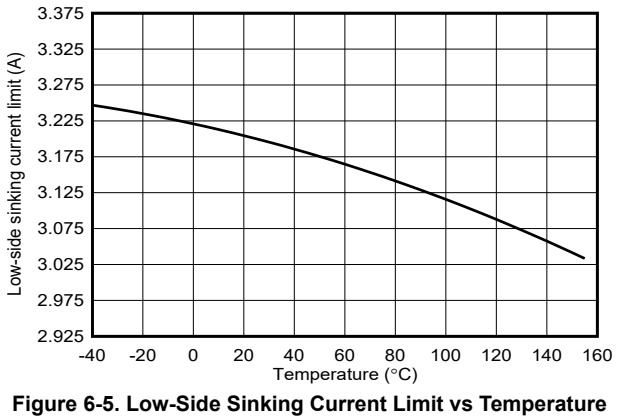


Figure 6-5. Low-Side Sinking Current Limit vs Temperature

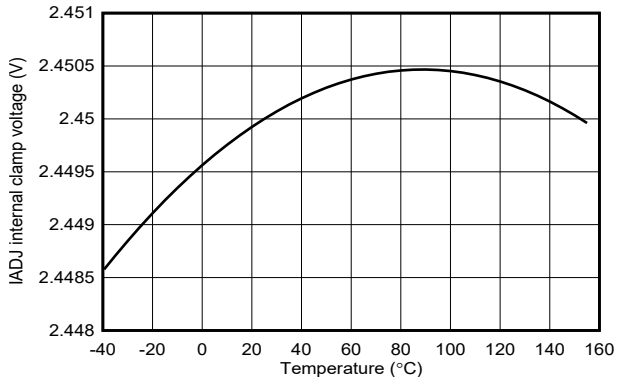


Figure 6-6. IADJ Internal Clamp Voltage vs Temperature

6.6 Typical Characteristics (continued)

–40°C < T_J < 150°C, V_{IN} = 14 V, V_{UDIM} = 5 V, V_{IADJ} = 2.1V , C_{VCC} = 2.2 µF, C_{BST} = 1 nF, C_{COMP} = 1 nF, R_{CS} = 100 mΩ, R_{ON} = 401 kΩ, V_{APWM} = 5 V, f_{SW} = 200 kHz

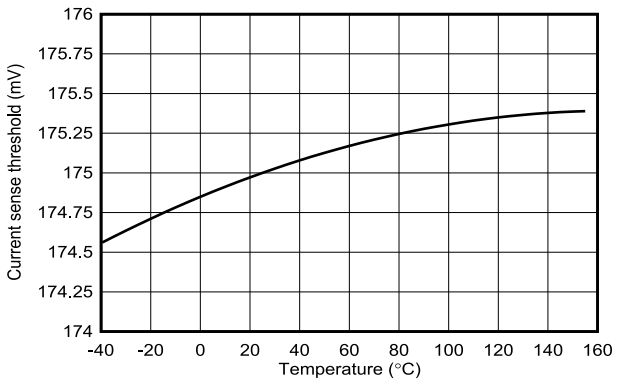


Figure 6-7. $V_{(CSP-CSN)}$ Sense Threshold vs Temperature

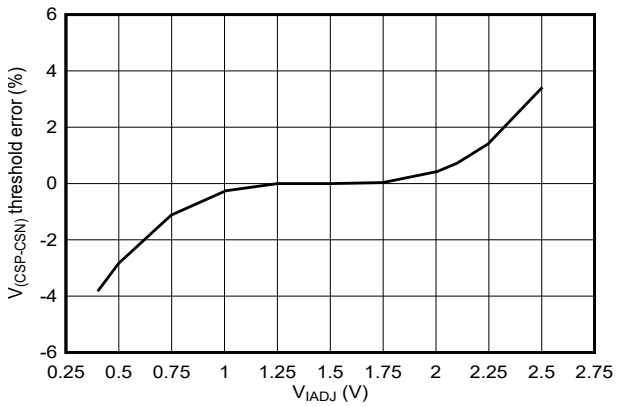


Figure 6-8. $V_{(CSP-CSN)}$ Sense Error vs IADJ Setpoint

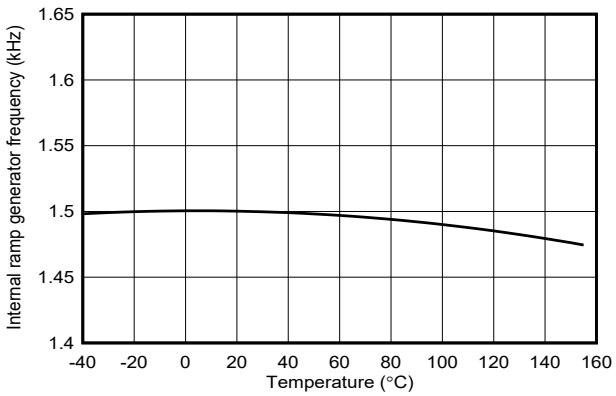


Figure 6-9. Internal Ramp Generator Frequency vs Temperature

7 Detailed Description

7.1 Overview

The TPS92643-Q1 is a wide input, synchronous buck LED driver. The device can deliver up to 3 A of continuous current and power a single string of one to 10 series-connected LEDs. The device implements an adaptive on-time current regulation control technique to achieve fast transient response. This architecture uses a comparator and a one-shot on-timer that varies inversely with input and output voltage to maintain a near-constant frequency. The integrated low offset rail-to-rail error amplifier enables closed-loop regulation of LED current and ensures better than 4% accuracy over a wide input, output, and temperature range. The LED current reference is set by the IADJ pin and is programmed by a voltage divider to achieve over a 15:1 linear analog dimming range. The high impedance IADJ input simplifies LED current binning and thermal protection.

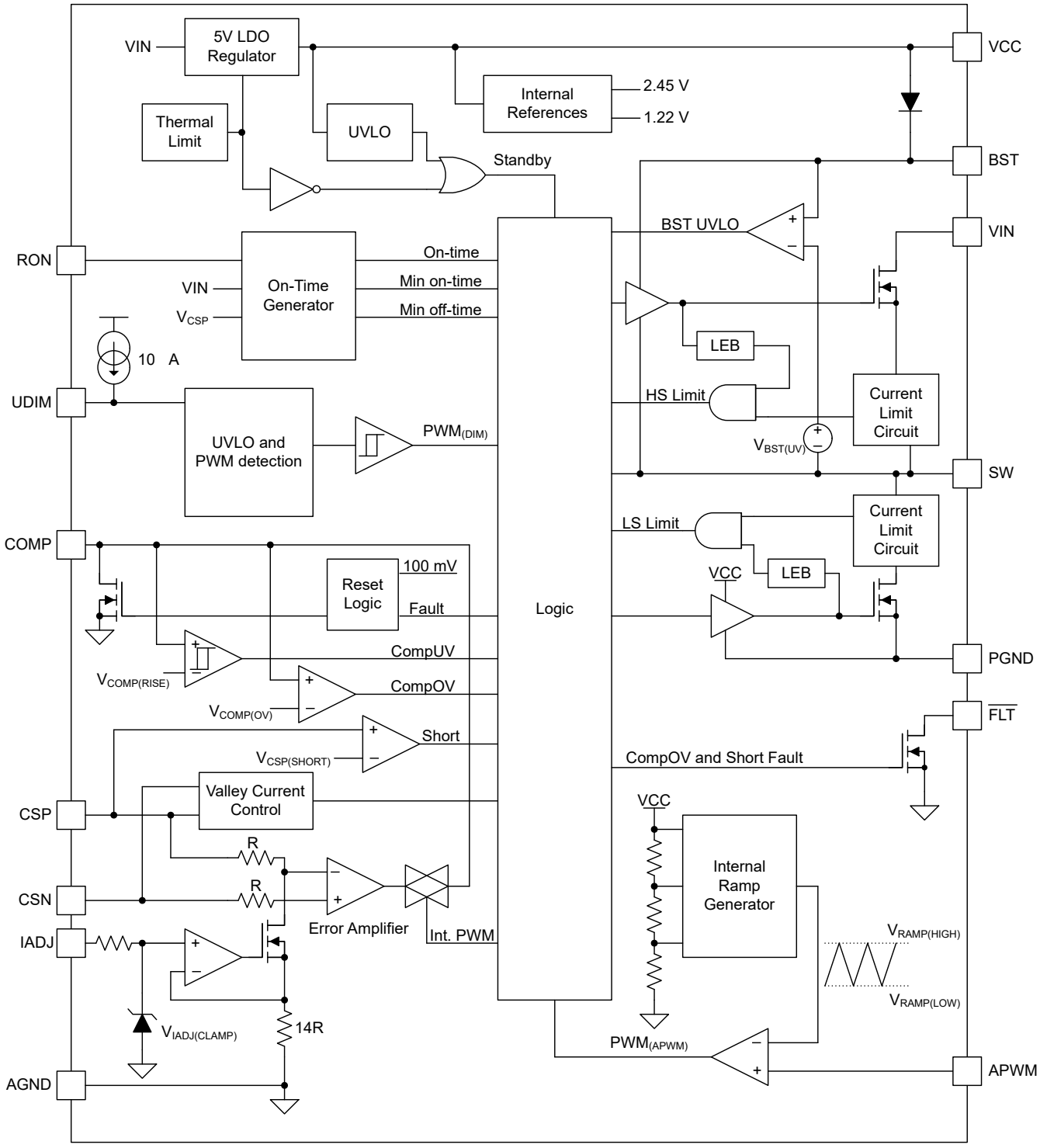
The TPS92643-Q1 device incorporates an internal ramp generator to control LED current through pulse width modulation (PWM) dimming. The PWM duty cycle can be varied from 0% to 100% by modulating the analog voltage on APWM from $V_{RAMP(LOW)}$ to $V_{RAMP(HIGH)}$. The PWM dimming frequency is internally set to typical value of 1.5 kHz. In addition, an external PWM input can control current by driving UDIM input. When both UDIM and APWM inputs are present, the internal PWM control command is derived by ANDing the two pulse width modulated signals. The APWM input can be tied to VCC to enable only external PWM control. Alternatively, APWM input can be biased using NTC to scale average LED current and enable temperature foldback protection of LEDs. This device optimizes the inductor current response and is capable of achieving over a 1000:1 PWM dimming ratio.

The device incorporates enhanced programmable fault features, including the following:

- Cycle-by-cycle switch overcurrent limit
- Input undervoltage protection
- Boot undervoltage protection
- Comp overvoltage warning
- Thermal warning
- LED short-circuit indication

In addition, thermal shutdown (TSD) protection is implemented to limit the junction temperature at 175°C (typical).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Regulator

The TPS92643-Q1 incorporates a 36-V input voltage rated linear regulator to generate the 5-V (typical) V_{CC} bias supply and other internal reference voltages. The device monitors the V_{CC} output to implement UVLO protection. Operation is enabled when V_{CC} exceeds the $V_{CC(UVLO)}$ rising threshold and is disabled when V_{CC} drops below $V_{CC(UVLO)}$ falling threshold. The comparator provides 200 mV of hysteresis to avoid chatter during transitions. The V_{CC} UVLO thresholds are internally fixed and cannot be adjusted. An internal current limit circuit is implemented to protect the device during VCC pin short-circuit conditions. The V_{CC} supply powers the internal circuitry, the low-side gate driver and the bootstrap supply for high-side gate driver. Place a bypass capacitor in the range of 4.7 µF to 10 µF close to the device, across the VCC pin to AGND. The capacitor from VCC must be five times larger than the bootstrap capacitor, C_{BST} to support proper operation. The regulator operates in dropout when input voltage, V_{IN} falls below 5 V, forcing V_{CC} to be lower than V_{IN} by V_{DO} for a 20-mA supply current. The V_{CC} is a regulated output of the internal regulator and is not recommended to be driven from an external power supply.

7.3.2 Buck Converter Switching Operation

The following operating description of the TPS92643-Q1 refers to the *Functional Block Diagram* and the waveforms in Figure 7-1. The main control loop of the TPS92643-Q1 is based on an adaptive on-time pulse width modulation (PWM) technique that combines a constant on-time control with an inductor valley current sense circuit for pseudo-fixed frequency operation. This proprietary control technique enables closed-loop regulation of LED current and fast dynamic response necessary to meet the requirements for dimming animation and fault protection.

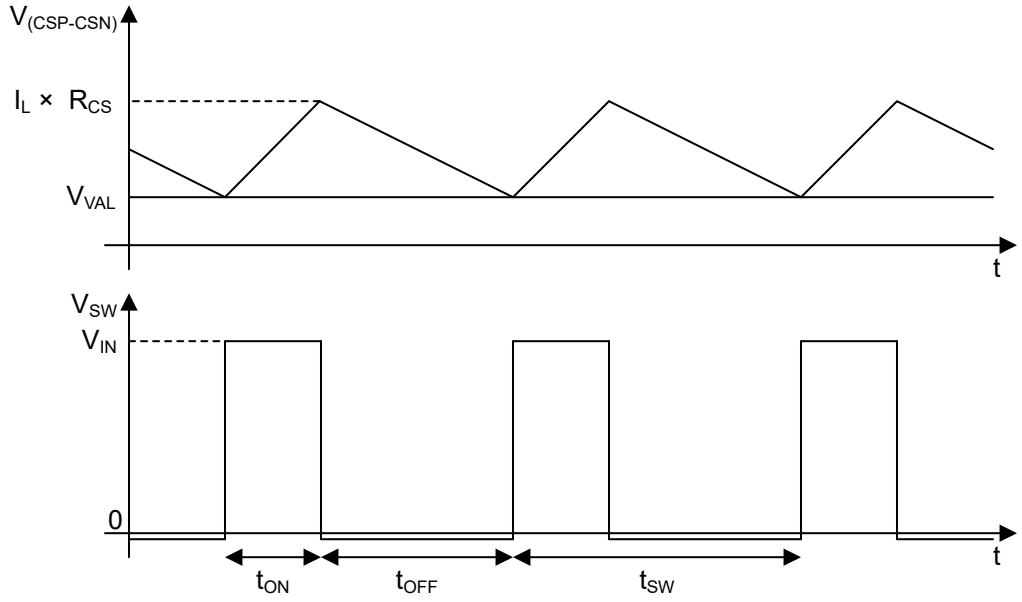


Figure 7-1. Adaptive On-Time Buck Converter Waveforms

In steady state, the high-side MOSFET is turned on at the beginning of each cycle. The on-time duration of this MOSFET is controlled by an internal one-shot timer and the high-side MOSFET is turned off after the timer expires. The one-shot timer duration is set by the output voltage measured at the CSP pin, V_{CSP}, and the input voltage measured at the VIN pin, V_{IN}, to maintain a pseudo-fixed frequency. During the on-time interval, the inductor current increases with a slope proportional to the voltage applied across its terminals ($V_{IN} – V_{CSP}$).

The low-side MOSFET is turned on after a fixed dead time and the inductor current then decreases with the constant slope proportional to the output voltage, V_{CSP}. Inductor current measured by the external sense resistor is compared to the valley threshold, V_{VAL}, by an internal high-speed comparator. This MOSFET is turned off and the one-shot timer is initiated when the sensed inductor current falls below the valley threshold voltage. The high-side MOSFET is turned on again after a fixed dead time.

The internal rail-to-rail error amplifier sets the valley threshold voltage and regulates the average inductor current based on a reference value set by V_{IADJ} pin. A simple integral loop compensation circuit consisting of a capacitor connected from the COMP pin to GND provides a stable and high-bandwidth response. As the inductor current is directly sensed by an external resistor, the device operation is not sensitive to the ESR of the output capacitors and is compatible with common multilayered ceramic capacitors (MLCC).

7.3.3 Bootstrap Supply

The TPS92643-Q1 contains both high-side and low-side N-channel MOSFETs. The high-side gate driver works in conjunction with an internal bootstrap diode and an external bootstrap capacitor, C_{BST}. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and C_{BST} is charged from the VCC supply through the internal diode and external R_{BST} resistor. TI recommends a 0.1-µF to 2.2-µF capacitor and 2.2-Ω to 10-Ω resistor connected in series between the BST and SW pins.

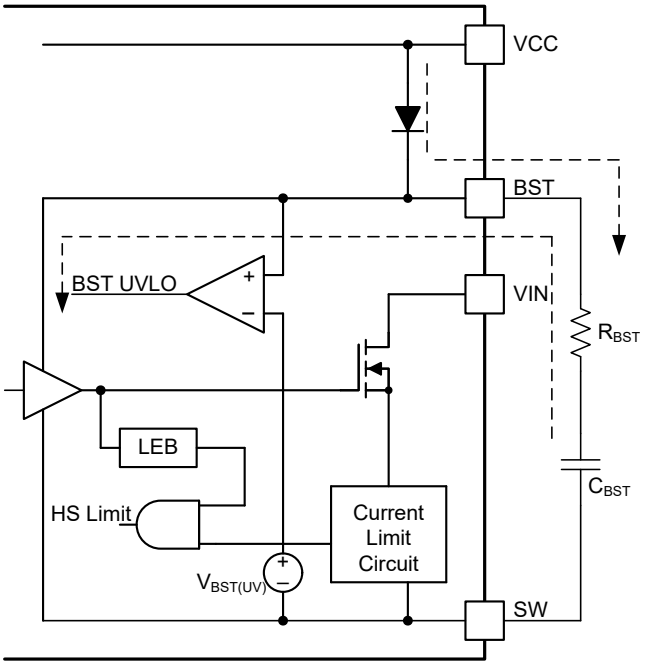


Figure 7-2. Bootstrap Network

A larger capacitor is required to prevent a bootstrap undervoltage fault when operating at low PWM dimming frequencies. Noise due to stored charge is reduced by the R_{BST}. In addition, the R_{BST} resistor allows optimization of EMI with respect to efficiency. A larger RBST resistor results in lower SW node rise time and allows energy in SW node harmonics to roll off near 100-MHz frequency. Switching with slower slew rate also decreases the efficiency.

7.3.4 Switching Frequency and Adaptive On-Time Control

The TPS92643-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The one-shot timer is programmed by the R_{ON} resistor. The on-time is calculated internally using Equation 1 and is inversely proportional to the measured input voltage, V_{IN}, and directly proportional to the measured CSP voltage, V_{CSP}.

$$t_{ON} = 10 \times 10^{-12} \times R_{ON} \times \left(\frac{V_{CSP}}{V_{IN}}\right) \quad (1)$$

Given the duty ratio of the buck converter is V_{CSP}/V_{IN}, the switching period, T_{SW}, remains nearly constant over different operating points. Use Equation 2 to calculate the switching period.

$$T_{SW} = t_{ON} \times \left(\frac{V_{CSP}}{V_{IN}}\right) = 10 \times 10^{-12} \times R_{ON} \quad (2)$$

The switching frequency is calculated internally using Equation 3.

$$f_{SW} = \frac{1}{10 \times 10^{-12} \times R_{ON}} \quad (3)$$

The minimum or maximum duty cycle is limited to finite minimum on-time, $T_{ON(MIN)}$ and minimum off-time, $T_{OFF(MIN)}$, respectively. As on-time is constant, the frequency is also a dependent on the efficiency of the device, η_{REG}, excluding inductor and sense resistor losses.

$$f_{SW} = \frac{1}{10 \times 10^{-12} \times R_{ON} \times \eta_{REG}} \quad (4)$$

TI recommends a switching frequency setting between 100 kHz and 2.2 MHz.

7.3.5 Minimum On-Time, Off-Time, and Inductor Ripple

Buck converter operation is impacted by minimum on-time, minimum off-time, and minimum peak-to-peak inductor ripple limitations. The converter reaches the minimum on-time of 96 ns (typical) when operating with high input voltage and low-output voltage. In this control scheme, the off-time continues to increase and the switching frequency reduces to regulate the inductor current and LED current to the desired value.

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{T_{ON(MIN)} \times V_{IN(MAX)}}; t_{ON} = t_{ON(MIN)} \quad (5)$$

The converter reaches the minimum off-time of 91 ns (typical) when operating in dropout (low input voltage and high output voltage). As the on-time and off-time are fixed, the duty cycle is constant and the buck converter operates in open-loop mode. The inductor current and LED current are not in regulation.

The behavior and response of valley comparator is dependent on sensed peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$, and is a function of current sense resistor, R_{CS}, and peak-to-peak inductor current ripple, $\Delta i_{L(PK-PK)}$. To ensure periodic switching, the sensed peak-to-peak ripple must exceed the minimum value. At high (near 100%) or low (near 0%) duty cycles, the inductor current ripple may not be sufficient to ensure periodic switching. Under such operating conditions, the converter transitions from periodic switching to a burst sequence, forcing multiple on-time and off-time cycles at a rate higher than the programmed frequency. Although the converter may not operate in a periodic manner, the closed-loop control continues regulating the average LED current with a larger ripple value corresponding to higher peak-to-peak inductor ripple. TI recommends choosing an inductor, output capacitor, and switching frequency to ensure minimum sensed peak-to-peak ripple voltage under nominal operating condition is greater than 8 mV. The *Application and Implementation* section summarizes the detailed design procedure.

7.3.6 LED Current Regulation and Error Amplifier

The reference voltage, V_{IADJ}, set by the V_{IADJ} and is internally scaled by a gain factor of 1/14 through a resistor network. An internal rail-to-rail error amplifier generates an error signal proportional to the difference between the scaled reference voltage (V_{IADJ} / 14) and the inductor current measured by the differential voltage drop between CSP and CSN, $V_{(CSP-CSN)}$. This error drives the COMP pin voltage, V_{COMP}, and directly controls the valley threshold of the inductor current. Zero average DC error and closed-loop regulation is achieved by implementing an integral compensation network consisting of a capacitor connected from the output of the error amplifier to GND. As a good starting point, TI recommends a capacitor value between 1 nF and 10 nF between the COMP pin and GND. The choice of compensation network must ensure a minimum of 60° of phase margin and 10 dB of gain margin.

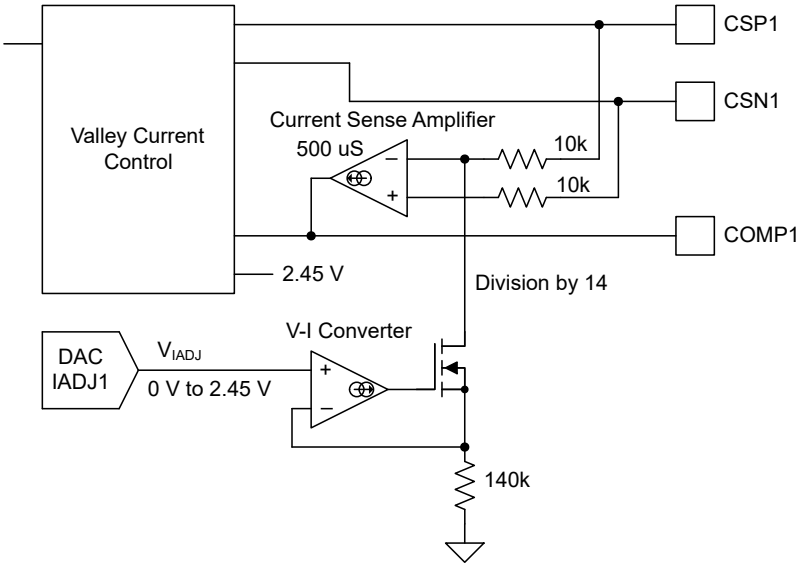


Figure 7-3. Closed-Loop LED Current Regulation

LED current is dependent on the current sense resistor, R_{CS}. Use Equation 15 to calculate the LED current.

LED current accuracy is a function of the tolerance of the external sense resistor, R_{CS}, and the variation in the sense threshold, $V_{(CSP-CSN)}$, caused by internal mismatch and temperature dependency of the analog components. The TPS92643-Q1 incorporates low offset rail-to-rail amplifiers, and is capable of achieving LED current accuracy of ±4% over common-mode range and a junction temperature range of –40°C to 150°C.

7.3.7 Start-Up Sequence

The start-up circuit allows the COMP pin voltage to gradually increase, thus reducing the LED current overshoot and current surges. The switching operation is initiated after the COMP pin voltage exceeds 2.45 V. A 440-mV hysteresis window allows the device to operate when COMP voltage is within the expected operating range of 2.2 V to 2.7 V. Switching is disabled on detection of low COMP voltage to avoid excessive negative inductor current.

The duration of soft start, t_{ss}, depends on the size of the compensation capacitor and the error amplifier source current, $I_{COMP(SRC)}$.

$$t_{SS} = \frac{2.45 \times C_{COMP}}{I_{COMP(SRC)}} \quad (6)$$

The source current, $I_{COMP(SRC)}$ is a function of the transconductance, g_M, of the error amplifier and error generated between the reference and the current sensed voltage.

$$I_{COMP(SRC)} = g_M \times \left(\frac{V_{IADJ}}{14} - V_{(CSP-CSN)}\right) \quad (7)$$

With no current flowing through the LEDs, the soft start duration depends on the choice of compensation capacitor, C_{COMP}, and the reference voltage, V_{IADJ}.

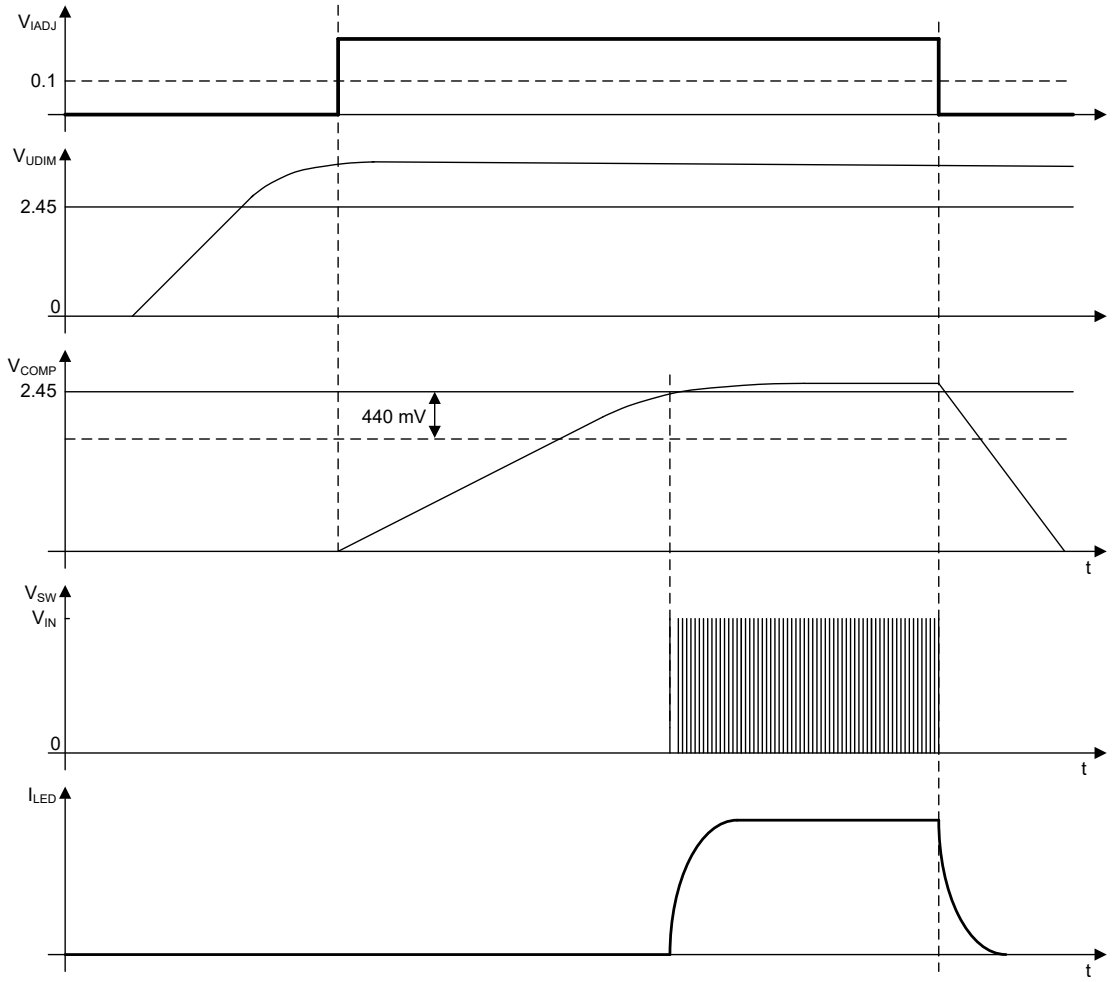


Figure 7-4. Soft-Start Sequence

The open drain fault indicator, $\overline{FLT}$, is set low when the COMP voltage deviates from the nominal range and exceeds $V_{COMP(OV)}$ threshold. This setting indicates a fault condition where the converter is operating in open-loop and the LED current is out of regulation. The device can be disabled by setting IADJ input below 100 mV or controlling the UDIM input.

7.3.8 Analog Dimming and Forced Continuous Conduction Mode

Analog dimming is accomplished by the voltage on IADJ pin, V_{IADJ}. The TPS92643-Q1 improves the linear range of analog dimming by supporting forced continuous conduction mode of operation. With synchronous MOSFETs, the inductor current is allowed to go negative for part of the switching cycle, thus enabling linear dimming with over 15:1 dimming range. TI recommends a 10-nF capacitor from IADJ pin to AGND pin to improve noise sensitivity.

7.3.9 External PWM Dimming and Input Undervoltage Lockout (UVLO)

The UDIM pin is a multifunction input that features an accurate input voltage detection based on band-gap thresholds with programmable hysteresis as shown in Figure 7-5. This pin functions as the external PWM dimming input for the LEDs and monitors VIN to detect dropout and undervoltage conditions. When the rising pin voltage exceeds the 2.45-V threshold, 10 µA (typical) of current is driven out of the UDIM pin into the resistor divider providing programmable hysteresis. TI recommends a bypass capacitor value of 1 nF between the UDIM pin and GND to improve noise immunity.

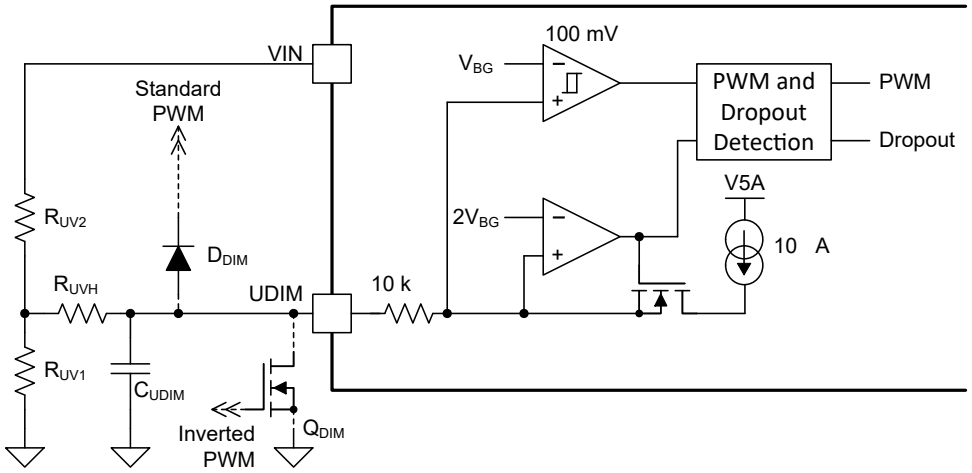


Figure 7-5. External PWM Dimming

The brightness of LEDs can be varied by modulating the duty cycle of the signal directly connected to the UDIM input. In addition, either an n-channel MOSFET or a Schottky diode can be used to couple an external PWM signal when using UDIM input in conjunction with UVLO functionality. With an n-channel MOSFET, the brightness is proportional to the negative duty cycle of the external PWM signal. With a Schottky diode, the brightness is proportional to the positive duty cycle of the external PWM signal.

Dropout and input undervoltage protection is achieved by connecting the resistor divider network from VIN to UDIM pin and UDIM pin to GND. Dropout protection is activated when UDIM pin voltage drops below $V_{UDIM(DO,\ FALL)}$ threshold but is held above $V_{UDIM(EN)}$ threshold. In dropout protection mode, the device disables the error amplifier and disconnects the COMP pin to maintain charge on the compensation network. The device continues switching, ensuring fast response with minimum led current overshoot as the converter recovers from dropout condition. The minimum input voltage, below which drop protection is activated is programmed using Equation 8.

$$V_{IN(DO,\,FALL)} = V_{IN(DO,\,RISE)} - I_{UDIM(DO)} \times \left(R_{UV2} + \frac{\left(R_{UVH} + 10 \times 10^{3}\right) \times \left(R_{UV1} + R_{UV2}\right)}{R_{UV1}} \right) \quad (8)$$

Equation 9 shows the input voltage rising threshold. When VIN exceeds the rising threshold, the error amplifier is enabled, the COMP pin is connected to the compensation network. The control loop now regulates the LED current regulation.

$$V_{IN(DO,\,RISE)} = V_{UDIM(DO,\,RISE)} \times \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \quad (9)$$

Additional hysteresis to internal 100 mV is programmed by connecting an external resistor, R_{UVH} in series with UDIM pin. This connection allows the standard resistor divider to have smaller values, minimizing PWM delays.

Input undervoltage protection is triggered when UDIM pin voltage drops below $V_{UDIM(EN)}$ thresholds. The device responds to very low VIN voltage or to the external PWM input signal by disabling the error amplifier, disconnecting the COMP pin and tri-stating the switch node. With switch disabled, inductor current and the LED current drops to zero and the charge on the compensation network is maintained. On rising edge of PWM or when VIN exceeds the internal hysteresis of 100 mV, the converter resumes switching operation. The inductor current quickly ramps to the previous steady-state value.

Equation 10 defines the VIN UVLO rising threshold.

$$V_{IN(UVLO,RISE)} = V_{UDIM(EN,RISE)} \times \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \quad (10)$$

Use Equation 11 to determine the VIN UVLO falling threshold.

$$V_{IN(UVLO,FALL)} = V_{UDIM(EN,FALL)} \times \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \quad (11)$$

7.3.10 Analog Pulse Width Modulator Circuit

The TPS92643-Q1 features analog circuitry to generate an internal PWM dimming signal. The frequency of the internal PWM signal is fixed to 1.5 kHz and the duty cycle is proportional to the applied voltage to APWM pin, V_{APWM}, according to Equation 12:

$$D_{PWM(INT)} = \frac{V_{APWM} - 1}{1.45} \times 100 \quad (12)$$

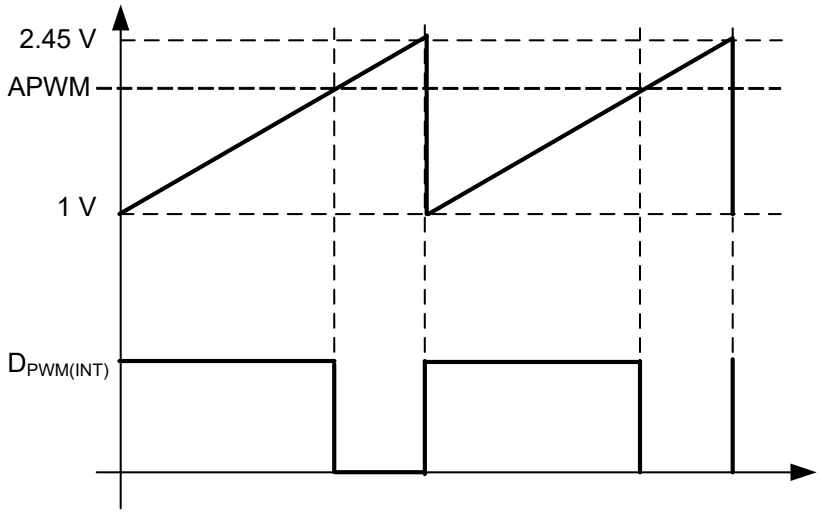


Figure 7-6. APWM Waveform

The internal PWM signal is ANDed with the external PWM signal applied to UDIM pin. Hence, if this pin is unused it should be tied to V_{CC} pin. The TPS92643-Q1 stops switching if V_{APWM} falls below 1.0 V. Pulse width modulated thermal fold-back can be implemented by connecting a NTC resistor, in conjunction with a voltage divider network, to APWM pin. TI recommends a bypass capacitor of 10 nF between APWM pin and GND to improve noise immunity.

7.3.11 Output Short and Open-Circuit Faults

The TPS92643-Q1 monitors the CSN voltage to detect output short circuit faults. A short failure is indicated by open drain $\overline{FLT}$ output when the CSN voltage drops below 1.5 V (typical). The device continues to regulate current and operate without interruption in case of short circuit. A short-circuit fault does not impact the device behavior. The device continues to operate and regulate current without interruption.

An LED open-circuit fault ultimately causes the output voltage to increase and settle close to the input voltage. When this event occurs, the TPS92643-Q1 switching operation is then controlled by the fixed on-time and minimum off-time resulting in a duty cycle close to 100%. The COMP pin voltage exceeds the COMP overvoltage threshold, $V_{COMP(OV)}$, and the fault in indicated by $\overline{FLT}$ output. However, during open circuit, the dynamic behavior of the device and buck converter is influenced by the input voltage, V_{IN}, and the output capacitor, C_{OUT}, value. The device response to open circuit can be categorized into the following two distinct cases.

Case 1: For a Buck converter design with a small output capacitor, the switching operation in open load condition exits the tank resonance forcing the output voltage to oscillate. The frequency and amplitude of the oscillation are based on the resonant frequency and Q-factor of the second order tank network.

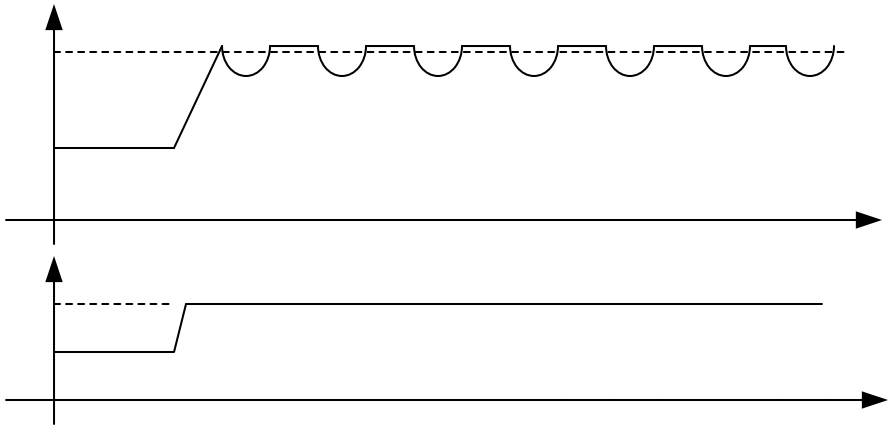


Figure 7-7. Open-Circuit Condition with Output Voltage Oscillation

Case 2: For a buck converter design with large output capacitor the inductor Q-factor and resonant frequency are much lower than the switching frequency. In this case, output voltage rises to input voltage and the converter continues to switch with minimum off-time.

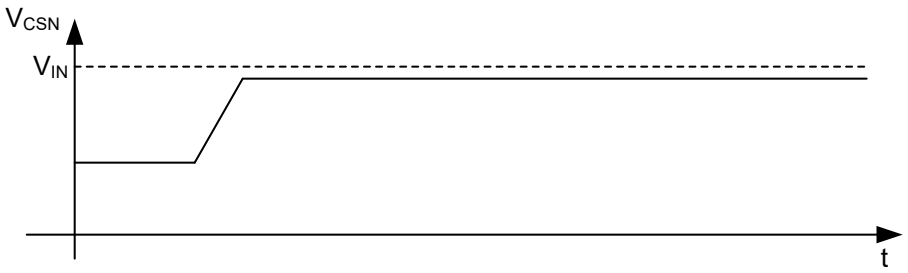


Figure 7-8. Open-Circuit Condition with Minimum Off-Time Operation

The voltage transient imposed on CSP and CSN inputs during short circuit and open circuit is dependent on the output capacitance and is influenced by the cable harness impedance. The inductance associated with a long cable harness resonates with the charge stored on the output capacitor and forces CSP and CSN voltage to ring above VIN and below ground. The magnitude of the voltage overshoot above VIN and below ground are dependent on the parasitic cable harness inductance and resistance.

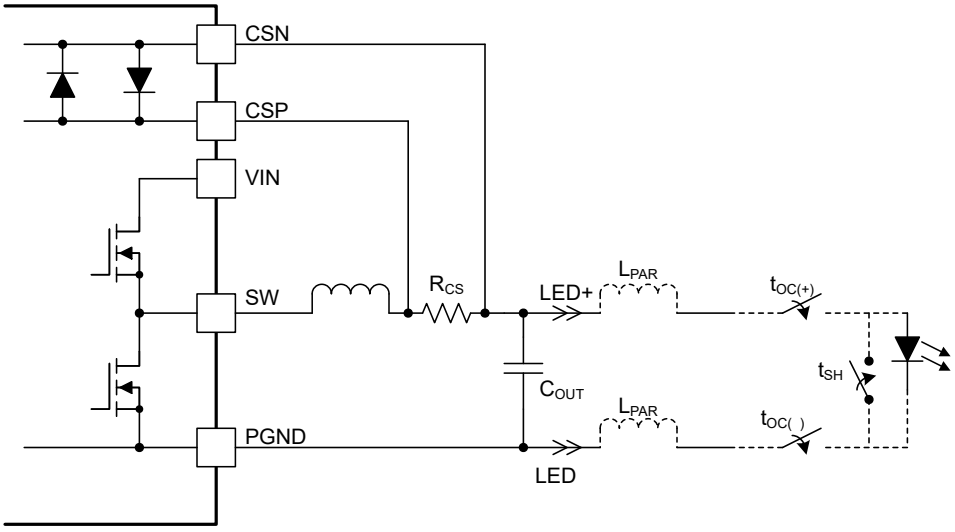


Figure 7-9. Cable Harness Parasitic Inductance

When using a long cable harness, TI recommends diodes to clamp the voltage across CSP and CSN input, as shown in Figure 7-10. TI recommends a low forward voltage Schottky diode or a fast recovery silicon diode with reverse blocking voltage rating greater than the maximum output voltage. The diode is required to be placed close to the output capacitor.

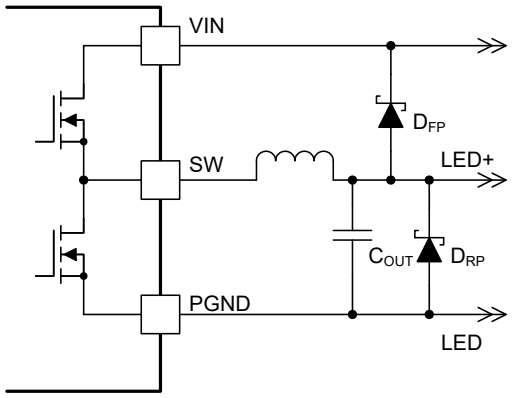


Figure 7-10. Transient Protection Using an External Diode

7.3.12 Overcurrent Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

The device turns off the high-side MOSFET and discharges the COMP capacitor when the drain current exceeds 4.8-A typical. The low-side switch is turned on to discharge the inductor current and output capacitor.

When the low-side switch is turned on, the switch current is also sensed and monitored. The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor when the drain current (from drain to PGND) exceeds 3.2-A typical.

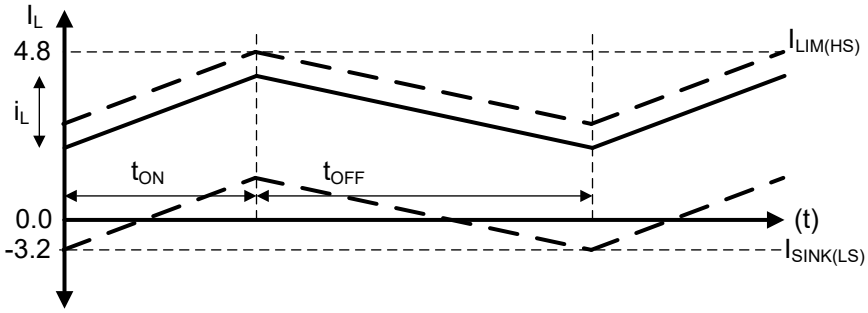


Figure 7-11. Overcurrent Protection Thresholds

The device employs hiccup mode overcurrent protection. In hiccup mode, the device shuts itself down and attempts to start after T_{OC}. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions.

7.3.13 Thermal Shutdown

Thermal shutdown prevents the device from extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 175°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 160°C. When the junction temperature falls below 160°C (typical), the device attempts to start up.

7.3.14 Fault Indicator and Diagnostics Summary

Table 7-1 summarizes the device behavior under fault conditions.

Table 7-1. Fault Description

FAULT	DETECTION	DESCRIPTION
Thermal protection	T_J > 175°C	The thermal protection is activated in the event the maximum MOSFET temperature exceeds the typical value of 175°C. This feature is designed to prevent overheating and damage to the internal switching MOSFETs.
VCC undervoltage lockout	$V_{CC(RISE)}$ < 4.4 V $V_{CC(FALL)}$ < 4.2 V	The device enters the Undervoltage Lockout (UVLO). The switching operation is disabled, the COMP capacitor is discharged.
VIN dropout protection	V_{UDIM} < 2.34 V	The device disables error amplifier and disconnects the compensation network for the corresponding channel. Error amplifier is enabled and compensation network is internally connected when the input voltage rises above the dropout rising threshold, $V_{IN(DO,RISE)}$.
VIN undervoltage lockout	V_{UDIM} < 1.12 V	The device disables switching operation for the corresponding channel. Switching is enabled when the input voltage rises above the turn-on threshold, $V_{IN(UVLO,RISE)}$.
BST undervoltage lockout	$V_{BST(RISE)}$ < 3.2 V $V_{BST(FALL)}$ < 2.93 V	The device turns off the high-side MOSFET and turns on the low-side MOSFET for the corresponding channel. Normal switching operation is resumed after the bootstrap voltage exceeds 3.2 V.
COMP overvoltage	V_{COMP} > 3.2 V	The $\overline{FLT}$ flag is set low to indicate that the COMP voltage exceeded the normal operating range. This condition indicates output open-circuit fault.
Short output	V_{CSN} < 1.5 V	The $\overline{FLT}$ flag is set low to indicate an output short-circuit condition based on sensed CSN voltage.
High-side switch current limit	I_{HS} > 4.8 A	The device turns off the high-side MOSFET, turns on low-side MOSFET and discharges the COMP capacitor. The device attempts to restart after a delay of 5.5 ms.
Low-side switch current limit	I_{LS} > 3.2 A	The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor. The device attempts to restart after a delay of 5.5 ms.

Output open and short circuit faults force the $\overline{FLT}$ pin low when biased through an external resistor and connected to a 5-V supply. The $\overline{FLT}$ output can be used in conjunction with a microcontroller or system basis chip (SBC) as an interrupt and aid in fault diagnostics.

7.4 Device Functional Modes

This device has no additional functional modes.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Figure 8-1 shows a schematic of a typical application for the TPS92643-Q1.

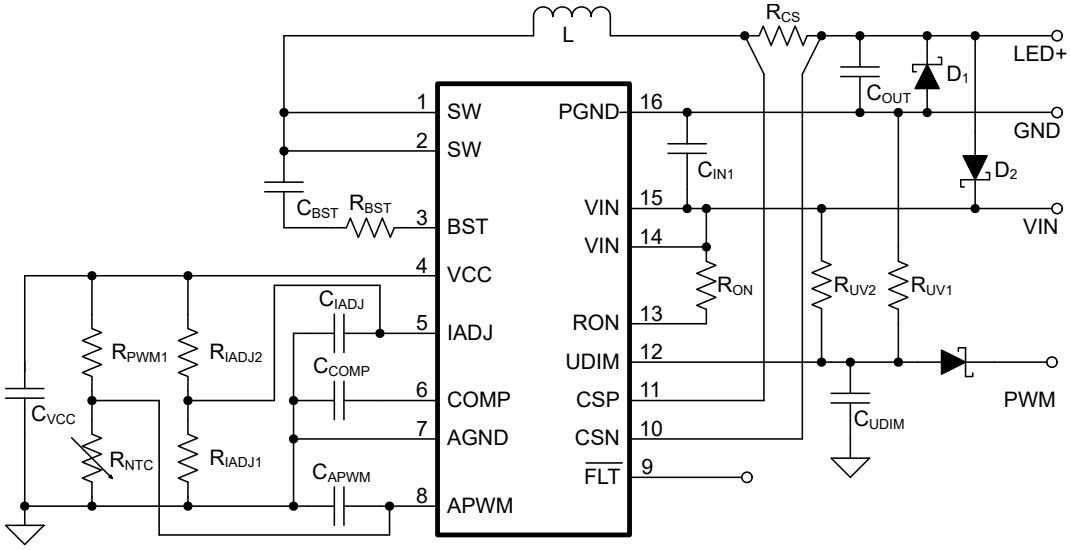


Figure 8-1. Typical Application Schematic

The TPS92643-Q1 controller is suitable for implementation of step-down LED driver topology. Use the following design procedure to select component values for the TPS92643-Q1 device. This section presents a simplified discussion of the design process for the Buck converter.

8.1.1 Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is defined using Equation 13:

$$D = \frac{V_{CSN}}{V_{IN}} \tag{13}$$

The buck converter maximum operating duty cycle, D_{MAX}, at minimum input voltage, $V_{IN,MIN}$ and maximum LED voltage, $V_{CSN,MAX}$.

$$D_{MAX} = \frac{V_{CSN,\,MAX}}{V_{IN,\,MIN}} \tag{14}$$

There is no limitation for small duty cycles, because at low duty cycles, the switching frequency is reduced as needed to always ensure current regulation. The maximum duty cycle attainable is limited by the minimum off-time duration and is a function of switching frequency.

8.1.2 Switching Frequency Selection

Nominal switching frequency is set by programming the R_{ON} resistor. The switching varies slightly over operating range and temperature based on converter efficiency. Table 8-1 shows common switching frequencies and corresponding R_{ON} resistor values.

Table 8-1. Center Switching Frequency Setting

R_{ON} (kΩ)	SWITCHING FREQUENCY (kHz)
267	400
243	435
221	480
50	2000
44.2	2200

8.1.3 LED Current Programming

The LED current is set by the external current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The LED current can be programmed by varying V_{IADJ} between 140 mV to 2.3 V. The LED current can be calculated using Equation 15:

$$I_{LED} = \frac{V_{IADJ}}{14 \times R_{CS}} \tag{15}$$

The LED current can be programmed by varying V_{IADJ} between 140 mV and 2.3 V. TI recommends a 10-nF capacitor from IADJ pin to AGND pin to filter high frequency switching noise.

8.1.4 Inductor Selection

The inductor is sized to meet the ripple specification at maximum operating duty cycle. TI recommends a minimum sensed peak-to-peak voltage ripple ($\Delta V_{(CSP\text{-}CSN)}$) of 8 mV to ensure periodic switching operation under.

$$\Delta V_{(CSP\,-\,CSN)} = \Delta i_L \times R_{CS} \tag{16}$$

Use Equation 17 to calculate the inductor value.

$$L = \frac{V_{IN,\,MIN} - V_{CSN,\,MAX}}{\Delta i_L \times f_{SW}} \times \frac{V_{CSN,\,MAX}}{V_{IN,\,MIN}} \tag{17}$$

The maximum inductor current ripple occurs at 50% duty cycle. Use Equation 18 to calculate the maximum peak-to-peak inductor current ripple, $\Delta i_{L(MAX)}$.

$$\Delta i_{L(MAX)} = \frac{V_{IN(TYP)}}{4 \times L \times f_{SW}} \quad (18)$$

Use Equation 19 and Equation 20 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$i_{L(RMS)} = \sqrt{\left(I_{LED(MAX)}^2 + \frac{\Delta I_{L(MAX)}^2}{12} \right)} \quad (19)$$

$$i_{L(PK)} = I_{LED(MAX)} + \frac{\Delta i_{L(MAX)}}{2} \quad (20)$$

8.1.5 Output Capacitor Selection

The output capacitor value depends on the total series resistance of the LED string, r_D, and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current, Δi_{LED}, is calculated using Equation 21.

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED}} \quad (21)$$

When choosing the output capacitors, consider the ESR and ESL characteristics because they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technology, consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with a voltage rating greater than maximum LED stack voltage.

8.1.6 Input Capacitor Selection

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. TI recommends a 10-µF input capacitor across the VIN pin and PGND placed close to the device, and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance.

In addition, a small case size 100-nF ceramic capacitor must be used across VIN to PGND, immediately adjacent to the device. This usage provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI.

The capacitance can be increased to further limit the input voltage deviation during PWM dimming operation.

8.1.7 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. The required capacitance depends on the PWM dimming frequency, PWM_{FREQ}, and is sized to avoid boot undervoltage and fault during PWM dimming operation. The bootstrap capacitance, C_{BST}, is calculated using Equation 22:

$$C_{BST} = \frac{I_{Q(BST,MAX)}}{\left(V_{CC} + V_{BST(HYS)} - V_{BST(UV)}\right) \times PWM_{FREQ}} \quad (22)$$

Table 8-2 summarizes the TI recommended bootstrap capacitor value for different PWM dimming frequencies.

Table 8-2. Bootstrap Capacitor Value

PWM DIMMING FREQUENCY (Hz)	BOOTSTRAP CAPACITOR (µF)
1500	0.1
1300	0.15
1000	0.22
800	0.22
600	0.33
400	0.47
200	1
100	2.2

8.1.8 Bootstrap Resistor Selection

A resistor can be connected between the C_{BST} capacitor and BST pin. A 4.7 resistor between the pins eliminates overshoot. Even with 2.2 Ω, overshoot and ringing are minimal, less than 4 V if input capacitors are placed correctly. A resistor value above 10 Ω is undesirable because the resulting incremental improvement in EMI is not enough to justify further decreased efficiency.

8.1.9 Compensation Capacitor Selection

TI recommends a simple integral compensator to achieve stable operation across the wide operating range. The buck converter behaves as a single pole system with additional phase lag caused by the switching behavior. The gain and phase margin are, consequently determined by the choice of the switching frequency and are independent of other design parameters. TI recommends a 1-nF to 10-nF capacitor to achieve bandwidth between 4 kHz and 40 kHz. The choice of compensation capacitor impacts the transient response and PWM dimming performance. TI recommends a larger compensation capacitor (lower bandwidth) to limit the LED current overshoot on the rising edge of internal or external PWM signal.

Table 8-3. Compensation Capacitor Value

BANDWIDTH (kHz)	BOOTSTRAP CAPACITOR (nF)
40	1
18	2.2
12	3.3
8.5	4.7
5.8	6.8
4.8	8.2
4	10

8.1.10 Input Dropout and Undervoltage Protection

Figure 8-1 shows that the undervoltage protection threshold is programmed using a resistor divider, R_{UV1} and R_{UV2}, from the input voltage, V_{IN} to PGND. Use Equation 23 and Equation 24 to calculate the resistor values.

$$R_{UV2} = \frac{2 \times V_{IN(UVLO,\,RISE)}}{I_{UDIM(DO)}} - \frac{V_{IN(DO,\,FALL)}}{I_{UDIM(DO)}} - 10 \times 10^{3} \quad (23)$$

$$R_{UV1} = \frac{V_{UDIM(EN,\,RISE)}}{V_{IN(UVLO,\,RISE)} - V_{UDIM(EN,\,RISE)}} \times R_{UV2} \quad (24)$$

A capacitor of 1 nF from UDIM pin to GND is placed close to device to improve noise immunity.

8.1.11 APWM Input and Thermal Protection

Figure 8-1 shows APWM input can be used in conjunction with NTC resistor to implement thermal foldback protection. TI recommends a network of 10-kΩ resistor and a 100-kΩ NTC with β-value (25/50°C) of 4250 K to implement thermal fold back from 80°C to 125°C.

8.1.12 Protection Diodes

External Schottky diodes are required to protect the CSP / CSN node by clamping the voltage during short circuit and open-circuit transients. The Schottky diode must be selected based on the length of the cable harness and the choice of output capacitor. TI recommends a Schottky diode with low forward voltage drop at room-temperature and non-repetitive peak surge current rating of 10 A for duration of 5 µs. The diodes from CSN to VIN and GND to CSN must be located close to the pin.

8.2 Typical Application

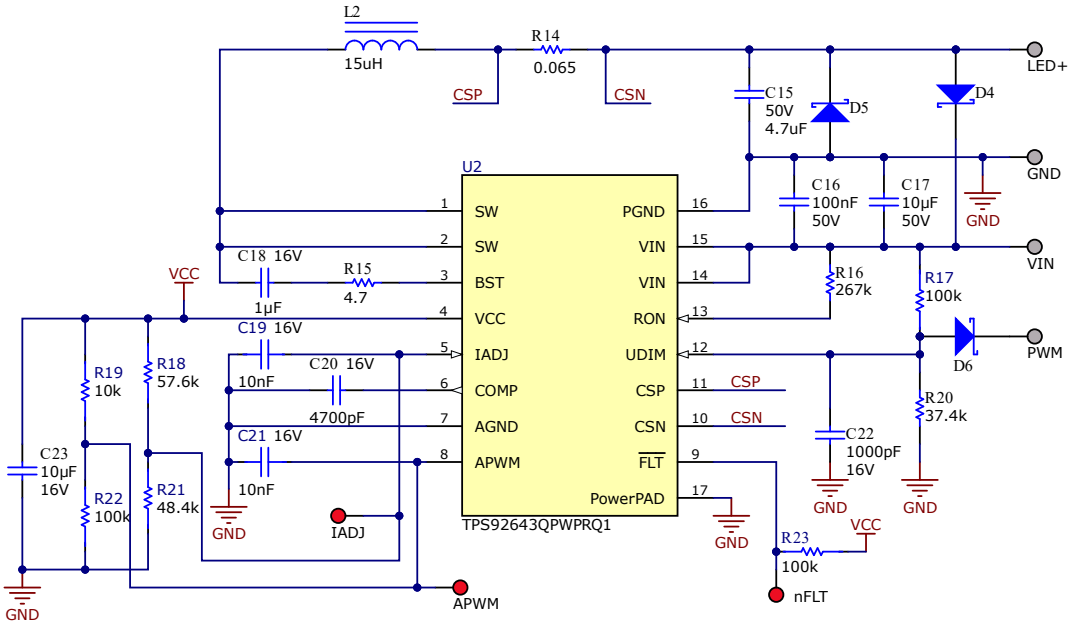


Figure 8-2. Application Schematic

8.2.1 Design Requirements

Table 8-4. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8	13.5	36	V
N_S	Number of LEDs			2		
V_{FLED}	LED forward voltage drop		2.6	3	3.4	V
r_D	LED string series resistance	$N \times r_{D(LED)}$	200		500	mΩ
V_{CSN}	Output voltage	$Ns \times V_{FLED}$	5.2	6	6.8	V
I_{LED}	LED current continuous		100		2500	mA
Δi_{LED}	LED current ripple				80	mA
Δi_L	Inductor current ripple	Defined as percentage peak-to-peak at maximum LED current	6.2			%
$V_{IN(DO,RISE)}$	Start input voltage	Input voltage rising		9		V
$V_{IN(DO,FALL)}$	Stop input voltage	Input voltage falling		7.9		V
f_{PWM}	PWM frequency			200		Hz
D_{PWM}	PWM dimming duty cycle		4		100	%
f_{SW}	Switching frequency			400		kHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Calculating Duty Cycle

Solve for duty cycle D, D_{MAX}, and D_{MIN}:

$$D_{MAX} = \frac{V_{CSN(MAX)}}{V_{IN(MIN)}} = \frac{6.8}{8} = 0.85 \quad (25)$$

$$D_{MIN} = \frac{V_{CSN(MIN)}}{V_{IN(MAX)}} = \frac{5.2}{36} = 0.144 \quad (26)$$

8.2.2.2 Calculating Minimum On-Time and Off-Time

Solve for minimum on-time, $t_{ON(DMIN)}$ at minimum duty cycle and minimum off-time, $t_{OFF(DMAX)}$ at maximum duty cycle:

$$t_{ON(DMAX)} = \frac{V_{CSN(MAX)}}{V_{IN(MIN)}} \times \frac{1}{f_{sw}} = \frac{6.8}{8} \times \frac{1}{400 \times 10^3} = 2125 \text{ ns} \quad (27)$$

$$t_{ON(DMIN)} = \frac{V_{CSN(MIN)}}{V_{IN(MAX)}} \times \frac{1}{f_{sw}} = \frac{5.2}{36} \times \frac{1}{400 \times 10^3} = 360 \text{ ns} \quad (28)$$

8.2.2.3 Minimum Switching Frequency

Confirm minimum switching frequency at $t_{ON(DMIN)}$, $f_{SW(MIN)}$:

$$f_{sw(MIN)} = \frac{V_{CSN(MIN)}}{t_{ON(DMIN)} \times V_{IN(MAX)}} = \frac{5.2}{360 \times 10^{-9} \times 36} = 401.2 \text{ kHz} \quad (29)$$

For the design specification, $t_{ON(DMIN)} > t_{ON(MIN)}$ and $f_{SW(MIN)} = f_{SW}$.

8.2.2.4 LED Current Set Point

Solve for sense resistor, R_{CS}:

$$R_{CS} = \frac{V_{IADJ(MAX)}}{14 \times I_{LED(MAX)}} = \frac{2.3}{14 \times 2.5} = 0.0657 \quad (30)$$

A standard resistor of 65 mΩ with tolerance better than 1 % and low temperature coefficient is selected. The power dissipated in R_{CS} is calculated:

$$P_{sense} = R_{CS} \times I^2_{LED(MAX)} = 0.065 \times 2.5^2 = 0.406 \text{ W} \quad (31)$$

A resistor with rated power of 500 mW and above must be selected.

A resistor divider network, with standard values 57.6 kΩ and 48.4 kΩ, from VCC pin to GND sets the maximum LED current reference voltage of 2.3 V. A 10-nF capacitor from IADJ pin to AGND pin is included to filter high frequency switching noise.

8.2.2.5 Inductor Selection

The inductor is selected to meet the recommended peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$:

$$L = \frac{V_{IN,MIN} - V_{CSN,MAX}}{\Delta i_L \times f_{SW}} \times \frac{V_{CSN,MAX}}{V_{IN,MIN}} = \frac{8 - 6.8}{155 \times 10^{-3} \times 400 \times 10^3} \times \frac{6.8}{8} = 16.45 \times 10^{-6} \quad (32)$$

The closest standard capacitor is 15 µH.

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost at the expense of reduced efficiency and larger output capacitor.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency but reduces the operating range based on minimum sense voltage ripple, $\Delta V_{(CSP-CSN)}$ specification.

8.2.2.6 Output Capacitor Selection

The minimum output capacitance is selected to meet the LED current ripple specification:

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_{D(MAX)} \times \Delta i_{LED}} = \frac{0.5625}{8 \times 400 \times 10^{3} \times 0.5 \times 80 \times 10^{-3}} = 4.4 \times 10^{-6} \quad (33)$$

A standard 4.7-µF, 50-V X7R capacitor is selected.

8.2.2.7 Bootstrap Capacitor Selection

Referring to Table 8-2 , a standard 1-µF, 16-V X7R capacitor is selected to support PWM frequency of 200 Hz.

8.2.2.8 Bootstrap Resistor Selection

A standard 4.7-Ω bootstrap resistor is selected to limit ringing and mitigate EMI.

8.2.2.9 Compensation Capacitor Selection

A compensation capacitor of 4.7 nF is selected to achieve balanced transient response between PWM dimming and shunt FET dimming.

8.2.2.10 VIN Dropout Protection and PWM Dimming

The resistor divider, R_{UV1} and R_{UV2}, is set to meet $V_{IN(UVLO,RISE)}$ and $V_{IN(DO,FALL)}$ thresholds.

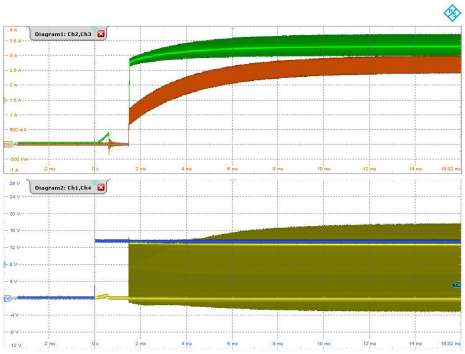
$$R_{UV2} = \frac{2 \times 4.5}{10 \times 10^{-6}} - \frac{7.9}{10 \times 10^{-6}} - 10 \times 10^{3} = 100 \times 10^{3} \quad (34)$$

$$R_{UV1} = \frac{1.22}{4.5 - 1.22} \times 100 \times 10^{3} = 37.2 \times 10^{3} \quad (35)$$

A standard value resistors of 100 kΩ and 37.4 kΩ are selected for R_{UV2} and R_{UV1}, respectively.

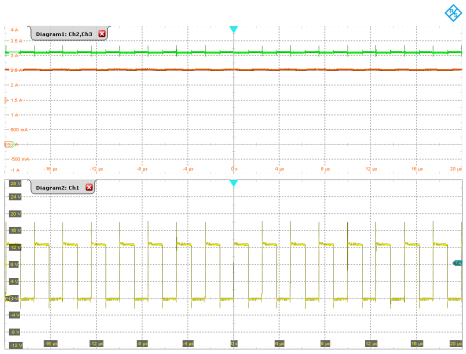
The external PWM signal is achieved by controlling UDIM input. The device modulates the LED current based on the PWM duty cycle of the external signal, coupled through external diode.

8.2.3 Application Curves



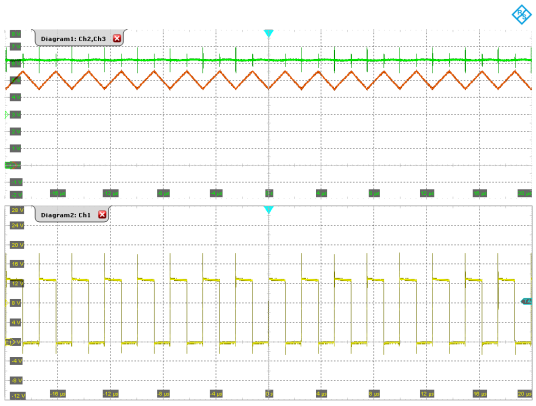
Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: Inductor current (500 mA/div); Ch4: VIN voltage (4 V/div); Time: 2 ms/div

Figure 8-3. Start-up Transient



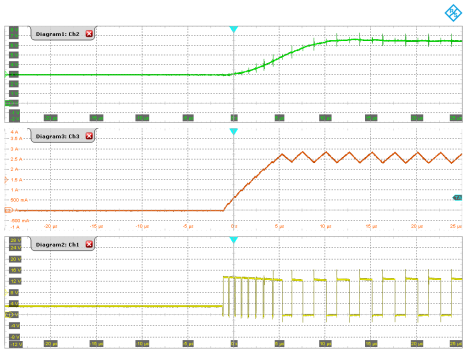
Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: LED current (500 mA/div); Time: 4 µs/div

Figure 8-4. Normal Operation



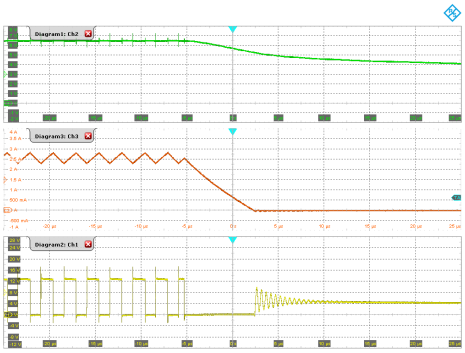
Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: Inductor current (500 mA/div); Time: 4 µs/div

Figure 8-5. Normal Operation



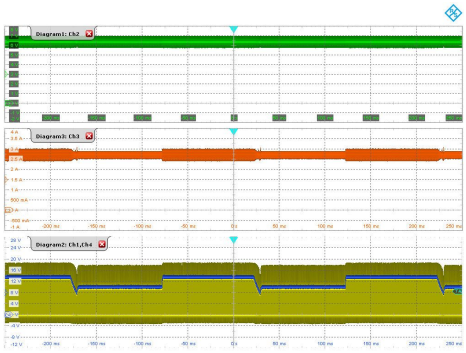
Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: Inductor current (500 mA/div); Time: 5 µs/div

Figure 8-6. PWM Dimming (Rising Edge)



Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: Inductor current (500 mA/div); Time: 5 µs/div

Figure 8-7. PWM Dimming (Falling Edge)

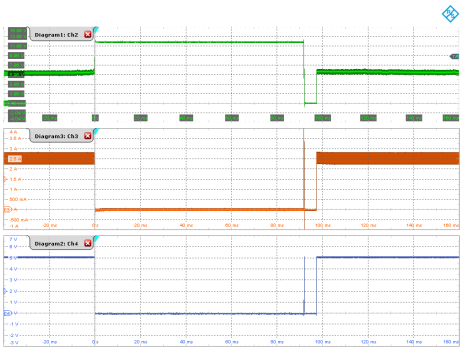


Ch1: SW voltage (4 V/div); Ch2: Output voltage (1 V/div); Ch3: LED current (500 mA/div); Ch4: VIN voltage (4 V/div); Time: 50 ms/div

Figure 8-8. Input Dropout Transient

Ch2: Output voltage (1 V/div); Ch3: LED current (500 mA/div); Ch4: $\overline{FLT}$ voltage (1 V/div); Time: 20 ms/div

Figure 8-9. Output Short-Circuit Fault



Ch2: Output voltage (1 V/div); Ch3: LED current (500 mA/div); Ch4: $\overline{FLT}$ voltage (1 V/div); Time: 20 ms/div

Figure 8-10. Output Open-Circuit Fault

9 Power Supply Recommendations

The characteristics of the input supply must be compatible with *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter.

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter or tripping UVLO. Additional bulk capacitance or an input filter can be required in addition to the ceramic bypass capacitors to address converter stability, noise, and EMI concerns.

10 Layout

10.1 Layout Guidelines

The performance of any switching converter depends as much on the layout of the PCB as the component selection. The following guidelines can help design a PCB with the best power converter performance.

- Place ceramic high-frequency bypass capacitors as close as possible to the TPS92643-Q1 VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pin.
- Place bypass capacitors for VCC close to the pins and ground the capacitors to device ground.
- Use wide traces for the C_{BST} capacitor and R_{BST} resistor. Place R_{BST} and C_{BST} network as close as possible to BST pin and SW pin.
- Differentially route the CSP and CSN pins to sense resistor. Route the traces away from noisy nodes, preferably through a layer on the other side of a shielding/ground layer.
- Use ground plane in one of the middle layers for noise shielding.
- Make VIN and ground connection as wide as possible. This action reduces any voltage drops on the input of the converter and maximizes efficiency.
- Keep switch area small. Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

10.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt from pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In buck converters, the pulsing current path is from the VIN side of the input capacitors through the HS switch, through the LS switch, and then returns to the ground of the input capacitor.

High-frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic capacitors as close as possible to the VIN and PGND pins is the key to EMI reduction.

The PCB copper connection of the SW pin to the inductor must be as short as possible and just wide enough to carry the LED current without excessive heating. Short, thick traces or, copper pours (shapes), must be used for high current conduction path to minimize parasitic resistance. Place the output capacitor close to the CSN pin and grounded closely to the PGND pin.

10.1.1.1 Ground Plane

TI recommends using one of the middle layers as a solid ground plane. The ground plane provides shielding for sensitive circuits and traces. the ground plane also provides a quiet reference potential for the control circuitry. Connect the GND, AGND and PGND pins to the ground plane using via right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations.

10.2 Layout Example

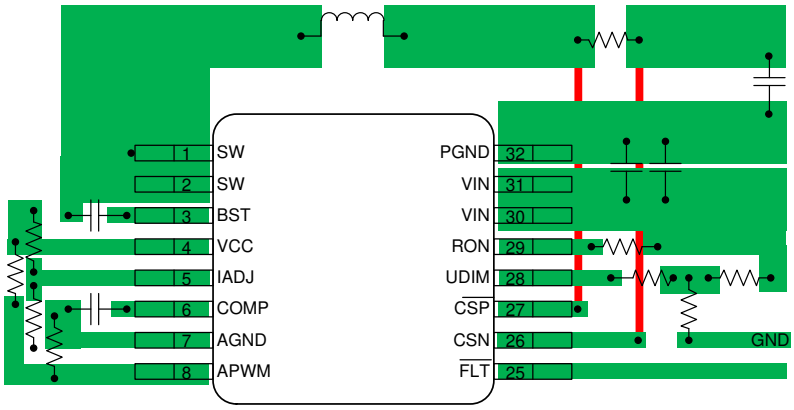


Figure 10-1. TPS92643-Q1 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92643QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92643Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

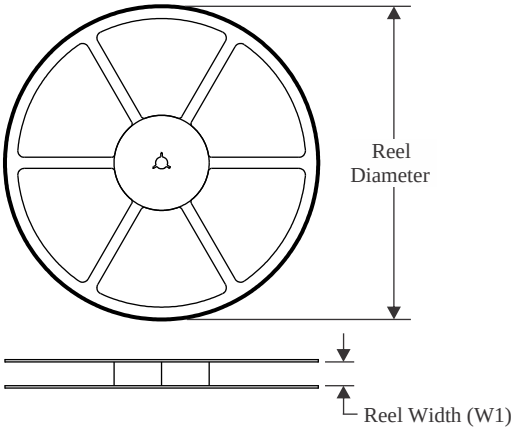
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

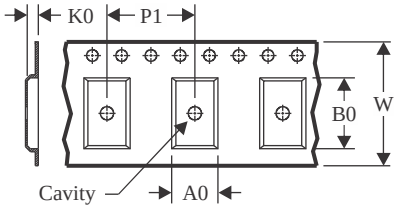
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

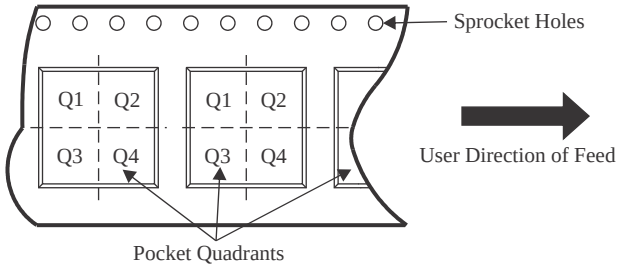


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

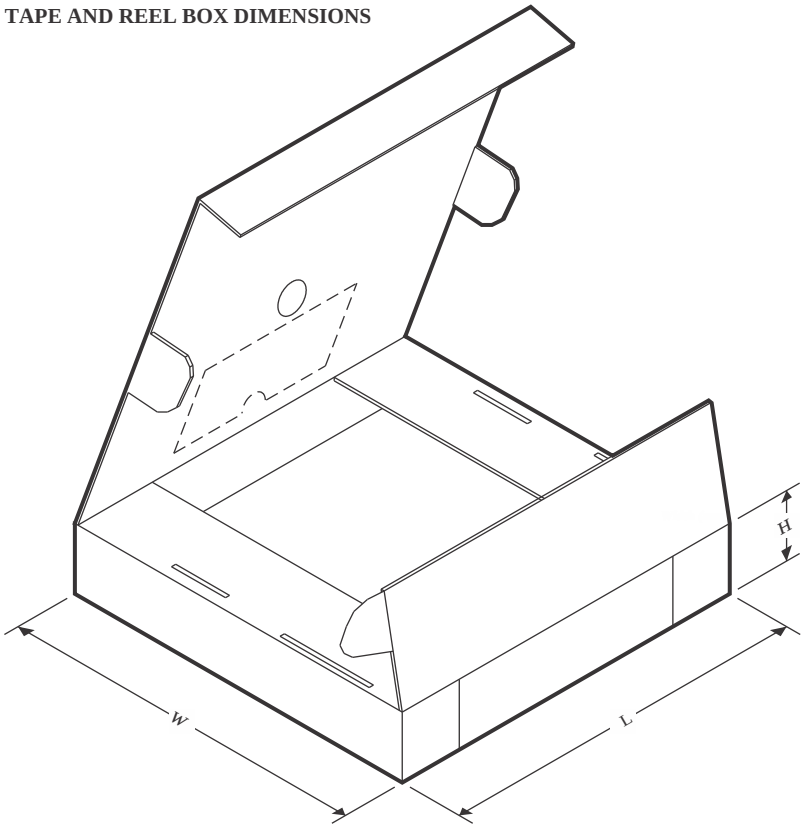
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92643QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

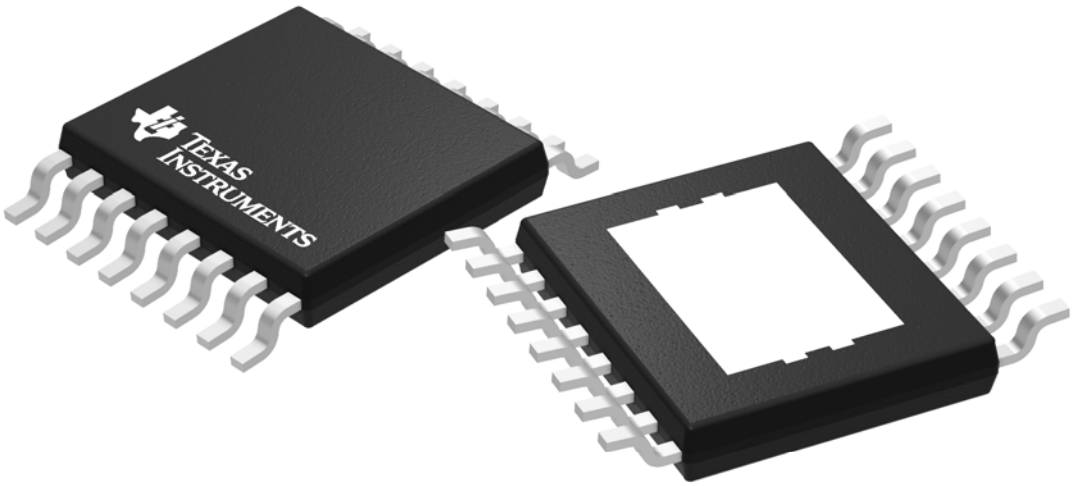


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92643QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



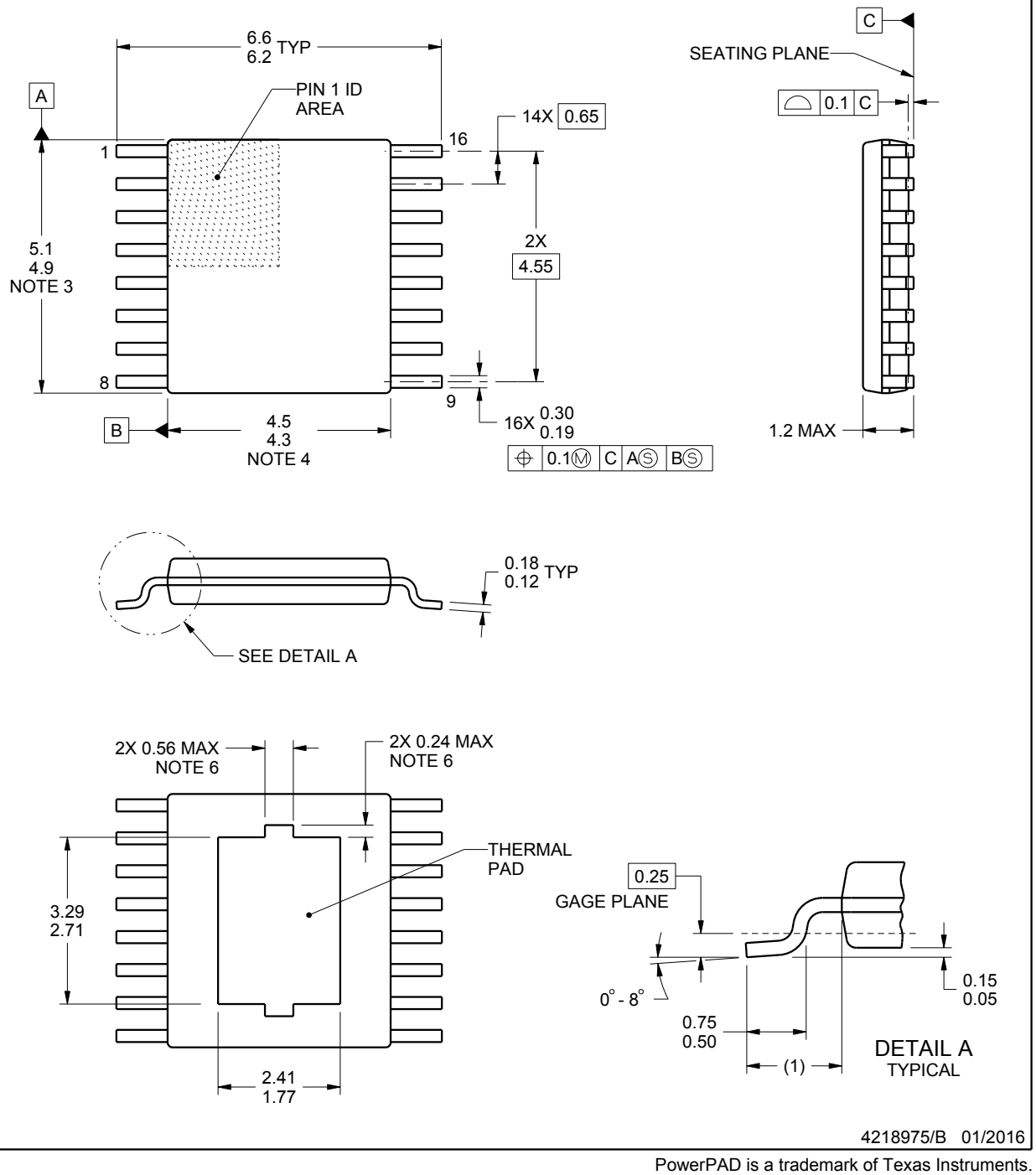
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PWP0016G

PowerPAD™ TSSOP - 1.2 mm max height

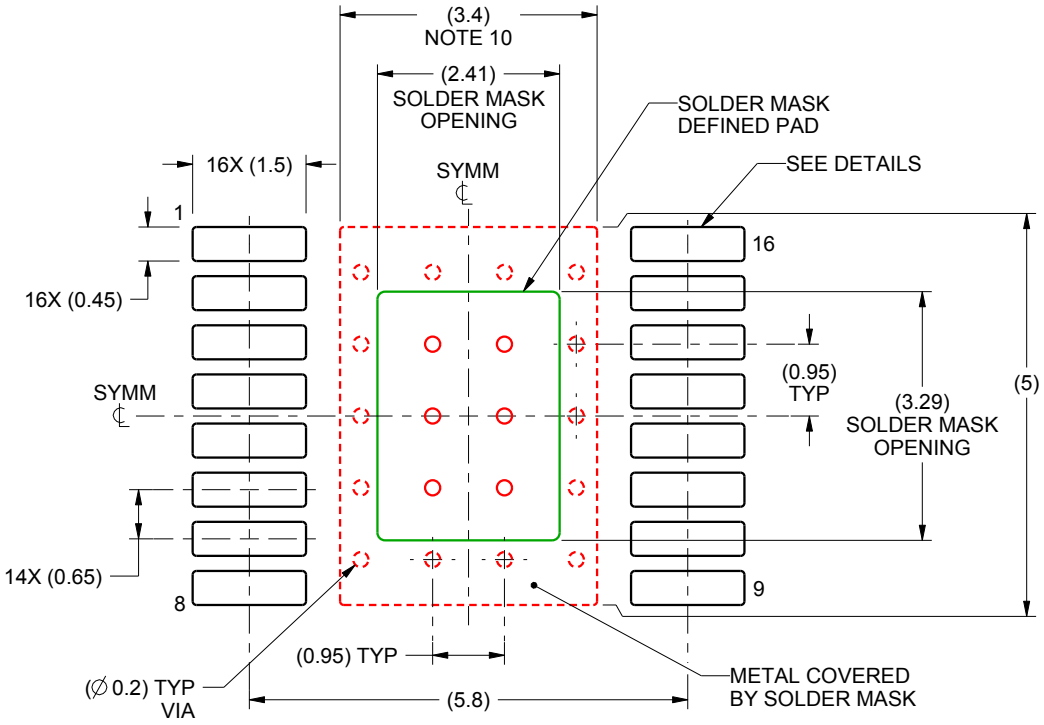
PLASTIC SMALL OUTLINE



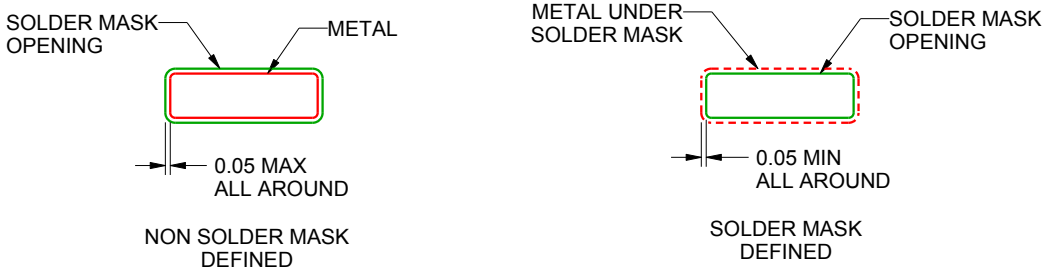
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
6. Features may not present.



LAND PATTERN EXAMPLE
SCALE:10X

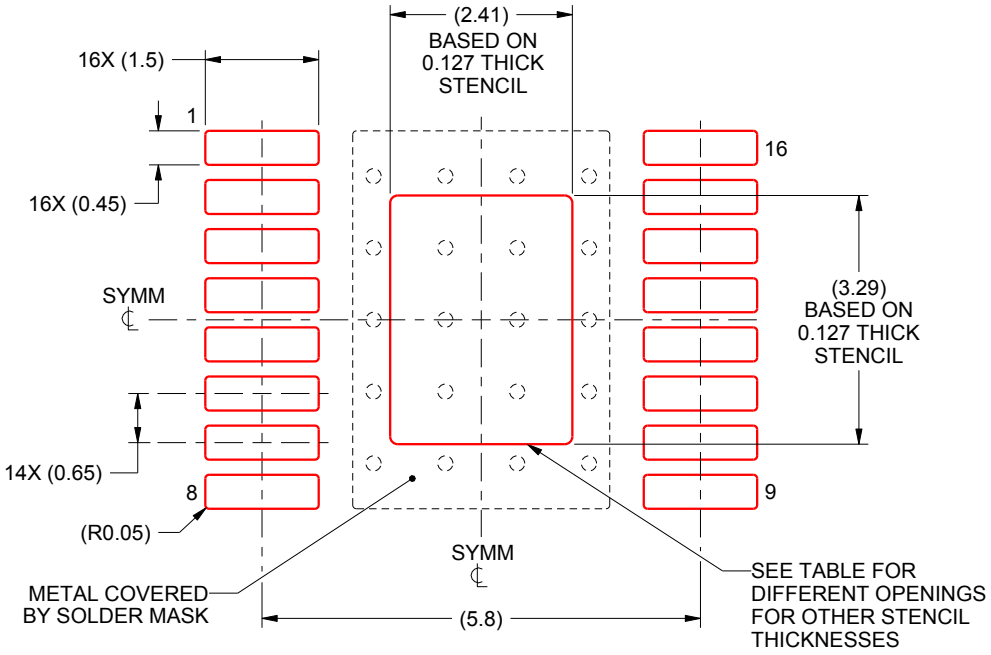


SOLDER MASK DETAILS
PADS 1-16

4218975/B 01/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.69 X 3.68
0.127	2.41 X 3.29 (SHOWN)
0.152	2.20 X 3.00
0.178	2.04 X 2.78

4218975/B 01/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
TPS92664-Q1
SLUSF16 – JULY 2022

TPS92664-Q1 Automotive Low Noise 16-Channel LED Matrix Manager with Advance Diagnostics, Integrated Oscillator, and EEPROM

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient temperature
  - Device HBM classification level H1C
  - Device CDM classification level C5
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL B
- 16 integrated bypass switches
  - Programmable 10-bit PWM dimming
  - Programmable slew rate control
  - LED open detection and protection
  - Single LED short detection
- UART serial communication
  - Internal oscillator for system clock
  - LVDS clock driver for synchronizing devices
  - Previous LMM generation compatible
  - CAN transceiver compatible
- Integrated ADC
  - LED voltage for each switch
  - LED current monitor
  - Die temperature
  - 2x general ADC inputs (thermistor compatible)
- Internal EEPROM (MTP)
  - Failsafe default settings
  - Customer calibration data

2 Applications

- Automotive headlight systems
- ADB or glare-free high beam
- Sequential turn, animated daytime running lights

3 Description

The TPS92664 LED matrix manager device enables fully dynamic adaptive lighting solutions by providing individual pixel-level LED control. The device includes four sub-strings of four series connected integrated switches for bypassing individual LEDs. The individual sub-strings allow the device to accept either single or multiple current sources.

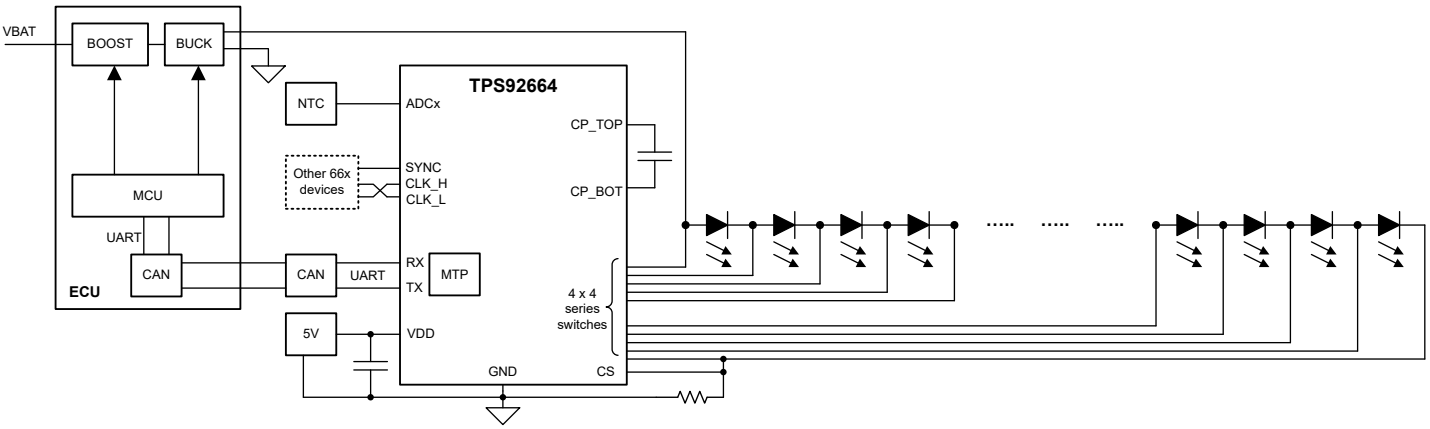
The TPS92664 features an internal oscillator. The internal oscillator can be shared to other system devices through the internal low noise LVDS transmitter and receiver blocks. The multi-drop, universal, asynchronous, receiver transmitter (UART) serial interface is compatible with TPS92665, TPS92667, TPS92662x and TPS92663x devices. The internal EEPROM can store system defaults as well as calibration and lighting module data. An on-board ADC with multiplexed inputs samples all LED channels as well as IC die temperature and an LED current sense. The ADC also samples dedicated ADC inputs for use with system temperature compensation, LED binning and coding.

The TPS92664 incorporates registers for programming phase shift and pulse width of each individual LED in the string and for reporting LED open, short faults and functional parameters.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS92664-Q1	PHP (HTQFP, 48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

4.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92664QPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92664Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

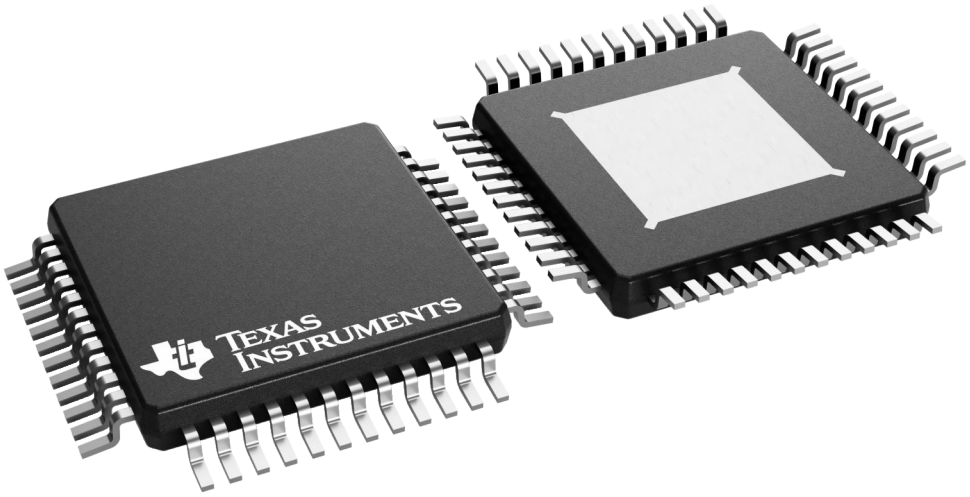
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



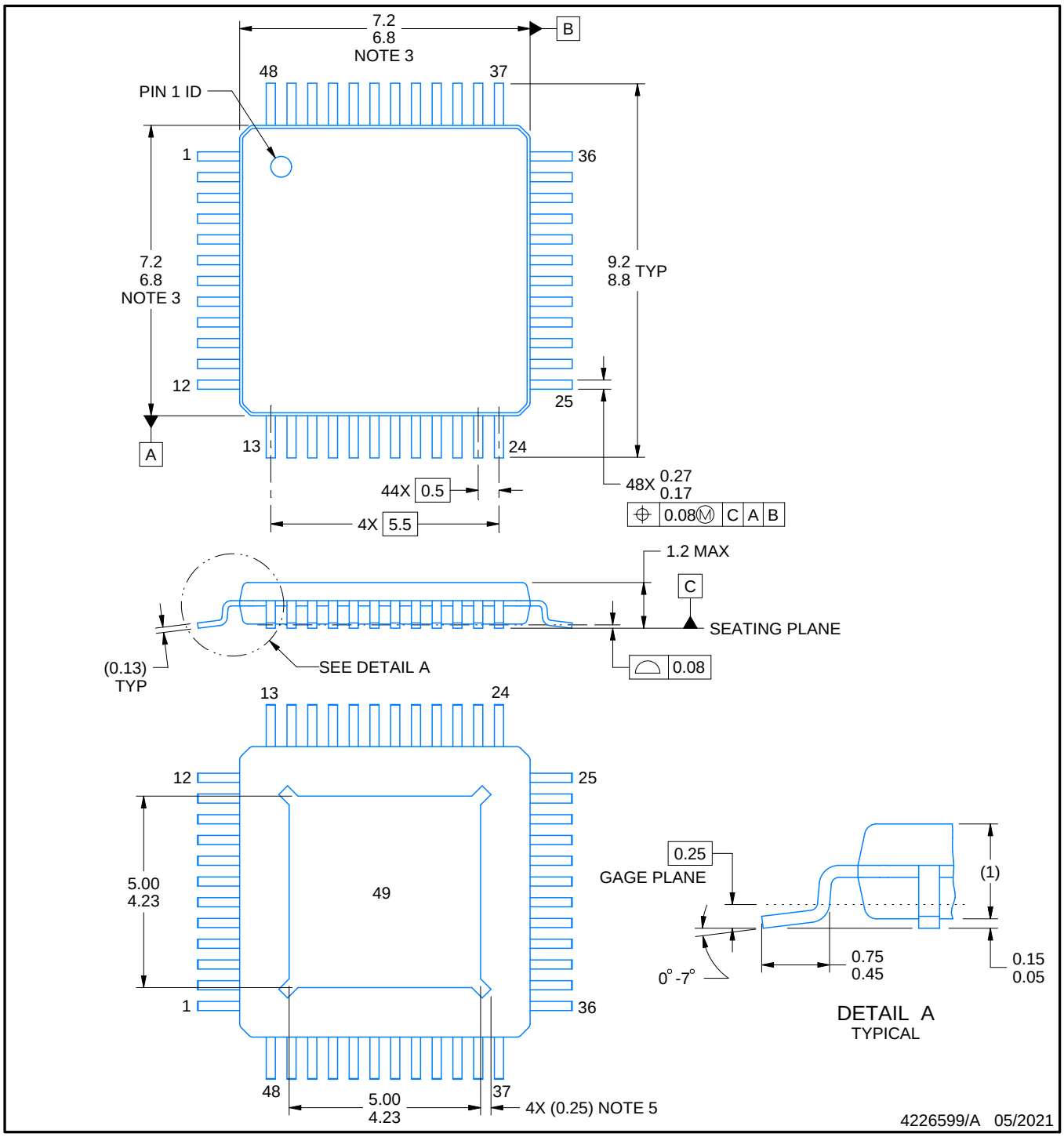
4226443/A

PACKAGE OUTLINE

PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

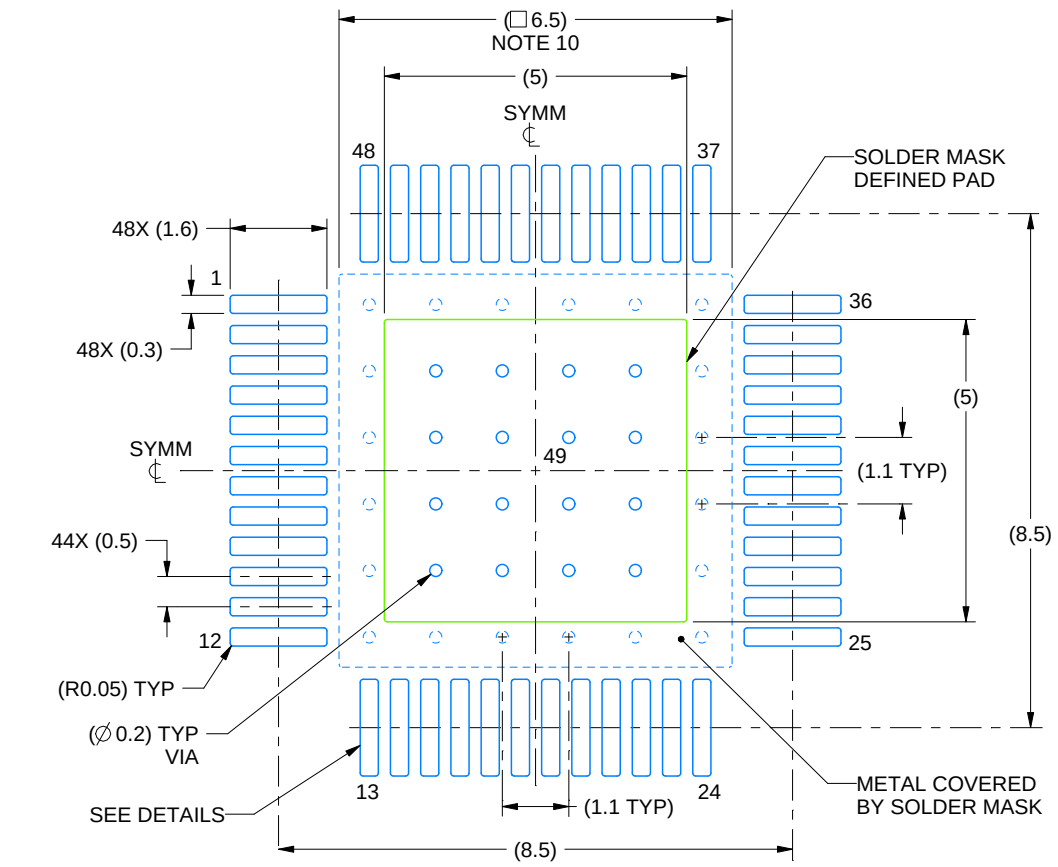
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

EXAMPLE BOARD LAYOUT

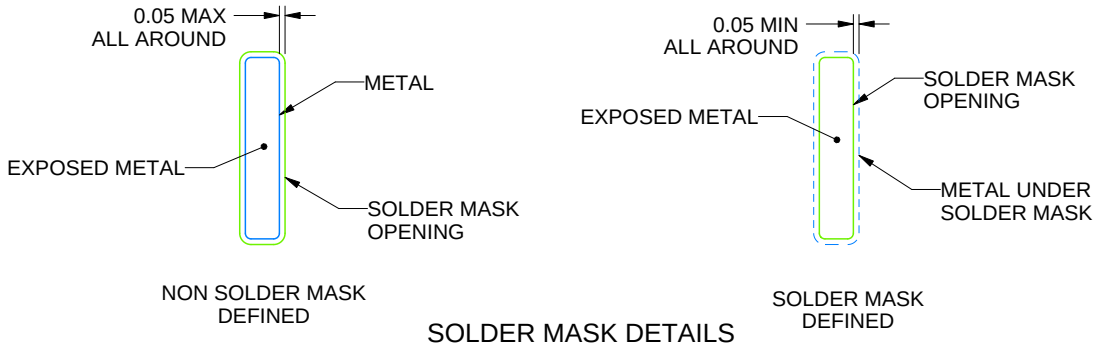
PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

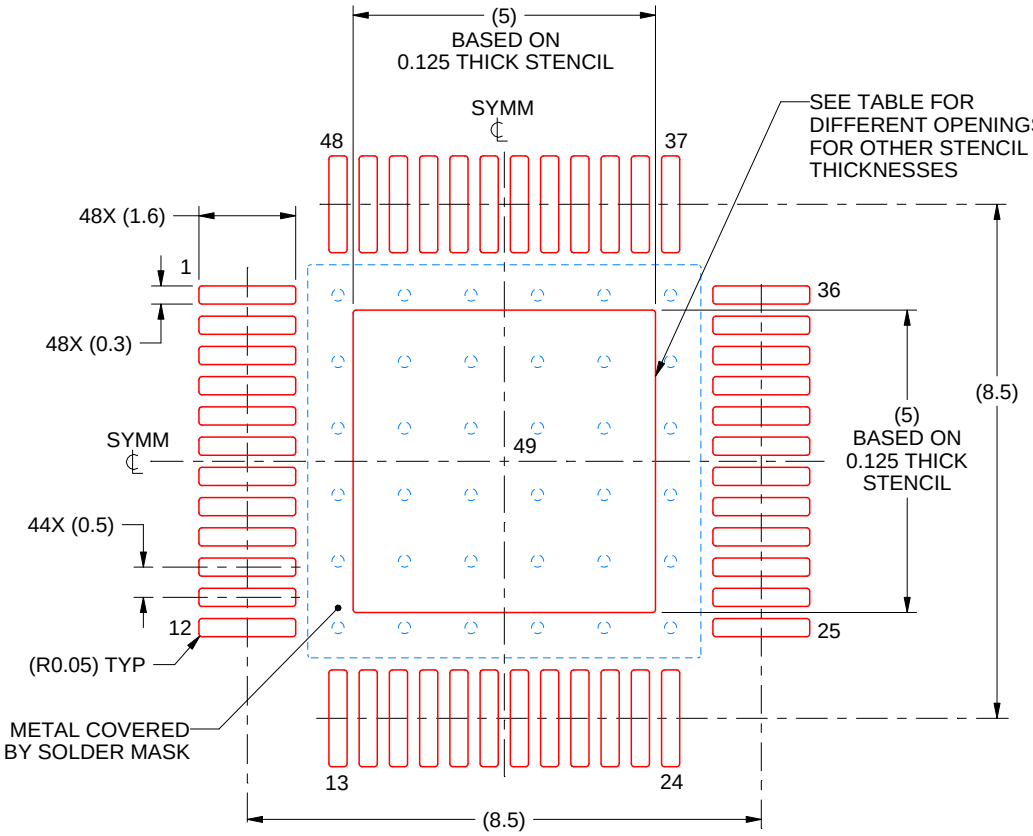


SOLDER MASK DETAILS

4226599/A 05/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.59 X 5.59
0.125	5.00 X 5.00 (SHOWN)
0.150	4.56 X 4.56
0.175	4.23 X 4.23

4226599/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPSI3052-Q1 Automotive Reinforced Isolated Switch Driver with Integrated 15-V Gate Supply

1 Features

- No isolated secondary supply required
- Drives external power transistors or SCRs
- 5-kV_{RMS} reinforced isolation
- 15-V gate drive with 1.5/3-A peak source and sink current
- Up to 50-mW supply for external auxiliary circuitry
- Supports AC or DC switching
- Supports two-wire or three-wire modes
- Seven levels of power transfer, resistor selectable
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Automotive temperature range –40 to 125°C, AEC-Q100 qualified ambient
- Safety-related certifications
  - Planned: 7071-V_{PK} reinforced isolation per DIN V VDE 0884-11:2017-01
  - Planned: 5-kV_{RMS} isolation for 1 minute per UL 1577

2 Applications

- Solid State Relays (SSR)
- Battery management system
- On-board charger
- Hybrid, electric, and powertrain systems
- Building automation
- Factory automation and control

3 Description

The TPSI3052-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated Solid State Relay (SSR). With a nominal gate drive voltage of 15 V with 1.5/3.0-A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required. Additionally, the TPSI3052-Q1 can optionally supply power to external supporting circuitry for various application needs.

The TPSI3052-Q1 supports two modes of operation based on the number of input pins required. In two-wire mode, typically found in driving mechanical relays, controlling the switch requires only two pins and supports a wide voltage range of operation of 6.5 V to 48 V. In three-wire mode, the primary supply of 3 V to 5.5 V is supplied externally, and the switch is controlled through a separate enable. Available in three-wire mode only, the TPSI3052S-Q1 features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

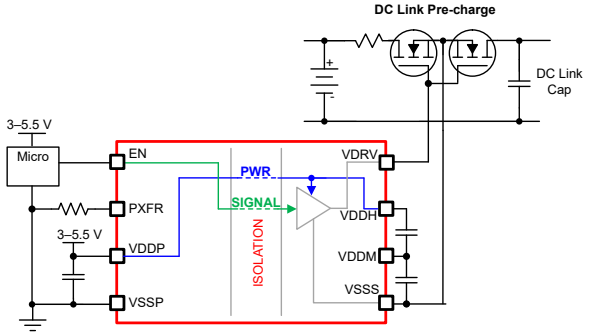
The secondary side provides a regulated, floating supply rail of 15 V for driving a large variety of power switches with no need for a secondary bias supply. The application can drive single power switches for DC applications or dual back-to-back power switches for AC applications, as well as various types of SCR. The TPSI3052-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than traditional mechanical relays and optocouplers.

The power transfer of the TPSI3052-Q1 can be adjusted by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP. This action allows for tradeoffs in power dissipation versus power provided on the secondary depending on the needs of the application.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPSI3052-Q1	SOIC 8-pin (DWZ)	7.50 mm × 5.85 mm
TPSI3052S-Q1	SOIC 8-pin (DWZ)	7.50 mm × 5.85 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TPSI3052-Q1 Simplified Schematic

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2022	*	Initial Release

5 Pin Configuration and Functions

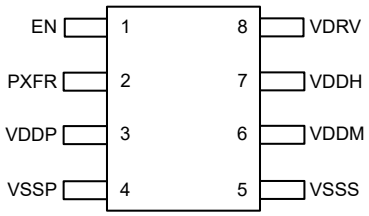


Figure 5-1. TPSI3052-Q1, TPSI3052S-Q1 8-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable
2	PXFR	I	—	Power transfer can be adjusted by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP. In three-wire mode, a given resistor setting sets the duty cycle of the power converter (see Table 8-1) and hence the amount of power transferred. In two-wire mode, a given resistor setting adjusts the current limit of the EN pin (see Table 8-2) and hence the amount of power transferred.
3	VDDP	—	P	Power supply for primary side
4	VSSP	—	GND	Ground supply for primary side
5	VSSS	—	GND	Ground supply for secondary side
6	VDDM	—	P	Generated mid supply
7	VDDH	—	P	Generated high supply
8	VDRV	O	—	Active high driver output

(1) P = power, GND = ground, NC = no connect

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary Side Supply(2)	VDDP	–0.3	6	V
Primary Side Supply(2)	EN	–0.3	60	V
Primary Side Supply(2)	PXFR	–0.3	60	V
Secondary Side Supply(3)	VDRV	–0.3	18	V
Secondary Side Supply(3)	VDDH	–0.3	18	V
Secondary Side Supply(3)	VDDM	–0.3	6	V
Secondary Side Supply(3)	VDDH-VDDM	–0.3	12	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP.
(3) All voltage values are with respect to VSSS.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C2a	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage(1)	3.0		5.5	V
EN	Enable in two-wire mode(1)	0		48.0	V
	Enable in three-wire mode(1)	0		5.5	V
PXFR	Power transfer control(1)	0		5.5	V
C_{IN}	Decoupling capacitance on VDDP and VSSP, two-wire mode(3)	220		500	nF
	Decoupling capacitance on VDDP and VSSP, three-wire mode(3)	0.22		20	µF
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.004		15	µF
C_{DIV2} (2)	Decoupling capacitances across VDDM and VSSS(3)	0.012		40	µF
T_A	Ambient operating temperature	–40		125	°C

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geq 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.

6.4 Thermal Information

THERMAL METRIC(1) (2)		DEVICE DWZ(SOIC) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	89.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	45.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W

(1) Estimate only.
(2) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	V_{VDDP} = 5 V, R_{PXFR} = 20 kΩ, three-wire mode, C_{VDRV} = 100 pF, C_{DIV1} = 33 nF, C_{DIV2} = 100 nF f_{EN} = 1-kHz square wave, V_{EN} = 5 V peak to peak.			250	mW
		R_{PXFR} = 20 kΩ, two-wire mode, C_{VDRV} = 100 pF, C_{DIV1} = 33 nF, C_{DIV2} = 100 nF f_{EN} = 1-kHz square wave, V_{EN} = 48 V peak to peak.k.			350	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8.5	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE 0884-11:2017-01, IEC 60747-17:2020				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}

ADVANCE INFORMATION

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test.	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production).	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	$V_{TEST} = 1.6 \times V_{IOSM} = 12000\ V_{PK}$ (qualification).	7500	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1697\ V_{PK}$, t_m = 10 s.	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2262\ V_{PK}$, t_m = 10 s.	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2651\ V_{PK}$, t_m = 1 s.	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	3	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{13}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{12}	
		V_{IO} = 500 V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN V VDE 0884-11:2017-01	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 7500 V_{PK}	Single protection, 5000 V_{RMS}
Certificate planned	Certificate planned

6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 89.3°C/W, V_{VDDP} = 5.5 V, T_J = 150°C, T_A = 25°C, three-wire mode.			254	mA
		$R_{\theta JA}$ = 89.3°C/W, V_{EN} = 24 V, T_J = 150°C, T_A = 25°C, two-wire mode.			58	
		$R_{\theta JA}$ = 89.3°C/W, V_{EN} = 48 V, T_J = 150°C, T_A = 25°C, two-wire mode.			29	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 89.3°C/W, T_J = 150°C, T_A = 25°C.			1.4	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
$V_{VDDP\_UV\_R}$	VDDP under-voltage threshold rising	VDDP rising	2.50	2.70	2.90	V
$V_{VDDP\_UV\_F}$	VDDP under-voltage threshold falling	VDDP falling	2.35	2.55	2.75	V
$V_{VDDP\_UV\_HYS}$	VDDP under-voltage threshold hysterisis			150		mV
TSD	Temperature shutdown			173		℃
TSDH	Temperature shutdown hysteresis			32		℃
R_{DSON_VDRV}	Driver on resistance in low state.	Force V_{VDDH} = 15 V, sink I_{VDRV} = 50 mA.			2.5	Ω
	Driver on resistance in high state.	Force V_{VDDH} = 15 V, source I_{VDRV} = 50 mA.			5.2	Ω
$V_{VDDH\_UV\_R}$	VDDH under-voltage threshold rising	VDDH rising.	12.5	13	13.4	V
$V_{VDDH\_UV\_F}$	VDDH under-voltage threshold falling. TPSI3052-Q1 only.	VDDH falling.	11.1	11.4	11.9	V
	VDDH under-voltage threshold falling. TPSI3052S-Q1 only. One-shot enable only available in three-wire mode.	VDDH falling.	11.8	12.1	12.6	V

ADVANCE INFORMATION

6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDDH\_UV\_HYS}$	VDDH under-voltage threshold hysterisis. TPSI3052-Q1 only. One-shot enable only available in three-wire mode.			1.5		V
	VDDH under-voltage threshold hysterisis. TPSI3052S-Q1 only.			0.8		V
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 1000 V			50	V/ns
TWO-WIRE MODE						
V_{IH_EN}	Minimum voltage on EN to be detected as a valid logic high.		6.5			V
V_{IL_EN}	Maximum voltage on EN to be detected as a valid logic low.				2.0	V
I_{EN_START}	Enable current at startup	EN = 0 V → 6.5 V		27		mA
I_{EN}	Enable current steady state	EN = 6.5 V, R_{PXFR} = 7.32 kΩ, R_{PXFR} ≥100 kΩ or R_{PXFR} ≤1 kΩ, V_{VDDH} in steady state.		1.9		mA
		EN = 6.5 V, R_{PXFR} = 20 kΩ, V_{VDDH} in steady state.		6.7		mA
V_{VDDP_H}	VDDP positive hysteretic control threshold	EN = 6.5 V, V_{VDDH} in steady state, measure positive peak VDDP level.		4.5		V
V_{VDDH}	VDDH output voltage	EN = 6.5 V, V_{VDDH} in steady state.	13.9	15	16.2	V
V_{VDRV_H}	VDRV output voltage driven high	EN = 6.5 V, V_{VDDH} in steady state, no DC loading.	13.9	15	16.2	V
V_{VDRV_L}	VDRV output voltage driven low	EN = 6.5 V, V_{VDDH} in steady state, sink 10 mA load.	0		0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	EN = 0 V → 6.5 V, measure peak current.		1.5		A
	VDRV peak output current during fall	EN = 6.5 V → 0 V, measure peak current.		3		A
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	EN = 6.5 V, steady state. R_{PXFR} = 7.32 kΩ, R_{PXFR} ≥ 100 kΩ or R_{PXFR} ≤ 1 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, source 0.275 mA from VDDM, measure VDDM voltage.	4.7		5.5	V
	Average VDDM voltage when sourcing external current.	EN = 6.5 V, steady state. R_{PXFR} = 20 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, source 1.4 mA from VDDM, measure VDDM voltage.	4.7		5.5	V
THREE-WIRE MODE						
V_{IH_EN}	Minimum voltage on EN to be detected as a valid logic high. $V_{IH(min)}$ = 0.7 x V_{VDDP}	V_{VDDP} = 3 V	2.1			V
		V_{VDDP} = 5.5 V	3.85			V

ADVANCE INFORMATION

6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_EN}	Maximum voltage on EN to be detected as a valid logic low.	V_{VDDP} = 3 V			0.9	V
		V_{VDDP} = 5.5 V			1.65	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.	V_{VDDP} = 3 V		0.33		V
		V_{VDDP} = 5.5 V		0.5		V
I_{VDDP_START}	VDDP current at startup	EN = 0 V, V_{VDDP} = 0 V → 3.3 V, Measure average current while power conversion is active.		32		mA
I_{VDDP}	VDDP average current in steady state	EN = 3.3 V, V_{VDDP} = 3.3 V, R_{PXFR} = 7.32 kΩ, R_{PXFR} ≥ 100 kΩ or R_{PXFR} ≤ 1 kΩ, V_{VDDH} in steady state, measure I_{VDDP}.		4.5		mA
		EN = 3.3 V, V_{VDDP} = 3.3 V, R_{PXFR} = 20 kΩ, V_{VDDH} in steady state, measure I_{VDDP}.		33		
V_{VDDH}	VDDH output voltage	V_{VDDP} = 3.0 V, EN = 3.0 V, V_{VDDH} in steady state.	13.9	15	16.2	V
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 3.0 V, EN = 3.0 V, V_{VDDH} in steady state, no DC loading.	13.9	15	16.2	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 3.0 V, EN = 0 V, V_{VDDH} in steady state, VDRV sinking 10 mA.	0		0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 3.3 V, EN = 0 V → 3.3 V, V_{VDDH} in steady state, measure peak current.		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 3.3 V, EN =3.3 V → 0 V, V_{VDDH} in steady state, measure peak current.		3		A
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 3.3 V, EN = 0.0 V, steady state. R_{PXFR} = 7.32 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 0.35 mA from VDDM measure V_{VDDM}.	4.7		5.5	V
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5.0 V, EN = 0.0 V, steady state. R_{PXFR} = 7.32 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 0.50 mA from VDDM measure V_{VDDM}.	4.7		5.5	V

ADVANCE INFORMATION

6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 3.3 V, EN = 0.0 V, steady state. R_{PXFR} = 20 kΩ C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 3.0 mA from VDDM measure V_{VDDM}.	4.7		5.5	V
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5.0 V, EN = 0.0 V, steady state. R_{PXFR} = 20 kΩ C_{DIV1} = 75 nF C_{DIV2} = 220 nF Source 5.0 mA from VDDM measure V_{VDDM}.	4.7		5.5	V

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_L = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TWO-WIRE MODE						
t_{LO_EN}	Low time of EN.		5			µs
$t_{LH\_VDDP\_H}$	Propagation delay time from EN rising to V_{VDDP_H}.	EN = 0 V → 6.5 V.		37		µs
t_{LH_VDDH}	Propagation delay time from EN rising to VDDH at 50% level.	EN = 0 V → 6.5 V, V_{VDDH} = 7.5 V.		175		µs
t_{HL_VDDH}	Propagation delay time from EN falling to VDDH at 50% level.	EN = 6.5 V → 0 V, V_{VDDH} = 7.5 V.		650		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level.	EN = 0 V → 6.5 V, V_{VDRV} = 13.5 V.		450		µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level.	EN = 6.5 V → 0 V, V_{VDRV} = 1.5 V.		2.5	3.0	µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level.	EN = 0 V → 6.5 V, V_{VDRV} = 2.25 V to 12.75 V.		5		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level.	EN = 6.5 V → 0 V, V_{VDRV} = 12.75 V to 2.25 V.		5		ns
THREE-WIRE MODE						
t_{LO_EN}	Low time of EN.	V_{VDDP} = 3.3 V, V_{VDDH} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDP} = 3.3 V, V_{VDDH} = steady state.	5			µs
t_{HI_VDRV}	High time of VDRV in one-shot enable mode. TPSI3052S-Q1 only. One-shot enable only available in three-wire mode.	V_{VDDP} = 3.3 V, steady state.		2.5		µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0 V, V_{VDDP} = 0 V → 3.3 V at 1 V/µs, V_{VDDH} = 7.5 V.		60		µs
t_{HL_VDDH}	Propagation delay time from VDDP falling to VDDH at 50% level	EN = 0 V, V_{VDDP} = 3.3 V → 0 V at -1 V/µs, V_{VDDH} = 7.5 V.		650		µs

ADVANCE INFORMATION

6.10 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_L = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 0 V → 3.3 V, V_{VDRV} = 13.5 V.		3	4	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 3.3 V → 0 V, V_{VDRV} = 1.5 V.		2.5	3.0	µs
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 3.3 V, V_{VDDP} = 3.3 V → 0 V at -1 V/µs, V_{VDRV} = 1.5 V.		300		µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 0 V → 3.3 V, V_{VDRV} = 2.25 V to 12.75 V.		5		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 3.3 V → 0 V, V_{VDRV} = 12.75 V to 2.25 V.		5		ns

ADVANCE INFORMATION

6.11 Insulation Characteristic Curves

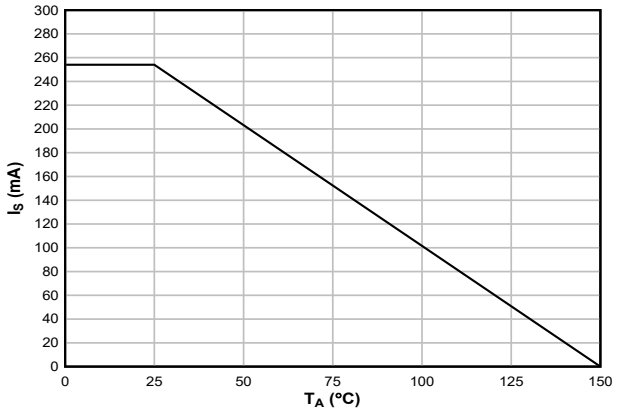


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE and IEC, Three-Wire Mode

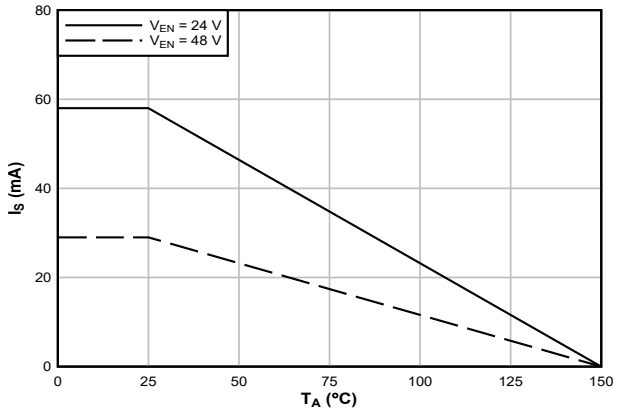


Figure 6-2. Thermal Derating Curve for Limiting Current per VDE and IEC, Two-Wire Mode

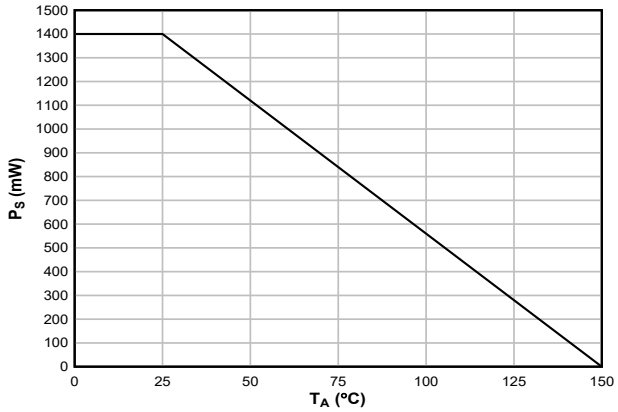
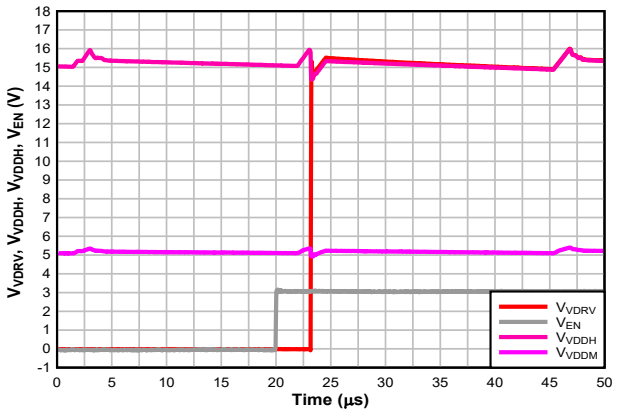


Figure 6-3. Thermal Derating Curve for Limiting Power per VDE and IEC

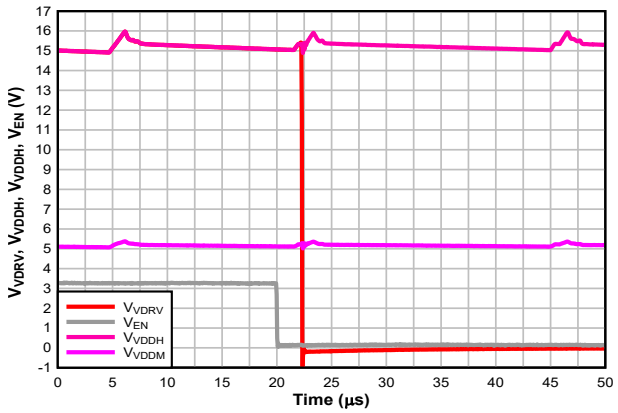
ADVANCE INFORMATION

6.12 Typical Characteristics



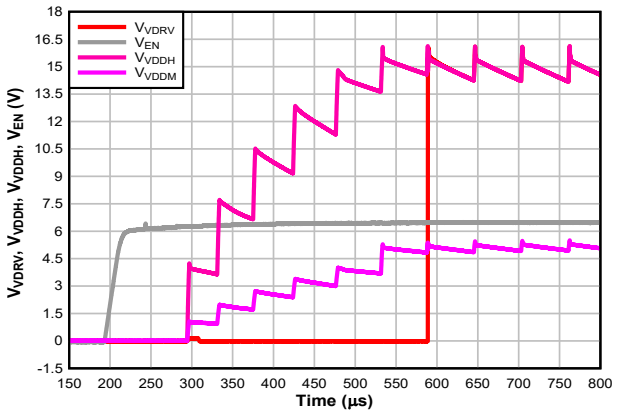
Three-wire mode VDDP = 5.0 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

Figure 6-4. t_{LH_VDRV}, Three-Wire Mode, TPSI3052-Q1



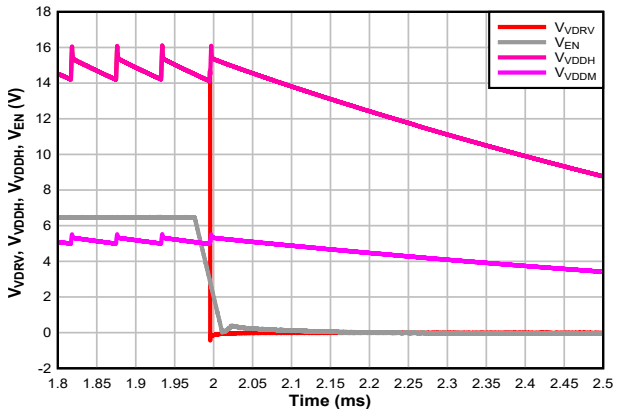
Three-wire mode VDDP = 5.0 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

Figure 6-5. t_{HL_VDRV}, Three-Wire Mode, TPSI3052-Q1



Two-wire mode EN = 6.5 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

Figure 6-6. t_{LH_VDRV}, Two-Wire Mode, TPSI3052-Q1



Two-wire mode EN = 6.5 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

Figure 6-7. t_{HL_VDRV}, Two-Wire Mode, TPSI3052-Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

7 Parameter Measurement Information

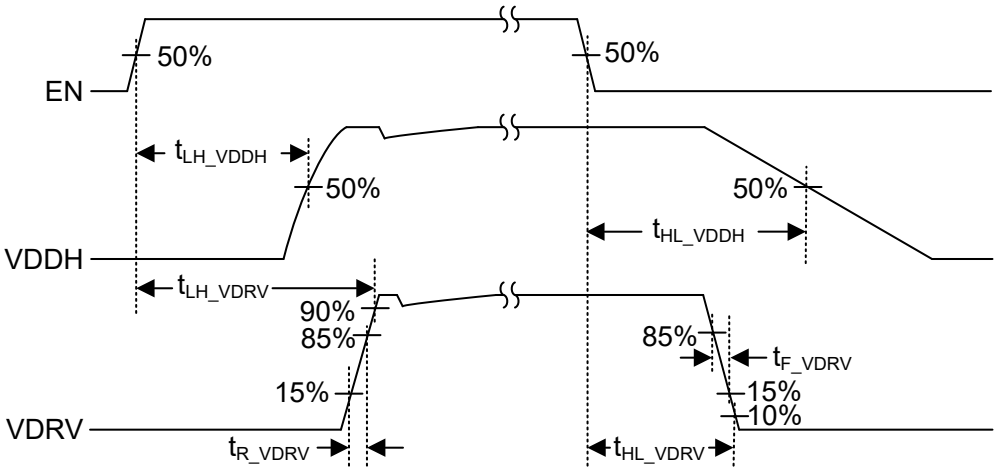


Figure 7-1. Two-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

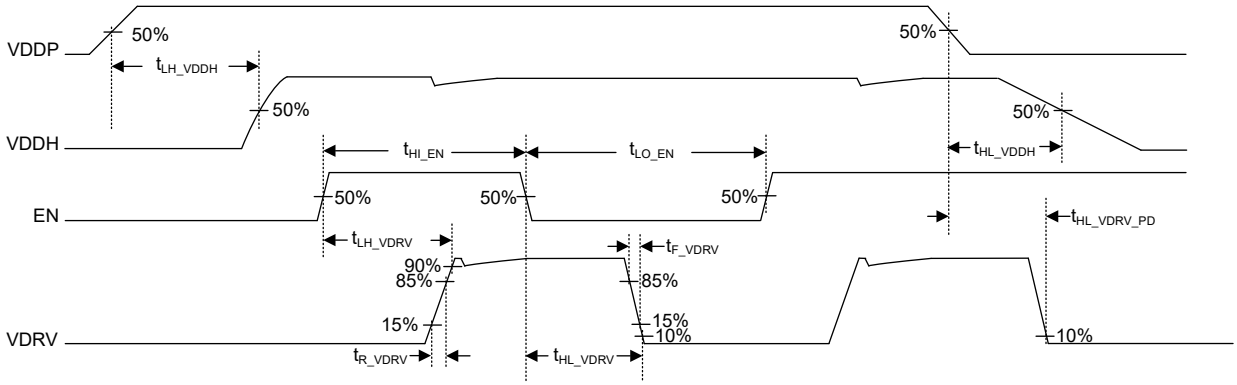


Figure 7-2. Three-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

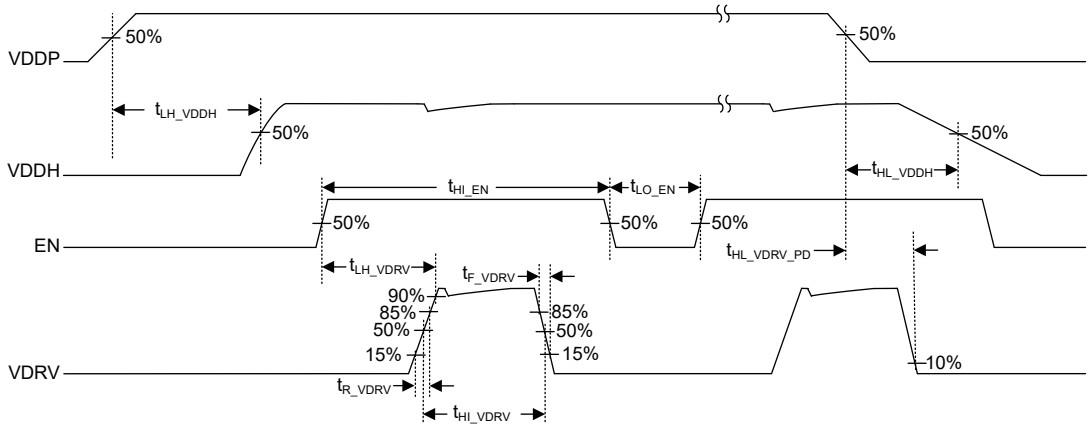


Figure 7-3. Three-Wire Mode Timing, One-Shot Enable (TPSI3052S-Q1 Only)

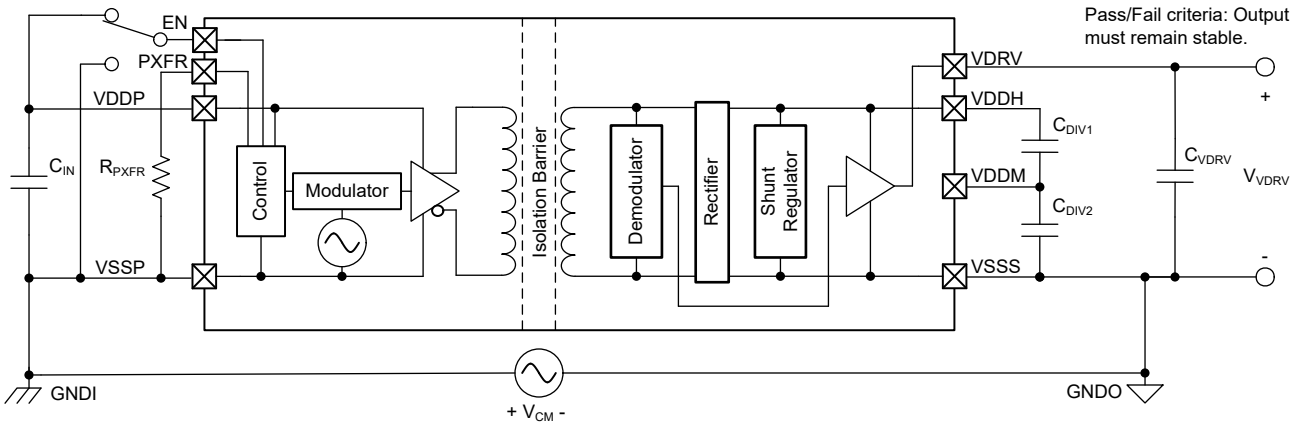


Figure 7-4. Common-Mode Transient Immunity Test Circuit

ADVANCE INFORMATION

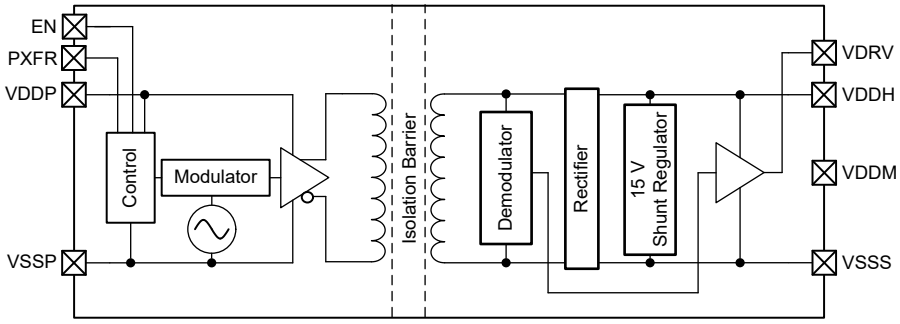
8 Detailed Description

8.1 Overview

The TPSI3052-Q1 is a fully integrated, reinforced isolated power switch driver, which when combined with an external power switch, forms a complete isolated power switch solution. With a nominal gate drive voltage of 15 V and 1.5/3.0-A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary supply from the power received from its primary side, so no isolated secondary bias supply is required.

The *Functional Block Diagram* shows the primary side that includes a transmitter that drives an alternating current into the primary winding of an integrated transformer at a rate determined by the setting of the PXFR pin and the logic state of the EN pin. The transmitter operates at high frequency to optimally drive the transformer to its peak efficiency. In addition, the transmitter uses spread spectrum techniques to greatly improve EMI performance, allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information transfers to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer is rectified, and the shunt regulator regulates the output voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low based on the logic state of the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Transmission of the Enable State

The TPSI3052-Q1 and TPSI3052S-Q1 use a modulation scheme to transmit the switch enable state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier (89-MHz typical), and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low based on the data received.

8.3.2 Power Transmission

The TPSI3052-Q1 and TPSI3052S-Q1 do not use a secondary side bias supply for their power. The secondary side power is obtained by the transferring of the primary side input power across the isolation transformer. The modulation scheme uses spread spectrum of the high frequency carrier (89-MHz typical) to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

8.3.3 Gate Driver

The TPSI3052-Q1 and TPSI3052S-Q1 have an integrated gate driver that provides a nominal 15-V gate voltage with 1.5/3.0-A peak source and sink current sufficient for driving many power transistors or Silicon-Controlled Rectifiers (SCR). When driving external power transistors, TI recommends bypass capacitors (C_{DIV2} = 3 * C_{DIV1}) from VDDH to VDDM and VDDM to VSSS of 20 times the equivalent gate capacitance.

ADVANCE INFORMATION

8.3.4 Modes Overview

The TPSI3052-Q1 and TPSI3052S-Q1 have two modes of operation: two-wire mode and three-wire mode.

In two-wire mode, the power on the primary side is provided directly by the EN pin. Setting EN high causes power transfer to the secondary side. As power transfers, the secondary rails, VDDM and VDDH, begin to rise. After sufficient power is available on the secondary side, VDRV is asserted high. Setting EN low causes VDRV to assert low and stop the power transfer to the secondary side.

In three-wire mode, the power on the primary side is provided by a dedicated, low output impedance supply connected to VDDP. In this case, power transfer is independent from the enable state. If VDDP power is present, power is transferred from the primary side to the secondary side regardless of the EN state. In steady state conditions, when sufficient power is available on the secondary side, setting EN high causes VDRV to assert high. Setting EN low causes VDRV to assert low.

In standard enable, available only on the TPSI3052-Q1, VDRV follows the state of the EN pin and is used in most load switch applications. In one-shot enable mode, available only on the TPSI3052S-Q1 in three-wire mode, when a rising transition occurs on EN, VDRV is asserted high momentarily and then automatically asserted low, forming a one-shot pulse on VDRV. This event is useful for driving SCR devices that require only one burst of power to trigger. To re-trigger VDRV, EN must first transition low, followed by another rising transition.

8.3.5 Three-Wire Mode

Three-wire mode is used for applications that require higher levels of power transfer or the shortest propagation delay TPSI3052-Q1 can offer. VDDP is supplied independently from the EN pin by a low output impedance external supply that can deliver the required power. In this mode, power from the primary side to the secondary side always occurs regardless of the state of the EN pin. Setting the EN pin logic high or low asserts or de-asserts VDRV, thereby enabling or disabling the external switch, respectively. Figure 8-1 shows the basic setup required for three-wire mode operation which requires EN, VDDP, and VSSP signals. EN can be driven up to 5.5 V which is normally driven from the circuitry residing on the same rail as VDDP. In this example, the TPSI3052-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. C_{IN} provides the required decoupling capacitance for the VDDP supply rail of the device. C_{DIV1} and C_{DIV2} provide the required decoupling capacitances of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

Figure 8-2 and Figure 8-3 show the basic operation from startup to steady state conditions. Figure 8-2 shows operation using standard enable of the TPSI3052-Q1. After power up, the TPSI3052-Q1 begins to transfer power from VDDP to the secondary side for a fixed time period (25-µs typical) at a duty cycle rate determined by R_{PXFR}, which begins to charge up the VDDH (and VDDM) secondary side rails. Power transfer continues as long as VDDP is present. The time required to fully charge VDDH depends on several factors including the values of VDDP, C_{DIV1}, C_{DIV2}, R_{PXFR}, and the overall power transfer efficiency. When the application drives the EN pin to a logic high, the TPSI3052-Q1 signals information from the primary side to the secondary side to assert VDRV and drive it high. Similarly, setting EN pin to a logic low causes VDRV to be driven low. Figure 8-3 shows operation using one-shot enable of the TPSI3052S-Q1. The start-up behavior is identical. In one-shot enable, when the application drives the EN pin to a logic high, VDRV is asserted high (t_{HI_VDRV}), then is automatically asserted low by the TPSI3052S-Q1. To assert VDRV high again, the EN pin must transition low first, followed by a transition high.

ADVANCE INFORMATION

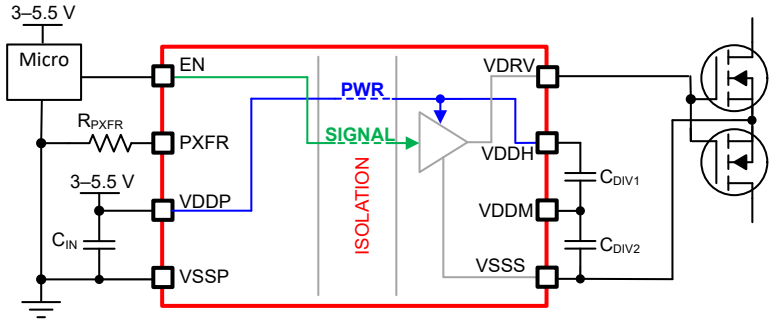


Figure 8-1. Three-Wire Mode Simplified Schematic

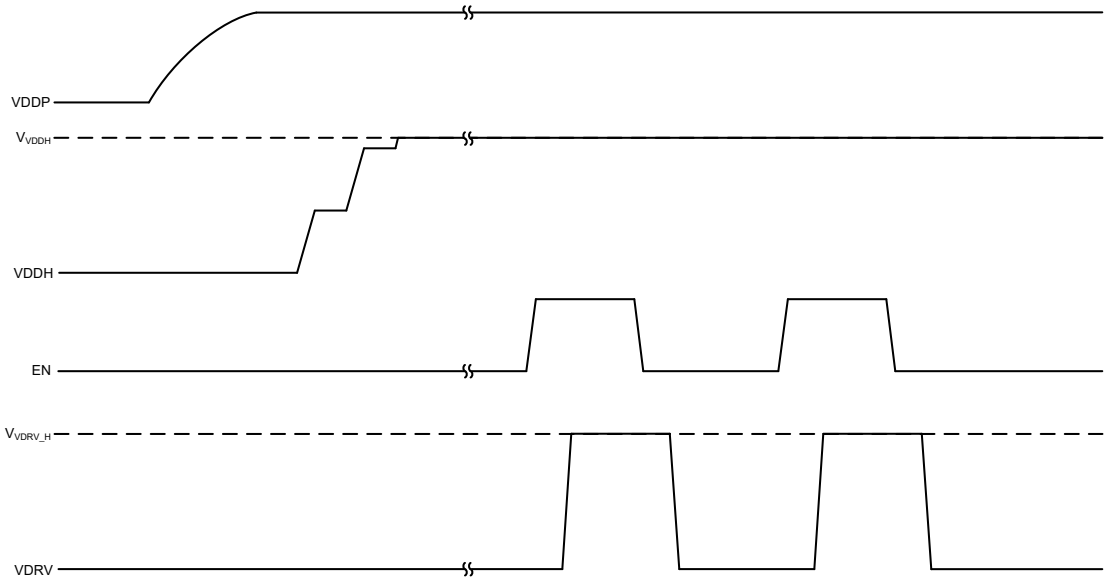


Figure 8-2. Three-Wire Mode with TPSI3052-Q1 (Standard Enable)

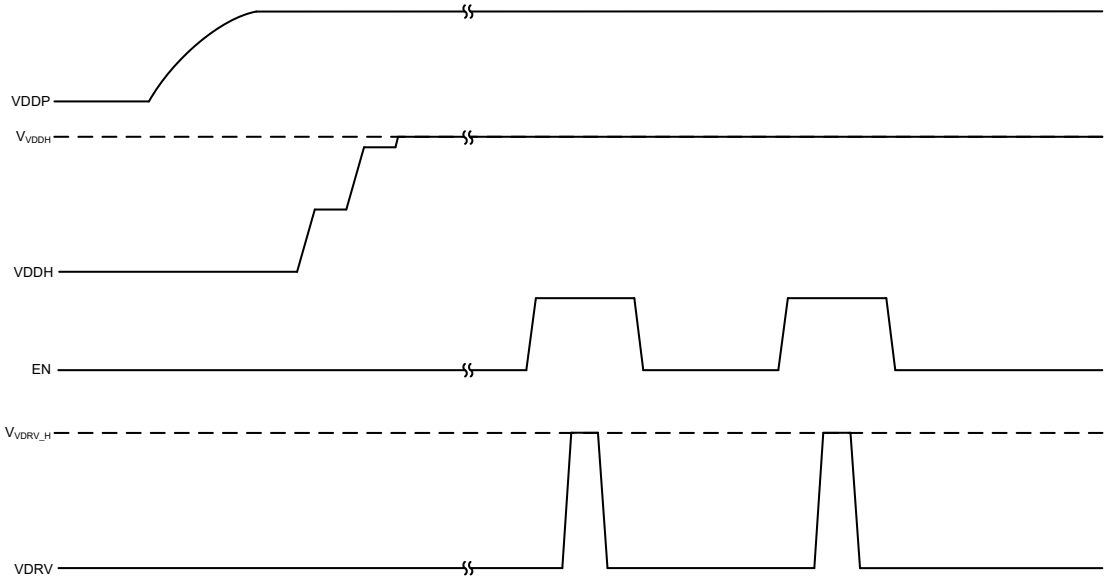


Figure 8-3. Three-Wire Mode with TPSI3052S-Q1 (One-shot Enable)

To reduce average power, the TPSI3052-Q1 transfers power from the primary side to the secondary side in a burst fashion. The period of the burst is fixed while the burst on time is programmable by selecting one of

ADVANCE INFORMATION

seven appropriate resistor values, R_{PXFR}, from the PXFR to VSSP pins, thereby changing the duty cycle of the power converter. This action provides flexibility in the application, allowing tradeoffs in power consumed versus power delivered. Higher power converter settings increase the burst on time which, in turn, increases average power consumed from the VDDP supply and increases the amount of power transferred to the secondary side VDDH and VDDM supplies. Similarly, lower power converter settings decrease the burst on time which, in turn, decreases average power consumed from the VDDP supply and decreases the amount of power transferred to the secondary side.

Table 8-1 summarizes the three-wire mode power transfer selection.

Table 8-1. Three-Wire Mode Power Transfer Selection

R_{PXFR} (1) (2)	Power Converter Duty Cycle (Three-Wire Mode, Nominal)	Description
7.32 kΩ	13.3%	The device supports seven, fixed power transfer settings, by selection of a corresponding R_{PXFR} value . Selecting a given power transfer setting adjusts the duty cycle of the power converter and hence the amount of power transferred. Higher power transfer settings leads to an increased duty cycle of the power converter leading to increased power transfer and consumption. During power up, the power transfer setting is determined and remains fixed at that setting until VDDP power cycles.
9.09 kΩ	26.7%	
11 kΩ	40.0%	
12.7 kΩ	53.3%	
14.7 kΩ	66.7%	
16.5 kΩ	80.0%	
20 kΩ	93.3%	

(1) Standard resistor (EIA E96), 1% tolerance, nominal value.
(2) $R_{PXFR} \geq 100$ kΩ or $R_{PXFR} \leq 1$ kΩ sets the duty cycle of the power converter to 13.3%.

8.3.6 Two-Wire Mode

Figure 8-4 shows the basic setup required for two-wire mode operation, which requires the EN signal and VSSP ground signal. EN can be driven up to 48 V. No current limiting resistor is required on EN because the TPSI3052-Q1 limits the input current based on the values set by the R_{PXFR} resistor (see Table 8-2). In this example, the TPSI3052-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. C_{IN} provides the required decoupling capacitance for the VDDP supply rail of the device. C_{DIV1} and C_{DIV2} provide the required decoupling capacitance of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

Figure 8-5 shows the typical operation in two-wire mode configured for standard enable. The application drives EN to a logic high and the TPSI3052-Q1 begins its power-up sequence. During power up, the current provided by the EN pin, I_{EN}, begins to charge up the external capacitance, C_{IN}, and the voltage on VDDP begins to rise until it reaches V_{VDDP_H}. After VDDP reaches V_{VDDP_H}, the TPSI3052-Q1 transfers stored energy on C_{IN} to the secondary side for a fixed time (3.3-µs typical) which begins to charge up the VDDH (and VDDM) secondary side rails thereby discharging the voltage on VDDP. This cycle repeats until the VDDH (and VDDM) secondary side rails are fully charged. The time required to fully charge VDDH depends on several factors including the values of C_{IN}, C_{DIV1}, C_{DIV2}, R_{PXFR}, and the overall power transfer efficiency. After VDDH is fully charged, VDRV is asserted high and remains high while the EN pin remains at a logic high. When the application drives the EN pin to a logic low, the charge on VDDP begins to discharge. Prior to VDDP reaching its UVLO falling threshold, TPSI3052-Q1 signals information from the primary side to the secondary side to de-assert VDRV and drive it low. Because power is no longer being transferred, all rails begin to fully discharge.

ADVANCE INFORMATION

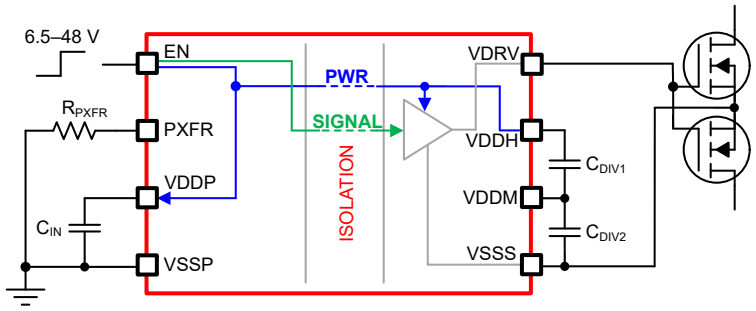


Figure 8-4. Two-Wire Mode Simplified Schematic

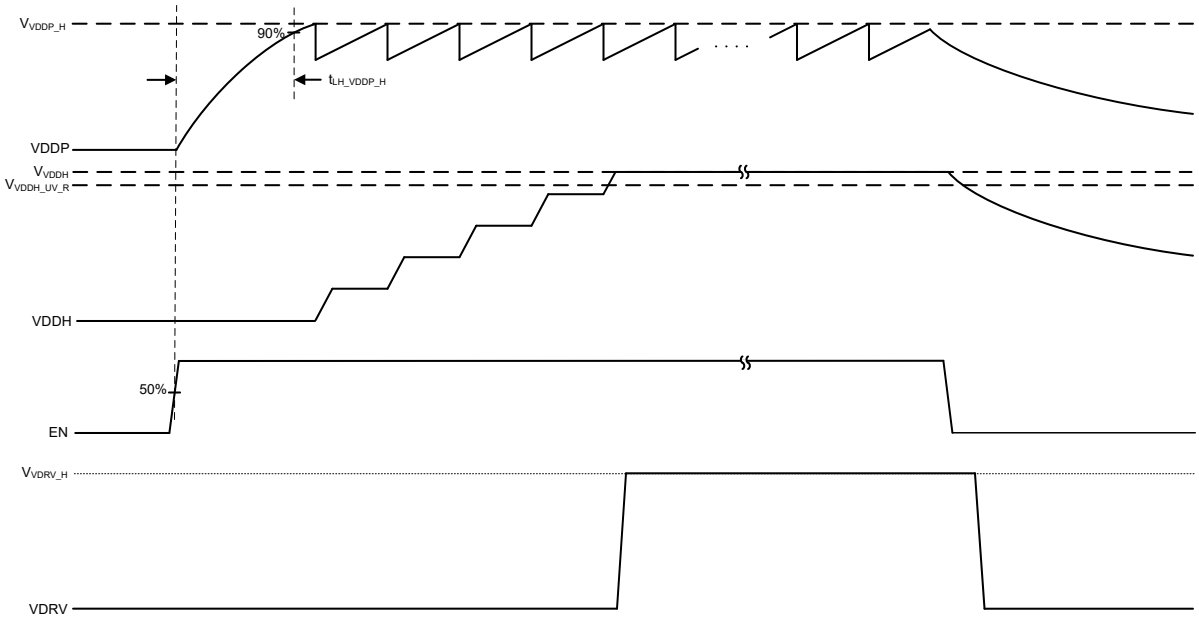


Figure 8-5. Two-Wire Mode with Standard Enable (TPSI3052-Q1 Only)

In two-wire mode, power is supplied directly by the EN pin. When EN is asserted high, the TPSI3052-Q1 transfers power to the secondary side for a fixed time (3.3-µs nominal) while the time period varies. The period varies due to the hysteretic control of the power transfer that ensures the average current supplied through the EN pin is maintained. The amount of average current, and hence the amount of power transferred, is programmable by selecting one of seven appropriate resistor values, R_{PXFR}, from the PXFR to VSSP pins. Higher settings of R_{PXFR} increase I_{EN} which increases the average power consumed from the EN pin and increases the amount of power transferred to the secondary side VDDH supply. Similarly, lower settings of R_{PXFR} decrease I_{EN}, which decreases the average power consumed from the EN pin and decreases the amount of power transferred to the secondary side.

Table 8-2 summarizes the two-wire mode power selection.

ADVANCE INFORMATION

Table 8-2. Two-Wire Mode Power Selection

R_{PXFR} (1) (2)	I_{EN} (Two-Wire Mode, Nominal)	Description
7.32 kΩ	1.9 mA	The device supports seven, fixed EN input current limit options selected by the corresponding R_{PXFR} specified value. Higher current limit selections lead to increased power transfer and consumption. During power up, the EN input current limit is determined and remains fixed at that setting until VDDP power cycles.
9.09 kΩ	2.8 mA	
11 kΩ	3.7 mA	
12.7 kΩ	4.5 mA	
14.7 kΩ	5.2 mA	
16.5 kΩ	6.0 mA	
20 kΩ	6.7 mA	

(1) Standard resistor (EIA E96), 1% tolerance, nominal value.
(2) $R_{PXFR} \geq 100$ kΩ or $R_{PXFR} \leq 1$ kΩ sets the I_{EN} to 1.9 mA.

8.3.7 VDDP and VDDH Undervoltage Lockout (UVLO)

TPSI3052-Q1 and TPSI3052S-Q1 implement an internal UVLO protection feature for both input and output power supplies, VDDP and VDDH. When either supply voltage is lower than the threshold voltage, the driver output, VDRV, is held low. VDRV only goes high when both VDDP and VDDH are out of the UVLO status. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn-on and turn-off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH power supply. The internal UVLO protection block ignores the associated noise during these normal switching transients.

8.3.8 Thermal Shutdown

The device contains an integrated temperature sensor to monitor its local temperature. When the sensor reaches its threshold, it automatically ceases power transfer from the primary side to the secondary side. In addition, if power is still present on VDDP, the driver is automatically asserted low. The power transfer is disabled until the local temperature reduces enough to re-engage.

ADVANCE INFORMATION

8.4 Device Functional Modes

Table 8-3 summarizes the functional modes for the TPSI3052-Q1 and TPSI3052S-Q1.

Table 8-3. TPSI3052-Q1, TPSI3052S-Q1 Device Functional Modes(1)

VDDP	VDDH	EN	VDRV	COMMENTS
Powered up(2)	Powered up(4)	L	L	Normal operation (TPSI3052-Q1 only): VDRV output state assumes logic state of EN logic state.
		H	H	
		L	L	Normal operation (TPSI3052S-Q1, three-wire mode only): rising edge of EN causes VDRV to be singly pulsed high. EN must be asserted low first to assert another pulse.
		L → H	L → H → L	
Powered down(3)	Powered down(5)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered up(2)	Powered down(5)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered down(3)	Powered up(4)	X	L	Disabled operation: when VDDP is powered down, output driver is disabled automatically after timeout, keep off circuitry applied.

(1) X: do not care.
(2) V_{VDDP} ≥ VDDP undervoltage lockout rising threshold, $V_{VDDP\_UV\_R}$.
(3) V_{VDDP} < VDDP undervoltage lockout falling threshold, $V_{VDDP\_UV\_F}$.
(4) V_{VDDH} ≥ VDDH undervoltage lockout rising threshold, $V_{VDDH\_UV\_R}$.
(5) V_{VDDH} < VDDH undervoltage lockout falling threshold, $V_{VDDH\_UV\_F}$.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSI3052-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a nominal gate drive voltage of 15 V with 1.5/3.0-A peak source and sink current, a large variety of external power switches such as MOSFETs, IGBTs, or SCRs can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The TPSI3052-Q1 supports two modes of operation based on the number of input pins required. In two-wire mode, typically found in driving mechanical relays, controlling the switch requires only two pins and supports a wide voltage range of operation of 6.5 V to 48 V. In three-wire mode, the primary supply of 3 V to 5.5 V is supplied externally, and the switch is controlled through a separate enable. Available in three-wire mode only, the TPSI3052S-Q1 features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

The secondary side provides a regulated, floating supply rail of 15 V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI3052-Q1 can support driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI3052-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The power dissipation of the TPSI3052-Q1 can be adjusted by an external resistor from the PXFR pin to VSSP. This feature allows for tradeoffs in power dissipation versus power provided on the secondary depending on the needs of the application.

9.2 Typical Application

The circuits in Figure 9-1 and Figure 9-2 show a typical application for driving silicon based MOSFETs in three-wire mode and two-wire mode, respectively.

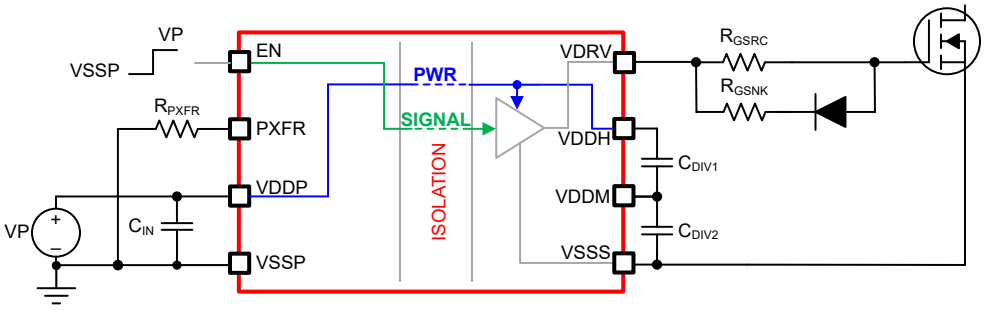


Figure 9-1. TPSI3052-Q1 Three-Wire Mode Driving MOSFETs

ADVANCE INFORMATION

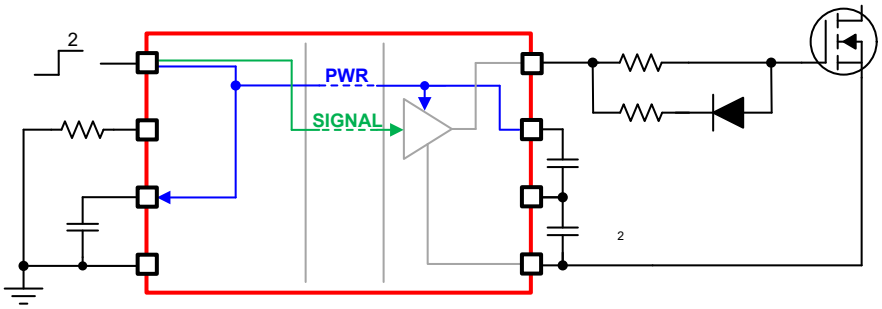


Figure 9-2. TPSI3052-Q1 Two-Wire Mode Driving MOSFETs

9.2.1 Design Requirements

Table 9-1 lists the design requirements of the TPSI3052-Q1 gate driver.

Table 9-1. TPSI3052-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	120 nC
FET turn-on time	1 µs
Propagation delay	< 4 µs
Switching frequency	10 kHz
Supply voltage (VDDP)	5 V ±5%

9.2.2 Detailed Design Procedure

9.2.2.1 Two-Wire or Three-Wire Mode Selection

The first design decision is to determine if two-wire or three-wire mode can be used in the application. For this design, note that the overall propagation delay is less than 4 µs and only three-wire mode is able to meet this requirement. In this case, two-wire mode is not applicable. Two-wire mode, due to its limited power transfer, is typically limited to very low frequency applications of less than a few kHz or when enable times are not critical.

9.2.2.2 Standard Enable, One-Shot Enable

Next, based on the application a decision must be if standard enable or one-shot enable mode is required. In this design, assume that after the switch is enabled, it is desired that the switch remain enabled until commanded to be disabled. Therefore, standard enable mode is assumed. In most applications that involve driving FETs, standard enable is appropriate. If driving SCRs or TRIACS, one-shot mode can be beneficial.

9.2.2.3 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitances required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the CDIV1 and CDIV2 capacitances is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of C_{DIV1} and C_{DIV2} be sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5-V drop of the VDDH supply rail that is used to supply power to the VDRV signal. Equation 1 and Equation 2 can be to used to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (1)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (2)$$

where

- n is a real number greater than or equal to 3.0.

ADVANCE INFORMATION

- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

Note

C_{DIV1} and C_{DIV2} represent absolute capacitances and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitances.

Larger values of ΔV can be used in the application, but excessive droop can cause the VDDH undervoltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitances increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming n = 3 and ΔV = 0.5 V, then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120\,nC}{0.5\,V} = 320\,nF \quad (3)$$

$$C_{DIV2} = 3 \times 320\,nF = 960\,nF \quad (4)$$

9.2.2.4 R_{PXFR} Selection

The selection of R_{PXFR} allows for a tradeoff between power consumed and power delivered, as described in the *Three-wire Mode* section. For this design, one must choose an appropriate R_{PXFR} selection that ensures enough power is transferred to support the amount of load being driven at the specified switching frequency.

During switching of the load, Q_{LOAD} of charge on VDDH is transferred to the load and VDDH supply voltage droops. After each switching cycle, this charge must be replenished before the next switching cycle occurs. This action ensures that the charge residing on VDDH does not deplete over time due to subsequent switching cycles of the load. The time it takes to recover this charge, $t_{RECOVER}$, can be estimated as follows:

$$t_{RECOVER} = \frac{1}{f_{MAX}} \cong \frac{Q_{LOAD}}{I_{OUT}} \quad (5)$$

where

- Q_{LOAD} is the load charge in Coulombs ©.
- I_{OUT} is the average current available from VDDH supply in Amperes (A).
- f_{MAX} is maximum switching frequency in Hertz (Hz).

For this design, Q_{LOAD} = 120 nC and f_{MAX} = 10 kHz are known, so I_{OUT} required can be estimated as

$$I_{OUT} \cong 120\,nC \times 10\,kHz = 1.2\,mA \quad (6)$$

I_{OUT} represents the minimum average current required to meet the design requirements. Using the TPSI3052-Q1 calculator tool, one can easily find the R_{PXFR} necessary by referring to the I_{OUT} or f_{MAX} columns directly. Table 9-2 shows the results from the tool, assuming VDDP = 4.75 V, to account for the supply tolerance specified in the design requirements. The TPSI3052-Q1 Calculator tool can be found at Table 12-1.

Table 9-2. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
7.32	13.3	4.13	19.3	5.6	0.37	0.37	6045	325.9	3.1
9.09	21.1	7.39	34.7	10.5	0.69	0.69	3241	173.3	5.8
11	40.0	15.29	72.3	23.0	1.52	1.52	1506	78.9	12.7
12.7	53.3	20.85	98.7	31.6	2.09	2.09	1112	57.4	17.4
14.7	66.7	26.45	125.3	40.2	2.66	2.66	885	45.1	22.2

ADVANCE INFORMATION

Table 9-2. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode (continued)

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
16.5	80.0	32.00	151.7	49.4	3.27	3.27	732	36.7	27.2
20	93.3	37.56	178.1	58.0	3.84	3.84	631	31.2	32.0

Table 9-3 summarizes the various output parameters of the calculator tool.

Table 9-3. TPSI3052-Q1 Calculator Tool Parameter Descriptions

Parameter	Description
R_{PXFR}	External resistor setting that controls the amount of power transferred to the load by adjusting the duty cycle. Higher R_{PXFR} settings lead to increased power transfer and power consumption.
Power Converter Duty Cycle	Nominal duty cycle of the power converter. Higher R_{PXFR} settings leads to higher duty cycles of the power converter and higher power transfer.
I_{VDDP}	Average current consumed from the VDDP supply
P_{IN}	Average power consumed from the VDDP supply
P_{OUT}	Average power delivered to the VDDH supply
I_{OUT}	Average current delivered to the VDDH supply
I_{OUT_CHG}	Average current available to charge the load present on VDDH. If no auxiliary current is being supplied from VDDM, then I_{OUT_CHG} equals I_{OUT}.
t_{START}	Start-up time from VDDP rising until VDDH supply rail is fully charged. This parameter assumes VDDH and VDDM supply rails are fully discharged initially.
$t_{RECOVER}$	Represents the time for the VDDH rail to recover after switching the load present on VDRV
f_{MAX}	Maximum switching frequency possible for a given R_{PXFR} setting for the applied loading conditions

For this design example, R_{PXFR} must be configured to the 9.09-kΩ setting or higher to transfer enough power to support switching the specified load at the required 10-kHz frequency.

9.2.2.5 C_{IN} Capacitance

For two-wire mode, the recommended capacitance C_{IN} from VDDP to VSSP is 220 nF.

For this design, three-wire mode is required to meet the design requirements. For three-wire mode, increasing the amount of capacitance, C_{IN}, improves the ripple on the VDDP supply. For this design, 1 µF in parallel with 100 nF is used.

9.2.2.6 Gate Driver Output Resistor

The optional external gate driver resistors, R_{GSRC} and R_{GSNK}, along with the diode are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage switching dv/dt, high current switching di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength for sourcing and sinking
4. Reduce electromagnetic interference (EMI)

The TPSI3052-Q1 has a pullup structure with a P-channel MOSFET with a peak source current of 1.5 A. Therefore, the peak source current can be predicted with:

$$I_{O+} \cong min\left(1.5\ A,\ \frac{V_{VDDH}}{R_{DSON\_VDRV} + R_{GSRC} + R_{GFET\_INT}}\right) \quad (7)$$

where

- R_{GSRC}: external turn-on resistance.
- R_{DSON_VDRV}: TPSI3052-Q1 driver on resistance in high state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1 V in this example.

- R_{GFET_INT}: external power transistor internal gate resistance, found in the power transistor data sheet. Assume 0 Ω for this example.
- I_{O+}: peak source current. The minimum value between 1.5 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

For this example, R_{DSON_VDRV} = 5.2 Ω, R_{GSRC} = 5.8 Ω, and R_{GFET_INT} = 0 Ω results in:

$$I_{O+} \cong min\left(1.5\ A, \frac{15.1\ V}{5.2\ \Omega + 5.8\ \Omega + 0\ \Omega}\right) = 1.37\ A \quad (8)$$

Similarly, the TPSI3052-Q1 has a pulldown structure with an N-channel MOSFET with a peak sink current of 3.0 A. Therefore, assuming R_{GFET_INT} = 0 Ω, the peak sink current can be predicted with:

$$I_{O-} \cong min\left[3.0\ A, (V_{VDDH} \times (R_{GSRC} + R_{GSNK}) - R_{GSRC} \times V_F) \times \frac{1}{R_{GSRC} \times R_{GSNK} + R_{DSON\_VDRV} \times (R_{GSRC} + R_{GSNK})}\right] \quad (9)$$

where

- R_{GSRC}: external turn-on resistance.
- R_{GSNK}: external turn-off resistance.
- R_{DSON_VDRV}: TPSI3052-Q1 driver on resistance in low state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1 V in this example.
- V_F: diode forward voltage drop. Assumed 0.7 V in this example.
- I_{O-}: peak sink current. The minimum value between 3.0 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

For this example, assuming R_{DSON_VDRV} = 2.5 Ω, R_{GSRC} = 5.8Ω, R_{GSNK} = 5.0 Ω, and R_{GFET_INT} = 0 Ω, results in:

$$I_{O-} \cong min\left[3.0\ A, (15.1\ V \times (5.8\ \Omega + 5.0\ \Omega) - 5.8\Omega \times 0.7\ V) \times \frac{1}{5.8\ \Omega \times 5.0\ \Omega + 2.5\ \Omega \times (5.8\Omega + 5.0\ \Omega)}\right] = 2.84\ A \quad (10)$$

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends to minimize the gate driver loop.

9.2.2.7 Start-up Time and Recovery Time

As described in the *C_{DIV1}, C_{DIV2} Capacitance* section, the start-up time of the fully discharged VDDH rail depends on the amount of capacitance present on the VDDH supply. The rate at which this capacitance is charged depends on the amount of power transferred from the primary side to the secondary side. The amount of power transferred can be adjusted by choosing R_{PXFR}. Increasing the resistor settings for R_{PXFR} transfers more power from the primary supply (VDDP) to the secondary supply (VDDH), thereby reducing the overall start-up and recovery times.

9.2.2.8 Supplying Auxiliary Current, I_{AUX} From VDDM

The TPSI3052-Q1 is capable of providing power from VDDM to support external auxiliary circuitry as shown in Figure 9-3. In this case, the required transfer power must include the additional power consumed by the auxiliary circuitry on the VDDM rail. The R_{PXFR} value must be set to meet the overall power requirements.

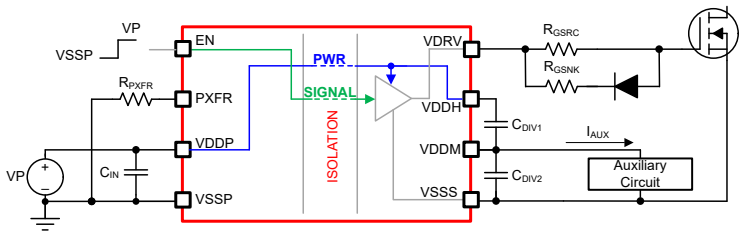


Figure 9-3. Supplying Auxiliary Power From VDDM

As an example, assume that the auxiliary circuitry requires an average current of 4 mA. Table 9-4 summarizes the results from the TPSI3052-Q1 calculator tool. The Calculator tool can be found at Table 12-1.

Table 9-4. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode with I_{AUX} = 4 mA

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
7.32	13.3	4.13	19.3	5.6	0.37	N/A	N/A	N/A	N/A
9.09	21.1	7.39	34.7	10.5	0.69	N/A	N/A	N/A	N/A
11	40.0	15.29	72.3	23.0	1.52	0.17	12976	703.1	1.4
12.7	53.3	20.85	98.7	31.6	2.09	0.74	3039	162.3	6.2
14.7	66.7	26.45	125.3	40.2	2.66	1.31	1737	91.4	10.9
16.5	80.0	32.00	151.7	49.4	3.27	1.92	1207	62.6	16.0
20	93.3	37.56	178.1	58.0	3.84	2.49	942	48.2	20.8

Based on the results in Table 9-4, several observations can be made:

- With R_{PXFR} = 7.32 kΩ and R_{PXFR} = 9.09 kΩ, insufficient power is available to meet the application power needs .
- With R_{PXFR} = 11 kΩ, sufficient power is transferred, but f_{MAX} is lower than the 10 kHz specified in the design requirements in Table 9-1.
- With R_{PXFR} = 12.7 kΩ and higher, sufficient power is transferred to meet the specified design requirements.
- For a given R_{PXFR}, because some of the transferred power is being provided to the auxiliary circuitry, t_{START} can be significantly longer, and f_{MAX} reduced when compared to the results shown in Table 9-2 with I_{AUX} = 0 mA.

9.2.2.9 VDDM Ripple Voltage

Note that when supplying power from VDDM, that is when I_{AUX} > 0 mA, additional voltage ripple is present on the VDDM rail. For a given R_{PXFR} setting, this ripple can be reduced by applying additional capacitance from VDDM to VSSS. For this design example, the ripple on VDDM, $VDDM_{ripple}$, computed in the calculator tool is 63 mV.

It is possible to reduce the $VDDM_{ripple}$ with the addition of capacitance while still maintaining the original $VDDH_{droop}$ = 0.5V. For example, applying C_{DIV1} = 300 nF and C_{DIV2} = 1200 nF in the calculator tool, reduces $VDDM_{ripple}$ to 50 mV, while still maintaining $VDDH_{droop}$ = 0.5 V. This additional capacitance leads to increased t_{START} times.

10 Power Supply Recommendations

In three-wire mode, to help ensure a reliable supply voltage, TI recommends that the C_{IN} capacitance from VDDP to VSSP consists of a 0.1-µF bypass capacitor for high frequency decoupling in parallel with a 1 µF for low frequency decoupling.

In two-wire mode, TI recommends that the C_{IN} capacitance placed from VDDP to VSSP consists of a 220-nF capacitor connected close to the device between the VDDP and VSSP pins. The recommended absolute capacitance must be 220 nF, so if derating is required, a higher component value can be needed.

Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

11 Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI3052-Q1. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.

ADVANCE INFORMATION

  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitances on the R_{PXFR} pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

ADVANCE INFORMATION

11.2 Layout Example

Figure 11-1 shows a PCB layout example with the signals and key components labeled.

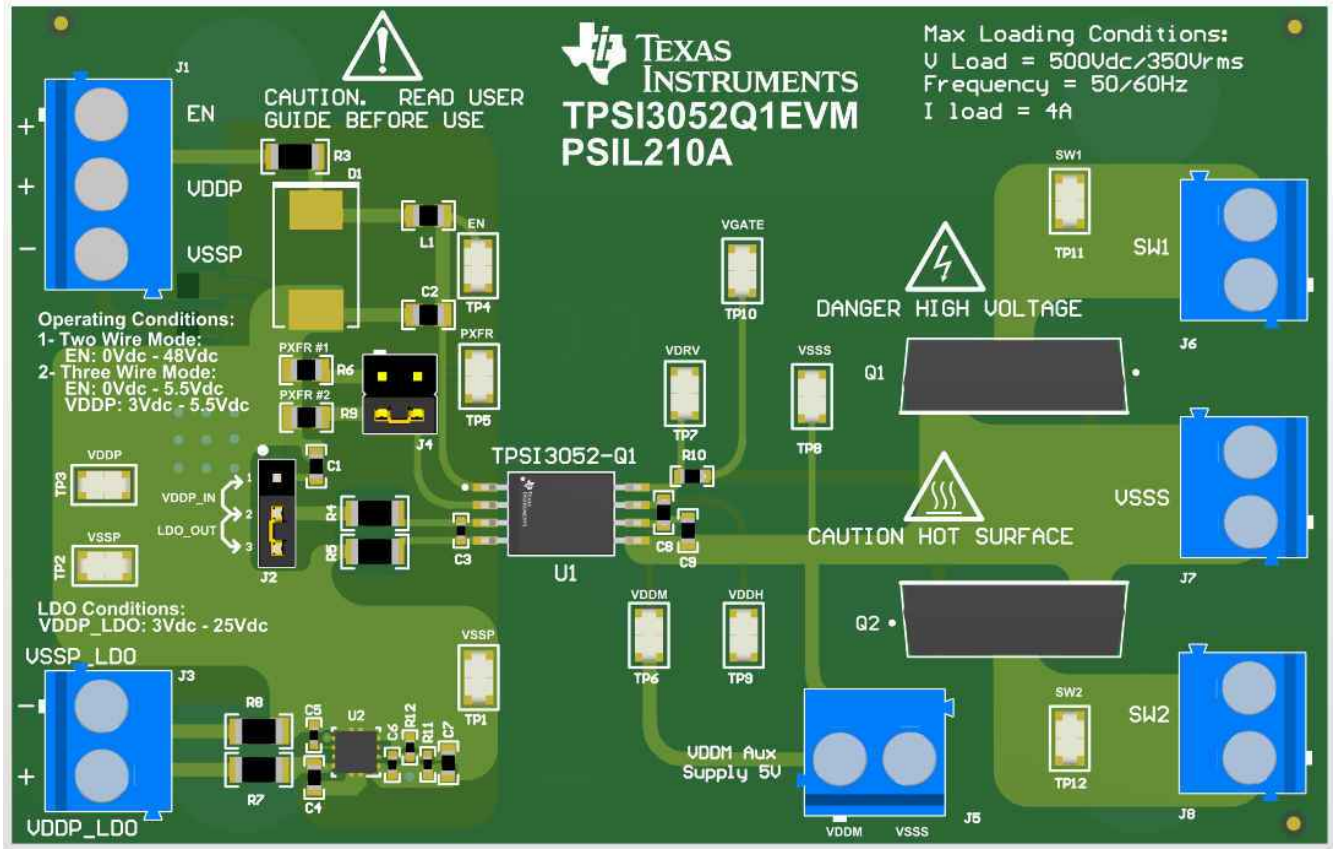


Figure 11-1. 3-D PCB View

Figure 11-2 and Figure 11-3 show the top and bottom layer traces and copper.

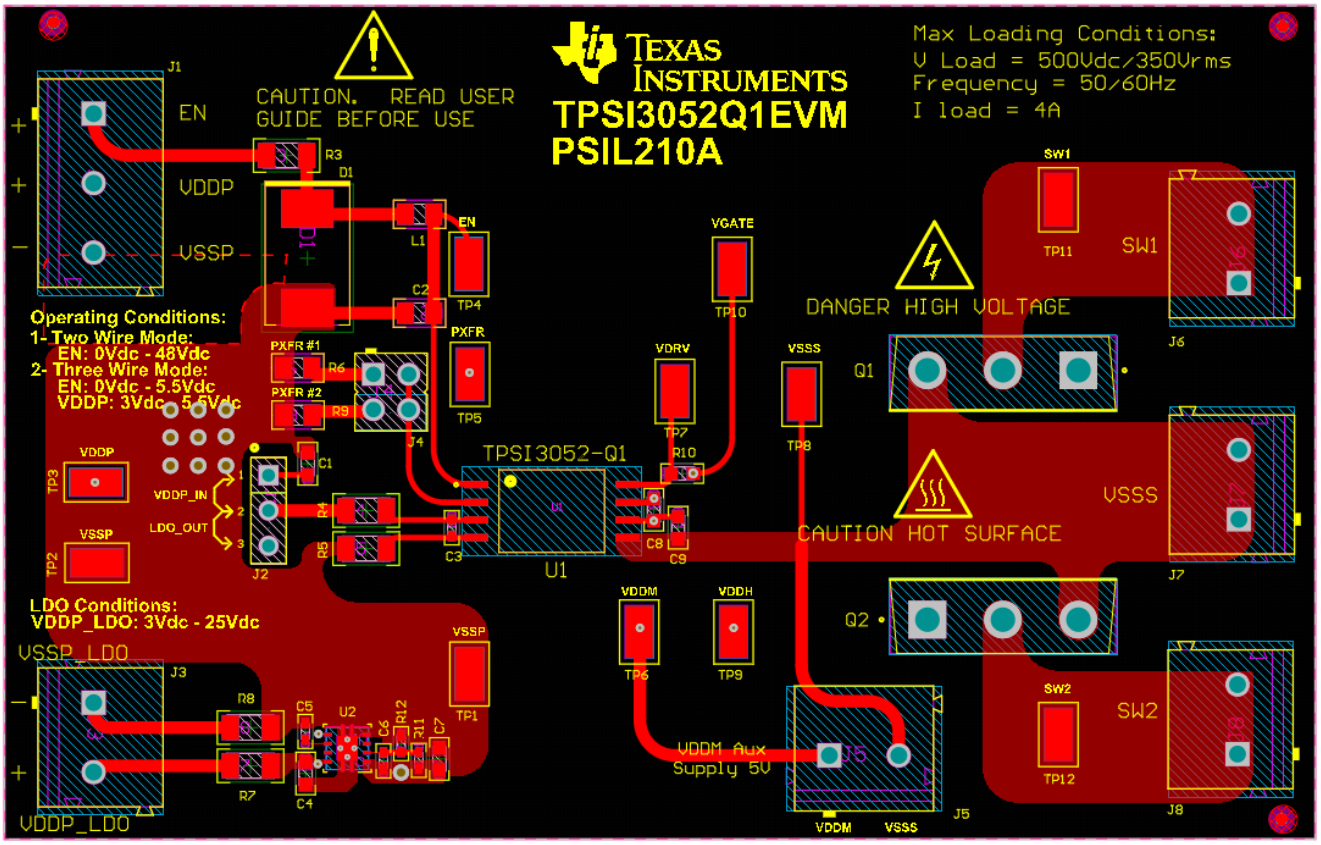


Figure 11-2. Top Layer

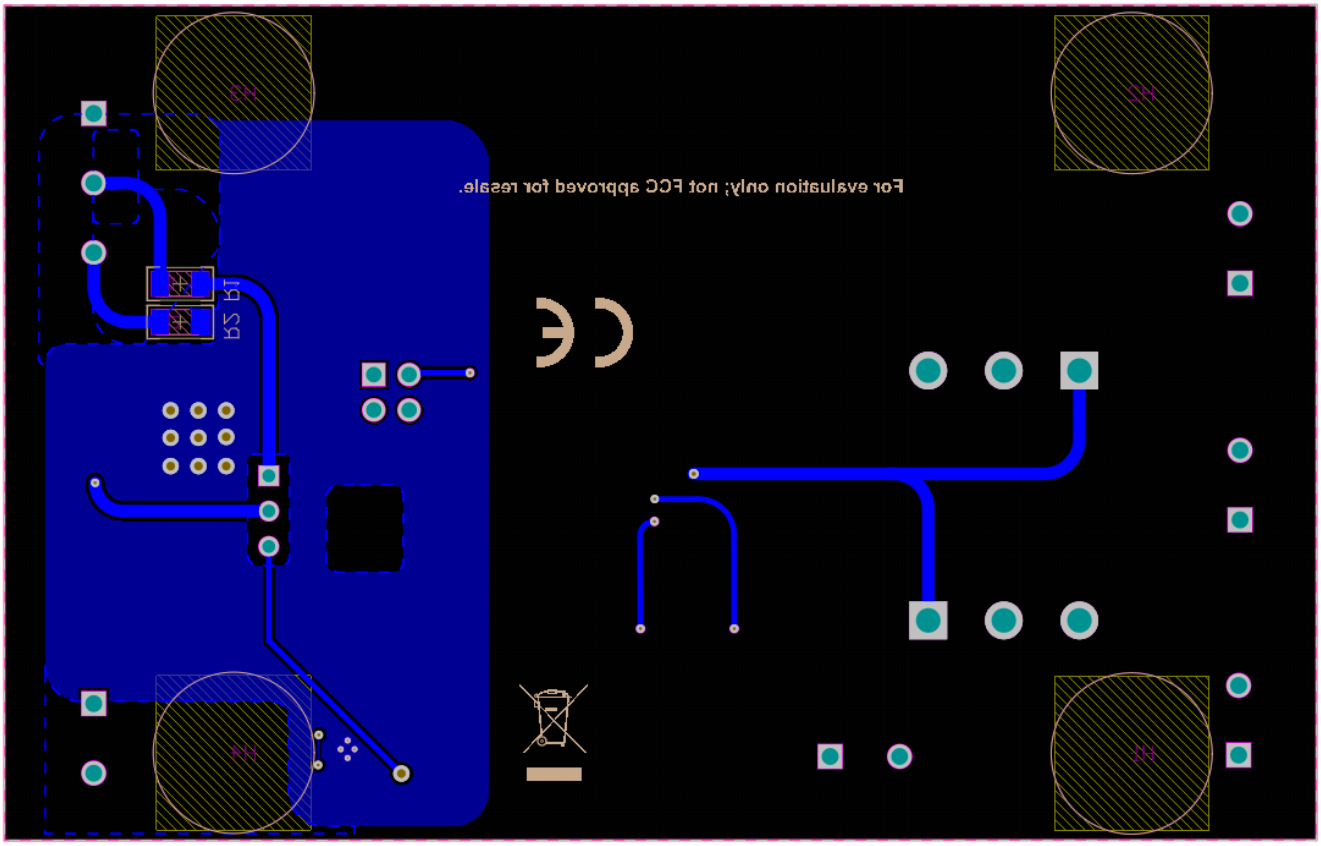


Figure 11-3. Bottom Layer

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPSI3052-Q1	Click here	Click here	Click here	Click here	Click here
TPSI3052S-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

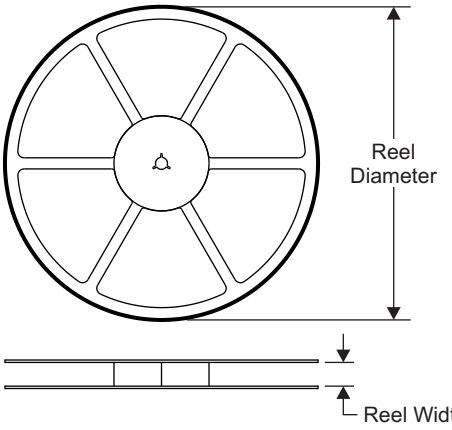
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

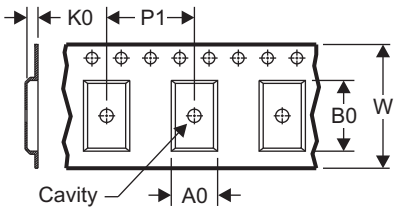
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

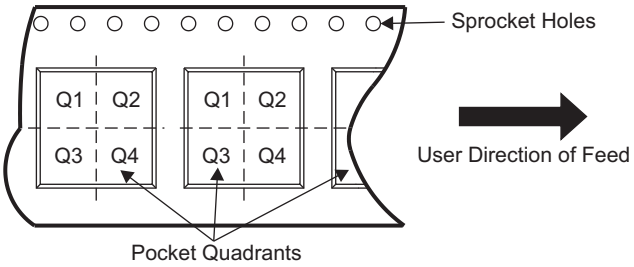


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

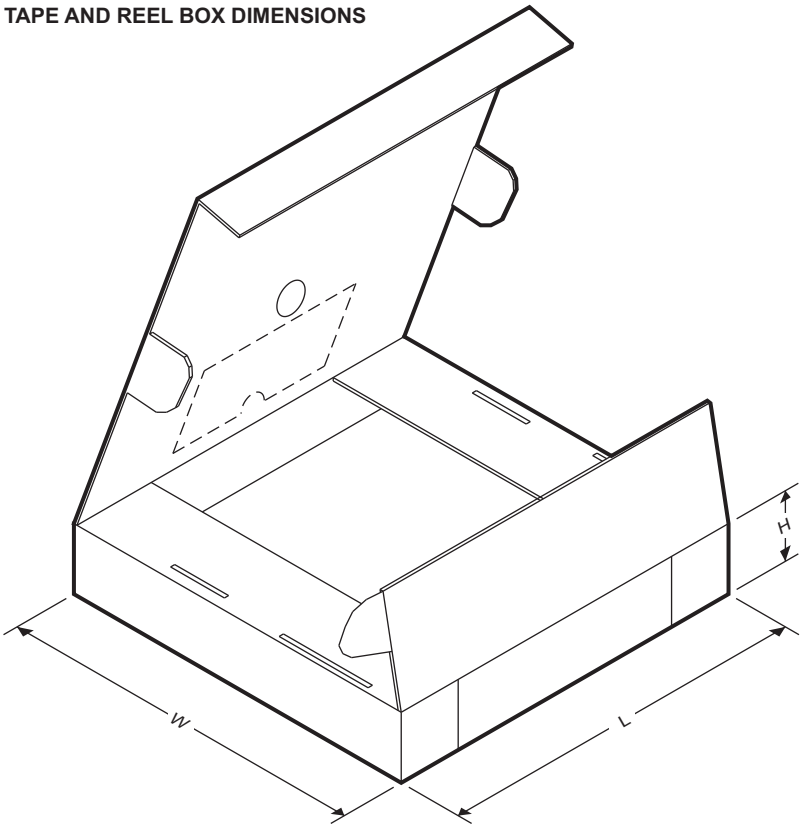
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPSI3052QDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
PTPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3052QDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPSI3052QDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
PTPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
TPSI3052QDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
TPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0

ADVANCE INFORMATION

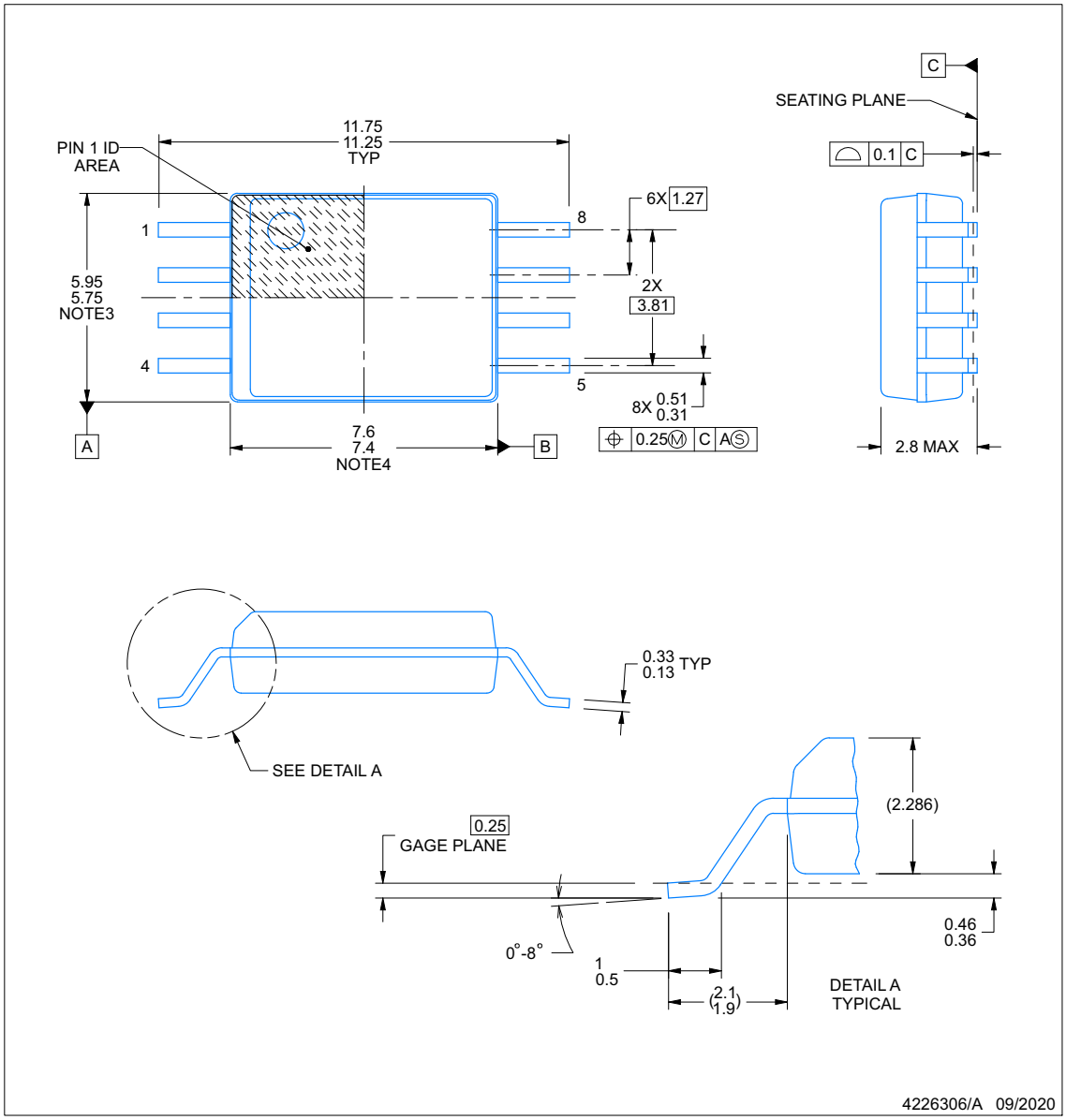
ADVANCE INFORMATION

PACKAGE OUTLINE

DWZ0008A

SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE



NOTES:

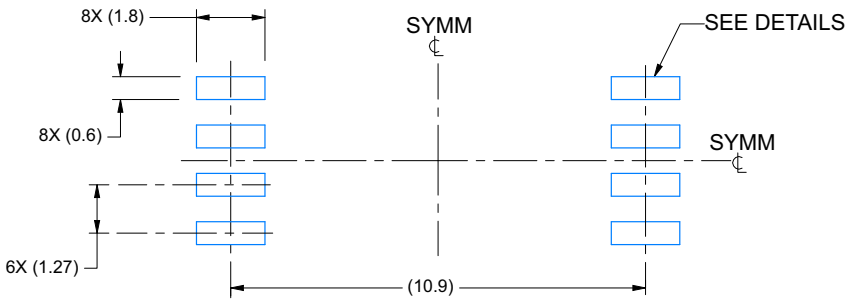
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

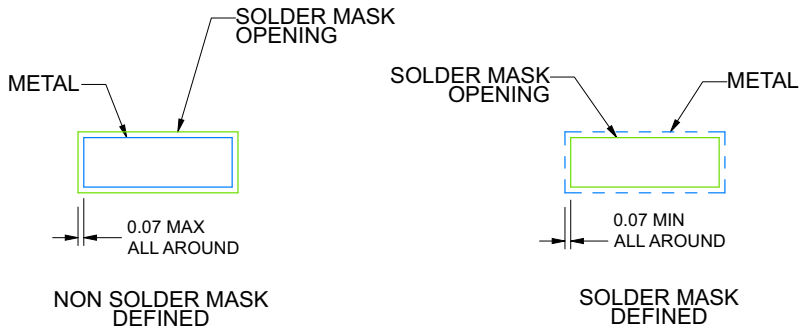
DWZ0008A

SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE: 6X



SOLDER MASK DETAILS

4226306/A 09/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

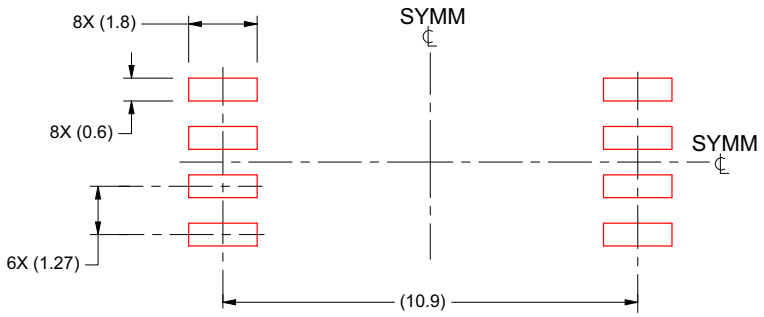
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DWZ0008A — SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4226306/A 09/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSI3052QDWZRQ1	ACTIVE	SO-MOD	DWZ	8	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPSI3052-Q1 :

- Catalog : TPSI3052

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TPSM63602
SLVSGK8 – APRIL 2022

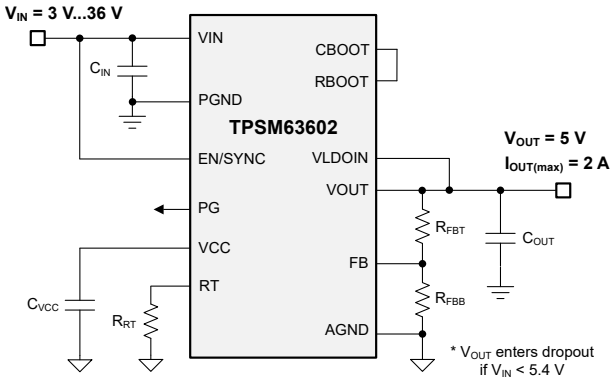
TPSM63602 High-Density, 3-V to 36-V Input, 1-V to 16-V Output, 2-A Power Module With Enhanced HotRod™ QFN Package

1 Features

- Versatile synchronous buck DC/DC module
  - Integrated MOSFETs, inductor, and controller
  - Wide input voltage range of 3 V to 36 V
  - Adjustable output voltage from 1 V to 16 V
  - 4-mm × 6-mm × 1.8-mm overmolded package
  - –40°C to 125°C junction temperature range
  - Frequency adjustable from 200 kHz to 2.2 MHz using the RT pin or an external SYNC signal
  - Negative output voltage capability
- Ultra-high efficiency across the full load range
  - 93% peak efficiency at 12 V_{IN}, 5 V_{OUT}, 1 MHz
  - External bias option for improved efficiency
  - Shutdown quiescent current of 0.6 µA (typical)
  - 0.3-V typical dropout voltage at 2-A load
- Ultra-low conducted and radiated EMI signatures
  - Low-noise package with dual input paths and integrated capacitors reduces switch ringing
  - Resistor-adjustable switch-node slew rate
  - Constant-frequency FPWM mode of operation
  - Meets CISPR 11 and 32 class B emissions
- Suitable for scalable power supplies
  - Pin compatible with the TPSM63603 (36 V, 3 A)
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and V_{IN} UVLO
  - Overcurrent and thermal shutdown protections
- Create a custom design using the TPSM63602 with the WEBENCH® Power Designer

2 Applications

- Test and measurement, aerospace and defense
- Factory automation and control
- Buckand inverting buck-boost power supplies



Typical Schematic

3 Description

The TPSM63602 synchronous buck power module is a highly integrated 36-V, 2-A DC/DC solution that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

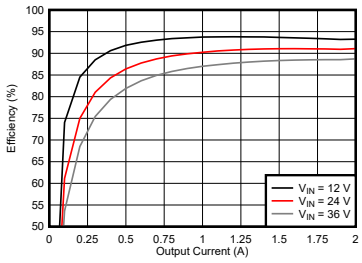
With an output voltage from 1 V to 16 V, the TPSM63602 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total solution requires as few as four external components and eliminates the magnetics and compensation part selection from the design process.

Although designed for small size and simplicity in space-constrained applications, the TPSM63602 module offers many features for robust performance: precision enable with hysteresis for adjustable input-voltage UVLO, resistor-programmable switch node slew rate for improved EMI, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPSM63602	B0QFN (30)	4.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Efficiency, V_{OUT} = 5 V, f_{SW} = 1 MHz

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2022	*	Initial Release

5 Device Comparison Table

Device	Orderable Part Number	Mode	Spread Spectrum	Output Voltage	External Sync	Junction Temperature
TPSM63602	TPSM63602RDHR	FPWM	No	Adjustable	Yes	–40°C to 125°C
TPSM63602V3	TPSM63602V3RDHR	FPWM	No	Fixed 3.3 V	Yes	–40°C to 125°C
TPSM63602V5	TPSM63602V5RDHR	FPWM	No	Fixed 5 V	Yes	–40°C to 125°C

6 Pin Configuration and Functions

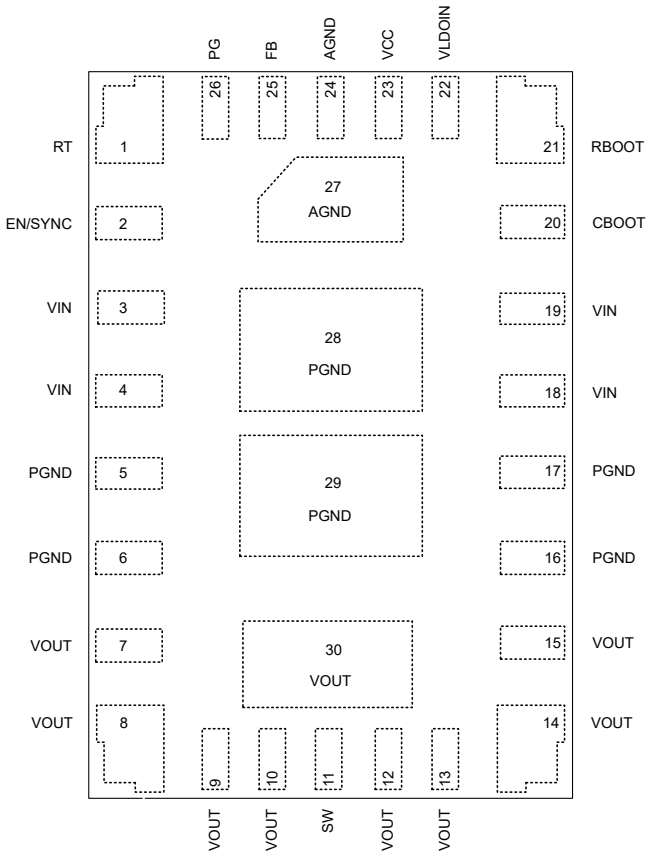


Figure 6-1. 30-Pin QFN, RDH Package (Top View)

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RT	1	I	Frequency setting pin. This analog pin is used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from this pin to AGND. Do not leave this pin open or connect this pin to ground.
EN/SYNC	2	I	Precision enable input pin. High = on, Low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. It also functions as the synchronization input pin. Used to synchronize the device switching frequency to a system clock. Triggers on the rising edge of an external clock. A capacitor can be used to AC couple the synchronization signal to this pin. The module can be turned off by using an open-drain or collector device to connect this pin to AGND. An external voltage divider can be placed between this pin, AGND, and VIN to create an external UVLO.
VIN	3, 4, 18, 19	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device. Refer to Section 11.2 for input capacitor placement example.
PGND	5, 6, 16, 17, 28, 29	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See Section 11.2 for a recommended layout.
VOUT	7–10, 12–15, 30	P	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
SW	11	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
CBOOT	20	I/O	Bootstrap pin for internal high-side driver circuitry. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. This pin is brought out to use in conjunction with RBOOT to effectively lower the value of the internal RBOOT resistor to adjust the SW node slew rate, if necessary.
RBOOT	21	I/O	External bootstrap resistor connection. Internal to the device, a 100-Ω bootstrap resistor is connected between this pin and the CBOOT pin. This pin is brought out to use in conjunction with CBOOT to effectively lower the value of the internal RBOOT resistor to adjust the switch node slew rate, if necessary.
VLDOIN	22	P	Input bias voltage. Supplies the control circuitry of the power module. Input to internal LDO. Connect to an output voltage point to improve efficiency. Connect an optional high-quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If the output voltage is above 12 V, connect this pin to ground.
VCC	23	O	Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF ceramic capacitor from this pin to PGND.
AGND	24, 27	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. *This pin must be connected to PGND at a single point.* See Section 11.2 for a recommended layout.
FB	25	I	Feedback input. For the adjustable output version, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. When connecting with feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See Section 11.2 for a feedback resistor placement. For a fixed output version, connect this pin directly to output capacitor. Do not leave open or connect to ground.
PG	26	O	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to PGND.

(1) P = Power, G = Ground, I = Input, O = Output, NC = No connect

7 Specifications

7.1 Absolute Maximum Ratings

Limits apply over T_J = –40°C to 125°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND, PGND	–0.3	40	V
	RBOOT to SW	–0.3	5.5	
	CBOOT to SW	–0.3	5.5	
	VLDOIN to AGND, PGND	–0.3	16	
	EN/SYNC to AGND, PGND	–0.3	40	
	RT to AGND, PGND	–0.3	5.5	
	FB to AGND, PGND	–0.3	16	
	PG to AGND, PGND	0	20	
	PGND to AGND	–1	2	
Output voltage	VCC to AGND, PGND	–0.3	5.5	V
	SW to AGND, PGND(2)	–0.3	40	
	VOUT to AGND, PGND	–0.3	16	
Input current	PG	—	10	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C
T_{stg}	Storage temperature	–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

			MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)		3		36	V
Input voltage	VLDOIN				12	V
Output voltage	VOUT(1)		1		16	V
Output voltage	VOUT(1)	TPSM63602V3		3.3		V
Output voltage	VOUT(1)	TPSM63602V5		5		V
Output current	IOUT(2)		0		2	A
Frequency	f_{SW} set by RT or SYNC		200		2200	kHz
Input current	PG				2	mA
Output voltage	PG		0		16	V
T_J	Operating junction temperature		–40		125	°C
T_A	Operating ambient temperature		–40		105	°C

(1) Under no conditions should the output voltage be allowed to fall below 0 V.
(2) Maximum continuous DC current may be derated when operating with high switching frequency, high ambient temperature, or both. Refer to the *Typical Characteristics* section for details.

7.4 Thermal Information

THERMAL METRIC(1)		RDH (QFN)	UNIT
		30 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63603 EVM)	29.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	21.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 64-mm × 83-mm four-layer PCB with 2-oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the *Layout* section.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1 mm from the device.

7.5 Electrical Characteristics

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, f_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over I_{OUT} range)	3.95		36	V
		Once operating (over I_{OUT} range)	3		36	V
V_{IN_HYS}	Hysteresis(1)			1.0		V
I_{Q_VIN}	Input operating quiescent current (non-switching)	T_A = 25°C, $V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		4		µA
I_{SDN_VIN}	VIN shutdown quiescent current	$V_{EN/SYNC}$ = 0 V, T_A = 25°C		3		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			0.91		V
V_{EN_HYS}	EN voltage hysteresis		0.275	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
I_{EN}	Input current into EN/SYNC (non-switching)	$V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		1.65		µA
t_{EN}	EN HIGH to start of switching delay(1)			0.7		ms
INTERNAL LDO VCC						
V_{CC}	Internal LDO VCC output voltage	3.4 V ≤ V_{LDOIN} ≤ 12.5 V		3.3		V
		V_{LDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{LDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis(2)	Hysteresis below V_{CC_UVLO}		1.1		V
I_{VLDOIN}	Input current into VLDOIN pin (non-switching, maximum at T_A = 125°C)(3)	$V_{EN/SYNC}$ = 3.3 V, V_{FB} = 1.5 V		25	31.2	µA
FEEDBACK						
V_{OUT}	Adjustable output voltage range (TPSM63602)	Over the I_{OUT} range	1		16	V
	Fixed output voltage (TPSM63602V3)			3.3		V
	Fixed output voltage (TPSM63602V5)			5.0		V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Over the V_{IN} range, V_{OUT} = 1 V, I_{OUT} = 0 A, f_{SW} = 200 kHz	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 3 A		0.1%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4.0 V ≤ V_{IN} ≤ 36 V		0.1%		
I_{FB}	Input current into the FB pin	V_{FB} = 1.0 V		10		nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		2.0	A
I_{OCL}	Output overcurrent (DC) limit threshold			3.8		A
I_{L_HS}	High-side switch current limit	Duty cycle approaches 0%	4.48	4.87	5.32	A
I_{L_LS}	Low-side switch current limit		2.07	2.4	2.80	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time ("hiccup" time before soft start) (1)			80		ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{REF} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if the output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms

7.5 Electrical Characteristics (continued)

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, f_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PG_{OV}	PG upper threshold — rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG lower threshold — falling	% of V_{OUT} setting	92%	94%	96.5%	
PG_{HYS}	PG upper threshold hysteresis (rising and falling)	% of V_{OUT} setting		1.3%		
$V_{IN\_PG\_VALID}$	Input voltage for valid PG output	46-µA pullup, $V_{EN/SYNC}$ = 0 V	1.0			V
V_{PG_LOW}	Low level PG function output voltage	2-mA pullup to the PG pin, $V_{EN/SYNC}$ = 3.3 V			0.4	V
I_{PG}	Input current into the PG pin when open-drain output is high	V_{PG} = 3.3 V		10		nA
I_{OV}	Pulldown current at the SW node under overvoltage condition			0.5		mA
$t_{PG\_FLT\_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG\_FLT\_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by R_T or SYNC		200		2200	kHz
f_{SW_RT1}	Default switching frequency by R_T	R_{RT} = 66.5 kΩ	180	200	220	kHz
f_{SW_RT2}	Default switching frequency by R_T	V_{IN} = 12 V, R_{RT} = 5.76 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
V_{EN_SYNC}	Edge amplitude necessary to sync using EN/SYNC	Rise and fall time < 30 ns	2.4			V
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off high-side switch			2.1		V
t_{ON_MIN}	Minimum ON pulse width(1)	V_{OUT} = 1 V, I_{OUT} = 1 A, RBOOT shorted to CBOOT		55	70	ns
t_{ON_MAX}	Maximum ON pulse width(1)			9		µs
t_{OFF_MIN}	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A, RBOOT shorted to CBOOT		65	85	ns
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
T_{HYST}	Thermal shutdown hysteresis(1)			10		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) Production tested with V_{IN} = 3 V.
(3) This is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. It does not represent the total input current to the system while regulating. For additional information, reference the *Systems Characteristics* and the *Input Supply Current* sections.

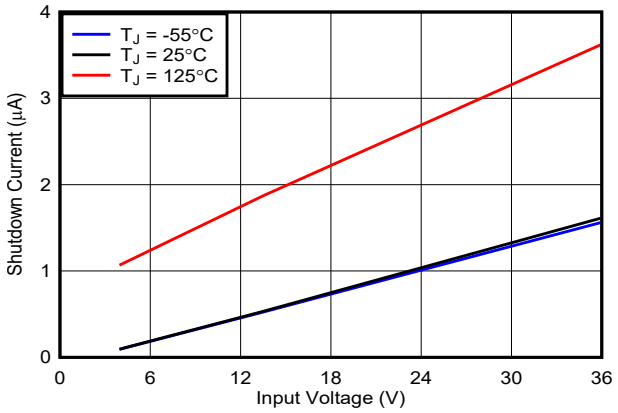
7.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, $V_{EN/SYNC}$ = V_{IN}, V_{VLDOIN} = V_{OUT}, f_{SW} = 800 kHz, I_{OUT} = 0 A		10		mA
OUTPUT VOLTAGE						
V_{FB}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.1 A to full load		1		mV
V_{FB}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 3 A		6		mV
V_{OUT}	Load transient	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 1 A to 2.5 A at 2 A/µs, $C_{OUT(derated)}$ = 49 µF		50		mV
EFFICIENCY						
η	Efficiency	V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 800 kHz		89.5%		
		V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 800 kHz		87.5%		
		V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 1 MHz		91%		
		V_{OUT} = 5 V, V_{IN} = 36 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 1 MHz		88.1%		
		V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 1.5 A, V_{LDOIN} = V_{OUT}, f_{SW} = 2 MHz		94.1%		

7.7 Typical Characteristics

V_{IN} = 24 V, unless otherwise specified



$V_{EN/SYNC}$ = 0 V

Figure 7-1. Shutdown Supply Current

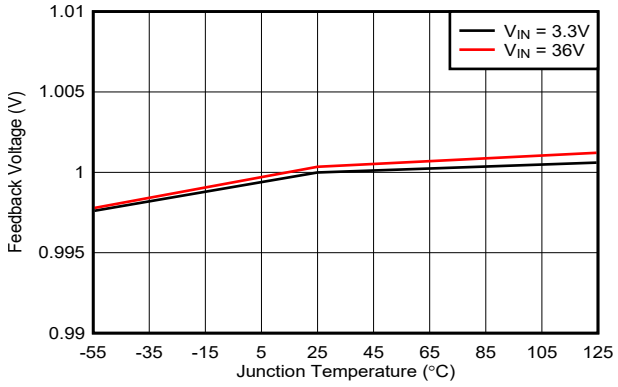


Figure 7-2. Feedback Voltage

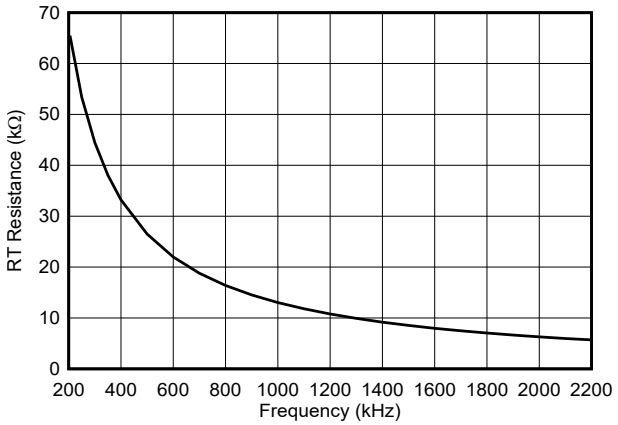


Figure 7-3. Switching Frequency Set by the RT Resistor

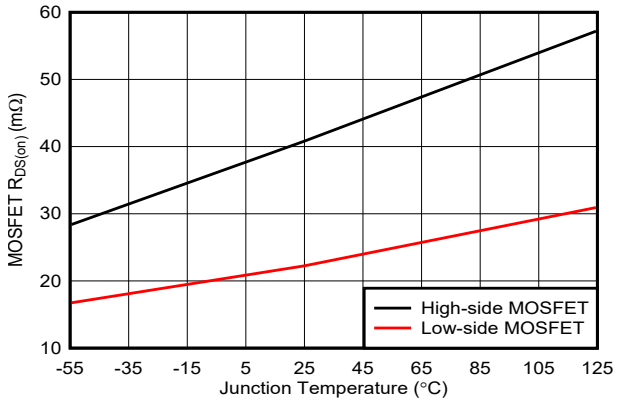


Figure 7-4. High-Side and Low-Side MOSFET $R_{DS(on)}$

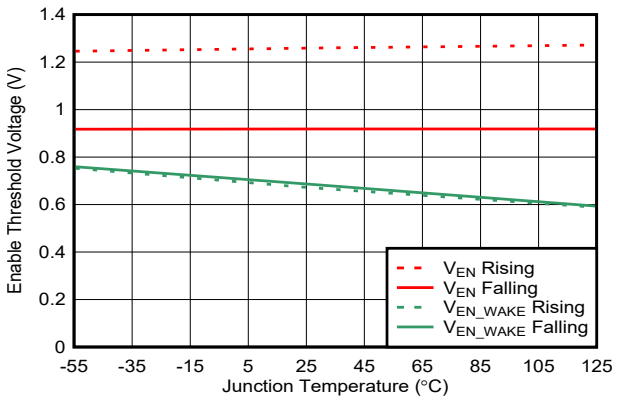


Figure 7-5. Enable Thresholds

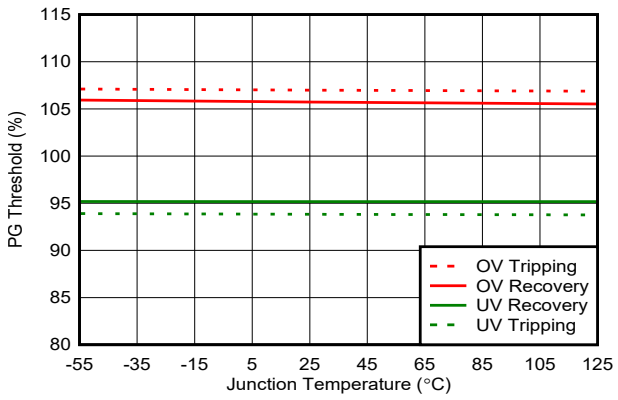
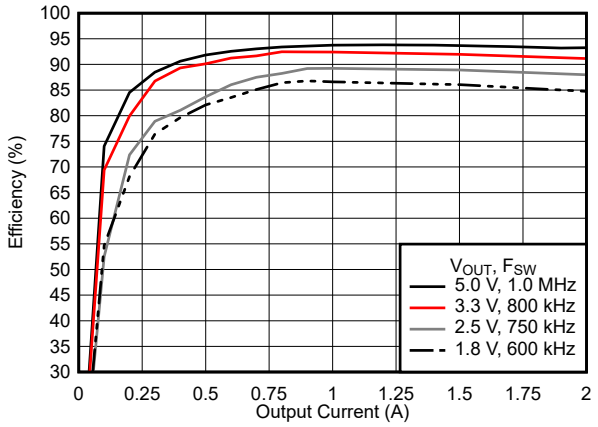


Figure 7-6. Power-Good (PG) Thresholds

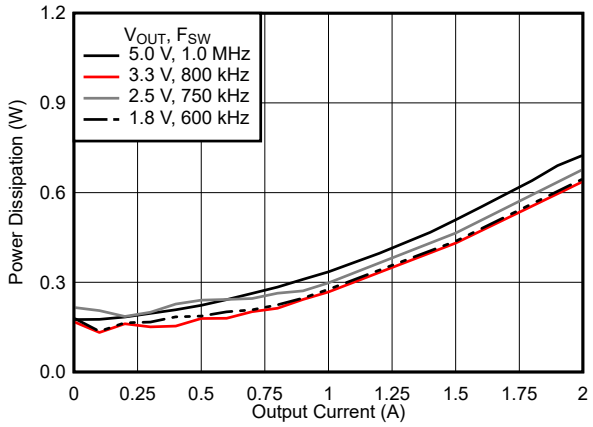
7.8 Typical Characteristics — 2-A Device (V_{IN} = 12 V)

Refer to Section 9.2 for circuit designs.



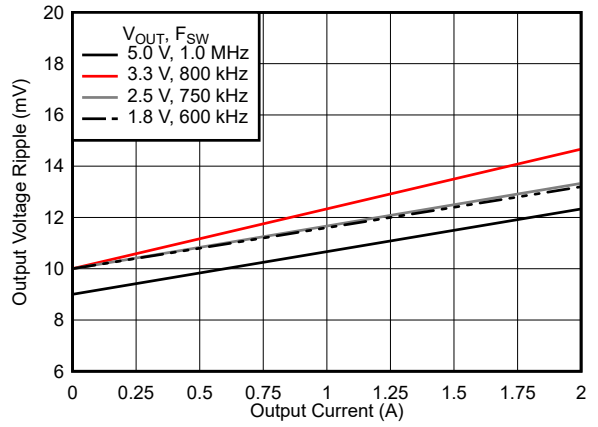
VLDOIN = VOUT

Figure 7-7. Efficiency



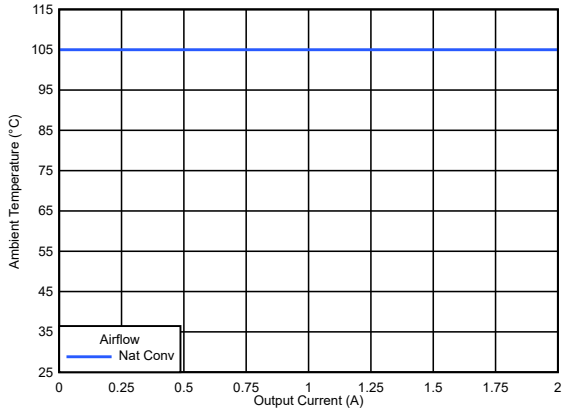
VLDOIN = VOUT

Figure 7-8. Power Dissipation



C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-9. Output Voltage Ripple

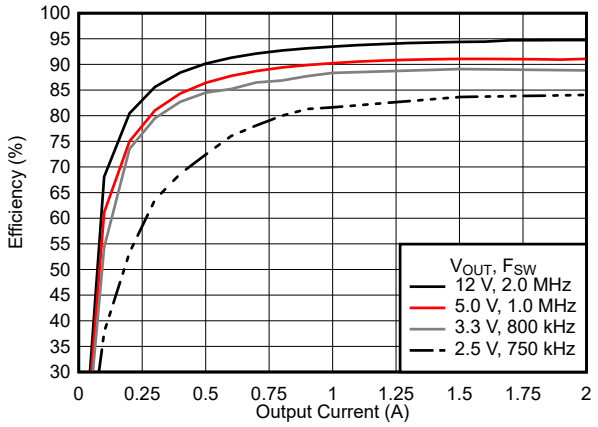


The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-10. Safe Operating Area (All V_{OUT})

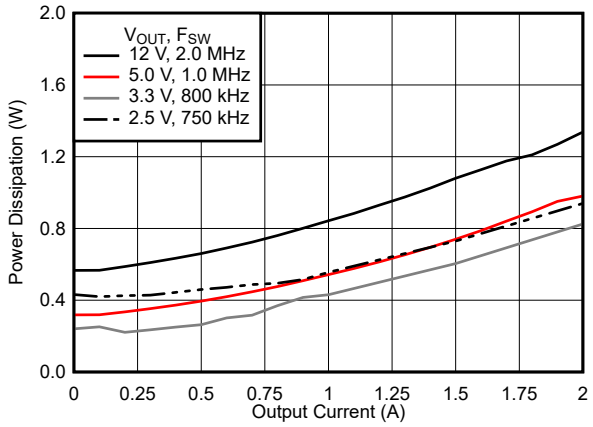
7.9 Typical Characteristics — 2-A Device (V_{IN} = 24 V)

Refer to Section 9.2 for circuit designs.



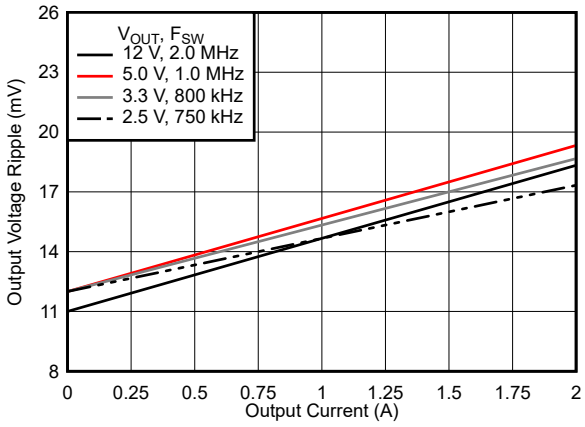
VLDOIN = VOUT

Figure 7-11. Efficiency



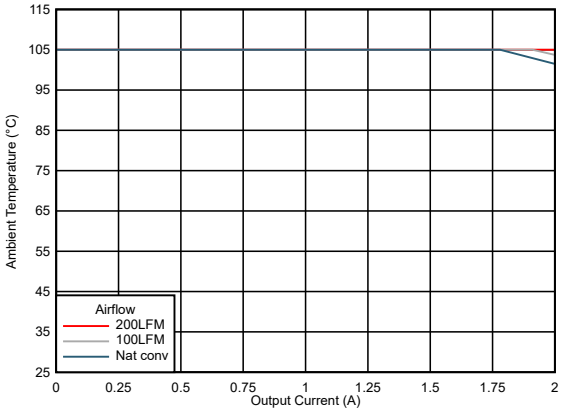
VLDOIN = VOUT

Figure 7-12. Power Dissipation



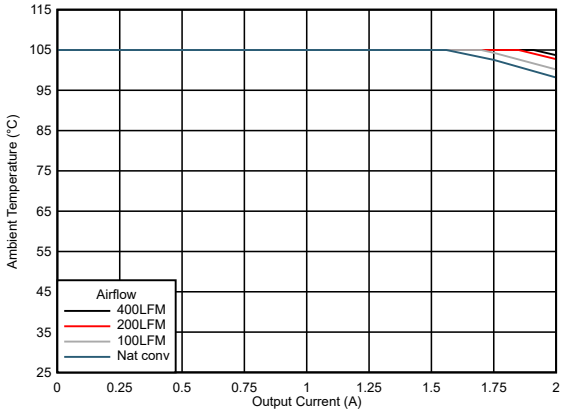
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-13. Output Voltage Ripple



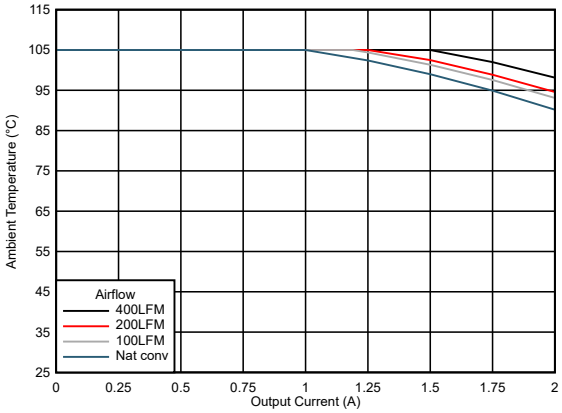
The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-14. Safe Operating Area (V_{OUT} = 3.3 V)



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-15. Safe Operating Area (V_{OUT} = 5.0 V)

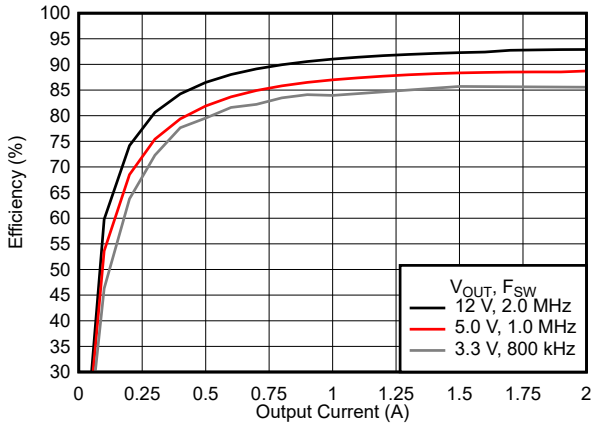


The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-16. Safe Operating Area (V_{OUT} = 12 V)

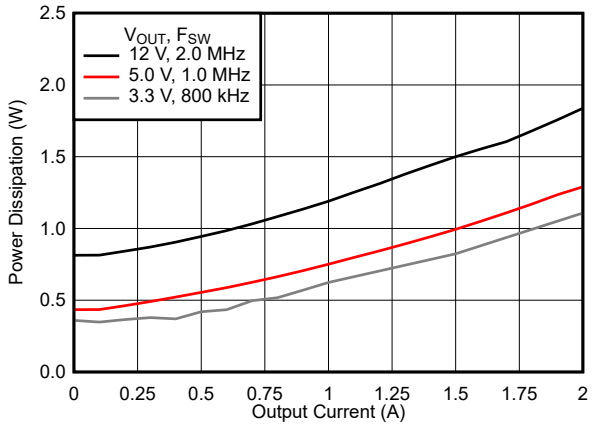
7.10 Typical Characteristics — 2-A Device (V_{IN} = 36 V)

Refer to Section 9.2 for circuit designs.



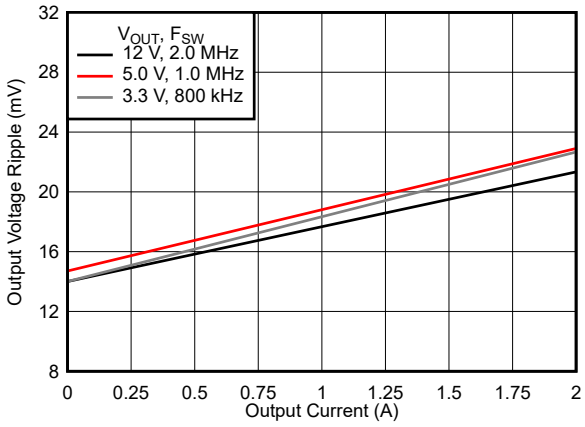
VLDOIN = VOUT

Figure 7-17. Efficiency



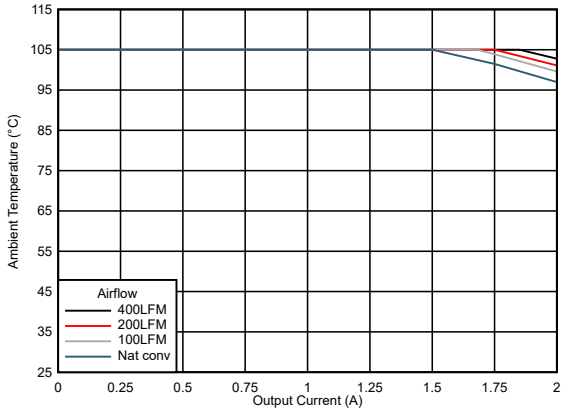
VLDOIN = VOUT

Figure 7-18. Power Dissipation



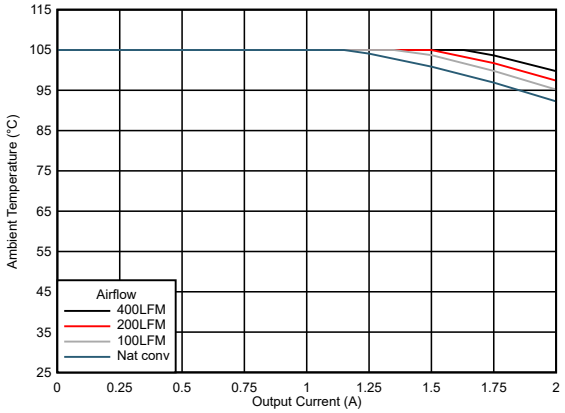
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 7-19. Output Voltage Ripple



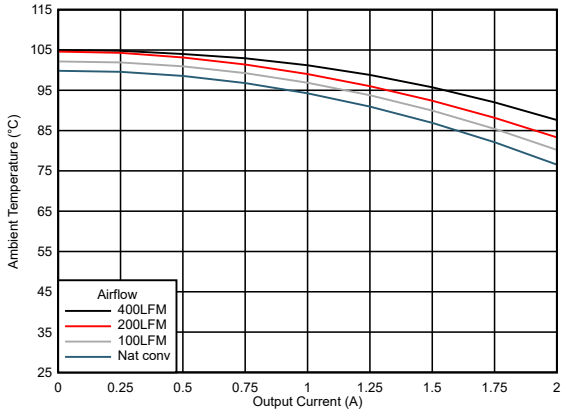
The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-20. Safe Operating Area (V_{OUT} = 3.3 V)



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-21. Safe Operating Area (V_{OUT} = 5.0 V)



The device is soldered to a 64-mm × 83-mm, 4-layer PCB.

Figure 7-22. Safe Operating Area (V_{OUT} = 12 V)

8 Detailed Description

8.1 Overview

The TPSM63602 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, and 24-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM63602 delivers up to 3-A DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin or an external clock signal, the TPSM63602 incorporates specific features to improve EMI performance in noise-sensitive applications:

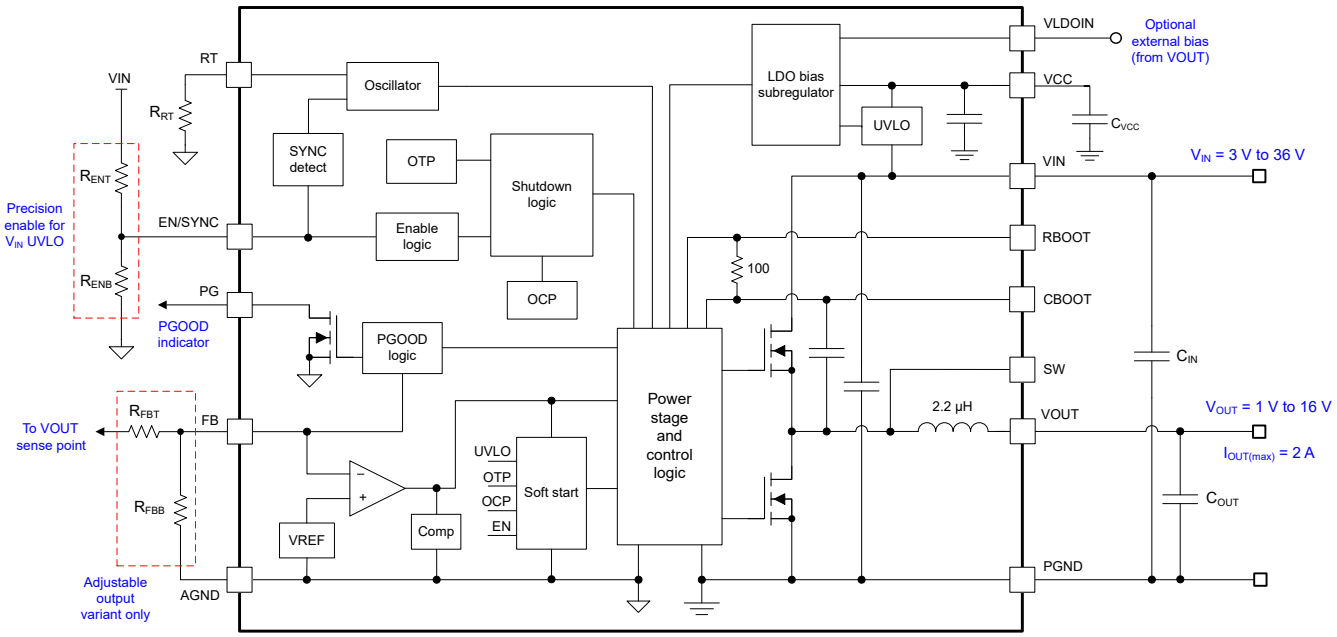
- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling.
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range.
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching.
- Adjustable switch-node slew rate allows optimization of EMI at higher frequency harmonics.

The TPSM63602 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components. See Section 11 for a layout example.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 36 V, the TPSM63602 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in Figure 8-1 shows all the necessary components to implement a TPSM63602-based buck regulator using a single input supply.

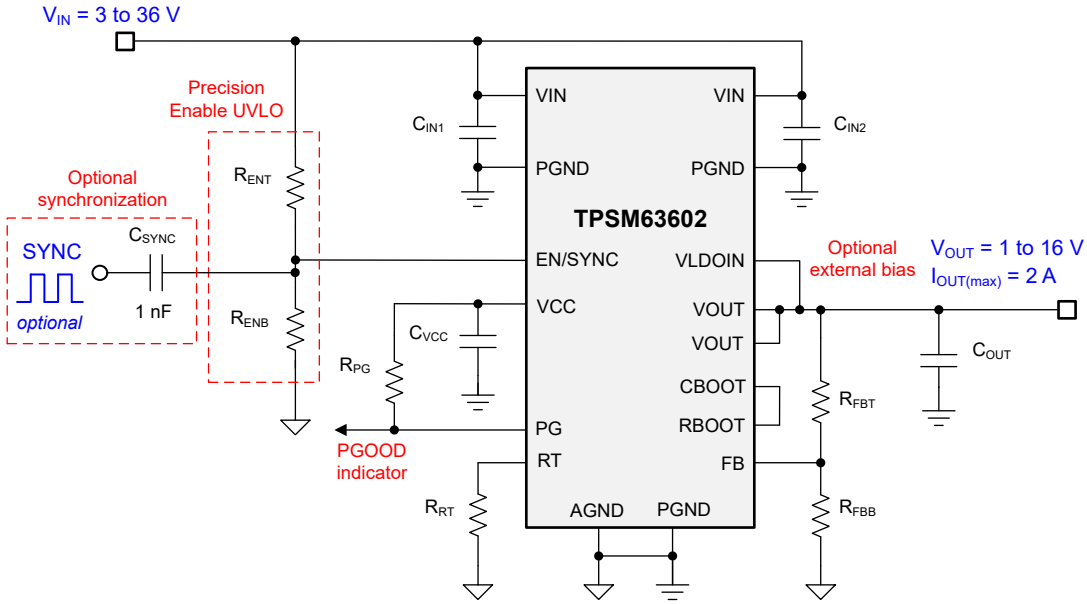


Figure 8-1. TPSM63602 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

Take extra care to make sure that the voltage at the VIN pins does not exceed the absolute maximum voltage rating of 40 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

8.3.2 Adjustable Output Voltage (FB)

The TPSM63602 has an adjustable output voltage range of 1 V to 16 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 8-2). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using Equation 1. Table 8-1 lists the standard resistor values for several output voltages and the recommended switching frequency. The minimum required output capacitance for each output voltage is also included in Table 8-1. The capacitance values listed represent the effective capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (1)$$

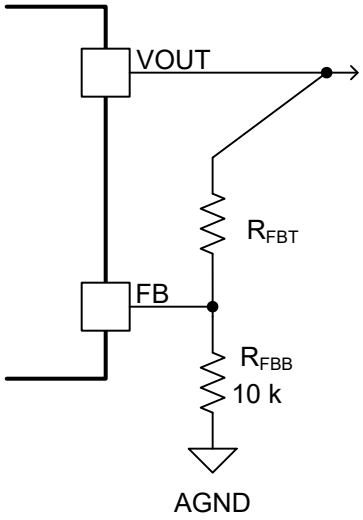


Figure 8-2. FB Resistor Divider

Table 8-1. Standard R_{FBT} Values, Recommended f_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ)(1)	Recommended f_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (Effective)	V_{OUT} (V)	R_{FBT} (kΩ)(1)	Recommended f_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (Effective)
1.0	Short	400	300	3.3	23.2	800	40
1.2	2	500	200	5.0	40.2	1000	25
1.5	4.99	500	160	7.5	64.9	1300	20
1.8	8.06	600	120	10	90.9	1500	15
2.0	10	600	100	12	110	2000	5
2.5	15	750	65	15	140	2200	4
3.0	20	750	50	16	150	2200	3

(1) R_{FBB} = 10 kΩ

Note that higher feedback resistances consume less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended because the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 11.

Fixed Output Voltage Variants

The TPSM63602V3 and TPSM63602V5 are the fixed output voltage variants of the module with 3.3-V and 5-V fixed output voltages, respectively. In these variants, the resistor feedback dividers are located internal to the module. Therefore, the FB pin can be connected directly to output voltage regulation point.

8.3.3 Input Capacitors

Input capacitors are required to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. Equation 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1 - D) + \frac{\Delta I_L^2}{12} \right)} \quad (2)$$

where

- D = V_{OUT} / V_{IN} is the module duty cycle.

Ideally, the DC and AC components of the input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} – I_{IN}) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resulting capacitive component of the AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 3 gives the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (3)$$

Equation 4 gives the input capacitance required for a particular load current.

$$C_{IN} \geq \frac{D \cdot (1 - D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \quad (4)$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TPSM63602 requires a minimum of 2 × 4.7-µF ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 8-2 includes a preferred list of capacitors by vendor.

Table 8-2. Recommended Input Capacitors

Vendor(1)	Dielectric	Part Number	Case Size	Capacitor Characteristics	
				Voltage Rating (V)	Capacitance (µF)(2)
TDK	X7R	C3216X7R1H475K160AC	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7
TDK	X7R	CGA6P3X7R1H475K250AB	1210	50	4.7
Murata	X7S	GCM31CC71H475KA03L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature.)

8.3.4 Output Capacitors

Table 8-1 lists the TPSM63602 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 8-3 for a preferred list of output capacitors by vendor.

Table 8-3. Recommended Output Capacitors

Vendor(1)	Temperature Coefficient	Part Number	Case Size	Capacitor Characteristics	
				Voltage (V)	Capacitance (µF)(2)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10

Table 8-3. Recommended Output Capacitors (continued)

Vendor(1)	Temperature Coefficient	Part Number	Case Size	Capacitor Characteristics	
				Voltage (V)	Capacitance (µF)(2)
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature.)

8.3.5 Switching Frequency (RT)

The switching frequency range of the TPSM63602 is 200 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Use Equation 5 to calculate the R_{RT} value for a desired frequency or simply select from Table 8-4. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if the RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization.

The switching frequency must be selected based on the output voltage setting of the device. See Table 8-4 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

$$R_{RT}\left[k\Omega\right] = \frac{13.46}{F_{SW}\left[MHz\right]} - 0.44 \quad (5)$$

Table 8-4. Switching Frequency Versus Output Voltage (I_{OUT} = A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} Range (V)		V_{OUT} Range (V)		V_{OUT} Range (V)		V_{OUT} Range (V)	
		Min	Max	Min	Max	Min	Max	Min	Max
200	66.5	1.0	2.0	1.0	2.0	1.0	1.5	1.0	1.5
400	33.2	1.0	3.0	1.0	4.0	1.0	3.3	1.2	3.0
600	22.1	1.0	3.5	1.0	6.0	1.5	6.0	1.8	5.0
800	16.5	1.0	3.5	1.0	7.0	1.5	9.0	2.5	7.0
1000	13.0	1.0	3.0	1.0	8.0	2.0	12.0	3.0	10.0
1200	10.7	1.0	3.0	1.5	9.0	2.5	13.0	3.5	14.0
1400	9.09	1.0	3.0	1.5	9.5	3.0	14.0	4.0	16.0
1600	8.06	1.0	3.0	1.5	9.0	3.0	15.0	4.5	16.0
1800	6.98	1.0	3.0	2.0	9.0	3.5	16.0	5.0	16.0
2000	6.34	1.2	2.5	2.0	9.0	4.0	16.0	5.5	16.0
2200	5.626	1.2	2.5	2.0	9.0	4.5	16.0	6.0	16.0

8.3.6 Output ON and OFF Enable (EN/SYNC) and V_{IN} UVLO

The EN/SYNC pin provides precision ON and OFF control for the TPSM63602. Once the EN/SYNC pin voltage exceeds the threshold voltage and V_{IN} is above the minimum turn-on threshold, the device starts operation. The simplest way to enable the TPSM63602 is to connect EN/SYNC directly to VIN, allowing the TPSM63602 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the employment of an enable divider network as shown in Figure 8-3, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

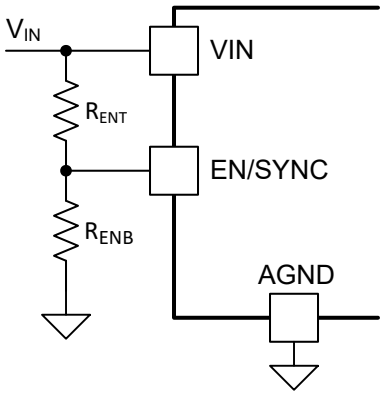


Figure 8-3. V_{IN} UVLO Using the EN/SYNC Pin

R_{ENB} can be calculated using Equation 6.

$$R_{ENB}\left[k\Omega\right] = R_{ENT}\left[k\Omega\right] \cdot \left(\frac{V_{EN\_RISE}\left[V\right]}{V_{IN(on)}\left[V\right] - V_{EN\_RISE}\left[V\right]} \right) \quad (6)$$

where

- R_{ENT} is 100 kΩ (typical).
- V_{EN} is 1.263 V (typical).
- $V_{IN(ON)}$ is the desired start-up input voltage.

Note

The EN/SYNC pin can also be used as an external synchronization clock input. See Section 8.3.7 for additional information. A blanking time of 4 µs to 28 µs is applied to the enable logic after a clock edge is detected. To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs. Any logic change within the blanking time is ignored. Blanking time is not applied when the device is in shutdown mode.

8.3.7 Frequency Synchronization (EN/SYNC)

The TPSM63602 can be synchronized to an external clock using the EN/SYNC pin. The synchronization frequency range is 200 kHz to 2.2 MHz. The internal oscillator can be synchronized by AC coupling a positive clock edge into the EN/SYNC pin, as shown in Figure 8-4. It is recommended to keep the parallel combination value of R_{ENT} and R_{ENB} in the 100-kΩ range. R_{ENT} is required for synchronization, but R_{ENB} can be left open. The external clock must be off before start-up to allow proper start-up sequencing. After a valid synchronization signal is applied for 2048 cycles, the clock frequency changes to that of the applied signal.

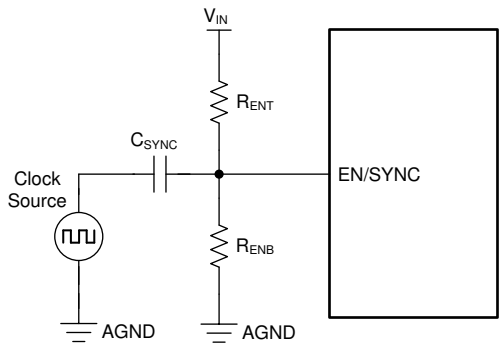


Figure 8-4. Typical Synchronization Using the EN/SYNC Pin

Referring to Figure 8-5, the AC-coupled voltage edge at the EN/SYNC pin must exceed the SYNC amplitude threshold, V_{EN_SYNC}, of 2.4 V to trip the internal synchronization pulse detector. In addition, the minimum EN/SYNC rising pulse and falling pulse durations must be longer than the SYNC signal hold time, t_{SYNC_EDGE}, of 100 ns and shorter than the minimum blanking time, t_B. A 3.3-V or higher amplitude pulse signal coupled through a 1-nF capacitor, C_{SYNC}, is suggested.

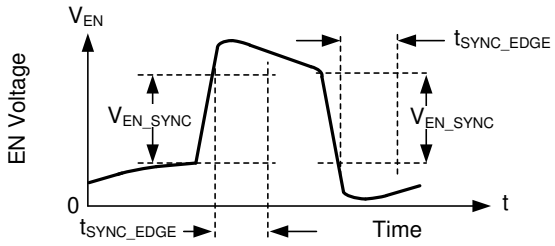


Figure 8-5. Typical SYNC Waveform

8.3.8 Power-Good Monitor (PG)

The TPSM63602 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. The PGOOD pin voltage goes low when the feedback voltage is outside of the PGOOD thresholds. This occurs during the following:

- While the device is disabled
- In current limit
- In thermal shutdown
- During normal start-up, when the output voltage has not reach its regulation value

A glitch filter prevents false flag operation for short excursions (< 120 µs typical) of the output voltage, such as during line and load transients.

PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 20 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in Figure 8-6, or for fault protection and output monitoring.

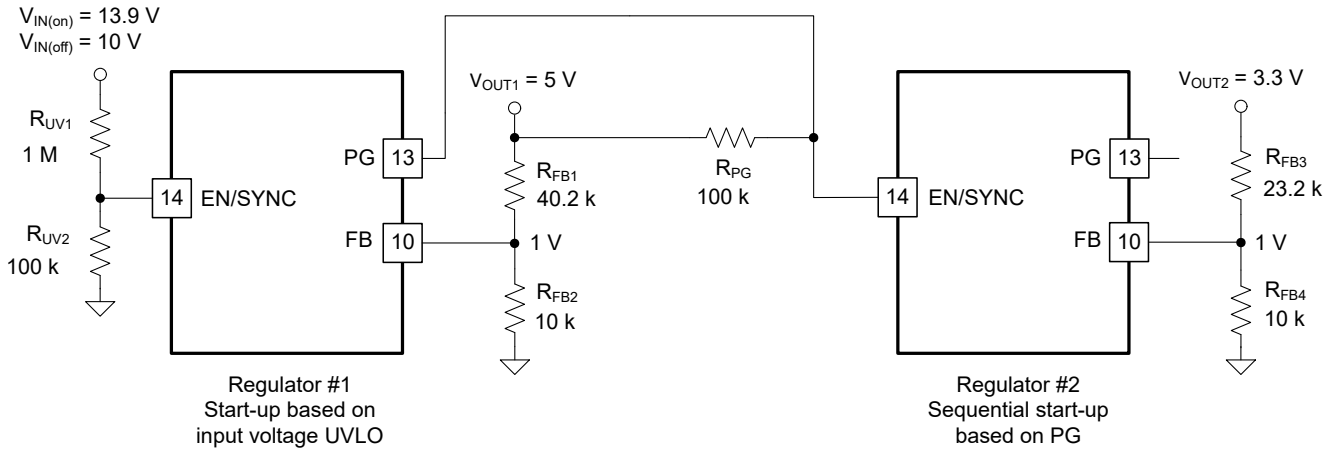


Figure 8-6. TPSM63602 Sequencing Implementation Using PG and EN/SYNC

8.3.9 Adjustable Switch-Node Slew Rate (RBOOT and CBOOT)

Adjust the switch-node slew rate of the TPSM63602 to slow the switch-node voltage rise time and improve EMI performance at high frequencies. However, slowing the rise time decreases efficiency. Take care to balance the improved EMI versus the decreased efficiency.

Internal to the device, a 100-Ω bootstrap resistor is connected between the RBOOT and CBOOT pins as shown in Figure 8-7. Leaving these pins open incorporates the 100-Ω resistor into the BOOT circuit, slowing the SW voltage slew rate and optimizing EMI. However, if improved EMI is not required, connecting RBOOT to CBOOT shorts the internal resistor, resulting in higher efficiency. Placing a resistor across RBOOT and CBOOT allows adjustment of the internal resistor to balance EMI and efficiency.

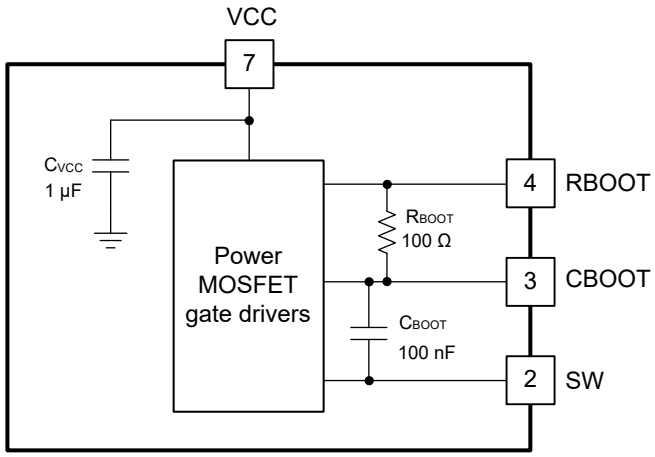


Figure 8-7. Internal BOOT Resistor

8.3.10 Internal LDO, VCC Output, and VLDOIN Input

The TPSM63602 has an internal LDO to power internal circuitry. The VCC pin is the output of the internal LDO. This pin must not be used to power external circuitry. Connect a high-quality, 1-µF capacitor from this pin to AGND, close to the device pins. Do not load the VCC pin or short it to ground.

The VLDOIN pin is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity.

The LDO generates the VCC voltage from one of the two inputs: V_{IN} or the VLDOIN input. When VLDOIN is tied to ground or below 3.1 V, the LDO is powered from V_{IN}. When VLDOIN is tied to a voltage higher than 3.1 V, the LDO input is powered from VLDOIN. VLDOIN voltage must be lower than both V_{IN} and 12.5 V.

The VLDOIN input is designed to reduce the LDO power loss. The LDO power loss is:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\_LDO} - V_{VCC}) \quad (7)$$

The higher the difference between the input and output voltages of the LDO, the more loss occurs to supply the same LDO output current. The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, to reduce the difference of the input and output voltages of the LDO, and reduce power loss. For example, if the LDO current were 10 mA at a certain frequency with V_{IN} = 24 V and V_{OUT} = 5 V. The LDO loss with VLDOIN tied to ground is:

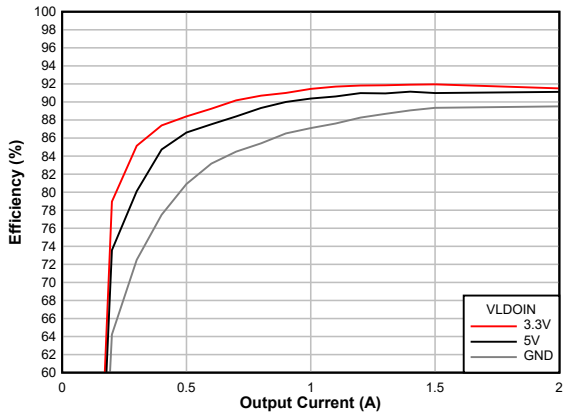
$$10\ mA \times (24\ V - 3.3\ V) = 207\ mW \quad (8)$$

The loss with VLDOIN tied to V_{OUT} (5 V) is:

$$10\ mA \times (5\ V - 3.3\ V) = 17\ mW \quad (9)$$

The efficiency improvement is more significant at light and mid loads because the LDO loss is a higher percentage of the total loss. The improvement is more significant with higher switching frequency because the LDO current is higher at higher switching frequency. The improvement is more significant when V_{IN} » V_{OUT} because the voltage difference is higher.

Figure 8-8 and Figure 8-9 show typical efficiency waveforms with VLDOIN powered by different input voltages.



V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz

I_{LDO} = 10 mA

Figure 8-8. Efficiency Improvements with VLDOIN (V_{OUT} = 5 V)

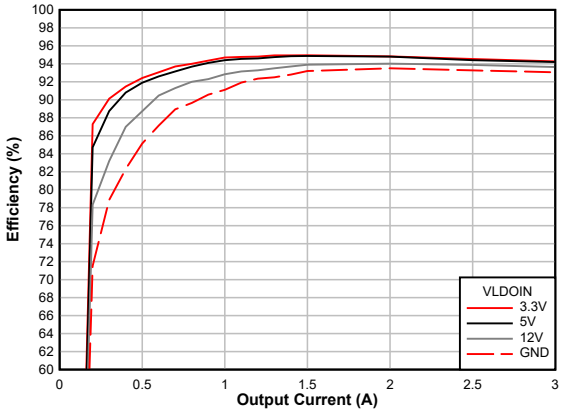


Figure 8-9. Efficiency Improvements with VLDOIN (V_{OUT} = 12 V)

8.3.11 Overcurrent Protection (OCP)

The TPSM63602 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TPSM63602 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the regulator is shut down and kept off for 80 ms (typical) before the TPSM63602 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

8.3.12 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM63602 attempts to restart when the junction temperature falls to 158°C (typical).

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN/SYNC pin provides ON and OFF control for the TPSM63602. When $V_{EN/SYNC}$ is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The input quiescent current in shutdown mode drops to 0.6 µA (typical). The TPSM63602 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

8.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator itself. When $V_{EN/SYNC}$ is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until $V_{EN/SYNC}$ rises above the precision enable threshold.

8.4.3 Active Mode

The TPSM63602 is in active mode when V_{IN} and $V_{EN/SYNC}$ are above their relevant thresholds and no fault conditions are present. The simplest way to enable the operation is to connect the EN/SYNC pin to V_{IN}, which allows self-start–up when the applied input voltage exceeds the minimum start-up voltage.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM63602 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. The following section describes the design procedure to configure the TPSM63602 power module. To expedite and streamline the design process, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. To expedite and streamline the design process for a TPSM63602-based regulator, a comprehensive TPSM63602 quickstart calculator.

As mentioned previously, the TPSM63602 also integrates several optional features to meet system design requirements, including the following:

- Precision enable with hysteresis
- External adjustable UVLO
- Adjustable SW node slew rate
- A power-good indicator

The following application circuits show the TPSM63602 configuration options suitable for several application use cases. Refer to the *TPSM63603EVM User's Guide* for more detail.

9.2 Typical Applications

The following designs show sample typical applications and design procedures to implement the TPSM63602.

9.2.1 Design 1 — 2-A Synchronous Buck Regulator for Industrial Applications

Figure 9-1 shows the schematic diagram of a 5-V, 2-A buck regulator with a switching frequency of 1 MHz. The nominal input voltage for the sample design is 24 V. A 13-kΩ R_{RT} resistor sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency for this specific application.

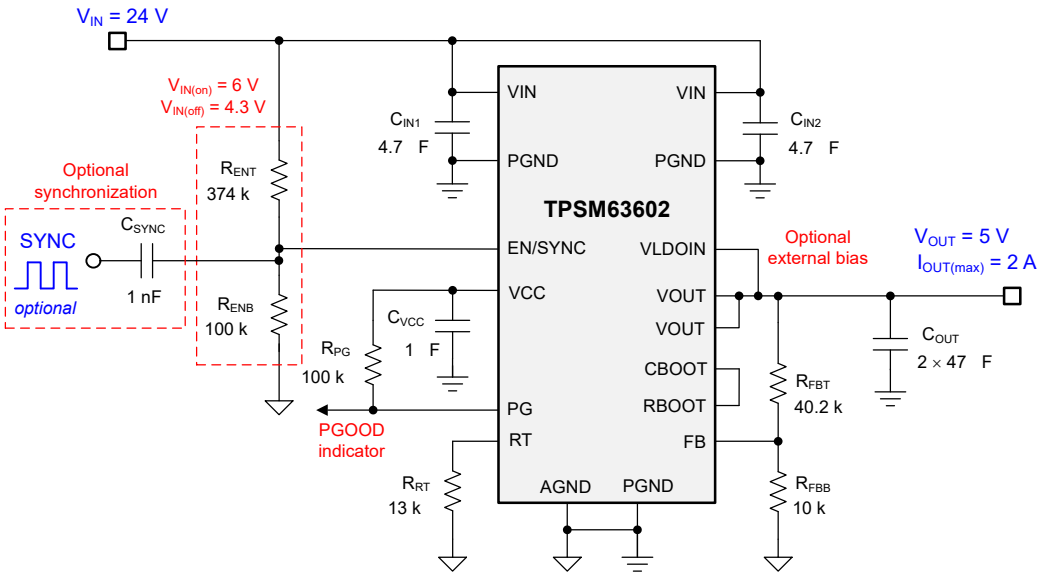


Figure 9-1. Circuit Schematic

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters and follow the design procedures in Section 9.2.1.2.

Table 9-1. Design Example Parameters

Design Parameter	Value
Input voltage	24 V
Output voltage	5 V
Output current	0 A to 2 A
Switching frequency	1 MHz

Table 9-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 9-2. List of Materials for Application Circuit 1

Reference Designator	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}	2	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 100 V, X7S, 1206, ceramic	Murata	GRM31CC72A475KE11L
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
		1 µF, 16 V, X5R, 0402, ceramic	Taiyo Yuden	EMK105BJ105KVHF
U_1	1	TPSM63602 36-V, 2-A synchronous buck module	Texas Instruments	TPSM63602RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TPSM63602 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Output Voltage Setpoint

The output voltage of the TPSM63602 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBB} can be selected from Table 8-1 or calculated using Equation 10:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \quad (10)$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

9.2.1.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 8-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND.

9.2.1.2.4 Input Capacitor Selection

The TPSM63602 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, select two 4.7-µF, 50-V, 1210 case size, ceramic capacitors.

9.2.1.2.5 Output Capacitor Selection

For a 5-V output, the TPSM63602 requires a minimum of 25 µF of effective output capacitance for proper operation (see Table 8-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

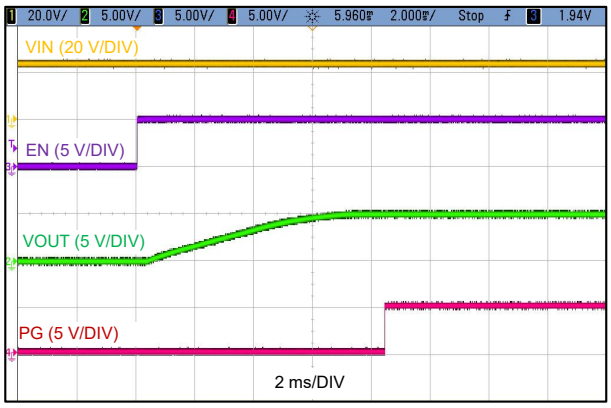
For this design example, select two 47-µF, 10-V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 48 µF at 5 V.

9.2.1.2.6 Other Connections

- Short RBOOT to CBOOT for best efficiency.
- Connect VLDOIN to VOUT to improve efficiency.
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

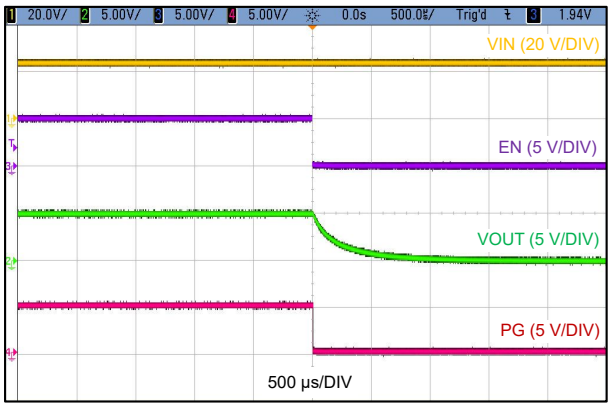
9.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 2 A), and f_{SW} = 1 MHz



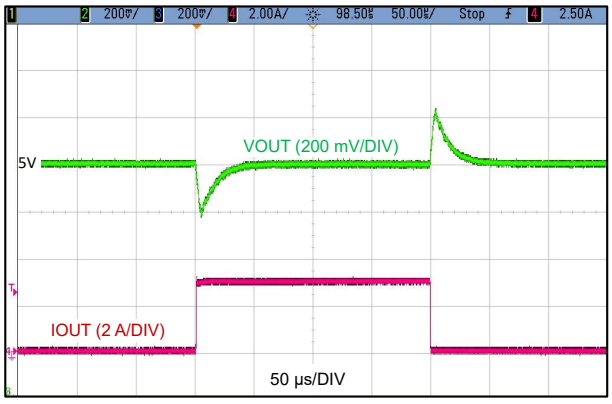
V_{IN} = 24 V V_{OUT} = 5 V

Figure 9-2. Start-Up Waveforms



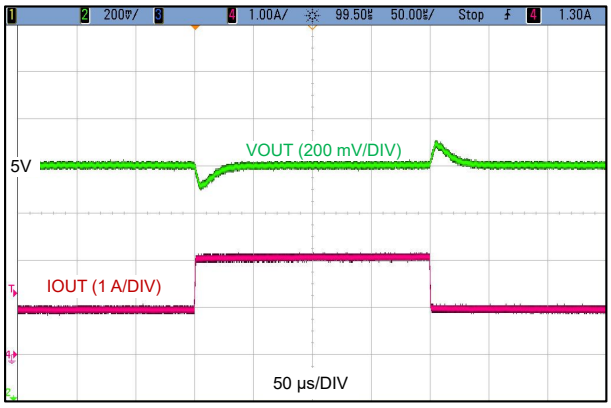
V_{IN} = 24 V V_{OUT} = 5 V

Figure 9-3. Shutdown Waveforms



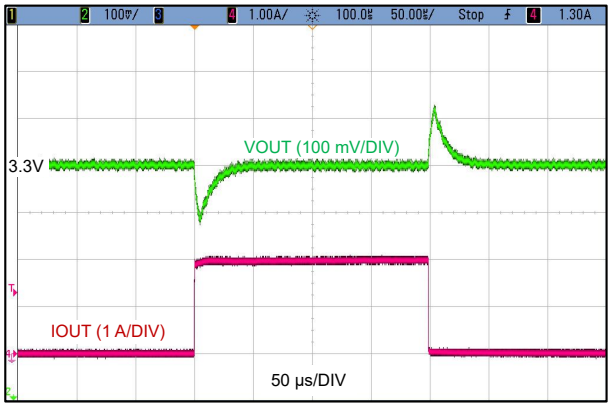
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-4. Load Transient, 0 A to 2 A, 1 A/µs



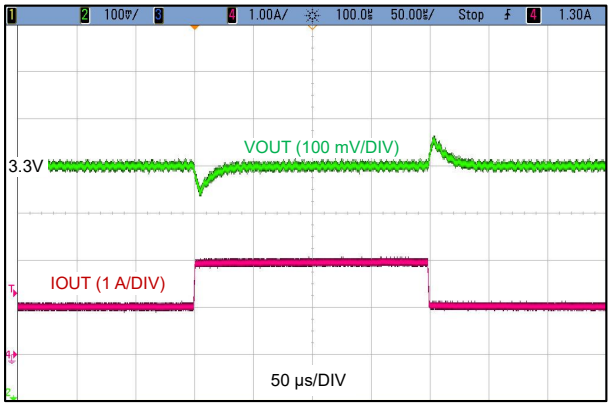
V_{IN} = 24 V V_{OUT} = 5 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-5. Load Transient, 1 A to 2 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-6. Load Transient, 0 A to 2 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 9-7. Load Transient, 1 A to 2 A, 1 A/µs

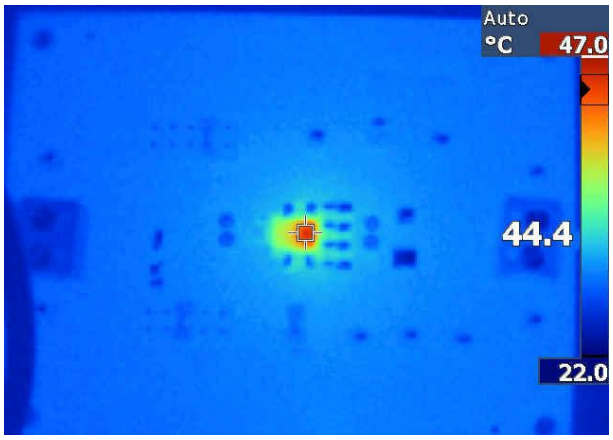


Figure 9-8. Thermal Image, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

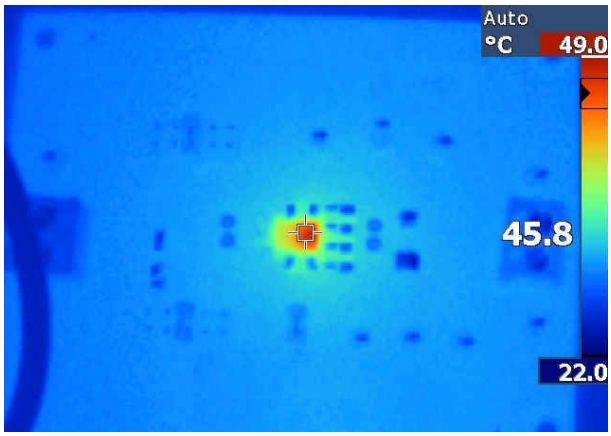


Figure 9-9. Thermal Image, V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

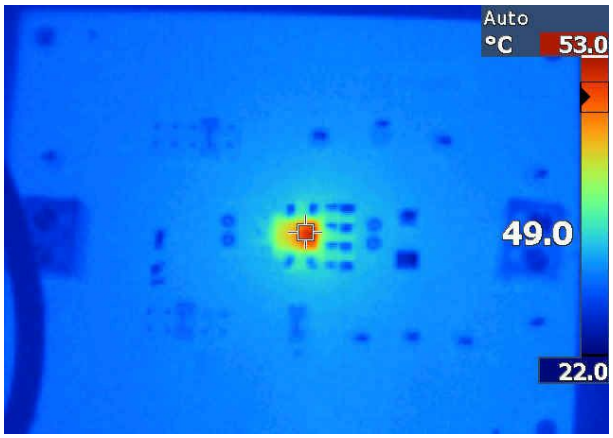


Figure 9-10. Thermal Image, V_{IN} = 24 V, V_{OUT} = 3.3 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

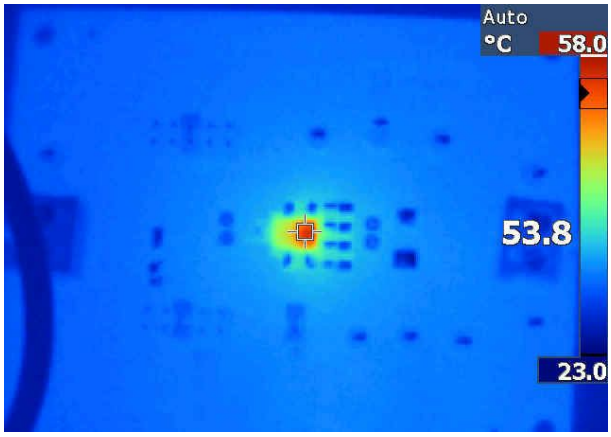


Figure 9-11. Thermal Image, V_{IN} = 24 V, V_{OUT} = 5 V, f_{SW} = 1 MHz, I_{OUT} = 2 A

9.2.2 Design 2 — Inverting Buck-Boost Regulator with a –5-V Output

Figure 9-12 shows the schematic diagram of a –5-V inverting buck-boost regulator with a switching frequency of 1 MHz. The input voltage range for the sample design is 12 V to 24 V.

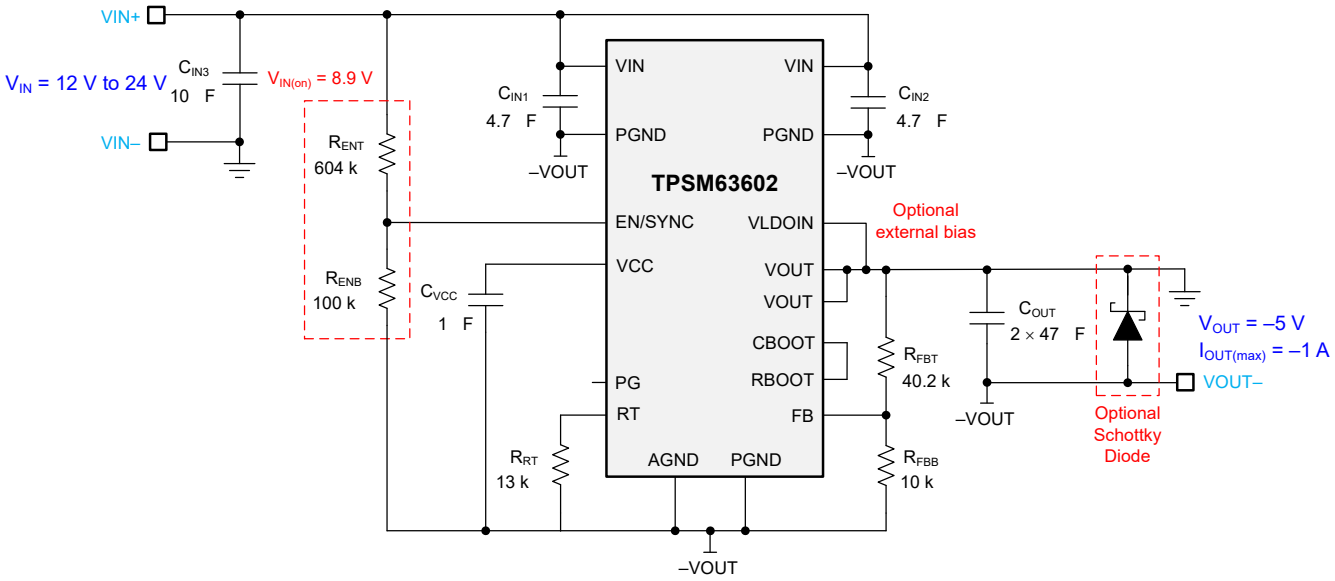


Figure 9-12. Circuit Schematic

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-3 as the input parameters and follow the design procedures in Section 9.2.2.2.

Table 9-3. Design Example Parameters

Design Parameter	Value
Input voltage	12 to 24 V
Output voltage	–5 V
Output current	0 A to 1 A
Switching frequency	1 MHz

Table 9-4 gives the selected module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 9-4. List of Materials for Application Circuit 2

Reference Designator	Qty	Specification	Manufacturer(1)	Part Number
C_{IN1}, C_{IN2}, C_{IN3}	3	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 50 V, X7S, 1206, ceramic	Murata	GCM31CC71H475KA03K
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
U_1	1	TPSM63602 36-V, 2-A synchronous buck module	Texas Instruments	TPSM63602RDLR

More generally, the TPSM63602 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Output Voltage Setpoint

The output voltage of the TPSM63602 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. Calculate the value for R_{FBT} using Equation 11.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1 \right) \tag{11}$$

For the desired output voltage of –5 V, enter the absolute value of 5 V for V_{OUT} in Equation 11. The formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

9.2.2.2.2 IBB Maximum Output Current

The achievable output current with an IBB topology using the TPSM63602 is:

$$I_{OUT(max)} = I_{LDC(max)} \times (1 - D) \tag{12}$$

where

- $I_{LDC(max)}$ = 2 A is the rated current of the module.
- $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the module duty cycle.

Therefore, in the case of V_{IN} = 12 V and V_{OUT} = –5 V, the maximum output current is 1.4 A.

9.2.2.2.3 Switching Frequency Selection

To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND pins of the module based on Equation 5.

9.2.2.2.4 Input Capacitor Selection

The TPSM63602 requires a minimum input capacitance of 2 × 4.7-µF ceramic type between the VIN pins and PGND pins as close as possible to the module. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. In an inverting buck-boost configuration, the maximum voltage between VIN and PGND pin of the module is equal to $V_{IN} + |V_{OUT}|$.

For this design, two 4.7-µF, 50-V, 1210 case size, ceramic capacitors are selected.

9.2.2.2.5 Output Capacitor Selection

The TPSM63602 requires a minimum of 25 µF of effective output capacitance for proper operation. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, two 47-µF, 10-V, 1210 case size, ceramic capacitors are used, which have a total effective capacitance of approximately 48 µF at 5 V.

9.2.2.2.6 Other Connections

Short RBOOT to CBOOT and connect VLDOIN to VOUT for the best efficiency.

Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

The right-half-plane zero of an IBB topology is at its lowest frequency at minimum input voltage. However, it does not appear at low frequency for a –5-V output and has minimal effect on the loop response for this application.

In an inverting buck-boost configuration, the input capacitor, C_{IN}, and output capacitor, C_{OUT}, can form an AC capacitive divider during a fast V_{IN} transient or hot-plugged event at the input. This event will result in a positive voltage spike at the output that can disturb the load. In this case, an optional Schottky diode can be installed between –VOUT and GND as shown in Figure 9-12 to clamp the output spike.

9.2.2.2.7 EMI

The TPSM63602 is compliant with EN55011 radiated emissions. Figure 9-13, Figure 9-14, and Figure 9-15 show typical examples of radiated emission plots for the TPSM63603 , which is in the same family of parts. The graphs include the plots of the antenna in the horizontal and vertical positions.

9.2.2.2.7.1 EMI Plots

EMI plots were measured using the standard TPSM63603EVM.

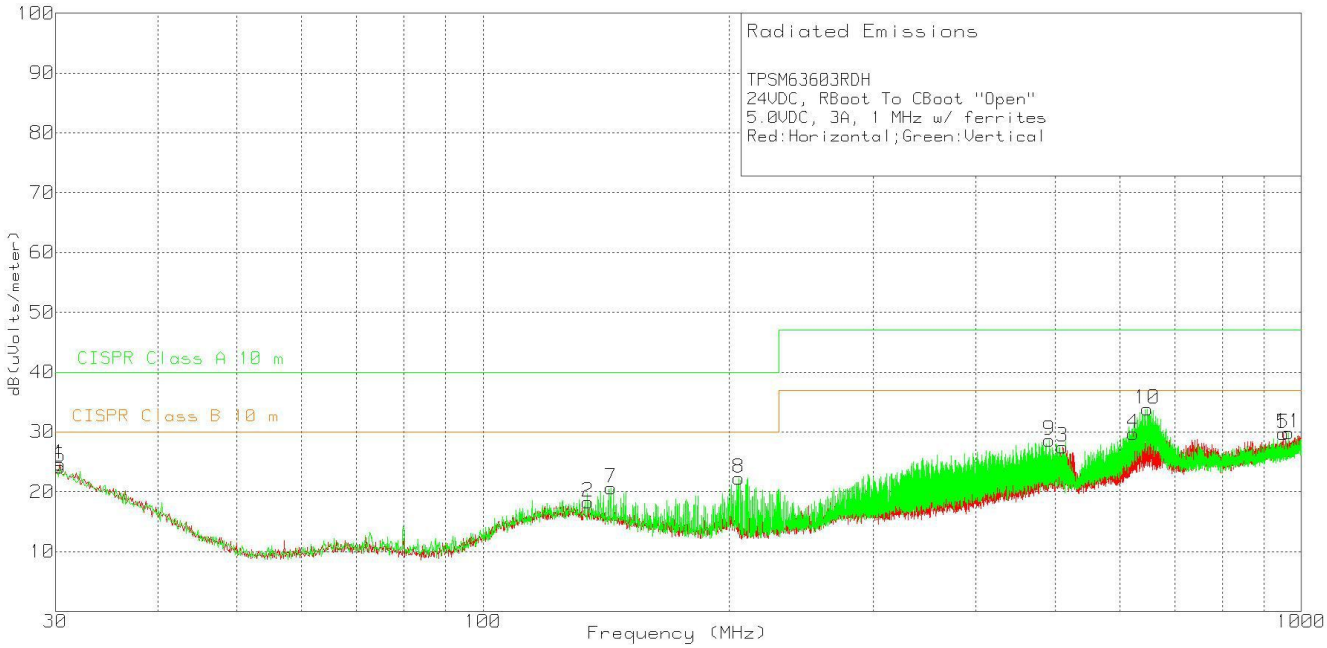


Figure 9-13. Radiated Emissions, 24-V Input, 5-V Output, 3-A Load

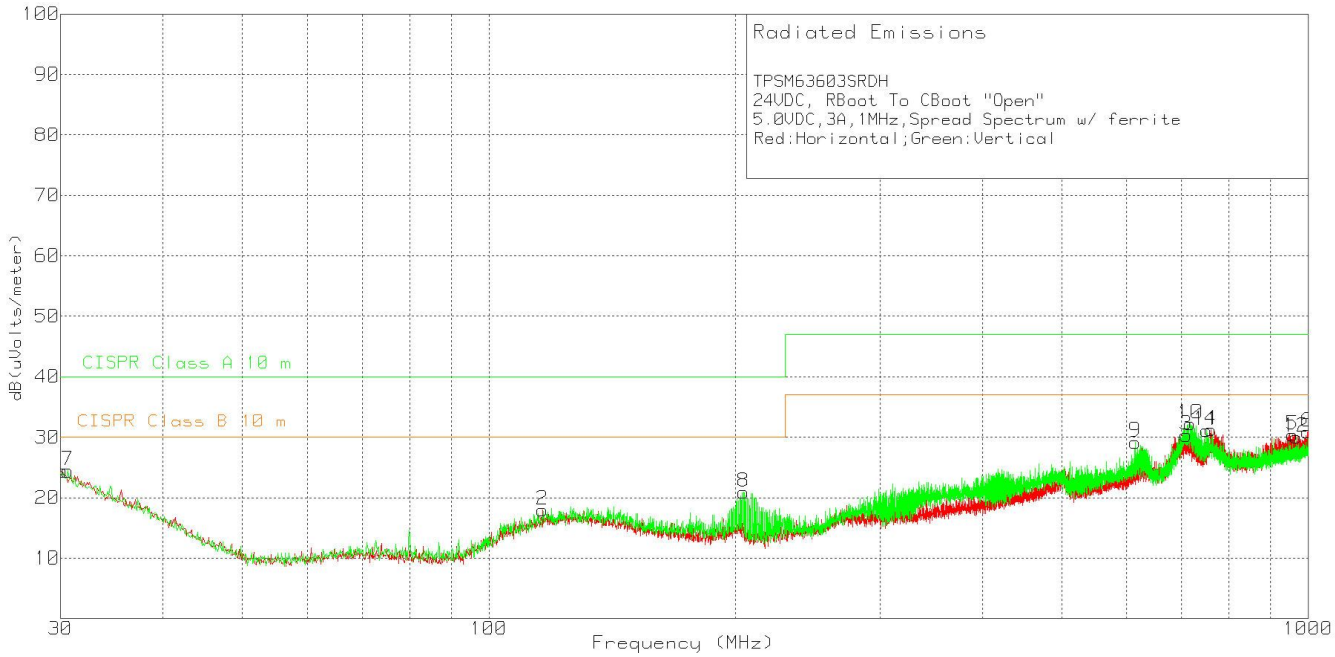


Figure 9-14. Radiated Emissions, 24-V Input, 5-V Output, 3-A Load, Spread Spectrum

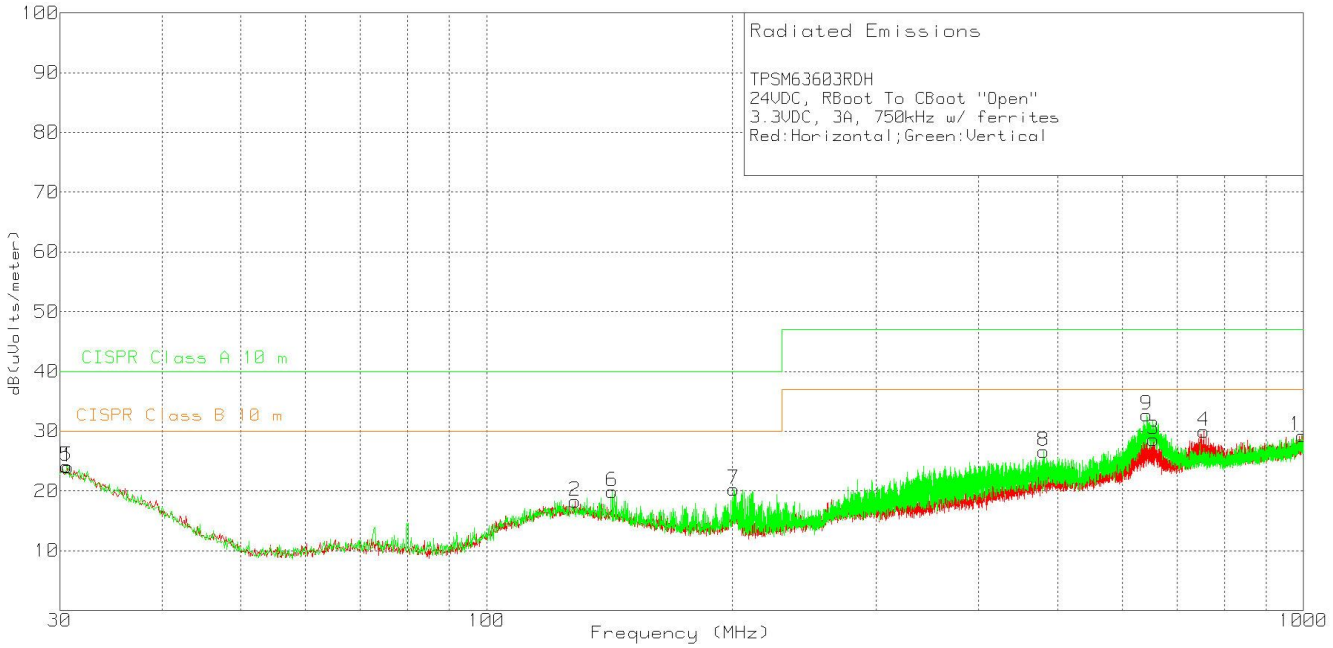


Figure 9-15. Radiated Emissions, 24-V Input, 3.3-V Output, 3-A Load

10 Power Supply Recommendations

The TPSM63602 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 13.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \ \eta} \tag{13}$$

where

- η is efficiency.

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

11 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

11.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 11-1 and Figure 11-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high-frequency noise.
- Locate additional output capacitors between the ceramic capacitors and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

11.2 Layout Example

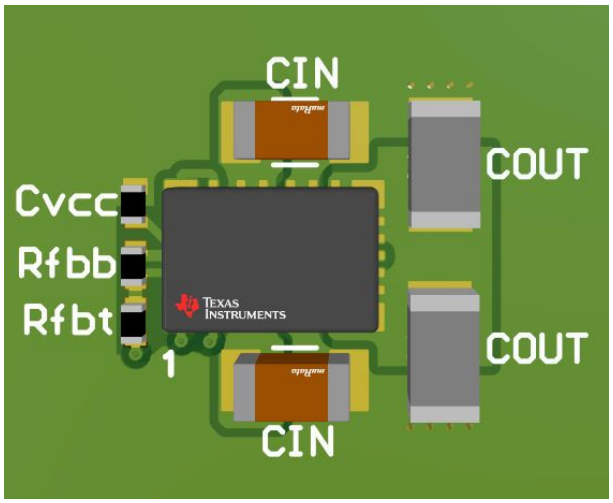


Figure 11-1. Typical Top-Layer Layout

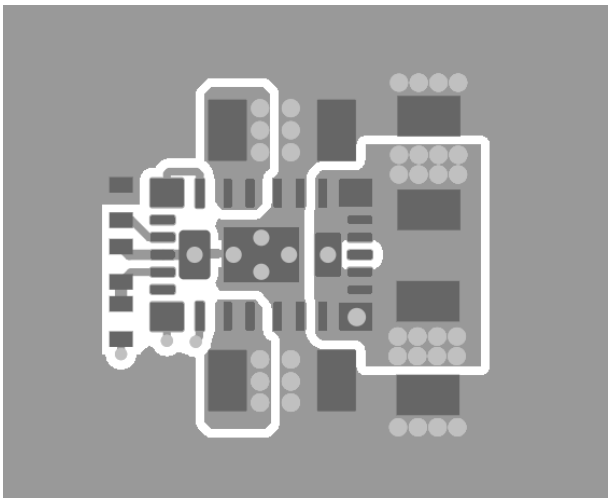


Figure 11-2. Typical Top Layer

11.2.1 Package Specifications

Table 11-1. Package Specifications Table

TPSM63602		Value	Unit
Weight		123	mg
Flammability	Meets UL 94 V-0		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	84	MHrs

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current from 2 A to 6 A, the TPSM63602, TPSM63603, TPSM63604, and TPSM63606 family of synchronous buck power modules specified in Table 12-1 provides flexibility, scalability and optimized solution size for a range of applications. These modules enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include pseudo-random spread spectrum (PRSS), RBOOT-configured switch-node slew rate control, and integrated input bypass capacitors. All modules are rated for an ambient temperature up to 105°C.

Table 12-1. Synchronous Buck DC/DC Power Module Family

DC/DC Module	Rated I_{OUT}	Package	Dimensions	Features	EMI Mitigation
TPSM63602	2 A	B0QFN (30)	4.0 × 6.0 × 1.8 mm	RT adjustable f_{SW}, external synchronization	PRSS, RBOOT, integrated input and BOOT capacitors
TPSM63603	3 A				
TPSM63604	4 A	B3QFN (20)	5.0 × 5.5 × 4.0 mm		PRSS, RBOOT, integrated input, VCC and BOOT capacitors
TPSM63606	6 A				

For development support, see the following:

- TPSM63602 *Quickstart Calculator*
- TPSM63602 *Simulation Models*
- *TPSM63603 and TPSM63603S EVM User's Guide*
- *TPSM63603 Altium Layout Design Files*
- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter.

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602, TPSM53603, and TPSM53604 for Negative Output Inverting Buck-Boost Applications* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM63602RDHR	ACTIVE	B0QFN	RDH	30	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	63602	Samples
TPSM63602V3RDHR	ACTIVE	B0QFN	RDH	30	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	63602V3	Samples
TPSM63602V5RDHR	ACTIVE	B0QFN	RDH	30	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	63602V5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

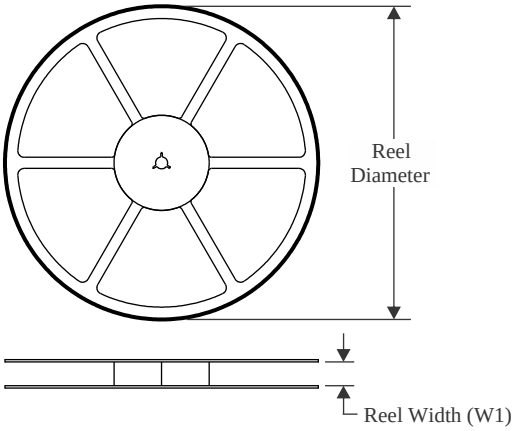
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

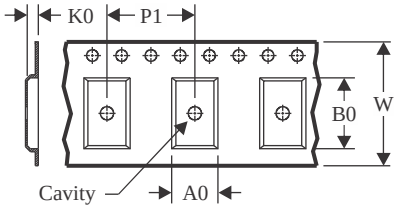
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

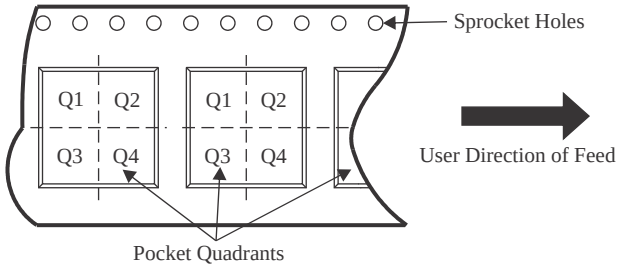


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

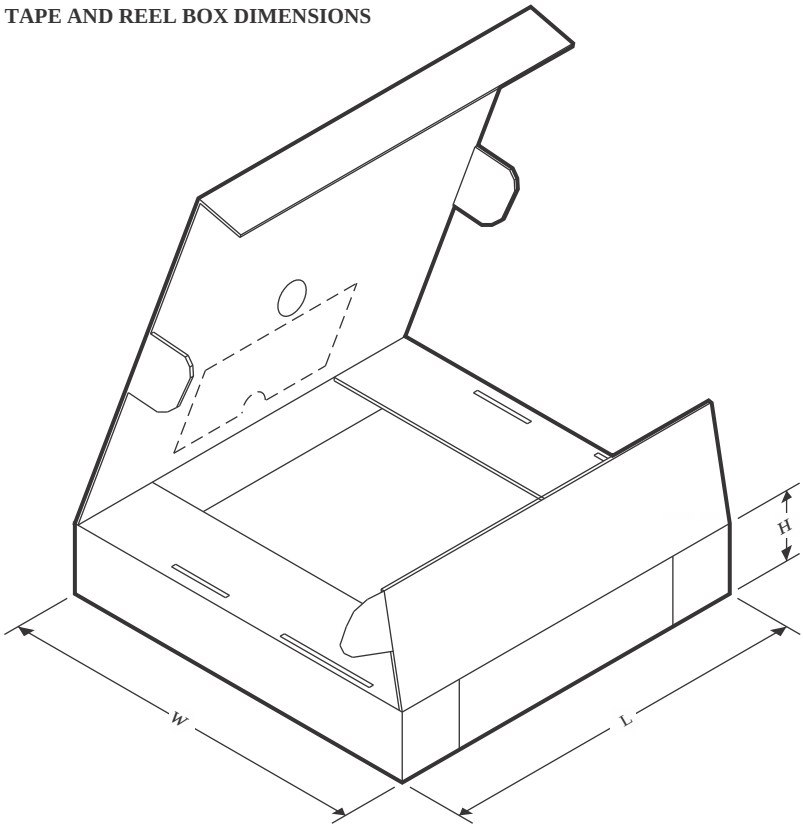
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM63602RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1
TPSM63602V3RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1
TPSM63602V5RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

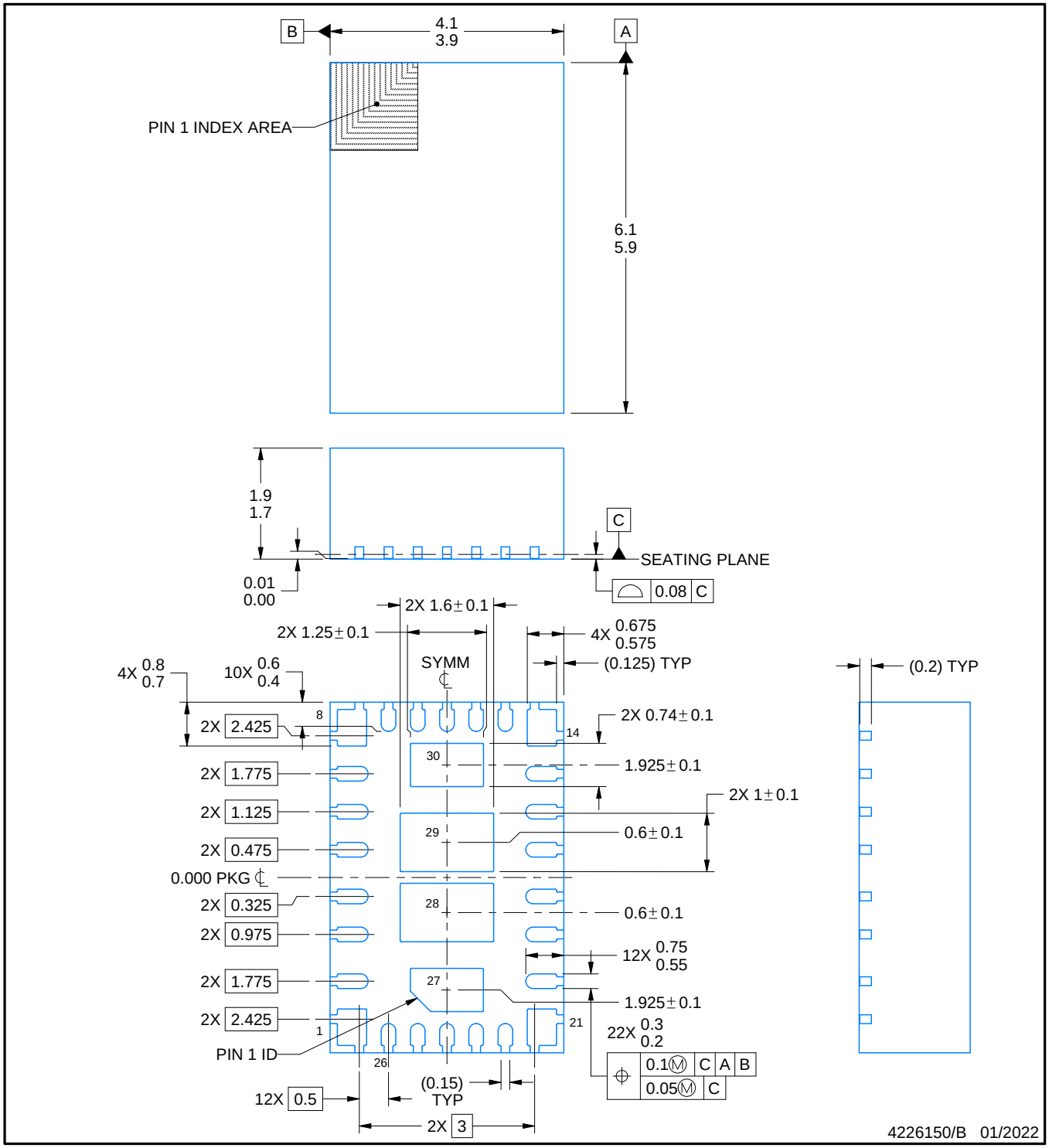
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM63602RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0
TPSM63602V3RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0
TPSM63602V5RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDH0030A

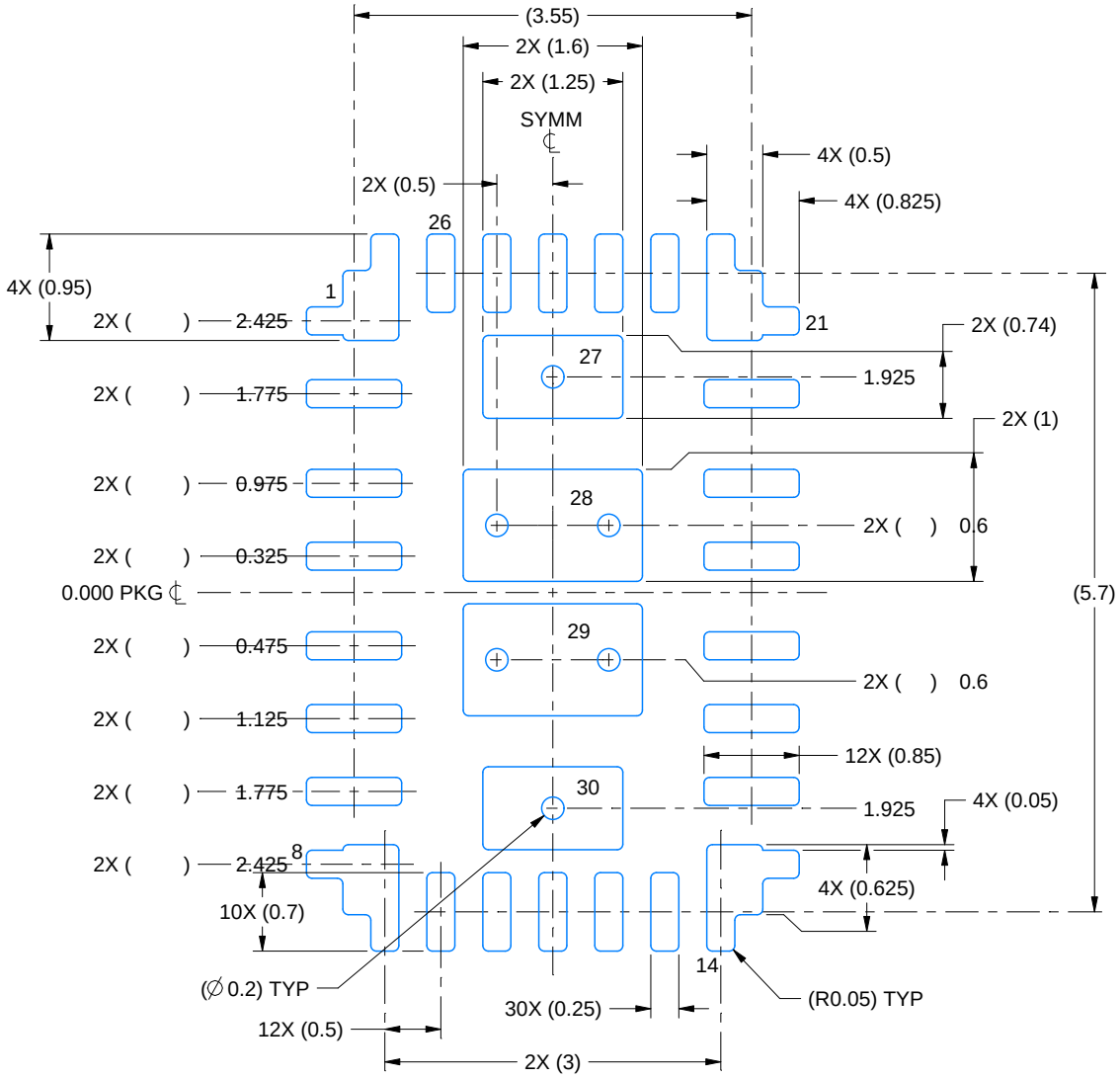
B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

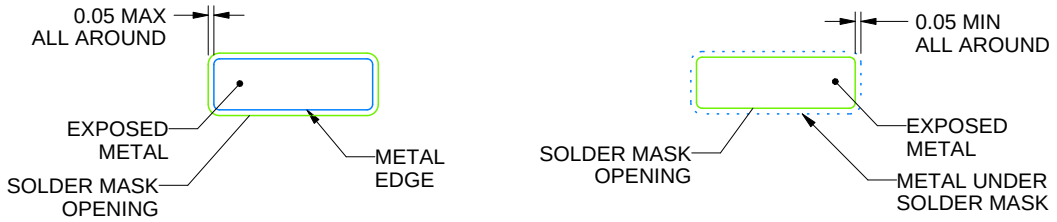


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

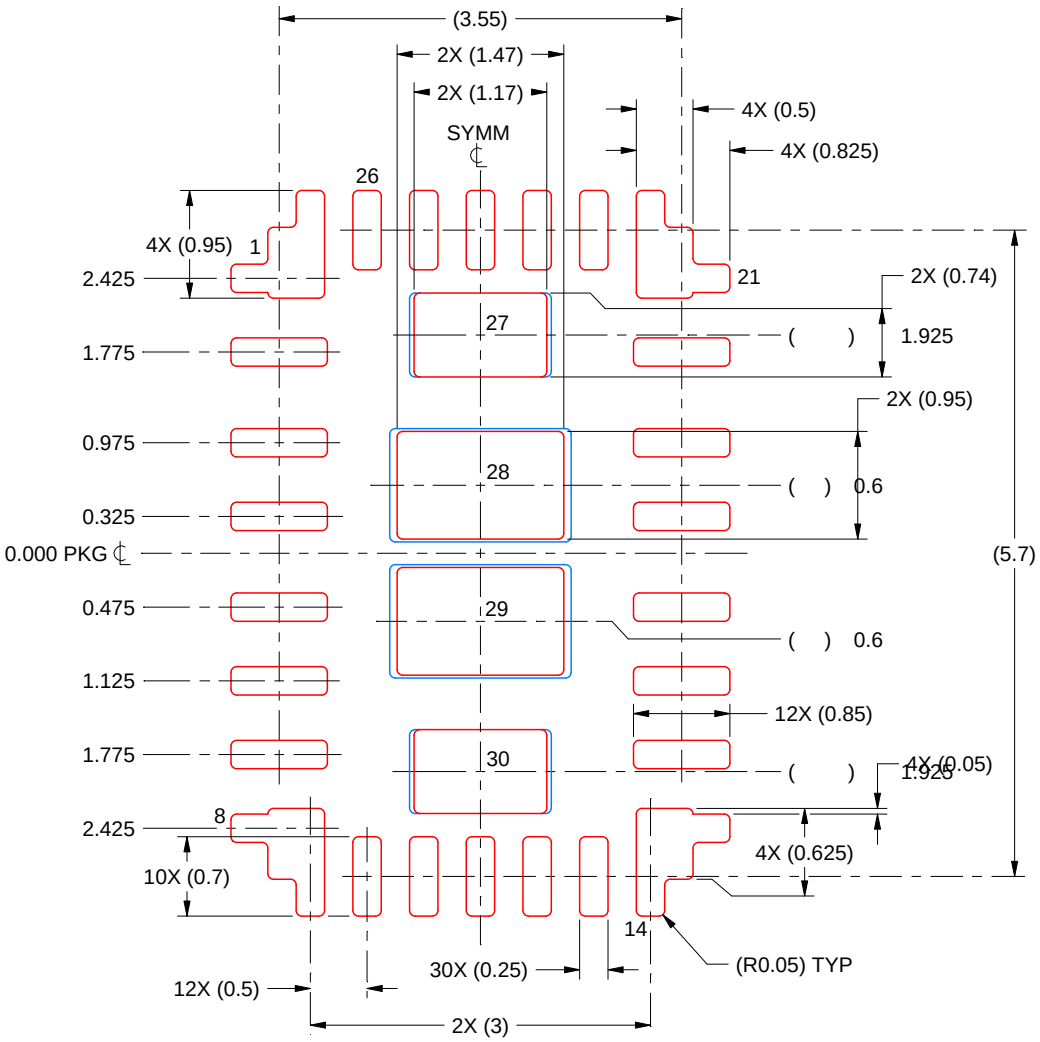


SOLDER MASK DETAILS

4226150/B 01/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 27 & 30:
94% PRINTED SOLDER COVERAGE BY AREA

EXPOSED PAD 28 & 29
87% PRINTED SOLDER COVERAGE BY AREA

SCALE:15X

4226150/B 01/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TUSS4440 Transformer Drive Ultrasonic Sensor IC With Logarithmic Amplifier

1 Features

- Integrated driver for transformer driven transducers and receiver stage with analog output for ultrasound applications
- 86-dB input dynamic range analog front-end
  - First stage low noise amplifier adjustable to 10, 12.5, 15 and 20 V/V
  - Configurable bandpass filter from 40 KHz to 500 KHz
  - Wide-band logarithmic amplifier
- Supported transducer frequencies (controlled by external clock)
  - 40 KHz to 400 KHz
- For low-power applications
  - Standby mode: 1.7 mA (typical)
  - Sleep mode: 220 µA (typical)
- Configurable drive stage:
  - Complimentary low-side drivers with current limit for transformer based transducer excitation
  - Configurable burst patterns using IO1 and IO2 pins
- Outputs:
  - Voltage output of the demodulated echo envelope on VOUT
  - Input signal zero crossing comparator output on OUT3 pin
  - Programmable VOUT threshold crossing on OUT4 pin
- Serial Peripheral Interface (SPI) for configuration by microcontroller (MCU)

2 Applications

- Position sensor
- Level transmitter
- Proximity sensor

3 Description

The TUSS4440 is a highly integrated transformer drive analog front end for industrial ultrasonic applications. The transducer drive stage consists of low-side complementary drivers that can be configured to drive an ultrasonic transducer through a step-up transformer. The device delivers constant current to the primary side of the transformer.

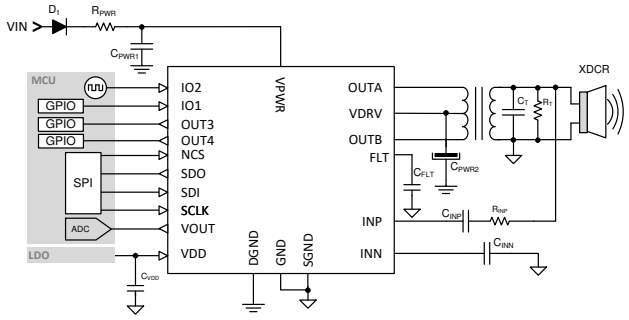
The receive signal path includes a low-noise linear amplifier, a bandpass filter, followed by a logarithmic gain amplifier for input dependent amplification. The logarithmic amplifier allows for high sensitivity for weak echo signals and offers excellent input dynamic range over full range of reflected echoes.

The drivers can be controlled directly through the microcontroller for complete customization of the burst signal, or can be programmed through SPI with a customizable burst length. The TUSS4440 can support a single transducer to send and receive burst signals, or can set up two transducers to split the send and receive functions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSS4440	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TUSS4440 Application Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2018) to Revision A (May 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed all instances of legacy terminology to controller and peripheral where SPI is mentioned	1
• Changed operating free-air temperature minimum from: –25°C to: –40°C	4

5 Pin Configuration and Functions

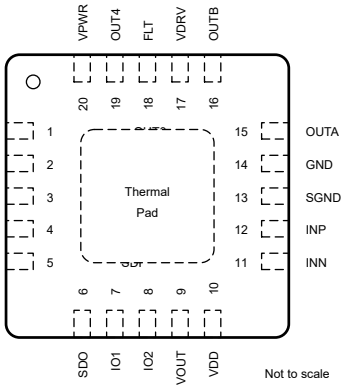


Figure 5-1. RTJ Package 20-Pin WQFN With Exposed Thermal Pad (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT3	I	General-purpose digital output
2	DGND	G	Digital ground
3	NCS	I	SPI negative chip select
4	SCLK	I	SPI CLK
5	SDI	I	SPI data input
6	SDO	O	SPI data output
7	IO1	I	General-purpose digital input
8	IO2	I	General-purpose digital input
9	VOUT	O	Demodulated echo analog output
10	VDD	P	Voltage regulator input
11	INN	I	Negative transducer receive
12	INP	I	Positive transducer receive
13	SGND	G	Sensor ground (quiet)
14	GND	G	Ground
15	OUTA	O	Transducer driver output A
16	OUTB	O	Transducer driver output B
17	VDRV	P	Center tap for transformer
18	FLT	I/O	Filter components
19	OUT4	O	General-purpose digital output
20	VPWR	P	Input supply voltage

(1) I = input, O = output, I/O = input and output, G = ground, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VPWR}	Supply voltage range	–0.3	40	V
V_{VDD}	Voltage regulator input voltage	–0.3	5.5	V
V_{VDRV}	Transformer center-tap voltage	–0.3	V_{VPWR} + 0.3	V
V_{FLT}	Filter component pin	–0.3	V_{VDD} + 0.3	V
V_{INX}	INP, INN pins input voltage	0.5	1.3	V
V_{DIG_IN}	SCLK, SDI, NCS, IOx pin input voltage	–0.3	V_{VDD} + 0.3	V
V_{VOUT}	Analog output voltage	–0.3	V_{VDD} + 0.3	V
V_{DIG_OUT}	SDO, OUTx, IOx pin output voltage	–0.3	V_{VDD} + 0.3	V
V_{OUTA_B}	OUTA, OUTB pins output voltage	–0.3	50	V
T_A	Ambient temperature	–40	105	°C
T_J	Junction temperature	–40	125	
T_{stg}	Storage temperature	–40	125	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage on VPWR pin, internal regulation on VDRV enabled (VDRV_HI_Z=0)	5		36	V
	Supply voltage on VPWR pin, internal regulation on VDRV disabled (VDRV_HI_Z=1), VPWR connected to the center tap of the transformer(1)	5		24	V
V_{VDIG_IO}	Digital I/O pins	–0.1		V_{VDD}	V
V_{VDD}	Regulated voltage Input	3.1		5.5	V
I_{VPWR_INDIR}	Current consumption at VPWR pin during ranging	150	240	340	µA
I_{VPWR_STDBY}	Current consumption at VPWR in standby mode	50	110	200	µA
I_{VDD_INDIR}	Current consumption at VDD pin during ranging	7	11.5	13	mA
I_{VDD_STDBY}	Current consumption at VDD in standby mode	1.2	1.5	2.5	mA
I_{VDD_SLEEP}	Current consumption in sleep mode			350	µA
T_A	Operating free-air temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

(1) Always $V_{VPWR} > V_{VDRV}$ + 0.3 V to prevent reverse current from VDRV pin to VPWR pin

6.4 Thermal Information

THERMAL METRIC[1]		TUSS4440 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power-Up Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PWR_ON}	Time to power up when SPI communication is possible				10	ms
V_{VDRV}	Regulated voltage on VDRV pin[1]	VDRV_VOLTAGE_LEVEL = 0x0; V_{VPWR} > V_{VDRV} + 100 mV	4.5	5	5.3	V
		VDRV_VOLTAGE_LEVEL = 0x4; V_{VPWR} > V_{VDRV} + 100 mV	8.1	9	9.9	
		VDRV_VOLTAGE_LEVEL = 0x7; V_{VPWR} > V_{VDRV} + 100 mV	11.5	12	12.6	
		VDRV_VOLTAGE_LEVEL = 0x8; V_{VPWR} > V_{VDRV} + 100 mV	12.09	13	13.91	
		VDRV_VOLTAGE_LEVEL = 0xC; V_{VPWR} > V_{VDRV} + 100 mV	15.81	17	18.9	
		VDRV_VOLTAGE_LEVEL = 0xD; V_{VPWR} > V_{VDRV} + 100 mV	16.74	18	19.26	
		VDRV_VOLTAGE_LEVEL = 0xE; V_{VPWR} > V_{VDRV} + 100 mV	17.67	19	20.33	
		VDRV_VOLTAGE_LEVEL = 0xF; V_{VPWR} > V_{VDRV} + 100 mV	19.0	20	21.4	
I_{VDRV}	VDRV capacitor charging current	VDRV_CURRENT_LEVEL = 0x0; V_{VPWR} > V_{VDRV} + 1 V	8.5	10	11.5	mA
		VDRV_CURRENT_LEVEL = 0x1; V_{VPWR} > V_{VDRV} + 1 V	17	20	23	

(1) Other VDRV voltage levels possible.

6.6 Transducer Drive

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CLAMP}	Current clamping range		50		500	mA
I_{LIMIT_LOW}	Minimum value on OUTA/OUTB during bursting for linear operation of current limit (headroom)		2			V
I_{CLAMP_ADJ}	Current clamping adjustment steps			64		

6.7 Receiver Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{LNA}	Low-noise amplifier fixed gain	LNA_GAIN = 0x00; f_{DRV_CLK} = 58 KHz	13.7	15	16.8	V/V
G_{LNA}		LNA_GAIN = 0x01; f_{DRV_CLK} = 58 KHz	9.4	10	12	
G_{LNA}		LNA_GAIN = 0x10; f_{DRV_CLK} = 58 KHz	17.6	20	21.8	
G_{LNA}		LNA_GAIN = 0x11; f_{DRV_CLK} = 58 KHz	11.6	12.5	14.2	
DR_{VIN_MIN}	Minimum receive input(2)	LOGAMP_DIS_FIRST=0x0;LOGAMP_DIS_LAST=0x0 LNA_GAIN=0x00; ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500KHz		2.4		µVrms
DR_{VIN_MAX}	Maximum receive input(2)			48		mVrms
SL_{AFE}	Slope of analog front end(4)	VOUT_SCALE_SEL = 0x0; f_{DRV_CLK} = 58 KHz	25	29.7	33	mV/dB
		VOUT_SCALE_SEL = 0x1; f_{DRV_CLK} = 58 KHz	38	45.1	46	
DR_{AFE}	Receiver path dynamic range (minimum to maximum input) (2)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	82		92	dB
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1 ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500 KHz	59		70	
	Receiver path dynamic Range (noise floor to maximum input) (3)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		84	
BW_{LOG}	Logamp bandwidth	Information only	40		1000	KHz
INT_{LOG}	Intercept point in dBV	LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0; f_{DRV_CLK} = 40 KHz	-108		-97	dBV
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-94		-86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-80		-70	
ERR_{LOG}	Log conformance error	Information only	-3		3	dB
f_{BPF}	Configurable range of center frequency of BPF	BPF_BYPASS = 0x0; BPF_FC_TRIM = 0x0; set by different values of BPF_HPF_FREQ	40		500	KHz
Q_{BPF}	Q of bandpass filter	BPF_BYPASS = 0x0; BPF_Q_SEL = 0x0(1)	3	4	5.2	
R_{LPF}	Internal resistor on FLT pin to ground			6.25		KΩ
V_{O_PDSTL}	Output pedestal level(2)	V_{VDD} = 3.3 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	0.3		0.45	V
		V_{VDD} = 5.0 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0;LOGAMP_DIS_LAST = 0x0	0.45		0.675	

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N\_pk\_pk}$	Output peak-to-peak noise	V_{VDD}=3.3 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x0	50		200	mVpp
		V_{VDD}=5.0 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	75		300	

(1) Other choices of Q possible.
(2) Measured with effectively very large C_{FLT}. Actual minimum signal detectable will depend on $V_{N\_pk\_pk}$. Minimum and maximum input levels are defined by ERR_{LOG}.
(3) Measured with different C_{FLT} values according to Equation 3. Noise floor is set by $V_{N\_PK\_PK}$ in addition to V_{O_PDSTL}.
(4) Slope measured with factory trim at f_{DRV_CLK} = 58 KHz. Slope can be adjusted with LOGAMP_SLOPE_ADJ bits for different f_{DRV_CLK} settings.

6.8 Echo Interrupt Comparator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT_SCALE_SEL = 0x0						
$V_{ECMP\_THR\_0}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.37	0.4	0.43	V
		ECHO_INT_THR_SEL = 0x5	0.56	0.6	0.64	
		ECHO_INT_THR_SEL = 0xA	0.75	0.8	0.85	
		ECHO_INT_THR_SEL = 0xF	0.94	1	1.06	
$V_{ECMP\_HYS\_0}$	Echo interrupt comparator hysteresis		7		68	mV
VOUT_SCALE_SEL = 0x1						
$V_{E\_CMP\_THR\_1}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.56	0.6	0.64	V
		ECHO_INT_THR_SEL = 0x5	0.84	0.9	0.96	
		ECHO_INT_THR_SEL = 0xA	1.13	1.2	1.27	
		ECHO_INT_THR_SEL = 0xF	1.41	1.5	1.59	
$V_{ECMP\_HYS\_1}$	Echo interrupt output threshold level hysteresis		7		68	mV

(1) Other thresholds possible.

6.9 Digital I/O Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_DIGIO}	Digital input high-level	NCS, SDI, SCLK and IOx pins	0.7			V_{VDD}
V_{IL_DIGIO}	Digital input low-level				0.3	V_{VDD}
V_{HYS_DIGIO}	Digital input hysteresis		100			mV
V_{OH_DIGIO}	Digital output high-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = – 1 mA	V_{VDD} – 0.1			V
V_{OL_DIGIO}	Digital output low-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = 1 mA			0.1	V
V_{O_CAP}	Maximum output load capacitance	SDO pin. Information Only			10	pF
R_{PU_DIGIO}	Digital input pullup resistance to VDD	NCS, IO1, IO2 pins	80	100	130	kΩ
R_{PD_DIGIO}	Digital Input pulldown resistance to GND	SCLK, SDI pins	80	100	130	kΩ

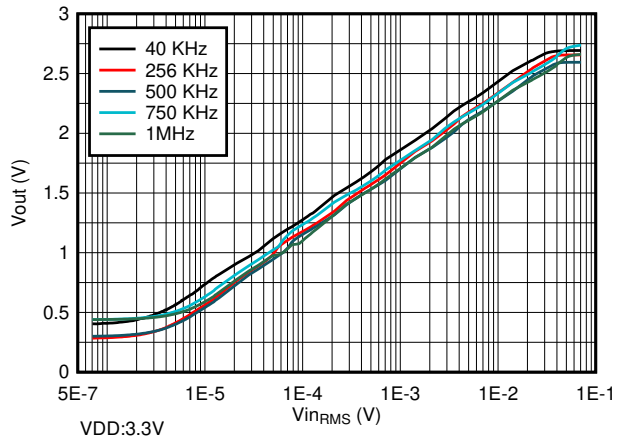
(1) No short-circuit protection on output pins. Damage may occur for currents higher than specified.

6.10 Switching Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

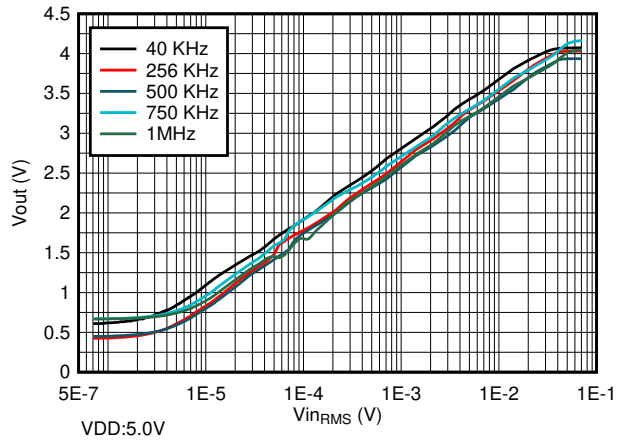
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{DRV_CLK}	Frequency of drive clock on IO1 and IO2 pin	Used as burst frequency	40		400	KHz
SPI_{RATE}	SPI bit rate				500	KHz

6.11 Typical Characteristics



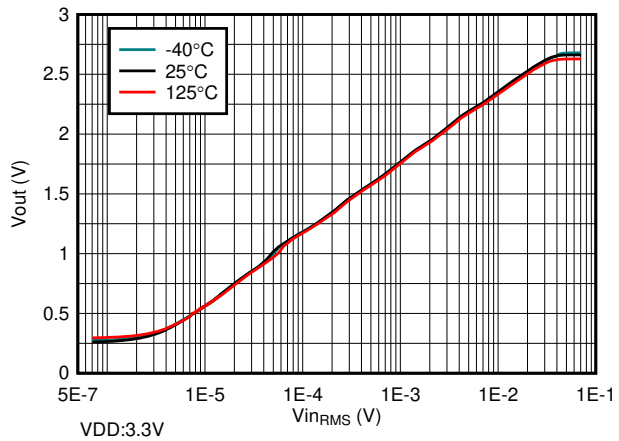
VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-1. Receive Signal Path Transfer Function for VDD = 3.3 V



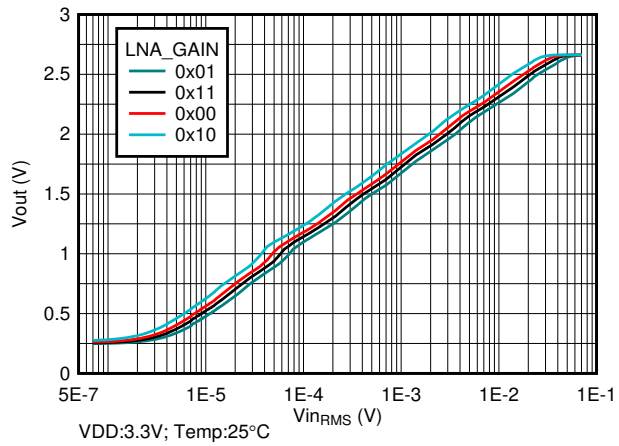
VDD:5.0V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x1
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-2. Receive Signal Path Transfer Function for VDD = 5 V



VDD:3.3V
F_c:256KHz
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-3. Receive Signal Path Transfer Function Across Temperature



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-4. Receive Signal Path Transfer Function Across LNA Gain

6.11 Typical Characteristics (continued)

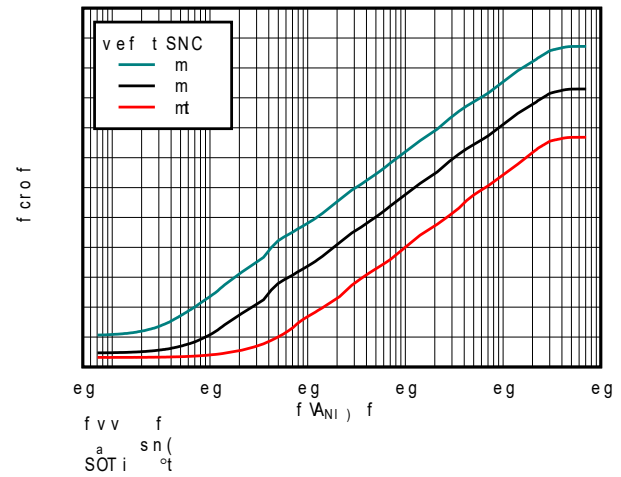
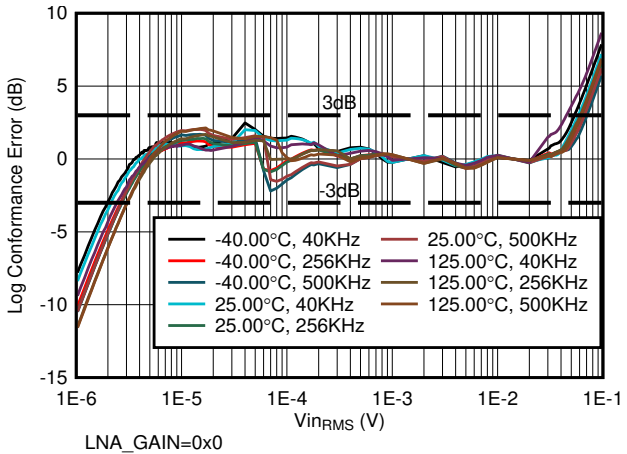
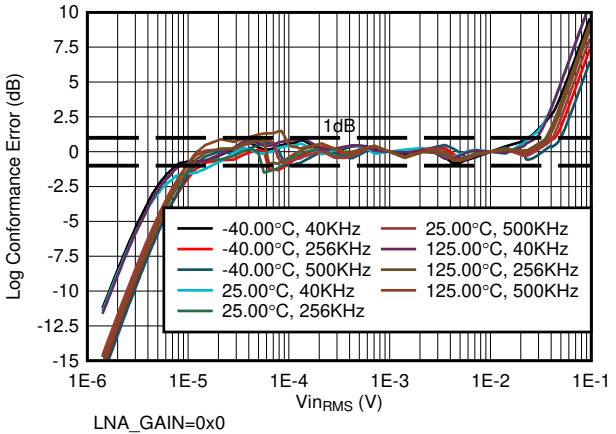


Figure 6-5. Receive Signal Path Transfer Function for Various Logamp Stages Disabled



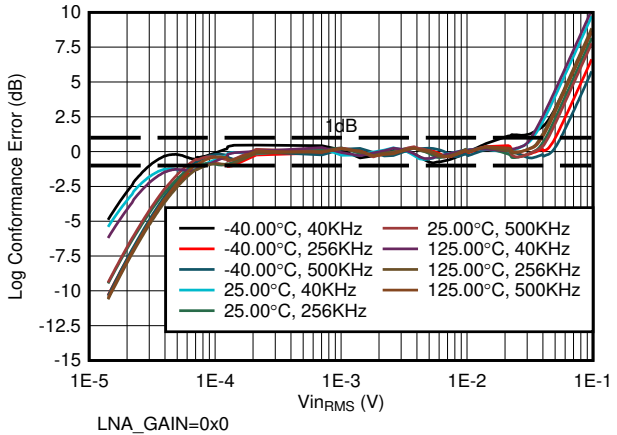
LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-6. Receive Signal Path Log Conformance Error With All Stages Enabled



LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x1

Figure 6-7. Receive Signal Path Log Conformance Error With Last Stage Disabled



LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x1; LOGAMP_DIS_LAST=0x1

Figure 6-8. Receive Signal Path Log Conformance Error With First and Last Stage Disabled

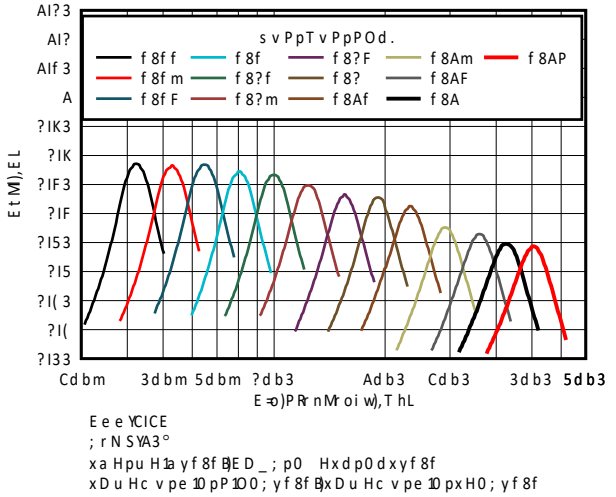
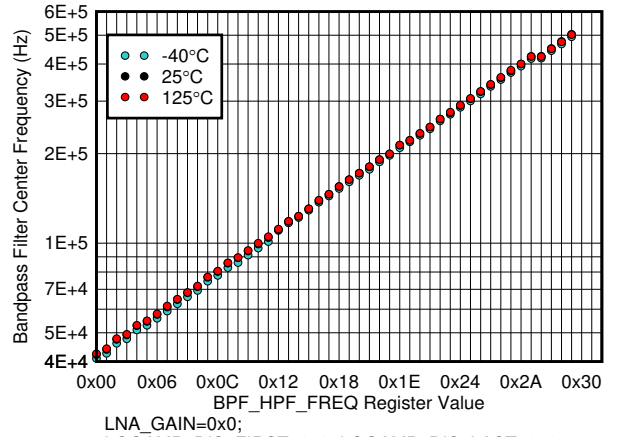


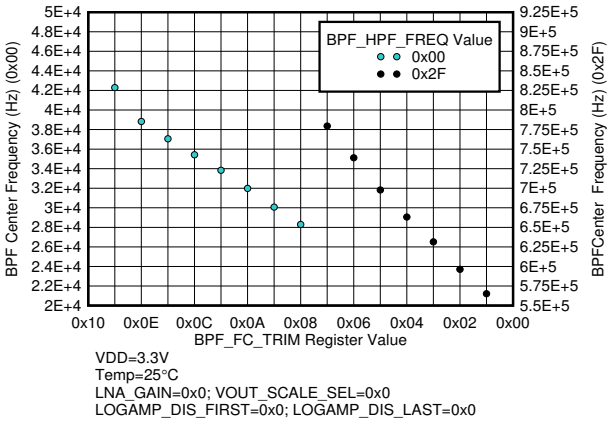
Figure 6-9. Receive Signal Path Bandpass Filter Transfer Function



LNA_GAIN=0x0;
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

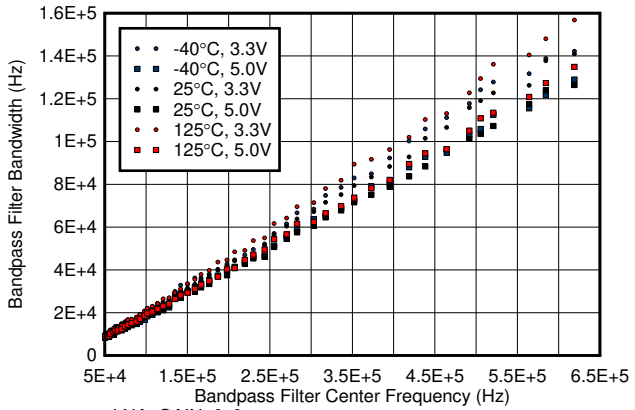
Figure 6-10. Receive Signal Path Bandpass Filter frequency for Various Register Settings

6.11 Typical Characteristics (continued)



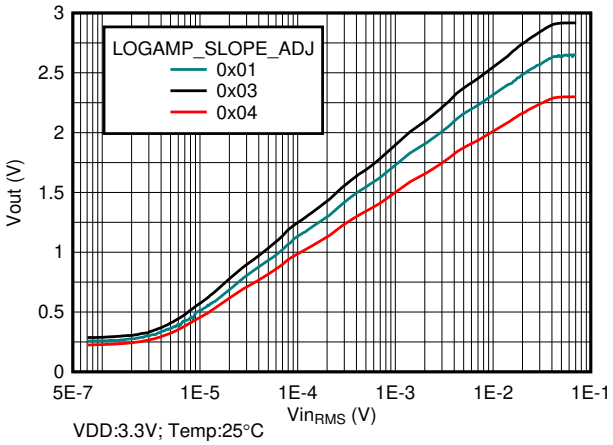
VDD=3.3V
Temp=25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-11. Receive Signal Path Bandpass Filter Center Frequency Trim



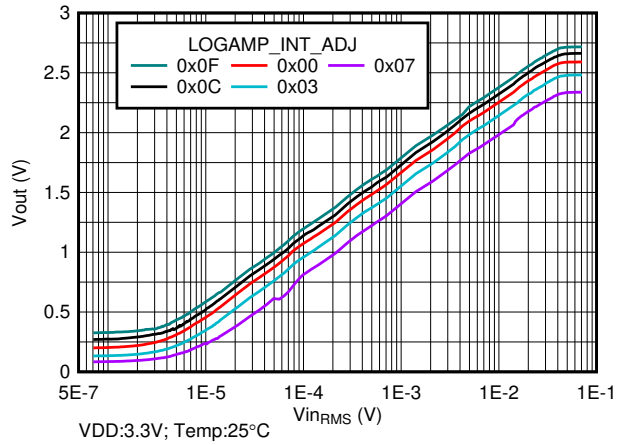
LNA_GAIN=0x0
BPF_Q_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-12. Receive Signal Path Bandpass Filter Bandwidth for Various Center Frequency Settings



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-13. Receive Signal Path Transfer Function for Various Slope Adjustments



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

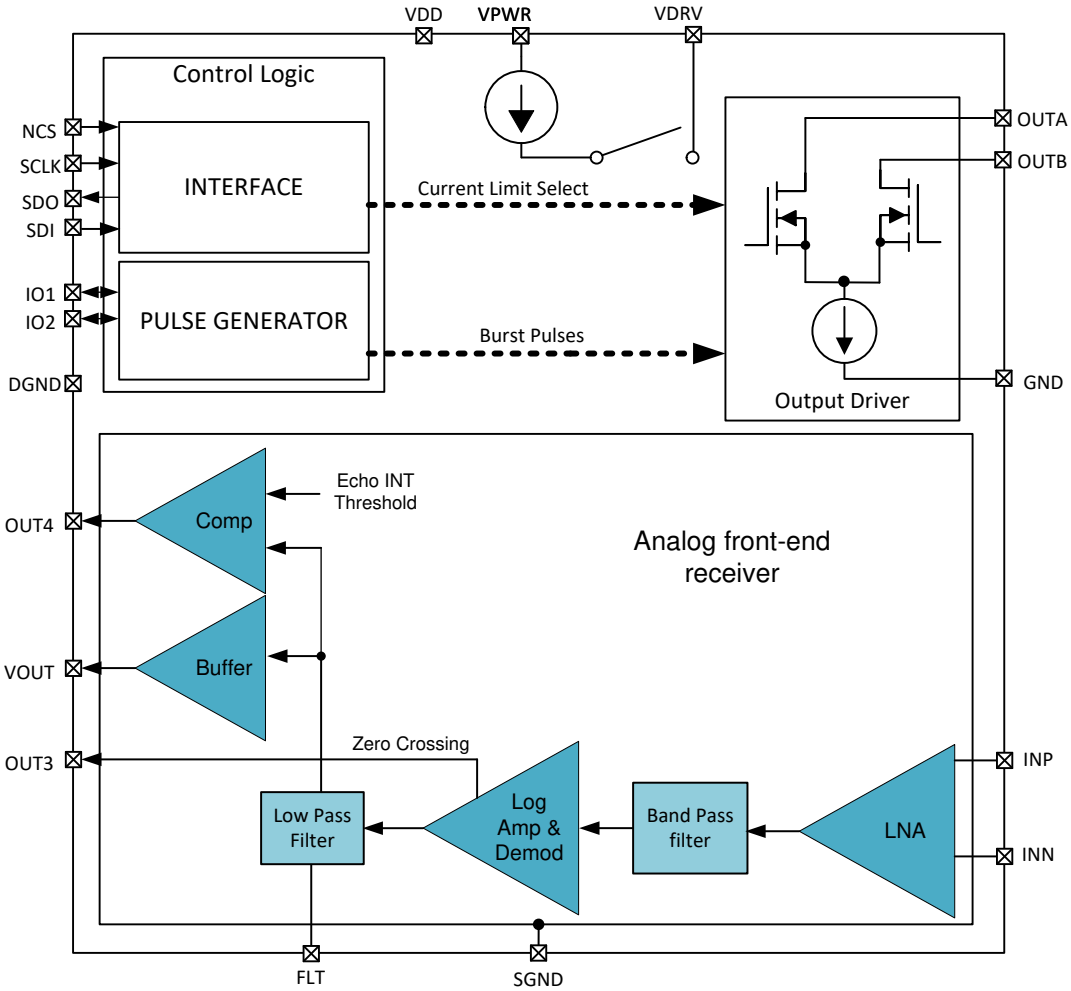
Figure 6-14. Receive Signal Path Transfer Function for Various Intercept Adjustments

7 Detailed Description

7.1 Overview

The TUSS4440 is a highly integrated driver and receiver IC designed especially for ultrasonic transducers operating between the range of 40 KHz to 1 MHz. The TUSS4440 integrates low-side complimentary FETs that can excite a ultrasonic transducer through a transformer. The transformer allows the user to step up the driving voltage to get higher sound pressure level. The The driver stage has flexible and configurable controls set through the SPI interface or through digital input pins that can be driven by an external MCU. The receive stage consists of a logarithmic amplifier receive chain. The logamp enables the TUSS4440 to have a wide dynamic input range. This enables applications where objects with different physical properties must be detected with the same sensor. A key advantage of the TUSS4440 is that it integrates a bandpass filter that can be tuned to the center frequency of the transducer. A demodulated analog output representing the receive echo, the zero crossing of the input signal, and a simple threshold crossing indicator enable a variety of end applications from complex object detection to simple presence detection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excitation Power Supply (VDRV)

The TUSS4440 device includes a current source which charges a capacitor connected to the VDRV pin. The VDRV pin serves as the power supply for the center tap of the transformer . The voltage on the VDRV pin (V_{VDRV}) is controlled by an internal voltage monitor which can be configured by the VDRV_VOLTAGE_LEVEL

bits. The current source is switched off after VDRV pin voltage crosses the configured V_{VDRV} value. The charging current (I_{VDRV}) can be configured using VDRV_CURRENT_LEVEL bits.

The use of VDRV pin has two advantages:

- It allows device to be used in applications where VPWR values can violate absolute maximum parameter for the OUTA / OUTB pins.
- In applications where VPWR can vary over a wide range, this allows the transducer drive voltage to be fixed for every burst for a deterministic sound pressure level created by the transducer. This is possible only when the minimum supply voltage on the VPWR pin is greater than the configured value of V_{VDRV}

The VDRV regulation is disabled at device power up indicated by VDRV_HI_Z bit being set. To enable VDRV this bit must be cleared. This feature enables applications where the center tap of transformer is connected to a separate power supply source.

Note

- When VDRV pin is supplied from an external power supply, it must be ensured that all times including during power up, $V_{VPWR} > V_{VDRV} + 0.3$ V to prevent any reverse current from VDRV pin to VPWR pin. Alternatively a reverse current prevention diode can be used on VPWR pin as shown in Figure 8-1 (D1).
- Very fast ramp-up rate on VPWR pin should be avoided to prevent damage to the device. If fast ramp rates are possible, a series resistor between power supply and VPWR pin as shown in Figure 8-1 (R_{PWR}) is recommended.

After a burst is completed and during the long receive time (listen mode), the capacitor on VDRV pin will discharge causing the charging current to turn on intermittently. This can inject switching noise which can be picked by the analog front end as a spurious echo. To eliminate this noise, the DIS_VDRV_REG_LSTN bit can be set. This disables charging of VDRV automatically after the burst is done. The VDRV charging current can be turned on again by setting the VDRV_TRIGGER bit. Setting this bit may create a spurious echo which can be ignored by the echo processing in the MCU. The VDRV_READY bit in DEV_STAT register can be monitored to know when the required voltage level has been reached and the device is ready to generate a new burst. The VDRV_TRIGGER bit must be un-set through SPI just before the start of burst and will have to be set again for next charging cycle. If the VDRV_TRIGGER bit is not un-set before next burst cycle, the VDRV charging current will not be automatically disabled after the burst even when DIS_VDRV_REG_LSTN is set. This functionality is ignored when the VDRV_HI_Z bit is set.

7.3.2 Burst Generation

TUSS4440 has multiple modes to excite the transducer through OUTA and OUTB pins. For each of the modes, the desired frequency of burst is supplied through an external clock on the IOx pins. This enables the user to supply a highly precise clock calibrated to the center frequency of transducer to enable the highest sound pressure level generation. These modes can be selected by the IO_MODE bits in the DEV_CTRL_3 register.

The burst mode is enabled first, then the start of burst (OUTA/OUTB changing states) happens at the next falling edge of IO1 or IO2, depending on the mode selected. These modes are described below.

- **IO_MODE = 0:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled by setting the CMD_TRIGGER in the TOF_CONFIG register through SPI, as shown in Figure 7-1. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. The end of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent, or when the CMD_TRIGGER = 0 is set through SPI, whichever occurs earlier. TI recommends that IO2 is held high before burst enable to count the number of pulses correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of CMD_TRIGGER from high to low to high again is required to initiate a new burst sequence.

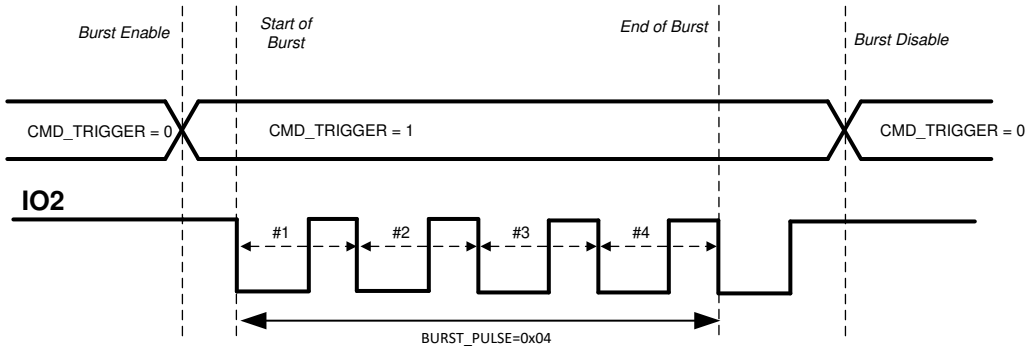


Figure 7-1. IO_MODE 0 Description

- **IO_MODE = 1:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled when IO1 pin transitions low (see Figure 7-2). The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent or IO1 transitions high, whichever occurs earlier. TI recommends that IO2 is held high before start of burst to count the number of pulse correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of IO1 from low to high to low again is required to initiate a new burst sequence.

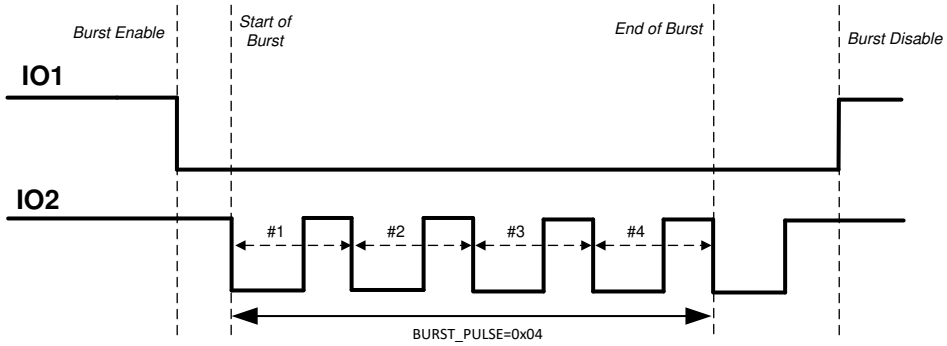


Figure 7-2. IO_MODE 1 Description

- **IO_MODE = 2:** In this mode both IO1 and IO2 are used to control OUTA and OUTB. The burst enable is triggered when either IO1 or IO2 transitions from high to low. Start of burst (OUTA and OUTB changing state) happens only at the next falling edge of IO1. Figure 7-3 shows the case where a high-to-low transition on IO2 is used to enable the burst. A burst is emulated when IO1 and IO2 are toggled in a non-overlapping sequence. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. During a burst, if there is a condition where both IO1 and IO2 are high for more than half period of the internal clock f_{INT_CLK} (caused by differential delays due to PCB parasitics or MCU code), an end of burst and burst mode disable will be triggered. Any falling edge just after this condition will be ignored to toggle OUTA and OUTB as it would be considered as a new burst enable signal. A systematic condition of overlap can cause a continuous end of burst trigger such that OUTA and OUTB do not toggle even though IO1 and IO2 are toggling. TI recommends no overlap or minimum non-overlap between the IO1 and IO2 signals when measured at the pins. BURST_PULSE has no effect in this mode.

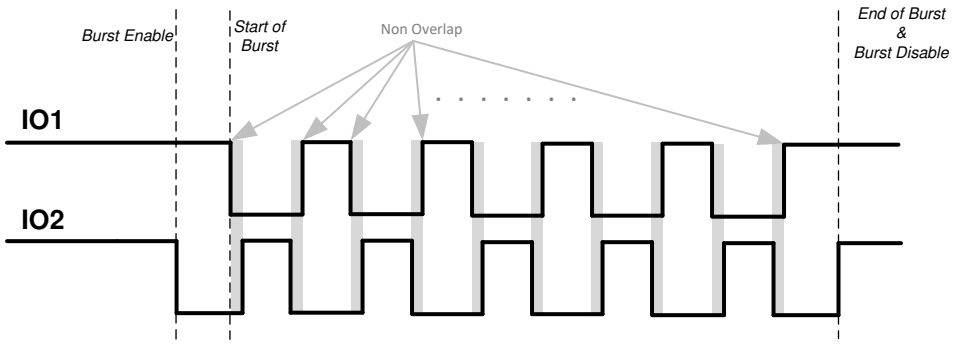


Figure 7-3. IO_MODE 2 Description

- **IO_MODE = 3:** In this mode, burst enable and start of burst are both triggered by the falling edge of IO2. TI recommends that IO2 pin is kept pulled up to VDD for this mode. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins (see Figure 7-4). The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent. After end of burst, a blank-out timer interval defined by the DRV_PLS_FLT_DT register is started to prevent triggering of a new start of burst in the event if the IO2 pin is still toggling. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins.

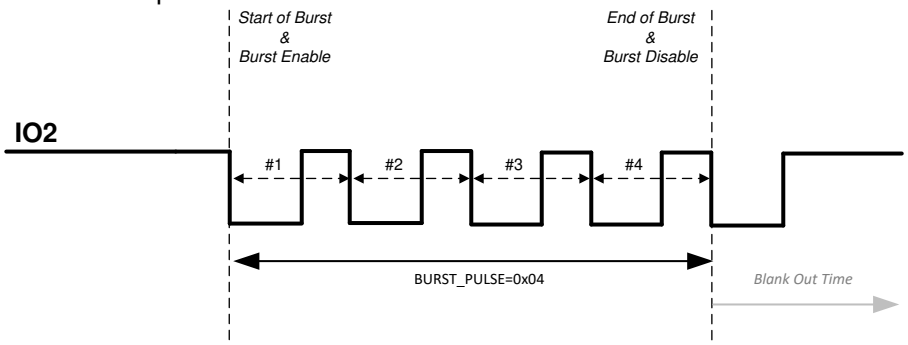


Figure 7-4. IO_MODE 3 Description

Note

- For IO_MODE 0 and 1, by setting BURST_PULSE = 0, the device will generate continuous burst pulses on OUTA and OUTB until the end of burst is signaled through SPI or the IO1 pin, respectively. Continuous bursting is not available for IO_MODE=3.
- A higher noise floor at the VOUT pin is expected in continuous mode where one transducer is used to transmit burst signals and another transducer is used to receive, as the switching noise of the digital IO pins can couple into the highly sensitive analog front end for the receive channel. This also applies to the single transducer use case where a continuous clock is applied on IO2 pin when the device is in indirect or listening mode.
- The range for frequency of switching for the output drivers is given by f_{DRV_CLK} parameter in the *Switching Characteristics* table.
- When the device is not in direct sensing or bursting mode, the device is always in indirect sensing or listening mode.

7.3.2.1 Burst Generation Diagnostics

In IO_MODE 0, 1 and 3, a pulse number diagnostic is active after start of burst (not when the burst is enabled) to monitor if the correct number of pulses (as set in BURST_PULSE) were generated before the end of burst was signaled through SPI or the IO1 pin. A fault, if detected, is then reported through the PULSE_NUM_FLT bit.

The pulse duration after start of burst (not when the burst is enabled) is monitored to detect a stuck condition, which will keep the FETs on OUTA or OUTB turned on. This can happen because of loss of external clock

or the driving signal on IO1 and IO2 pins being stuck in one state. The device expects to see a toggle on IOx pins (based on IO_MODE) within the time period as defined in the DRV_PLS_FLT_DT register. If this diagnostic triggers, it will force an end of burst. The fault is reported by setting the DRV_PULSE_FLT bit. If a DRV_PULSE_FLT is set in IO_MODE 0, 1 and 3—and the programmed number of pulses were not sent before end of burst—the PULSE_NUM_FLT will also be set.

Note

- The DRV_PULSE_FLT bit is cleared when a new start of burst is triggered, when DRV_PLS_FLT_DT = 0x7 is set, or if the device is put into Standby or Sleep mode.
- The PULSE_NUM_FLT bit is cleared when a new start of burst is triggered, or if the device is put into Standby or Sleep mode.

7.3.3 Transformer Transducer Drive

The device provides burst generation by exciting the primary side of a step-up transformer connected at the OUTA / OUTB pins. The VDRV pin is used as the power supply source. Figure 7-5 shows the TUSS4440 device transformer drive block diagram when using a center-tap transformer. The drive stage in the TUSS4440 is realized as two low-side N-Channel power FETs. The current limit control block tries to drive current efficiently into the primary side of the transformer to achieve the maximum swing (set by voltage on the center tap and turn ratio of the transformer) on the secondary side. The secondary side total resistance, turn ratio, and the required peak-to-peak voltage will set the minimum value that will drive the OUTA/OUTB pin for a given set current limit. The current limit block supports multiple current levels selected by the XFMR_DRV_ILIM bits. The voltage on VDRV pin can be set as described in the *Excitation Power Supply (VDRV)* section.

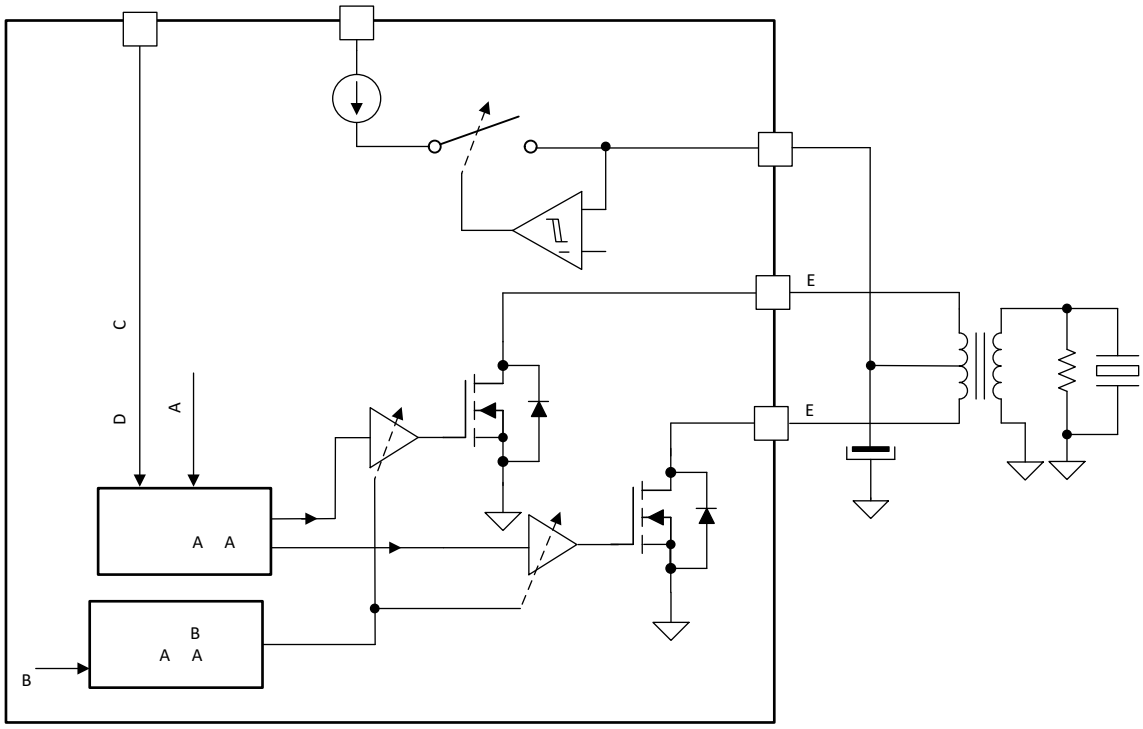


Figure 7-5. TUSS4440 Center-Tap transformer drive.

For a center-tap transformer configuration, the TUSS4440 will drive the low-side FETs in an out-of-phase manner. The device also supports a single primary coil transformer configuration where the FETs are driven in-phase. This is done by setting the HALF_BRG_MODE bit. In this mode, the effective current limit remains the same as set in XFMR_DRV_ILIM. Refer to *Application and Implementation* for an application diagram and information on how the polarity and state of the OUTA and OUTB pins are defined with respect to the IO1 and IO2 pin states and other register settings.

Note

For a center-tap transformer, the voltage swing on OUTA and OUTB can be as high as 2 × V_{VDRV}. If the center tap of the transformer is connected directly to VPWR, then it must be ensured that the maximum voltage on OUTA and OUTB pins do not go above the absolute maximum limits.

7.3.4 Analog Front End

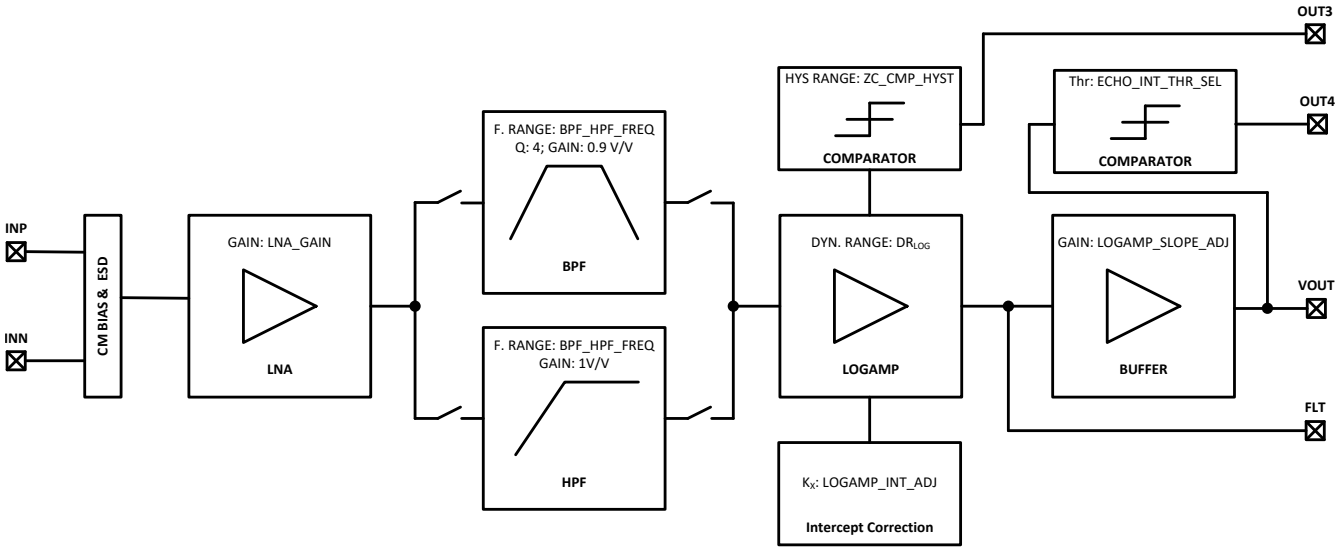


Figure 7-6. TUSS4440 Analog Front-End Block Diagram

Figure 7-6 shows the analog front-end block diagram that can receive and condition the signals from the transducer during listen mode. The received echo is first amplified with a fixed linear low-noise amplifier, followed by either a bandpass filter or a high-pass filter to remove noise out of the expected signal band. After filtering the signal, the signal is fed into a logarithmic amplifier. The output of the logarithmic amplifier is then buffered to the VOUT pin. In Figure 7-6, every block has the register name associated with it that can be used to configure the signal path. The final equation for the signal path is given by Equation 2:

$$V_{OUT} = G_{VOUT} \cdot SL_{LOG} \cdot G_{LNA} \cdot G_{BPF} \cdot 20\log_{10}\left(\frac{V_{IN} \cdot G_{LNA} \cdot G_{BPF}}{INT_{LOG} \cdot K_X}\right) \quad (1)$$

where

- G_{VOUT} is set by the LOGAMP_SLOPE_ADJ bits.
- SL_{LOG} is slope of logarithmic amplifier as specified in the *Receiver Characteristics* table.
- G_{LNA} is set by the LNA_GAIN bits.
- G_{BPF} is typically 0.9V/V.
- V_{IN} is the input V_{INP}
- INT_{LOG} is logarithmic amplifier intercept specified in the *Receiver Characteristics* table.
- K_X is the log intercept adjustment set by the LOGAMP_INT_ADJ bits.

The bandpass filter is critical for reducing noise to allow utilization of the complete dynamic range of the logarithmic amplifier. The center frequency of the bandpass filter can be configured to be close the transducer frequency which is set by the BPF_HPF_FREQ bits. Table 7-1 shows the nominal values for the BPF center frequency corresponding to the BPF_HPF_FREQ register value. The TUSS4440 supports a wide range of frequencies, therefore a factory trim is used to remove process variation for a particular pre-determined frequency. It is possible that all other frequencies listed in Table 7-1 do not correspond exactly to value of BPF_HPF_FREQ in a factory trim. The user can vary the value of the BPF_HPF_FREQ register around the desired center frequency while actively bursting and observing the VOUT signal. The value with maximum voltage at VOUT pin will the desired setting for the BPF_HPF_FREQ register.

Table 7-1. Bandpass Filter Center Frequency Configuration

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x00	40.64
0x01	44.05
0x02	45.6
0x03	48.86
0x04	50.58
0x05	52.96
0x06	56.75
0x07	60.11
0x08	62.95
0x09	66.68
0x0A	71.44
0x0B	74.81
0x0C	79.24
0x0D	82.03
0x0E	86.89
0x0F	92.04
0x10	97.49
0x11	103.27
0x12	109.4
0x13	114.54
0x14	121.33
0x15	128.52
0x16	134.58
0x17	142.55
0x18	151.01
0x19	159.94
0x1A	167.48
0x1B	177.41
0x1C	185.77
0x1D	196.78
0x1E	206.05
0x1F	218.26
0x20	228.54
0x21	244.89
0x22	256.43
0x23	271.63
0x24	284.43
0x25	301.28
0x26	319.13
0x27	338.14
0x28	353.97
0x29	374.95
0x2A	397.16
0x2B	408.17
0x2C	420.7

Table 7-1. Bandpass Filter Center Frequency Configuration (continued)

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x2D	455.63
0x2E	472.03
0x2F	500

The factory trim can be overridden by setting the BPF_FC_TRIM_FRC bit first and varying the BPF_FC_TRIM bit after. This is useful in two ways:

- If the factory trimmed bandpass filter center frequency is higher than the desired value for BPF_HPF_FREQ = 0x00, or lower than desired value for BPF_HPF_FREQ = 0x2F, then BPF_FC_TRIM can be used to recover the range.
- This setting can also be used to extend the frequency range of the bandpass filter center frequency.

The BPF_FC_TRIM acts like an offset on top of the BPF_HPF_FREQ setting. Table 7-2 shows the nominal value of center frequency when this offset is added to the minimum and maximum BPF_HPF_FREQ code. Figure 6-11 shows the measured data. For BPF_HPF_FREQ values greater than 0x08 and less than 0x27, varying BPF_FC_TRIM keeping BPF_HPF_FREQ fixed is the same as setting BPF_FC_TRIM = 0x00 and varying BPF_HPF_FREQ to find the optimum setting.

Table 7-2. Bandpass Filter Center Frequency Range Extension

BPF_HPF_FREQ (hex) + BPF_FC_TRIM (hex) (BPF_FC_TRIM_FRC = 1)	BPF_F_c (KHz)
0x00 + 0x8	27.48
0x00 + 0x9	29.44
0x00 + 0xA	30.83
0x00 + 0xB	31.19
0x00 + 0xC	32.65
0x00 + 0xD	34.19
0x00 + 0xE	35.8
0x00 + 0xF	38.81
0x2F + 0x1	523.56
0x2F + 0x2	554.59
0x2F + 0x3	587.45
0x2F + 0x4	622.23
0x2F + 0x5	651.58
0x2F + 0x6	690.19
0x2F + 0x7	731.09

Note

- The Q factor of the filter is specified in the *Receiver Characteristics* table, and can be selected by the BPF_Q_SEL bits.
- The bandpass filter can also be converted into a high-pass filter by setting the BPF_BYPASS bit for transducer frequencies in the range above what is shown in Table 7-1. The corner frequency for high-pass filter is also controlled by the BPF_HPF_FREQ bits.
- BPF_Q_SEL and BPF_FC_TRIM have no effect when BPF_BYPASS = 1.

The logamp provides compression for large signal inputs and amplifies linearly small signal inputs. Logamp simplifies system design to detect varying strengths of echoes that happens because of difference in reflectivity of different types of objects and objects at different distances. It automatically adjusts its gain based on the input signal level. The logamp also demodulates the incoming signal.

The logamp consists of multiple gain stages and range extension stages that are combined to give a logarithmic response. The current consumption of the device can be reduced by turning off the either the first stage, the last stage of the logamp, or both, by setting the LOGAMP_DIS_FIRST and LOGAMP_DIS_LAST bits. Disabling the stages will reduce the input dynamic range on the lower side of the range (see Figure 6-4). The pedestal noise floor will be lower because the gain stages are disabled, but the minimum detectable signal value becomes higher due to the reduced dynamic range. Depending on the received input signal strength, stages can be disabled to get optimum object detection. For very small inputs, all stages should be enabled to get maximum input dynamic range even though the noise floor is higher. Figure 6-6, Figure 6-7, and Figure 6-8 show the effect on the log conformance error when all stages are enabled, when the last stage is disabled, and when both first and last stages are disabled. When stages are disabled, a lower error is obtained with a lower noise floor, but the input dynamic range is reduced.

At the output of the logamp, the user can apply an adjustment to the intercept of the logamp curve. This is denoted by the K_X factor in Equation 1. The intercept adjustment is controlled by the LOGAMP_INT_ADJ bits. Table 7-3 shows the nominal values of K_X factor corresponding to register values, and Figure 6-14 shows its effect on the transfer function.

Table 7-3. Logamp Intercept Adjustment

LOGAMP_INT_ADJ	K_X
0x00	1
0x01	1.155
0x02	1.334
0x03	1.54
0x04	1.778
0x05	2.054
0x06	2.371
0x07	2.738
0x08	1
0x09	0.931
0x0A	0.866
0x0B	0.806
0x0C	0.75
0x0D	0.698
0x0E	0.649
0x0F	0.604

The output of the logamp is filtered using a low-pass filter to remove the high-frequency components and provide a sufficient peak hold time for the demodulated envelope signal. The cut-off frequency of the low-pass filter is set by the internal impedance of the FLT pin and the value of an external capacitor connected to the pin. As this filter capacitance (C_{FLT}) suppresses the high frequency fluctuations, it also slows down the response time of the logamp. Higher C_{FLT} capacitance will result in lower peak-to-peak voltage variations at VOUT, and slower rise and fall times for the VOUT voltage to reach its maximum value for a given input signal. A nominal value can be calculated using Equation 3, and must be optimized depending on the application.

The output of the low-pass filter is buffered to the VOUT pin using an internal buffer. The buffer is designed to support an ADC input of a MCU. It is possible to change output dynamic range of the VOUT buffer using the VOUT_SCALE_SEL bit. Once the range is set, the gain of the VOUT buffer can be set by the LOGAMP_SLOPE_ADJ bits. The slope variation of the receiver analog front end is show in Figure 6-13.

Echo interrupt signal is available on the OUT4 pin that goes high when the signal on the VOUT pin crosses a threshold as defined by the ECHO_INT_THR_SEL bits. As long as the VOUT signal is higher than this threshold, the echo interrupt signal is held high. The signal goes low asynchronously when the VOUT signal drops below the programmed threshold. This signal can be used to interrupt a MCU when an object has been detected. The threshold value is also dependent on the setting of the VOUT_SCALE_SEL bit.

A zero-crossing signal is output at the OUT3 pin which can be used to validate the frequency of the received echo signal to provide robustness against interference from other signals. This zero-crossing signal is derived from the raw amplified input signal from a particular stage as it is being demodulated in the logamp block. This function is disabled at device power up. but can be enabled by setting the ZC_CMP_EN bit. When enabled, the ZC_CMP_STG_SEL bits are used to select which logamp gain stage is used to generate the zero crossing signal while the ZC_CMP_HYST bits control the hysteresis of the zero-crossing comparator. The stage selection to see the OUT3 pin toggling depends on the strength of signal received by the logamp and has to be configured depending on the application. For large amplitude of input signal, a lower stage of the logamp should be selected, whereas for lower amplitude signal, a higher stage should be selected. To avoid switching noise generated by the toggling of the zero-crossing comparator when the ZC_EN_ECHO_INT bit is set, the zero-crossing output will be only enabled while the echo interrupt signal is high.

7.4 Device Functional Modes

The device has four functional modes:

Sleep Mode — Ultra-low current consumption sleep mode

In this mode, all major blocks of the device are disabled, including VDRV regulation. The SPI interface is still active. This transition into and out of this mode is done using the SLEEP_MODE_EN register bit. Upon issuing a command to exit this mode, the device transitions to other modes only when the VDRV pin reaches the programmed regulation voltage.

Standby Mode — Low current standby mode

In this state, the VDRV regulation is active, but other analog blocks are shut down to reduce quiescent current consumption. The STDBY_MODE_EN bit is used to enter and exit this mode through SPI. The device can transition very quickly from this state to one of the active states for bursting and listening.

Listen Mode — Default mode of the device

This is the default mode of the device when it is not in Sleep mode or Standby mode. In this mode, there is no activity on the transmitter block and the device is actively listening for any ultrasonic signals.

Burst Mode — Mode in which the device is enabled to start a burst to drive the transducer

In this mode, the transmitter blocks are active and enabled to drive the transducer depending on when the start of burst occurs. The receiving path is also active at the same time listening for signals at the input. This mode is entered when a burst enable event occurs and exited when an end of burst occurs as described in *Burst Generation* section.

Figure 7-7 shows an example of the transitions between the different modes of the device for IO_MODE = 0, where the burst is activated through a SPI command and end of burst occurs as the number of programmed pulses are sent.

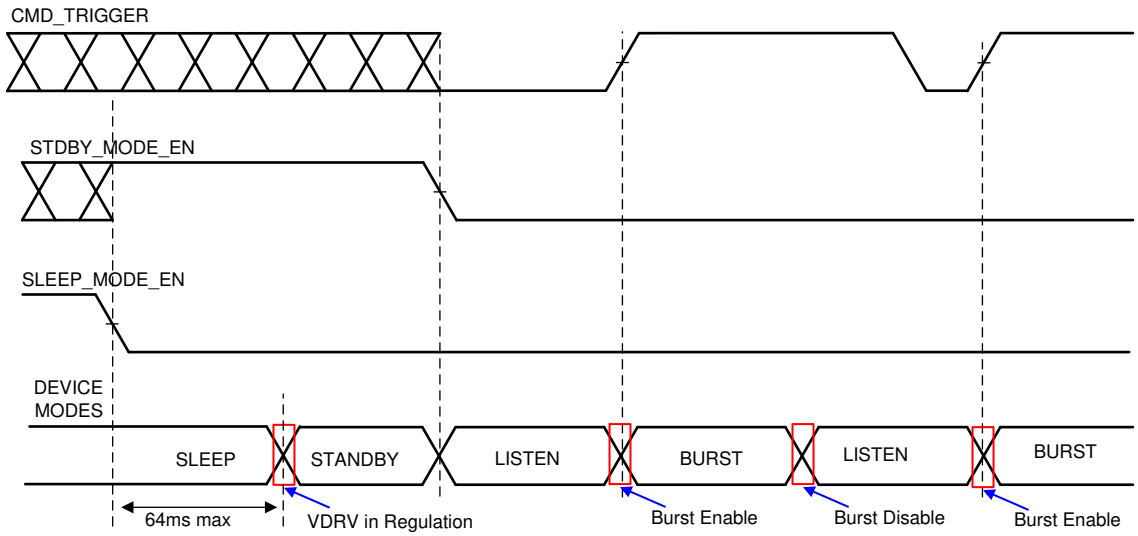


Figure 7-7. Device Modes Timing Diagram

Note

- The transition to standby or active mode (listen or burst) from power-up or sleep mode is done only once the VDRV voltage crosses the programmed VDRV_VOLTAGE_LEVEL bit, or is higher 64 ms, whichever occurs earlier.
- In the case when VDRV is disabled, the device immediately transitions from power or sleep mode to standby and active modes.

7.5 Programming

The primary communication between the IC and the external MCU is through an SPI bus that provides full-duplex communications in a controller-peripheral configuration. The external MCU is **always** a SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The device is **always** a SPI peripheral device that receives command requests and sends responses to the external MCU over the SDO line. The following lists the characteristics of the SPI:

- The SPI is a 4-pin interface.
- The frame size is 16 bits and is assigned as follows:

Controller-to-peripheral (MCU to TUSS4440 over the SDI line)	1 RW bit, 6 bits for the register address, 1 ODD parity bit for entire SPI frame, 8 bits for data
Peripheral-to-controller (TUSS4440 to MCU over the SDO line)	1 bit for Controller Parity error reporting during previous frame reception, 6 bits for the status, 1 bit for ODD parity for entire SPI frame, 8 bits for data

- SPI commands and data are shifted with the MSB first and the LSB last.
- The SDO line is sampled on the falling edge of the SCLK pin.
- The SDI line is shifted out on the rising edge of the SCLK pin.

The SPI communication begins with the NCS falling edge and ends with the NCS rising edge. The NCS high-level maintains the SPI peripheral-interface in the RESET state. The SDO output is in the tri-state condition.

The SPI does not support *back-to-back* SPI frame operation. After each SPI transfer the NCS pin must go from low to high before the next SPI transfer can begin.

Figure 7-8 shows an overview of a complete 16-bit SPI frame.

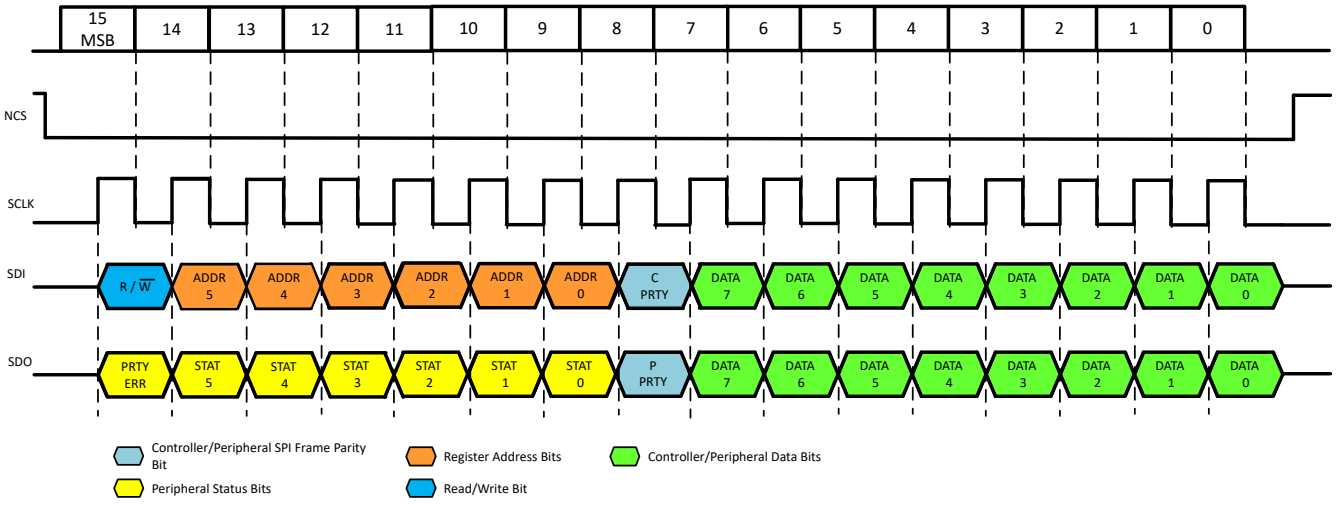


Figure 7-8. 16-Bit SPI Frame

Figure 7-9 shows a SPI transfer sequence between the controller and the peripheral TUSS4440 device. When the controller is writing a SPI frame, the parity error bit indicates if there was a parity error for the previous frame. When the controller is transmitting the data for the SPI write, the peripheral echoes back register address that was sent just before in the command.

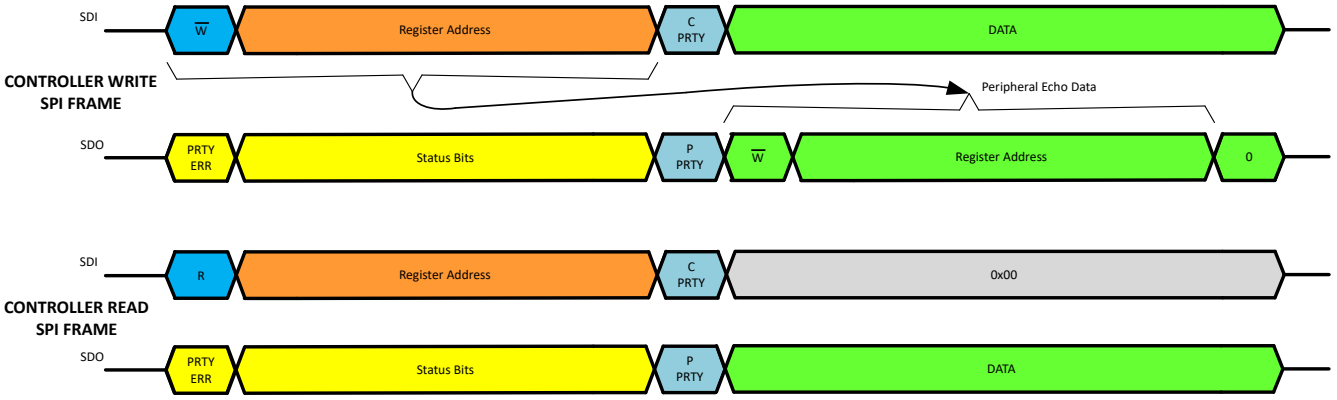


Figure 7-9. SPI Transfer Sequence

The status bits are defined in Table 7-4:

Table 7-4. SPI Interface Status Bits Description

STATUS BIT	DESCRIPTION
STAT 5 - VDRV_READY	Set when VDRV power regulator has reached the programmed voltage level. This is also indicated by VDRV_READY bit.
STAT 4- PULSE_NUM_FLT	Set if the burst sequence was terminated before completing the pulse number selected. This is also indicated by PULSE_NUM_FLT bit.
STAT 3 - DRV_PULSE_FLT	Set if there is a "stuck" fault detected during pulsing in a burst sequence. This is also indicated by DRV_PULSE_FLT
STAT 2 - EE_CRC_FLT	Set if there is a CRC Error when loading internal EEPROM memory. This is also indicated by EE_CRC_FLT bit.
STAT <1:0> - DEV_STATE	Device State: 00 - LISTEN 01 - BURST 10 - STANDBY 11 - SLEEP

7.6 Register Maps

This section lists the REG_USER registers that are part of the volatile memory that can be configured by the MCU at power up or any time during the operation of the device. For register bits that are marked reserved, their reset value should not be changed.

7.6.1 REG_USER Registers

Table 7-5 lists the REG_USER registers. All register offset addresses not listed in Table 7-5 should be considered as reserved locations and the register contents should not be modified.

Table 7-5. REG_USER Registers

Address	Acronym	Register Name	Section
0x10	BPF_CONFIG_1	Bandpass filter settings	Go
0x11	BPF_CONFIG_2	Bandpass filter settings	Go
0x12	DEV_CTRL_1	Log-amp configuration	Go
0x13	DEV_CTRL_2	Log-amp configuration	Go
0x14	DEV_CTRL_3	Device Configuration	Go
0x16	VDRV_CTRL	VDRV Regulator Control	Go
0x17	ECHO_INT_CONFIG	Echo Interrupt Control	Go
0x18	ZC_CONFIG	Zero Crossing configuration	Go
0x19	XFMR_DRV_LIM	Transformer drive config	Go
0x1A	BURST_PULSE	Burst pulse configuration	Go
0x1B	TOF_CONFIG	Time of Flight Config	Go
0x1C	DEV_STAT	Fault status bits	Go
0x1D	DEVICE_ID	Device ID	Go
0x1E	REV_ID	Revision ID	Go

Complex bit access types are encoded to fit into small table cells. Table 7-6 shows the codes that are used for access types in this section.

Table 7-6. REG_USER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 BPF_CONFIG_1 Register (Address = 0x10) [reset = 0x0]

BPF_CONFIG_1 is shown in Table 7-7.

Return to the Summary Table.

Table 7-7. BPF_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BPF_FC_TRIM_FRC	R/W	0x0	Override factor settings for Bandpass filter trim and control via BPF_FC_TRIM register. Valid only when BPF_BYPASS = 0 0x0 = Factory trim 0x1 = Override Factory trim

Table 7-7. BPF_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BPF_BYPASS	R/W	0x0	Select between Bandpass filter or high pass filter 0x0 = BPF Enabled 0x1 = HPF Enabled (BPF Bypass)
5:0	BPF_HPF_FREQ	R/W	0x0	If BPF_BYPASS = 0: Band pass filter center frequency. See "Bandpass filter center frequency configuration" table If BPF_BYPASS = 1: High pass filter corner frequency 0x00 - 0x0F - 200kHz 0x10 - 0x1F - 400kHz 0x20 - 0x2F - 50kHz 0x30 - 0x3F - 100kHz

7.6.1.2 BPF_CONFIG_2 Register (Address = 0x11) [reset = 0x0]

BPF_CONFIG_2 is shown in Table 7-8.

Return to the Summary Table.

Table 7-8. BPF_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	BPF_Q_SEL	R/W	0x0	Bandpass filter Q factor. Valid only when BPF_BYPASS = 0 0x0 = 4 0x1 = 5 0x2 = 2 0x3 = 3
3:0	BPF_FC_TRIM	R/W	0x0	Offset BPF_HPF_FREQ when BPF_FC_TRIM_FRC = 1: BPF_HPF_FREQ = BPF_HPF_FREQ + BPF_FC_TRIM See "Bandpass filter center frequency range extension" table.

7.6.1.3 DEV_CTRL_1 Register (Address = 0x12) [reset = 0x0]

DEV_CTRL_1 is shown in Table 7-9.

Return to the Summary Table.

Table 7-9. DEV_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_FRC	R/W	0x0	Override for factory settings for LOGAMP_SLOPE_ADJ and LOGAMP_INT_ADJ
6:4	LOGAMP_SLOPE_ADJ	R/W	0x0	Slope or gain adjustment at the final output on VOUT pin. Slope adjustment depends on the setting of VOUT_SCALE_SEL. 0x0 = 3.0× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.56×VOUT_SCALE_SEL V/V 0x1 = 3.1× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.71×VOUT_SCALE_SEL V/V 0x2 = 3.2× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.86×VOUT_SCALE_SEL V/V 0x3 = 3.3× $\overline{\text{VOUT\_SCALE\_SEL}}$+5.01×VOUT_SCALE_SEL V/V 0x4 = 2.6× $\overline{\text{VOUT\_SCALE\_SEL}}$+3.94×VOUT_SCALE_SEL V/V 0x5 = 2.7× $\overline{\text{VOUT\_SCALE\_SEL}}$+ 4.10×VOUT_SCALE_SEL V/V 0x6 = 2.8× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.25×VOUT_SCALE_SEL V/V 0x7 = 2.9× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.4×VOUT_SCALE_SEL V/V
3:0	LOGAMP_INT_ADJ	R/W	0x0	Logamp Intercept adjustment. See "Logamp intercept adjustment" table in specification for values.

7.6.1.4 DEV_CTRL_2 Register (Address = 0x13) [reset = 0x0]

DEV_CTRL_2 is shown in Table 7-10.

Return to the Summary Table.

Table 7-10. DEV_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_DIS_FIRST	R/W	0x0	Disable first logamp stage to reduce quiescent current
6	LOGAMP_DIS_LAST	R/W	0x0	Disable last logamp stage quiescent current
3	RESERVED	R	0x0	Reserved
2	VOUT_SCALE_SEL	R/W	0x0	Select VOUT scaling 0x0 = Select Vout gain to map output to 3.3 V 0x1 = Select Vout gain to map output to 5.0 V
1:0	LNA_GAIN	R/W	0x0	Adjust LNA Gain in V/V 0x0 = 15 V/V 0x1 = 10 V/V 0x2 = 20 V/V 0x3 = 12.5 V/V

7.6.1.5 DEV_CTRL_3 Register (Address = 0x14) [reset = 0x0]

DEV_CTRL_3 is shown in Table 7-11.

Return to the Summary Table.

Table 7-11. DEV_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
4:2	DRV_PLS_FLT_DT	R/W	0x0	Driver Pulse Fault Deglitch Time. In IO_MODE = 0 or IO_MODE = 1, DRV_PULSE_FLT will be set if start of burst is triggered and IO2 pin has not toggled for greater than deglitch Time. In IO_MODE = 2, DRV_PULSE_FLT will be set if start of burst is triggered and if IO1 or IO2 do not toggle a period longer than the deglitch time except when both pins are high. 0x0 = 64 µs 0x1 = 48 µs 0x2 = 32 µs 0x3 = 24 µs 0x4 = 16 µs 0x5 = 8 µs 0x6 = 4 µs 0x7 = Check Disabled
1:0	IO_MODE	R/W	0x0	Configuration for low voltage IO pins. 0x0 = IOMODE 0 0x1 = IOMODE 1 0x2 = IOMODE 2 0x3 = IOMODE 3

7.6.1.6 VDRV_CTRL Register (Address = 0x16) [reset = 0x20]

VDRV_CTRL is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. VDRV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DIS_VDRV_REG_LSTN	R/W	0x0	Automatically disable VDRV charging in listen mode every time after burst mode is exited given VDRV_TRIGGER =0x0. 0x0 = Do not automatically disable VDRV charging 0x1 = Automatically disable VDRV charging
5	VDRV_HI_Z	R/W	0x1	Turn off current source between VPWR and VRDV and disable VDRV regulation. 0x0 = VDRV not Hi-Z 0x1 = VDRV in Hi-Z mode
4	VDRV_CURRENT_LEVEL	R/W	0x0	Pull up current at VDRV pin 0x0 = 10 mA 0x1 = 20 mA
3:0	VDRV_VOLTAGE_LEVEL	R/W	0x0	Regulated Voltage at VDRV pin Value is calculated as : VDRV = VDRV_VOLTAGE_LEVEL + 5 [V]

7.6.1.7 ECHO_INT_CONFIG Register (Address = 0x17) [reset = 0x7]

ECHO_INT_CONFIG is shown in Table 7-13.

Return to the Summary Table.

Table 7-13. ECHO_INT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	ECHO_INT_CMP_EN	R/W	0x0	Enable echo interrupt comparator output
3:0	ECHO_INT_THR_SEL	R/W	0x7	Threshold level to issue interrupt on OUT4 pin. Applied to Low pass filter output. If VOUT_SCALE_SEL=0x0 : Threshold = 0.04 x ECHO_INT_THR_SEL + 0.4 [V] If VOUT_SCALE_SEL=0x1: Threshold = 0.06 x ECHO_INT_THR_SEL + 0.6 [V]

7.6.1.8 ZC_CONFIG Register (Address = 0x18) [reset = 0x14]

ZC_CONFIG is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. ZC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ZC_CMP_EN	R/W	0x0	Enable Zero Cross Comparator for Frequency detection
6	ZC_EN_ECHO_INT	R/W	0x0	When set, provides ZC information only when object is detected
5	ZC_CMP_IN_SEL	R/W	0x0	Zero Comparator Input Select 0x0 = INP - VCM 0x1 = INP - INN
4:3	ZC_CMP_STG_SEL	R/W	0x2	Zero Cross Comparator Stage Select

Table 7-14. ZC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	ZC_CMP_HYST	R/W	0x4	Zero Cross Comparator Hysteresis Selection 0x0 = 30 mV 0x1 = 80 mV 0x2 = 130 mV 0x3 = 180 mV 0x4 = 230 mV 0x5 = 280 mV 0x6 = 330 mV 0x7 = 380 mV

7.6.1.9 XFMR_DRV_LIM Register (Address = 0x19) [reset = 0x0]

XFMR_DRV_LIM is shown in Table 7-15.

Return to the Summary Table.

Table 7-15. XFMR_DRV_LIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	XFMR_DRV_ILIM	R/W	0x0	Current clamp for low side transformer drive. Value calculated as = [50 + (REG_VAL) x 7.14] mA

7.6.1.10 BURST_PULSE Register (Address = 0x1A) [reset = 0x0]

BURST_PULSE is shown in Table 7-16.

Return to the Summary Table.

Table 7-16. BURST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALF_BRG_MODE	R/W	0x0	Use output driver in half-bridge mode. When enabled, drive low-side FETs in-phase 0x0 = Disable half-bridge mode 0x1 = Enable half bridge mode
5:0	BURST_PULSE	R/W	0x0	Number of burst pulses. REG_VALUE=0x00 enables continuous burst mode

7.6.1.11 TOF_CONFIG Register (Address = 0x1B) [reset = 0x0]

TOF_CONFIG is shown in Table 7-17.

Return to the Summary Table.

Table 7-17. TOF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_MODE_EN	R/W	0x0	For entering or exiting sleep mode 0x0 = Wake up or exit Sleep Mode 0x1 = Enter sleep mode
6	STDBY_MODE_EN	R/W	0x0	For entering or exiting standby mode 0x0 = Exit Standby Mode 0x1 = Enter Standby mode
5:2	RESERVED	R	0x0	Reserved

Table 7-17. TOF_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VDRV_TRIGGER	R/W	0x0	Control charging of VDRV pin when DIS_VDRV_REG_LSTN = 1. This has no effect when VDRV_HI_Z=0x1. 0x0 = Disable I_{VDRV} 0x1 = Enable I_{VDRV}
0	CMD_TRIGGER	R/W	0x0	For IO_MODE=0x0, control enabling of burst mode. Ignored for other IO_MODE values. 0x0 = Disable burst mode 0x1 = Enable burst mode

7.6.1.12 DEV_STAT Register (Address = 0x1C) [reset = 0x0]

DEV_STAT is shown in Table 7-18.

Return to the Summary Table.

Table 7-18. DEV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	VDRV_READY	R	0x0	VDRV pin voltage status 0x0 = VDRV is below configured voltage 0x1 = VDRV is equal or above configured voltage
2	PULSE_NUM_FLT	R	0x0	The Driver has not received the number of pulses defined by BURST_PULSE
1	DRV_PULSE_FLT	R	0x0	The Driver has been stuck in a single state in burst mode for a period longer than delgitch time set by DRV_PLS_FLT_DT
0	EE_CRC_FLT	R	0x0	CRC error for internal memory

7.6.1.13 DEVICE_ID Register (Address = 0x1D) [reset = X]

DEVICE_ID is shown in Table 7-19.

Return to the Summary Table.

Table 7-19. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	X	Device ID: 0x99

7.6.1.14 REV_ID Register (Address = 0x1E) [reset = 0x2]

REV_ID is shown in Table 7-20.

Return to the Summary Table.

Table 7-20. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	0x2	Revision ID

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSS4440 device must be paired with an external ultrasonic transducer. The TUSS4440 device drives the transducer to generate an ultrasonic echo and applies logarithmic gain scaling to the received echo signal in the analog front end. The transducer should be chosen based on the resonant frequency, input voltage requirements, sensitivity, beam pattern, and decay time. The TUSS4440 device is flexible enough to meet most transducer requirements by adjusting the driving frequency, driving current limit, and center frequency of the band-pass filter.An external transformer should be chosen to meet the driver voltage requirements of the transducer and have a saturation current rated equal to or greater than the configured driving current limit of the TUSS4440 device. The only available interface to configure the device registers is SPI. During the burst-and-listen cycles, an external ADC or analog receiver should be used to capture the echo envelope from the VOUT pin to compute time of flight (ToF), distance, amplitude, and/or width of the return echo.

8.2 Typical Application

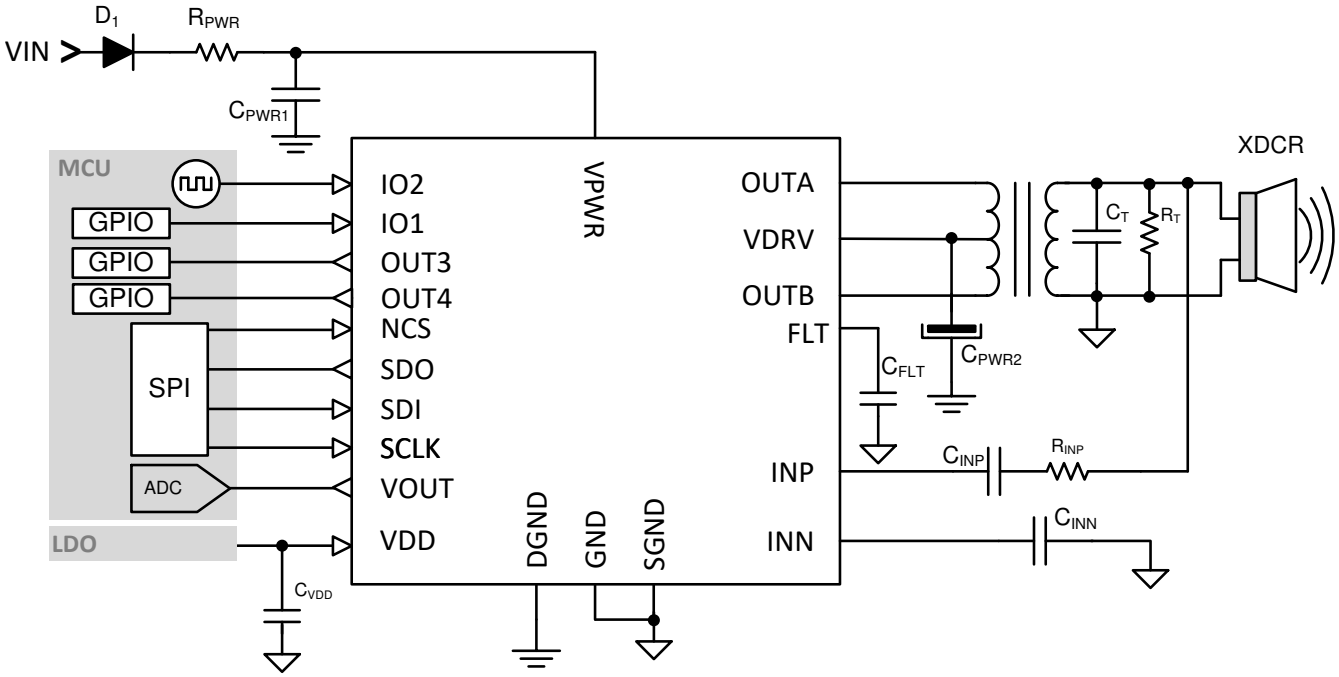


Figure 8-1. TUSS4440 Application Diagram

Table 8-1. Recommended Component Values for Typical Applications

DESIGNATOR	VALUE	COMMENT
R_{PWR}	10 Ω	Optional (to limit fast voltage transient on VPWR pin during power up)
$R_{(INP)}$	3kΩ (1/4 Watt)	Optional for EMI/ESD robustness
C_{PWR1}	50V, 100nF	
C_{PWR2}	40V, 100µF	
C_{VDD}	>5V, 10nF	
C_{INP}	40V, 330pF	
C_{INN}	>5V, C_{INN}	Use equation below to estimate value of C_{INN} depending on the burst frequency $\frac{1}{2 \times 150 \times \frac{f_{BURST}}{4}}$ (2)
C_{FLT}	5V, C_{FLT}	Use equation below to estimate value of C_{FLT} depending on the burst frequency . Value has to be optimized for application depending on noise and response time requirements. $\frac{25}{2 \times 6250 \times f_{BURST}}$ (3)
C_T		Optional. Value depends on transducer and transformer used
R_T		Optional. Value depends on transducer and transformer used
D1	1N4001 or equivalent	Optional for reverse supply and reverse current protection.
XDCR (transducer)		Example devices for low-frequency range: Closed top: 40 kHz: PUI Audio UTR-1440K-TT-R Open top: muRata MA40H1S-R, SensComp 40LPT16, Kobitone 255-400PT160-ROX Example devices for high-frequency range: Closed top: 300 kHz: Murata MA300D1-1
XFMR (transformer)		Example devices: TDK EPCOS B78416A2232A003, muRata-Toko N1342DEA-0008BQE=P3, Mitsumi K5-R4

8.2.1 Transformer Drive Configuration Options

The TUSS4440 supports two pulsing modes to accommodate specific system needs based on the transformer used as shown in Figure 8-2. The typical application diagram in Figure 8-1 is considered as "Case 1".

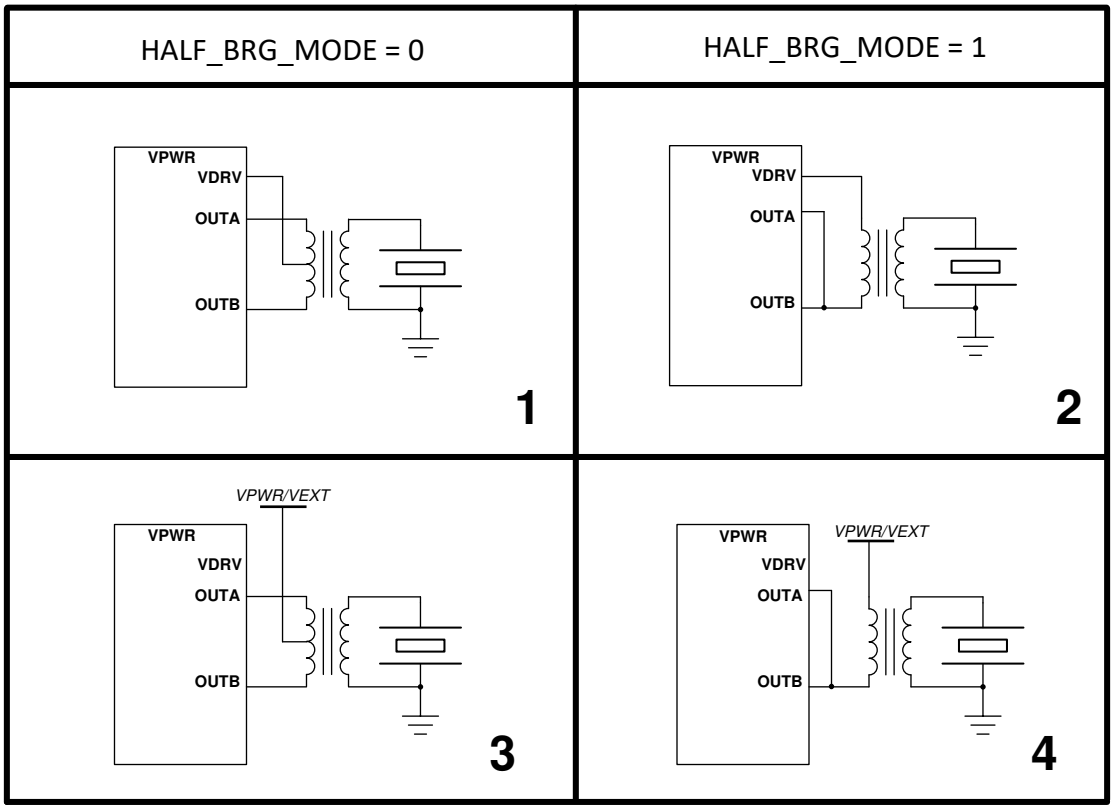


Figure 8-2. TUSS4440 Transducer Drive Options

The behavior of the internal FETs of TUSS4440 is different for each configuration in Table 8-2. The relationship between the IOx pins and the state of the OUTA and OUTB pins for different register settings is shown in Table 8-2 and Table 8-3.

Table 8-2. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 2

IO MODE 2						
START OF BURST	HALF_BRG_ MODE	IO1	IO2	OUTA	OUTB	APPLICATION CASE
YES	0	0	0	Hi-Z	Hi-Z	CASE 1, CASE 3
	0	0	1	Hi-Z	GND	
	0	1	0	GND	Hi-Z	
NO	0	1	1	Hi-Z	Hi-Z	
YES	1	0	0	Hi-Z	Hi-Z	CASE 2, CASE 4
	1	0	1	GND	GND	
	1	1	0	Hi-Z	Hi-Z	
NO	1	1	1	Hi-Z	Hi-Z	

Table 8-3. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3

IO MODE 0, IO MODE 1, IO MODE 3							
START OF BURST	HALF_BRG_ MODE	CMD_TRIG GER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	0	0	1	0	Hi-Z	Hi-Z	CASE 1, CASE 3
	0	0	1	1			
YES	0	1	0	0	Hi-Z	GND	
	0	1	0	1	GND	Hi-Z	

Table 8-3. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3 (continued)

IO MODE 0, IO MODE 1, IO MODE 3							
START OF BURST	HALF_BRG_ MODE	CMD_TRIG GER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	1	0	1	0	Hi-Z	Hi-Z	CASE 2, CASE 4
	1	0	1	1			
YES	1	1	0	0	Hi-Z	Hi-Z	
	1	1	0	1	GND	GND	

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-4 as the input and operating parameters. All other device settings can be assumed to be factory default.

Table 8-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 to 36 V
Input voltage recommended	5 V, 12 V
Transformer turns ratio	(1-2) : (2-3) : (4-6) = 1:1:8.42
Transformer driving current rating	300 mA
Transducer driving voltage	70 V_{AC}
Transducer frequency	40 kHz, 400 kHz
Transducer pulse count	16

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Transducer:
  - Transducer driving voltage
  - Transducer resonant frequency
  - Transducer pulse count maximum
- Transformer:
  - Transformer turns ratio
  - Transformer saturation current
  - Transformer main voltage (4-6) rating

8.2.1.2.1 Transducer Driving Voltage

When a voltage is applied to piezoelectric ceramics, mechanical distortion is generated according to the voltage and frequency. The mechanical distortion is measured in units of sound pressure level (SPL) to indicate the volume of sound, and can be derived from a free-field microphone voltage measurement using Equation 4.

$$\text{SPL (db)} = 20 \times \log \frac{\left(\frac{V_{(MIC)}}{3.4\ mV} \right)}{P_O} \tag{4}$$

where

- $V_{(MIC)}$ is the measured sensor sound pressure (mV_{RMS}).
- P_O is a referenced sound pressure of 20 µPa.

The SPL does not increase indefinitely with the driving voltage. After a particular driving voltage, the amount of SPL that a transducer can generate becomes saturated. A transducer is given a maximum driving voltage specification to indicate when the maximum SPL is generated. Driving the transducer beyond the maximum

driving voltage makes the ultrasonic module less power-efficient and can damage or decrease the life expectancy of the transducer.

8.2.1.2.2 Transducer Driving Frequency

The strength of ultrasonic waves propagated into the air attenuate proportionally with distance. This attenuation is caused by diffusion, diffraction, and absorption loss as the ultrasonic energy transmits through the medium of air. As shown in Figure 8-3, the higher the frequency of the ultrasonic wave, the larger the attenuation rate and the shorter the distance the wave reaches.

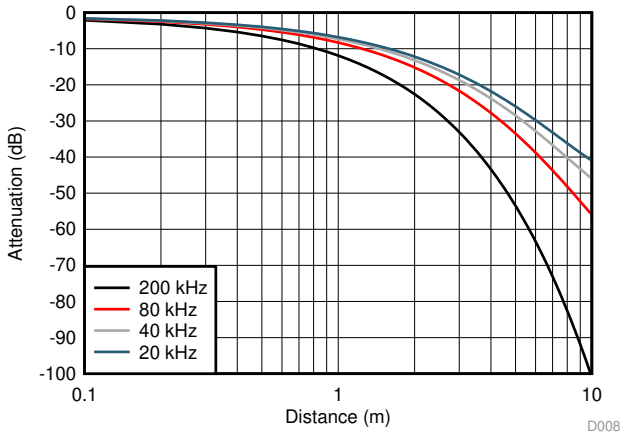


Figure 8-3. Attenuation Characteristics of Sound Pressure by Distance

An ultrasonic transducer has a fixed resonant center frequency with a typical tolerance of ±2%. The lower frequency range of 30 kHz to 100 kHz is the default operating range for common long range applications for a step resolution of 1 cm and typical range of 30 cm to 5 m. The upper frequency range of 100 kHz to 1000 kHz is reserved for high-precision applications with a step resolution of 1 mm and a typical range of 5 cm to 1 m.

8.2.1.2.3 Transducer Pulse Count

The pulse count determines how many alternating periods are applied to the transducer by the complementary low-side drivers and determines the total width of the ultrasonic ping that was transmitted. The larger the width of the transmitted ping, the larger the width of the returned echo signature of the reflected surface and the more resolution available to set a stable threshold. A disadvantage of a large pulse count is a large ringing-decay period, which limits how detectable objects are at short distances.

Select a pulse count based on the minimum object distance requirement. If short-distance object detection is not a priority, a high pulse count is not a concern. Certain transducers can be driven continuously while others have a limit to the maximum driving-pulse count. Refer to the specification for the selected transducer to determine if the pulse count must be limited.

8.2.1.2.4 Transformer Turns Ratio

A center-tap transformer is typically paired with the transducer to convert a DC voltage to a high-sinusoidal AC voltage. The center tap is a contact made to a point halfway along the primary winding of the transformer. The center tap is supplied with the DC voltage that is then multiplied on the secondary side based on the turns ratio of the transformer. Figure 8-4 shows the typical pinout of a center-tap transformer where pin 2 is the center tap, pins 1 and 3 are connected to OUTB and OUTA, pin 4 is connected to the positive terminal of the transducer, and pin 6 is connected to ground.

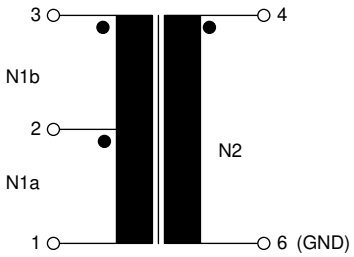


Figure 8-4. Typical Pinout of Center-Tap Transformer for Ultrasonic Transducers

Two modes to generate the transducer voltage using the center-tap transformer are available. These modes are defined as follows:

Push-pull In this mode, the two internal low-side switches of the TUSS4440 device are used to turn current on and off in two primary coils of the center-tap transformer.

The primary coils have the same number of turns. The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The direction of current in the primary coils generates voltages of opposite polarity in the secondary coils which effectively doubles the peak-to-peak voltage in the secondary coil.

Single-ended In this mode, one low-side switch is used to turn current on and off in the primary of the transformer.

The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The center tap of the transformer is not required for this mode, and can be left floating. Instead, the reference voltage is connected to an outermost primary-side terminal (pin 3) and either OUTA or OUTB is connected to the other primary-side terminal (pin 1).

8.2.1.2.5 Transformer Saturation Current and Main Voltage Rating

Leakage inductance is caused when magnetic flux is not completely coupled between windings in a transformer. Magnetic saturation of a transformer core can be caused by excessive primary voltage, operation at too low of a frequency, by the presence of a DC current in any of the windings, or a combination of these causes. The TUSS4440 device can limit the primary-side driver current of the transformer internally from 50 mA to 500 mA. The center-tap voltage is typically referenced to the VPWR voltage. However, if the VPWR voltage is too high of a voltage on the center tap of the primary side, then the voltage must be down-regulated. If the VPWR is too low, then the voltage must be up-regulated.

8.2.1.3 Application Curves

Figure 8-5 and Figure 8-6 show the typical ranging performance of a 40-kHz, closed-top transducer under nominal operating conditions as indicated in the Table 8-4. The targeted object is a PVC pole measuring 1000 mm in height and 75 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1.

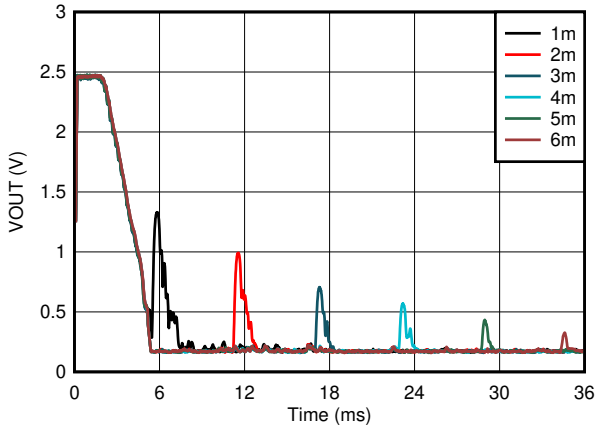


Figure 8-5. TUSS4440 40 kHz Ranging at 5-V Center Tap With Last Log-Amp Stage Disabled

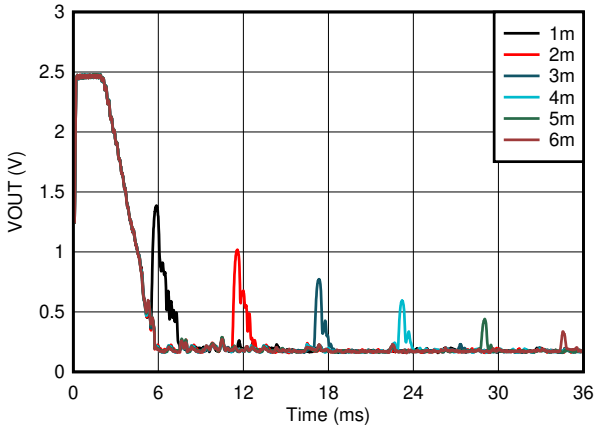


Figure 8-6. TUSS4440 40 kHz Ranging at 12-V Center Tap With Last Log-Amp Stage Disabled

Figure 8-7 and Figure 8-8 show the typical ranging performance of a 400-kHz, closed-top transducer under nominal operating conditions as indicated in the Table 8-4. The targeted object is an aluminum pole measuring 100 mm in height and 10 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0.

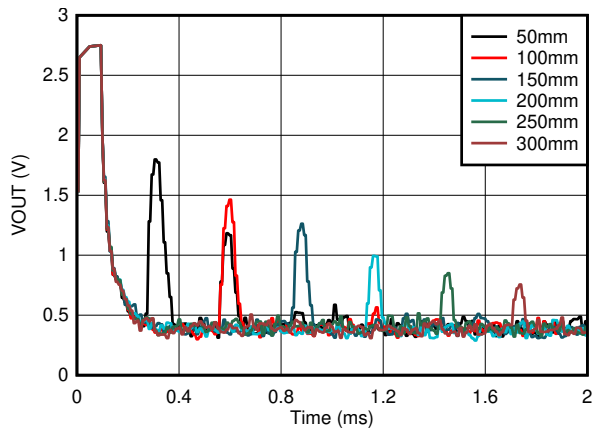


Figure 8-7. TUSS4440 400 kHz Ranging at 5-V Center Tap

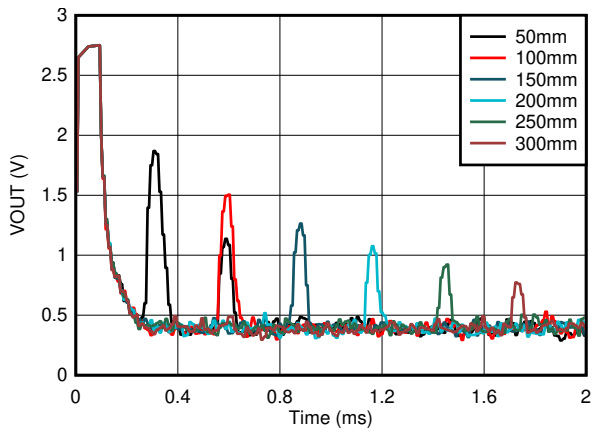


Figure 8-8. TUSS4440 400 kHz Ranging at 12-V Center Tap

9 Power Supply Recommendations

The TUSS4440 device is designed to operate from two independent supplies, a driver supply and a regulated supply.

The driver input voltage supply (VPWR) range can operate from 5 V to 24 V (when VDRV is disabled) or to 36 V (when VDRV is enabled). In applications where the TUSS4440 device may be exposed to battery transients and reverse battery currents, use external component-safeguards, such as component D1 or parallel TVS diodes, to help protect the device. If the input supply is placed more than a few inches from the TUSS4440 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors near the VPWR pin. In the event VDRV is disabled, the electrolytic capacitor at the VDRV pin is intended to act as a fast discharge capacitor during the bursting stage of the TUSS4440 device. The center-tap transformer can be supplied with an independent center-tap voltage that is isolated from the VPWR and VDRV pins, but must remain within half the specified maximum voltage rating of the OUTA and OUTB outputs. If the center-tap voltage is to be supplied by an independent source, the VDRV pin can remain floating, and VDRV should be disabled.

The regulated supply (VDD) is used as the supply reference for the analog front end, filtering, and analog output blocks, so this supply should be stable for maximum performance. TI recommends using an LDO or other regulated external power source with bypass capacitor placed closely to the VDD pin. As VDD becomes less stable, the noise floor of the VOUT signal will increase, and result in a loss of long range object detection as a consequence.

To prevent damage to the device, always avoid hot-plugging or providing instantaneous power at the VPWR and VDRV pins at start-up, unless these pins are properly protected with an RC filter or TVS diode to minimize transient effects. VPWR must always be equal to or greater than the value present at VDRV.

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to accomplish a small-form factor ultrasonic module design. The layers should be separated by analog and digital signals. The pin map of the device is routed such that the power and digital signals are on the opposing side of the analog driver and receiver pins. Consider the following best practices for TUSS4440 device layout in order of descending priority:

- Separating the grounding types is important to reduce noise at the AFE input of the TUSS4440. In particular, the transducer sensor ground, supporting driver, and return-path circuitry should have a separate ground before being connected to the main ground. Separating the sensor and main grounds through a ferrite bead is best practice, but not require. A copper-trace or 0-Ω short is also acceptable when bridging grounds.
- The analog return path pins, INP and INN, are most susceptible to noise and therefore should be routed as short and directly to the transducer as possible. Ensure the INN capacitor is close to the pin to reduce the length of the ground wire.
- The analog output pin trace should be routed as short and directly to an external ADC or microcontroller input to avoid signal-to-noise losses due to parasitic-effects or noise coupling onto the trace from external radiating aggressors.
- In applications where protection from an ESD strike on the case of the transducer is important, ground routing of the capacitor on the INN pin should be separate from the device ground and connected directly with the shortest possible trace to the connector ground.
- The analog drive pins can be high-current, high-voltage, or both and therefore the design limitation of the OUTA and OUTB pins is based on the copper trace profile. The driver pins are recommended to be as short and direct as possible when using a transformer to drive the primary windings with a high-current limit.
- The decoupling capacitors for the VDD and VPWR pins should be placed as close to the pins as possible.
- Any digital communication should be routed away from the analog receiver pins. TXD, RXD, SCLK, NCS, IO1, IO2, OUT3, and OUT4 pins should be routed on the opposite side of the PCB, away from of the analog signals.

10.2 Layout Example

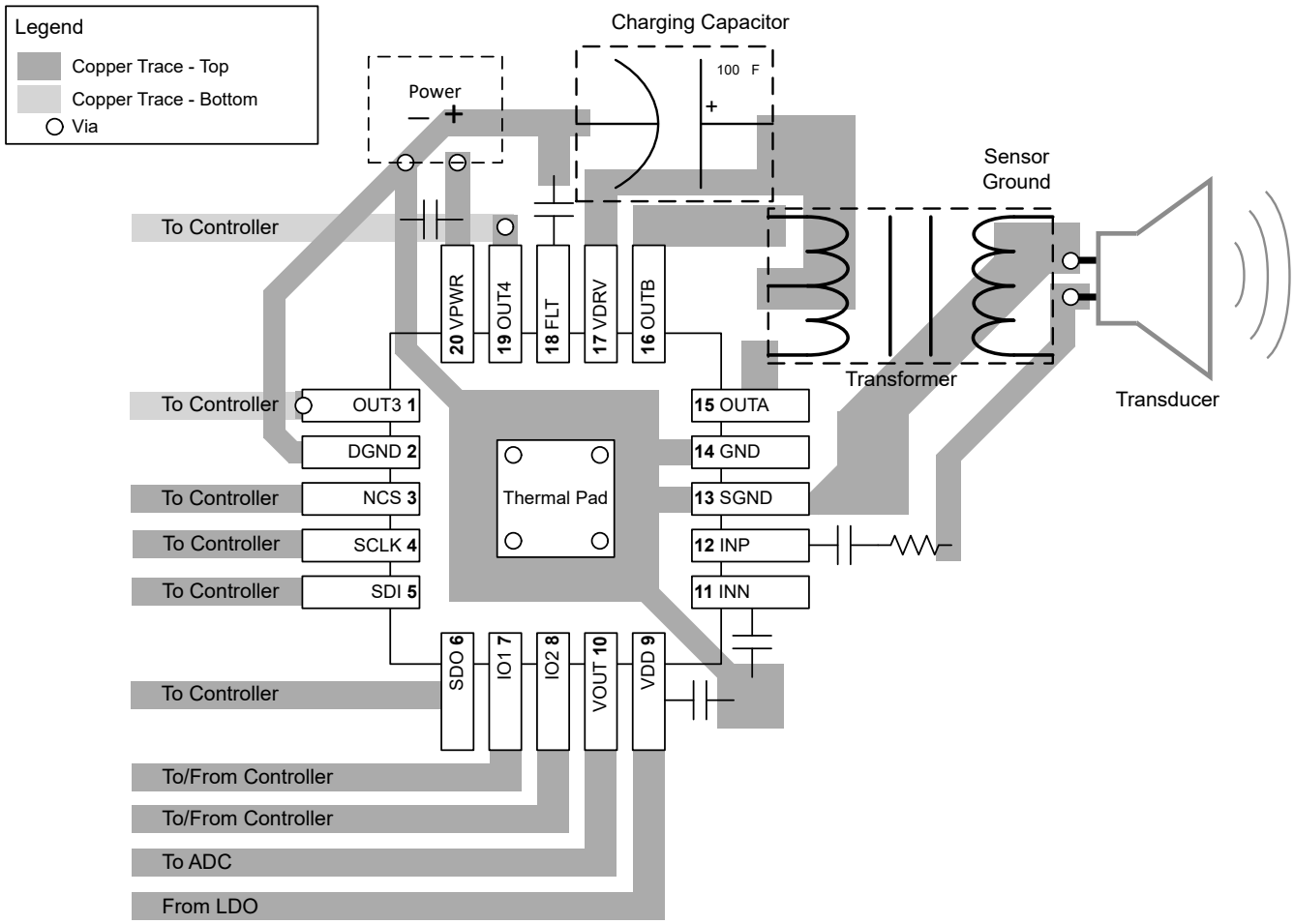


Figure 10-1. TUSS4440 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSS4440TRTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4440	Samples
TUSS4440TRTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4440	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

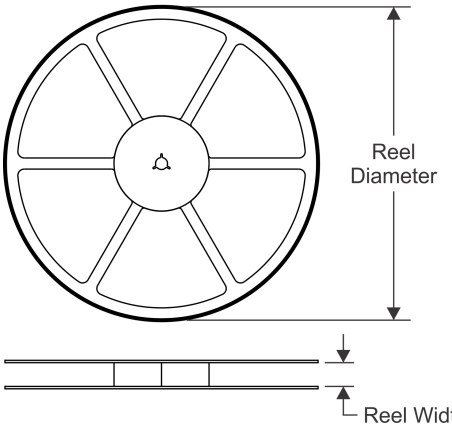
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

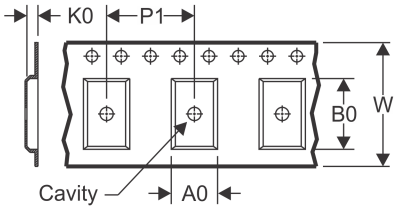
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

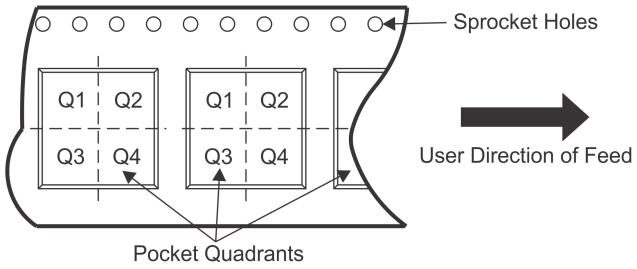


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

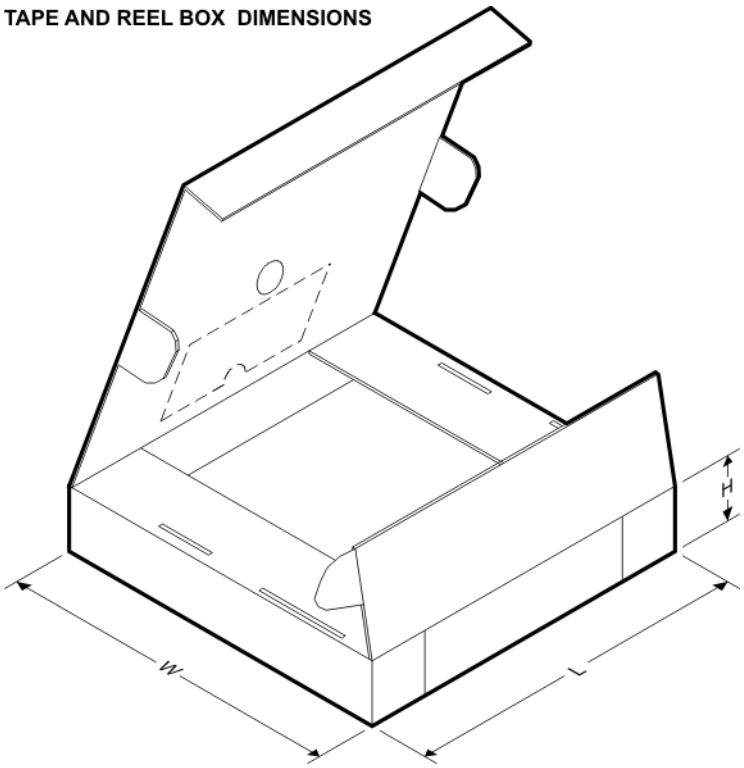
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSS4440TRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSS4440TRTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSS4440TRTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TUSS4440TRTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

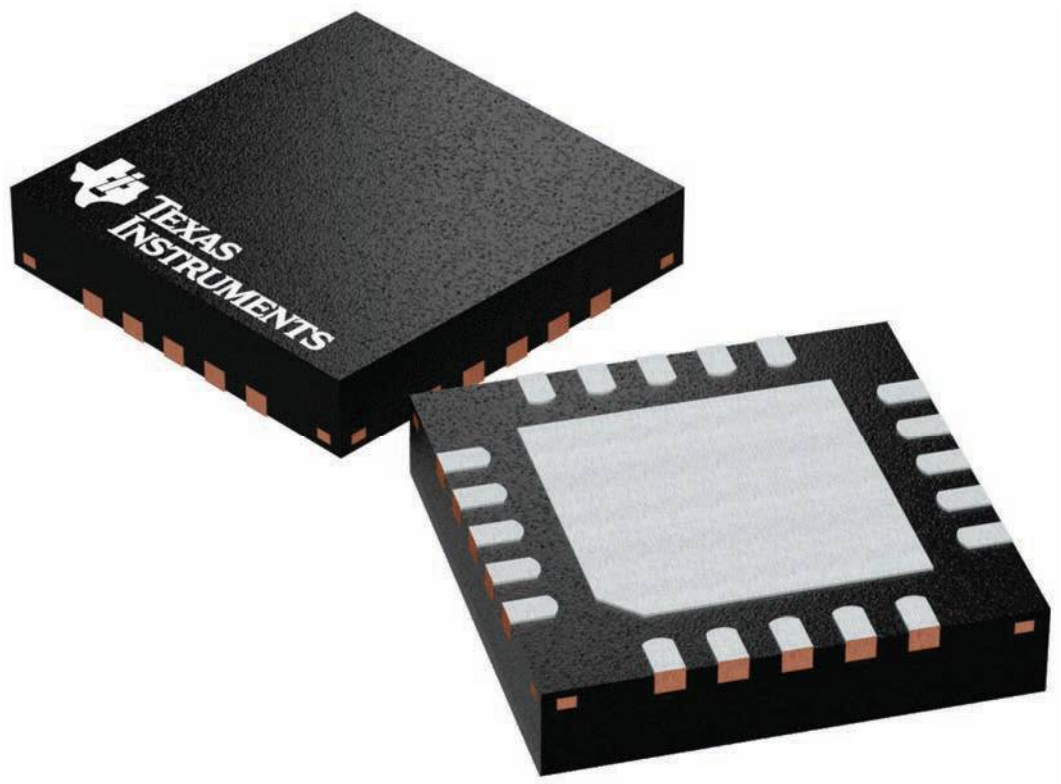
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
ENGINEER: T. TANG	DATE: 09/12/2016		
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016		

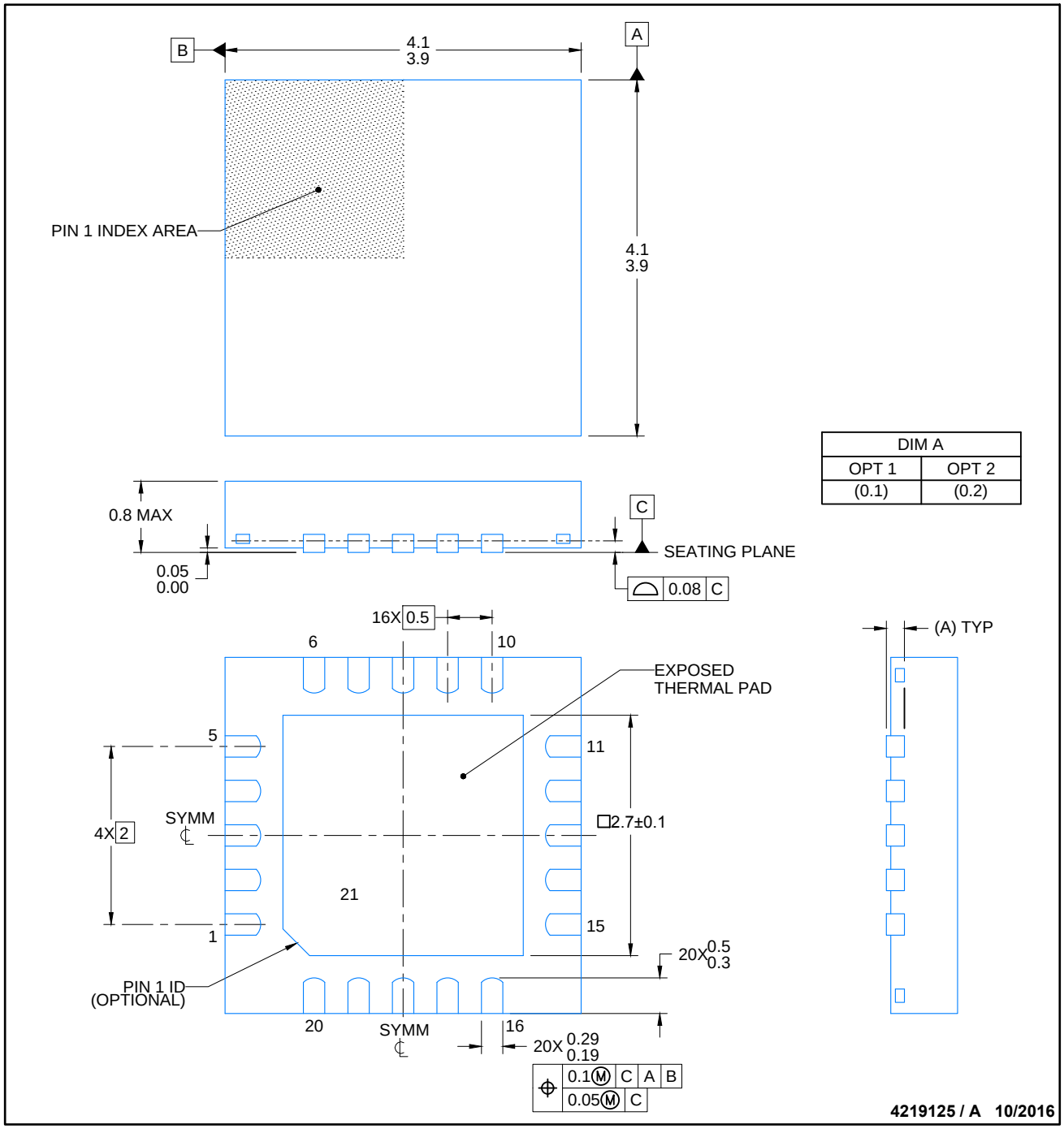
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5

PACKAGE OUTLINE

RTJ0020D

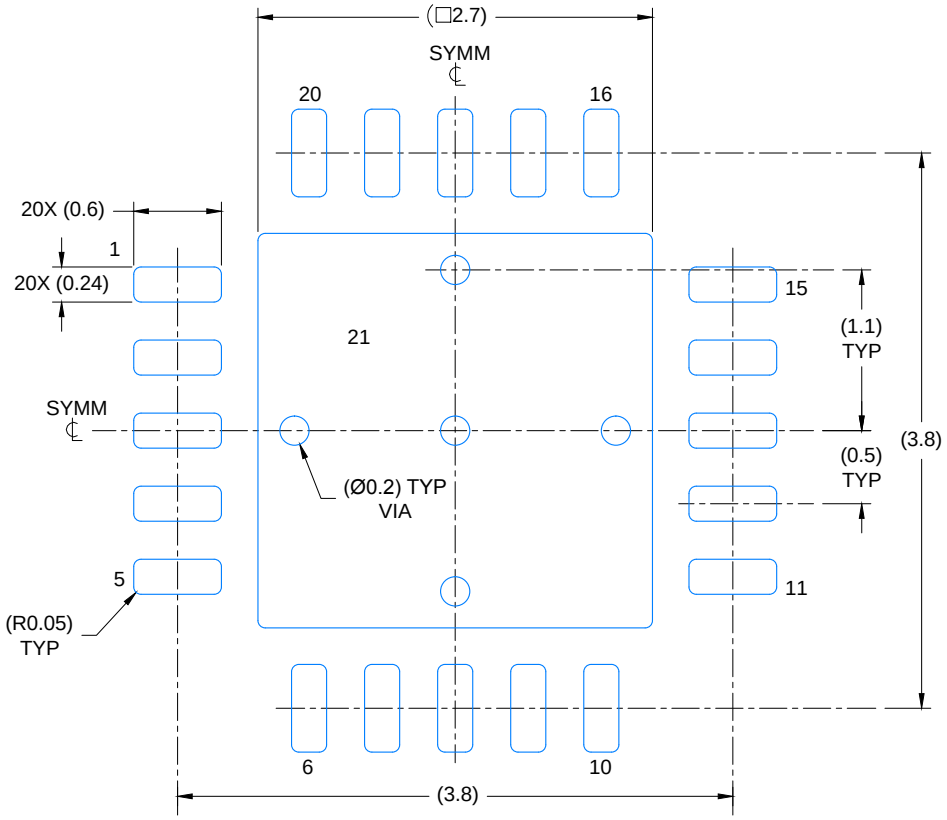
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



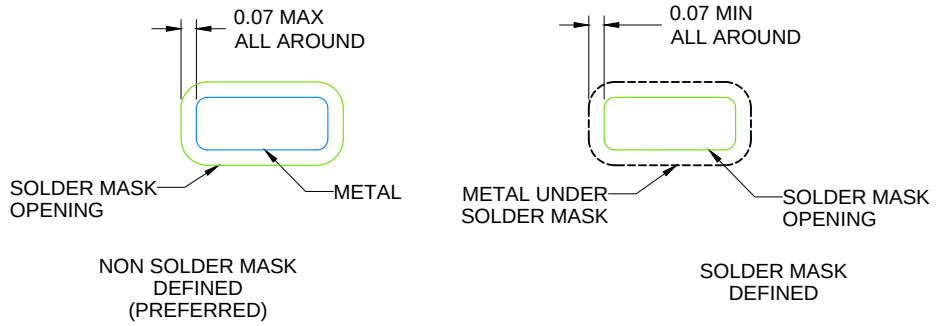
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

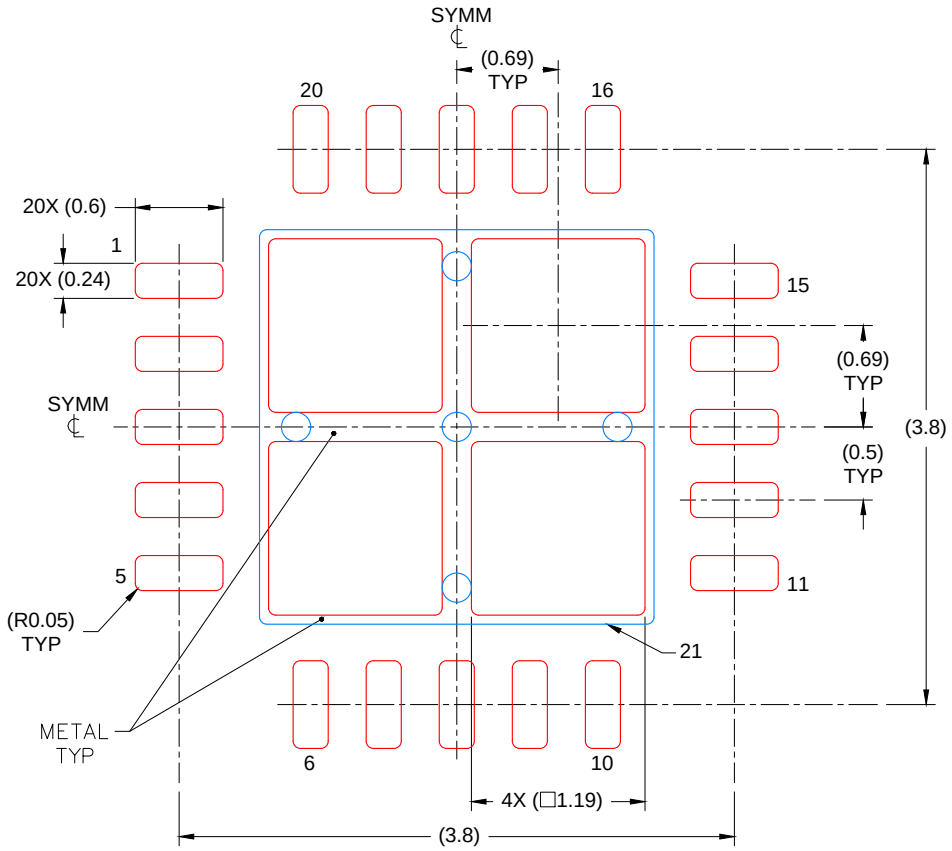
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TUSS4470 Transformer Drive Ultrasonic Sensor IC With Logarithmic Amplifier

1 Features

- Integrated driver for directly driving transducers and receiver stage with analog output for ultrasound applications
- 86-dB input dynamic range analog front-end
  - First stage low noise amplifier adjustable to 10, 12.5, 15 and 20 V/V
  - Configurable bandpass filter from 40 KHz to 500 KHz
  - Wide-band logarithmic amplifier
- Supported transducer frequencies (controlled by external clock)
  - 40 KHz to 1 MHz
  - Pre-driver mode: 40 KHz to 440 KHz
- For low-power applications
  - Standby mode: 1.7 mA (typical)
  - Sleep mode: 220 µA (typical)
- Configurable drive stage:
  - Direct drive using internal H-Bridge for transducer excitation
  - Pre-driver configuration to use internal H-bridge to drive external Field Effect Transistors (FETs) for higher current drive
  - Configurable burst patterns using IO1 and IO2 pins
- Outputs:
  - Voltage output of the demodulated echo envelope on VOUT
  - Input signal zero crossing comparator output on OUT3 pin
  - Programmable VOUT threshold crossing on OUT4 pin
- Serial Peripheral Interface (SPI) for configuration by microcontroller (MCU)

2 Applications

- Position sensor
- Level transmitter
- Proximity sensor

3 Description

The TUSS4470 is a highly integrated direct drive analog front end for industrial ultrasonic applications. The transducer drive stage is an internal H-bridge that can be configured to drive the transducer in direct-drive mode to achieve maximum voltage across the transducer. The internal H-bridge can also be configured as a pre-driver for external FETs, enabling higher current and voltage drive for larger transducers.

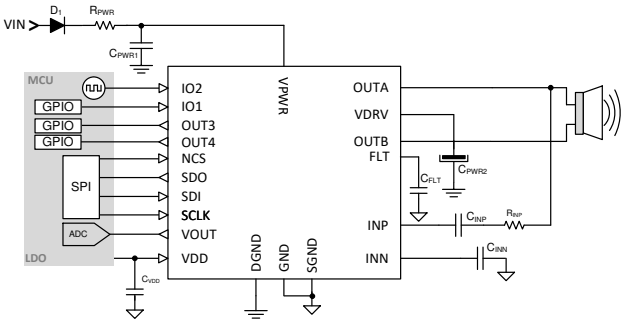
The receive signal path includes a low-noise linear amplifier, a bandpass filter, followed by a logarithmic gain amplifier for input dependent amplification. The logarithmic amplifier allows for high sensitivity for weak echo signals and offers excellent input dynamic range over full range of reflected echoes.

The drivers can be controlled directly through the microcontroller for complete customization of the burst signal, or can be programmed through SPI with a customizable burst length. The TUSS4470 can support a single transducer to send and receive burst signals, or can set up two transducers to split the send and receive functions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSS4470	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TUSS4470 Application Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2018) to Revision A (May 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed all instances of legacy terminology to controller and peripheral where SPI is mentioned	1
• Changed operating free-air temperature minimum from: –25°C to: –40°C	4

5 Pin Configuration and Functions

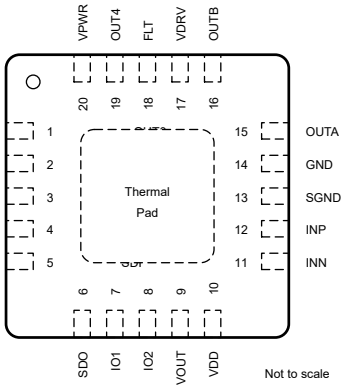


Figure 5-1. RTJ Package 20-Pin WQFN With Exposed Thermal Pad (Top View)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OUT3	O	General-purpose digital output
2	DGND	G	Digital ground
3	NCS	I	SPI negative chip select
4	SCLK	I	SPI CLK
5	SDI	I	SPI data input
6	SDO	O	SPI data output
7	IO1	I	General-purpose digital input
8	IO2	I	General-purpose digital input
9	VOUT	O	Demodulated echo analog output
10	VDD	P	Voltage regulator input
11	INN	I	Negative transducer receive
12	INP	I	Positive transducer receive
13	SGND	G	Sensor ground (quiet)
14	GND	G	Ground
15	OUTA	O	Transducer driver output A
16	OUTB	O	Transducer driver output B
17	VDRV	P	H-bridge driver supply voltage
18	FLT	I/O	Filter components
19	OUT4	O	General-purpose digital output
20	VPWR	P	Input supply voltage

(1) I = input, O = output, I/O = input and output, G = ground, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VPWR}	Supply voltage range	–0.3	40	V
V_{VDD}	Voltage regulator input voltage	–0.3	5.5	V
V_{VDRV}	H-bridge drive voltage	–0.3	V_{VPWR} + 0.3	V
V_{FLT}	Filter component pin	–0.3	V_{VDD} + 0.3	V
V_{INX}	INP, INN pins input voltage	0.5	1.3	V
V_{DIG_IN}	SCLK, SDI, NCS, IOx pin input voltage	–0.3	V_{VDD} + 0.3	V
V_{VOUT}	Analog output voltage	–0.3	V_{VDD} + 0.3	V
V_{DIG_OUT}	SDO, OUTx, IOx pin output voltage	–0.3	V_{VDD} + 0.3	V
V_{OUTA_B}	OUTA, OUTB pins output voltage	–0.3	V_{VDRV} + 0.3	V
T_A	Ambient temperature	–40	105	°C
T_J	Junction temperature	–40	125	
T_{stg}	Storage temperature	–40	125	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage on VPWR pin	5		36	V
V_{VDRV}	Voltage on VDRV pin, internal regulation on VDRV disabled (VDRV_HI_Z=1)(1)	5		36	V
	VDRV voltage Pre driver mode (PRE_DRIVER_MODE=1), internal regulation on VDRV disabled (VDRV_HI_Z=1)(1)	5		15	V
V_{VDIG_IO}	Digital I/O pins	–0.1		V_{VDD}	V
V_{VDD}	Regulated voltage Input	3.1		5.5	V
I_{VPWR_INDIR}	Current consumption at VPWR pin during ranging	150	240	340	µA
I_{VPWR_STDBY}	Current consumption at VPWR in standby mode	150	220	340	µA
I_{VDD_INDIR}	Current consumption at VDD pin during ranging	7	11.5	13	mA
I_{VDD_STDBY}	Current consumption at VDD in standby mode	1.2	1.5	2.5	mA
I_{VDD_SLEEP}	Current consumption in sleep mode			350	µA
T_A	Operating free-air temperature	–40		105	°C
T_J	Operating junction temperature	–40		125	°C

(1) Always $V_{VPWR} > V_{VDRV} + 0.3$ V to prevent reverse current from VDRV pin to VPWR pin

6.4 Thermal Information

THERMAL METRIC[1]		TUSS4470 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power-Up Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PWR_ON}	Time to power up when SPI communication is possible				10	ms
V_{VDRV}	Regulated voltage on VDRV pin[1]	VDRV_VOLTAGE_LEVEL = 0x0; V_{VPWR} > V_{VDRV} + 100 mV	4.5	5	5.3	V
		VDRV_VOLTAGE_LEVEL = 0x4; V_{VPWR} > V_{VDRV} + 100 mV	8.1	9	9.9	
		VDRV_VOLTAGE_LEVEL = 0x7; V_{VPWR} > V_{VDRV} + 100 mV	11.5	12	12.6	
		VDRV_VOLTAGE_LEVEL = 0x8; V_{VPWR} > V_{VDRV} + 100 mV	12.09	13	13.91	
		VDRV_VOLTAGE_LEVEL = 0xC; V_{VPWR} > V_{VDRV} + 100 mV	15.81	17	18.9	
		VDRV_VOLTAGE_LEVEL = 0xD; V_{VPWR} > V_{VDRV} + 100 mV	16.74	18	19.26	
		VDRV_VOLTAGE_LEVEL = 0xE; V_{VPWR} > V_{VDRV} + 100 mV	17.67	19	20.33	
		VDRV_VOLTAGE_LEVEL = 0xF; V_{VPWR} > V_{VDRV} + 100 mV	19.0	20	21.4	
I_{VDRV}	VDRV capacitor charging current	VDRV_CURRENT_LEVEL = 0x0; V_{VPWR} > V_{VDRV} + 1 V	8.5	10	11.5	mA
		VDRV_CURRENT_LEVEL = 0x1; V_{VPWR} > V_{VDRV} + 1 V	17	20	23	

(1) Other VDRV voltage levels possible.

6.6 Transducer Drive

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HS_FET}	High-side MOSFET on-resistance	T_A =+105°C			30	Ω
R_{LS_FET}	Low-side MOSFET on-resistance	T_A =+105°C			20	Ω

6.7 Receiver Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{LNA}	Low-noise amplifier fixed gain	LNA_GAIN = 0x00; f_{DRV_CLK} = 58 KHz	13.7	15	16.8	V/V
G_{LNA}		LNA_GAIN = 0x01; f_{DRV_CLK} = 58 KHz	9.4	10	12	
G_{LNA}		LNA_GAIN = 0x10; f_{DRV_CLK} = 58 KHz	17.6	20	21.8	
G_{LNA}		LNA_GAIN = 0x11; f_{DRV_CLK} = 58 KHz	11.6	12.5	14.2	
DR_{VIN_MIN}	Minimum receive input(2)	LOGAMP_DIS_FIRST=0x0;LOGAMP_DIS_LAST=0x0 LNA_GAIN=0x00; ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500KHz		2.4		µVrms
DR_{VIN_MAX}	Maximum receive input(2)			48		mVrms
SL_{AFE}	Slope of analog front end(4)	VOUT_SCALE_SEL = 0x0; f_{DRV_CLK} = 58 KHz	25	29.7	33	mV/dB
		VOUT_SCALE_SEL = 0x1; f_{DRV_CLK} = 58 KHz	38	45.1	46	
DR_{AFE}	Receiver path dynamic range (minimum to maximum input) (2)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	82		92	dB
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1 ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500 KHz	59		70	
	Receiver path dynamic Range (noise floor to maximum input) (3)	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		84	
BW_{LOG}	Logamp bandwidth	Information only	40		1000	KHz
INT_{LOG}	Intercept point in dBV	LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0; f_{DRV_CLK} = 40 KHz	-108		-97	dBV
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-94		-86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-80		-70	
ERR_{LOG}	Log conformance error	Information only	-3		3	dB
f_{BPF}	Configurable range of center frequency of BPF	BPF_BYPASS = 0x0; BPF_FC_TRIM = 0x0; set by different values of BPF_HPF_FREQ	40		500	KHz
Q_{BPF}	Q of bandpass filter	BPF_BYPASS = 0x0; BPF_Q_SEL = 0x0(1)	3	4	5.2	
R_{LPF}	Internal resistor on FLT pin to ground			6.25		KΩ
V_{O_PDSTL}	Output pedestal level(2)	V_{VDD} = 3.3 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	0.3		0.45	V
		V_{VDD} = 5.0 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0;LOGAMP_DIS_LAST = 0x0	0.45		0.675	

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N\_pk\_pk}$	Output peak-to-peak noise	V_{VDD}=3.3 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x0	50		200	mVpp
		V_{VDD}=5.0 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	75		300	

(1) Other choices of Q possible.
(2) Measured with effectively very large C_{FLT}. Actual minimum signal detectable will depend on $V_{N\_pk\_pk}$. Minimum and maximum input levels are defined by ERR_{LOG}.
(3) Measured with different C_{FLT} values according to Equation 3. Noise floor is set by $V_{N\_PK\_PK}$ in addition to V_{O_PDSTL}.
(4) Slope measured with factory trim at f_{DRV_CLK} = 58 KHz. Slope can be adjusted with LOGAMP_SLOPE_ADJ bits for different f_{DRV_CLK} settings.

6.8 Echo Interrupt Comparator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT_SCALE_SEL = 0x0						
$V_{ECMP\_THR\_0}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.37	0.4	0.43	V
		ECHO_INT_THR_SEL = 0x5	0.56	0.6	0.64	
		ECHO_INT_THR_SEL = 0xA	0.75	0.8	0.85	
		ECHO_INT_THR_SEL = 0xF	0.94	1	1.06	
$V_{ECMP\_HYS\_0}$	Echo interrupt comparator hysteresis		7		68	mV
VOUT_SCALE_SEL = 0x1						
$V_{E\_CMP\_THR\_1}$	Echo interrupt comparator threshold(1)	ECHO_INT_THR_SEL = 0x0	0.56	0.6	0.64	V
		ECHO_INT_THR_SEL = 0x5	0.84	0.9	0.96	
		ECHO_INT_THR_SEL = 0xA	1.13	1.2	1.27	
		ECHO_INT_THR_SEL = 0xF	1.41	1.5	1.59	
$V_{ECMP\_HYS\_1}$	Echo interrupt output threshold level hysteresis		7		68	mV

(1) Other thresholds possible.

6.9 Digital I/O Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_DIGIO}	Digital input high-level	NCS, SDI, SCLK and IOx pins	0.7			V_{VDD}
V_{IL_DIGIO}	Digital input low-level				0.3	V_{VDD}
V_{HYS_DIGIO}	Digital input hysteresis		100			mV
V_{OH_DIGIO}	Digital output high-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = – 1 mA	V_{VDD} – 0.1			V
V_{OL_DIGIO}	Digital output low-level(1)	SDO, OUTx pins; I_{DIGIO_OUT} = 1 mA			0.1	V
V_{O_CAP}	Maximum output load capacitance	SDO pin. Information Only			10	pF
R_{PU_DIGIO}	Digital input pullup resistance to VDD	NCS, IO1, IO2 pins	80	100	130	kΩ
R_{PD_DIGIO}	Digital Input pulldown resistance to GND	SCLK, SDI pins	80	100	130	kΩ

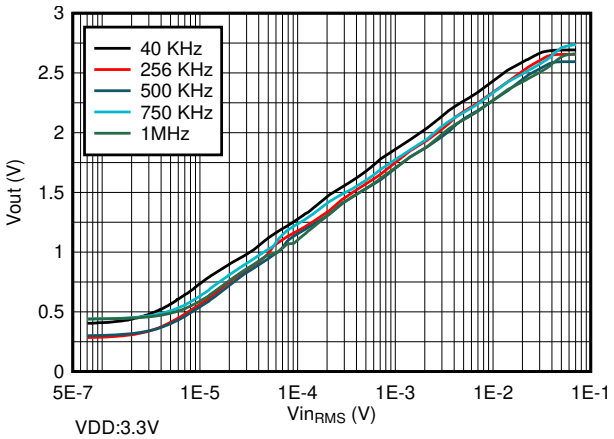
(1) No short-circuit protection on output pins. Damage may occur for currents higher than specified.

6.10 Switching Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

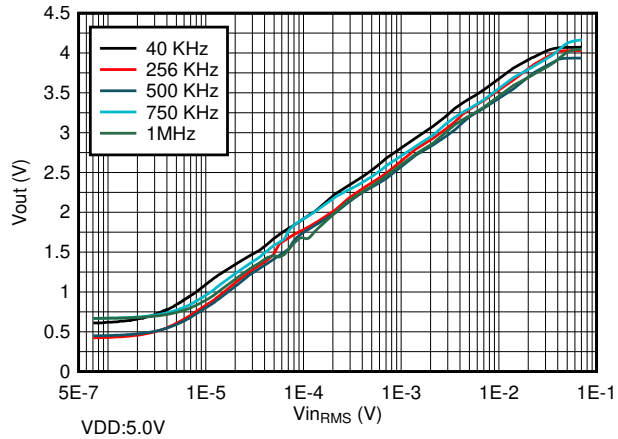
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{DRV_CLK}	Frequency of drive clock at IO1 and IO2 pin ; depends on the VDRV voltage	Used as burst frequency; PRE_DRIVER_MODE = 0x0	40		1000	KHz
	Frequency of drive clock at IO1 and IO2 pin	Used as burst frequency; PRE_DRIVER_MODE = 0x1; Load cap on OUTA/OUTB = 2nF	40		440	KHz
SPI_{RATE}	SPI bit rate				500	KHz

6.11 Typical Characteristics



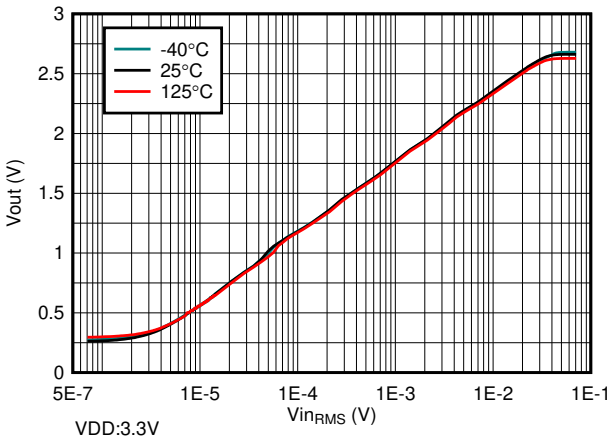
VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-1. Receive Signal Path Transfer Function for VDD = 3.3 V



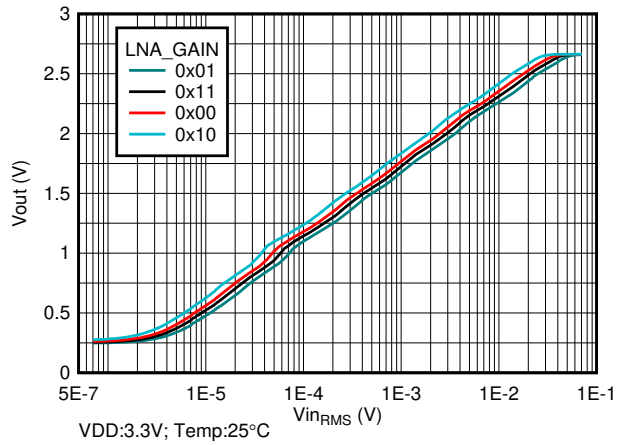
VDD:5.0V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x1
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-2. Receive Signal Path Transfer Function for VDD = 5 V



VDD:3.3V
F_c:256KHz
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

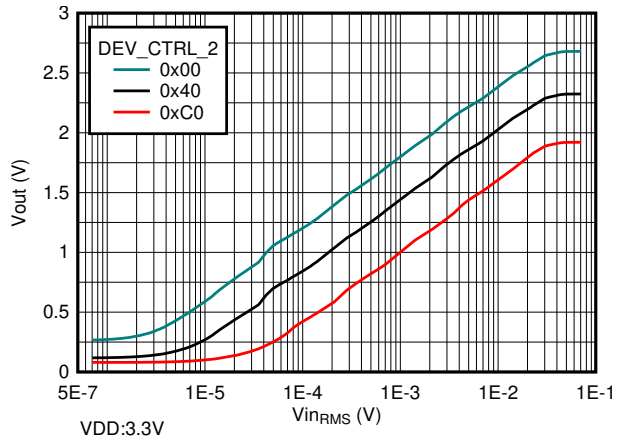
Figure 6-3. Receive Signal Path Transfer Function Across Temperature



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

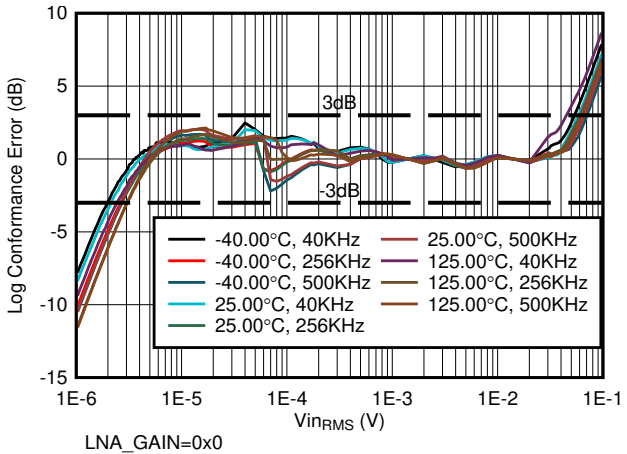
Figure 6-4. Receive Signal Path Transfer Function Across LNA Gain

6.11 Typical Characteristics (continued)



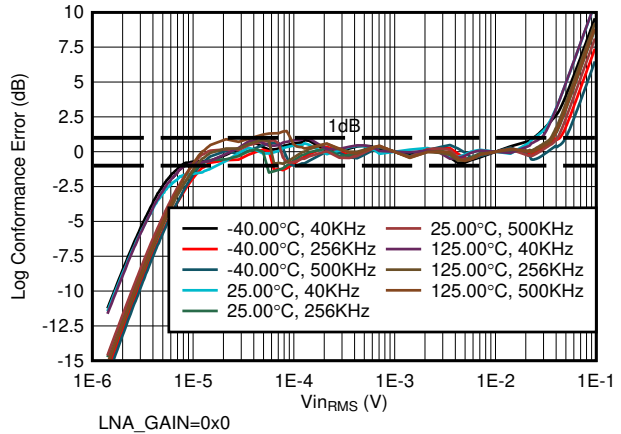
VDD:3.3V
F_c:256KHz
Temp:25°C

Figure 6-5. Receive Signal Path Transfer Function for Various Logamp Stages Disabled



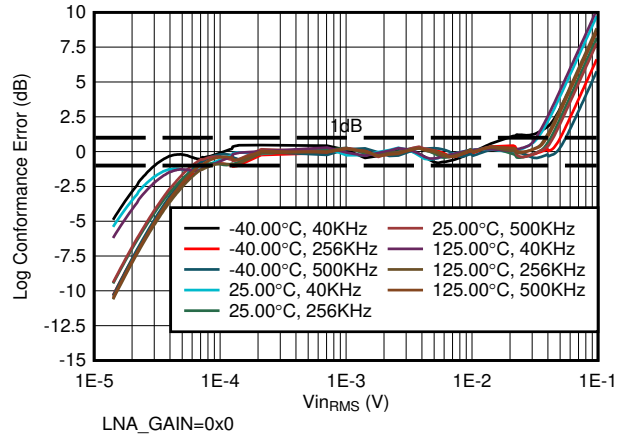
LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-6. Receive Signal Path Log Conformance Error With All Stages Enabled



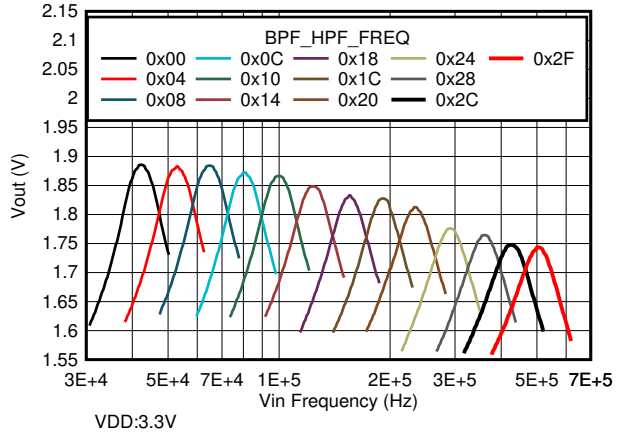
LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x1

Figure 6-7. Receive Signal Path Log Conformance Error With Last Stage Disabled



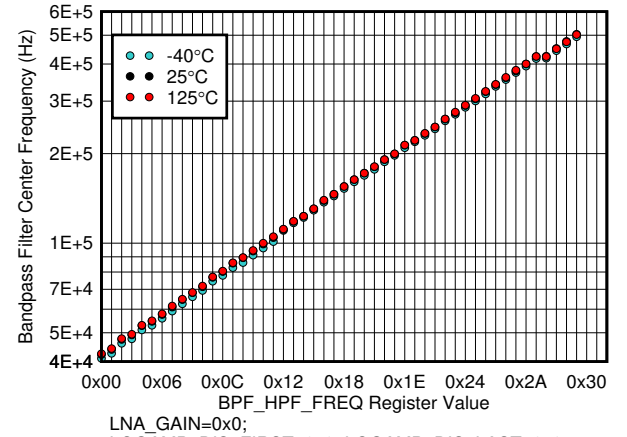
LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x1; LOGAMP_DIS_LAST=0x1

Figure 6-8. Receive Signal Path Log Conformance Error With First and Last Stage Disabled



VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

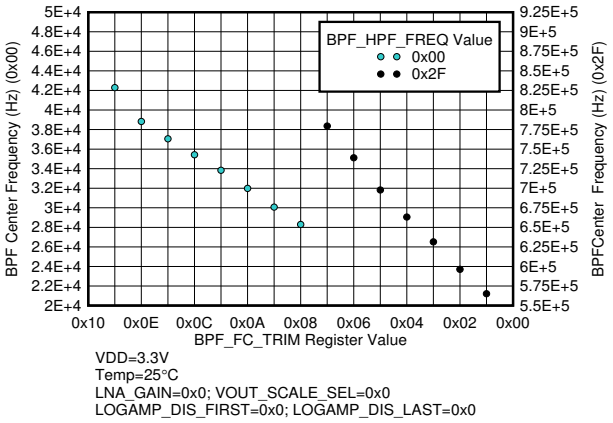
Figure 6-9. Receive Signal Path Bandpass Filter Transfer Function



LNA_GAIN=0x0;
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

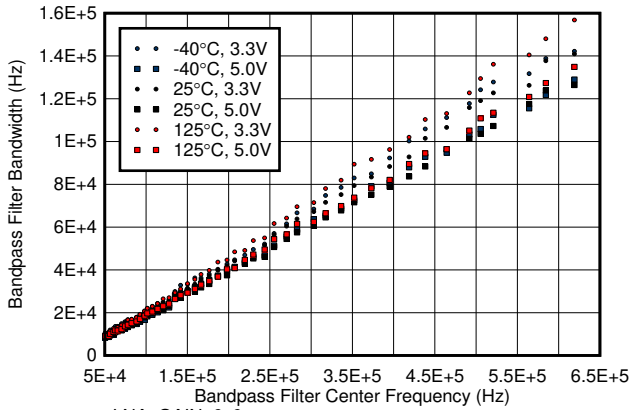
Figure 6-10. Receive Signal Path Bandpass Filter frequency for Various Register Settings

6.11 Typical Characteristics (continued)



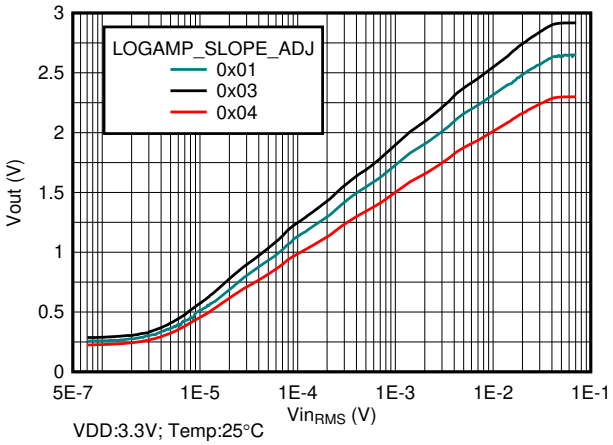
VDD=3.3V
Temp=25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-11. Receive Signal Path Bandpass Filter Center Frequency Trim



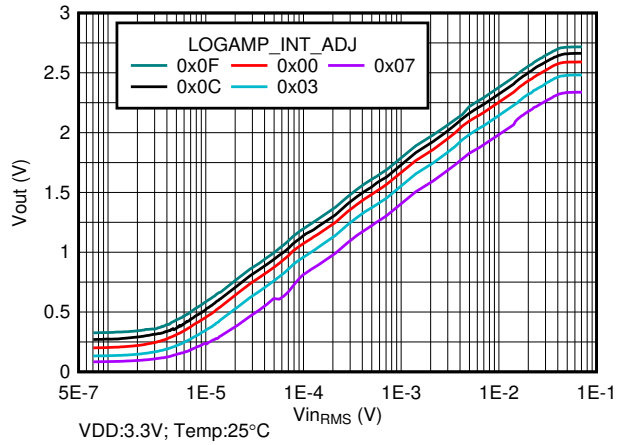
LNA_GAIN=0x0
BPF_Q_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-12. Receive Signal Path Bandpass Filter Bandwidth for Various Center Frequency Settings



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 6-13. Receive Signal Path Transfer Function for Various Slope Adjustments



VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

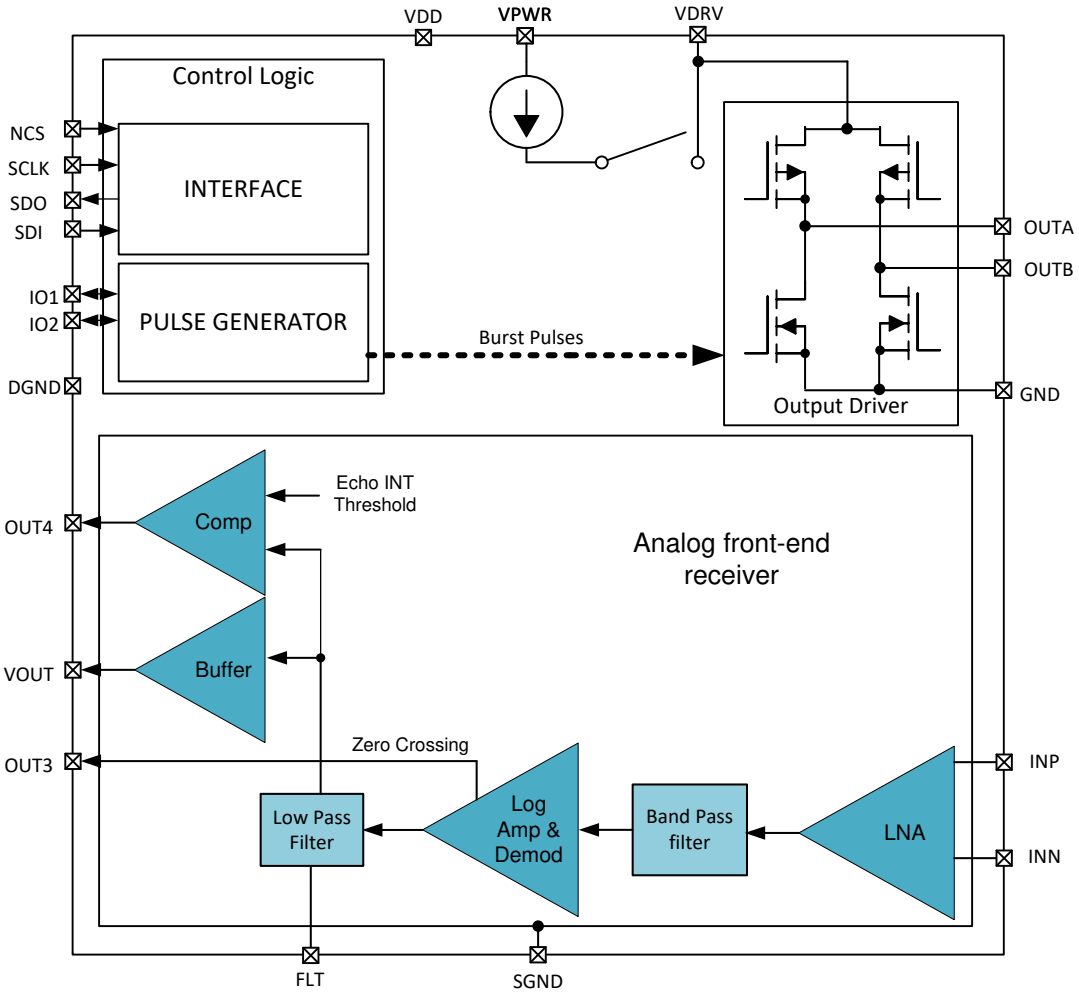
Figure 6-14. Receive Signal Path Transfer Function for Various Intercept Adjustments

7 Detailed Description

7.1 Overview

The TUSS4470 is a highly integrated driver and receiver IC designed especially for ultrasonic transducers operating between the range of 40 KHz to 1 MHz. The TUSS4470 integrates an H-bridge to drive the transducer directly. This is useful in applications where the receive transducer sensitivity is high and large driving voltage is not required to create sufficient sound pressure level and where short distance measurements are needed. The driver stage has flexible and configurable controls set through the SPI interface or through digital input pins that can be driven by an external MCU. The receive stage consists of a logarithmic amplifier receive chain. The logamp enables the TUSS4470 to have a wide dynamic input range. This enables applications where objects with different physical properties must be detected with the same sensor. A key advantage of the TUSS4470 is that it integrates a bandpass filter that can be tuned to the center frequency of the transducer. A demodulated analog output representing the receive echo, the zero crossing of the input signal, and a simple threshold crossing indicator enable a variety of end applications from complex object detection to simple presence detection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excitation Power Supply (VDRV)

The TUSS4470 device includes a current source which charges a capacitor connected to the VDRV pin. The VDRV pin serves as the power supply for the integrated H-Bridge driver circuit The voltage on the VDRV pin (V_{VDRV}) is controlled by an internal voltage monitor which can be configured by the VDRV_VOLTAGE_LEVEL

bits. The current source is switched off after VDRV pin voltage crosses the configured V_{VDRV} value. The charging current (I_{VDRV}) can be configured using VDRV_CURRENT_LEVEL bits.

In applications where VPWR can vary over a wide range, this allows the transducer drive voltage to be fixed for every burst for a deterministic sound pressure level created by the transducer. This is possible only when the minimum supply voltage on the VPWR pin is greater than the configured value of V_{VDRV}.

The VDRV regulation is disabled at device power up indicated by VDRV_HI_Z bit being set. To enable VDRV this bit must be cleared. This feature enables applications where the the H-Bridge driver supply is connected to an external power supply source through the VDRV pin.

Note

- When VDRV pin is supplied from an external power supply, it must be ensured that all times including during power up, $V_{VPWR} > V_{VDRV} + 0.3$ V to prevent any reverse current from VDRV pin to VPWR pin. Alternatively a reverse current prevention diode can be used on VPWR pin as shown in Figure 8-1 (D1).
- Very fast ramp-up rate on VPWR pin should be avoided to prevent damage to the device. If fast ramp rates are possible, a series resistor between power supply and VPWR pin as shown in Figure 8-1 (R_{PWR}) is recommended.

After a burst is completed and during the long receive time (listen mode), the capacitor on VDRV pin will discharge causing the charging current to turn on intermittently. This can inject switching noise which can be picked by the analog front end as a spurious echo. To eliminate this noise, the DIS_VDRV_REG_LSTN bit can be set. This disables charging of VDRV automatically after the burst is done. The VDRV charging current can be turned on again by setting the VDRV_TRIGGER bit. Setting this bit may create a spurious echo which can be ignored by the echo processing in the MCU. The VDRV_READY bit in DEV_STAT register can be monitored to know when the required voltage level has been reached and the device is ready to generate a new burst. The VDRV_TRIGGER bit must be un-set through SPI just before the start of burst and will have to be set again for next charging cycle. If the VDRV_TRIGGER bit is not un-set before next burst cycle, the VDRV charging current will not be automatically disabled after the burst even when DIS_VDRV_REG_LSTN is set. This functionality is ignored when the VDRV_HI_Z bit is set.

7.3.2 Burst Generation

TUSS4470 has multiple modes to excite the transducer through OUTA and OUTB pins. For each of the modes, the desired frequency of burst is supplied through an external clock on the IOx pins. This enables the user to supply a highly precise clock calibrated to the center frequency of transducer to enable the highest sound pressure level generation. These modes can be selected by the IO_MODE bits in the DEV_CTRL_3 register.

The burst mode is enabled first, then the start of burst (OUTA/OUTB changing states) happens at the next falling edge of IO1 or IO2, depending on the mode selected. These modes are described below.

- **IO_MODE = 0:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled by setting the CMD_TRIGGER in the TOF_CONFIG register through SPI, as shown in Figure 7-1. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. The end of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent, or when the CMD_TRIGGER = 0 is set through SPI, whichever occurs earlier. TI recommends that IO2 is held high before burst enable to count the number of pulses correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of CMD_TRIGGER from high to low to high again is required to initiate a new burst sequence.

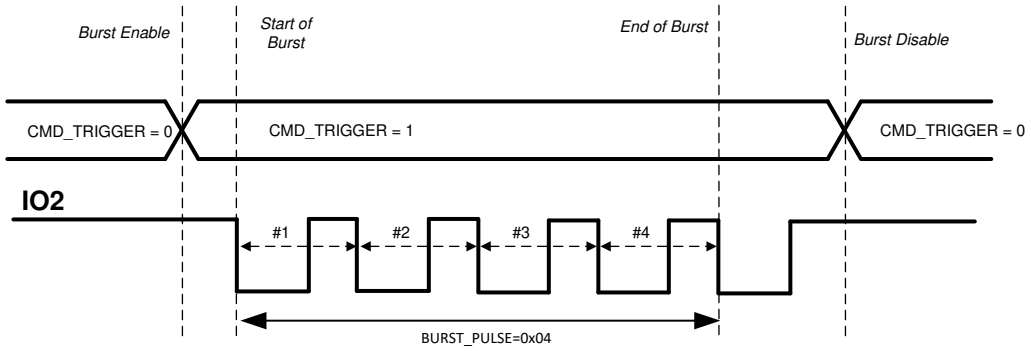


Figure 7-1. IO_MODE 0 Description

- **IO_MODE = 1:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled when IO1 pin transitions low (see Figure 7-2). The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent or IO1 transitions high, whichever occurs earlier. TI recommends that IO2 is held high before start of burst to count the number of pulse correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. A transition of IO1 from low to high to low again is required to initiate a new burst sequence.

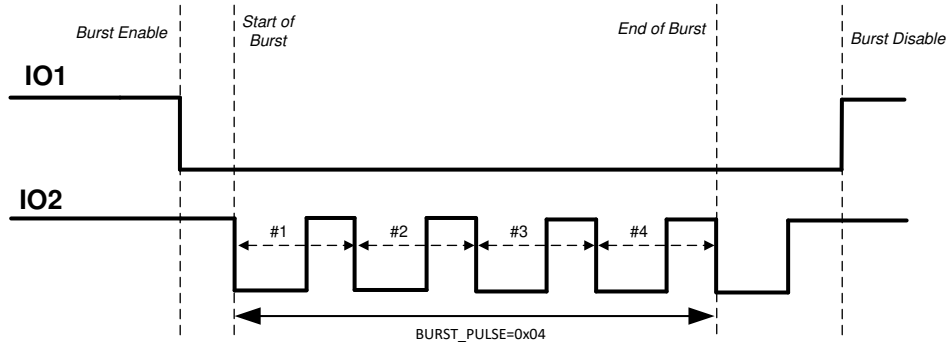


Figure 7-2. IO_MODE 1 Description

- **IO_MODE = 2:** In this mode both IO1 and IO2 are used to control OUTA and OUTB. The burst enable is triggered when either IO1 or IO2 transitions from high to low. Start of burst (OUTA and OUTB changing state) happens only at the next falling edge of IO1. Figure 7-3 shows the case where a high-to-low transition on IO2 is used to enable the burst. A burst is emulated when IO1 and IO2 are toggled in a non-overlapping sequence. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins. During a burst, if there is a condition where both IO1 and IO2 are high for more than half period of the internal clock f_{INT_CLK} (caused by differential delays due to PCB parasitics or MCU code), an end of burst and burst mode disable will be triggered. Any falling edge just after this condition will be ignored to toggle OUTA and OUTB as it would be considered as a new burst enable signal. A systematic condition of overlap can cause a continuous end of burst trigger such that OUTA and OUTB do not toggle even though IO1 and IO2 are toggling. TI recommends no overlap or minimum non-overlap between the IO1 and IO2 signals when measured at the pins. BURST_PULSE has no effect in this mode.

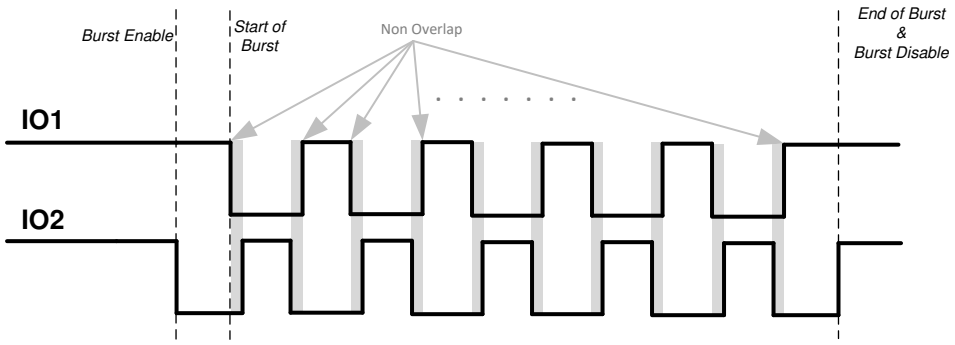


Figure 7-3. IO_MODE 2 Description

- **IO_MODE = 3:** In this mode, burst enable and start of burst are both triggered by the falling edge of IO2. TI recommends that IO2 pin is kept pulled up to VDD for this mode. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins (see Figure 7-4). The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent. After end of burst, a blank-out timer interval defined by the DRV_PLS_FLT_DT register is started to prevent triggering of a new start of burst in the event if the IO2 pin is still toggling. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins.

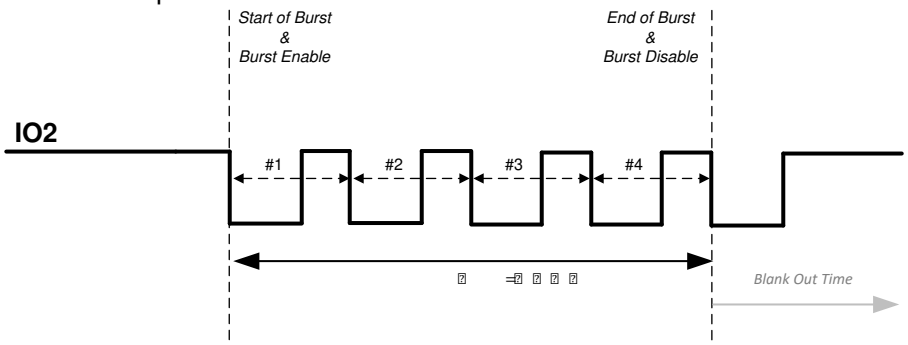


Figure 7-4. IO_MODE 3 Description

Note

- For IO_MODE 0 and 1, by setting BURST_PULSE = 0, the device will generate continuous burst pulses on OUTA and OUTB until the end of burst is signaled through SPI or the IO1 pin, respectively. Continuous bursting is not available for IO_MODE=3.
- A higher noise floor at the VOUT pin is expected in continuous mode where one transducer is used to transmit burst signals and another transducer is used to receive, as the switching noise of the digital IO pins can couple into the highly sensitive analog front end for the receive channel. This also applies to the single transducer use case where a continuous clock is applied on IO2 pin when the device is in indirect or listening mode.
- The range for frequency of switching for the output drivers is given by f_{DRV_CLK} parameter in the *Switching Characteristics* table.
- When the device is not in direct sensing or bursting mode, the device is always in indirect sensing or listening mode.

7.3.2.1 Burst Generation Diagnostics

In IO_MODE 0, 1 and 3, a pulse number diagnostic is active after start of burst (not when the burst is enabled) to monitor if the correct number of pulses (as set in BURST_PULSE) were generated before the end of burst was signaled through SPI or the IO1 pin. A fault, if detected, is then reported through the PULSE_NUM_FLT bit.

The pulse duration after start of burst (not when the burst is enabled) is monitored to detect a stuck condition, which will keep the FETs on OUTA or OUTB turned on. This can happen because of loss of external clock

or the driving signal on IO1 and IO2 pins being stuck in one state. The device expects to see a toggle on IOx pins (based on IO_MODE) within the time period as defined in the DRV_PLS_FLT_DT register. If this diagnostic triggers, it will force an end of burst. The fault is reported by setting the DRV_PULSE_FLT bit. If a DRV_PULSE_FLT is set in IO_MODE 0, 1 and 3—and the programmed number of pulses were not sent before end of burst—the PULSE_NUM_FLT will also be set.

Note

- The DRV_PULSE_FLT bit is cleared when a new start of burst is triggered, when DRV_PLS_FLT_DT = 0x7 is set, or if the device is put into Standby or Sleep mode.
- The PULSE_NUM_FLT bit is cleared when a new start of burst is triggered, or if the device is put into Standby or Sleep mode.

7.3.3 Direct Transducer Drive

Figure 7-5 shows the internal structure for driving an ultrasonic transducer connected directly to the device output using an H-bridge output stage. This configuration drives 2 × V_{VDRV} as the peak-to-peak voltage across the transducer. The voltage on VDRV pin can be set as described in the *Excitation Power Supply (VDRV)* section.

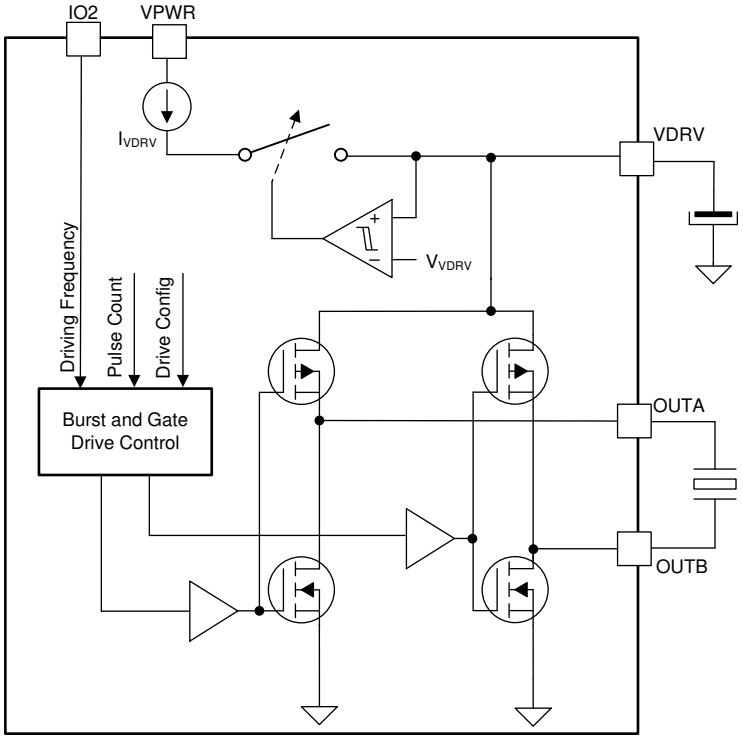


Figure 7-5. Direct Drive Configuration Using Internal FETs

Figure 7-5 shows the most common application case for the TUSS4470 device, in which the output driver pulses the two half-bridges out-of-phase. It is also possible to use the driver in half-bridge mode by setting the HALF_BRG_MODE bit. In this mode, only V_{VDRV} is applied across the transducer. This mode is useful for transducers where one side of the membrane must be always grounded.

The device can also be configured as a pre-driver to drive external FETs or BJTs to drive higher current and voltage into the primary side of the transformer, as shown in Figure 7-6, by setting the PRE_DRIVER_MODE bit. The high-side and low-side devices are used to drive the external low-side drivers. The VDRV voltage level can be configured to ensure that the OUTA and OUTB voltages do not violate the V_{GS} or V_{BE} specification for external the FET or BJT, respectively. In the configuration shown in Figure 7-6, it is possible to use a voltage (VBOOST) which is higher than the supply of the system for generating higher voltage across the transducer.

Refer to *Application and Implementation* for an application diagram and information on how the polarity and state of OUTA and OUTB pins are defined with respect to IO1 and IO2 pin states and other register settings.

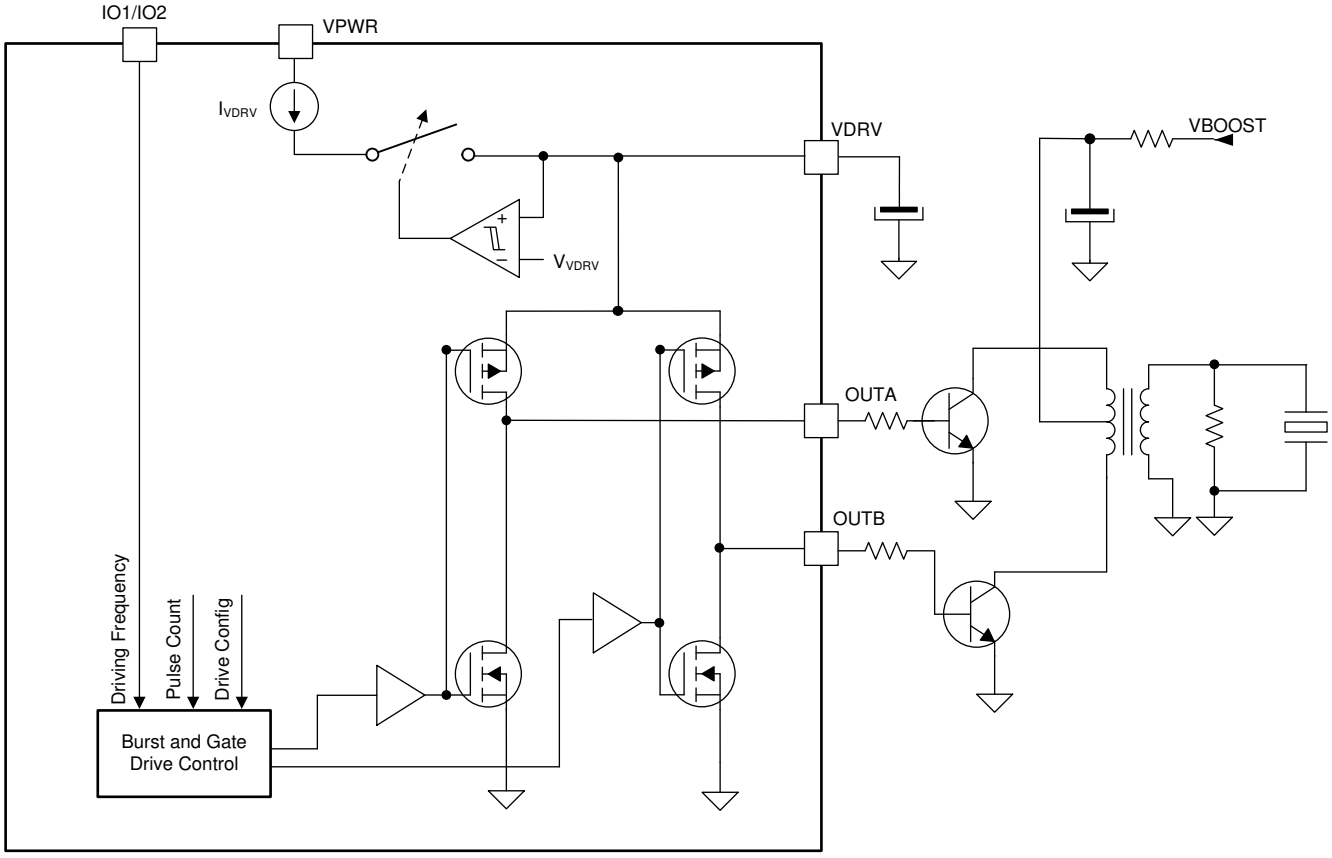


Figure 7-6. Center-Tap Transformer Drive Using External FETs

7.3.4 Analog Front End

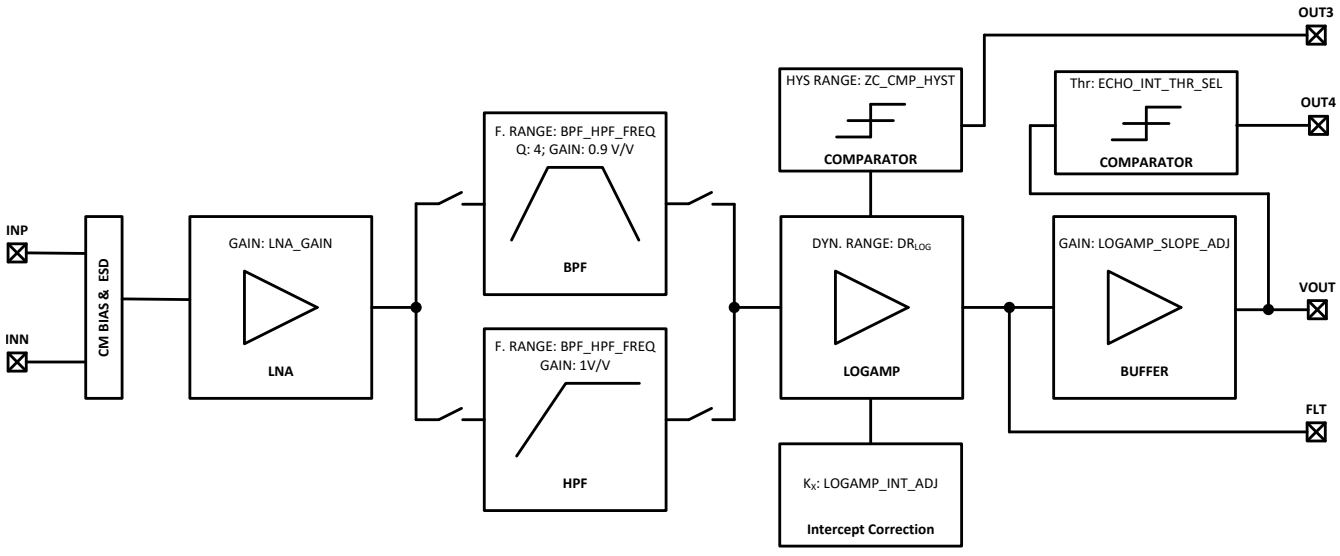


Figure 7-7. TUSS4470 Analog Front-End Block Diagram

Figure 7-7 shows the analog front-end block diagram that can receive and condition the signals from the transducer during listen mode. The received echo is first amplified with a fixed linear low-noise amplifier, followed

by either a bandpass filter or a high-pass filter to remove noise out of the expected signal band. After filtering the signal, the signal is fed into a logarithmic amplifier. The output of the logarithmic amplifier is then buffered to the VOUT pin. In Figure 7-7, every block has the register name associated with it that can be used to configure the signal path. The final equation for the signal path is given by Equation 2:

$$V_{OUT} = G_{VOUT} \cdot SL_{LOG} \cdot 20\log_{10}\left(\frac{G_{LNA} \cdot G_{BPF} \cdot V_{IN}}{INT_{LOG} \cdot K_X}\right) \quad (1)$$

where

- G_{VOUT} is set by the LOGAMP_SLOPE_ADJ bits.
- SL_{LOG} is slope of logarithmic amplifier as specified in the *Receiver Characteristics* table.
- G_{LNA} is set by the LNA_GAIN bits.
- G_{BPF} is typically 0.9V/V.
- V_{IN} is the input V_{INP}
- INT_{LOG} is logarithmic amplifier intercept specified in the *Receiver Characteristics* table.
- K_X is the log intercept adjustment set by the LOGAMP_INT_ADJ bits.

The bandpass filter is critical for reducing noise to allow utilization of the complete dynamic range of the logarithmic amplifier. The center frequency of the bandpass filter can be configured to be close the transducer frequency which is set by the BPF_HPF_FREQ bits. Table 7-1 shows the nominal values for the BPF center frequency corresponding to the BPF_HPF_FREQ register value. The TUSS4470 supports a wide range of frequencies, therefore a factory trim is used to remove process variation for a particular pre-determined frequency. It is possible that all other frequencies listed in Table 7-1 do not correspond exactly to value of BPF_HPF_FREQ in a factory trim. The user can vary the value of the BPF_HPF_FREQ register around the desired center frequency while actively bursting and observing the VOUT signal. The value with maximum voltage at VOUT pin will the desired setting for the BPF_HPF_FREQ register.

Table 7-1. Bandpass Filter Center Frequency Configuration

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x00	40.64
0x01	44.05
0x02	45.6
0x03	48.86
0x04	50.58
0x05	52.96
0x06	56.75
0x07	60.11
0x08	62.95
0x09	66.68
0x0A	71.44
0x0B	74.81
0x0C	79.24
0x0D	82.03
0x0E	86.89
0x0F	92.04
0x10	97.49
0x11	103.27
0x12	109.4
0x13	114.54
0x14	121.33
0x15	128.52

Table 7-1. Bandpass Filter Center Frequency Configuration (continued)

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F_c (KHz)
0x16	134.58
0x17	142.55
0x18	151.01
0x19	159.94
0x1A	167.48
0x1B	177.41
0x1C	185.77
0x1D	196.78
0x1E	206.05
0x1F	218.26
0x20	228.54
0x21	244.89
0x22	256.43
0x23	271.63
0x24	284.43
0x25	301.28
0x26	319.13
0x27	338.14
0x28	353.97
0x29	374.95
0x2A	397.16
0x2B	408.17
0x2C	420.7
0x2D	455.63
0x2E	472.03
0x2F	500

The factory trim can be overridden by setting the BPF_FC_TRIM_FRC bit first and varying the BPF_FC_TRIM bit after. This is useful in two ways:

- If the factory trimmed bandpass filter center frequency is higher than the desired value for BPF_HPF_FREQ = 0x00, or lower than desired value for BPF_HPF_FREQ = 0x2F, then BPF_FC_TRIM can be used to recover the range.
- This setting can also be used to extend the frequency range of the bandpass filter center frequency.

The BPF_FC_TRIM acts like an offset on top of the BPF_HPF_FREQ setting. Table 7-2 shows the nominal value of center frequency when this offset is added to the minimum and maximum BPF_HPF_FREQ code. Figure 6-11 shows the measured data. For BPF_HPF_FREQ values greater than 0x08 and less than 0x27, varying BPF_FC_TRIM keeping BPF_HPF_FREQ fixed is the same as setting BPF_FC_TRIM = 0x00 and varying BPF_HPF_FREQ to find the optimum setting.

Table 7-2. Bandpass Filter Center Frequency Range Extension

BPF_HPF_FREQ (hex) + BPF_FC_TRIM (hex) (BPF_FC_TRIM_FRC = 1)	BPF_F_c (KHz)
0x00 + 0x8	27.48
0x00 + 0x9	29.44
0x00 + 0xA	30.83
0x00 + 0xB	31.19
0x00 + 0xC	32.65

Table 7-2. Bandpass Filter Center Frequency Range Extension (continued)

BPF_HPF_FREQ (hex) + BPF_FC_TRIM (hex) (BPF_FC_TRIM_FRC = 1)	BPF_F_c (KHz)
0x00 + 0xD	34.19
0x00 + 0xE	35.8
0x00 + 0xF	38.81
0x2F + 0x1	523.56
0x2F + 0x2	554.59
0x2F + 0x3	587.45
0x2F + 0x4	622.23
0x2F + 0x5	651.58
0x2F + 0x6	690.19
0x2F + 0x7	731.09

Note

- The Q factor of the filter is specified in the *Receiver Characteristics* table, and can be selected by the BPF_Q_SEL bits.
- The bandpass filter can also be converted into a high-pass filter by setting the BPF_BYPASS bit for transducer frequencies in the range above what is shown in Table 7-1. The corner frequency for high-pass filter is also controlled by the BPF_HPF_FREQ bits.
- BPF_Q_SEL and BPF_FC_TRIM have no effect when BPF_BYPASS = 1.

The logamp provides compression for large signal inputs and amplifies linearly small signal inputs. Logamp simplifies system design to detect varying strengths of echoes that happens because of difference in reflectivity of different types of objects and objects at different distances. It automatically adjusts its gain based on the input signal level. The logamp also demodulates the incoming signal.

The logamp consists of multiple gain stages and range extension stages that are combined to give a logarithmic response. The current consumption of the device can be reduced by turning off the either the first stage, the last stage of the logamp, or both, by setting the LOGAMP_DIS_FIRST and LOGAMP_DIS_LAST bits. Disabling the stages will reduce the input dynamic range on the lower side of the range (see Figure 6-4). The pedestal noise floor will be lower because the gain stages are disabled, but the minimum detectable signal value becomes higher due to the reduced dynamic range. Depending on the received input signal strength, stages can be disabled to get optimum object detection. For very small inputs, all stages should be enabled to get maximum input dynamic range even though the noise floor is higher. Figure 6-6, Figure 6-7, and Figure 6-8 show the effect on the log conformance error when all stages are enabled, when the last stage is disabled, and when both first and last stages are disabled. When stages are disabled, a lower error is obtained with a lower noise floor, but the input dynamic range is reduced.

At the output of the logamp, the user can apply an adjustment to the intercept of the logamp curve. This is denoted by the K_X factor in Equation 1. The intercept adjustment is controlled by the LOGAMP_INT_ADJ bits. Table 7-3 shows the nominal values of K_X factor corresponding to register values, and Figure 6-14 shows its effect on the transfer function.

Table 7-3. Logamp Intercept Adjustment

LOGAMP_INT_ADJ	K_X
0x00	1
0x01	1.155
0x02	1.334
0x03	1.54
0x04	1.778
0x05	2.054

Table 7-3. Logamp Intercept Adjustment (continued)

LOGAMP_INT_ADJ	K_X
0x06	2.371
0x07	2.738
0x08	1
0x09	0.931
0x0A	0.866
0x0B	0.806
0x0C	0.75
0x0D	0.698
0x0E	0.649
0x0F	0.604

The output of the logamp is filtered using a low-pass filter to remove the high-frequency components and provide a sufficient peak hold time for the demodulated envelope signal. The cut-off frequency of the low-pass filter is set by the internal impedance of the FLT pin and the value of an external capacitor connected to the pin. As this filter capacitance (C_{FLT}) suppresses the high frequency fluctuations, it also slows down the response time of the logamp. Higher C_{FLT} capacitance will result in lower peak-to-peak voltage variations at VOUT, and slower rise and fall times for the VOUT voltage to reach its maximum value for a given input signal. A nominal value can be calculated using Equation 3, and must be optimized depending on the application.

The output of the low-pass filter is buffered to the VOUT pin using an internal buffer. The buffer is designed to support an ADC input of a MCU. It is possible to change output dynamic range of the VOUT buffer using the VOUT_SCALE_SEL bit. Once the range is set, the gain of the VOUT buffer can be set by the LOGAMP_SLOPE_ADJ bits. The slope variation of the receiver analog front end is show in Figure 6-13.

Echo interrupt signal is available on the OUT4 pin that goes high when the signal on the VOUT pin crosses a threshold as defined by the ECHO_INT_THR_SEL bits. As long as the VOUT signal is higher than this threshold, the echo interrupt signal is held high. The signal goes low asynchronously when the VOUT signal drops below the programmed threshold. This signal can be used to interrupt a MCU when an object has been detected. The threshold value is also dependent on the setting of the VOUT_SCALE_SEL bit.

A zero-crossing signal is output at the OUT3 pin which can be used to validate the frequency of the received echo signal to provide robustness against interference from other signals. This zero-crossing signal is derived from the raw amplified input signal from a particular stage as it is being demodulated in the logamp block. This function is disabled at device power up. but can be enabled by setting the ZC_CMP_EN bit. When enabled, the ZC_CMP_STG_SEL bits are used to select which logamp gain stage is used to generate the zero crossing signal while the ZC_CMP_HYST bits control the hysteresis of the zero-crossing comparator. The stage selection to see the OUT3 pin toggling depends on the strength of signal received by the logamp and has to be configured depending on the application. For large amplitude of input signal, a lower stage of the logamp should be selected, whereas for lower amplitude signal, a higher stage should be selected. To avoid switching noise generated by the toggling of the zero-crossing comparator when the ZC_EN_ECHO_INT bit is set, the zero-crossing output will be only enabled while the echo interrupt signal is high.

7.4 Device Functional Modes

The device has four functional modes:

Sleep Mode — Ultra-low current consumption sleep mode

In this mode, all major blocks of the device are disabled, including VDRV regulation. The SPI interface is still active. This transition into and out of this mode is done using the SLEEP_MODE_EN register bit. Upon issuing a command to exit this mode, the device transitions to other modes only when the VDRV pin reaches the programmed regulation voltage.

Standby Mode

Low current standby mode

In this state, the VDRV regulation is active, but other analog blocks are shut down to reduce quiescent current consumption. The STDBY_MODE_EN bit is used to enter and exit this mode through SPI. The device can transition very quickly from this state to one of the active states for bursting and listening.

Listen Mode

Default mode of the device

This is the default mode of the device when it is not in Sleep mode or Standby mode. In this mode, there is no activity on the transmitter block and the device is actively listening for any ultrasonic signals.

Burst Mode

Mode in which the device is enabled to start a burst to drive the transducer

In this mode, the transmitter blocks are active and enabled to drive the transducer depending on when the start of burst occurs. The receiving path is also active at the same time listening for signals at the input. This mode is entered when a burst enable event occurs and exited when an end of burst occurs as described in *Burst Generation* section.

Figure 7-8 shows an example of the transitions between the different modes of the device for IO_MODE = 0, where the burst is activated through a SPI command and end of burst occurs as the number of programmed pulses are sent.

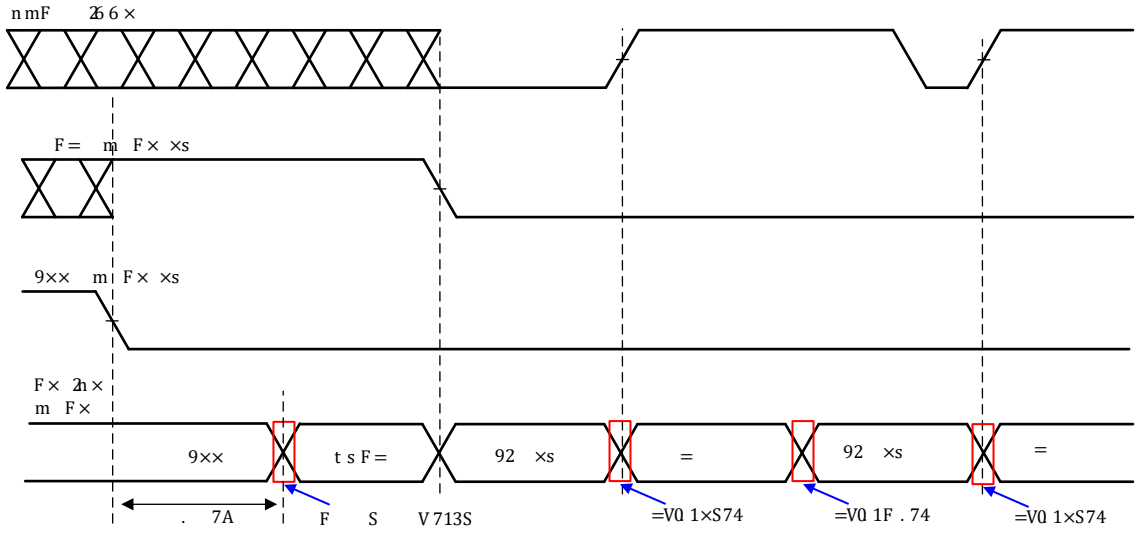


Figure 7-8. Device Modes Timing Diagram

Note

- The transition to standby or active mode (listen or burst) from power-up or sleep mode is done only once the VDRV voltage crosses the programmed VDRV_VOLTAGE_LEVEL bit, or is higher 64 ms, whichever occurs earlier.
- In the case when VDRV is disabled, the device immediately transitions from power or sleep mode to standby and active modes.

7.5 Programming

The primary communication between the IC and the external MCU is through an SPI bus that provides full-duplex communications in a controller-peripheral configuration. The external MCU is **always** a SPI controller that sends command requests on the SDI pin and receives device responses on the SDO pin. The device is **always** a SPI peripheral device that receives command requests and sends responses to the external MCU over the SDO line. The following lists the characteristics of the SPI:

- The SPI is a 4-pin interface.
- The frame size is 16 bits and is assigned as follows:

Controller-to-peripheral (MCU to TUSS4470 over the SDI line)	1 RW bit, 6 bits for the register address, 1 ODD parity bit for entire SPI frame, 8 bits for data
Peripheral-to-controller (TUSS4470 to MCU over the SDO line)	1 bit for Controller Parity error reporting during previous frame reception, 6 bits for the status, 1 bit for ODD parity for entire SPI frame, 8 bits for data

- SPI commands and data are shifted with the MSB first and the LSB last.
- The SDO line is sampled on the falling edge of the SCLK pin.
- The SDI line is shifted out on the rising edge of the SCLK pin.

The SPI communication begins with the NCS falling edge and ends with the NCS rising edge. The NCS high-level maintains the SPI peripheral-interface in the RESET state. The SDO output is in the tri-state condition.

The SPI does not support *back-to-back* SPI frame operation. After each SPI transfer the NCS pin must go from low to high before the next SPI transfer can begin.

Figure 7-9 shows an overview of a complete 16-bit SPI frame.

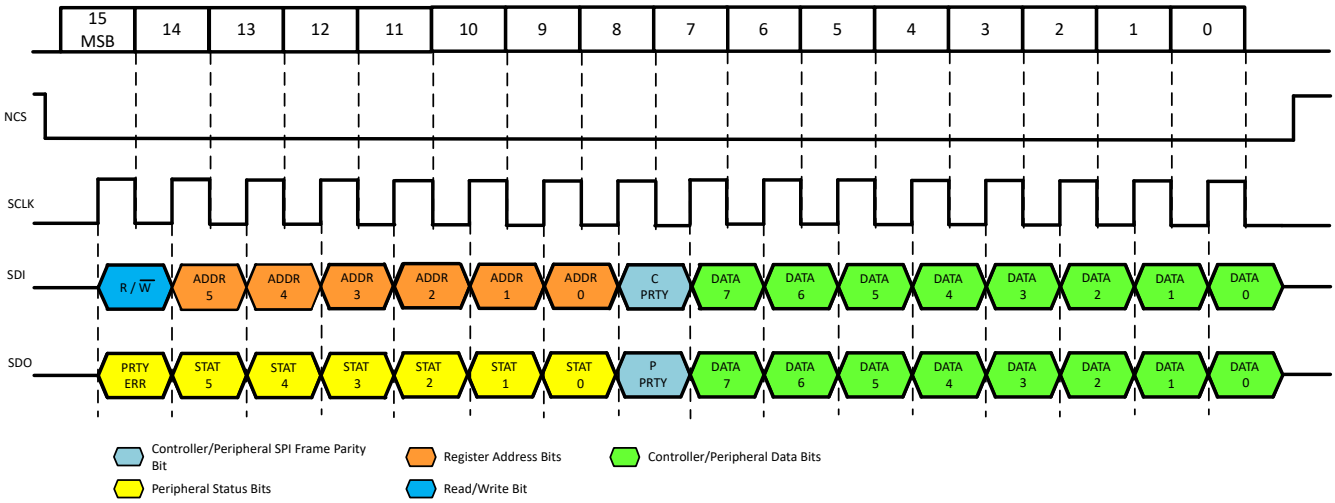


Figure 7-9. 16-Bit SPI Frame

Figure 7-10 shows a SPI transfer sequence between the controller and the peripheral TUSS4470 device. When the controller is writing a SPI frame, the parity error bit indicates if there was a parity error for the previous frame. When the controller is transmitting the data for the SPI write, the peripheral echoes back register address that was sent just before in the command.

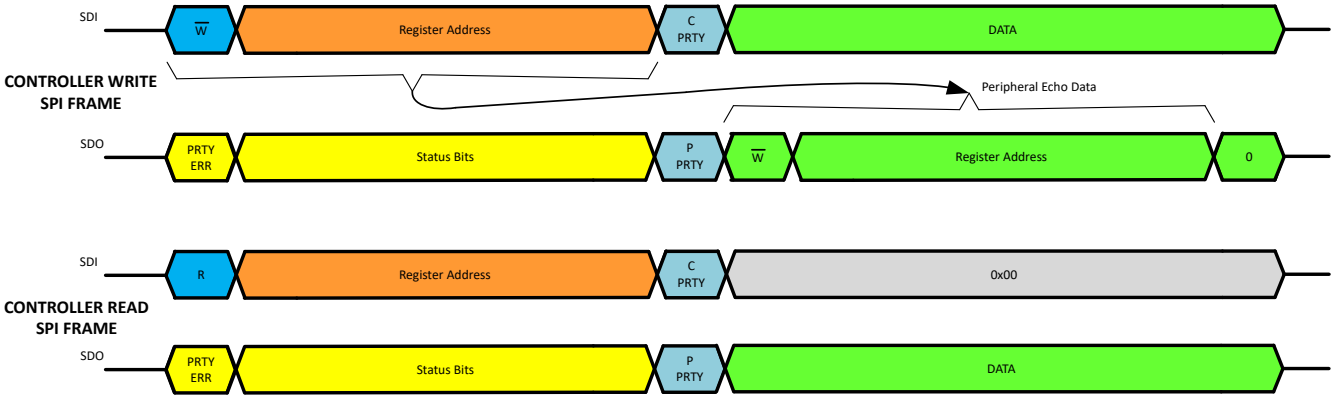


Figure 7-10. SPI Transfer Sequence

The status bits are defined in Table 7-4:

Table 7-4. SPI Interface Status Bits Description

STATUS BIT	DESCRIPTION
STAT 5 - VDRV_READY	Set when VDRV power regulator has reached the programmed voltage level. This is also indicated by VDRV_READY bit.
STAT 4- PULSE_NUM_FLT	Set if the burst sequence was terminated before completing the pulse number selected. This is also indicated by PULSE_NUM_FLT bit.
STAT 3 - DRV_PULSE_FLT	Set if there is a "stuck" fault detected during pulsing in a burst sequence. This is also indicated by DRV_PULSE_FLT
STAT 2 - EE_CRC_FLT	Set if there is a CRC Error when loading internal EEPROM memory. This is also indicated by EE_CRC_FLT bit.
STAT <1:0> - DEV_STATE	Device State: 00 - LISTEN 01 - BURST 10 - STANDBY 11 - SLEEP

7.6 Register Maps

This section lists the REG_USER registers that are part of the volatile memory that can be configured by the MCU at power up or any time during the operation of the device. For register bits that are marked reserved, their reset value should not be changed.

7.6.1 REG_USER Registers

Table 7-5 lists the REG_USER registers. All register offset addresses not listed in Table 7-5 should be considered as reserved locations and the register contents should not be modified.

Table 7-5. REG_USER Registers

Address	Acronym	Register Name	Section
0x10	BPF_CONFIG_1	Bandpass filter settings	Go
0x11	BPF_CONFIG_2	Bandpass filter settings	Go
0x12	DEV_CTRL_1	Log-amp configuration	Go
0x13	DEV_CTRL_2	Log-amp configuration	Go
0x14	DEV_CTRL_3	Device Configuration	Go
0x16	VDRV_CTRL	VDRV Regulator Control	Go
0x17	ECHO_INT_CONFIG	Echo Interrupt Control	Go
0x18	ZC_CONFIG	Zero Crossing configuration	Go
0x1A	BURST_PULSE	Burst pulse configuration	Go
0x1B	TOF_CONFIG	Time of Flight Config	Go
0x1C	DEV_STAT	Fault status bits	Go
0x1D	DEVICE_ID	Device ID	Go
0x1E	REV_ID	Revision ID	Go

Complex bit access types are encoded to fit into small table cells. Table 7-6 shows the codes that are used for access types in this section.

Table 7-6. REG_USER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

Table 7-6. REG_USER Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

7.6.1.1 BPF_CONFIG_1 Register (Address = 0x10) [reset = 0x0]

BPF_CONFIG_1 is shown in Table 7-7.

Return to the Summary Table.

Table 7-7. BPF_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BPF_FC_TRIM_FRC	R/W	0x0	Override factor settings for Bandpass filter trim and control via BPF_FC_TRIM register. Valid only when BPF_BYPASS = 0 0x0 = Factory trim 0x1 = Override Factory trim
6	BPF_BYPASS	R/W	0x0	Select between Bandpass filter or high pass filter 0x0 = BPF Enabled 0x1 = HPF Enabled (BPF Bypass)
5:0	BPF_HPF_FREQ	R/W	0x0	If BPF_BYPASS = 0: Band pass filter center frequency. See "Bandpass filter center frequency configuration" table If BPF_BYPASS = 1: High pass filter corner frequency 0x00 - 0x0F - 200kHz 0x10 - 0x1F - 400kHz 0x20 - 0x2F - 50kHz 0x30 - 0x3F - 100kHz

7.6.1.2 BPF_CONFIG_2 Register (Address = 0x11) [reset = 0x0]

BPF_CONFIG_2 is shown in Table 7-8.

Return to the Summary Table.

Table 7-8. BPF_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	BPF_Q_SEL	R/W	0x0	Bandpass filter Q factor. Valid only when BPF_BYPASS = 0 0x0 = 4 0x1 = 5 0x2 = 2 0x3 = 3
3:0	BPF_FC_TRIM	R/W	0x0	Offset BPF_HPF_FREQ when BPF_FC_TRIM_FRC = 1: BPF_HPF_FREQ = BPF_HPF_FREQ + BPF_FC_TRIM See "Bandpass filter center frequency range extension" table.

7.6.1.3 DEV_CTRL_1 Register (Address = 0x12) [reset = 0x0]

DEV_CTRL_1 is shown in Table 7-9.

Return to the Summary Table.

Table 7-9. DEV_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_FRC	R/W	0x0	Override for factory settings for LOGAMP_SLOPE_ADJ and LOGAMP_INT_ADJ
6:4	LOGAMP_SLOPE_ADJ	R/W	0x0	Slope or gain adjustment at the final output on VOUT pin. Slope adjustment depends on the setting of VOUT_SCALE_SEL. 0x0 = 3.0× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.56×VOUT_SCALE_SEL V/V 0x1 = 3.1× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.71×VOUT_SCALE_SEL V/V 0x2 = 3.2× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.86×VOUT_SCALE_SEL V/V 0x3 = 3.3× $\overline{\text{VOUT\_SCALE\_SEL}}$+5.01×VOUT_SCALE_SEL V/V 0x4 = 2.6× $\overline{\text{VOUT\_SCALE\_SEL}}$+3.94×VOUT_SCALE_SEL V/V 0x5 = 2.7× $\overline{\text{VOUT\_SCALE\_SEL}}$+ 4.10×VOUT_SCALE_SEL V/V 0x6 = 2.8× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.25×VOUT_SCALE_SEL V/V 0x7 = 2.9× $\overline{\text{VOUT\_SCALE\_SEL}}$+4.4×VOUT_SCALE_SEL V/V
3:0	LOGAMP_INT_ADJ	R/W	0x0	Logamp Intercept adjustment. See "Logamp intercept adjustment" table in specification for values.

7.6.1.4 DEV_CTRL_2 Register (Address = 0x13) [reset = 0x0]

DEV_CTRL_2 is shown in Table 7-10.

Return to the Summary Table.

Table 7-10. DEV_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_DIS_FIRST	R/W	0x0	Disable first logamp stage to reduce quiescent current
6	LOGAMP_DIS_LAST	R/W	0x0	Disable last logamp stage quiescent current
3	RESERVED	R	0x0	Reserved
2	VOUT_SCALE_SEL	R/W	0x0	Select VOUT scaling 0x0 = Select Vout gain to map output to 3.3 V 0x1 = Select Vout gain to map output to 5.0 V
1:0	LNA_GAIN	R/W	0x0	Adjust LNA Gain in V/V 0x0 = 15 V/V 0x1 = 10 V/V 0x2 = 20 V/V 0x3 = 12.5 V/V

7.6.1.5 DEV_CTRL_3 Register (Address = 0x14) [reset = 0x0]

DEV_CTRL_3 is shown in Table 7-11.

Return to the Summary Table.

Table 7-11. DEV_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
4:2	DRV_PLS_FLT_DT	R/W	0x0	Driver Pulse Fault Deglitch Time. In IO_MODE = 0 or IO_MODE = 1, DRV_PULSE_FLT will be set if start of burst is triggered and IO2 pin has not toggled for greater than deglitch Time. In IO_MODE = 2, DRV_PULSE_FLT will be set if start of burst is triggered and if IO1 or IO2 do not toggle a period longer than the deglitch time except when both pins are high. 0x0 = 64 µs 0x1 = 48 µs 0x2 = 32 µs 0x3 = 24 µs 0x4 = 16 µs 0x5 = 8 µs 0x6 = 4 µs 0x7 = Check Disabled
1:0	IO_MODE	R/W	0x0	Configuration for low voltage IO pins. 0x0 = IOMODE 0 0x1 = IOMODE 1 0x2 = IOMODE 2 0x3 = IOMODE 3

7.6.1.6 VDRV_CTRL Register (Address = 0x16) [reset = 0x20]

VDRV_CTRL is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. VDRV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DIS_VDRV_REG_LSTN	R/W	0x0	Automatically disable VDRV charging in listen mode every time after burst mode is exited given VDRV_TRIGGER =0x0. 0x0 = Do not automatically disable VDRV charging 0x1 = Automatically disable VDRV charging
5	VDRV_HI_Z	R/W	0x1	Turn off current source between VPWR and VRDV and disable VDRV regulation. 0x0 = VDRV not Hi-Z 0x1 = VDRV in Hi-Z mode
4	VDRV_CURRENT_LEVEL	R/W	0x0	Pull up current at VDRV pin 0x0 = 10 mA 0x1 = 20 mA
3:0	VDRV_VOLTAGE_LEVEL	R/W	0x0	Regulated Voltage at VDRV pin Value is calculated as : VDRV = VDRV_VOLTAGE_LEVEL + 5 [V]

7.6.1.7 ECHO_INT_CONFIG Register (Address = 0x17) [reset = 0x7]

ECHO_INT_CONFIG is shown in Table 7-13.

Return to the Summary Table.

Table 7-13. ECHO_INT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	ECHO_INT_CMP_EN	R/W	0x0	Enable echo interrupt comparator output

Table 7-13. ECHO_INT_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ECHO_INT_THR_SEL	R/W	0x7	Threshold level to issue interrupt on OUT4 pin. Applied to Low pass filter output. If VOUT_SCALE_SEL=0x0 : Threshold = 0.04 x ECHO_INT_THR_SEL + 0.4 [V] If VOUT_SCALE_SEL=0x1: Threshold = 0.06 x ECHO_INT_THR_SEL + 0.6 [V]

7.6.1.8 ZC_CONFIG Register (Address = 0x18) [reset = 0x14]

ZC_CONFIG is shown in Table 7-14.

Return to the Summary Table.

Table 7-14. ZC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ZC_CMP_EN	R/W	0x0	Enable Zero Cross Comparator for Frequency detection
6	ZC_EN_ECHO_INT	R/W	0x0	When set, provides ZC information only when object is detected
5	ZC_CMP_IN_SEL	R/W	0x0	Zero Comparator Input Select 0x0 = INP - VCM 0x1 = INP - INN
4:3	ZC_CMP_STG_SEL	R/W	0x2	Zero Cross Comparator Stage Select
2:0	ZC_CMP_HYST	R/W	0x4	Zero Cross Comparator Hysteresis Selection 0x0 = 30 mV 0x1 = 80 mV 0x2 = 130 mV 0x3 = 180 mV 0x4 = 230 mV 0x5 = 280 mV 0x6 = 330 mV 0x7 = 380 mV

7.6.1.9 BURST_PULSE Register (Address = 0x1A) [reset = 0x0]

BURST_PULSE is shown in Table 7-15.

Return to the Summary Table.

Table 7-15. BURST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALF_BRG_MODE	R/W	0x0	Use output driver in half-bridge mode. When enabled, drive both high-side FET together and low-side FETs together. 0x0 = Disable half-bridge mode 0x1 = Enable half bridge mode
6	PRE_DRIVER_MODE	R/W	0x0	Pre-driver mode to drive external FETs 0x0 = Disable pre-driver mode 0x1 = Enable pre-driver mode
5:0	BURST_PULSE	R/W	0x0	Number of burst pulses. REG_VALUE=0x00 enables continuous burst mode

7.6.1.10 TOF_CONFIG Register (Address = 0x1B) [reset = 0x0]

TOF_CONFIG is shown in Table 7-16.

Return to the Summary Table.

Table 7-16. TOF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_MODE_EN	R/W	0x0	For entering or exiting sleep mode 0x0 = Wake up or exit Sleep Mode 0x1 = Enter sleep mode
6	STDBY_MODE_EN	R/W	0x0	For entering or exiting standby mode 0x0 = Exit Standby Mode 0x1 = Enter Standby mode
5:2	RESERVED	R	0x0	Reserved
1	VDRV_TRIGGER	R/W	0x0	Control charging of VDRV pin when DIS_VDRV_REG_LSTN = 1. This has no effect when VDRV_HI_Z=0x1. 0x0 = Disable I_{VDRV} 0x1 = Enable I_{VDRV}
0	CMD_TRIGGER	R/W	0x0	For IO_MODE=0x0, control enabling of burst mode. Ignored for other IO_MODE values. 0x0 = Disable burst mode 0x1 = Enable burst mode

7.6.1.11 DEV_STAT Register (Address = 0x1C) [reset = 0x0]

DEV_STAT is shown in Table 7-17.

Return to the Summary Table.

Table 7-17. DEV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	VDRV_READY	R	0x0	VDRV pin voltage status 0x0 = VDRV is below configured voltage 0x1 = VDRV is equal or above configured voltage
2	PULSE_NUM_FLT	R	0x0	The Driver has not received the number of pulses defined by BURST_PULSE
1	DRV_PULSE_FLT	R	0x0	The Driver has been stuck in a single state in burst mode for a period longer than delgitch time set by DRV_PLS_FLT_DT
0	EE_CRC_FLT	R	0x0	CRC error for internal memory

7.6.1.12 DEVICE_ID Register (Address = 0x1D) [reset = X]

DEVICE_ID is shown in Table 7-18.

Return to the Summary Table.

Table 7-18. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	X	Device ID: 0xB9

7.6.1.13 REV_ID Register (Address = 0x1E) [reset = 0x2]

REV_ID is shown in Table 7-19.

Return to the Summary Table.

Table 7-19. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	0x2	Revision ID

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TUSS4470 device must be paired with an external ultrasonic transducer. The TUSS4470 device drives the transducer to generate an ultrasonic echo and applies logarithmic gain scaling to the received echo signal in the analog front end. The transducer should be chosen based on the resonant frequency, input voltage requirements, sensitivity, beam pattern, and decay time. The TUSS4470 device is flexible enough to meet most transducer requirements by adjusting the driving frequency, driving current limit, and center frequency of the band-pass filter. The only available interface to configure the device registers is SPI. During the burst-and-listen cycles, an external ADC or analog receiver should be used to capture the echo envelope from the VOUT pin to compute time of flight (ToF), distance, amplitude, and/or width of the return echo.

8.2 Typical Application

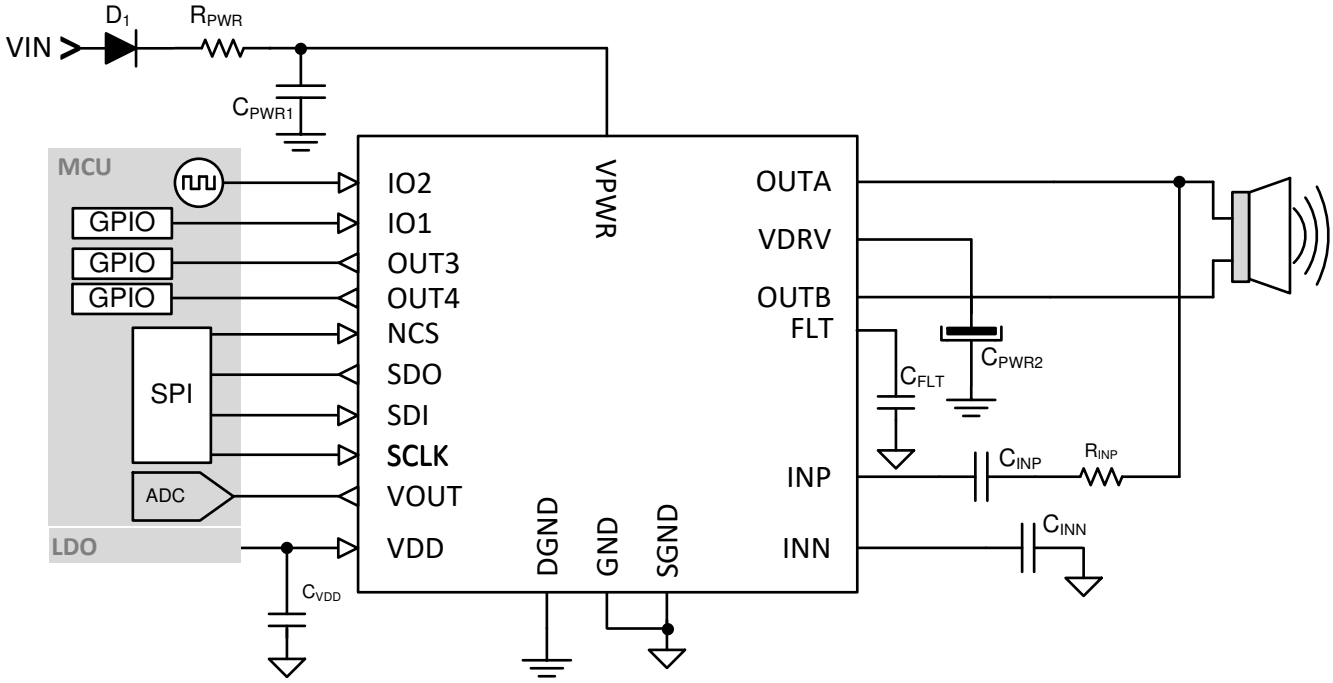


Figure 8-1. TUSS4470 Application Diagram

Table 8-1. Recommended Component Values for Typical Applications

DESIGNATOR	VALUE	COMMENT
R_{PWR}	10 Ω	Optional (to limit fast voltage transient on VPWR pin during power up)
$R_{(INP)}$	200Ω (1/4 Watt)	Optional higher value for EMI/ESD robustness
C_{PWR1}	50V, 100nF	
C_{PWR2}	40V, 2µF	
C_{VDD}	>5V, 10nF	
C_{INP}	40V, 330pF	
C_{INN}	>5V, C_{INN}	Use equation below to estimate value of C_{INN} depending on the burst frequency $$C_{INN} = \frac{1}{2 \times \pi \times 150\,\Omega \times \frac{f_{DRV}}{4}} \quad (2)$$
C_{FLT}	5V, C_{FLT}	Use equation below to estimate value of C_{FLT} depending on the burst frequency . Value has to be optimized for application depending on noise and response time requirements. $$C_{FLT} = \frac{25}{2 \times \pi \times 6250\,\Omega \times f_{DRV}} \quad (3)$$
D1	1N4001 or equivalent	Optional for reverse supply and reverse current protection.
XDCR (transducer)		Example devices for low-frequency range: Closed top: 40 kHz: PUI Audio UTR-1440K-TT-R Open top: muRata MA40H1S-R, SensComp 40LPT16, Kobitone 255-400PT160-ROX Example devices for high-frequency range: Closed top: 300 kHz: Murata MA300D1-1

8.2.1 Transducer Drive Configuration Options

For different transducer drive configurations, the TUSS4470 supports multiple configurations to accommodate specific system needs as shown in Figure 8-2. The typical application diagram in Figure 8-1 is considered as "Case 1".

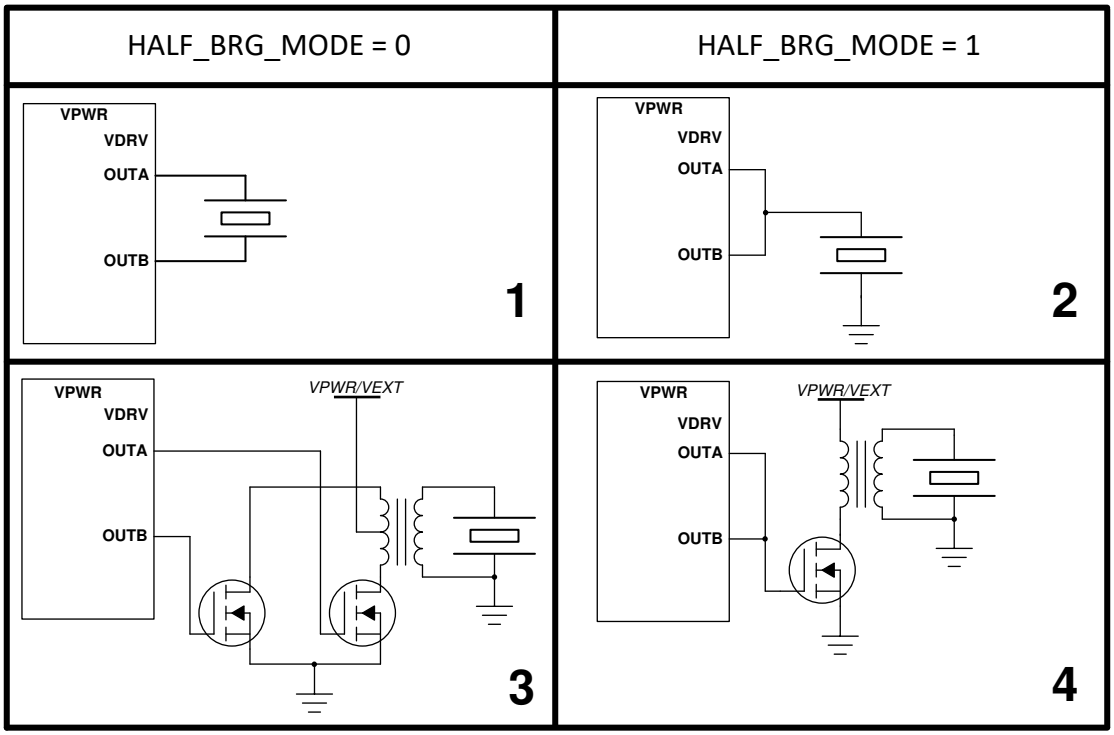


Figure 8-2. TUSS4470 Transducer Drive Options

The behavior of the internal FETs in the TUSS4470 device is different for each configuration in Figure 8-2. Table 8-2 and Table 8-3 shows the relationship between the IOx pins and the state of the OUTA and OUTB pins for different register settings.

Table 8-2. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 2

IO MODE 2							
START OF BURST	PRE_DRIVER_MODE	HALF_BRG_MODE	IO1	IO2	OUTA	OUTB	APPLICATION CASE
YES	0	0	0	0	GND	GND	CASE 1
	0	0	0	1	GND	V_{VDRV}	
	0	0	1	0	V_{VDRV}	GND	
NO	0	0	1	1	Hi-Z	GND	
YES	0	1	0	0	Hi-Z	Hi-Z	CASE 2
	0	1	0	1	V_{VDRV}	V_{VDRV}	
	0	1	1	0	GND	GND	
NO	0	1	1	1	Hi-Z	Hi-Z	
YES	1	0	0	0	GND	GND	CASE 3
	1	0	0	1	GND	V_{VDRV}	
	1	0	1	0	V_{VDRV}	GND	
NO	1	0	1	1	GND	GND	
YES	1	1	0	0	GND	GND	CASE 4
	1	1	0	1	V_{VDRV}	V_{VDRV}	
	1	1	1	0	GND	GND	
NO	1	1	1	1	GND	GND	

Table 8-3. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3

IO MODE 0, IO MODE 1, IO MODE 3								
START OF BURST	PRE_DRIVER_MODE	HALF_BRG_MODE	CMD_TRIGGER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	0	0	0	1	0	Hi-Z	GND	CASE 1
	0	0	0	1	1			
YES	0	0	1	0	0	GND	V_{VDRV}	
	0	0	1	0	1	V_{VDRV}	GND	
NO	0	1	0	1	0	Hi-Z	Hi-Z	CASE 2
	0	1	0	1	1			
YES	0	1	1	0	0	GND	GND	
	0	1	1	0	1	V_{VDRV}	V_{VDRV}	
NO	1	0	0	1	0	GND	GND	CASE 3
	1	0	0	1	1			
YES	1	0	1	0	0	GND	V_{VDRV}	
	1	0	1	0	1	V_{VDRV}	GND	
NO	1	1	0	1	0	GND	GND	CASE 4
	1	1	0	1	1			
YES	1	1	1	0	0	GND	GND	
	1	1	1	0	1	V_{VDRV}	V_{VDRV}	

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-4 as the input and operating parameters. All other device settings can be assumed to be factory default.

Table 8-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 to 36 V
Input voltage recommended	5 V or 20 V
Transducer driving voltage	5 V_{AC} or 20 V_{AC}
Transducer frequency	40 kHz or 400 kHz
Transducer pulse count	16

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Transducer
  - Transducer driving voltage
  - Transducer resonant frequency
  - Transducer pulse count maximum

8.2.1.2.1 Transducer Driving Voltage

When a voltage is applied to piezoelectric ceramics, mechanical distortion is generated according to the voltage and frequency. The mechanical distortion is measured in units of sound pressure level (SPL) to indicate the volume of sound, and can be derived from a free-field microphone voltage measurement using Equation 4.

$$\text{SPL (db)} = 20 \times \log \frac{\left(\frac{V_{(MIC)}}{3.4\ mV} \right)}{P_O} \tag{4}$$

where

- $V_{(MIC)}$ is the measured sensor sound pressure (mV_{RMS}).
- P_O is a referenced sound pressure of 20 µPa.

The SPL does not increase indefinitely with the driving voltage. After a particular driving voltage, the amount of SPL that a transducer can generate becomes saturated. A transducer is given a maximum driving voltage specification to indicate when the maximum SPL is generated. Driving the transducer beyond the maximum driving voltage makes the ultrasonic module less power-efficient and can damage or decrease the life expectancy of the transducer.

8.2.1.2.2 Transducer Driving Frequency

The strength of ultrasonic waves propagated into the air attenuate proportionally with distance. This attenuation is caused by diffusion, diffraction, and absorption loss as the ultrasonic energy transmits through the medium of air. As shown in Figure 8-3, the higher the frequency of the ultrasonic wave, the larger the attenuation rate and the shorter the distance the wave reaches.

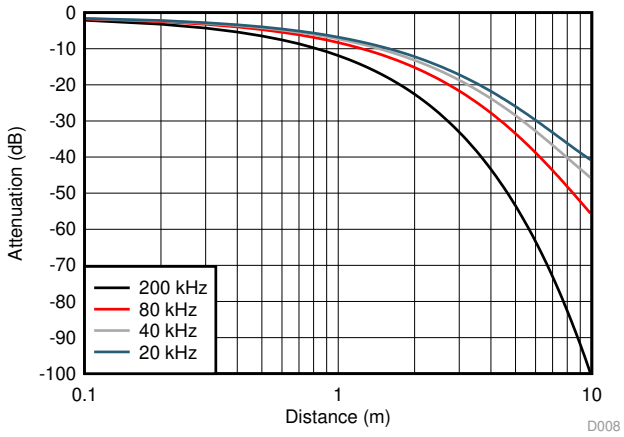


Figure 8-3. Attenuation Characteristics of Sound Pressure by Distance

An ultrasonic transducer has a fixed resonant center frequency with a typical tolerance of ±2%. The lower frequency range of 30 kHz to 100 kHz is the default operating range for common long range applications for a step resolution of 1 cm and typical range of 30 cm to 5 m. The upper frequency range of 100 kHz to 1000 kHz is reserved for high-precision applications with a step resolution of 1 mm and a typical range of 5 cm to 1 m.

8.2.1.2.3 Transducer Pulse Count

The pulse count determines how many alternating periods are applied to the transducer by the complementary low-side drivers and determines the total width of the ultrasonic ping that was transmitted. The larger the width of the transmitted ping, the larger the width of the returned echo signature of the reflected surface and the more resolution available to set a stable threshold. A disadvantage of a large pulse count is a large ringing-decay period, which limits how detectable objects are at short distances.

Select a pulse count based on the minimum object distance requirement. If short-distance object detection is not a priority, a high pulse count is not a concern. Certain transducers can be driven continuously while others have a limit to the maximum driving-pulse count. Refer to the specification for the selected transducer to determine if the pulse count must be limited.

8.2.1.3 Application Curves

Figure 8-4 and Figure 8-5 show the typical ranging performance of a 40-kHz, closed-top transducer under nominal operating conditions as indicated in Table 8-4. The targeted object is a PVC pole measuring 1000 mm in height and 75 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1.

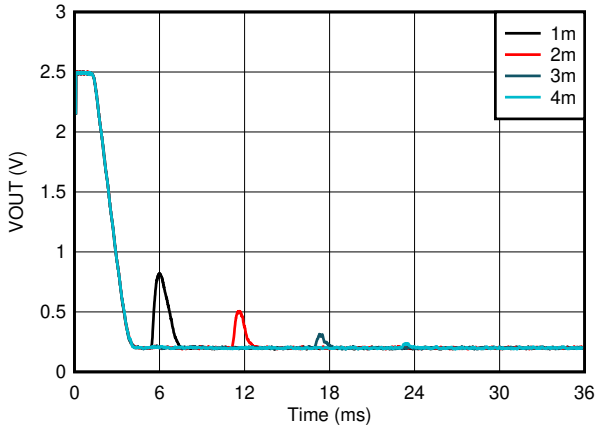


Figure 8-4. TUSS4470 40 kHz Ranging at 5-V Driver With Last Log-Amp Stage Disabled

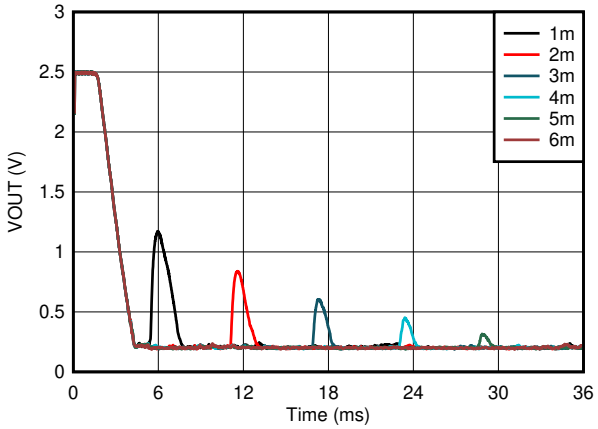


Figure 8-5. TUSS4470 40 kHz Ranging at 20-V Driver With Last Log-Amp Stage Disabled

Figure 8-6 and Figure 8-7 show the typical ranging performance of a 400-kHz, closed-top transducer under nominal operating conditions as indicated in Table 8-4. The targeted object is an aluminum pole measuring 100 mm in height and 10 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0.

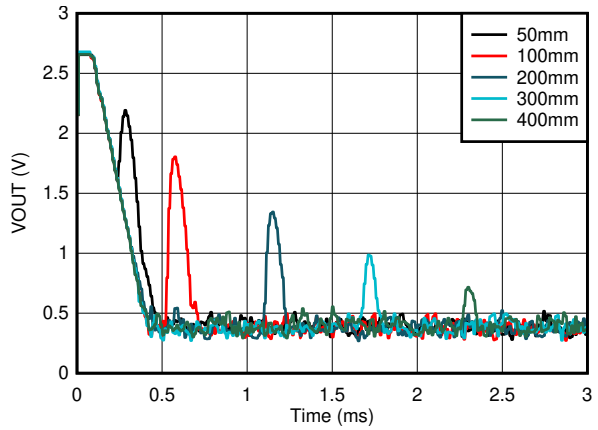


Figure 8-6. TUSS4470 400 kHz Ranging at 5-V Drive

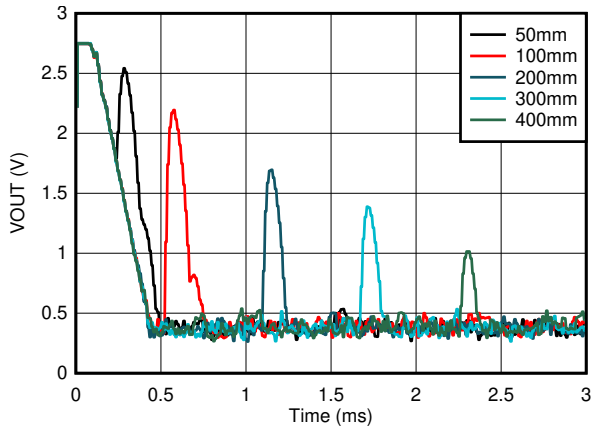


Figure 8-7. TUSS4470 400 kHz Ranging at 20-V Driver

9 Power Supply Recommendations

The TUSS4470 device is designed to operate from two independent supplies, a driver supply and a regulated supply.

The driver input voltage supply (VPWR) range can operate from 5 V to 36 V. In applications where the TUSS4470 device may be exposed to battery transients and reverse battery currents, use external component-safeguards, such as component D1 or parallel TVS diodes, to help protect the device. If the input supply is placed more than a few inches from the TUSS4470 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors near the VPWR pin. In the event both the VDRV and pre-driver modes is enabled, limit the VPWR voltage to the maximum rated voltage of the externally driven transistor's gate-source or base-emitter rating. The electrolytic capacitor at the VDRV pin is intended to act as a fast discharge capacitor during the bursting stage of the TUSS4470 device. The H-bridge high-side voltage can be supplied with an independent voltage at the VDRV pin to isolate the driver from VPWR, but must remain within the specified maximum voltage rating of the VDRV, OUTA, and OUTB outputs. If the H-bridge high-side voltage is to be supplied by an independent source, VDRV should be disabled.

The regulated supply (VDD) is used as the supply reference for the analog front end, filtering, and analog output blocks, so this supply should be stable for maximum performance. TI recommends using an LDO or other regulated external power source with bypass capacitor placed closely to the VDD pin. As VDD becomes less stable, the noise floor of the VOUT signal will increase, and result in a loss of long range object detection as a consequence.

To prevent damage to the device, always avoid hot-plugging or providing instantaneous power at the VPWR and VDRV pins at start-up, unless these pins are properly protected with an RC filter or TVS diode to minimize transient effects. VPWR must always be equal to or greater than the value present at VDRV.

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to accomplish a small-form factor ultrasonic module design. The layers should be separated by analog and digital signals. The pin map of the device is routed such that the power and digital signals are on the opposing side of the analog driver and receiver pins. Consider the following best practices for TUSS4470 device layout in order of descending priority:

- Separating the grounding types is important to reduce noise at the AFE input of the TUSS4470. In particular, the transducer sensor ground, supporting driver, and return-path circuitry should have a separate ground before being connected to the main ground. Separating the sensor and main grounds through a ferrite bead is best practice, but not require. A copper-trace or 0-Ω short is also acceptable when bridging grounds.
- The analog return path pins, INP and INN, are most susceptible to noise and therefore should be routed as short and directly to the transducer as possible. Ensure the INN capacitor is close to the pin to reduce the length of the ground wire.
- The analog output pin trace should be routed as short and directly to an external ADC or microcontroller input to avoid signal-to-noise losses due to parasitic-effects or noise coupling onto the trace from external radiating aggressors.
- In applications where protection from an ESD strike on the case of the transducer is important, ground routing of the capacitor on the INN pin should be separate from the device ground and connected directly with the shortest possible trace to the connector ground.
- The analog drive pins can be high-current, high-voltage, or both and therefore the design limitation of the OUTA and OUTB pins is based on the copper trace profile. The driver pins are recommended to be as short and direct as possible when driving a transducer with a high-voltage.
- The decoupling capacitors for the VDD and VPWR pins should be placed as close to the pins as possible.
- Any digital communication should be routed away from the analog receiver pins. TXD, RXD, SCLK, NCS, IO1, IO2, OUT3, and OUT4 pins should be routed on the opposite side of the PCB, away from of the analog signals.

10.2 Layout Example

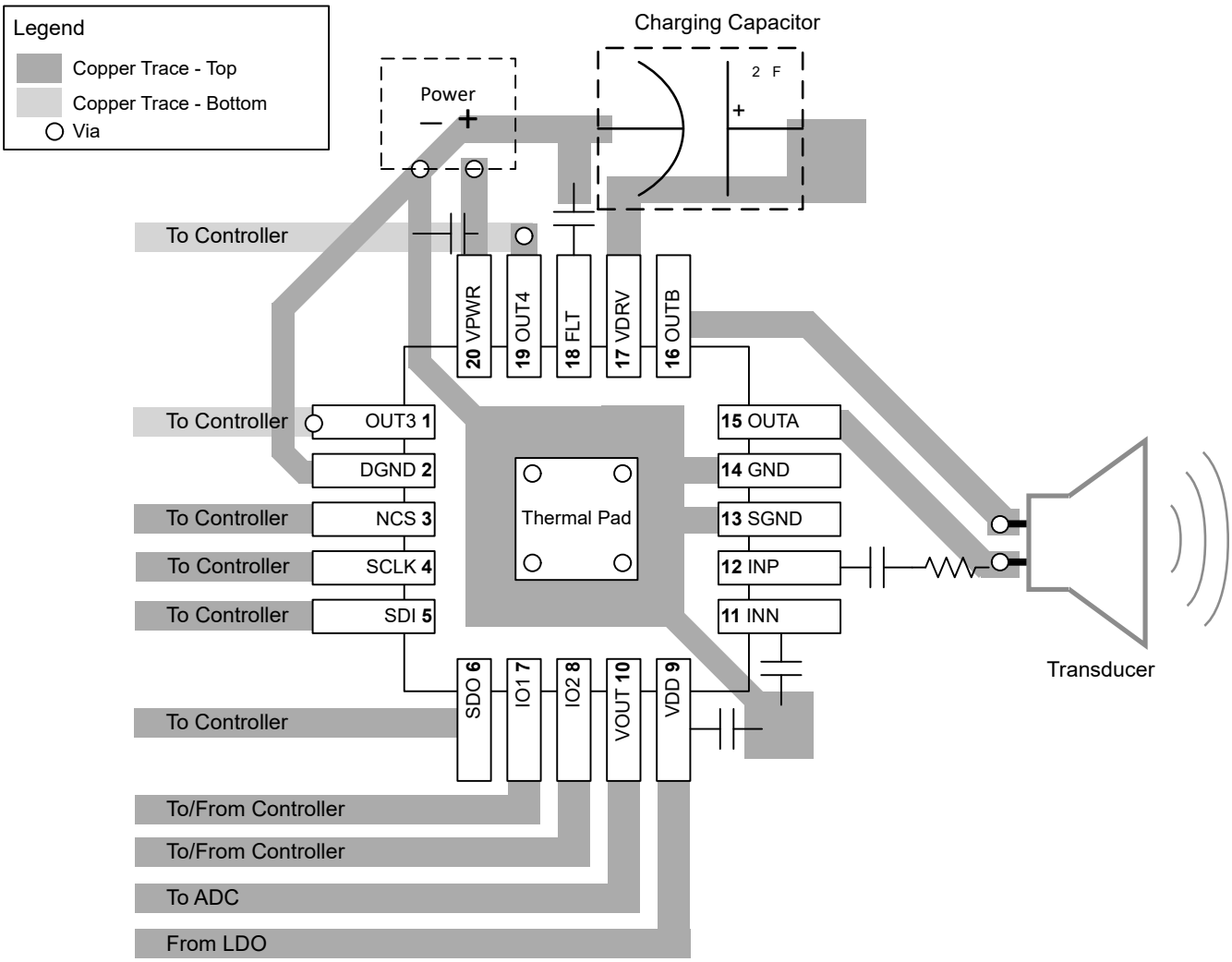


Figure 10-1. TUSS4470 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSS4470TRTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4470	Samples
TUSS4470TRTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 105	USS4470	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

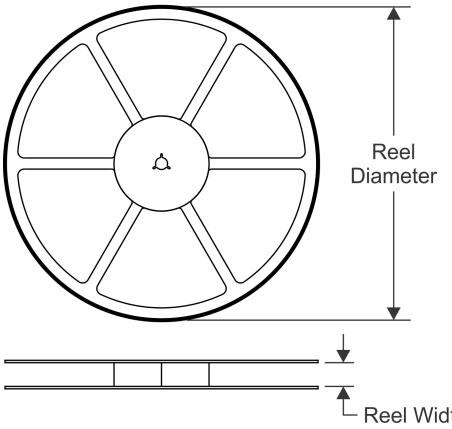
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

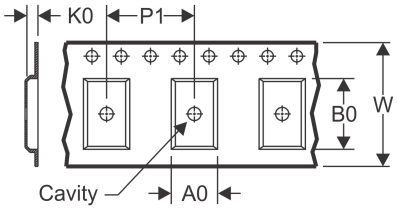
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

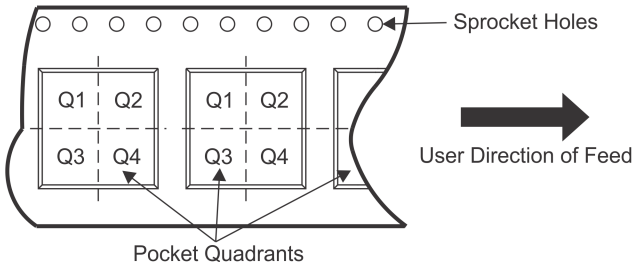


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

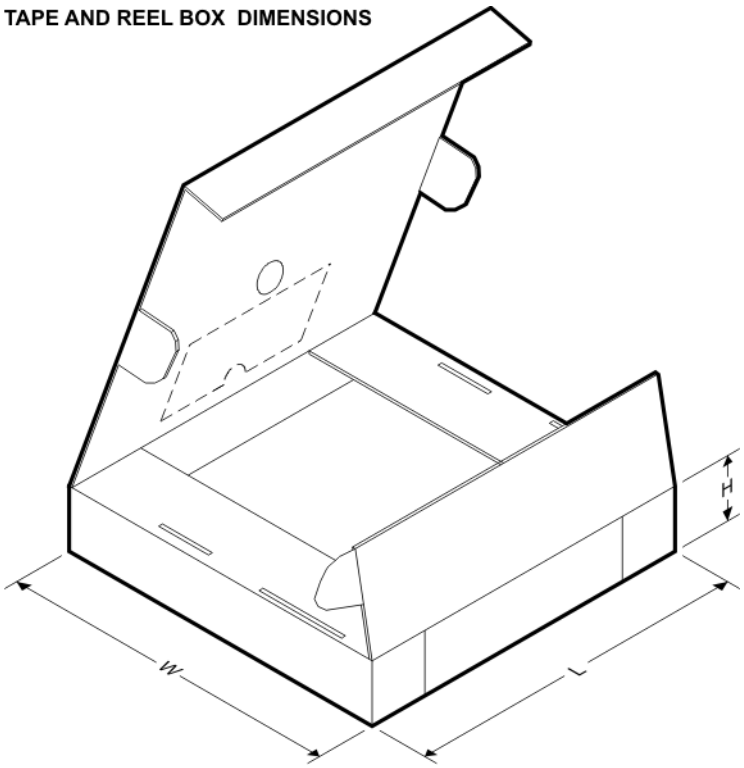
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSS4470TRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSS4470TRTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSS4470TRTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TUSS4470TRTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

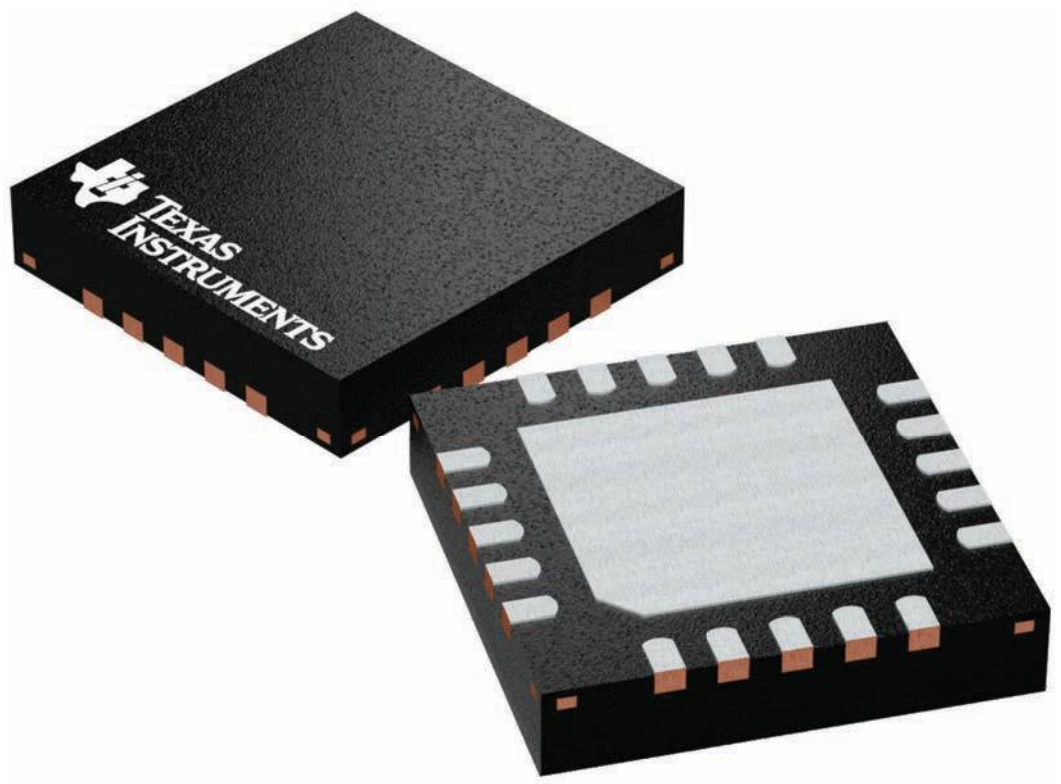
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
ENGINEER: T. TANG	DATE: 09/12/2016		
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016		

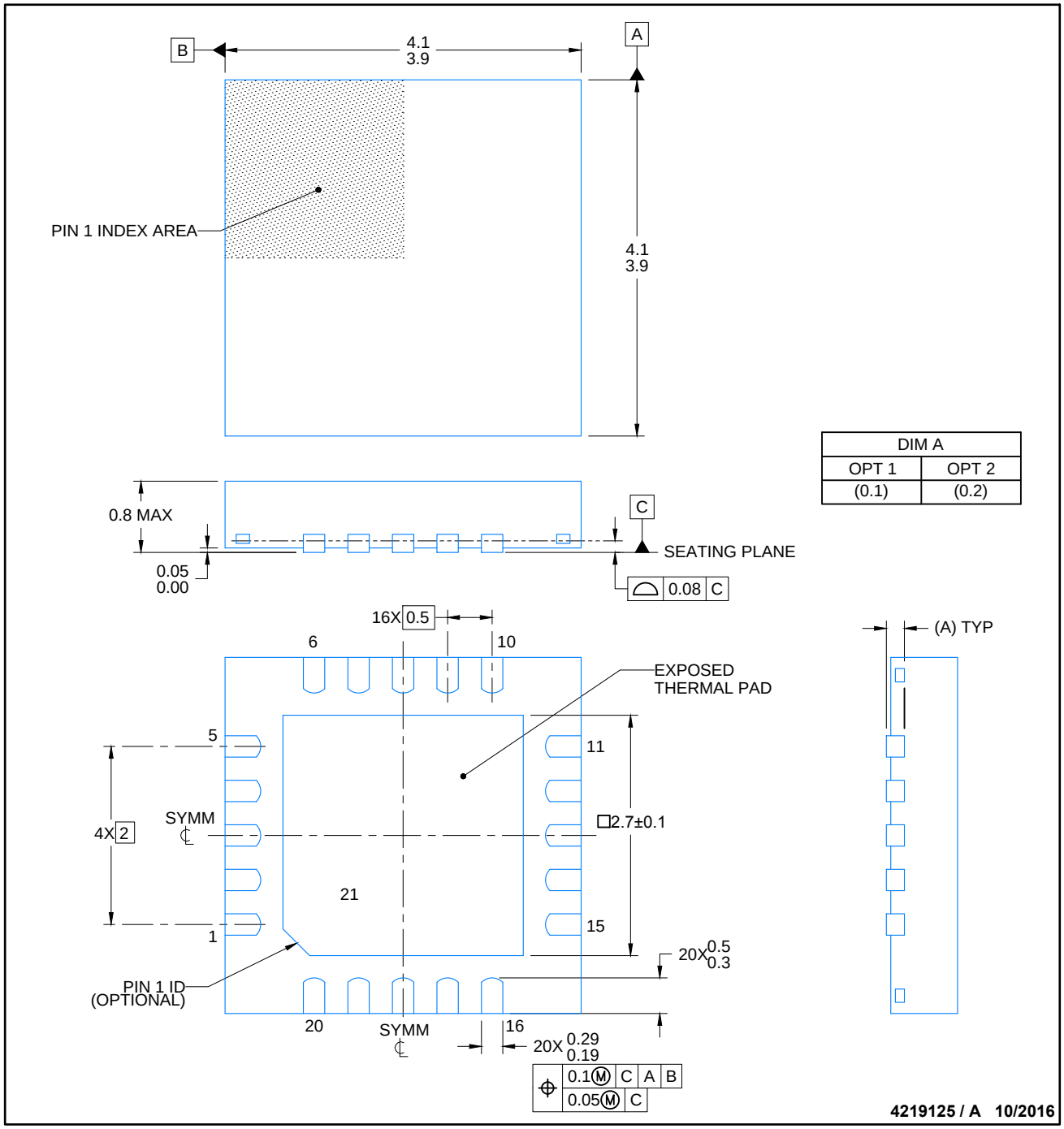
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5

PACKAGE OUTLINE

RTJ0020D

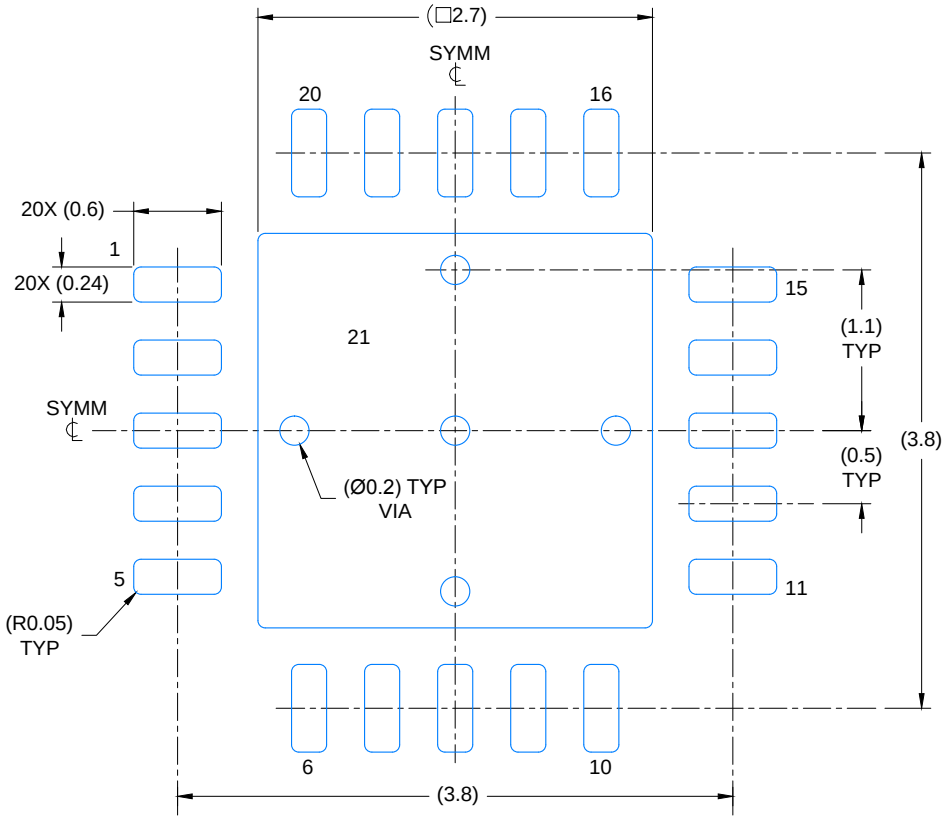
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



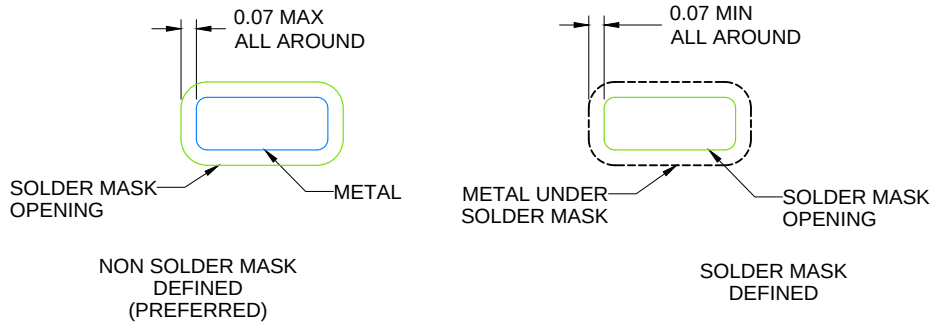
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

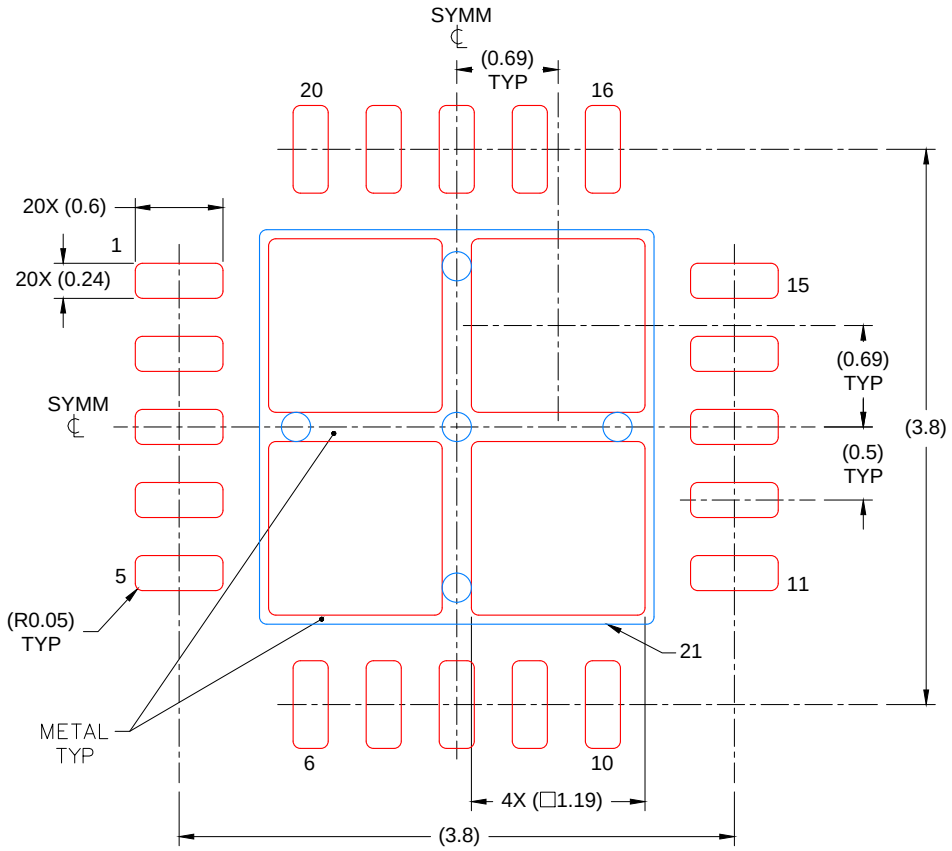
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
UCC27624-Q1
SLUSES4A – MARCH 2022 – REVISED MAY 2022

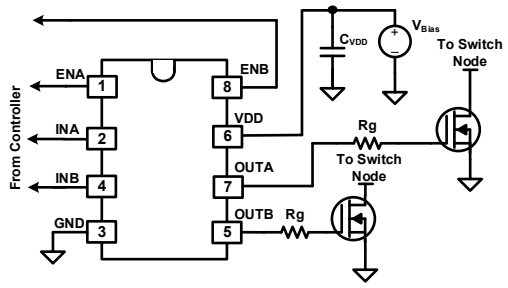
UCC27624-Q1 30-V, 5-A Dual-Channel Low-Side Gate Driver with –10-V Input Capability

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified
  - Device Temperature Grade 1
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C6
- Typical 5-A peak source and sink drive current for each channel
- Input and enable pins capable of handling –10 V
- Output capable of handling –2-V transients
- Absolute maximum VDD voltage: 30 V
- Wide VDD operating range from 4.5 V to 26 V with UVLO
- Hysteretic-logic thresholds for high noise immunity
- VDD independent input thresholds (TTL compatible)
- Fast propagation delays (17-ns typical)
- Fast rise and fall times (6-ns and 10-ns typical)
- 1-ns typical delay matching between the two channels
- Two channels can be paralleled for higher drive current
- SOIC8 and VSSOP8 PowerPAD™ package options
- Operating junction temperature range of –40°C to 150°C

2 Applications

- Automotive DC/DC Converters
- Switched-mode power supplies (SMPS)
- Power factor correction (PFC) circuits
- DC/DC converter
- Motor drives
- Solar power supplies
- Pulse transformer driver



Simplified Application Diagram

3 Description

The UCC27624-Q1 is a dual-channel, high-speed, low-side gate driver that effectively drives MOSFET, IGBT, SiC, and GaN power switches. UCC27624-Q1 has a typical peak drive strength of 5 A, which reduces rise and fall times of the power switches, lowers switching losses, and increases efficiency. The device's fast propagation delay (17-ns typical) yields better power stage efficiency by improving the deadtime optimization, pulse width utilization, control loop response, and transient performance of the system.

UCC27624-Q1 can handle –10 V at its inputs, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs for maximum control flexibility. An independent enable signal allows the power stage to be controlled independently of main control logic. In the event of a system fault, the gate driver can quickly shut-off by pulling enable low. Many high-frequency switching power supplies exhibit noise at the gate of the power device, which can get injected into the output pin on the gate driver and can cause the driver to malfunction. The device's transient reverse current and reverse voltage capability allow it to tolerate noise on the gate of the power device or pulse-transformer and avoid driver malfunction.

The UCC27624-Q1 also features undervoltage lockout (UVLO) for improved system robustness. When there is not enough bias voltage to fully enhance the power device, the gate driver output is held low by the strong internal pull down MOSFET.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
UCC27624-Q1	SOIC (8)	4.90 mm × 3.91 mm
UCC27624-Q1	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2022) to Revision A (May 2022)	Page
• Added automotive certifications	1
• Updated ESD ratings	4

5 Pin Configuration and Functions

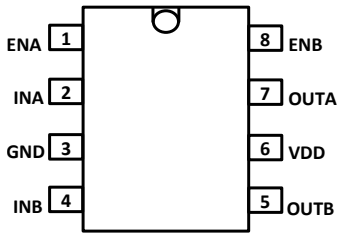


Figure 5-1. D Package 8-Pin SOIC Top View

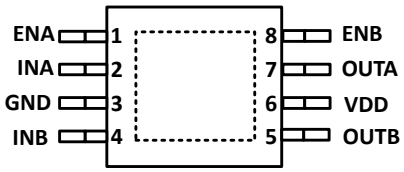


Figure 5-2. DGN Package 8-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DGN	D		
ENA	1	1	I	Enable input for Channel A. Biasing ENA, LOW will disable Channel A output regardless of the state of INA. Pulling ENA, HIGH enables the Channel A output. If ENA is left floating, Channel A is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
ENB	8	8	I	Enable input for Channel B. Biasing ENB, LOW disables Channel B output regardless of the state of INB. Pulling ENB, HIGH enables the Channel B output. If ENB is left floating, Channel B is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
GND	3	3	—	Ground: All signals are referenced to this pin.
INA	2	2	I	Input to Channel A. INA is the non-inverting input of the UCC27624-Q1 device. OUTA is held LOW if INA is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.
INB	4	4	I	Input to Channel B. INB is the non-inverting input of the UCC27624-Q1 device. OUTB is held LOW if INB is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.
OUTA	7	7	O	Channel A Output
OUTB	5	5	O	Channel B Output
VDD	6	6	I	Bias supply input. Bypass this pin with two ceramic capacitors, generally ≥ 1 µF and 0.1 µF, which are referenced to GND pin of this device.
	Thermal Pad	—	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I = Input; O = Output

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage, VDD		–0.3	30	V
Output Voltage, OUTA, OUTB	DC	–0.3	VDD +0.3	V
	200ns Pulse	–2	VDD +3	V
Input Voltage INA, INB, ENA, ENB		–10	30	V
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *Section 6.4* of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	26	V
Input voltage, INA, INB, ENA, ENB	–10		26	V
Output Voltage, OUTA, OUTB	0		VDD	V
Operating junction temperature, T_J	–40		150	°C

6.4 Thermal Information

THERMAL METRIC		UCC27624-Q1		UNIT
		DGN	D	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	126.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.8	67.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	69.9	
ψ_{JT}	Junction-to-top characterization parameter	2.6	19.2	
ψ_{JB}	Junction-to-board characterization parameter	22.3	69.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	n/a	

6.5 Electrical Characteristics

Unless otherwise noted, VDD = 12 V, $T_A = T_J$ = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDDq}	VDD quiescent supply current	V_{INx} = 3.3 V, VDD = 3.4 V, ENx = VDD		300	450	µA
I_{VDD}	VDD static supply current	V_{INx} = 3.3 V, ENx = VDD		0.6	1.0	mA
I_{VDD}	VDD static supply current	V_{INx} = 0 V, ENx = VDD		0.7	1.0	mA
I_{VDDO}	VDD operating current	f_{SW} = 1000 kHz, ENx = VDD, V_{INx} = 0 V – 3.3 V PWM		3.2	3.8	mA
I_{DIS}	VDD disable current	V_{INx} = 3.3 V, ENx = 0 V		0.8	1.1	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{VDD_ON}	VDD UVLO rising threshold		3.8	4.1	4.4	V
V_{VDD_OFF}	VDD UVLO falling threshold		3.5	3.8	4.1	V
V_{VDD_HYS}	VDD UVLO hysteresis			0.3		V
INPUT (INA, INB)						
V_{INx_H}	Input signal high threshold	Output High, ENx = HIGH	1.8	2	2.3	V
V_{INx_L}	Input signal low threshold	Output Low, ENx = HIGH	0.8	1	1.2	V
V_{INx_HYS}	Input signal hysteresis			1		V
R_{INx}	INx pin pulldown resistor	INx = 3.3 V		120		kΩ
ENABLE (ENA, ENB)						
V_{ENx_H}	Enable signal high threshold	Output High, INx = HIGH	1.8	2	2.3	V
V_{ENx_L}	Enable signal low threshold	Output Low, INx = HIGH	0.8	1	1.2	V
V_{ENx_HYS}	Enable signal hysteresis			1		V
R_{ENx}	EN pin pullup resistance	ENx = 0 V		200		kΩ
OUTPUTS (OUTA, OUTB)						
I_{SRC} (1)	Peak output source current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
I_{SNK} (1)	Peak output sink current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–5		A
R_{OH} (2)	Pullup resistance	I_{OUT} = –50 mA See Section 7.3.4.		5	8.5	Ω
R_{OL}	Pulldown resistance	I_{OUT} = 50 mA		0.6	1.1	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

ADVANCE INFORMATION

6.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 12 V, T_A = T_J = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Rx}	Rise time	C_{LOAD} = 1.8 nF, 20% to 80%, Vin = 0 V – 3.3 V		6	10	ns
t_{Fx}	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, Vin = 0 V – 3.3 V		10	14	ns
t_{D1x}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D2x}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D3x}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D4x}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_M	Delay matching between two channels	C_{LOAD} = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, INA = INB, $\lvert t_{RA} - t_{RB} \rvert$, $\lvert t_{FA} - t_{FB} \rvert$		1	2	ns
t_{PWmin}	Minimum input pulse width	C_L = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, Vo > 1.5 V		10	15	ns

(1) Switching parameters are not tested in production.

ADVANCE INFORMATION

6.7 Timing Diagrams

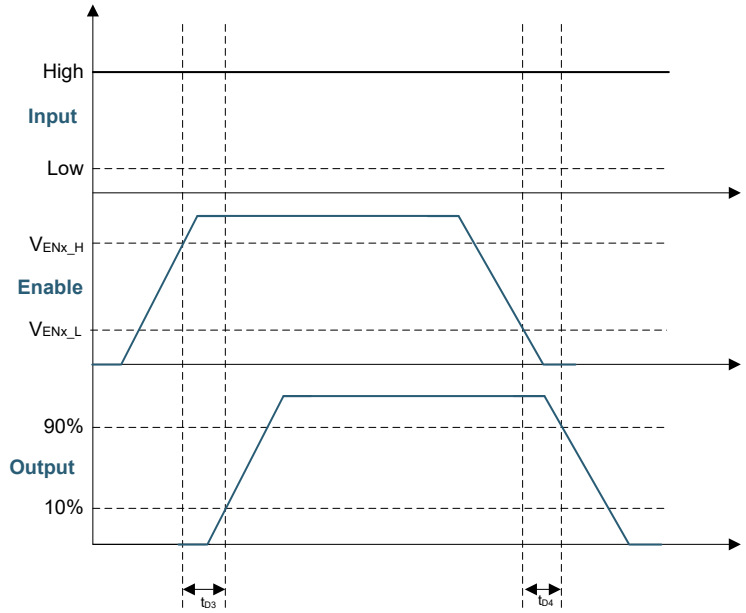


Figure 6-1. Enable Function

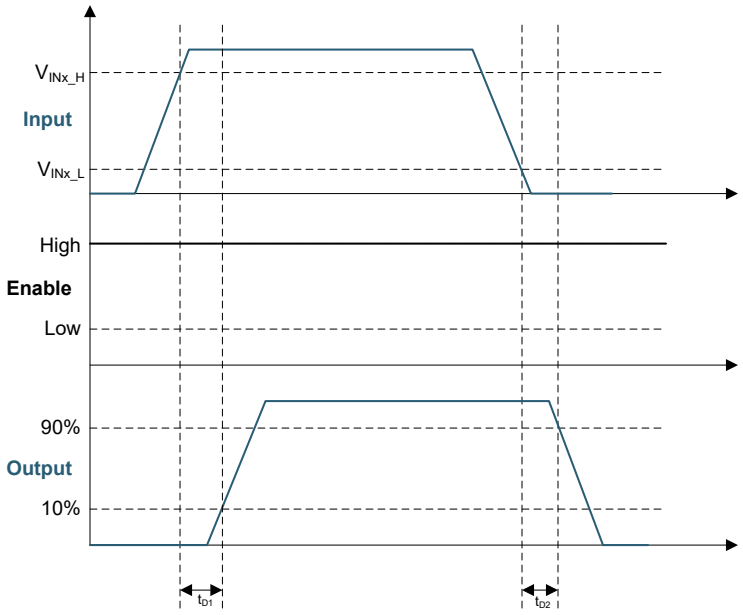


Figure 6-2. Input-Output Operation

ADVANCE INFORMATION

ADVANCE INFORMATION

6.8 Typical Characteristics

Unless otherwise specified, VDD=12 V, INx = 3.3 V, ENx = 3.3 V, T_J = 25°C, no load

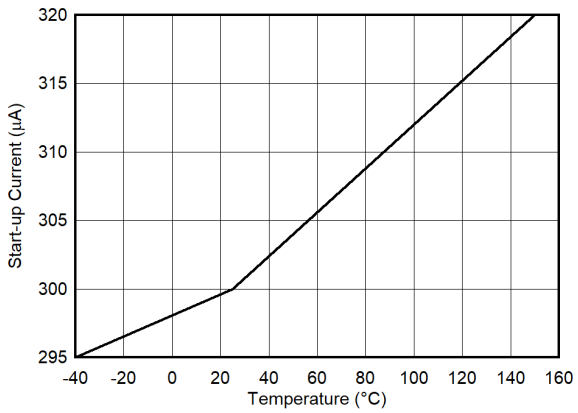


Figure 6-3. Start-Up and Quiescent Current

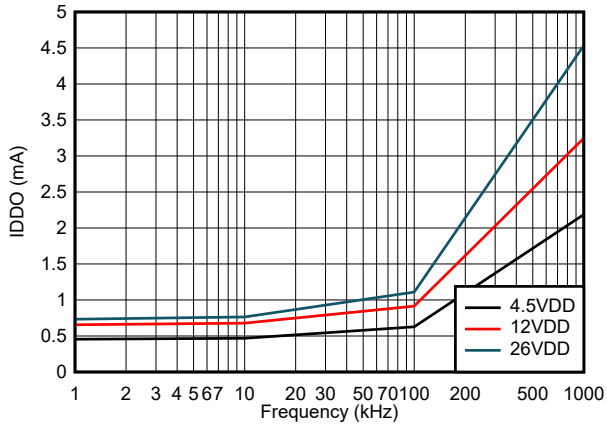


Figure 6-4. Operating Supply Current (Both Outputs Switching)

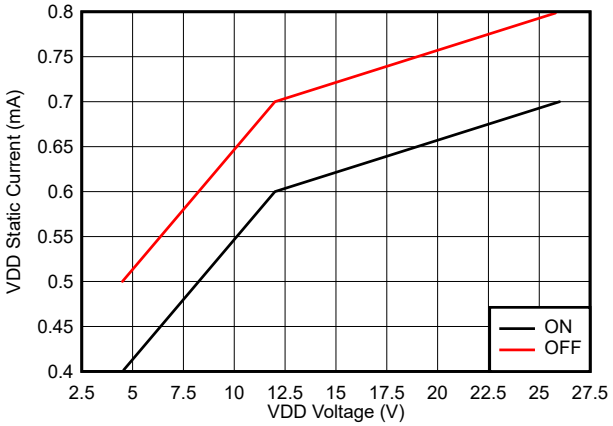


Figure 6-5. Static Supply Current (Outputs in DC On or Off Condition)

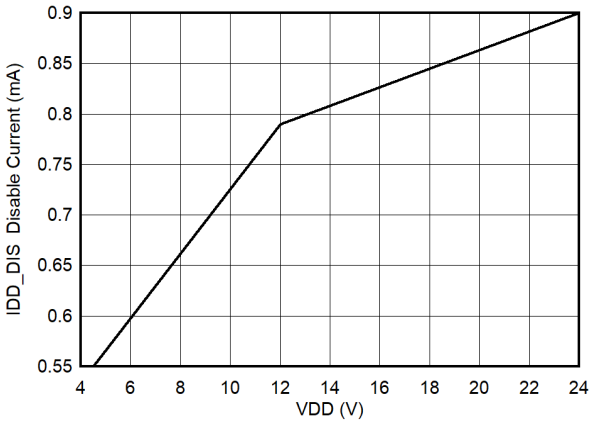


Figure 6-6. Disable Current (EN = 0 V)

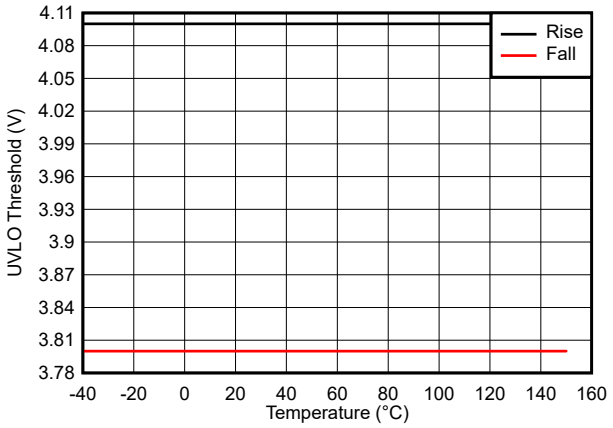


Figure 6-7. VDD UVLO Threshold

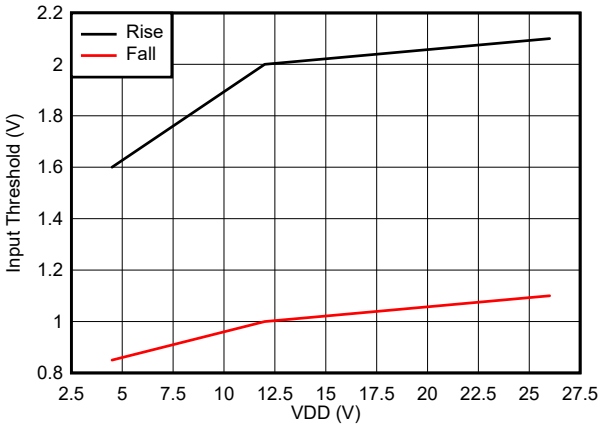


Figure 6-8. Input Thresholds

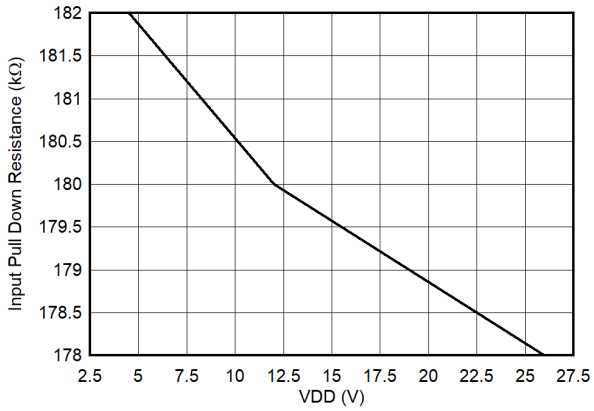


Figure 6-9. Input Pulldown Resistance

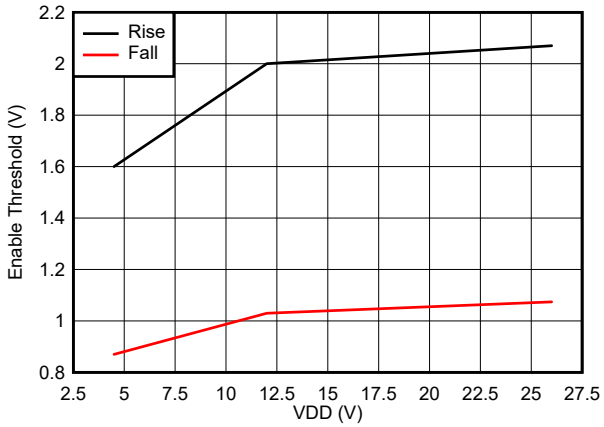


Figure 6-10. Enable Threshold

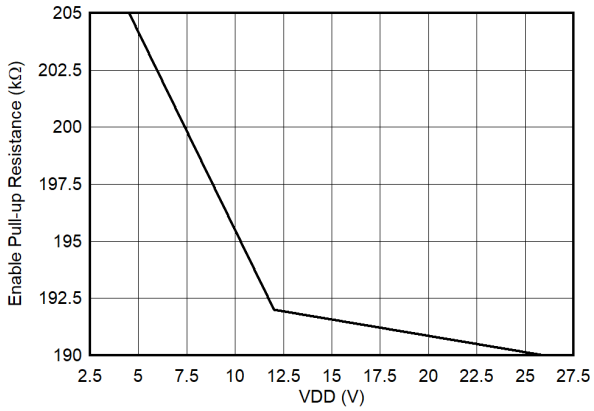


Figure 6-11. Enable Pullup Resistance

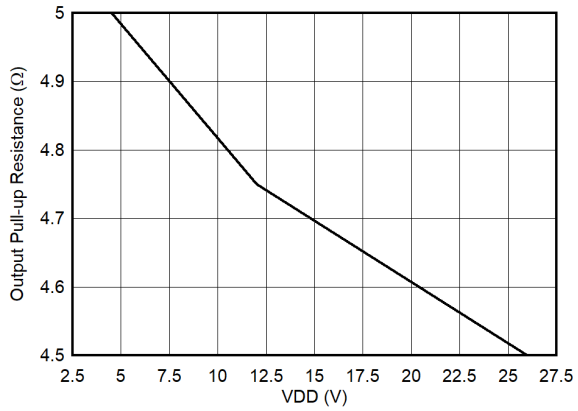


Figure 6-12. Output Pullup Resistance

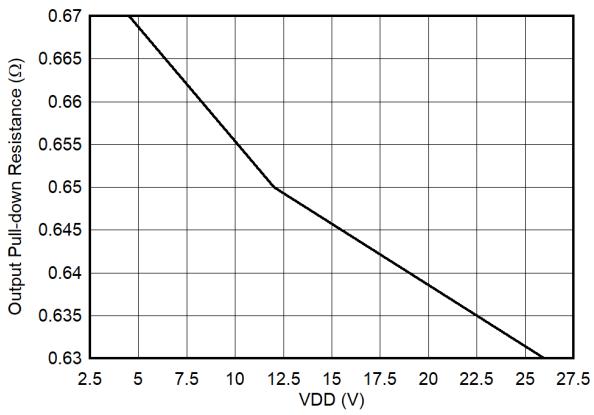
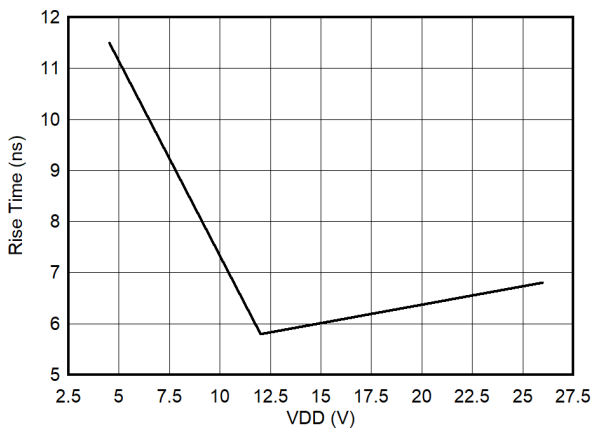


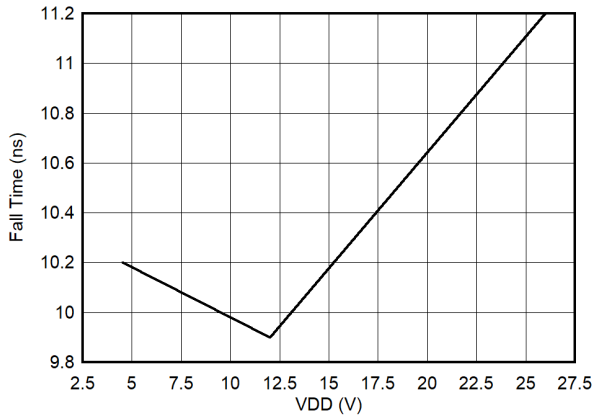
Figure 6-13. Output Pulldown Resistance



C_{LOAD} = 1.8 nF

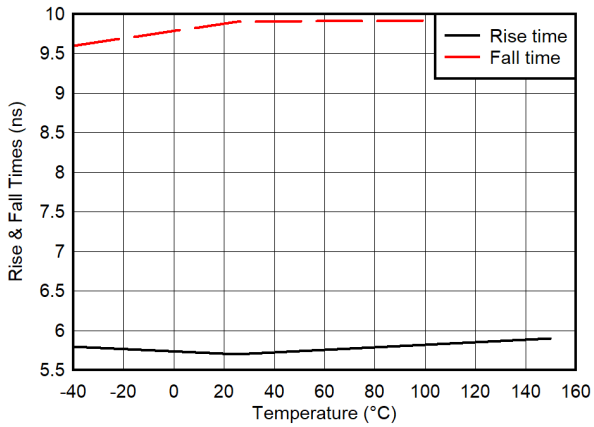
Figure 6-14. Output Rise Time vs VDD

ADVANCE INFORMATION



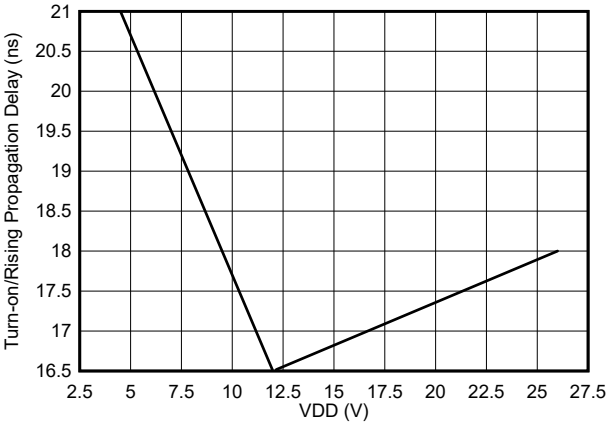
C_{LOAD} = 1.8 nF

Figure 6-15. Output Fall Time vs VDD



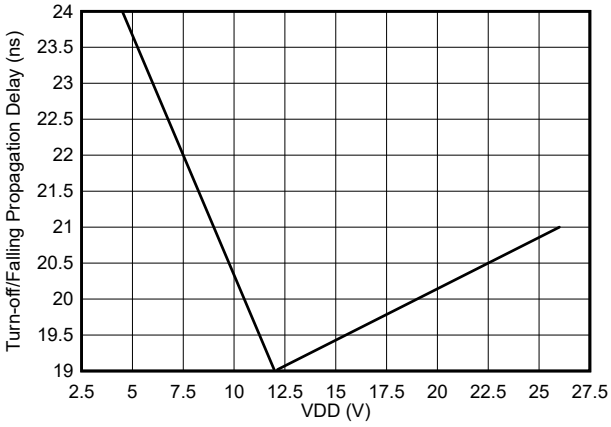
C_{LOAD} = 1.8 nF

Figure 6-16. Output Rise and Fall Time vs Temperature



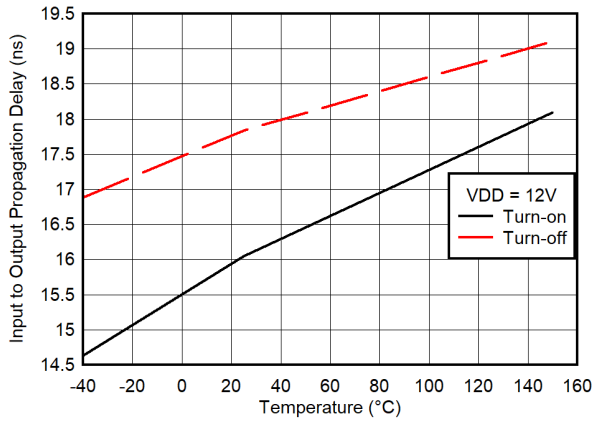
C_{LOAD} = 1.8 nF

Figure 6-17. Input to Output Rising (Turn-On) Propagation Delay vs VDD



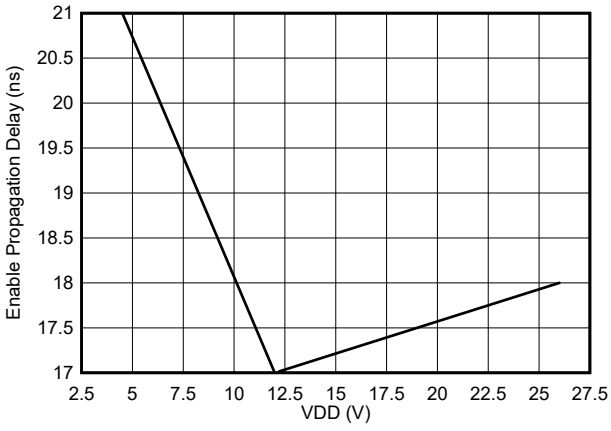
C_{LOAD} = 1.8 nF

Figure 6-18. Input to Output Falling (Turn-Off) Propagation Delay vs VDD



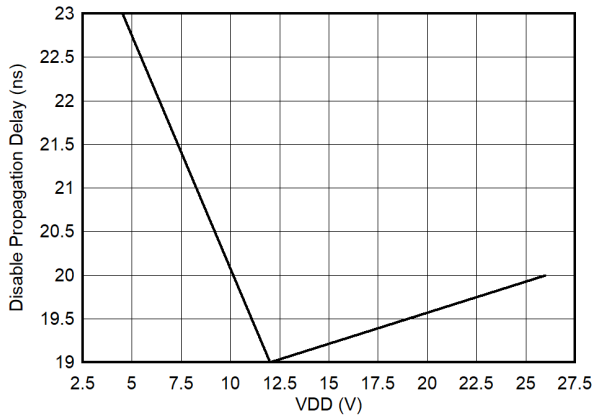
C_{LOAD} = 1.8 nF

Figure 6-19. Input Propagation Delay vs Temperature



C_{LOAD} = 1.8 nF

Figure 6-20. Enable to Output Rising Propagation Delay



C_{LOAD} = 1.8 nF

Figure 6-21. Enable to Output Falling Propagation Delay

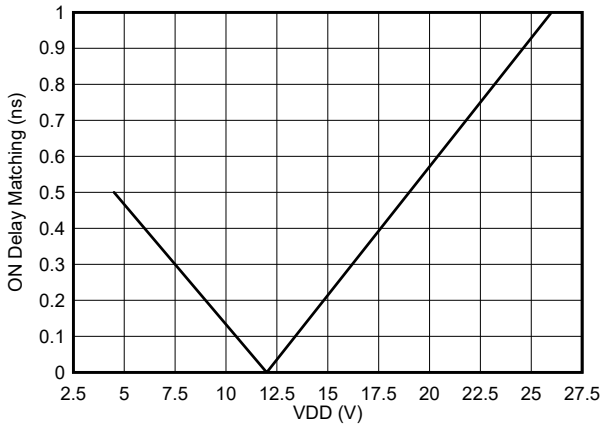


Figure 6-22. Turn-on/Rising Delay Matching

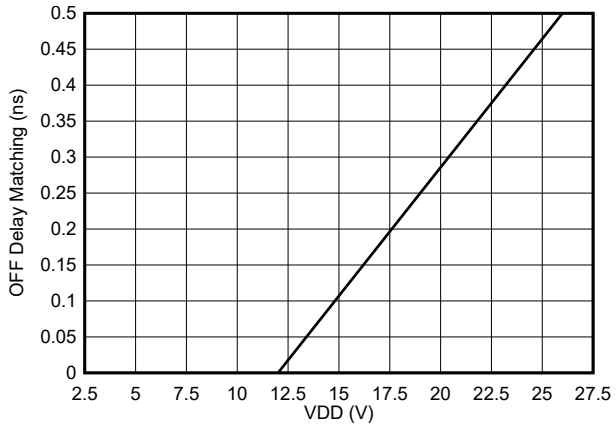


Figure 6-23. Turn-Off and Falling Delay Matching

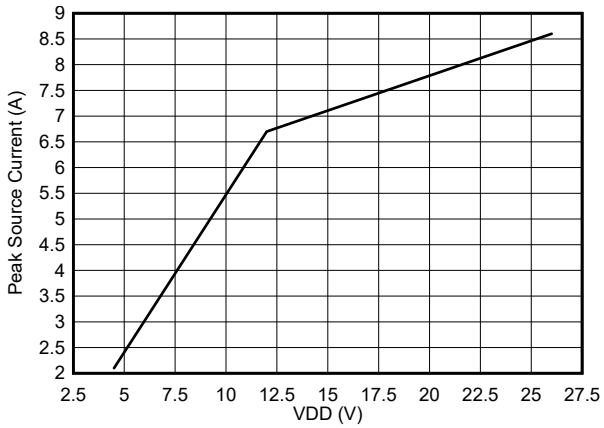


Figure 6-24. Peak Source Current vs VDD

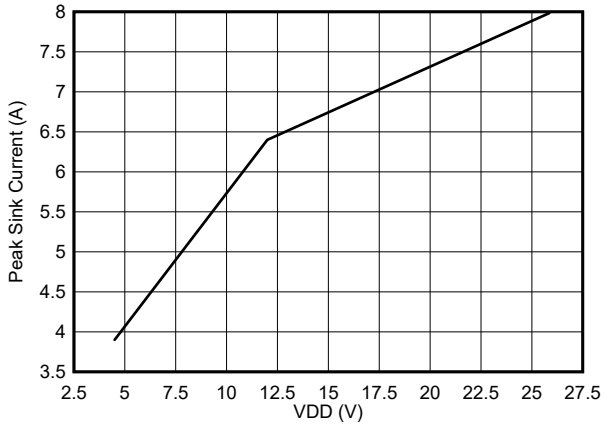


Figure 6-25. Peak Sink Current vs VDD

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The UCC27624-Q1 device represents TI's latest generation of dual-channel, low-side, high-speed, gate driver devices featuring 5-A source and sink current capability, fast switching characteristics, and a host of other features. *UCC27624-Q1 Features and Benefits* details the advantages of the gate driver's features, which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits. The robust inputs of UCC27624-Q1 can handle –10 V, ensuring reliable operation in noisy environments. The driver has good transient handling capability on its output due to its reverse current handling, as well as rail-to-rail output drive, and a small propagation delay (typically 17 ns). With this built-in robustness, the UCC27624-Q1 device can also be directly connected to a gate drive transformer.

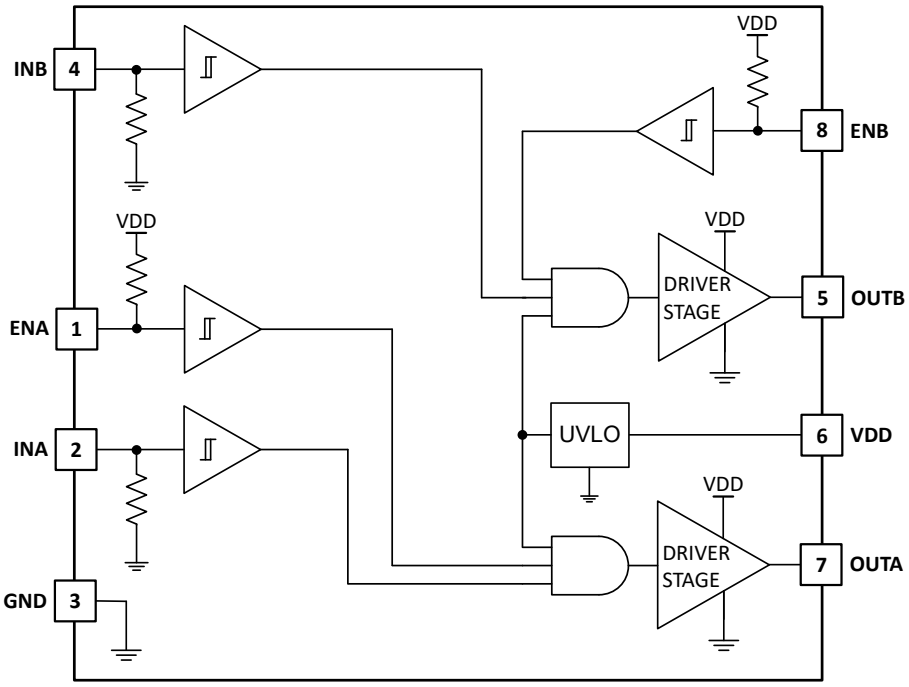
The input threshold of UCC27624-Q1 is compatible with TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS-based controllers as long as the threshold requirement is met. The 1-V typical hysteresis offers excellent noise immunity.

Each channel has an enable pin, ENx, with a fixed TTL compatible threshold. The ENx pins are internally pulled up. Pulling ENx low disables the corresponding channel, while leaving ENx open provides normal operation. The ENx pins can be used as an additional input with the same performance as the INx pins.

Table 7-1. UCC27624-Q1 Features and Benefits

FEATURE	BENEFIT
–10-V IN and EN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver
17-ns (typical) propagation delay	Extremely low-pulse transmission distortion
1-ns (typical) delay matching between channels	Ease of paralleling outputs for higher (two times) current capability. This helps when driving parallel-power switches.
Expanded VDD operating range of 4.5 V to 26 V	Flexibility in system design. Covers a wide range of power switches
Expanded operating temperature range of –40°C to +150°C	Flexibility in system design. System robustness improvement
VDD UVLO protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
Outputs are held low when input pins (INx) are in floating condition.	Protection feature, especially useful in passing abnormal condition tests during safety certification
Outputs are enabled when enable pins (ENx) are in floating condition.	Pin-to-pin compatibility with legacy devices from Texas Instruments in designs where Pin 1 and Pin 8 are "No Connect" pins
Input and enable threshold with wide hysteresis	Enhanced noise immunity while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Inputs independent of VDD	System simplification, especially related to auxiliary bias supply architecture

7.2 Functional Block Diagram



Typical ENx pullup resistance is 200 kΩ and INx pulldown resistance is 120 kΩ.

7.3 Feature Description

7.3.1 Operating Supply Current

The UCC27624-Q1 device features low quiescent I_{DD} currents. The typical operating supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in the Electrical Characteristics table. The lowest quiescent current (I_{DD}) is achieved when the device is fully on and the outputs are in a static state (DC high or DC low). During this state, all of the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and any current related to pullup resistors on the enable pins. Knowing the operating switching frequency (f_{SW}) and the MOSFET gate charge (Q_G) at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

Typical Characteristics provides a complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages. The linear variation and close correlation with the theoretical value of the average I_{OUT} indicate a negligible shoot-through inside the gate driver device, displaying its high-speed characteristics.

7.3.2 Input Stage

The input pins of the UCC27624-Q1 gate driver device are based on a TTL compatible input threshold logic that is independent of the VDD supply voltage. With a high threshold of 2 V and a low threshold of 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power controller devices. Wider hysteresis (1-V typical) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27624-Q1 devices also feature tight control of the input pin threshold voltage levels, which eases system design considerations and ensures stable operation across temperature (refer to *Typical Characteristics*). The very low input capacitance on these pins reduces loading and increases switching speed.

ADVANCE INFORMATION

The UCC27624-Q1 device features an important protection feature that holds the output of a channel low when the respective input pin is in a floating condition. This is achieved through the internal pulldown resistors to ground on both of the input pins (INA, INB), as shown in .

The input pins can handle wide range of slew rate. In most power supply applications, the gate driver is either driven by the output of a digital controller or logic gates. Therefore, in most applications the input signal slew rate is fast and is no concern for the UCC27624 family of devices. The wide hysteresis offered in UCC27624-Q1 alleviates the concern of chattering compared to many other drivers that have very small hysteresis at the input. If limiting the rise or fall times to the power device is the primary goal, then an external gate resistor is highly recommended between the output of the driver and the gate of the switching power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. In short, some of the power gets dissipated in the gate resistor rather than inside of the gate driver. Additionally, the input pins of UCC27624-Q1 are capable of handling –10 V. This improves the system robustness in noisy (electrical) applications. This also enables the driver to directly connect to the output of a gate drive transformer without the use of rectifying diodes, which saves board space and BOM cost.

7.3.3 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs are disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27624-Q1 device is equipped with independent enable pins (ENx) for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the driver outputs are disabled. Similar to the input pins, the enable pins are also based on a TTL compatible threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V or 5-V controllers. The UCC27624-Q1 device also features tight control of the enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The ENx pins are internally pulled up to VDD using pullup resistors, as a result of which the outputs of the device are enabled in the default state. Hence even if the ENx pins are left floating the driver output is enabled. Essentially, this floating allows the UCC27624-Q1 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27324, UCC27424, UCC27524), where Pin 1 and Pin 8 are either ENx or N/C pins. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB must be connected and driven together. The ENx pins of the UCC27624-Q1 are capable of handling –10 V, which improves system robustness in noisy (electrical) applications.

7.3.4 Output Stage

The UCC27624-Q1 device output stage features a unique architecture on the pullup structure, which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn-on. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.04 Ω when activated.

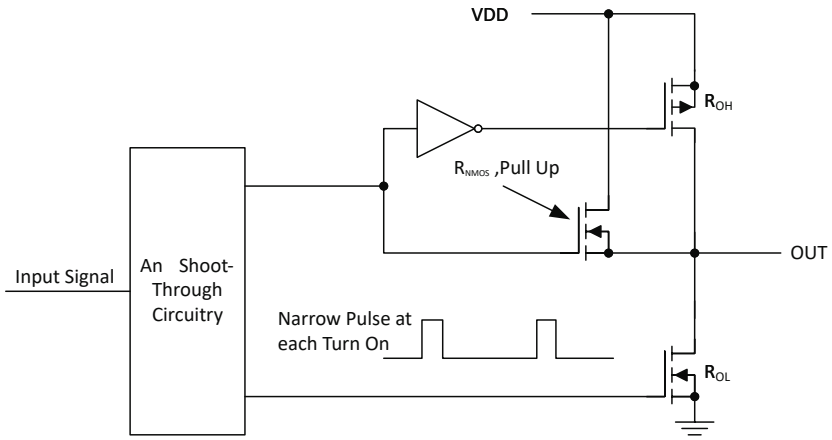


Figure 7-1. UCC27624-Q1 Gate Driver Output Structure

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27624-Q1 pull-up stage during the turn-on instance is much lower than what is represented by R_{OH} parameter.

The pull-down structure in the UCC27624-Q1 device is simply comprised of a N-Channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in the UCC27624-Q1 device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 5A of peak reverse current transients without damage to the device.

The UCC27624-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

7.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27624-Q1 driver device features a very small, 17-ns (typical) propagation delay between input and output, which offers the lowest level of pulse width distortion for high-frequency switching applications. For example, in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive the SR MOSFETs. Additionally, the driver devices also feature extremely accurate, 1-ns (typical) matched internal propagation delays between the two channels, which is beneficial for applications that require dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels driven by a common control signal from the PFC controller. In this case, the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion, minimizing turn-on and turn-off delay differences. Another benefit of the tight matching between the two channels is that the two channels can be connected together to effectively double the drive current capability. That is, A and B channels may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together; then, a single signal controls the paralleled power devices.

ADVANCE INFORMATION

7.4 Device Functional Modes

Table 7-2. Device Logic Table

ENA	ENB	INA	INB	UCC27624-Q1	
				OUTA	OUTB
H	H	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H
L	L	Any	Any	L	L
Any	Any	Float	Float	L	L
Float	Float	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to achieve fast switching of power devices and reduce associated switching-power losses, a powerful gate driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning ON a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn ON the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer-drive functions. Gate driver devices also find other needs ,such as minimizing the effect of high frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power device technologies, such as SiC MOSFETs and GaN switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include a wide operating voltage range (5 V to 26 V), low propagation delays, good delay matching, and availability in compact, low inductance packages with good thermal capability. In summary, gate driver devices are an extremely important component in switching power combining benefits of high performance, low cost, low component count, board space reduction, and simplified system design.

ADVANCE INFORMATION

8.2 Typical Application

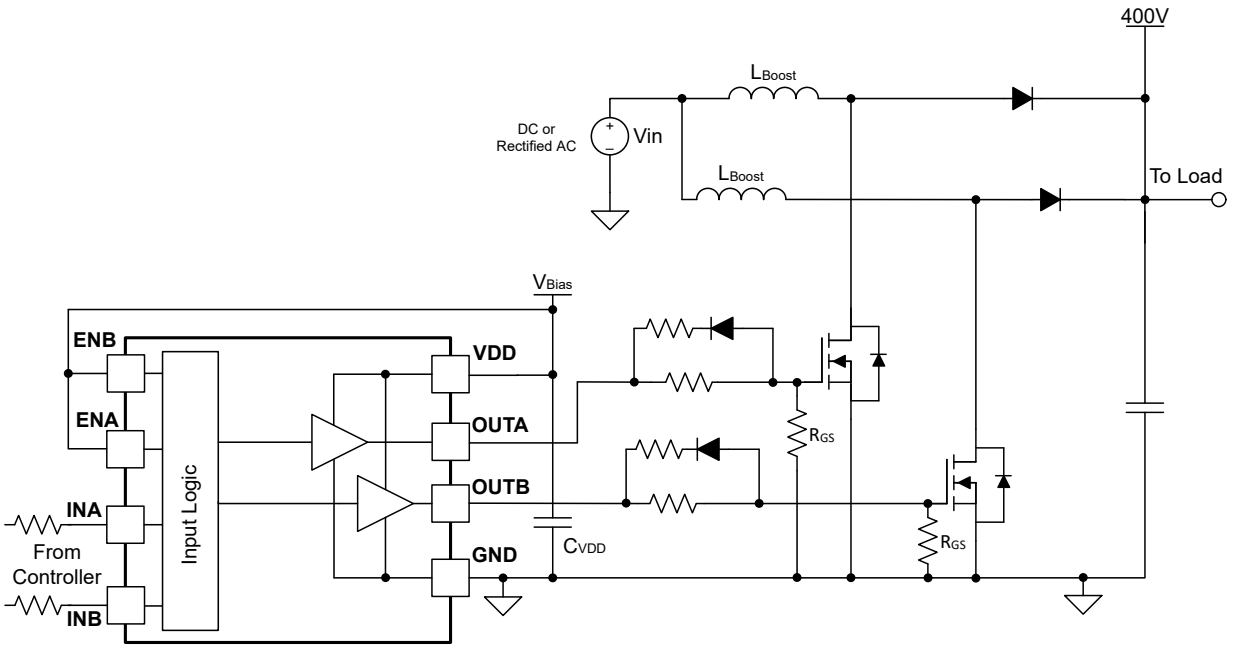


Figure 8-1. UCC27624-Q1 Typical Application Diagram

8.2.1 Design Requirements

When selecting and designing-in the gate driver device for an end application, some functional aspects must be considered and evaluated first, in order to make the most appropriate selection. Among these considerations are bias voltage, UVLO, drive current, and power dissipation.

8.2.2 Detailed Design Procedure

8.2.2.1 VDD and Undervoltage Lockout

The UCC27624-Q1 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4 V with 300-mV typical hysteresis. This hysteresis prevents chatter when VDD supply voltages have noise, specifically at the lower end of the VDD operating range. UVLO hysteresis is also important to avoid any false tripping due to the bias noise generated because of fast switching transitions, where large peak currents are drawn from the bias supply bypass capacitors. The driver capability to operate at wide bias voltage range, along with good switching characteristics, is especially important in driving emerging power semiconductor devices, such as advanced low gate charge fast MOSFETs, GaN FETs, and SiC MOSFETs.

At power-up, the UCC27624-Q1 driver device output remains low until the VDD voltage reaches the UVLO rising threshold, irrespective of the state of any other input pins such as INx and ENx. After the UVLO rising threshold, the magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached.

For the best high-speed circuit performance and to prevent noise problems because the device draws current from the VDD pin to bias all internal circuits, use two VDD bypass capacitors. Also, use surface mount, low ESR capacitors. A 0.1-µF ceramic capacitor should be located less than 1 mm from the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (≥1 µF) must be connected in parallel (also as close to the driver IC as possible) to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

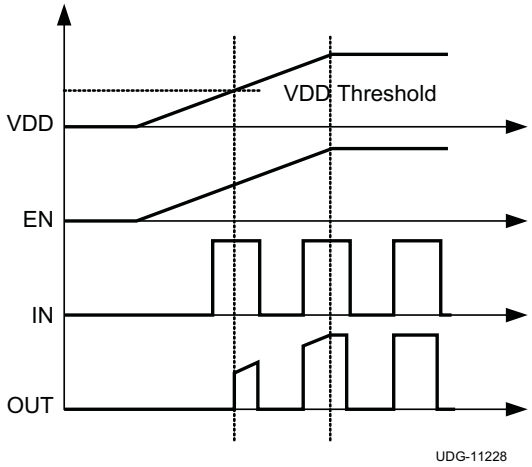


Figure 8-2. Power-Up Sequence

8.2.2.2 Drive Current and Power Dissipation

The UCC27624-Q1 driver is capable of delivering 5 A of peak current to a switching power device gate (MOSFET, IGBT, SiC MOSFET, GaN FET) for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn ON the device quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground, which repeats at the operating switching frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out).
- Switching frequency
- External gate resistors

Because UCC27624-Q1 features low-quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is very small compared to the losses due to switching of the power device.

When a driver device is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. The following equation provides an example of the energy that must transfer from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{1}$$

where

- C_{LOAD} is the load capacitor.
- V_{DD} is the bias voltage of the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. This leads to a total power loss, as shown in the following equation example.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{2}$$

where

- f_{SW} is the switching frequency.

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz, the switching power loss is calculated as follows:

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \tag{3}$$

ADVANCE INFORMATION

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must dissipate when charging a capacitor is determined, which by using the equivalence $Q_g = C_{LOAD}V_{DD}$ is shown in the following equation.

$$P_G = C_{LOAD}V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

Assuming that the UCC27624-Q1 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated using the equation below.

$$P_G = 2 \times 60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \quad (6)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure)

The above equation is necessary when the external gate resistor is large enough to reduce the peak current of the driver. In addition to the above gate-charge related power dissipation, dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in the electrical characteristics table, the quiescent current is less than 1 mA. The power loss due to DC current consumption of the driver internal circuit can be calculated as below.

$$P_Q = I_{DD} V_{DD} \quad (7)$$

Assuming total internal current consumption to be 0.6 mA (typical) at bias voltage of 12 V, the DC power loss in the driver is:

$$P_Q = 0.6\,mA \times 12\,V = 7.2\,mW \quad (8)$$

This power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\,W}{12\,V} = 0.036\,A \quad (9)$$

If the gate driver is used with inductive load, then special attention should be paid to the ringing on each pin of the gate driver device. The ringing should not exceed the recommended operating rating of the pin.

8.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27624-Q1 device used in high-voltage boost converter application. In this application, the UCC27624-Q1 is driving the IGBT switch that has a gate charge of
110 nC.

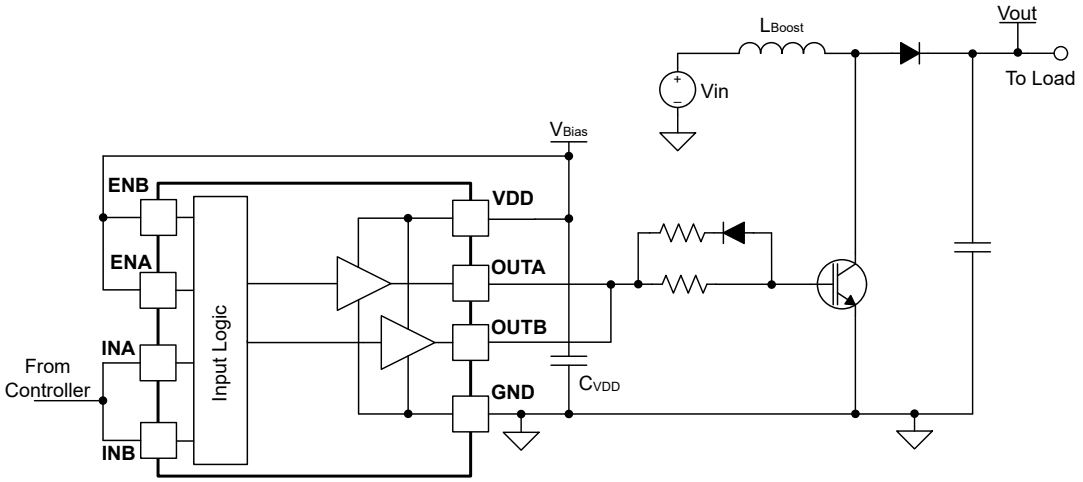
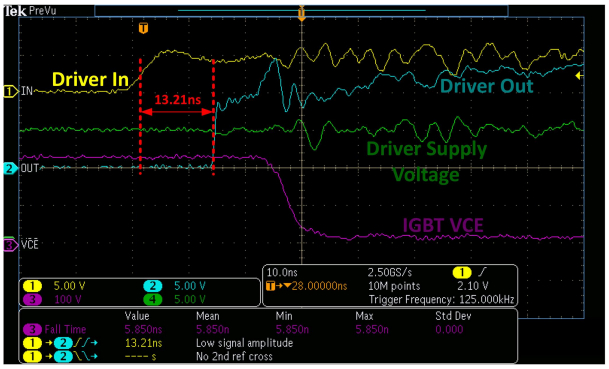
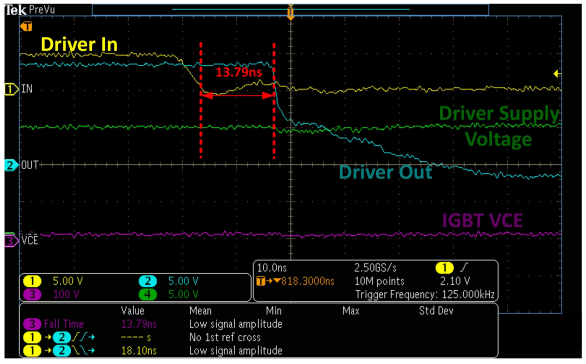


Figure 8-3. UCC27624-Q1 Used to Drive IGBT in the Boost Converter



Vin = 210 V, Vout = 235 V, Iout = 1.14 A, Fsw = 125 kHz, driver supply voltage = 15 V, gate resistor = 0 Ω

Figure 8-4. Turn-On Propagation Delay Waveform



Vin = 210 V, Vout = 235 V, Iout = 1.14 A, Fsw = 100 kHz, driver supply voltage = 15 V, gate resistor = 0 Ω

Figure 8-5. Turn-Off Propagation Delay Waveform

ADVANCE INFORMATION

9 Power Supply Recommendations

The bias supply voltage range for the UCC27624-Q1 device is rated to operate is from 4.5 V to 26 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. If the driver is in a UVLO condition when the V_{DD} pin voltage is below the VDD UVLO turn-on (rising) threshold, the UVLO protection feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 30-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). It is necessary to have sufficient margin from the absolute maximum rating of the device to realize full operating life of the device. Therefore, the upper limit of recommended voltage of the VDD pin is 26 V.

The UVLO protection feature also has a hysteresis function. This means, when the VDD pin bias voltage exceeds the rising threshold voltage, the device begins to operate normally. If the VDD bias voltage drops below the rising threshold while on, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification of the falling threshold. Therefore, while operating at or near the 4.5-V, design engineer should ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device. Otherwise, the device output may turn-off. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD turn-off (falling) threshold, which must be accounted for while evaluating system shutdown timing or sequencing requirements. At system startup, the device does not begin operation until the VDD pin voltage has exceeded VDD turn-on (rising) threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin capacitor, is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that the local bypass capacitors are provided between the VDD and GND pins and locate them as close to the device pins as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is required. TI recommends having two capacitors: a 0.1-µF ceramic surface-mount capacitor placed less than 1 mm from the VDD pin of the device and another larger ceramic capacitor (≥1 µF) must be connected in parallel.

UCC27624-Q1 is a high-current gate driver. If the gate driver is placed far from the switching power device, such as a MOSFET, then that could create a large inductive loop. A large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress that exceeds device recommended ratings. Therefore, place the gate driver as close to the switching power device as possible. Also, use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27624-Q1 gate driver incorporates small propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate very quick voltage transitions. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver IC as close as possible to the power device in order to minimize the length of high-current traces between the driver IC output pins and the gate of the switching power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver IC with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD pin, during turn-on of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as 50V rated X7R chip capacitors are highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances, namely during turn-on and turn-off transients, which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin of the driver IC may corrupt the input signals of the driver IC. The ground plane must not be a conduction path for any high current (power stage) loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- External gate resistor and parallel diode-resistor combination may come in handy when replacing any gate driver IC with UCC27624-Q1 device in existing or new designs, specifically if they do not have the same drive strength.

ADVANCE INFORMATION

10.2 Layout Example

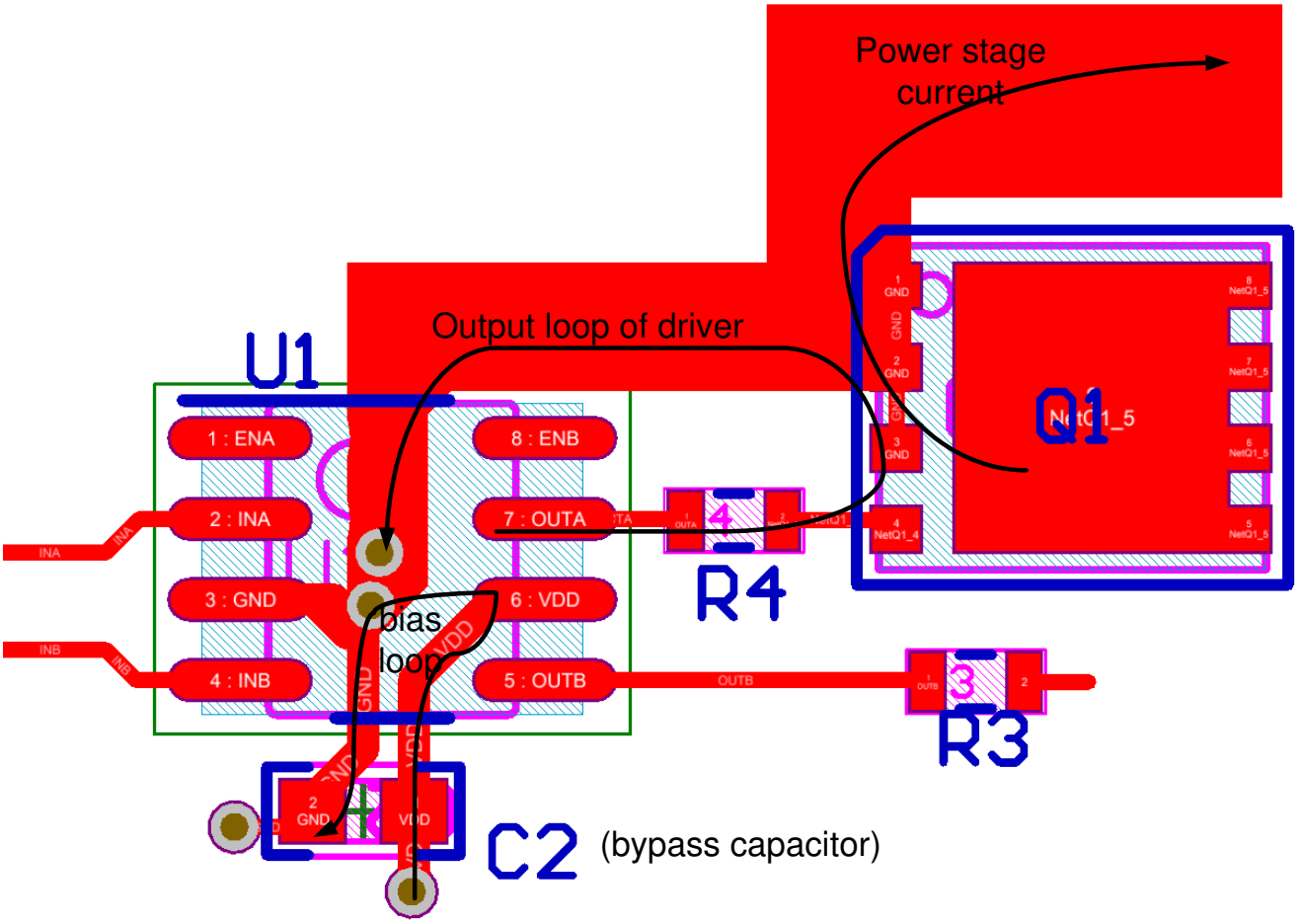


Figure 10-1. UCC27624-Q1 Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within the specified limit. For detailed information regarding the thermal information table, please refer to the *Semiconductor and IC Package Thermal Metrics Application Note* (SPRA953).

Among the different package options available for the UCC27624-Q1 device, power dissipation capability of the DGN package is of particular mention. The VSSOP-8 (DGN) package offers thermal pad for removing the heat from the semiconductor junction through the bottom of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the VSSOP-8 package are not directly connected to any leads of the package, however, PowerPAD is thermally connected to the substrate of the device. TI recommends to externally connect the exposed pads to GND pin of the driver IC in PCB layout.

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC27624QDRQ1	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

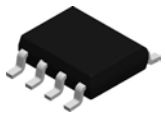
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27624-Q1 :

- Catalog : UCC27624

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

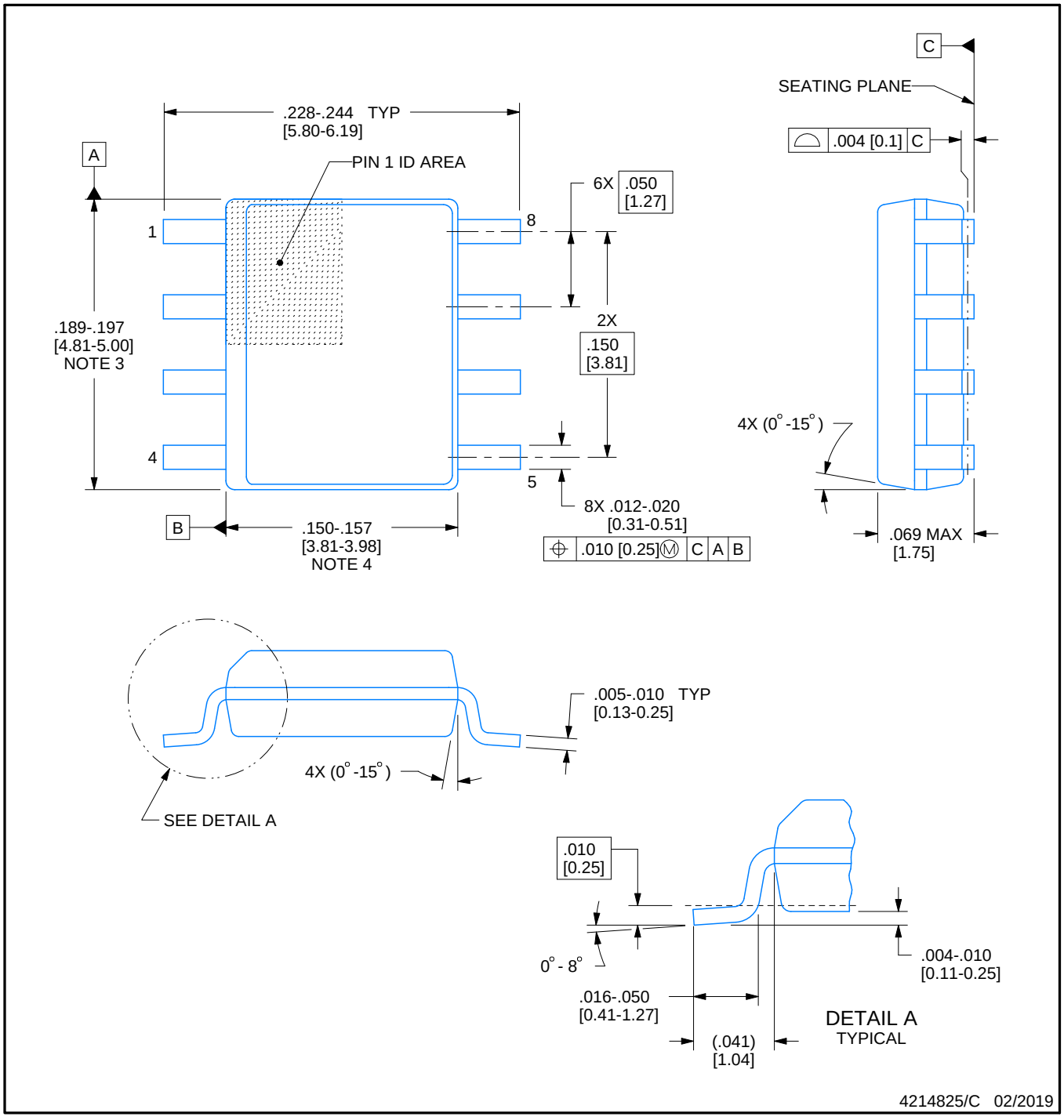


PACKAGE OUTLINE

D0008A

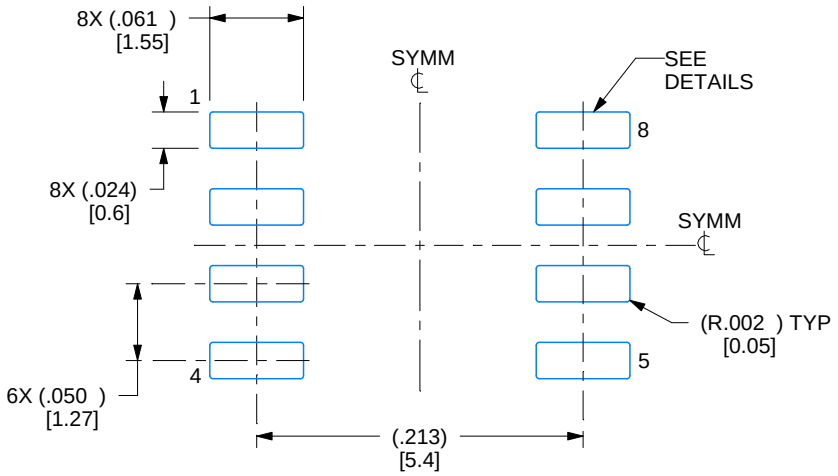
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

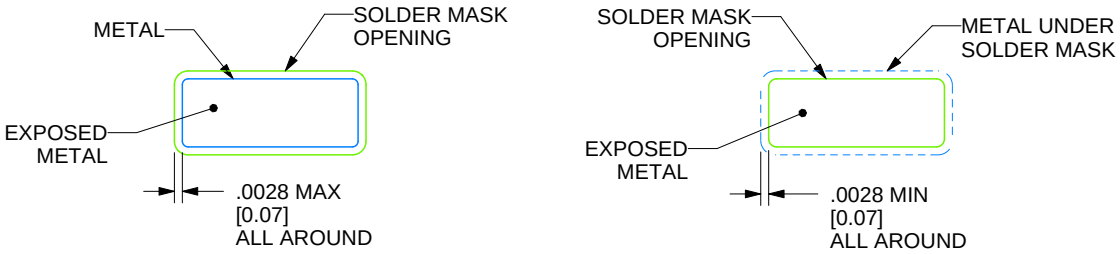


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

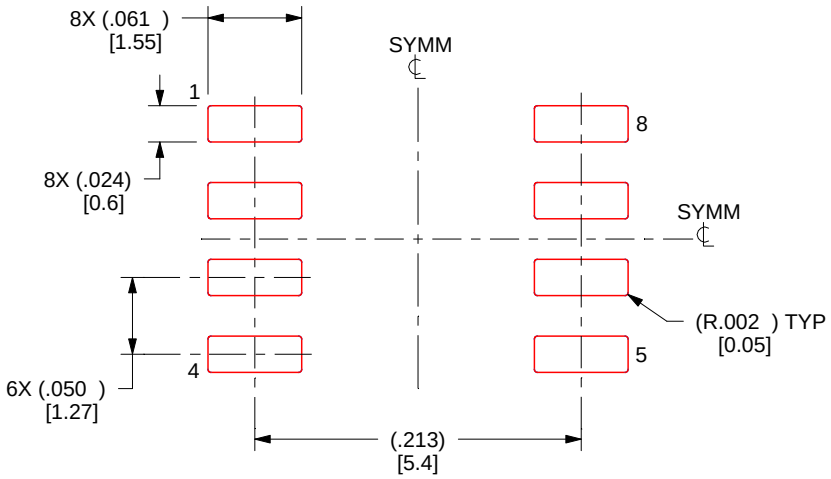
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

CD4027B CMOS Dual J-K Flip Flop

1 Features

- Set-reset capability
- Static flip-flop operation – retains state indefinitely with clock level either *high* or *low*
- Medium speed operation – 16 MHz (typical) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC tentative standard No. 138, *standard specifications for description of 'B' series CMOS devices*

2 Applications

- Registers, counters, control circuits

3 Description

CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K flip flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatibile operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the postitive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffice), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

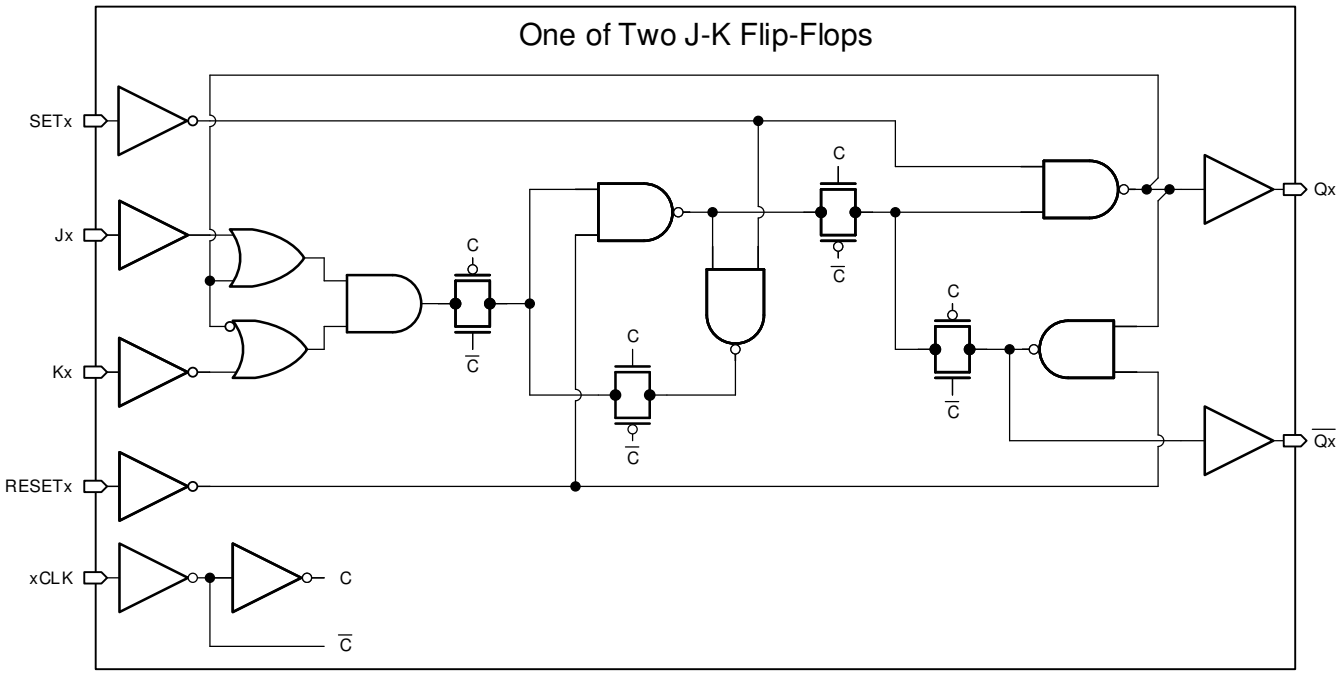


Figure 3-1. Logic Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2003) to Revision D (July 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

5 Pin Configuration and Functions

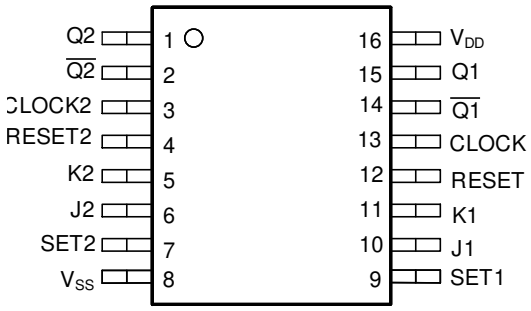


Figure 5-1. Terminal Assignment

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK1	13	I	Clock input for channel 1
CLOCK2	3	I	Clock input for channel 2
J1	10	I	J input for channel 1
J2	6	I	J input for channel 2
K1	11	I	K input for channel 1
K2	5	I	K input for channel 2
Q1	15	O	Q output for channel 1
$\overline{Q1}$	14	O	Inverted Q output for channel 1
Q2	1	O	Q output for channel 2
$\overline{Q2}$	2	O	Inverted Q output for channel 2
RESET1	12	I	Reset input for channel 1
RESET2	4	I	Reset input for channel 2
SET1	9	I	Set input for channel 1
SET2	7	I	Set input for channel 2
V_{DD}	16	—	Supply
V_{SS}	8	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{DD}	DC Supply Voltage Range	Voltages referenced to V_{SS} Terminal	–0.5	20	V
All Inputs	Input Voltage Range		–0.5	V_{DD} + 0.5	V
Any One Input	DC Input Current			±10	mA
P_D	Power Dissipation per Package	For T_A = –55°C to + 100°C		500	mW
		For T_A = +100°C to +125°C	12mW/°C	200	mW
	Device Dissipation per Output Transistor	For T_A = Full package-temperature range (all package types)		100	mW
T_A	Operating- Temperature Range		–55	125	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead Temperatur (During Soldering)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max		265	°C

6.2 Recommended Operating Conditions

at T_A = 25°C, except as noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC			V_{DD} (V)	LIMITS		UNIT
				ALL PACKAGES		
				MIN	MAX	
	Supply-Voltage Range	For T_A = Full Package Temperature Range		3	18	V
t_S	Data Setup Time		5	200		ns
			10	75		
			15	50		
t_W	Clock Pulse Width		5	140		ns
			10	60		
			15	40		
f_{CL}	Clock Input Frequency (Toggle Mode)		5		3.5	MHz
			10	dc	8	
			15		12	
t_rCL, t_fCL(1)	Clock Rise or Fall Time		5		45	µs
			10		5	
			15		2	
t_W	Set or Reset Pulse Width		5	180		ns
			10	80		
			15	50		

(1) If more than one unite is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transitiopn time of the output driving stage for the estimated capacitive load.

6.3 Static Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNIT
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	–40	+85	+125	+25			
								MIN	TYP	MAX	
Quiescent		0, 5	5	1	1	30	30		0.02	1	μa
Device		0, 10	10	2	2	60	60		0.02	2	μa
Current		0, 15	15	4	4	120	120		0.02	4	μa
I_{DD} Max.		0, 20	20	20	20	600	600		0.04	20	μa
Output Low (Sink)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1		mA
Current	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6		mA
I_{OL} Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8		mA
Output High	4.6	0, 5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1		mA
(Source)	2.5	0, 5	5	–2	–1.8	–1.3	–1.15	–1.6	–3.2		mA
Current	9.5	0, 10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6		mA
I_{OH} Min.	13.5	0, 15	15	– 4.2	–4	–2.8	–2.4	–3.4	–6.8		mA
Output Voltage		0, 5	5	0.05					0	0.05	V
Low-Level		0, 10	10	0.05					0	0.05	V
V_{OL} Max.		0, 15	15	0.05					0	0.05	V
Output Voltage		0, 5	5	4.95				4.95	5		V
High-Level		0, 10	10	9.95				9.95	10		V
V_{OH} Min.		0, 15	15	14.95				14.95	15		V
Input Low	0,5, 4.5		5	1.5						1.5	V
Voltage	1, 9		10	3						3	V
V_{IL} Max.	1.5, 13.5		15	4						4	V
Input High	0.5, 4.5		5	3.5				3.5			V
Voltage	1, 9		10	7				7			V
V_{IH} Min.	1.5, 13.5		15	11				11			V
Input Current, V_{IH} Max.		0, 18	18	±0.1	±0.1	±1	±1		$\pm 10^{-5}$	±0.1	μA

6.4 Dynamic Electrical Characteristics

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Propagation Delay Time	5		150	300	ns
Clock to Q or $\overline{Q}$ Outputs	10		65	130	ns
t_{PHL}, t_{PLH}	15		45	90	ns
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5		150	300	ns
	10		65	130	ns
	15		45	90	ns
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5		200	400	ns
	10		85	170	ns
	15		60	120	ns
Transition Time	5		100	200	ns
t_{THL}, t_{TLH}	10		50	100	ns
	15		40	80	ns

6.4 Dynamic Electrical Characteristics (continued)

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Maximum Clock Input Frequency (Toggle Mode)(1) f_{CL}	5	3.5	7		MHz
	10	8	16		
	15	12	24		
Minimum Clock Pulse Width, t_W	5		70	140	ns
	10		30	60	
	15		20	40	
Minimum Set or Reset Pulse Width, t_W	5		90	180	ns
	10		40	80	
	15		25	50	
Minimum Data Setup Time, t_S	5		100	200	ns
	10		35	75	
	15		25	50	
Clock Input Rise or Fall Time t_{rCL}, t_{fCL}	5			45	µs
	10			5	
	15			2	
Input Capacitance, C_I			5	7.5	pF

(1) Input t_r, t_f = 5 ns

6.5 Typical Characteristics

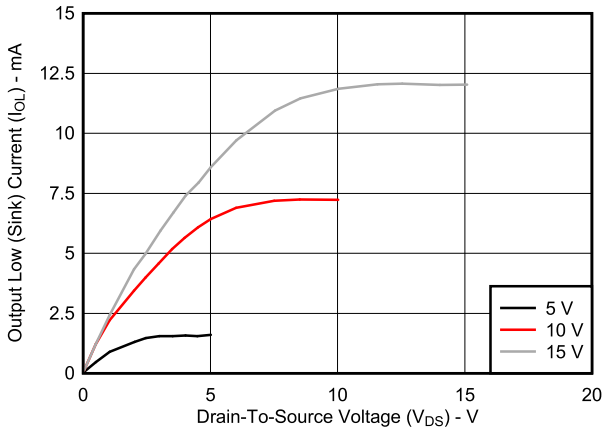


Figure 6-1. Typical Output Low (Sink) Current Characteristics

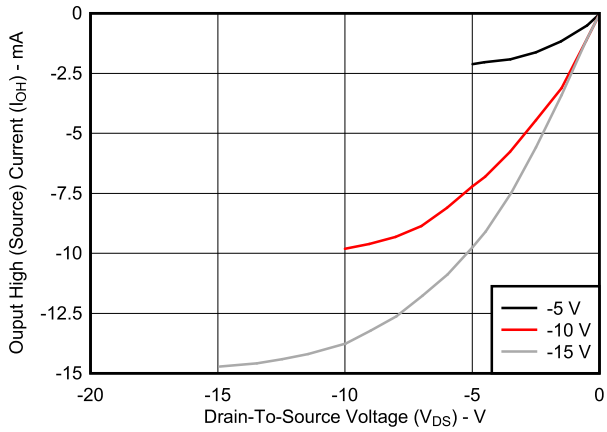


Figure 6-2. Typical Output High (Source) Current Characteristics

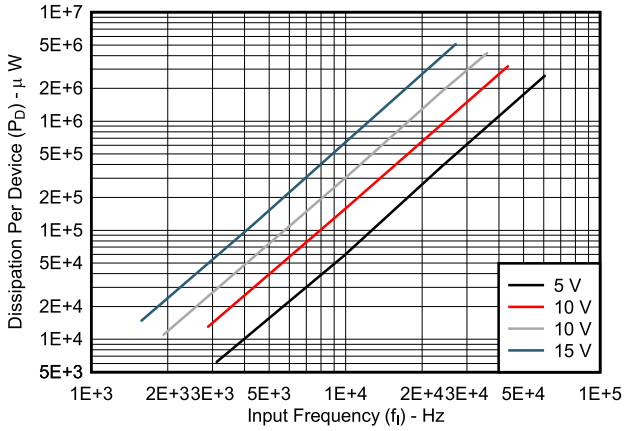


Figure 6-3. Typical Power Dissipation vs Frequency

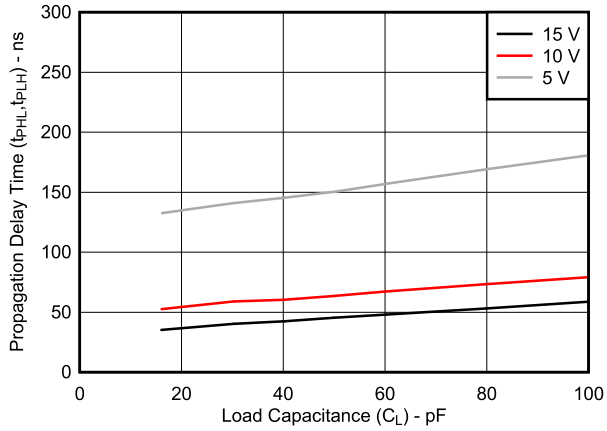


Figure 6-4. Typical Propagation Delay Time vs Load Capacitance (Clock or Set to Q, Clock or Reset to $\overline{Q}$)

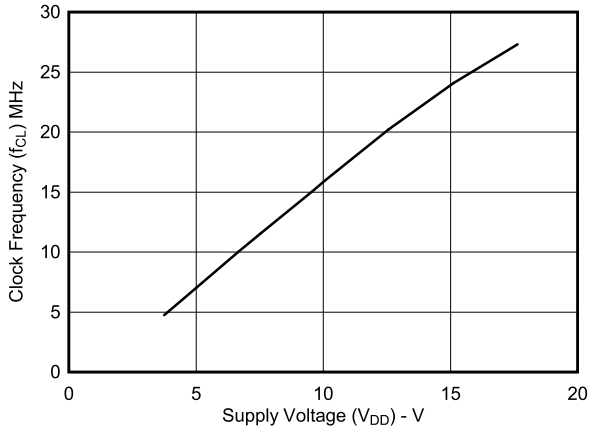


Figure 6-5. Typical Maximum Clock Frequency vs Supply Voltage (Toggle Mode)

7 Parameter Measurement Information

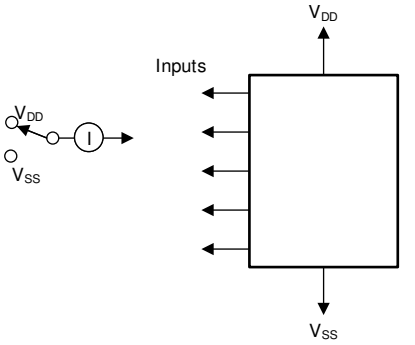


Figure 7-1. Input Current Test Circuit

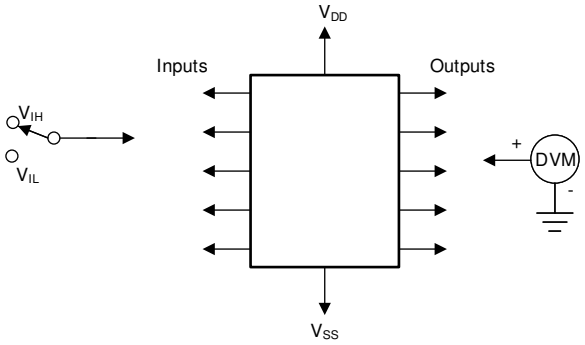


Figure 7-2. Input-Voltage Test Circuit

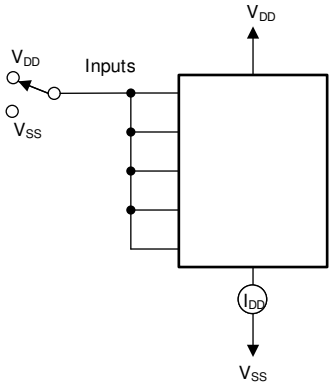
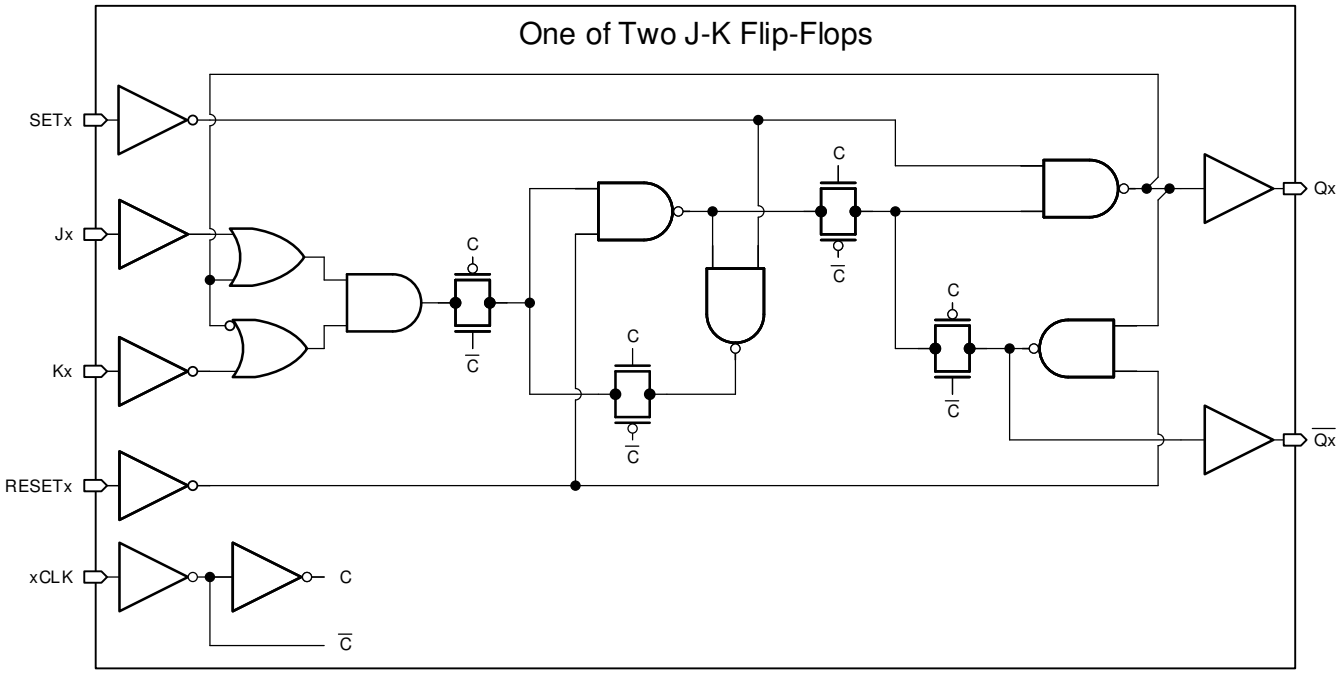


Figure 7-3. Quiescent Device Current Test Circuit

8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes[1]

PRESENT STATE					CL[2]	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	O	_/‾	O	$\overline{O}$
I	X	O	O	O	_/‾	I	O
X	O	O	O	I	_/‾	I	O
O	X	O	O	O	_/‾	O	I
X	I	O	O	I	_/‾	O	I
X	X	O	O	X	‾_	No change	No change
X	X	I	O	X	X	I	O
X	X	O	I	X	X	O	I
X	X	I	I	X	X	I	I

(1) Logic I = High Level, Logic O = Low Level, X = Do not care
(2) Level change

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4027BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4027BE	Samples
CD4027BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF	Samples
CD4027BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4027BF3A	Samples
CD4027BM	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BM96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BME4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BMT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM	Samples
CD4027BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B	Samples
CD4027BNSRG4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B	Samples
CD4027BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
CD4027BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
CD4027BPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B	Samples
JM38510/05152BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples
M38510/05152BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05152BEA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4027B, CD4027B-MIL :

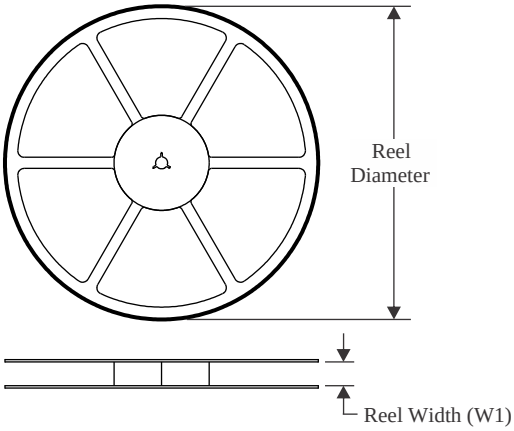
- Catalog : CD4027B
- Military : CD4027B-MIL

NOTE: Qualified Version Definitions:

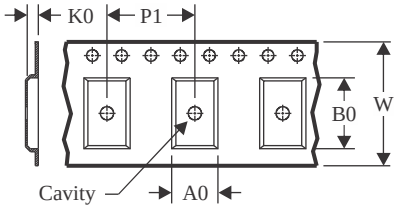
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

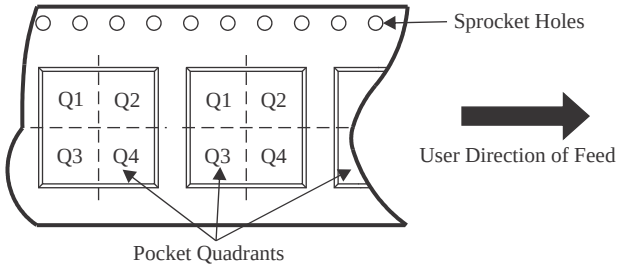


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

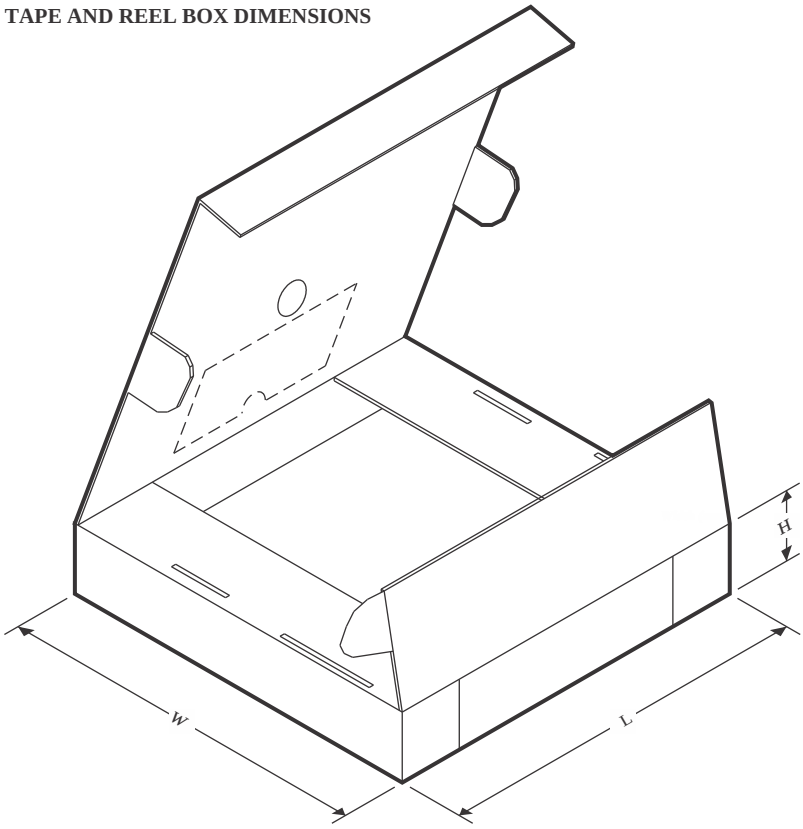
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

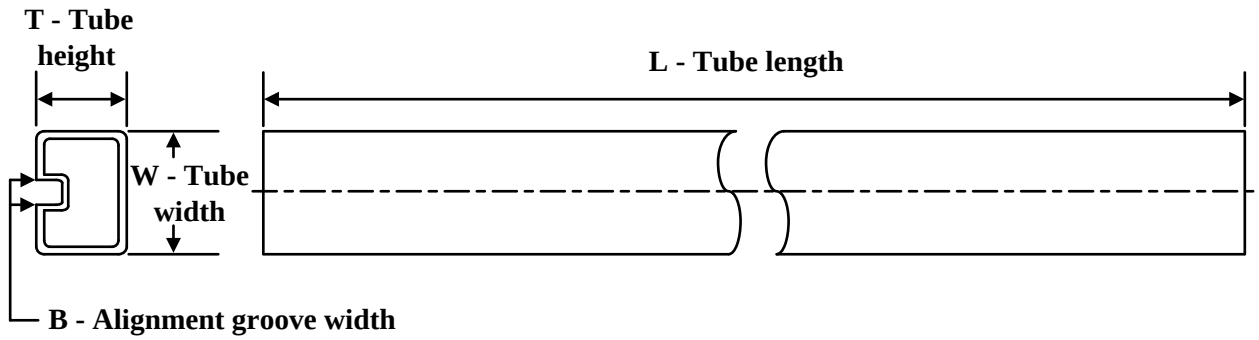
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4027BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD4027BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

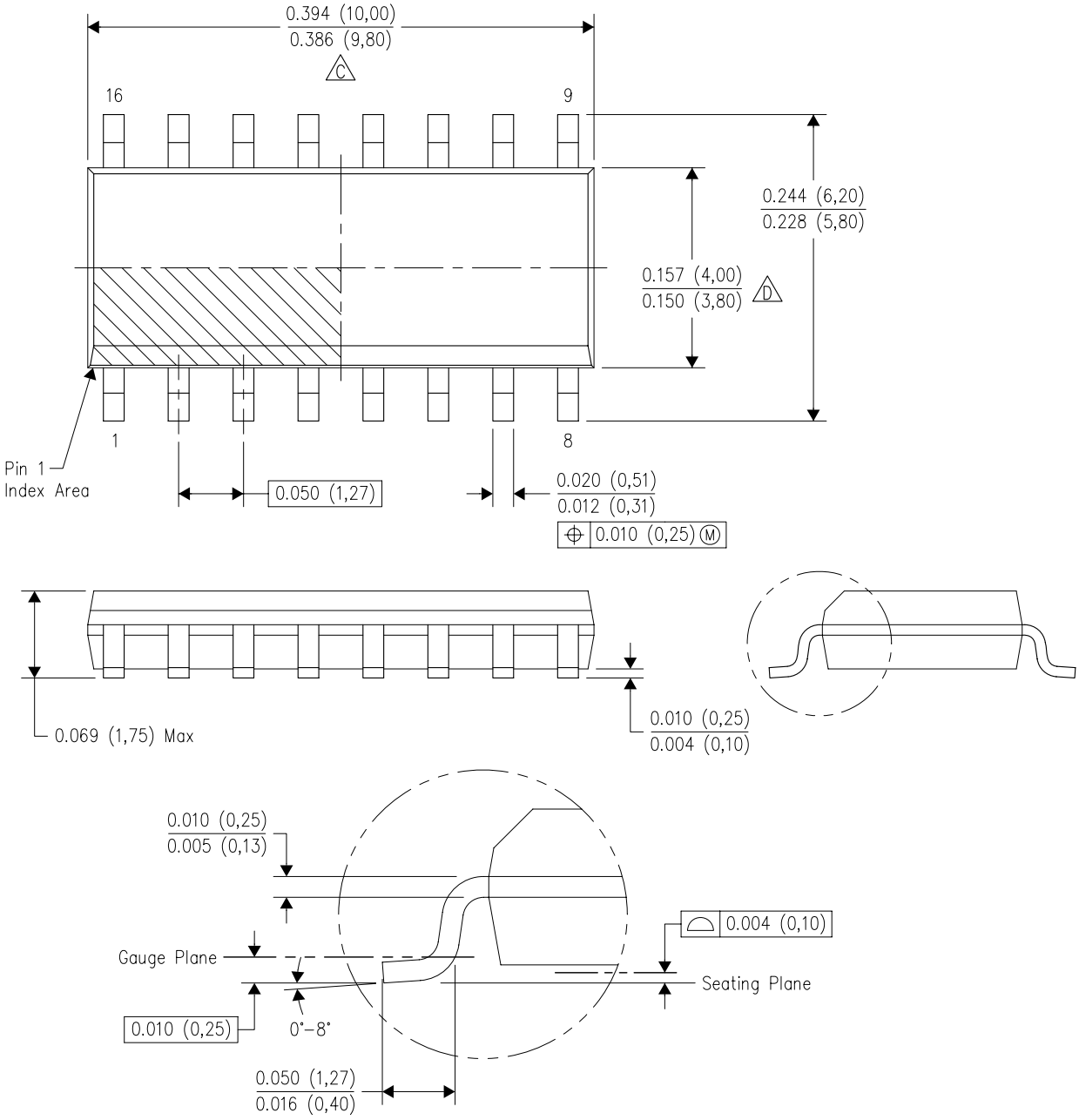
TUBE



*All dimensions are nominal

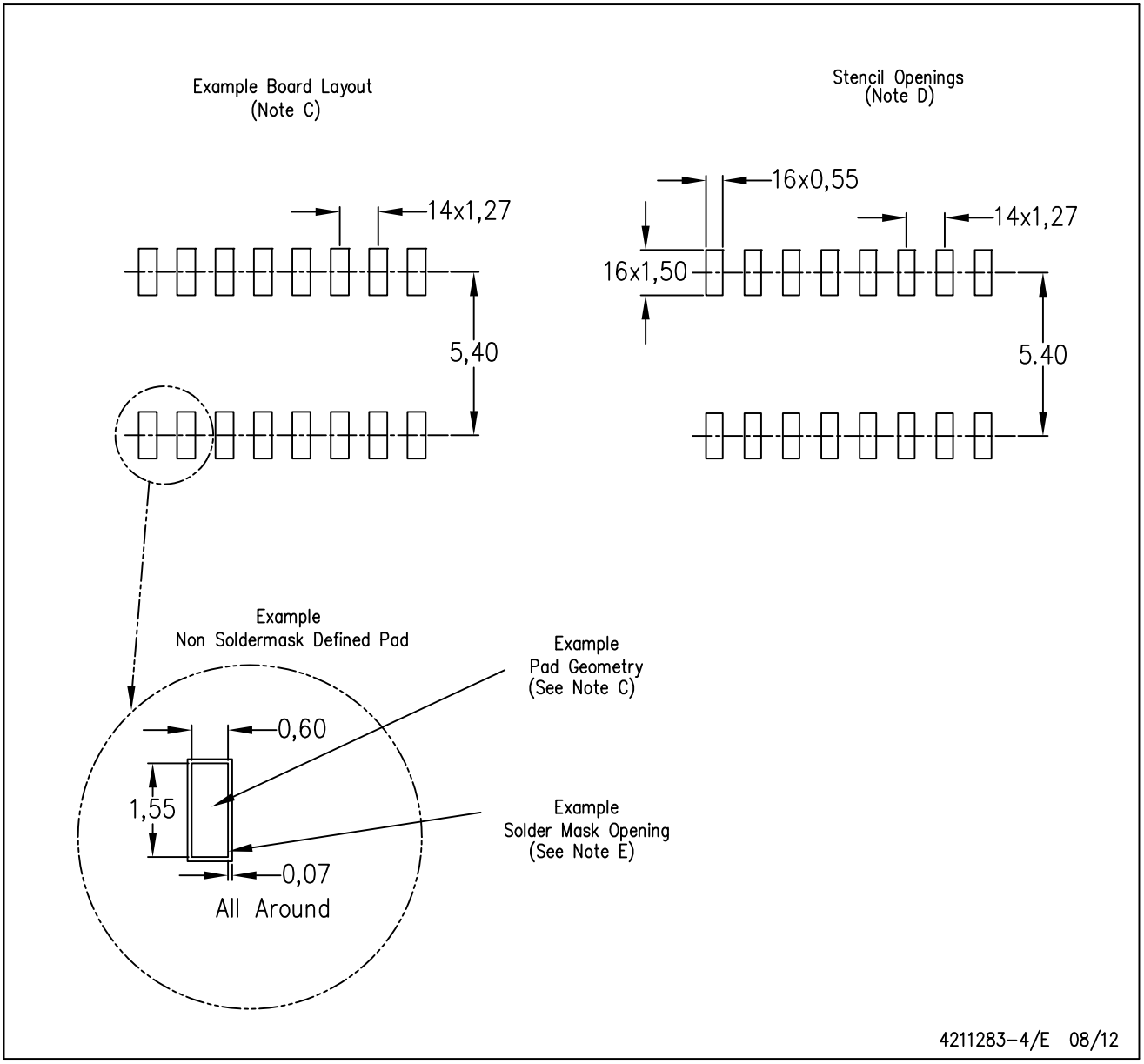
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BM	D	SOIC	16	40	507	8	3940	4.32
CD4027BME4	D	SOIC	16	40	507	8	3940	4.32
CD4027BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



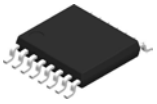
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

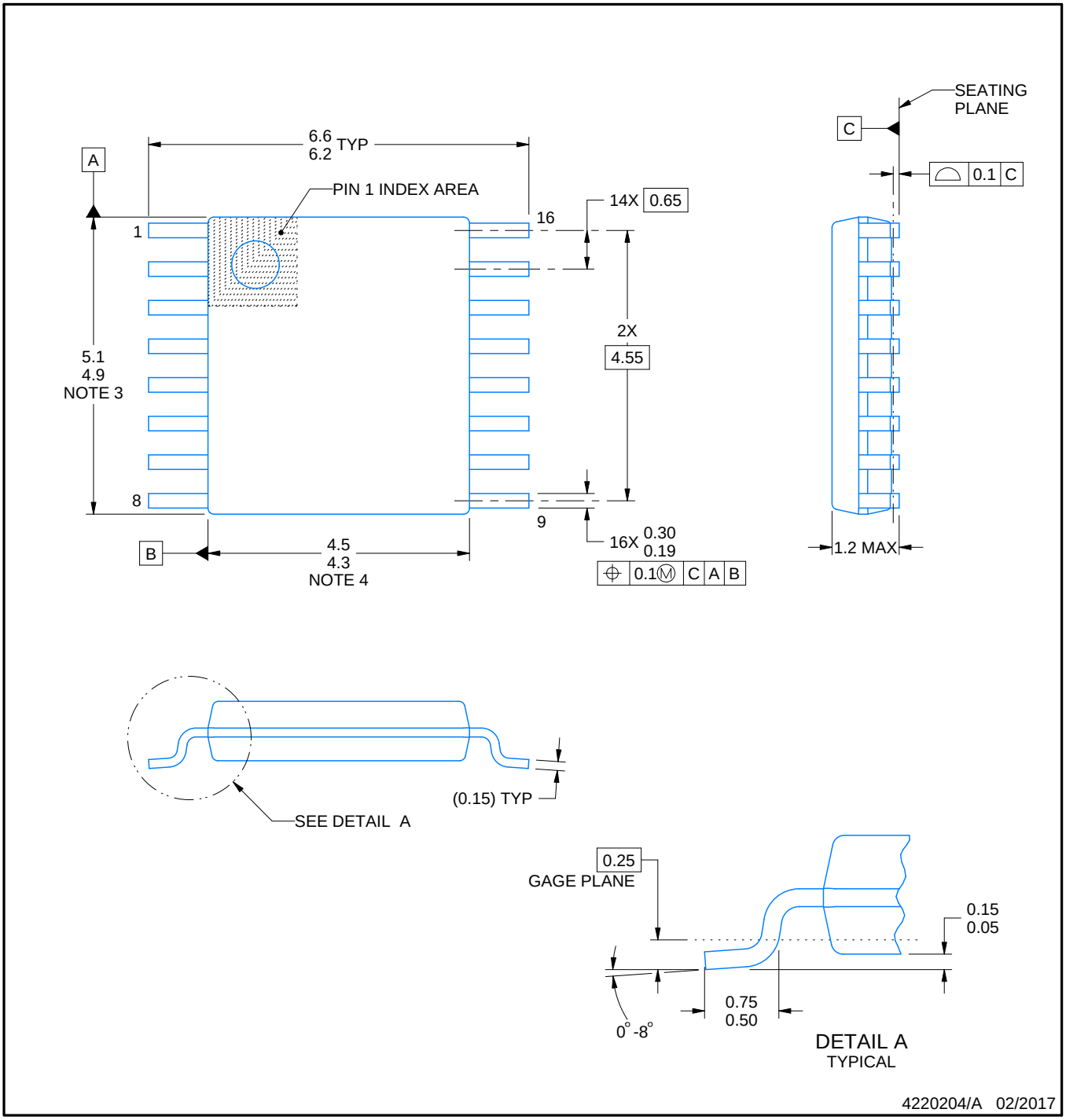
PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

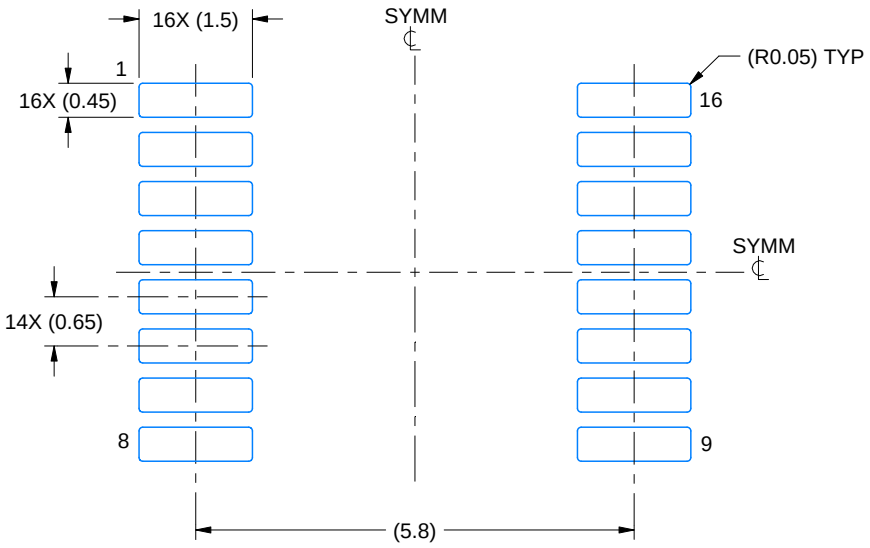
SMALL OUTLINE PACKAGE





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



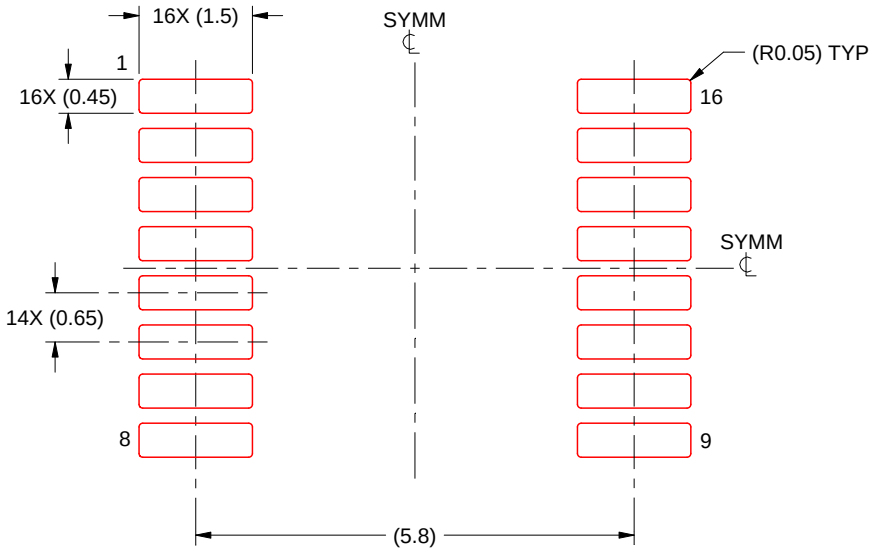
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

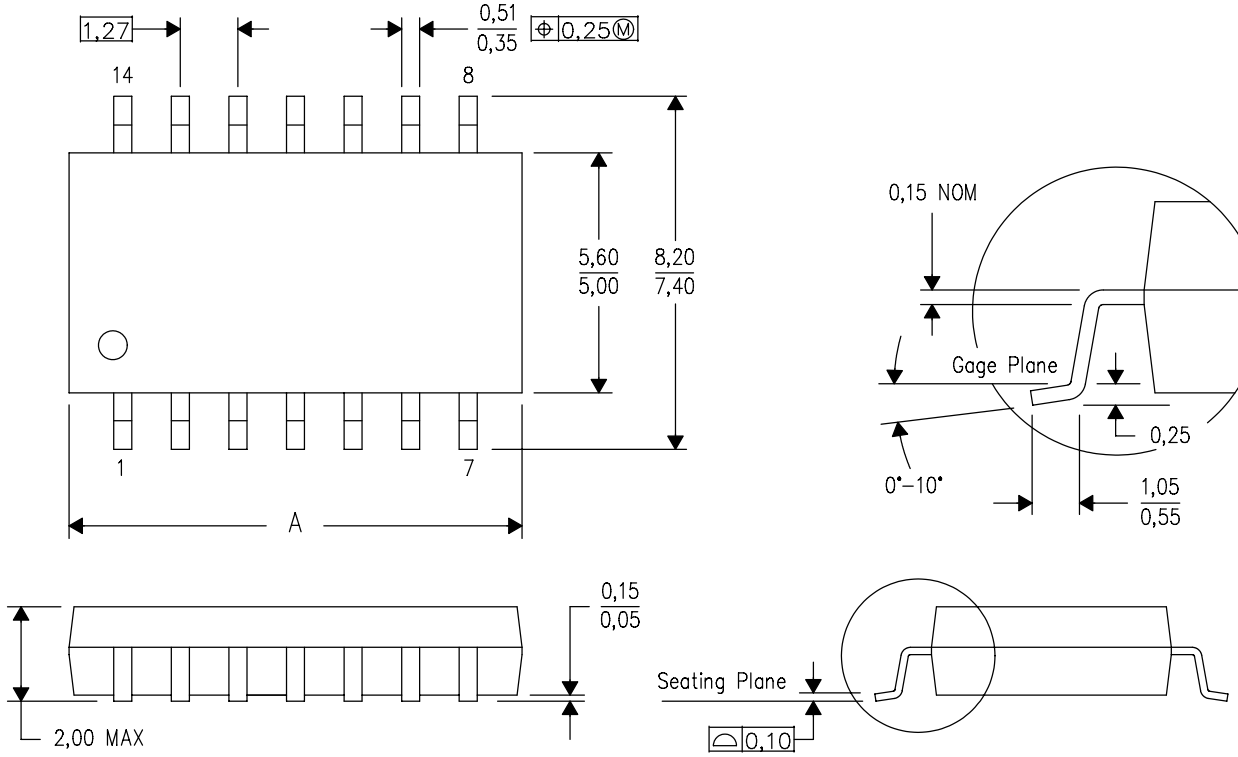
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

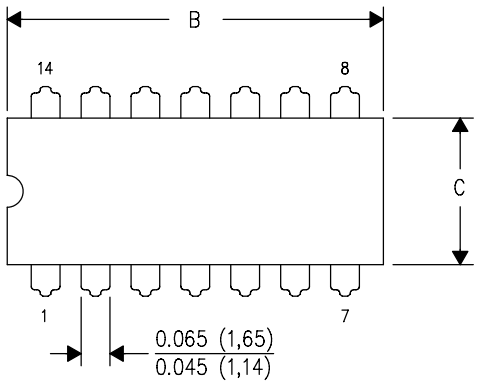
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

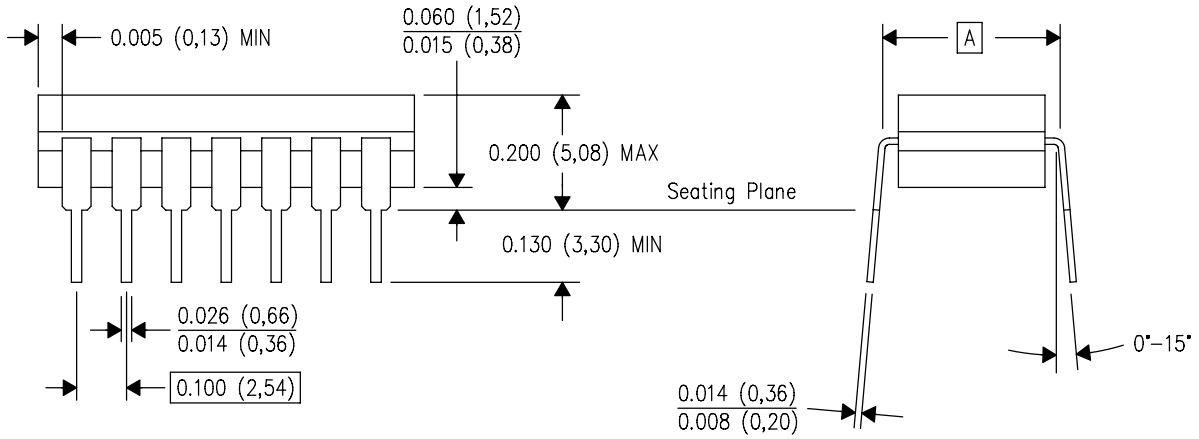
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



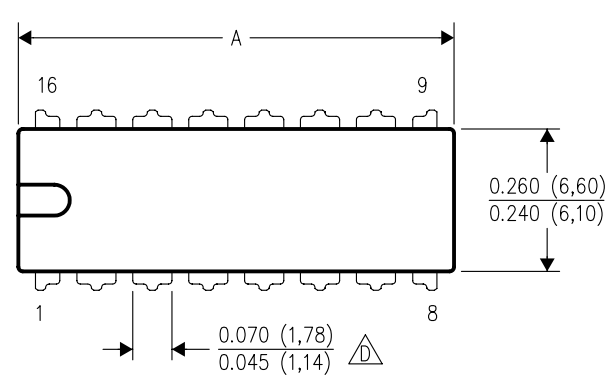
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

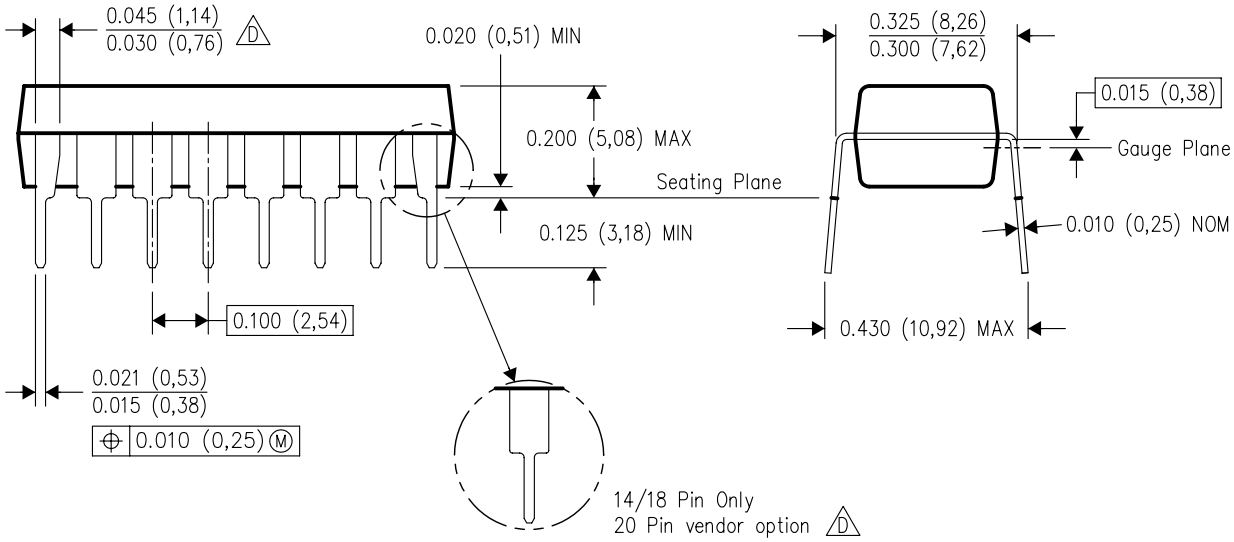
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

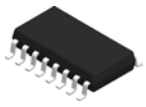


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

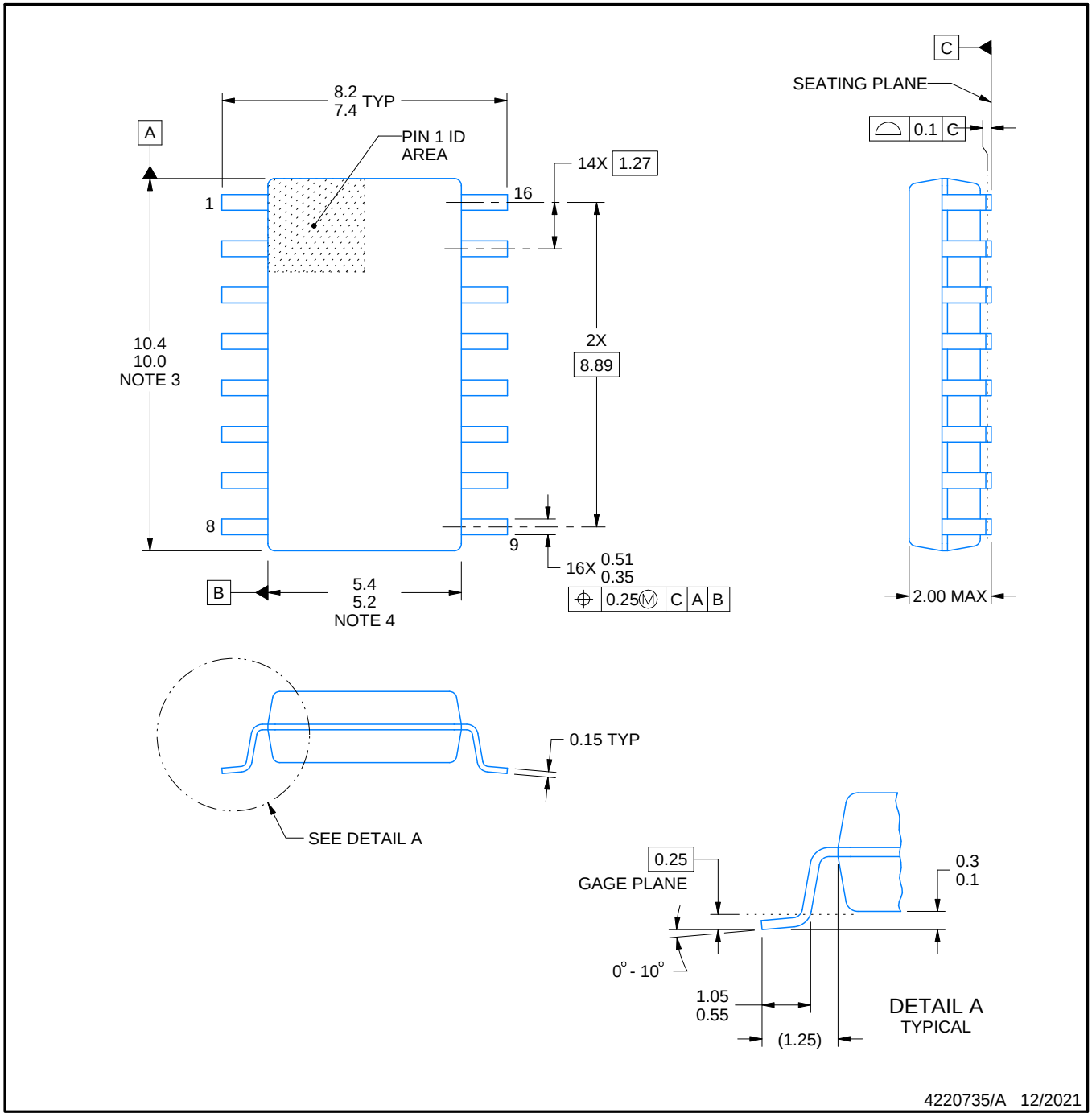


PACKAGE OUTLINE

NS0016A

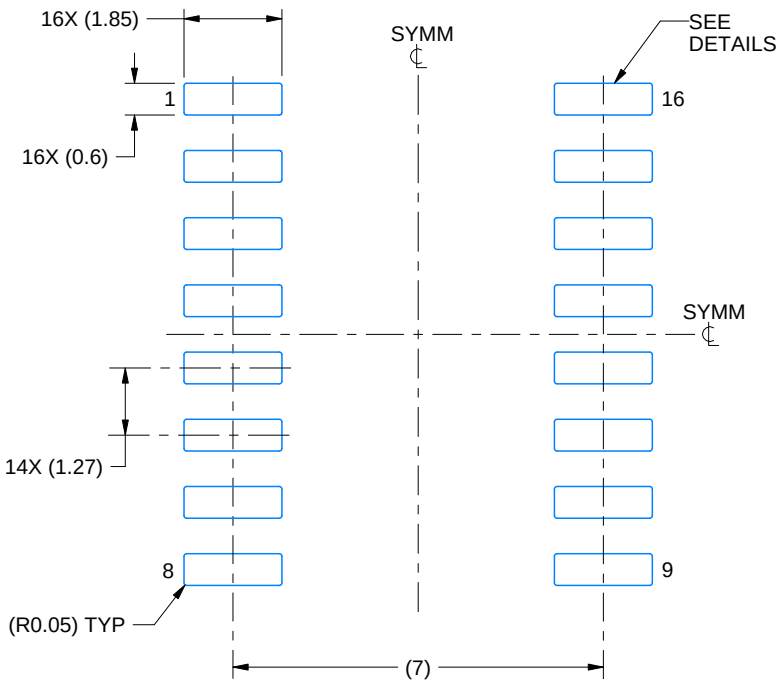
SOP - 2.00 mm max height

SOP

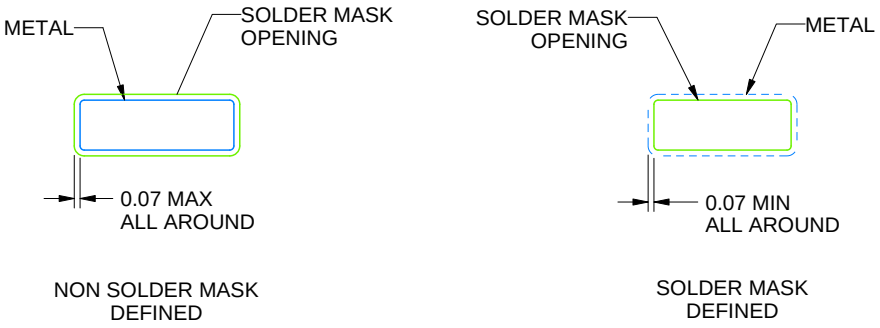


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

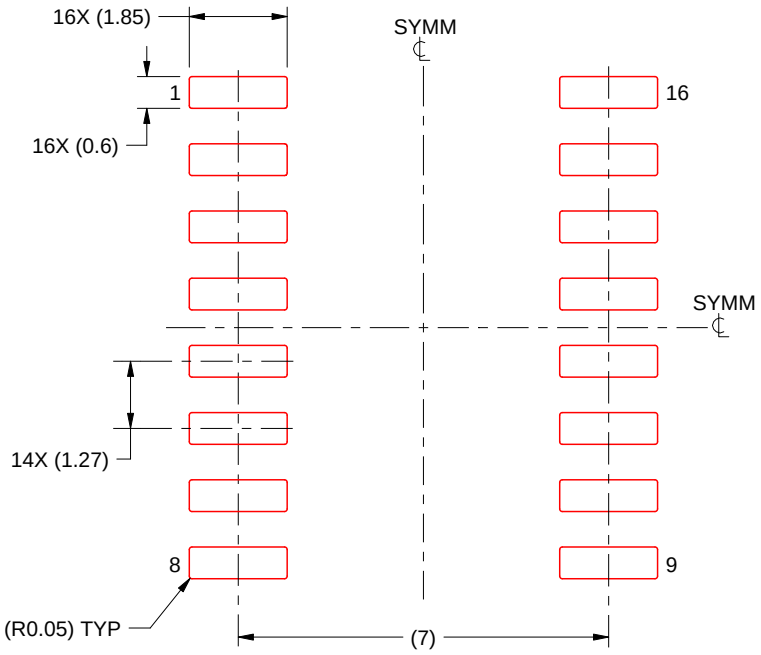


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

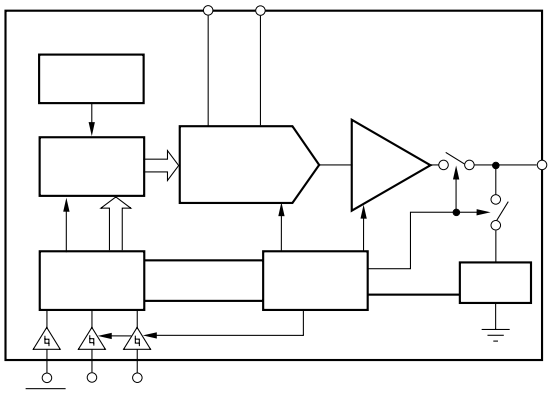
These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265



ABSOLUTE MAXIMUM RATINGS(1)

V_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
V_{OUT} to GND	–0.3V to $+V_{DD}$ + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
SOT23 Package:	
Power Dissipation	(T_J max — T_A)/ $_{JA}$
$_{JA}$ Thermal Impedance	240°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C
MSOP Package:	
Power Dissipation	(T_J max — T_A)/ $_{JA}$
$_{JA}$ Thermal Impedance	206°C/W
$_{JC}$ Thermal Impedance	44°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

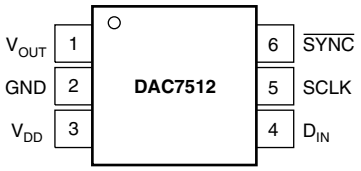
PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA, QUANTITY
DAC7512E	±8	±1	MSOP-8	DGK	–40°C to +105°C	D12E	DAC7512E/250	Tape and Reel, 250
"	"	"	"	"	"	"	DAC7512E/2K5	Tape and Reel, 2500
DAC7512N	±8	±1	SOT23-6	DBV	–40°C to +105°C	D12N	DAC7512N/250	Tape and Reel, 250
"	"	"	"	"	"	"	DAC7512N/3K	Tape and Reel, 3000

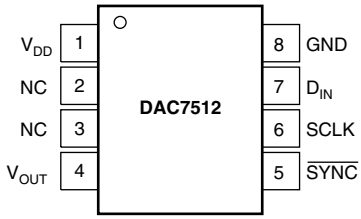
NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC7512E/2K5" will get a single 2500-piece Tape and Reel.

PIN CONFIGURATIONS

Top View SOT23-6



MSOP-8

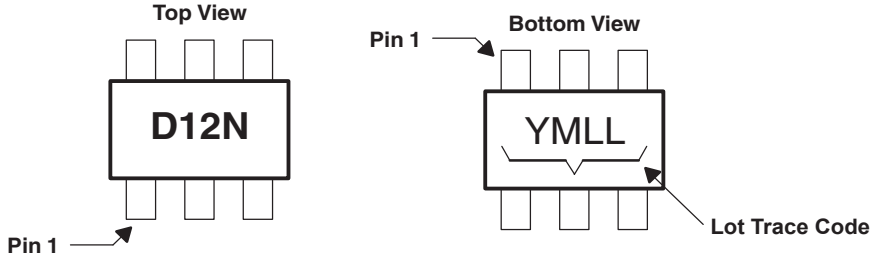


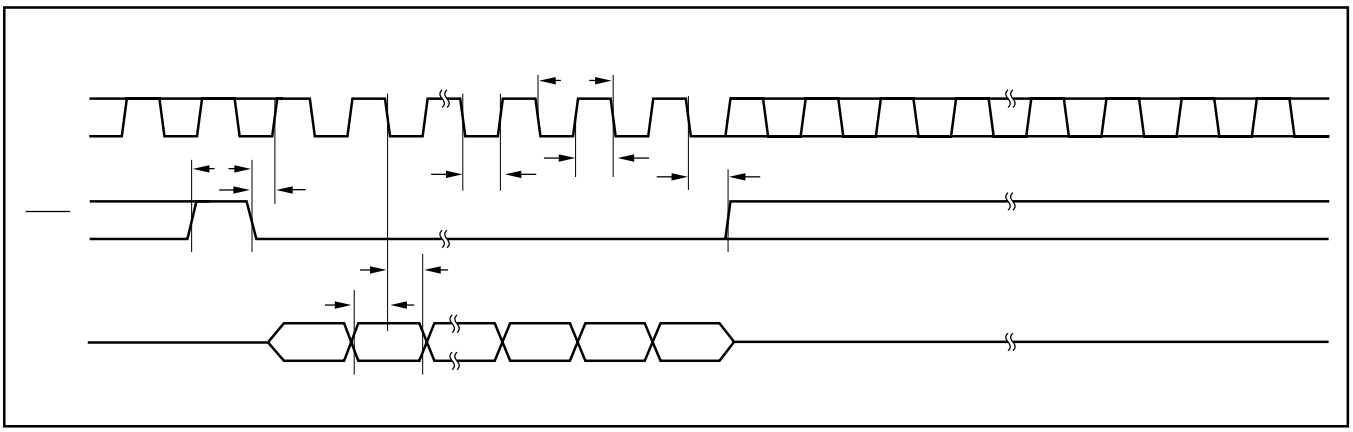
NC = No Internal Connection

PIN DESCRIPTION (SOT23-6)

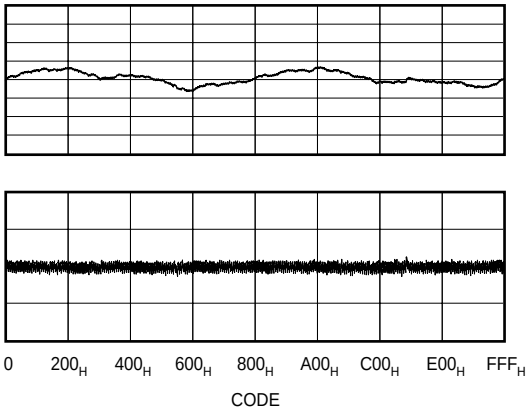
PIN	NAME	DESCRIPTION
1	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
2	GND	Ground reference point for all circuitry on the part.
3	V_{DD}	Power Supply Input, +2.7V to 5.5V.
4	D_{IN}	Serial Data Input. Data is clocked into the 16-bit input shift register on the falling edge of the serial clock input.
5	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz.
6	$\overline{SYNC}$	Level triggered control input (active LOW). This is the frame sychronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC7512.

DAC7512N LOT TRACE LOCATION

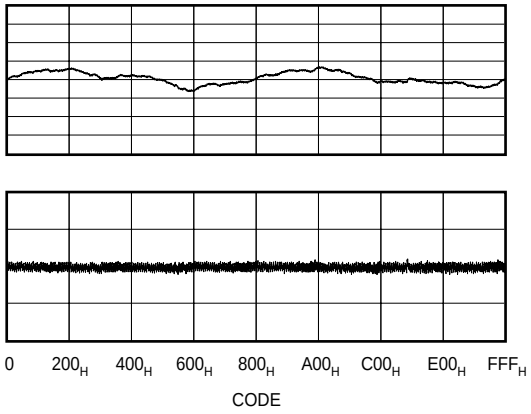




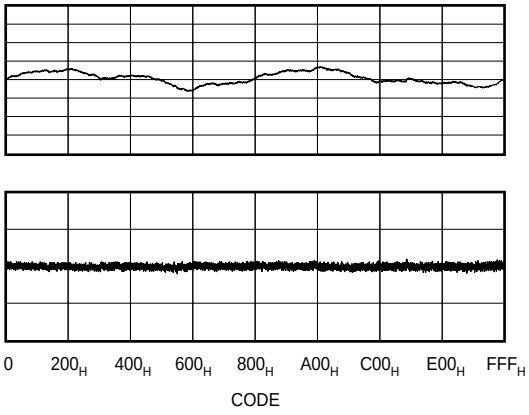
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(Ð40 C)



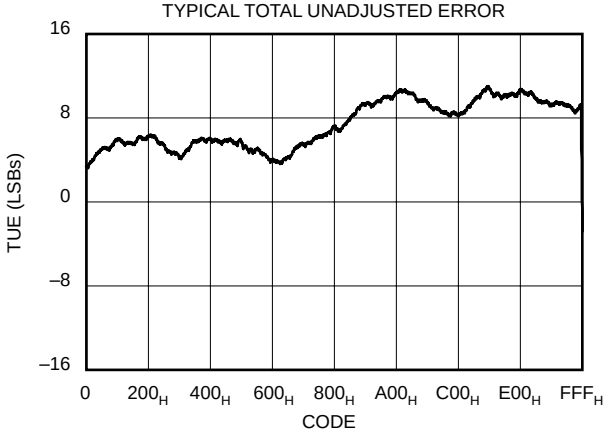
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25 C)



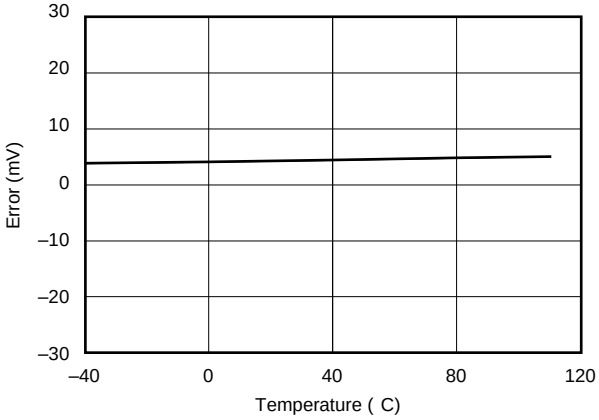
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+105 C)



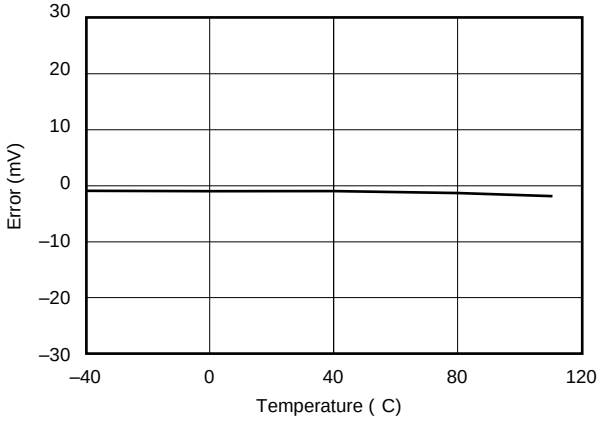
TYPICAL TOTAL UNADJUSTED ERROR

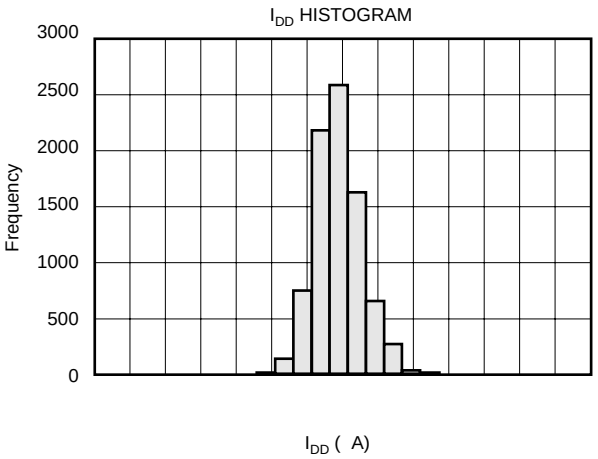


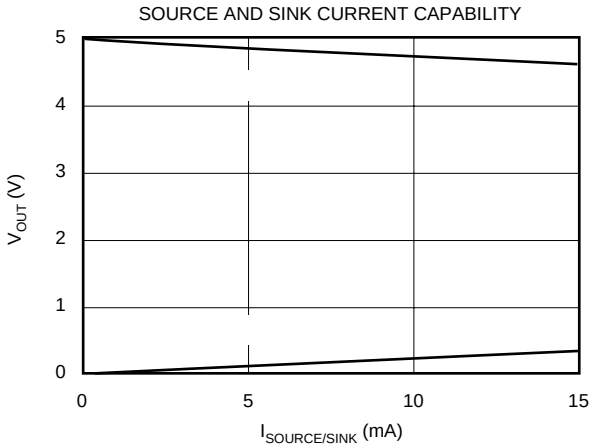
ZERO-SCALE ERROR vs TEMPERATURE

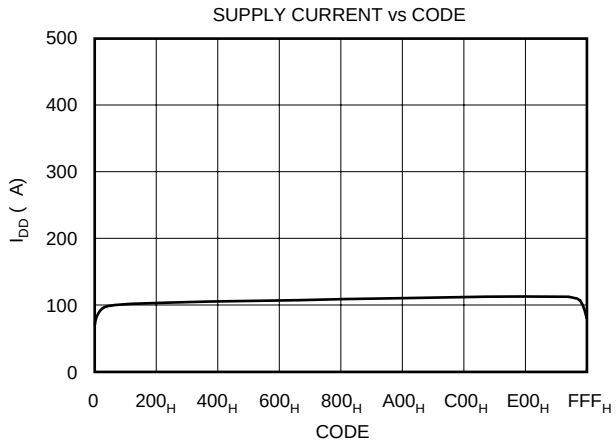


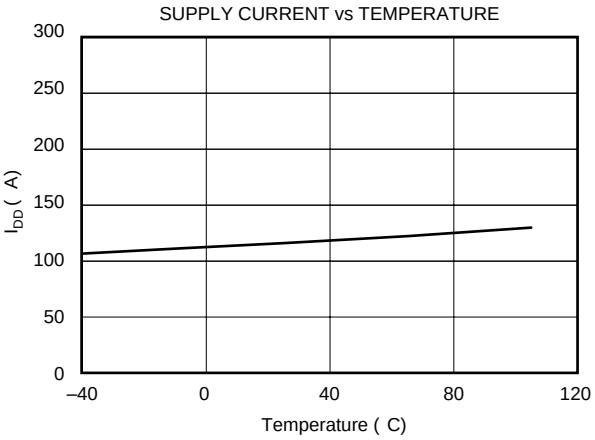
FULL-SCALE ERROR vs TEMPERATURE

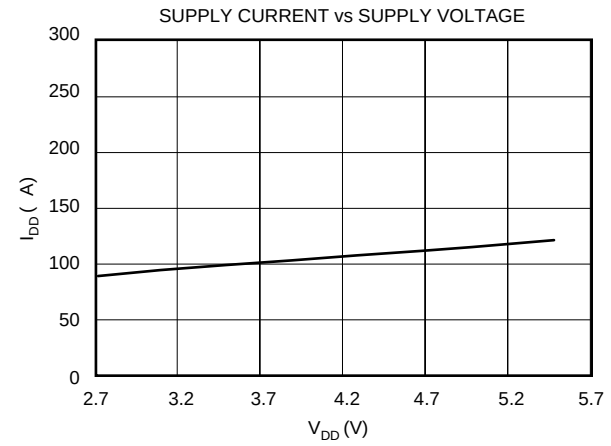


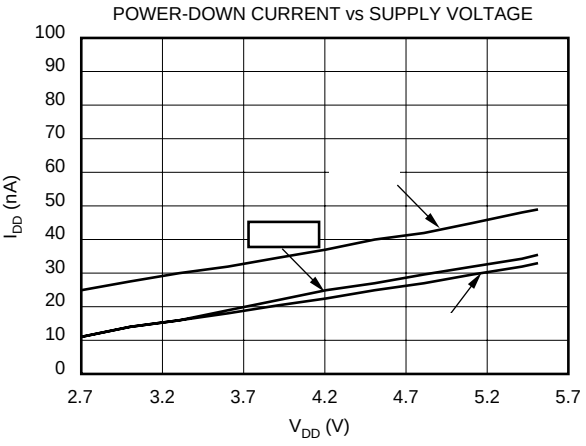

I_{DD} HISTOGRAM
Frequency
3000
2500
2000
1500
1000
500
0
I_{DD} (A)


SOURCE AND SINK CURRENT CAPABILITY
V_{OUT} (V)
5
4
3
2
1
0
0
5
10
15
$I_{SOURCE/SINK}$ (mA)

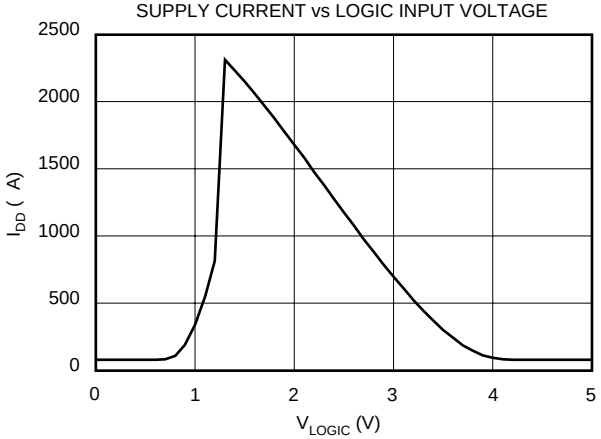

SUPPLY CURRENT vs CODE
I_{DD} (A)
500
400
300
200
100
0
0
200_H
400_H
600_H
800_H
$A00_H$
$C00_H$
$E00_H$
FFF_H
CODE


SUPPLY CURRENT vs TEMPERATURE
I_{DD} (A)
300
250
200
150
100
50
0
–40
0
40
80
120
Temperature (C)

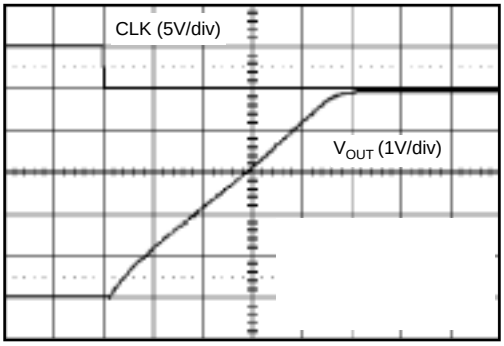

SUPPLY CURRENT vs SUPPLY VOLTAGE
I_{DD} (A)
300
250
200
150
100
50
0
2.7
3.2
3.7
4.2
4.7
5.2
5.7
V_{DD} (V)


POWER-DOWN CURRENT vs SUPPLY VOLTAGE
I_{DD} (nA)
100
90
80
70
60
50
40
30
20
10
0
2.7
3.2
3.7
4.2
4.7
5.2
5.7
V_{DD} (V)

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

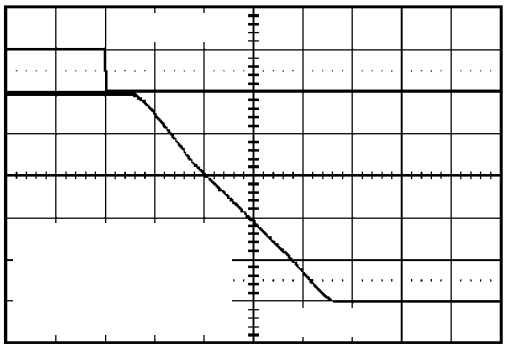


FULL-SCALE SETTLING TIME



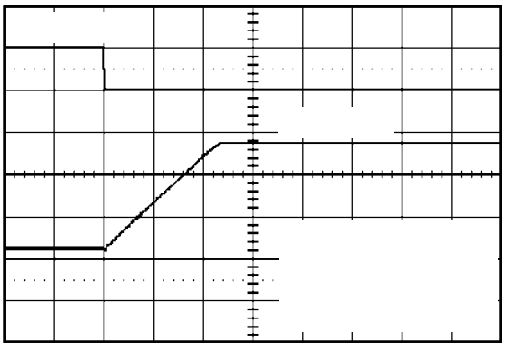
Time (1 s/div)

FULL-SCALE SETTLING TIME



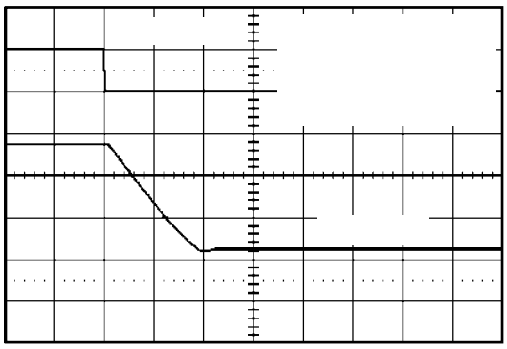
Time (1 s/div)

HALF-SCALE SETTLING TIME



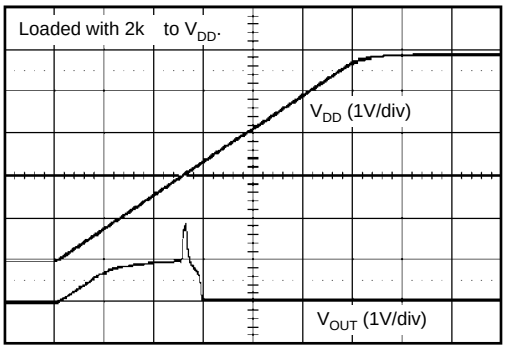
Time (1 s/div)

HALF-SCALE SETTLING TIME



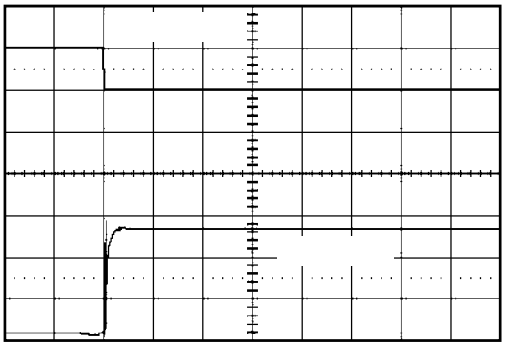
Time (1 s/div)

POWER-ON RESET TO 0V



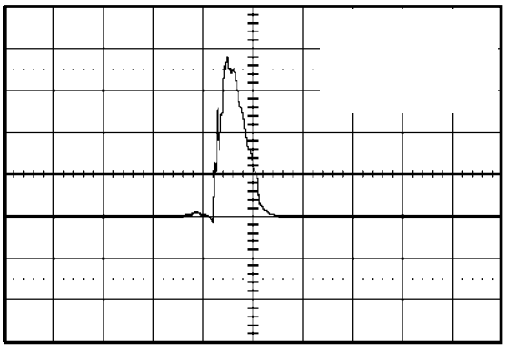
Time (20 s/div)

EXITING POWER-DOWN
(800_H Loaded)



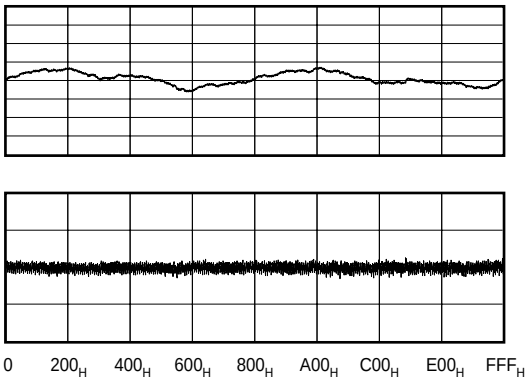
Time (5 s/div)

CODE CHANGE GLITCH

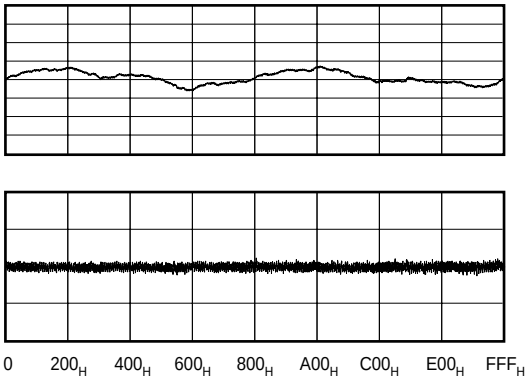


Time (0.5 s/div)

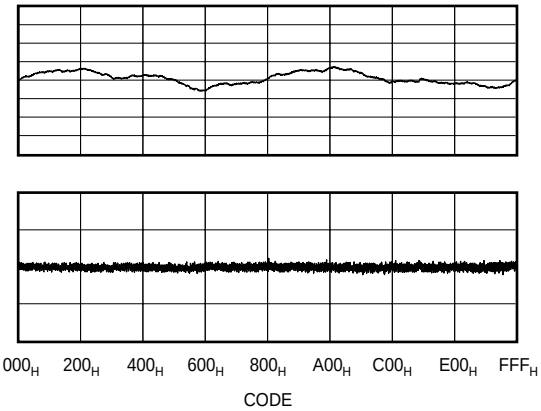
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(Ð40 C)



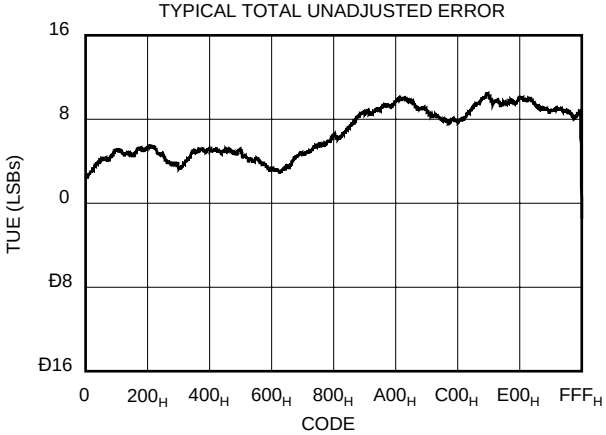
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25 C)



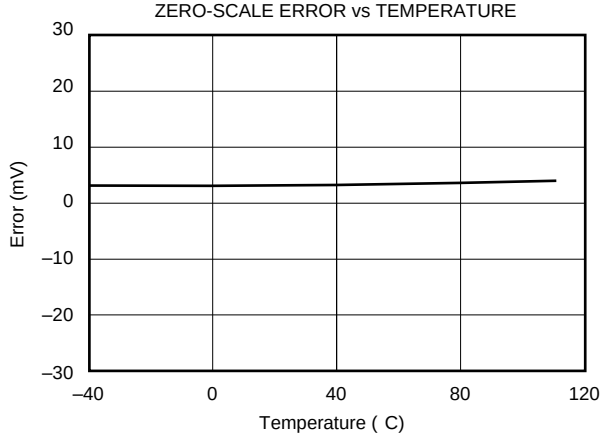
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+105 C)



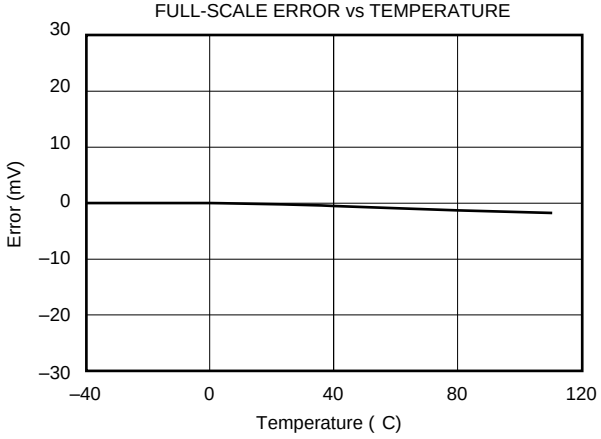
TYPICAL TOTAL UNADJUSTED ERROR



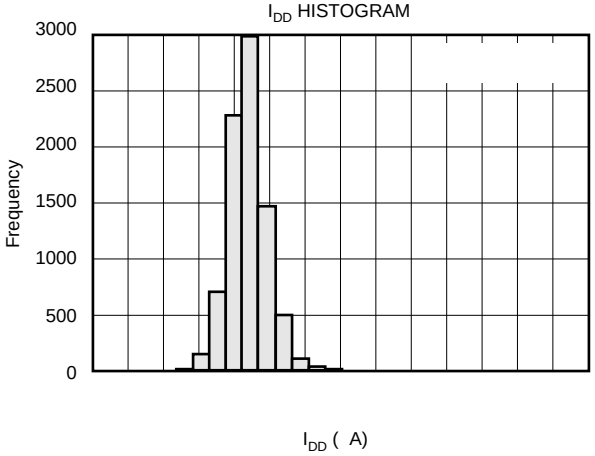
ZERO-SCALE ERROR vs TEMPERATURE



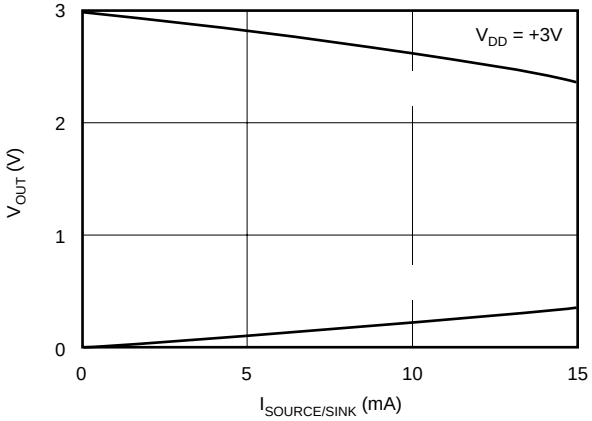
FULL-SCALE ERROR vs TEMPERATURE



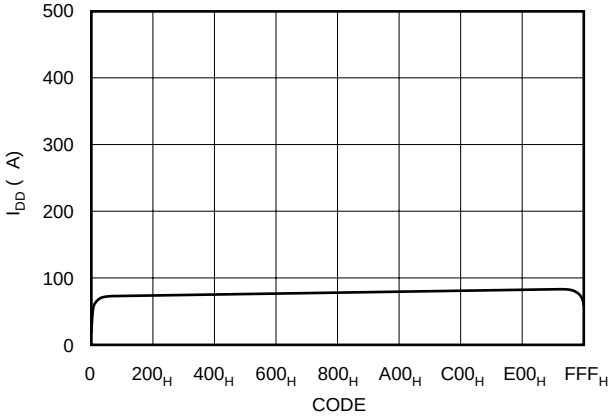
I_{DD} HISTOGRAM



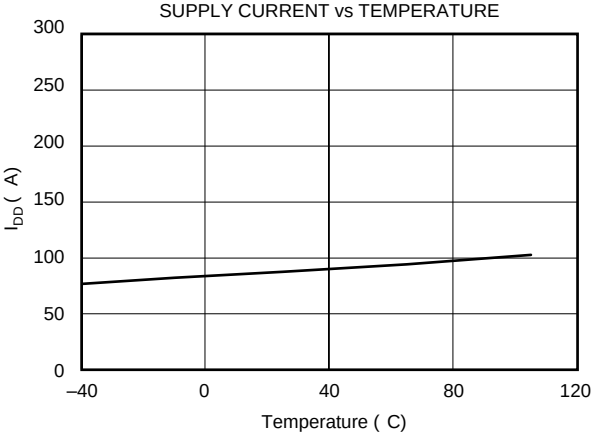
SOURCE AND SINK CURRENT CAPABILITY



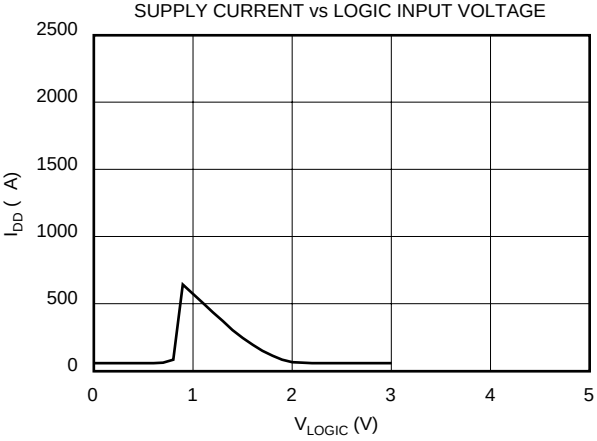
SUPPLY CURRENT vs CODE



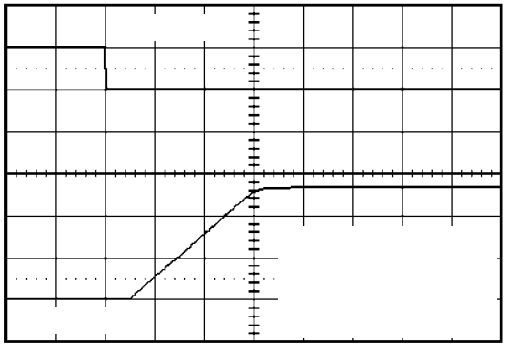
SUPPLY CURRENT vs TEMPERATURE



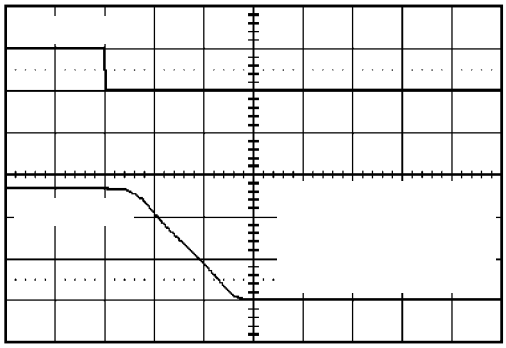
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



FULL-SCALE SETTLING TIME

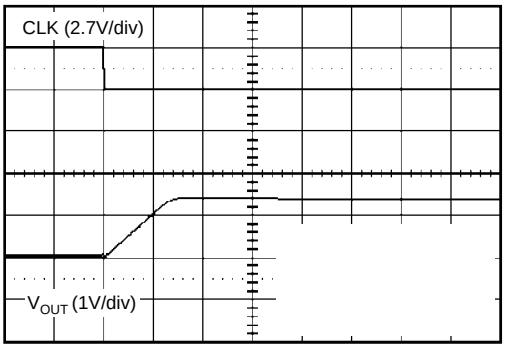


FULL-SCALE SETTLING TIME



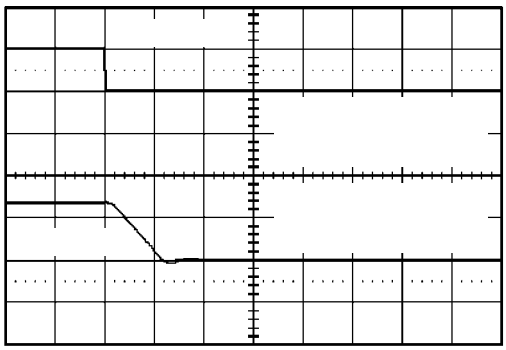
Time (1 s/div)

HALF-SCALE SETTLING TIME

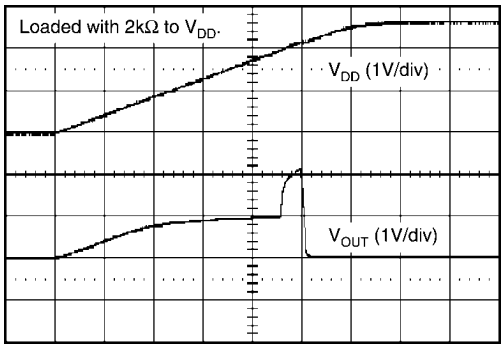


Time (1 s/div)

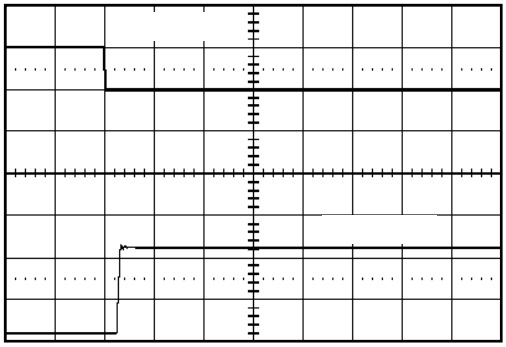
HALF-SCALE SETTLING TIME



Time (1 s/div)

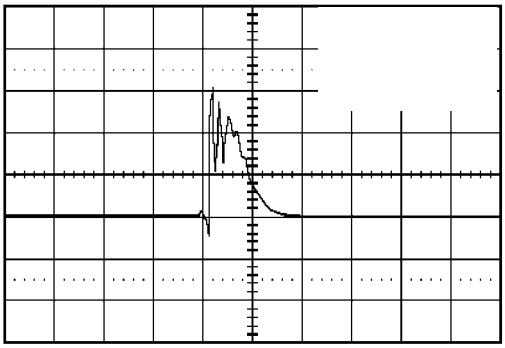


EXITING POWER-DOWN
(800_H Loaded)

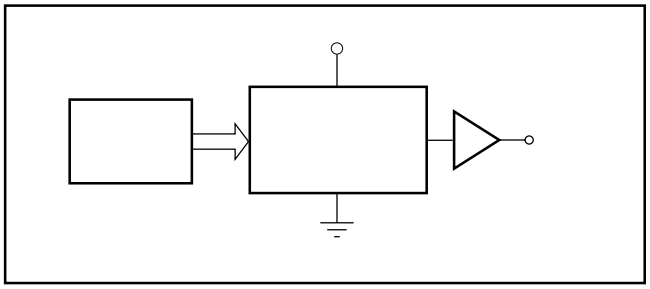


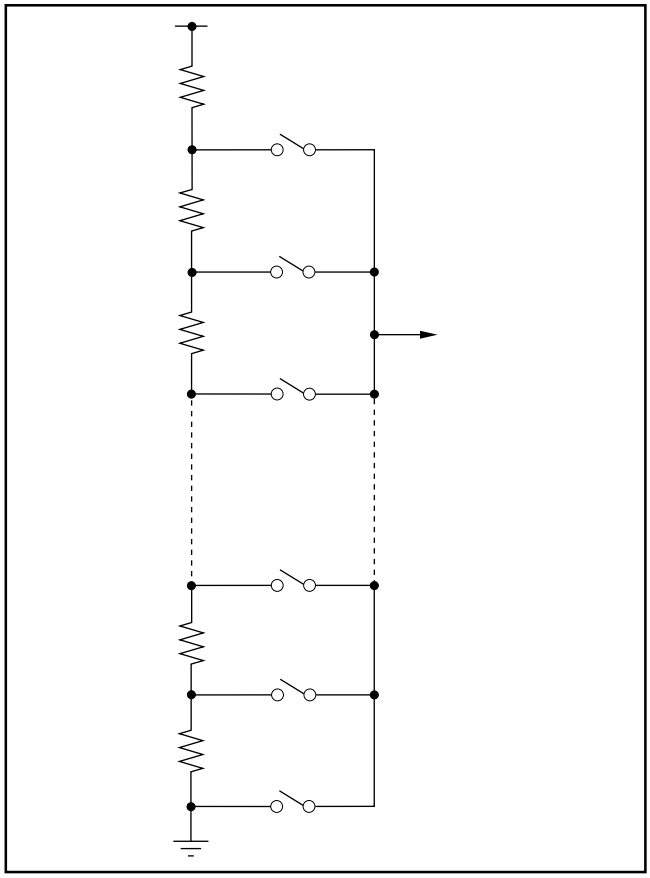
Time (5 s/div)

CODE CHANGE GLITCH

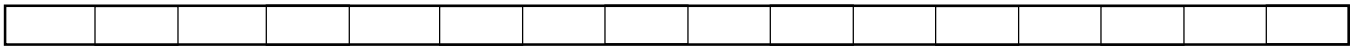


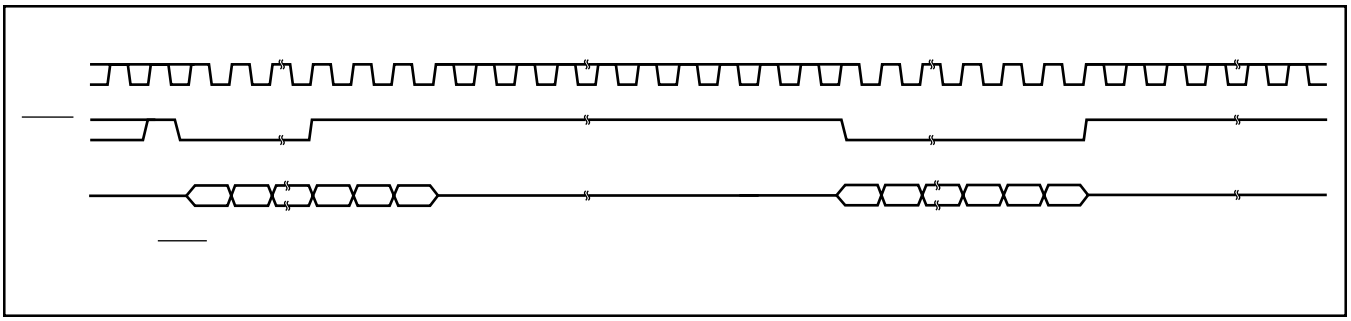
Time (0.5 s/div)

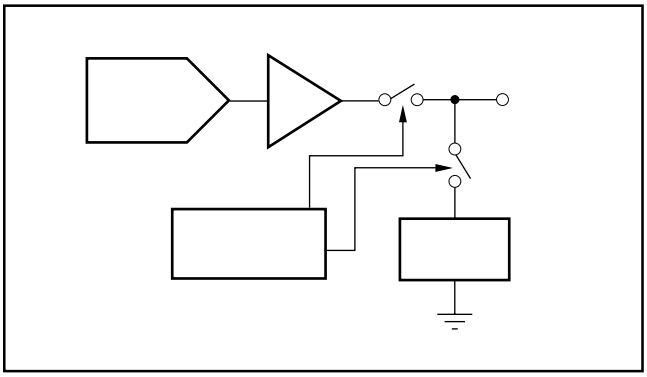


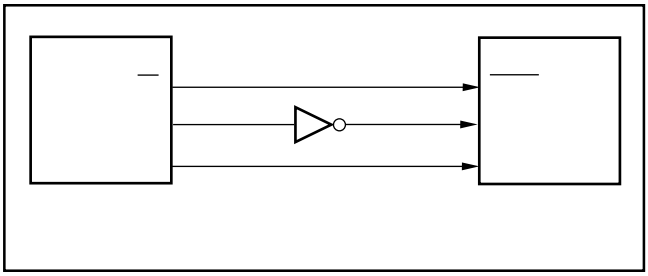


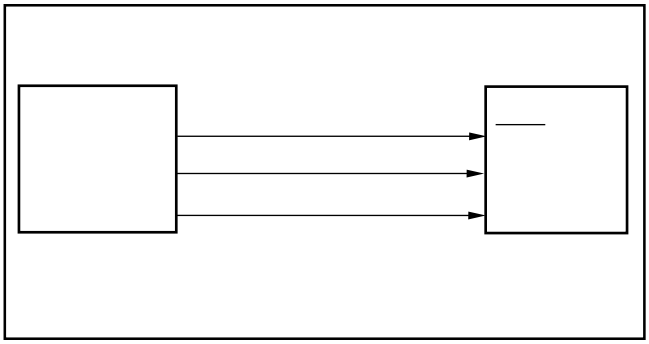
$$V_{OUT} \quad V_{DD} \quad \frac{D}{4096}$$

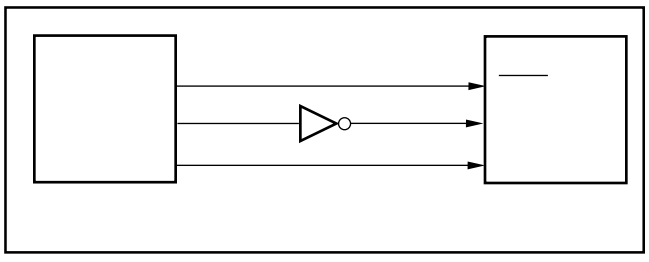


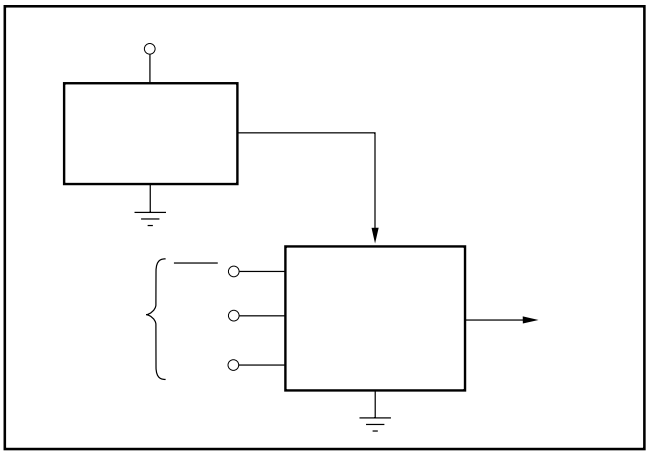






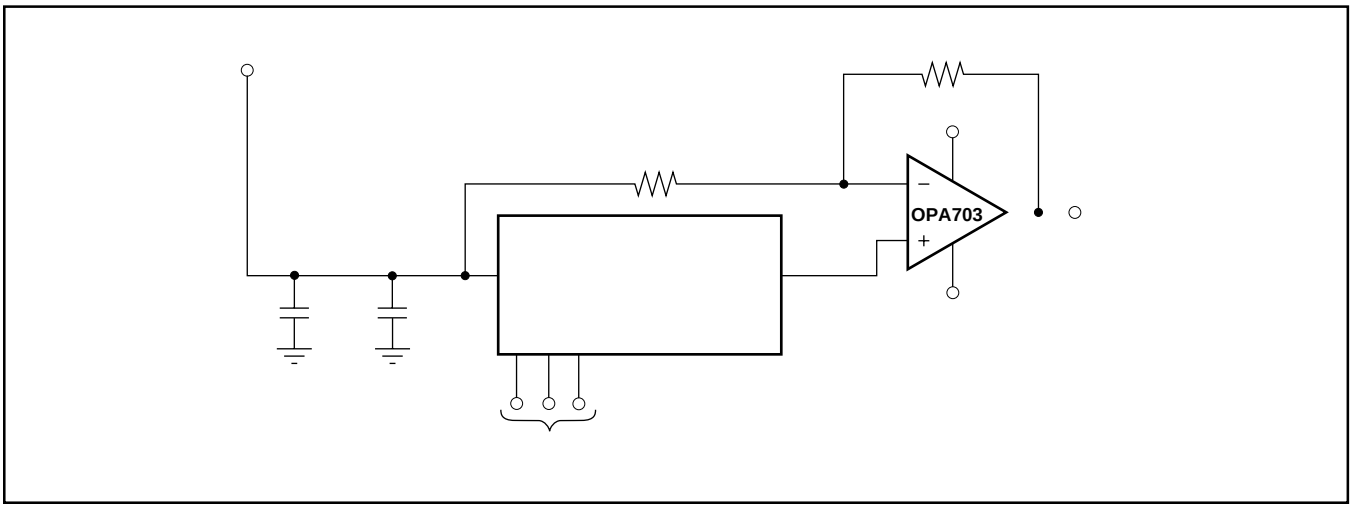


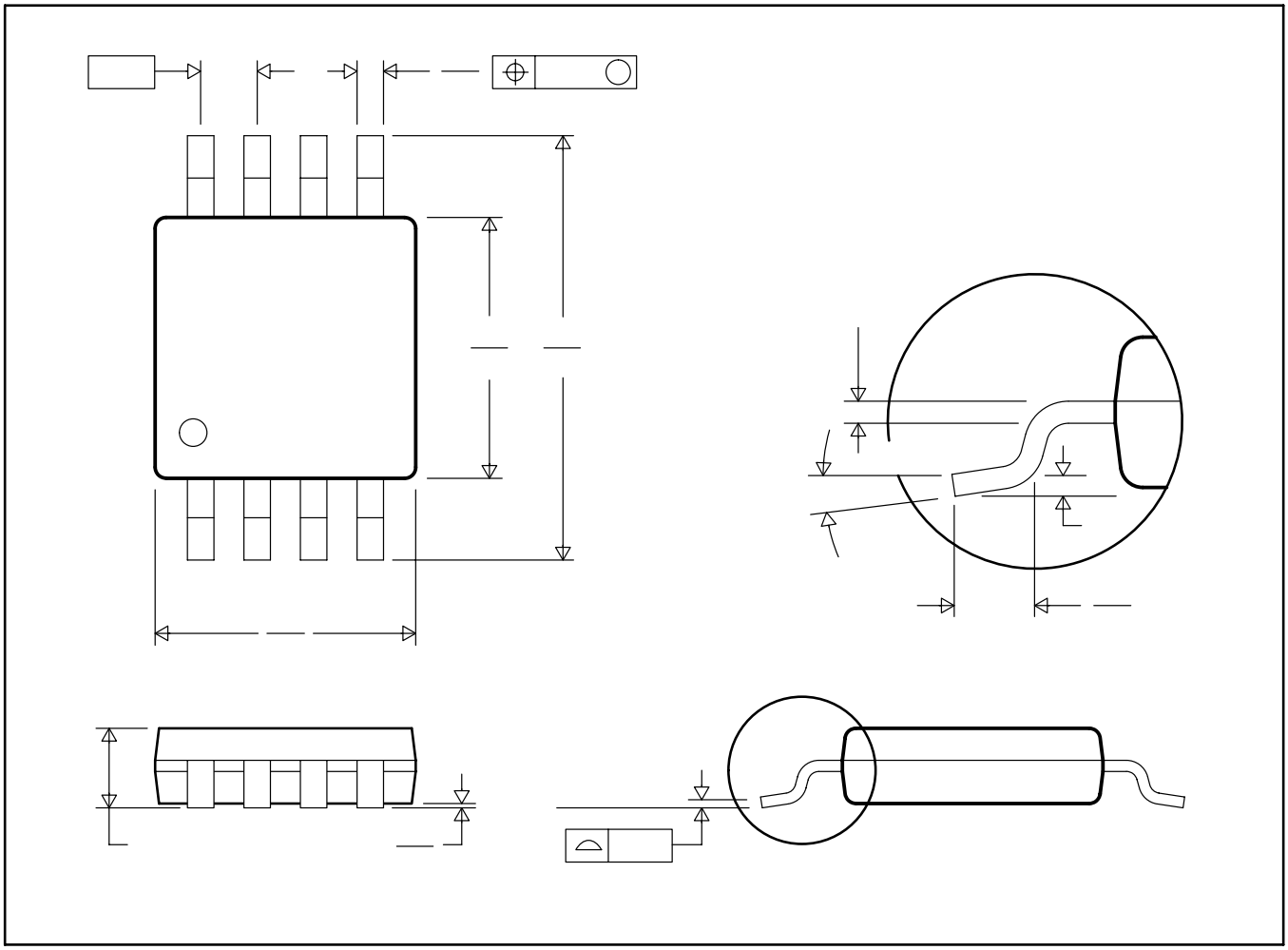


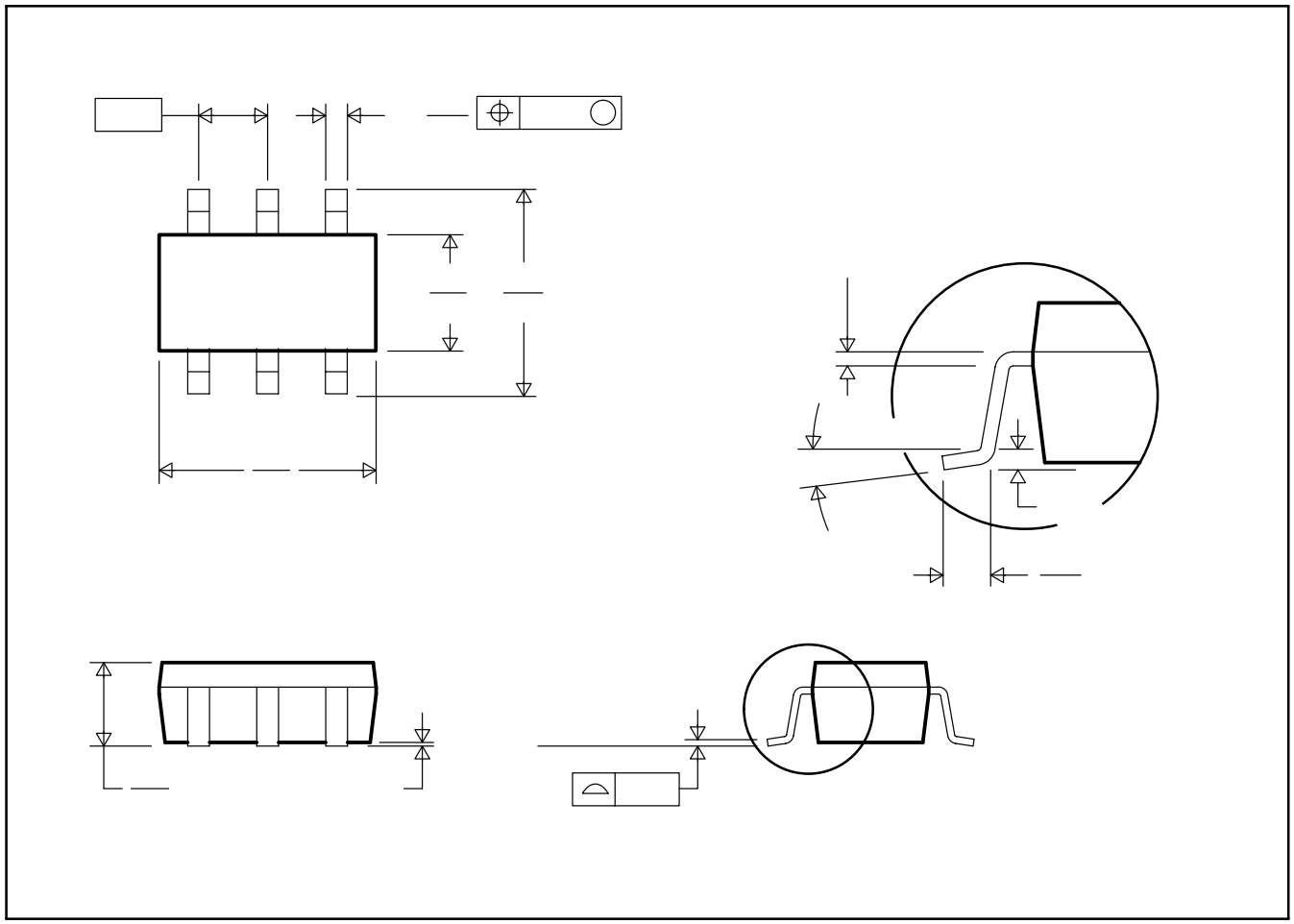


$$V_O \quad V \quad \frac{D}{4096} \quad \frac{R_1 \quad R_2}{R_1} \quad - V_{DD} \quad \frac{R_2}{R_1}$$

$$V_O \quad \frac{10 \quad D}{4096} \quad - 5V$$







PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7512E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512E/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512E/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512N/250	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/250G4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/3K	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/3KG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

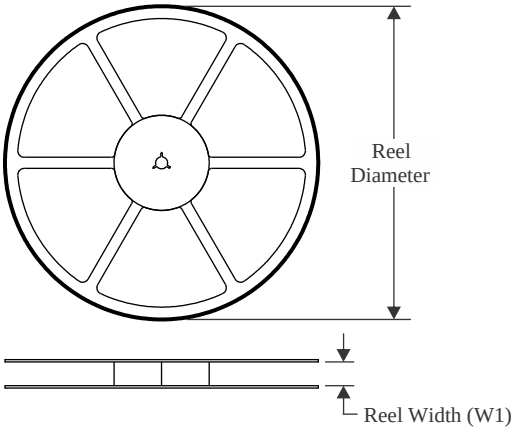
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

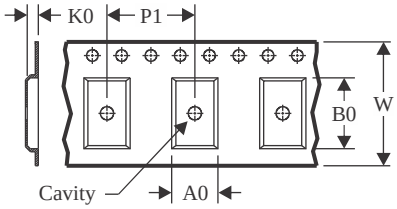
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

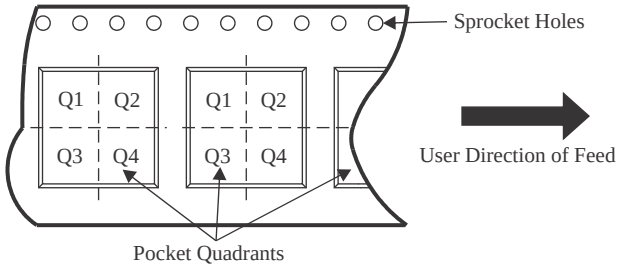


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

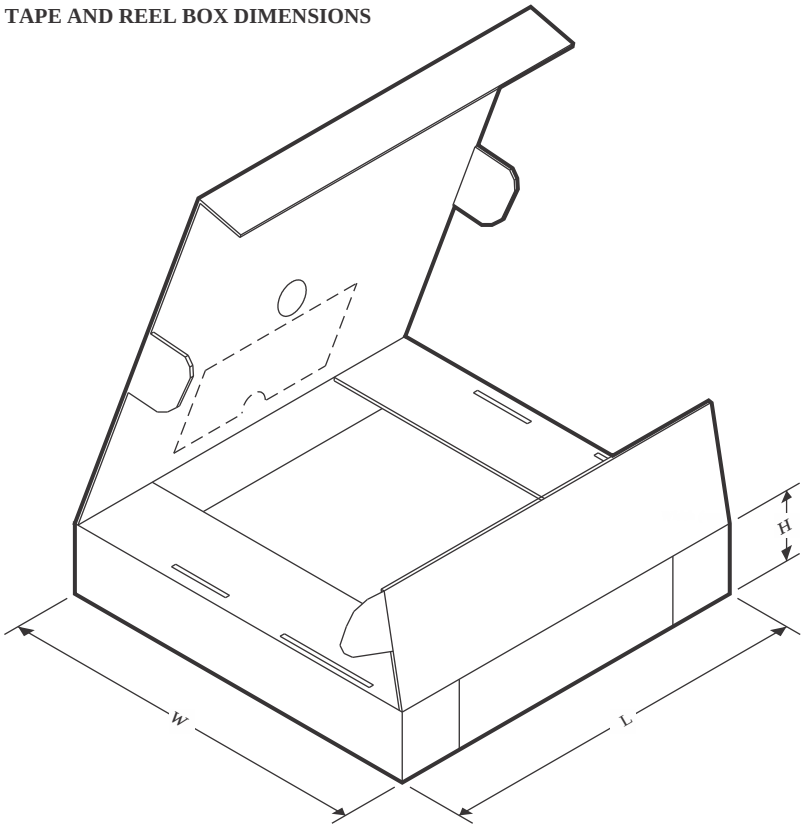
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7512N/250	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
DAC7512N/3K	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

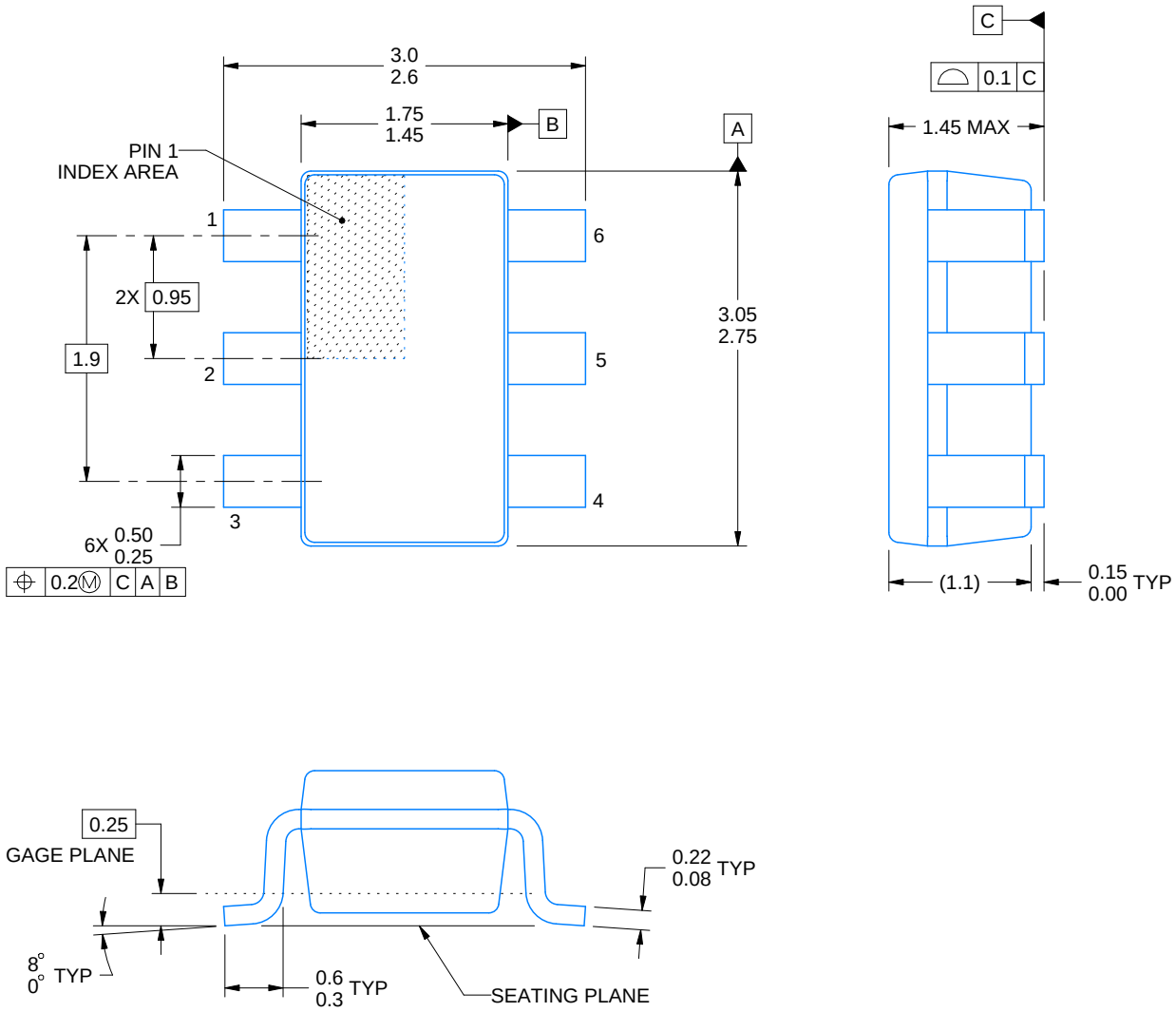
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7512N/250	SOT-23	DBV	6	250	180.0	180.0	18.0
DAC7512N/3K	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

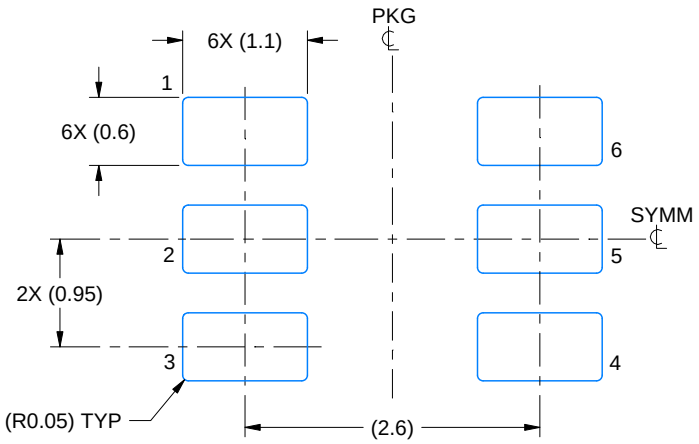
SMALL OUTLINE TRANSISTOR



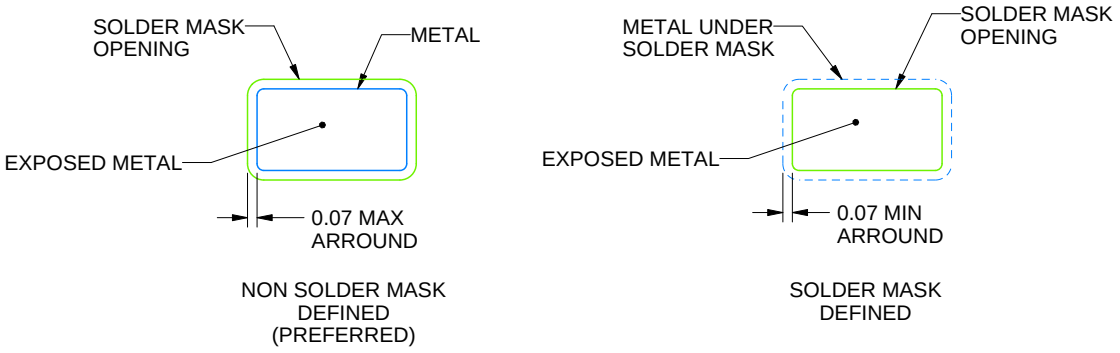
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

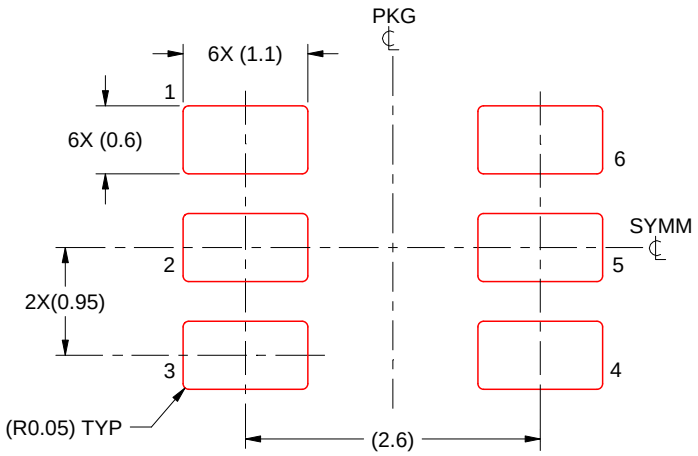


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



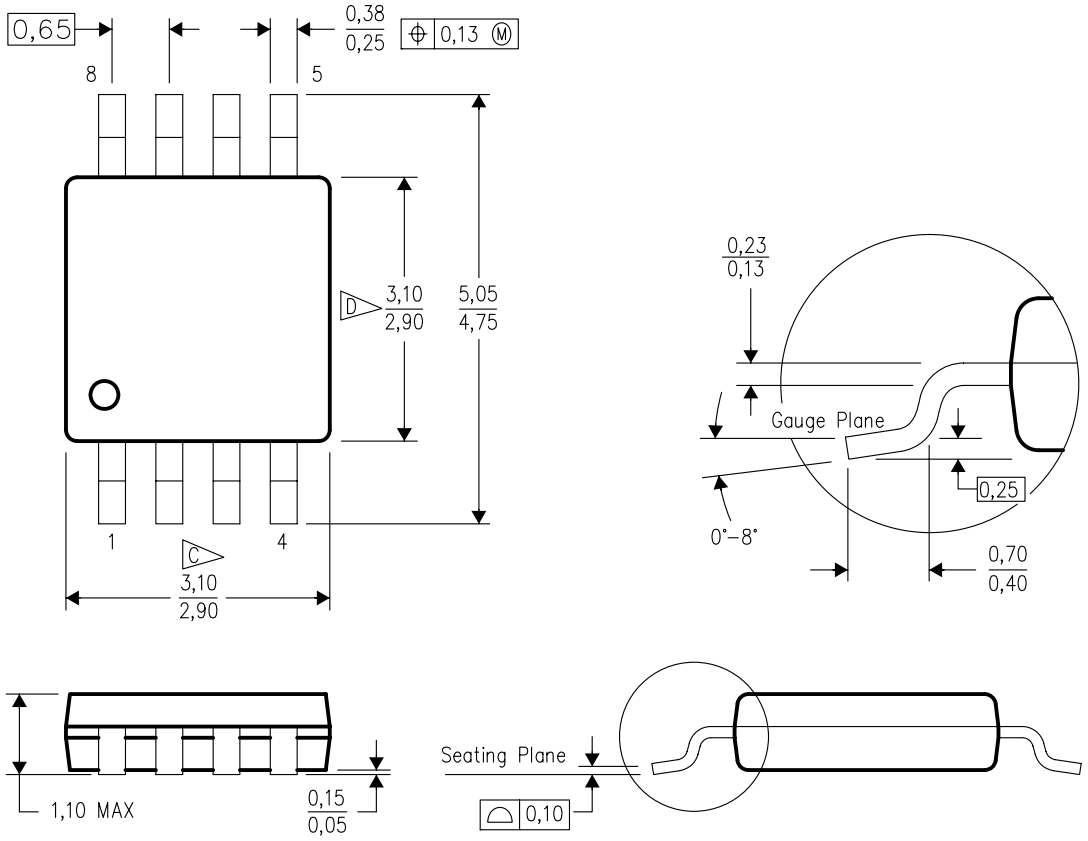
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

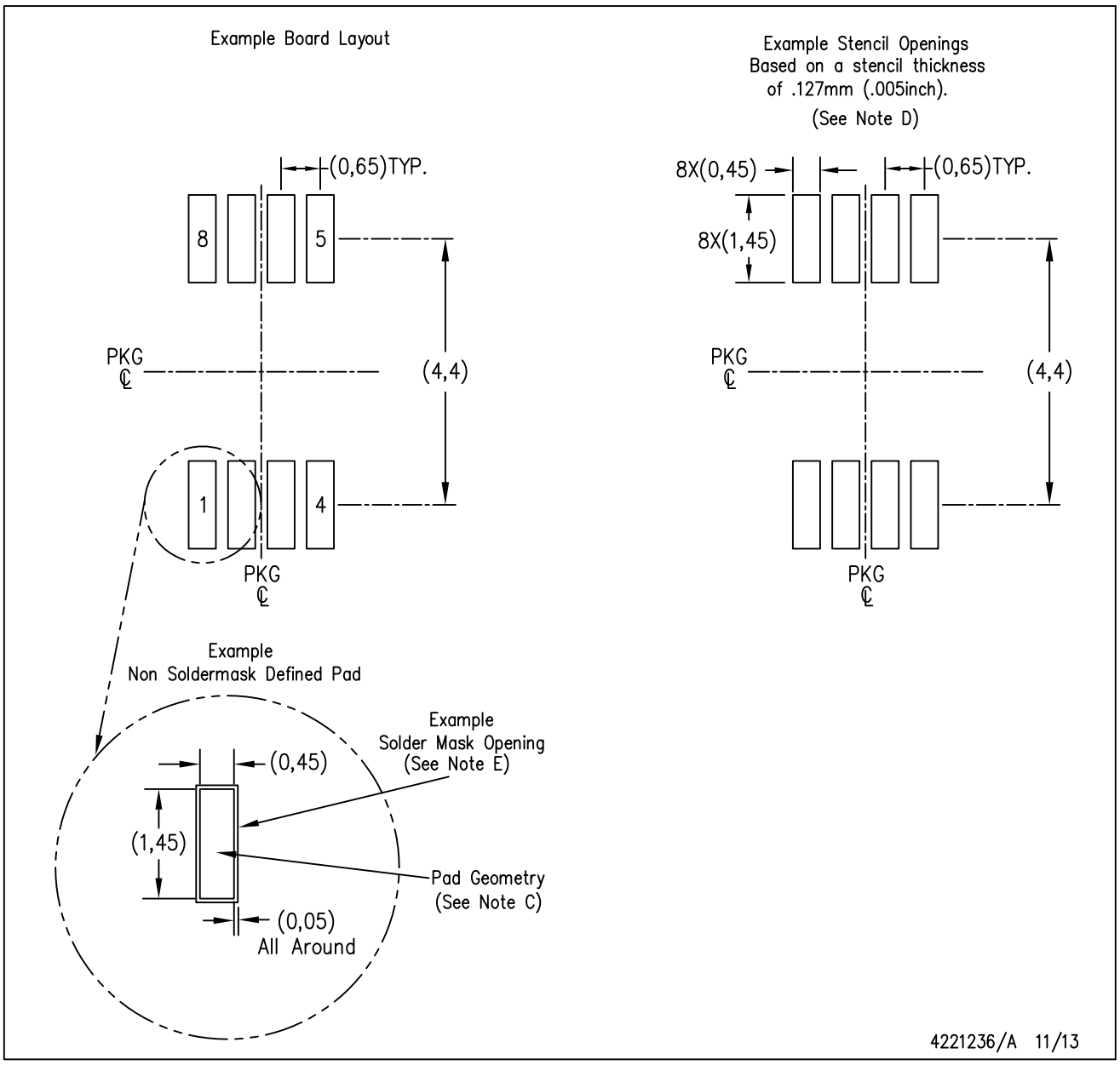
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS

DAC7562T, DAC7563T, DAC8162T
DAC8163T, DAC8562T, DAC8563T

SLASE61A – SEPTEMBER 2015 – REVISED OCTOBER 2015

DACxx6xT Dual 16-, 14-, 12-Bit, Low-Power, Voltage-Output DACs With 2.5-V, 4-PPM/°C Internal Reference, and 5-V TTL I/O

1 Features

- Relative Accuracy: 4 LSB INL at 16 Bits
- Low Glitch Impulse: 0.1 nV-s
- Bidirectional Reference Pin: Input or 2.5-V Output
  - 4-ppm/°C Temperature Drift (Typ)
- Power-On Reset to Zero Scale or Mid-Scale
- Low-Power: 4 mW at 5-V AVDD
- Wide Power-Supply Range: 2.7 V to 5.5 V
- 50-MHz SPI With Schmitt-Triggered Inputs
- LDAC and CLR Functions
- Output Buffer With Rail-to-Rail Operation
- Pin-to-Pin Compatible With DAC8562 Family
- 5-V TTL I/O Enabled
- Packages: WSON-10 (3 mm × 3 mm), VSSOP-10
- Temperature Range: –40°C to 125°C

2 Applications

- Portable Instrumentation
- PLC Analog Output Module
- Bipolar Outputs (Section 9.2.2)
- Closed-Loop Servo Control
- Voltage Controlled Oscillator Tuning
- Data Acquisition Systems
- Programmable Gain and Offset Adjustment

3 Description

The DAC856xT, DAC816xT, and DAC756xT devices are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 4-ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN}/V_{REFOUT} pin.

These devices are monotonic, providing excellent linearity and minimizing undesired code-to-code transient voltages (glitch). They use a versatile three-wire serial interface that operates at clock rates up to 50 MHz. The interface is compatible with standard SPI™, QSPI™, Microwire, and digital signal processor (DSP) interfaces. The DACxx62T devices incorporate a power-on-reset circuit that ensures the DAC output powers up and remains at zero scale until a valid code is written to the device, whereas the DACxx63T devices similarly power up at mid-scale. These devices contain a power-down feature that reduces current consumption to typically 550 nA at 5 V. The low power consumption, internal reference, and small footprint make these devices ideal for portable, battery-operated equipment.

The DACxx62T devices are drop-in and function-compatible with each other, as are the DACxx63T devices. The entire family is available in VSSOP-10 and WSON-10 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8562T	VSSOP (10), WSON (10)	3.00 mm × 3.00 mm
DAC8162T		
DAC7562T		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

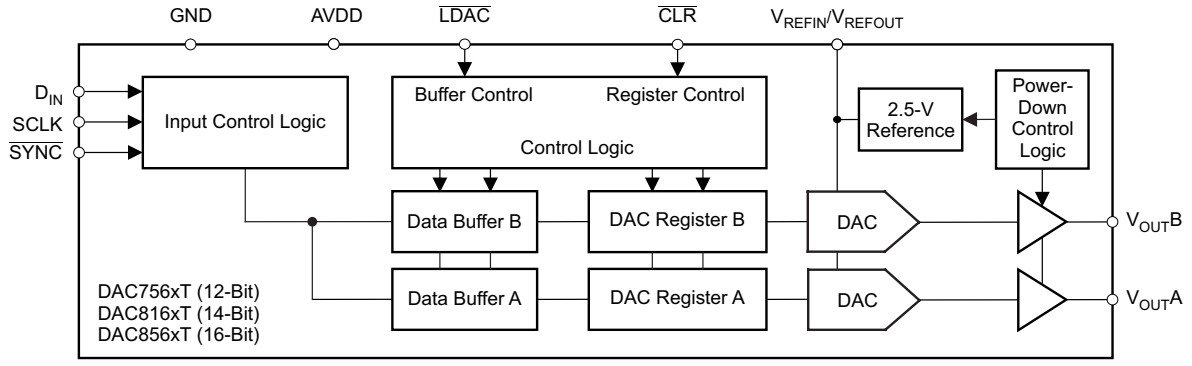


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

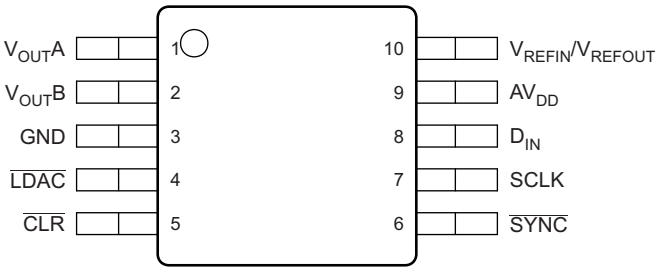
Changes from Original (September 2015) to Revision A	Page
• Changed From: Product Preview To: Production Data	1

5 Device Comparison Table

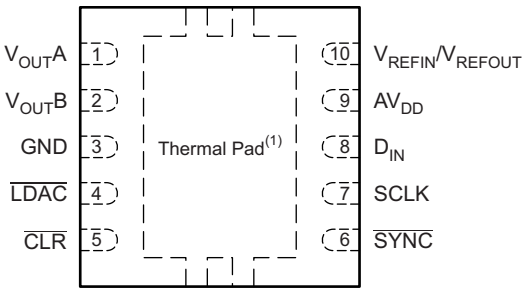
DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	RESET TO
DAC7562T	±0.75	±0.25	10	Zero
DAC7563T				Mid-scale
DAC8162T	±3	±0.5	10	Zero
DAC8163T				Mid-scale
DAC8562T	±12	±1	10	Zero
DAC8563T				Mid-scale

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
(Top View)



DSC Package
10-Pin WSON
(Top View)



(1) TI recommends connecting the thermal pad to the ground plane for better thermal dissipation.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AV_{DD}	9	I	Power-supply input, 2.7 V to 5.5 V
$\overline{CLR}$	5	I	Asynchronous clear input. The $\overline{CLR}$ input is falling-edge sensitive. On activation of $\overline{CLR}$, zero scale (DACxx62T) or mid-scale (DACxx63T) is loaded to all input and DAC registers. This sets the DAC output voltages accordingly. The device exits clear code mode on the 24th falling edge of the next write to the device. Activating $\overline{CLR}$ during a write sequence aborts the write.
D_{IN}	8	I	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-trigger logic input
GND	3	—	Ground reference point for all circuitry on the device
$\overline{LDAC}$	4	I	In *synchronous* mode, data update occurs with the falling edge of the 24th SCLK cycle, which follows a falling edge of $\overline{SYNC}$. Such *synchronous* updates do not require the $\overline{LDAC}$, which must be connected to GND permanently or asserted and held low before sending commands to the device. In *asynchronous* mode, the $\overline{LDAC}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel commands can be written in order to set different channel buffers to desired values and then make a falling edge on the $\overline{LDAC}$ pin to update the DAC output registers simultaneously.
SCLK	7	I	Serial clock input. Data can be transferred at rates up to 50 MHz. Schmitt-trigger logic input
$\overline{SYNC}$	6	I	Level-triggered control input (active-low). This input is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock falling edge. If $\overline{SYNC}$ is taken high before the 23rd clock edge, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC756xT, DAC816xT, and DAC856xT devices. Schmitt-trigger logic input
$V_{OUT}A$	1	O	Analog output voltage from DAC-A
$V_{OUT}B$	2	O	Analog output voltage from DAC-B
V_{REFIN}/V_{REFOUT}	10	I/O	Bidirectional voltage reference pin. If internal reference is used, 2.5-V output.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating ambient temperature range (unless otherwise noted).

	MIN	MAX	UNIT
AV_{DD} to GND	–0.3	6	V
$\overline{CLR}$, D_{IN}, $\overline{LDAC}$, SCLK and $\overline{SYNC}$ input voltage to GND	–0.3	AV_{DD} + 0.3	V
V_{OUT}[A, B] to GND	–0.3	AV_{DD} + 0.3	V
V_{REFIN}/V_{REFOUT} to GND	–0.3	AV_{DD} + 0.3	V
Operating temperature range	–40	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Supply voltage	AV_{DD} to GND	2.7		5.5	V
DIGITAL INPUTS						
	Digital input voltage	$\overline{CLR}$, D_{IN}, $\overline{LDAC}$, SCLK and $\overline{SYNC}$	0		AV_{DD}	V
REFERENCE INPUT						
V_{REFIN}	Reference input voltage		0		AV_{DD}	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC		DAC756xT, DAC816xT, DAC856xT		UNIT
		DSC (WSON)	DGS (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.8	173.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.3	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	79.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.5	68.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	46.2	N/A	°C/W

7.5 Electrical Characteristics

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC756xT	Resolution		12			Bits
	Relative accuracy	Using line passing through codes 32 and 4,064		±0.3	±0.75	LSB
	Differential nonlinearity	12-bit monotonic		±0.05	±0.25	
DAC816xT	Resolution		14			Bits
	Relative accuracy	Using line passing through codes 128 and 16,256		±1	±3	LSB
	Differential nonlinearity	14-bit monotonic		±0.1	±0.5	
DAC856xT	Resolution		16			Bits
	Relative accuracy	Using line passing through codes 512 and 65,024		±4	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.2	±1	
Offset error		Extrapolated from two-point line(1), unloaded		±1	±4	mV
Offset error drift				±2		µV/°C
Full-scale error		DAC register loaded with all 1s, DAC output unloaded		±0.03	±0.2	% FSR
Zero-code error		DAC register loaded with all 0s, DAC output unloaded		1	4	mV
Zero-code error drift				±2		µV/°C
Gain error		Extrapolated from two-point line(1), unloaded		±0.01	±0.15	% FSR
Gain temperature coefficient				±1		ppm FSR/°C
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time(3)		DACs unloaded		7		µs
		R_L = 1 MΩ		10		
Slew rate		Measured between 20%–80% of a full-scale transition		0.75		V/µs
Capacitive load stability		R_L = ∞		1		nF
		R_L = 2 kΩ		3		
Code-change glitch impulse		1-LSB change around major carry		0.1		nV-s
Digital feedthrough		SCLK toggling, $\overline{SYNC}$ high		0.1		nV-s
Power-on glitch impulse		R_L = 2 kΩ, C_L = 470 pF, AV_{DD} = 5.5 V		40		mV
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel, External reference		5		µV
		Full-scale swing on adjacent channel, Internal reference		15		
DC output impedance		At mid-scale input		5		Ω
Short-circuit current		DAC outputs at full-scale, DAC outputs shorted to GND		40		mA
Power-up time, including settling time		Coming out of power-down mode		50		µs
AC PERFORMANCE(2)						
DAC output noise density		T_A = 25°C, at mid-scale input, f_{OUT} = 1 kHz		90		nV/√Hz
DAC output noise		T_A = 25°C, at mid-scale input, 0.1 Hz to 10 Hz		2.6		$µV_{PP}$
LOGIC INPUTS(2)						
Input-pin leakage current			–1	±0.1	1	µA
Logic input LOW voltage V_{IL}			0		0.8	V
Logic input HIGH voltage V_{IH}			2.1		AV_{DD}	V
Pin capacitance					3	pF

(1) 16-bit: codes 512 and 65,024; 14-bit: codes 128 and 16,256; 12-bit: codes 32 and 4,064, All digital inputs kept at same IO levels before and after write to the DAC
(2) Specification based on design or characterization
(3) Transition time between 1 / 4 scale and 3 / 4 scale, including settling to within ±0.024% FSR

Electrical Characteristics (continued)

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
External reference current	External V_{REF} = 2.5 V (when internal reference is disabled), all channels active using gain = 1		15		µA
Reference input impedance	Internal reference disabled, gain = 1		170		kΩ
	Internal reference disabled, gain = 2		85		
REFERENCE OUTPUT					
Output voltage	T_A = 25°C	2.495	2.5	2.505	V
Initial accuracy	T_A = 25°C	–5	±0.1	5	mV
Output-voltage temperature drift	Internal reference output voltage temperature drift is characterized from –40°C to 125°C.		4	10	ppm/°C
Output-voltage noise	f = 0.1 Hz to 10 Hz		12		μV_{PP}
Output-voltage noise density (high-frequency noise)	T_A = 25°C, f = 1 kHz, C_L = 0 µF		250		nV/√Hz
	T_A = 25°C, f = 1 MHz, C_L = 0 µF		30		
	T_A = 25°C, f = 1 MHz, C_L = 4.7 µF		10		
Load regulation, sourcing(4)	T_A = 25°C		20		µV/mA
Load regulation, sinking(4)	T_A = 25°C		185		µV/mA
Output-current load capability(2)			±20		mA
Line regulation	T_A = 25°C		50		µV/V
Long-term stability or drift (aging)(4)	T_A = 25°C, time = 0 to 1900 hours		100		ppm
Thermal hysteresis(4)	First cycle		200		ppm
	Additional cycles		50		
POWER REQUIREMENTS(5)					
Power supply current (I_{DD})	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference off, Digital inputs at VDD or GND		0.25	0.5	mA
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference off, Digital inputs at TTL level			4	
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference on, Digital inputs at VDD or GND		0.9	1.6	
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference on, Digital inputs at TTL level			5	
	AV_{DD} = 3.6 V to 5.5 V, power-down modes, Digital inputs at VDD or GND		0.55	4	µA
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference off, Digital inputs at VDD or GND		0.2	0.4	mA
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference off, Digital inputs at TTL level			0.8	
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference on, Digital inputs at VDD or GND		0.73	1.4	
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference on, Digital inputs at TTL level			1.8	
	AV_{DD} = 2.7 V to 3.6 V, power-down modes, Digital inputs at VDD or GND		0.35	3	µA

(4) See the *Application Information* section of this data sheet.
(5) Input code = mid-scale, no load

Electrical Characteristics (continued)

At AV_{DD} = 2.7 V to 5.5 V and T_A = –40°C to 125°C (unless otherwise noted).

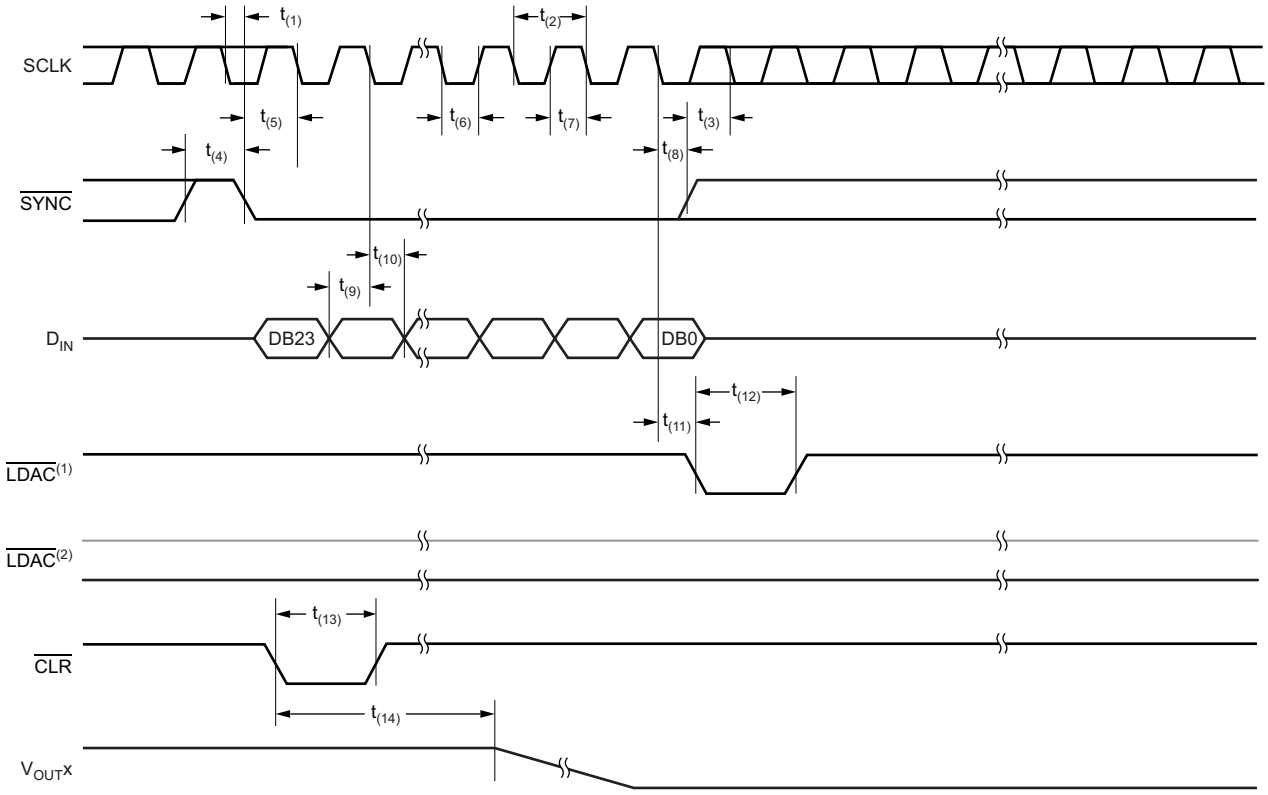
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference off, Digital inputs at VDD or GND		0.9	2.75	mW
	AV_{DD} = 3.6 V to 5.5 V, normal mode, internal reference on, Digital inputs at VDD or GND		3.2	8.8	
	AV_{DD} = 3.6 V to 5.5 V, power-down modes, Digital inputs at VDD or GND		2	22	µW
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference off, Digital inputs at VDD or GND		0.54	1.44	mW
	AV_{DD} = 2.7 V to 3.6 V, normal mode, internal reference on, Digital inputs at VDD or GND		1.97	5	
	AV_{DD} = 2.7 V to 3.6 V, power-down modes, Digital inputs at VDD or GND		0.95	10.8	µW

7.6 Timing Requirements(1)(2)

At AV_{DD} = 2.7 V to 5.5 V, external V_{REFIN} = 2.5 V to 5.5 V, and over –40°C to 125°C (unless otherwise noted). See Figure 1.

		DAC756xT, DAC816xT, DAC856xT			UNIT
		MIN	TYP	MAX	
$f_{(SCLK)}$	Serial clock frequency			50	MHz
$t_{(1)}$	SCLK falling edge to $\overline{SYNC}$ falling edge (for successful write operation)	10			ns
$t_{(2)}$	SCLK cycle time	20			ns
$t_{(3)}$	$\overline{SYNC}$ rising edge to 23rd SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	13			ns
$t_{(4)}$	Minimum $\overline{SYNC}$ HIGH time	15			ns
$t_{(5)}$	$\overline{SYNC}$ to SCLK falling edge setup time	13			ns
$t_{(6)}$	SCLK LOW time	8			ns
$t_{(7)}$	SCLK HIGH time	8			ns
$t_{(8)}$	SCLK falling edge to $\overline{SYNC}$ rising edge	10			ns
$t_{(9)}$	Data setup time	6			ns
$t_{(10)}$	Data hold time	6			ns
$t_{(11)}$	SCLK falling edge to $\overline{LDAC}$ falling edge for asynchronous LDAC update mode	5			ns
$t_{(12)}$	$\overline{LDAC}$ pulse duration, LOW time	10			ns
$t_{(13)}$	$\overline{CLR}$ pulse duration, LOW time	80			ns
$t_{(14)}$	$\overline{CLR}$ falling edge to start of V_{OUT} transition			100	ns

(1) All input signals are specified with $t_r = t_f$ = 1 ns/V (10% to 90% of AV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) See the *Serial Write Operation* timing diagram (Figure 1).



(1) Asynchronous $\overline{LDAC}$ update mode. For more information, see the *LDAC Functionality* section.
(2) Synchronous $\overline{LDAC}$ update mode; $\overline{LDAC}$ remains low. For more information, see the *LDAC Functionality* section.

Figure 1. Timing Diagram, Serial Write Operation

7.7 Typical Characteristics

Table 1. Typical Characteristics: Internal Reference Performance

MEASUREMENT	POWER-SUPPLY VOLTAGE	FIGURE NUMBER
Internal Reference Voltage vs Temperature	5.5 V	Figure 2
Internal Reference Voltage Temperature Drift Histogram		Figure 3
Internal Reference Voltage vs Load Current		Figure 4
Internal Reference Voltage vs Time		Figure 5
Internal Reference Noise Density vs Frequency		Figure 6
Internal Reference Voltage vs Supply Voltage	2.7 V–5.5 V	Figure 7

Table 2. Typical Characteristics: DAC Static Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
FULL-SCALE, GAIN, OFFSET AND ZERO-CODE ERRORS			
Full-Scale Error vs Temperature		5.5 V	Figure 16
Gain Error vs Temperature			Figure 17
Offset Error vs Temperature			Figure 18
Zero-Code Error vs Temperature			Figure 19
Full-Scale Error vs Temperature		2.7 V	Figure 63
Gain Error vs Temperature			Figure 64
Offset Error vs Temperature			Figure 65
Zero-Code Error vs Temperature			Figure 66
LOAD REGULATION			
DAC Output Voltage vs Load Current		5.5 V	Figure 30
		2.7 V	Figure 74
DIFFERENTIAL NONLINEARITY ERROR			
Differential Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 9
	T = 25°C		Figure 11
	T = 125°C		Figure 13
Differential Linearity Error vs Temperature			Figure 15
Differential Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 56
	T = 25°C		Figure 58
	T = 125°C		Figure 60
Differential Linearity Error vs Temperature			Figure 62
INTEGRAL NONLINEARITY ERROR (RELATIVE ACCURACY)			
Linearity Error vs Digital Input Code	T = –40°C	5.5 V	Figure 8
	T = 25°C		Figure 10
	T = 125°C		Figure 12
Linearity Error vs Temperature			Figure 14
Linearity Error vs Digital Input Code	T = –40°C	2.7 V	Figure 55
	T = 25°C		Figure 57
	T = 125°C		Figure 59
Linearity Error vs Temperature			Figure 61

Table 2. Typical Characteristics: DAC Static Performance (continued)

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
POWER-DOWN CURRENT			
Power-Down Current vs Temperature		5.5 V	Figure 28
Power-Down Current vs Power-Supply Voltage		2.7 V – 5.5 V	Figure 29
Power-Down Current vs Temperature		2.7 V	Figure 73
POWER-SUPPLY CURRENT			
Power-Supply Current vs Temperature	External V_{REF}	5.5 V	Figure 20
	Internal V_{REF}		Figure 21
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 22
	Internal V_{REF}		Figure 23
Power-Supply Current Histogram	External V_{REF}		Figure 24
	Internal V_{REF}		Figure 25
Power-Supply Current vs Power-Supply Voltage	External V_{REF}	2.7 V – 5.5 V	Figure 26
	Internal V_{REF}		Figure 27
Power-Supply Current vs Temperature	External V_{REF}	3.6 V	Figure 49
	Internal V_{REF}		Figure 50
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 51
	Internal V_{REF}		Figure 52
Power-Supply Current Histogram	External V_{REF}		Figure 53
	Internal V_{REF}		Figure 54
Power-Supply Current vs Temperature	External V_{REF}	2.7 V	Figure 67
	Internal V_{REF}		Figure 68
Power-Supply Current vs Digital Input Code	External V_{REF}		Figure 69
	Internal V_{REF}		Figure 70
Power-Supply Current Histogram	External V_{REF}		Figure 71
	Internal V_{REF}		Figure 72

Table 3. Typical Characteristics: DAC Dynamic Performance

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
CHANNEL-TO-CHANNEL CROSSTALK			
Channel-to-Channel Crosstalk	5-V Rising Edge	5.5 V	Figure 43
	5-V Falling Edge		Figure 44
CLOCK FEEDTHROUGH			
Clock Feedthrough	500 kHz, Midscale	5.5 V	Figure 48
		2.7 V	Figure 87
GLITCH IMPULSE			
Glitch Impulse, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	5.5 V	Figure 37
	Falling Edge, Code 8000h to 7FFFh		Figure 38
Glitch Impulse, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 39
	Falling Edge, Code 8000h to 7FFCh		Figure 40
Glitch Impulse, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 41
	Falling Edge, Code 8000h to 7FF0h		Figure 42

Table 3. Typical Characteristics: DAC Dynamic Performance (continued)

MEASUREMENT		POWER-SUPPLY VOLTAGE	FIGURE NUMBER
Glitch Impulse, 1-LSB Step	Rising Edge, Code 7FFFh to 8000h	2.7 V	Figure 79
	Falling Edge, Code 8000h to 7FFFh		Figure 80
Glitch Impulse, 4-LSB Step	Rising Edge, Code 7FFCh to 8000h		Figure 81
	Falling Edge, Code 8000h to 7FFCh		Figure 82
Glitch Impulse, 16-LSB Step	Rising Edge, Code 7FF0h to 8000h		Figure 83
	Falling Edge, Code 8000h to 7FF0h		Figure 84
NOISE			
DAC Output Noise Density vs Frequency	External V_{REF}	5.5 V	Figure 45
	Internal V_{REF}		Figure 46
DAC Output Noise 0.1 Hz to 10 Hz	External V_{REF}		Figure 47
POWER-ON GLITCH			
Power-On Glitch	Reset to Zero Scale	5.5 V	Figure 35
	Reset to Midscale		Figure 36
	Reset to Zero Scale	2.7 V	Figure 85
	Reset to Midscale		Figure 86
SETTLING TIME			
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	5.5 V	Figure 31
	Falling Edge, Code FFFFh to 0h		Figure 32
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 33
	Falling Edge, Code C000h to 4000h		Figure 34
Full-Scale Settling Time	Rising Edge, Code 0h to FFFFh	2.7 V	Figure 75
	Falling Edge, Code FFFFh to 0h		Figure 76
Half-Scale Settling Time	Rising Edge, Code 4000h to C000h		Figure 77
	Falling Edge, Code C000h to 4000h		Figure 78

7.7.1 Typical Characteristics: Internal Reference

At T_A = 25°C, AV_{DD} = 5.5 V, gain = 2, and V_{REFOUT} unloaded, unless otherwise noted.

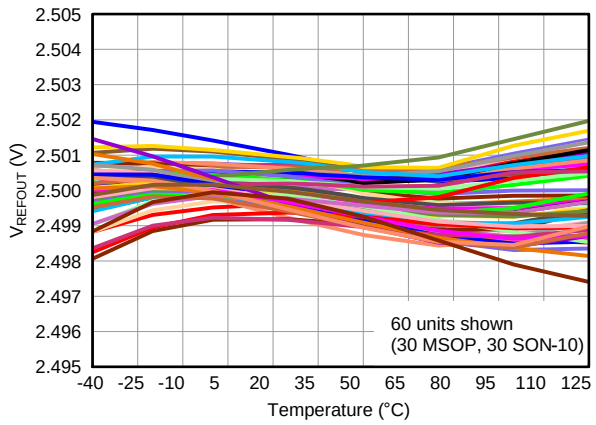


Figure 2. Internal Reference Voltage vs Temperature

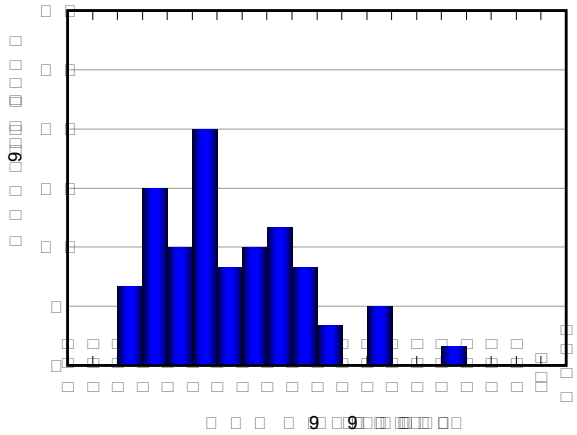


Figure 3. Internal Reference Voltage, Temperature Drift Histogram

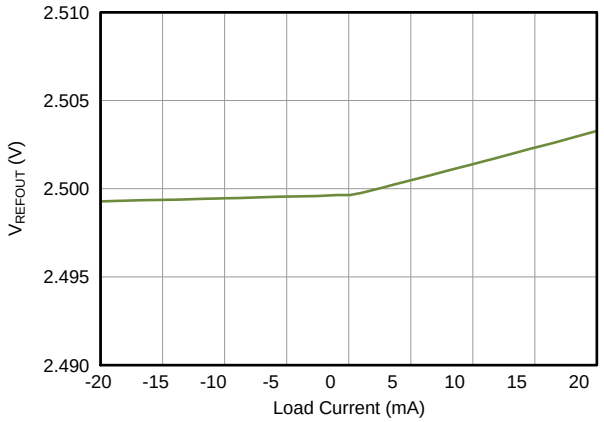


Figure 4. Internal Reference Voltage vs Load Current

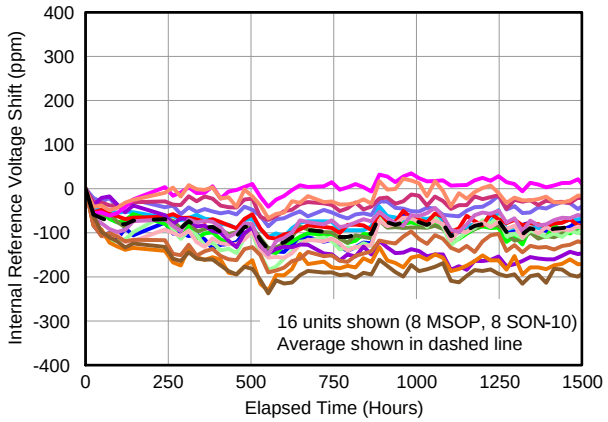


Figure 5. Internal Reference Voltage vs Time

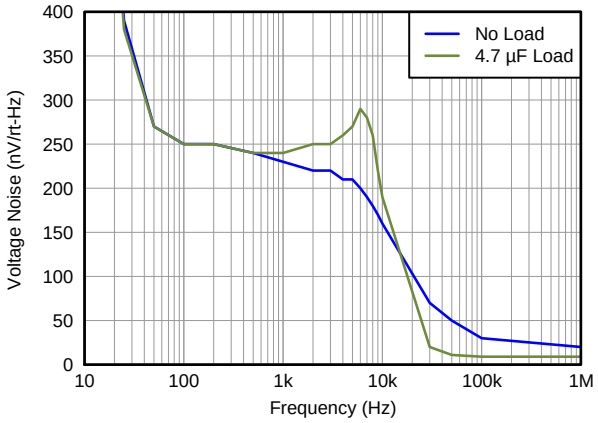


Figure 6. Internal Reference Noise Density vs Frequency

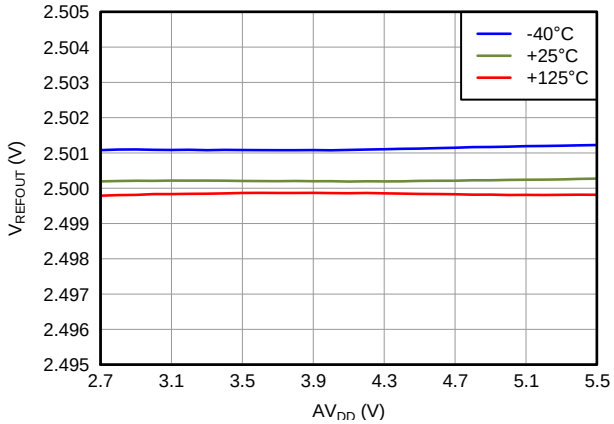


Figure 7. Internal Reference Voltage vs Supply Voltage

7.7.2 Typical Characteristics: DAC at AV_{DD} = 5.5 V

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

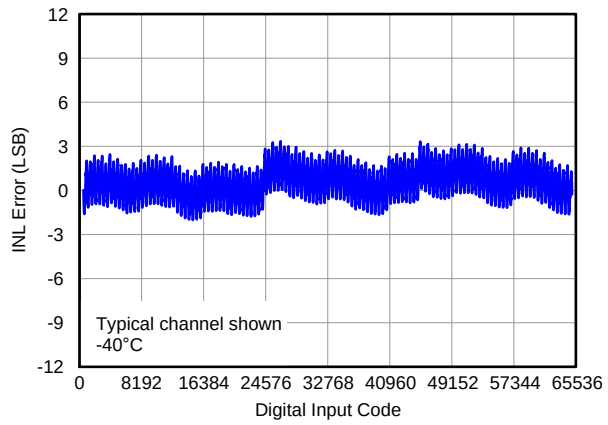


Figure 8. Linearity Error vs Digital Input Code (–40°C)

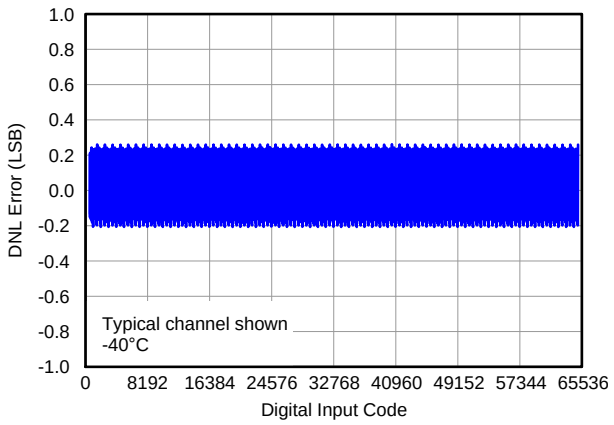


Figure 9. Differential Linearity Error vs Digital Input Code (–40°C)

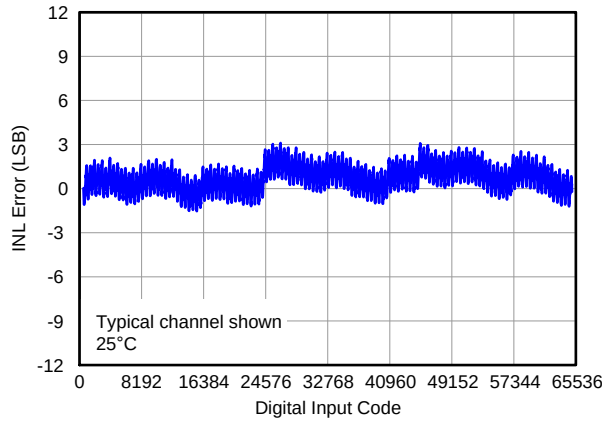


Figure 10. Linearity Error vs Digital Input Code (25°C)

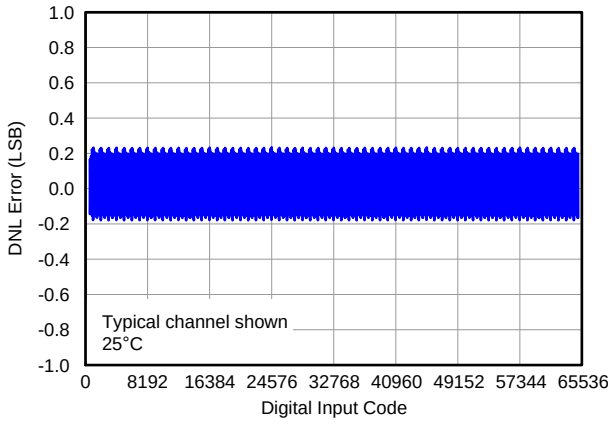


Figure 11. Differential Linearity Error vs Digital Input Code (25°C)

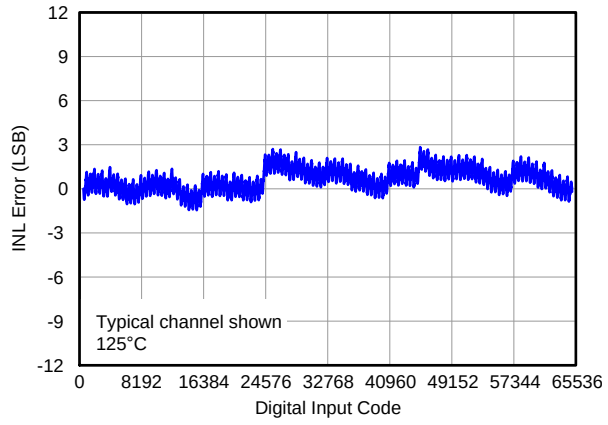


Figure 12. Linearity Error vs Digital Input Code (125°C)

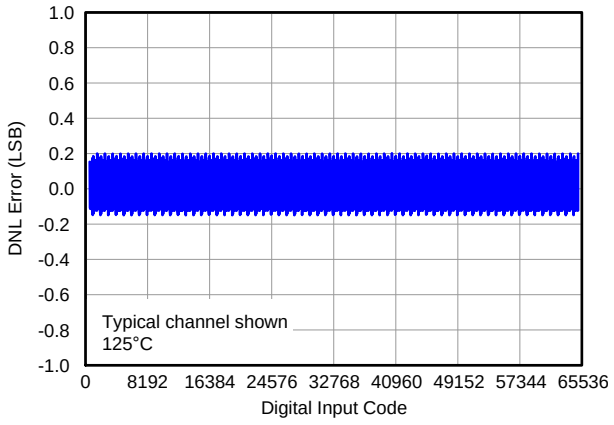


Figure 13. Differential Linearity Error vs Digital Input Code (125°C)

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

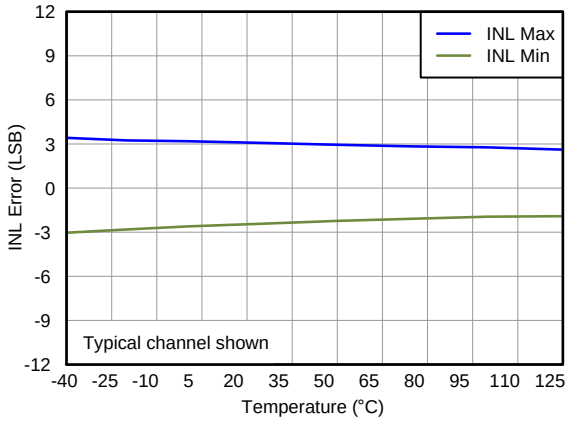


Figure 14. Linearity Error vs Temperature

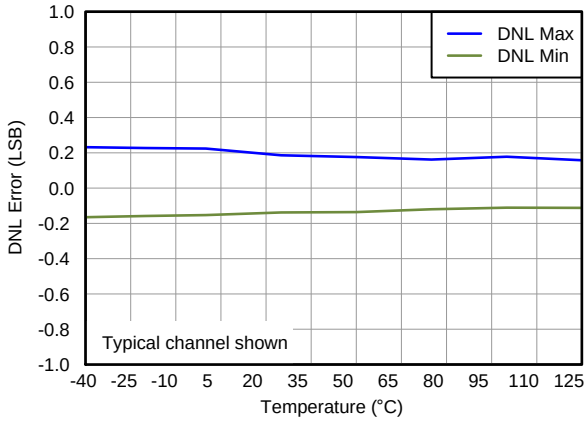


Figure 15. Differential Linearity Error vs Temperature

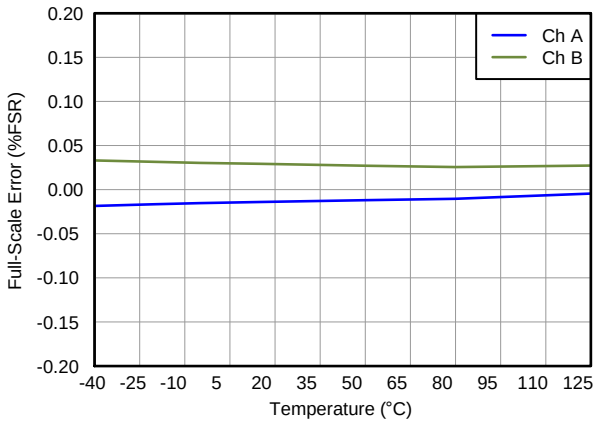


Figure 16. Full-Scale Error vs Temperature

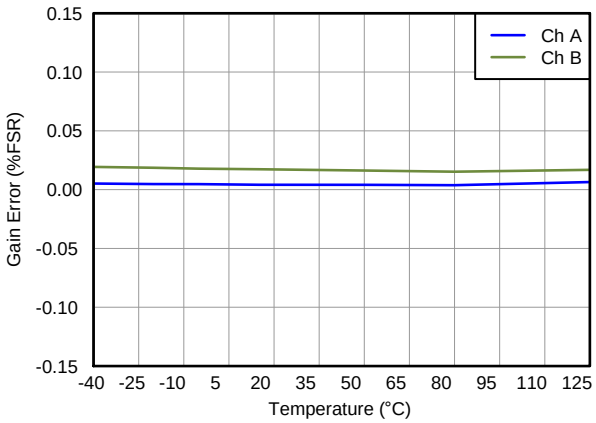


Figure 17. Gain Error vs Temperature

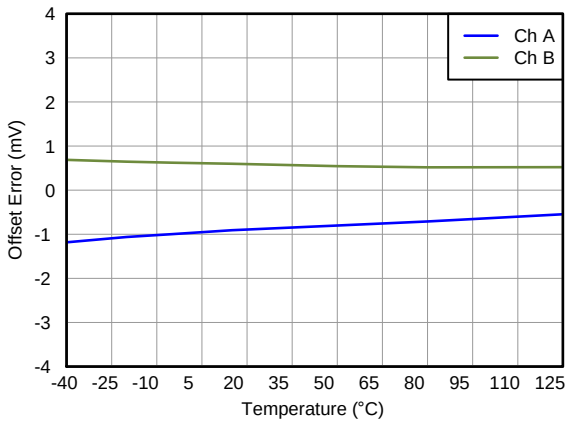


Figure 18. Offset Error vs Temperature

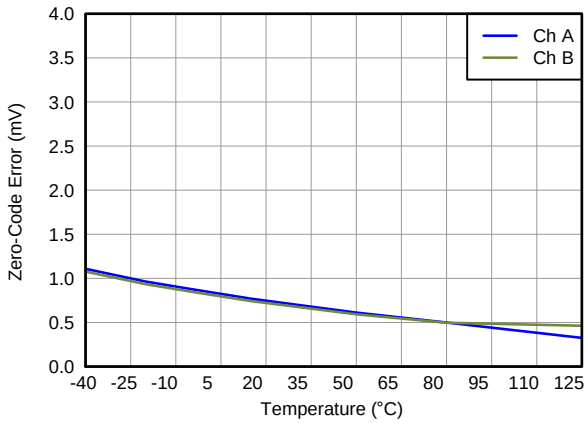


Figure 19. Zero-Code Error vs Temperature

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

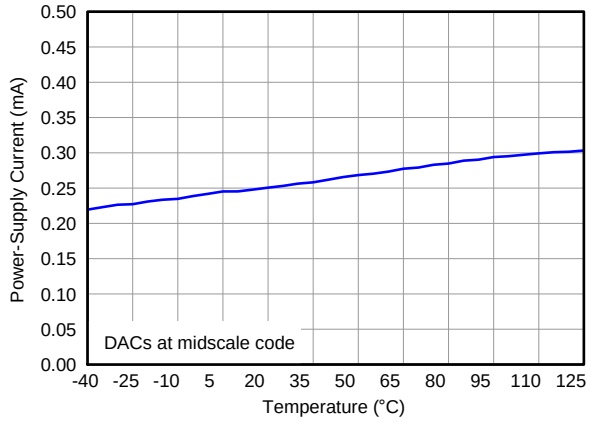


Figure 20. Power-Supply Current vs Temperature

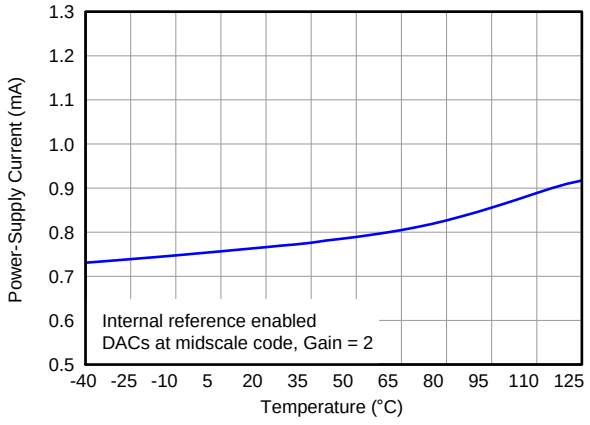


Figure 21. Power-Supply Current vs Temperature

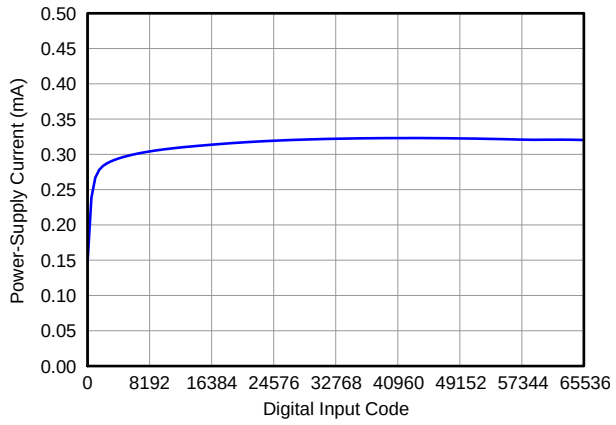


Figure 22. Power-Supply Current vs Digital Input Code

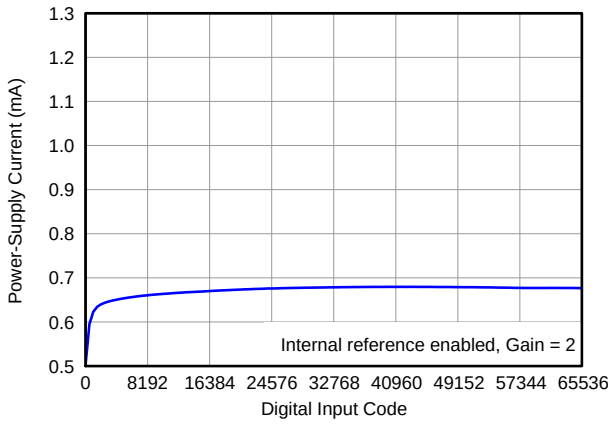


Figure 23. Power-Supply Current vs Digital Input Code

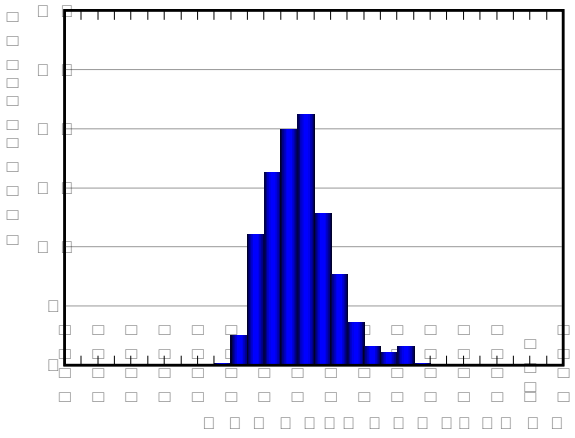


Figure 24. Power-Supply Current Histogram

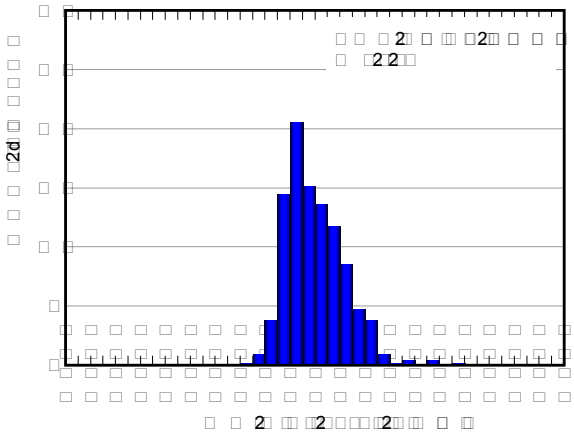


Figure 25. Power-Supply Current Histogram

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

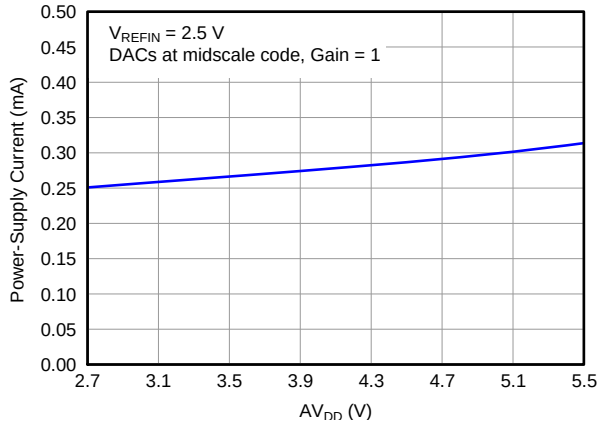


Figure 26. Power-Supply Current vs Power-Supply Voltage

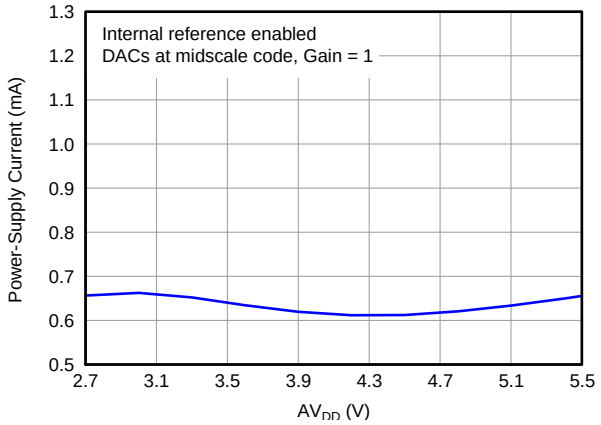


Figure 27. Power-Supply Current vs Power-Supply Voltage

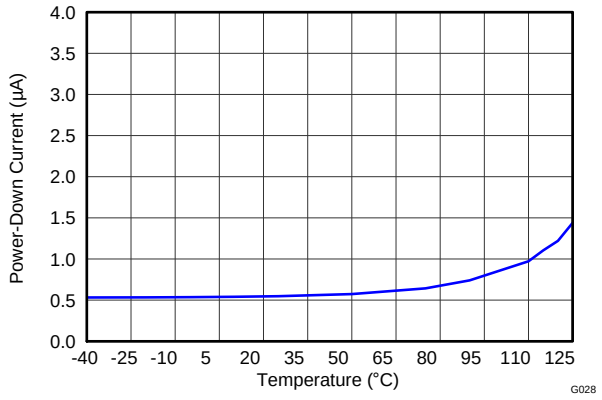


Figure 28. Power-Down Current vs Temperature

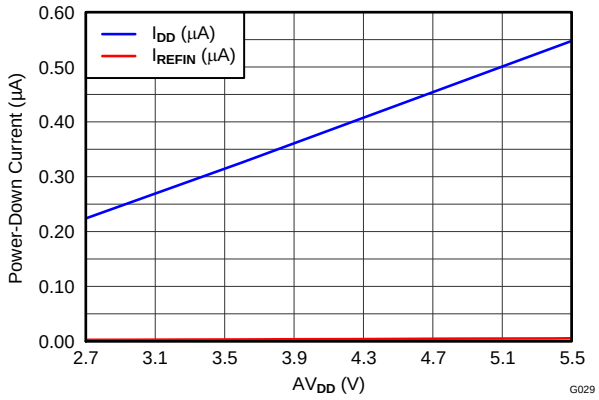


Figure 29. Power-Down Current vs Power-Supply Voltage

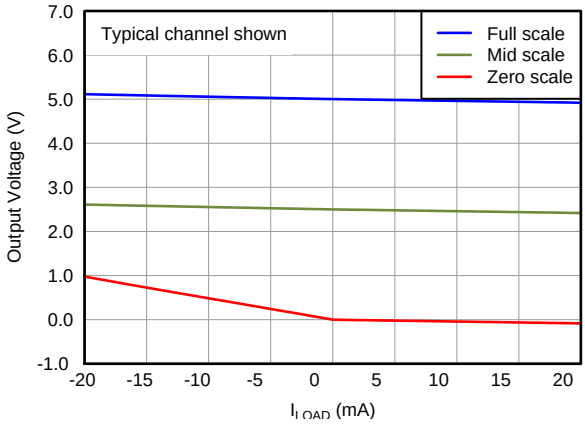


Figure 30. DAC Output Voltage vs Load Current

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

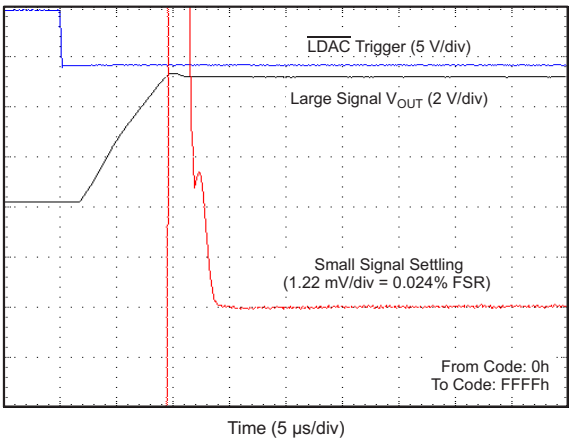


Figure 31. Full-Scale Settling Time, Rising Edge

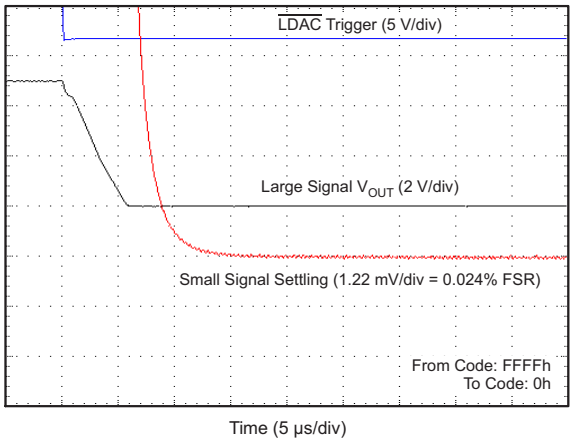


Figure 32. Full-Scale Settling Time, Falling Edge

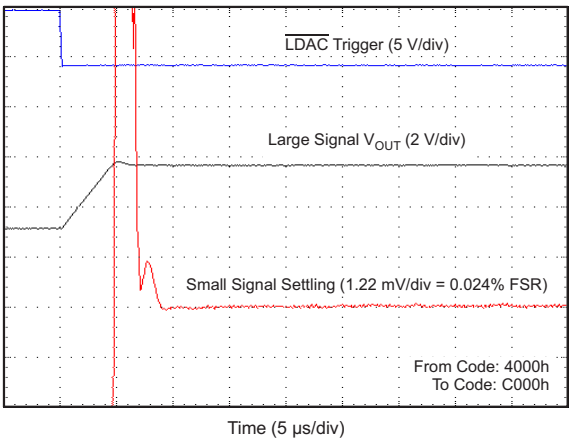


Figure 33. Half-Scale Settling Time, Rising Edge

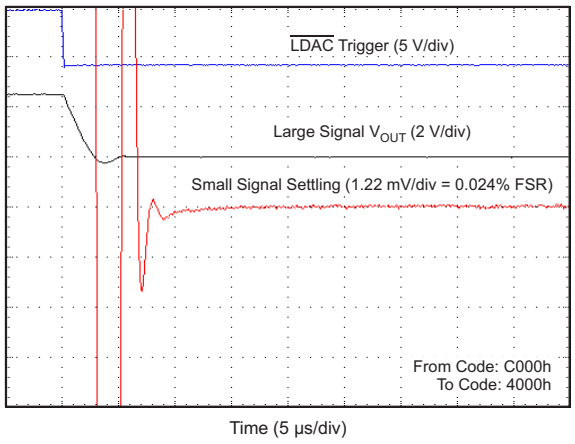


Figure 34. Half-Scale Settling Time, Falling Edge

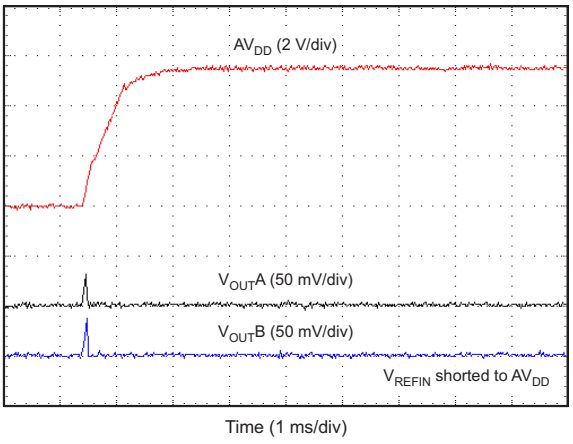


Figure 35. Power-On Glitch, Reset to Zero Scale

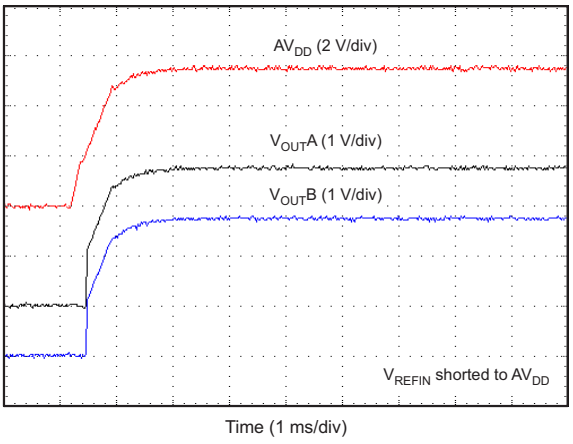


Figure 36. Power-On Glitch, Reset to Midscale

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

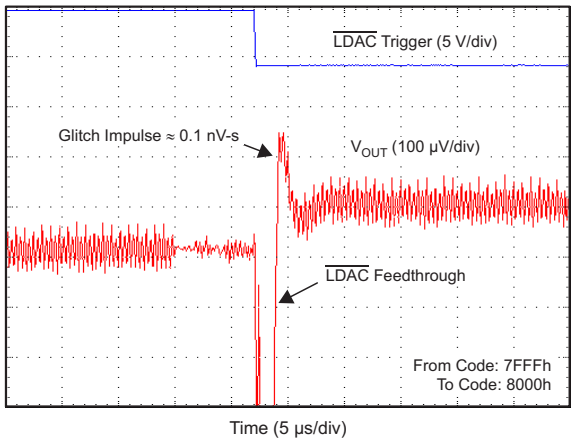


Figure 37. Glitch Impulse, Rising Edge, 1-LSB Step

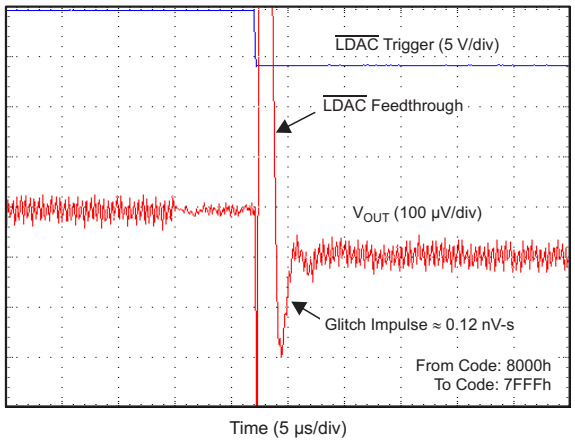


Figure 38. Glitch Impulse, Falling Edge, 1-LSB Step

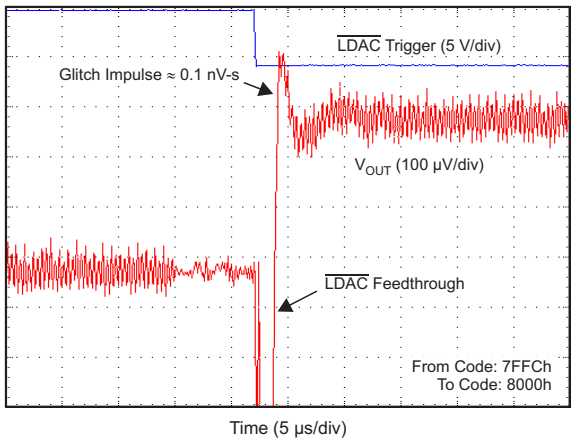


Figure 39. Glitch Impulse, Rising Edge, 4-LSB Step

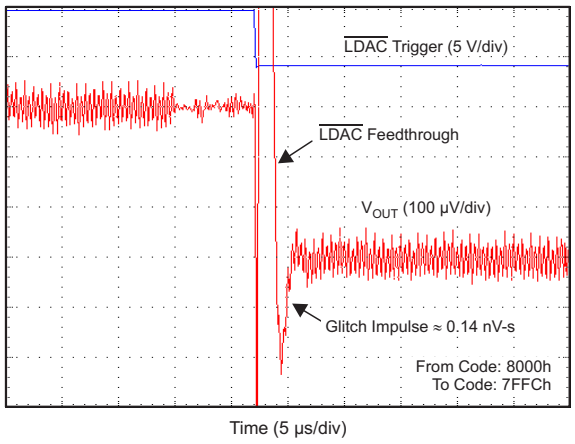


Figure 40. Glitch Impulse, Falling Edge, 4-LSB Step

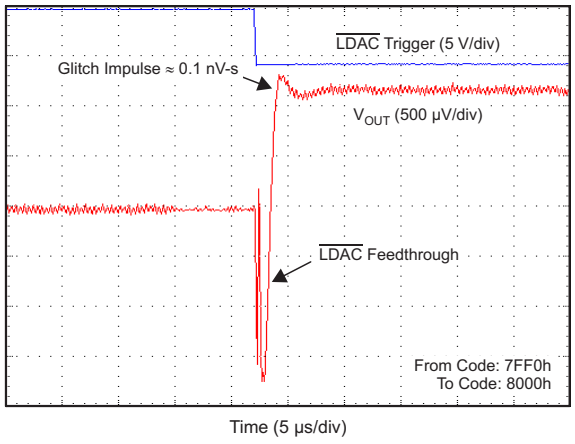


Figure 41. Glitch Impulse, Rising Edge, 16-LSB Step

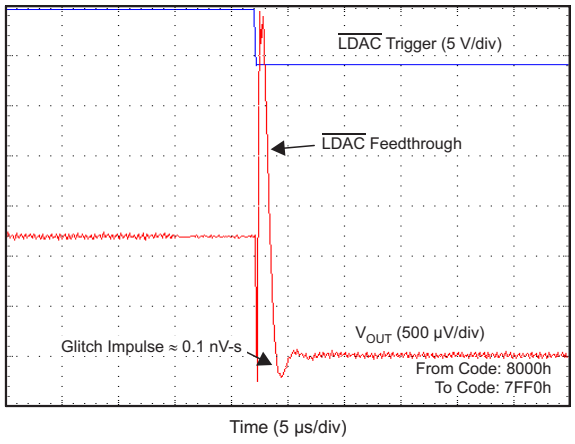


Figure 42. Glitch Impulse, Falling Edge, 16-LSB Step

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

At T_A = 25°C, 5-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

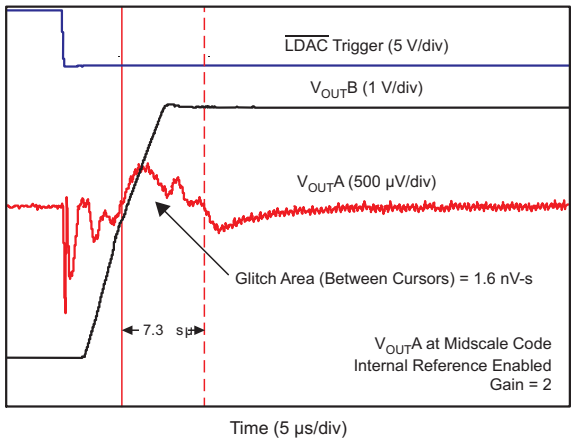


Figure 43. Channel-to-Channel Crosstalk, 5-V Rising Edge

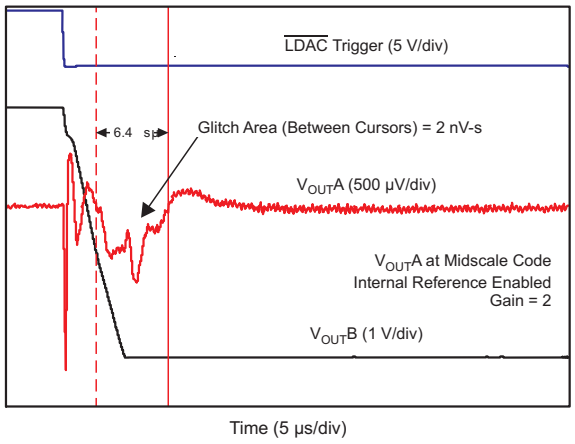


Figure 44. Channel-to-Channel Crosstalk, 5-V Falling Edge

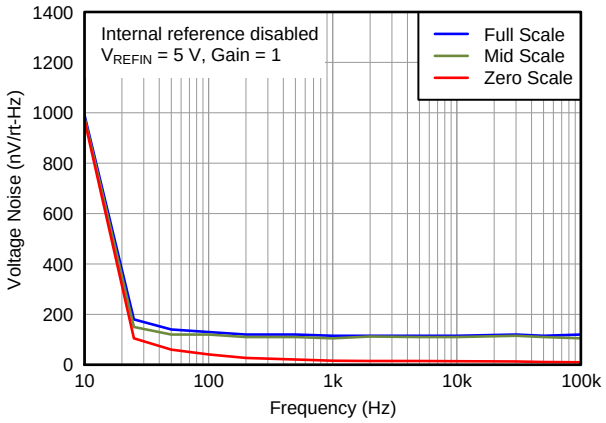


Figure 45. DAC Output Noise Density vs Frequency

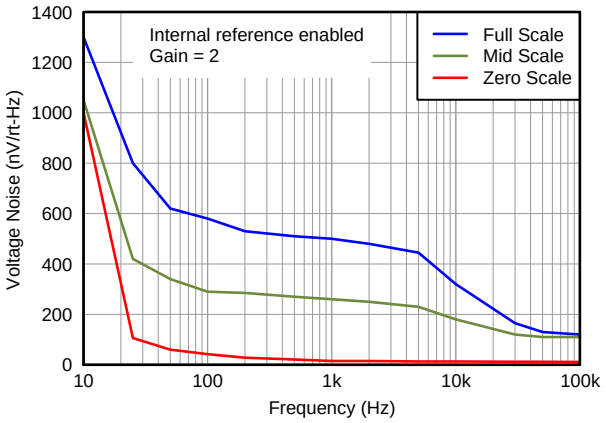


Figure 46. DAC Output Noise Density vs Frequency

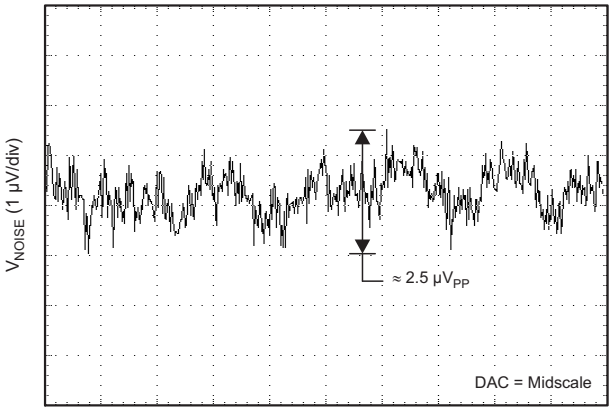


Figure 47. DAC Output Noise, 0.1 Hz to 10 Hz

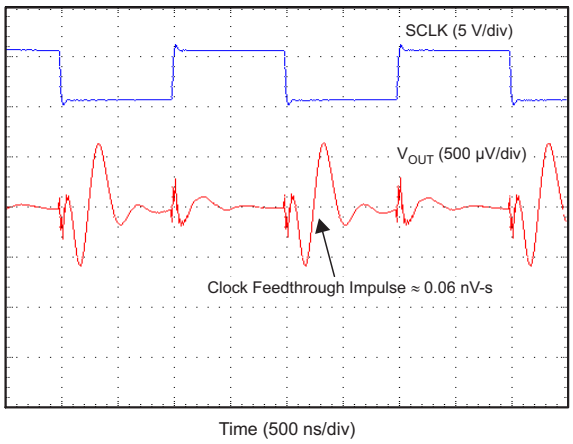


Figure 48. Clock Feedthrough, 500 kHz, Midscale

7.7.3 Typical Characteristics: DAC at AV_{DD} = 3.6 V

At T_A = 25°C, 3.3-V external reference used, gain = 1 and DAC output not loaded, unless otherwise noted.

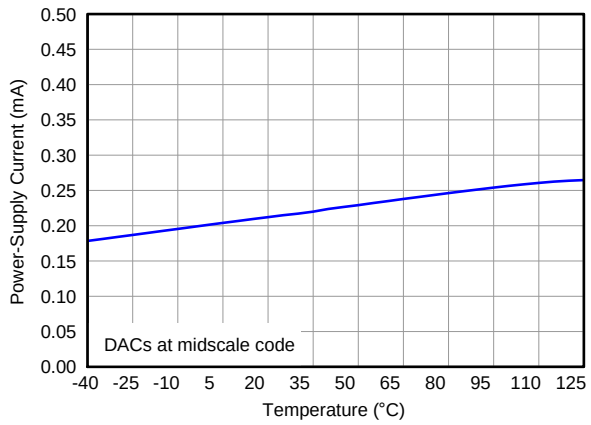


Figure 49. Power-Supply Current vs Temperature

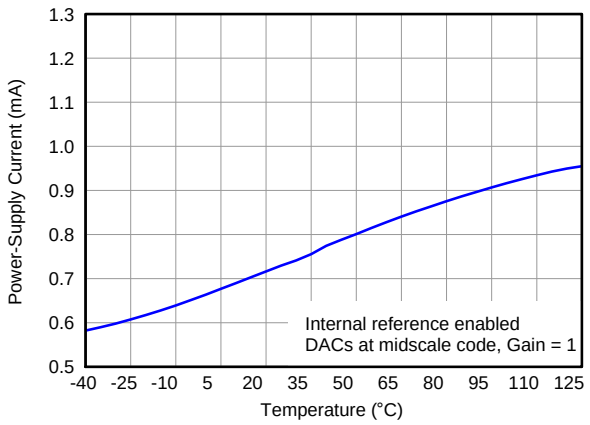


Figure 50. Power-Supply Current vs Temperature

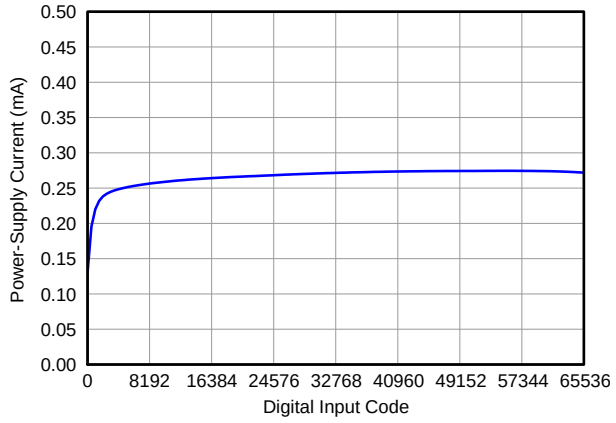


Figure 51. Power-Supply Current vs Digital Input Code

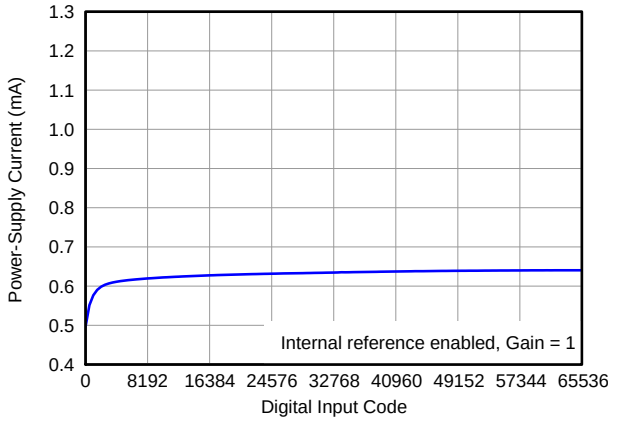


Figure 52. Power-Supply Current vs Digital Input Code

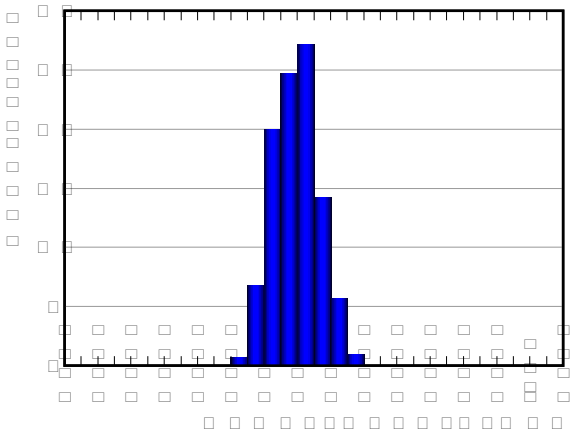


Figure 53. Power-Supply Current Histogram

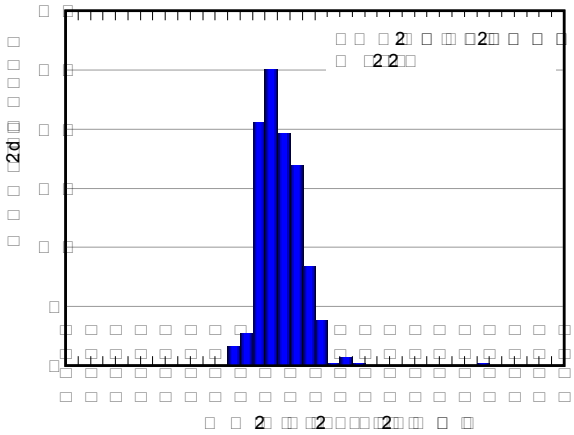


Figure 54. Power-Supply Current Histogram

7.7.4 Typical Characteristics: DAC at AV_{DD} = 2.7 V

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

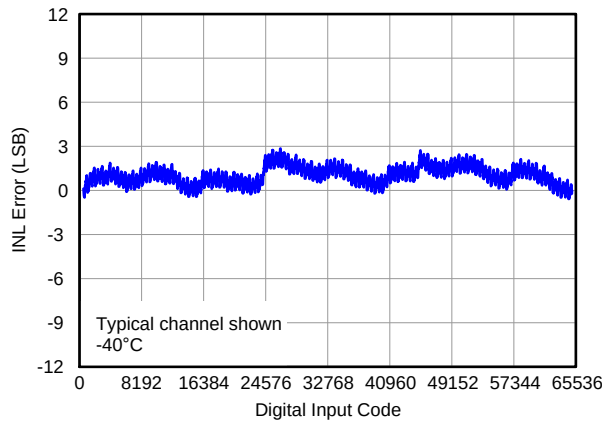


Figure 55. Linearity Error vs Digital Input Code (–40°C)

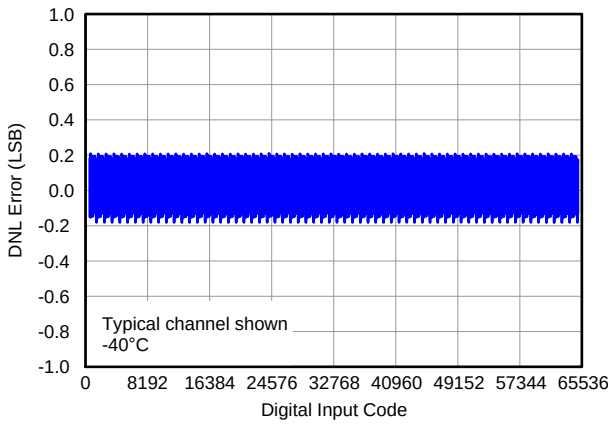


Figure 56. Differential Linearity Error vs Digital Input Code (–40°C)

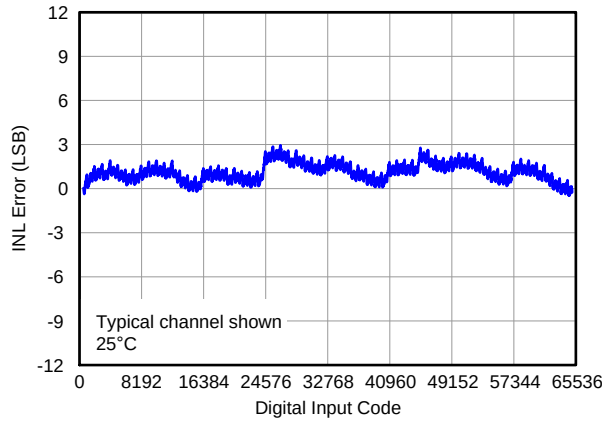


Figure 57. Linearity Error vs Digital Input Code (25°C)

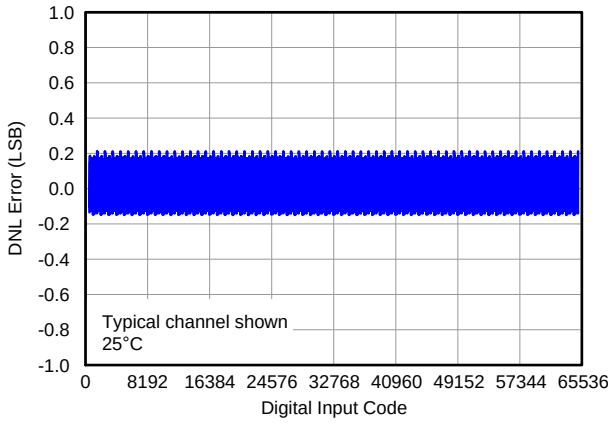


Figure 58. Differential Linearity Error vs Digital Input Code (25°C)

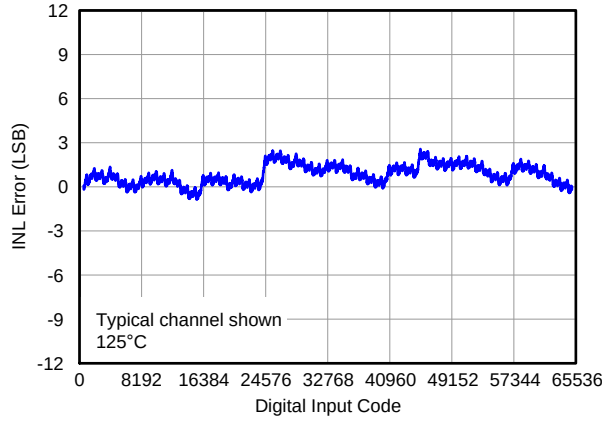


Figure 59. Linearity Error vs Digital Input Code (125°C)

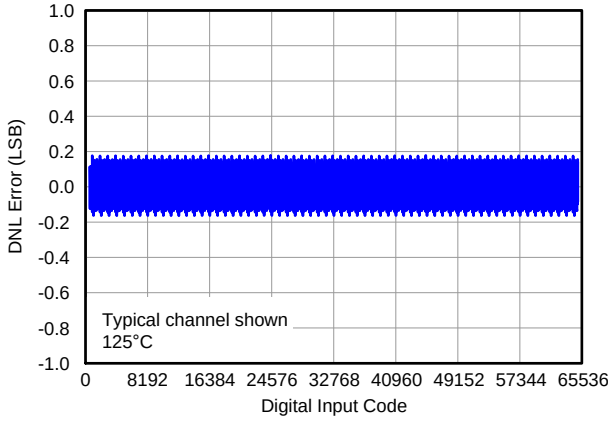


Figure 60. Differential Linearity Error vs Digital Input Code (125°C)

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

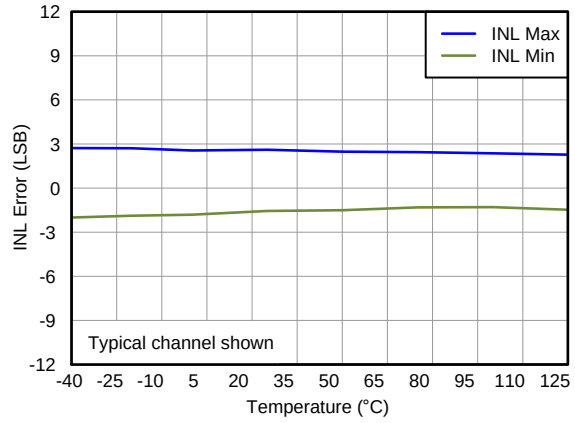


Figure 61. Linearity Error vs Temperature

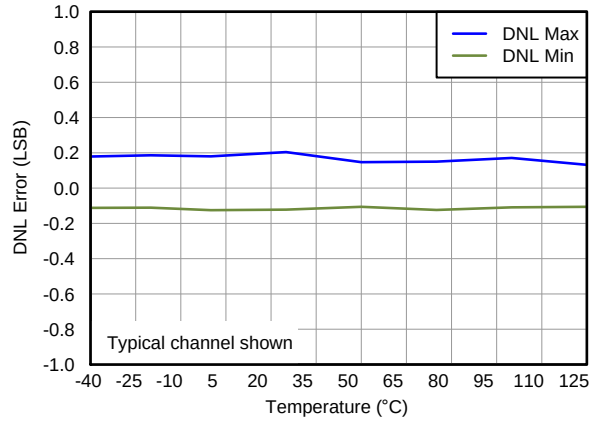


Figure 62. Differential Linearity Error vs Temperature

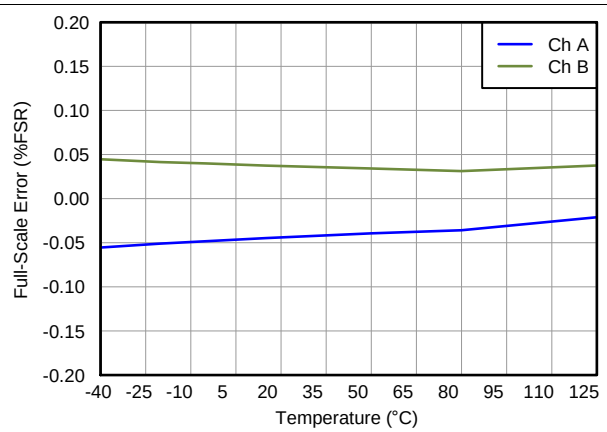


Figure 63. Full-Scale Error vs Temperature

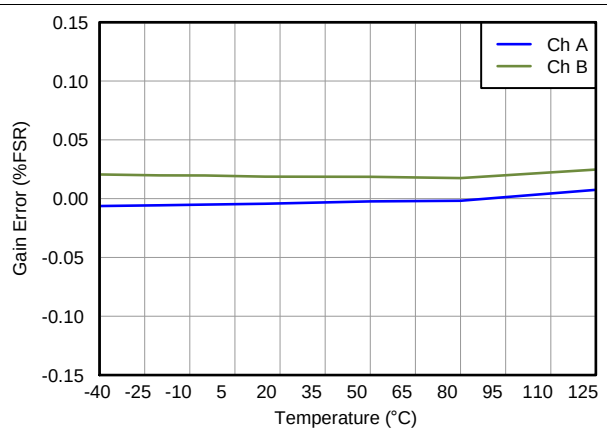


Figure 64. Gain Error vs Temperature

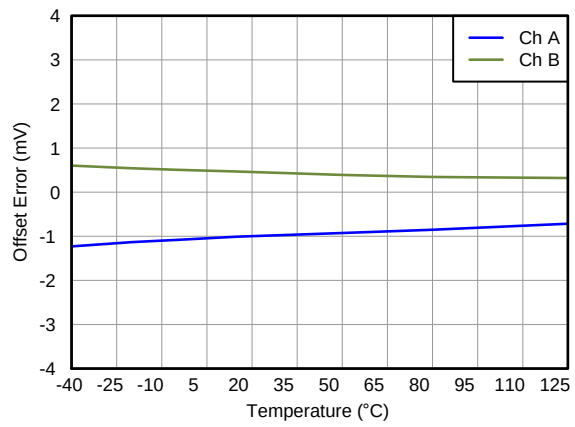


Figure 65. Offset Error vs Temperature

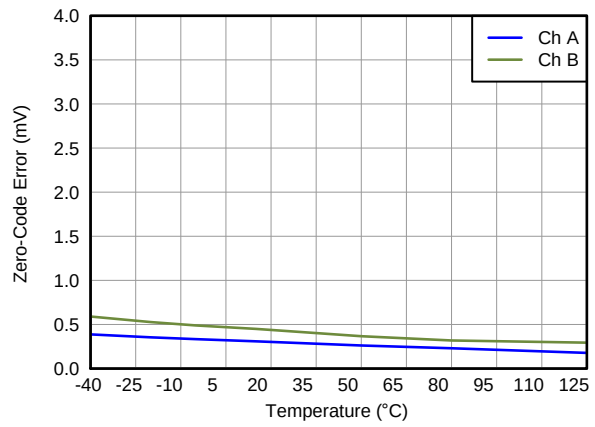


Figure 66. Zero-Code Error vs Temperature

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

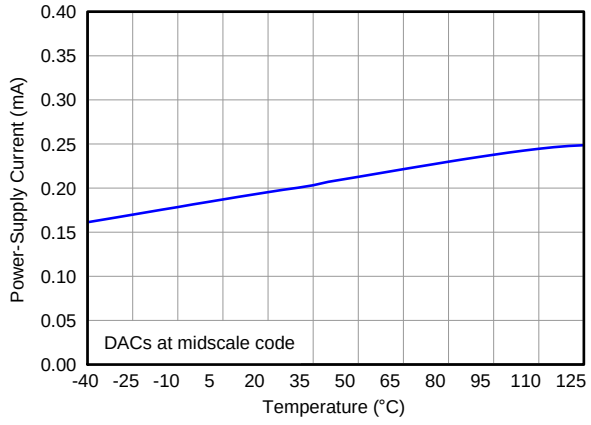


Figure 67. Power-Supply Current vs Temperature

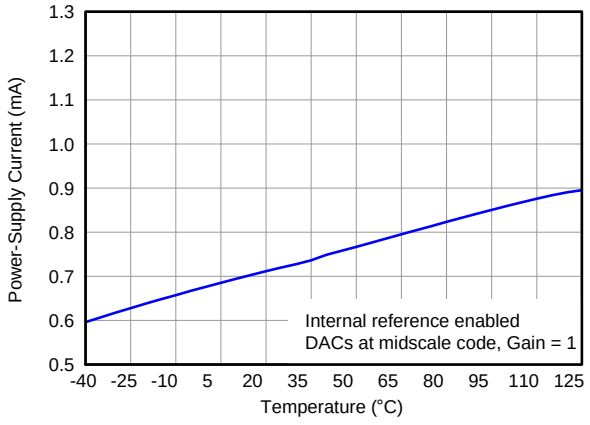


Figure 68. Power-Supply Current vs Temperature

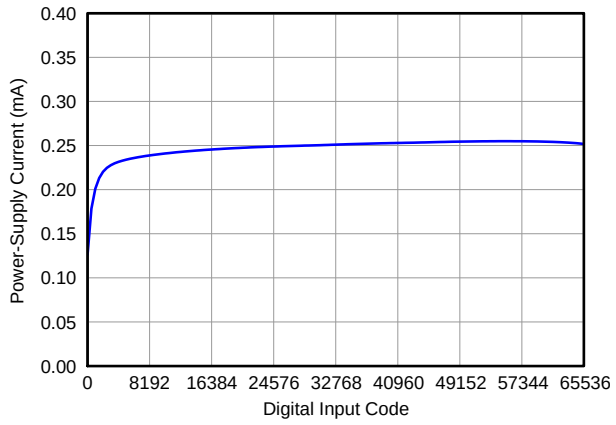


Figure 69. Power-Supply Current vs Digital Input Code

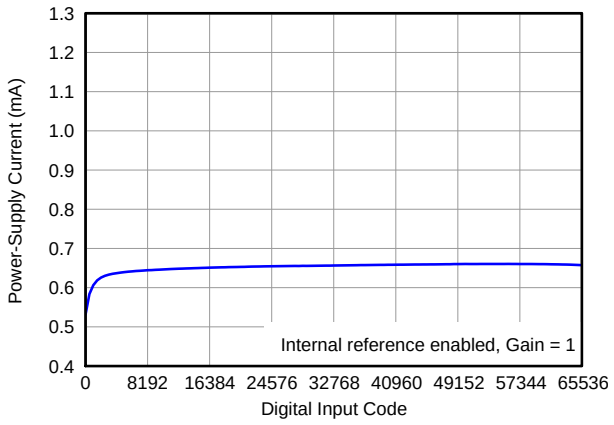


Figure 70. Power-Supply Current vs Digital Input Code

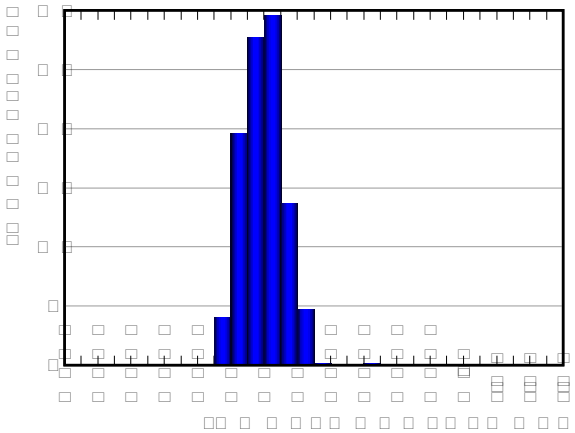


Figure 71. Power-Supply Current Histogram

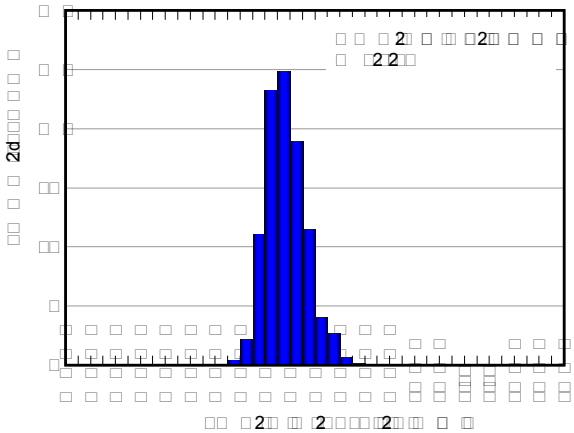


Figure 72. Power-Supply Current Histogram

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

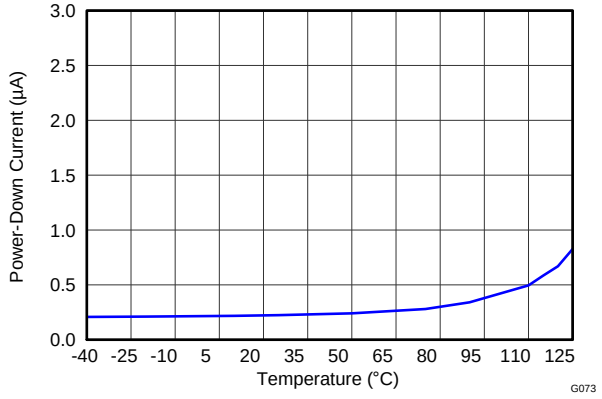


Figure 73. Power-Down Current vs Temperature

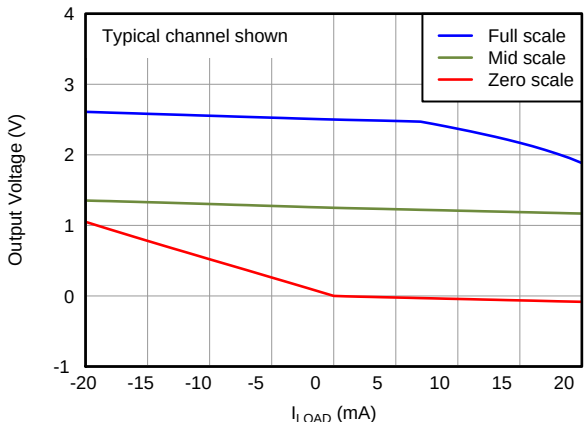


Figure 74. DAC Output Voltage vs Load Current

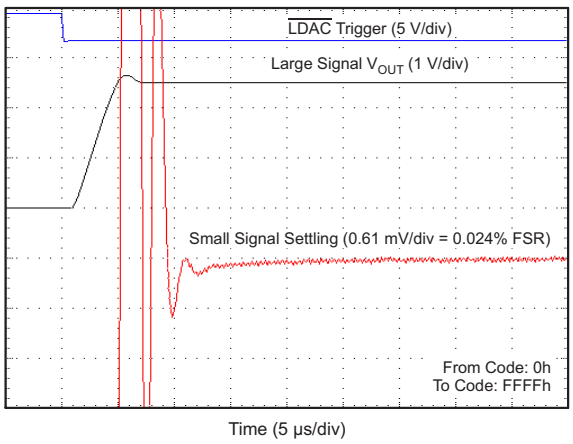


Figure 75. Full-Scale Settling Time, Rising Edge

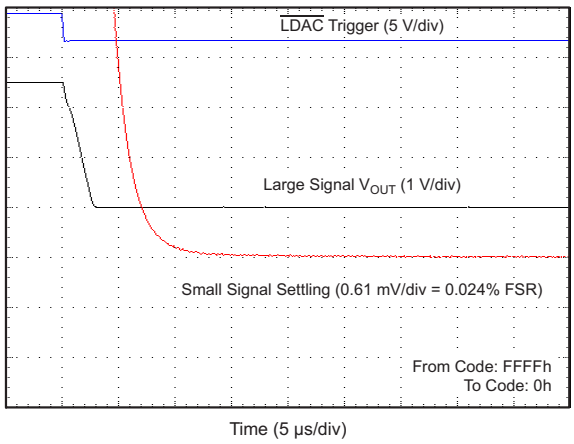


Figure 76. Full-Scale Settling Time, Falling Edge

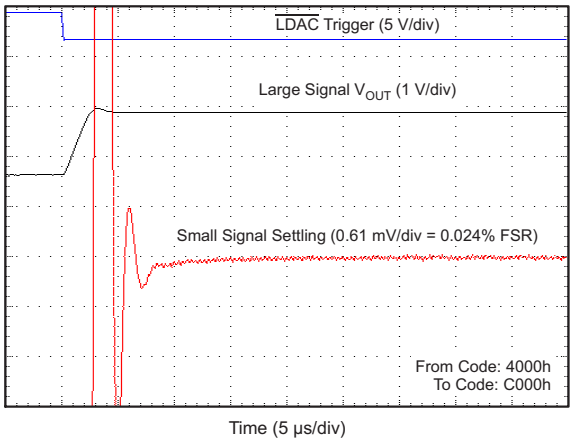


Figure 77. Half-Scale Settling Time, Rising Edge

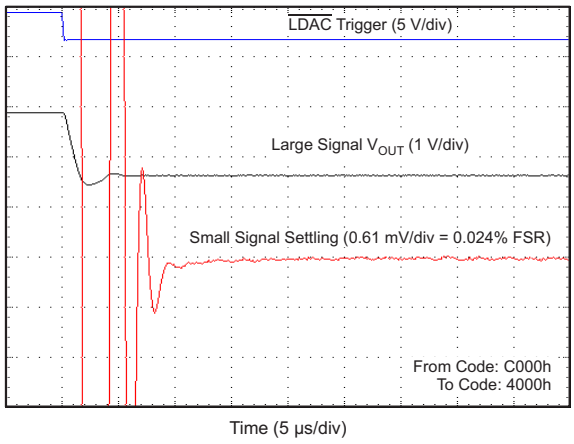


Figure 78. Half-Scale Settling Time, Falling Edge

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

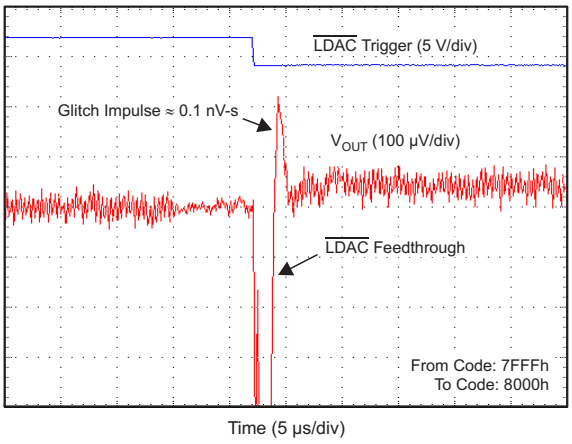


Figure 79. Glitch Impulse, Rising Edge, 1-LSB Step

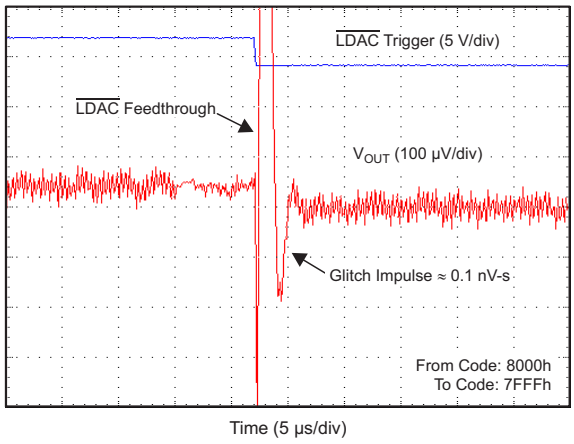


Figure 80. Glitch Impulse, Falling Edge, 1-LSB Step

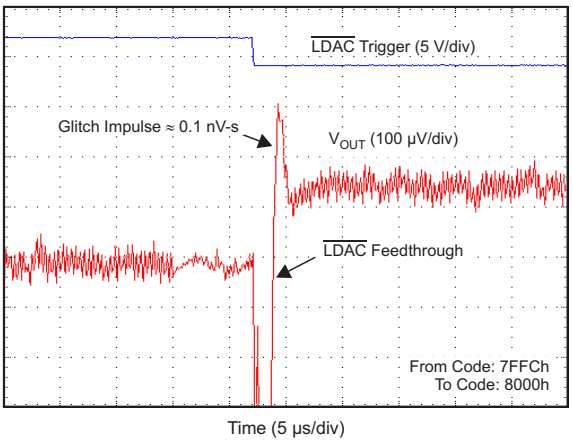


Figure 81. Glitch Impulse, Rising Edge, 4-LSB Step

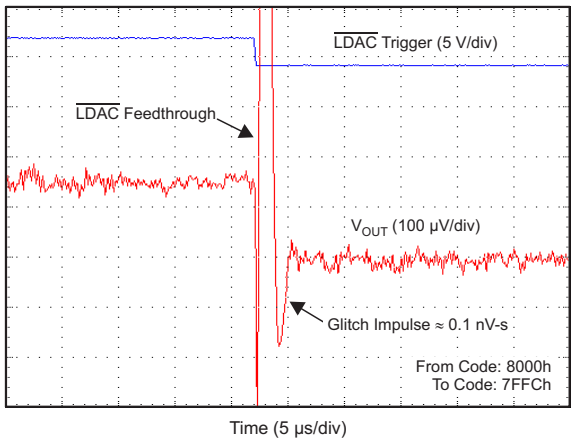


Figure 82. Glitch Impulse, Falling Edge, 4-LSB Step

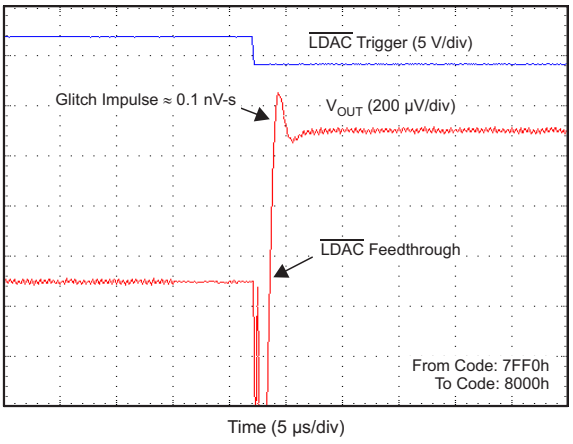


Figure 83. Glitch Impulse, Rising Edge, 16-LSB Step

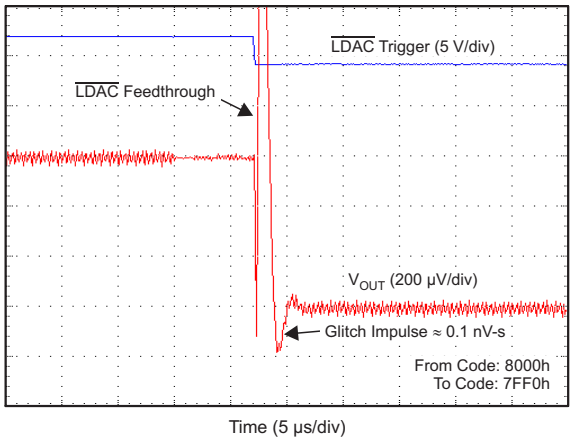


Figure 84. Glitch Impulse, Falling Edge, 16-LSB Step

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

At T_A = 25°C, 2.5-V external reference used, gain = 1, and DAC output not loaded, unless otherwise noted.

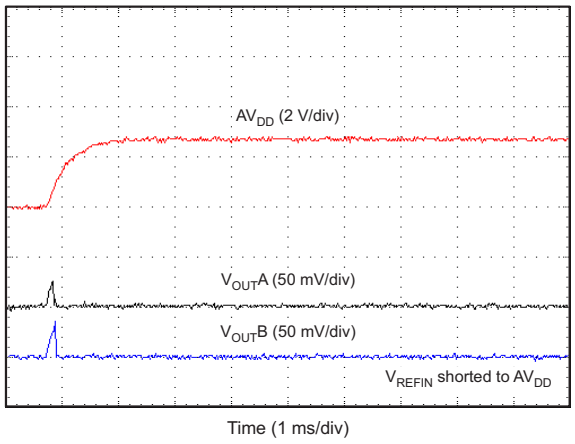


Figure 85. Power-On Glitch, Reset to Zero Scale

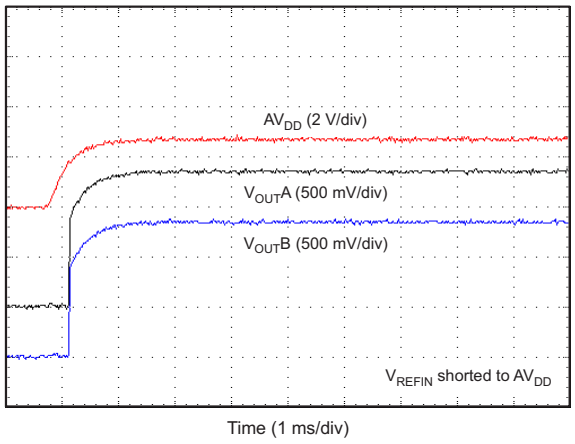


Figure 86. Power-On Glitch, Reset to Midscale

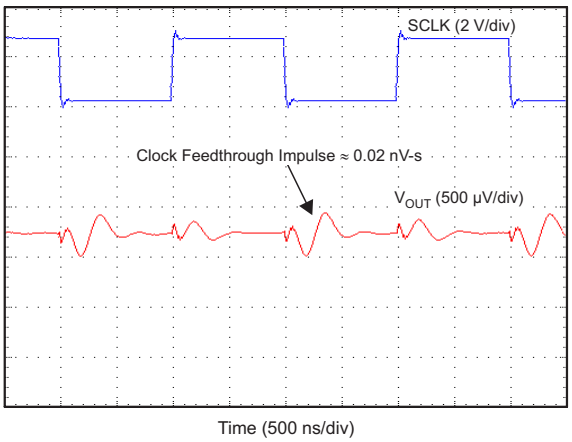


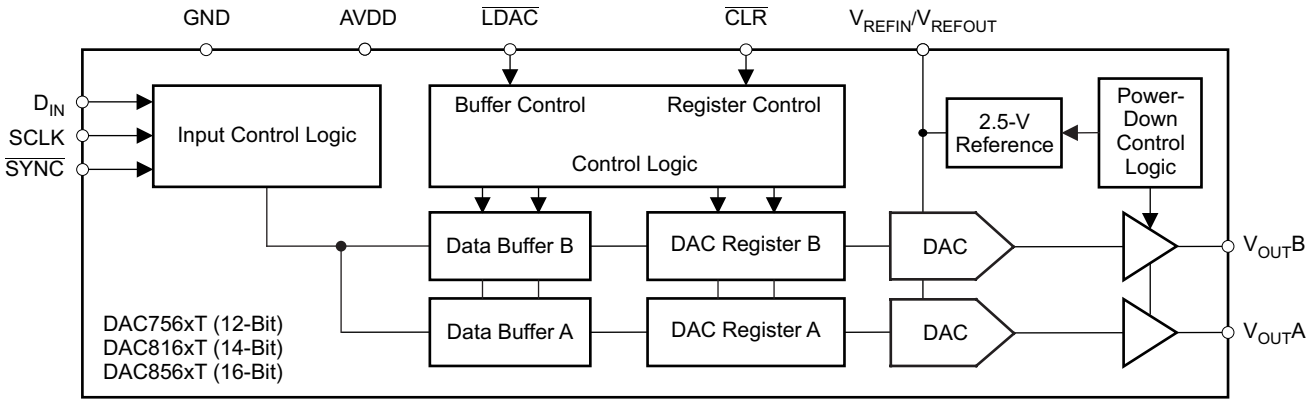
Figure 87. Clock Feedthrough, 500 kHz, Midscale

8 Detailed Description

8.1 Overview

The DAC756xT, DAC816xT, and DAC856xT devices are low-power, voltage-output, dual-channel, 16-, 14-, and 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 4-ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V or 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN}/V_{REFOUT} pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC)

The DAC756xT, DAC816xT, and DAC856xT architecture consists of two string DACs, each followed by an output buffer amplifier. The devices include an internal 2.5-V reference with 4-ppm/°C temperature drift performance. Figure 88 shows a principal block diagram of the DAC architecture.

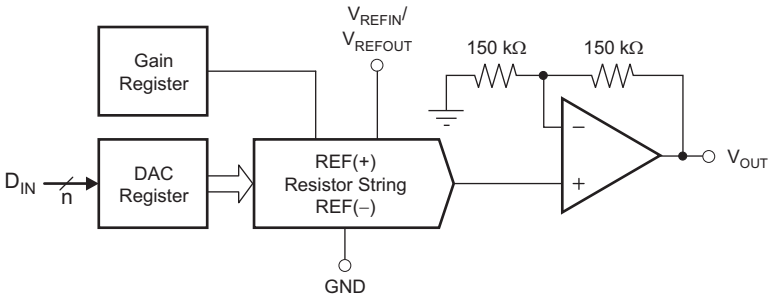


Figure 88. DAC Architecture

The input coding to the DAC756xT, DAC816xT, and DAC856xT devices is straight binary, so the ideal output voltage is given by Equation 1:

$$V_{OUT} = \left(\frac{D_N}{2^n}\right) \times V_{REF} \times Gain \quad (1)$$

where:

- n = resolution in bits; either 12 (DAC756xT), 14 (DAC816xT) or 16 (DAC856xT)
- D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. D_{IN} ranges from 0 to $2^n - 1$.
- V_{REF} = DAC reference voltage; either V_{REFOUT} from the internal 2.5-V reference or V_{REFIN} from an external reference.
- Gain = 1 by default when internal reference is disabled (using external reference), and gain = 2 by default when using internal reference. Gain can also be manually set to either 1 or 2 using the gain register. See the *Gain Function* section for more information.

Feature Description (continued)

8.3.1.1 Resistor String

The resistor string section is shown in Figure 89. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. The resistor string architecture results in monotonicity. The $R_{DIVIDER}$ switch is controlled by the gain registers (see the *Gain Function* section). Because the output amplifier has a gain of 2, $R_{DIVIDER}$ is not shorted when the DAC-n gain is set to 1 (default if internal reference is disabled), and is shorted when the DAC-n gain is set to 2 (default if internal reference is enabled).

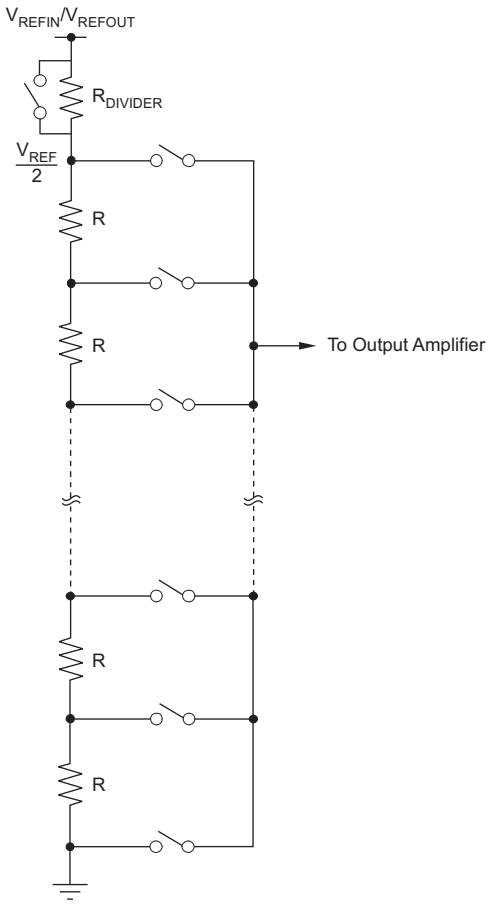


Figure 89. Resistor String

8.3.1.2 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0 V to AV_{DD}. It is capable of driving a load of 2 kΩ in parallel with 3 nF to GND. The typical slew rate is 0.75 V/µs, with a typical full-scale settling time of 14 µs as shown in Figure 31, Figure 32, Figure 75 and Figure 76.

Feature Description (continued)

8.3.2 Internal Reference

The DAC756xT, DAC816xT, and DAC856xT devices include a 2.5-V internal reference that is disabled by default. The internal reference is externally available at the V_{REFIN}/V_{REFOUT} pin. The internal reference output voltage is 2.5 V and can sink and source up to 20 mA.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC756xT, DAC816xT, and DAC856xT devices is a bipolar transistor-based precision band-gap voltage reference. Figure 90 shows the basic band-gap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} - V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is amplified and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100 mA.

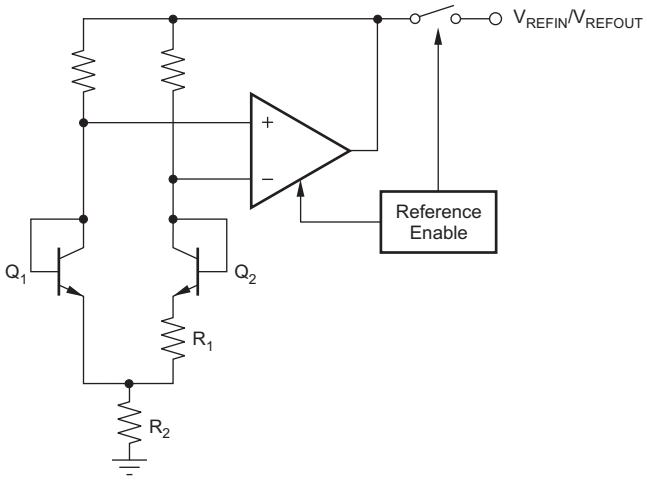


Figure 90. Band-Gap Reference Simplified Schematic

8.3.3 Power-On Reset

8.3.3.1 Power-On Reset to Zero-Scale

The DAC7562T, DAC8162T, and DAC8562T devices contain a power-on-reset circuit that controls the output voltage during power up. All device registers are reset as shown in Table 4. At power up, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before applying power to the device. The internal reference is disabled by default and remains that way until a valid reference-change command is executed.

8.3.3.2 Power-On Reset to Mid-Scale

The DAC7563T, DAC8163T, and DAC8563T devices contain a power-on reset circuit that controls the output voltage during power up. At power up, all DAC registers are reset to mid-scale code and the output voltages of all DAC channels are set to V_{REFIN} / 2 volts. Each DAC channel remains that way until a valid load command is written to it. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before applying power to the device. The internal reference is powered off or down by default and remains that way until a valid reference-change command is executed. If using an external reference, it is acceptable to power on the V_{REFIN} pin either at the same time as or after applying AV_{DD}.

Table 4. DACxx62T and DACxx63T Power-On Reset Values

REGISTER	DEFAULT SETTING	
DAC and input registers	DACxx62T	Zero-scale
	DACxx63T	Mid-scale
LDAC registers	$\overline{\text{LDAC}}$ pin enabled for both channels	
Power-down registers	DACs powered up	
Internal reference register	Internal reference disabled	
Gain registers	Gain = 1 for both channels	

8.3.3.3 Power-On Reset (POR) Levels

When the device powers up, a POR circuit sets the device in default mode as shown in Table 4. The POR circuit requires specific AV_{DD} levels, as indicated in Figure 91, to ensure discharging of internal capacitors and to reset the device on power up. In order to ensure a power-on reset, AV_{DD} must be below 0.7 V for at least 1 ms. When AV_{DD} drops below 2.2 V but remains above 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, TI recommends a power-on reset. When AV_{DD} remains above 2.2 V, a power-on reset does not occur.

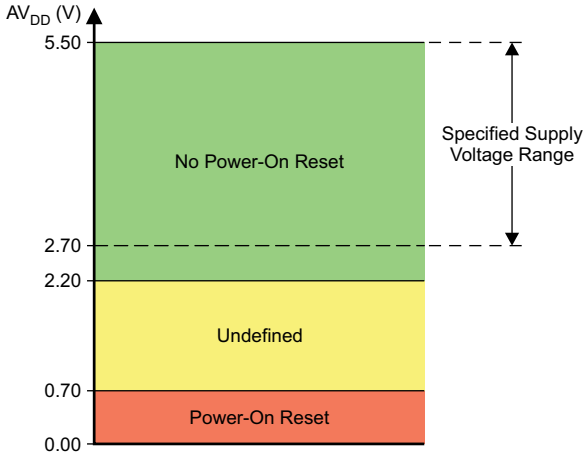


Figure 91. Relevant Voltage Levels for POR Circuit

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The DAC756xT, DAC816xT, and DAC856xT devices have two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. The internal reference is forced to a powered-down state while both DAC channels are powered down, and is only enabled if any DAC channel is also in the normal mode of operation. For more information on the internal reference control, see the *Internal Reference Enable Register* section.

8.4.1.1 DAC Power-Down Commands

The DAC756xT, DAC816xT, and DAC856xT DACs use four modes of operation. These modes are accessed by setting the serial interface command bits to 100. Once the command bits are set correctly, the four different power-down modes are software programmable by setting bits DB5 and DB4 in the shift register. Table 5 and Table 6 show the different power-down options. For more information on how to set the DAC operating mode see Table 17.

Table 5. DAC-n Operating Modes

DB5	DB4	DAC Modes of Operation
0	0	Selected DACs power up (normal mode, default)
0	1	Selected DACs power down, output 1 kΩ to GND
1	0	Selected DACs power down, output 100 kΩ to GND
1	1	Selected DACs power down, output Hi-Z to GND

Table 6. DAC-n Selection for Operating Modes

DAC-B (DB1), DAC-A (DB0)	Operating Mode
0	DAC-n does not change operating mode
1	DAC-n operating mode set to value on PD1 and PD0

It is possible to write to the DAC register or buffer of the DAC channel that is powered down. When the DAC channel is then powered up, it powers up to this new value.

The advantage of the available power-down modes is that the output impedance of the device is known while it is in power-down mode. As described in Table 5, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or open-circuited (Hi-Z). The DAC power-down circuitry is shown in Figure 92.

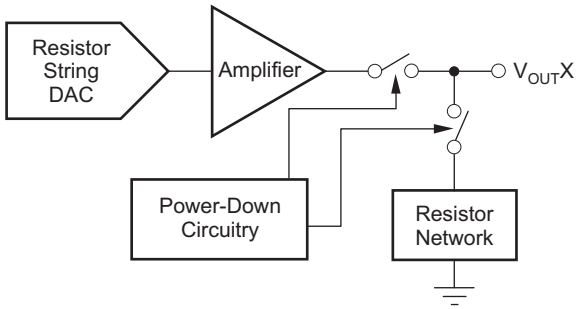


Figure 92. Output Stage

8.4.2 Gain Function

The gain register controls the GAIN setting in the DAC transfer function:

$$V_{OUT} = \left(\frac{D_N}{2^n}\right) \times V_{REF} \times G \quad (2)$$

The DAC756xT, DAC816xT, and DAC856xT devices have a gain register for each channel. The gain for each channel, in Equation 2, is either 1 or 2. This gain is automatically set to 2 when using the internal reference, and is automatically set to 1 when the internal reference is disabled (default). However, each channel can have either gain by setting the registers appropriately. The gain registers are accessible by setting the serial interface command bits to 000, address bits to 010, and using DB1 for DAC-B and DB0 for DAC-A. See Table 7 and Table 17 for the full command structure. The gain registers are automatically reset to provide either gain of 1 or 2 when the internal reference is powered off or on, respectively. After the reference is powered off or on, the gain register is again accessible to change the gain.

Table 7. DAC-n Selection for Gain Register Command

DB1, DB0	Value	Gain
DB0	0	DAC-A uses gain = 2 (default with internal reference)
	1	DAC-A uses gain = 1 (default with external reference)
DB1	0	DAC-B uses gain = 2 (default with internal reference)
	1	DAC-B uses gain = 1 (default with external reference)

8.4.3 Software Reset Function

The DAC756xT, DAC816xT, and DAC856xT devices contain a software reset feature. The software reset function is accessed by setting the serial interface command bits to 101. The software reset command contains two reset modes which are software-programmable by setting bit DB0 in the shift register. Table 8 and Table 17 show the available software reset commands.

Table 8. Software Reset

DB0	Registers Reset to Default Values
0	DAC registers Input registers
1	DAC registers Input registers LDAC registers Power-down registers Internal reference register Gain registers

8.4.4 Internal Reference Enable Register

The internal reference in the DAC756xT, DAC816xT, and DAC856xT devices is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered up and powered down by setting the serial interface command bits to 111 and configuring DB0 (see Table 9). The internal reference is forced to a powered down state while both DAC channels are powered down, and can only be enabled if any DAC channel is in normal mode of operation. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the V_{REFIN}/V_{REFOUT} pin (Hi-Z output).

Table 9. Internal Reference

DB0	Internal Reference Configuration
0	Disable internal reference and reset DACs to gain = 1
1	Enable internal reference and reset DACs to gain = 2

8.4.4.1 Enabling Internal Reference

To enable the internal reference, refer to the command structure in Table 17. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence powers up the internal reference. However, the internal reference is forced to a disabled state while both DAC channels are powered down, and remains disabled until either DAC channel is returned to the normal mode of operation. See *DAC Power-Down Commands* for more information on DAC channel modes of operation.

8.4.4.2 Disabling Internal Reference

To disable the internal reference, refer to the command structure in Table 17. When performing a power cycle to reset the device, the internal reference is disabled (default mode).

8.4.5 CLR Functionality

The edge-triggered $\overline{\text{CLR}}$ pin can be used to set the input and DAC registers immediately according to Table 10. When the $\overline{\text{CLR}}$ pin receives a falling edge signal the clear mode is activated and changes the DAC output voltages accordingly. The device exits clear mode on the 24th falling edge of the next write to the device. If the $\overline{\text{CLR}}$ pin receives a falling edge signal during a write sequence in normal operation, the clear mode is activated and changes the input and DAC registers immediately according to Table 10.

Table 10. Clear Mode Reset Values

DEVICE	DAC Output Entering Clear Mode
DAC8562T, DAC8162T, DAC7562T	Zero-scale
DAC8563T, DAC8163T, DAC7563T	Mid-scale

8.4.6 LDAC Functionality

The DAC756xT, DAC816xT, and DAC856xT devices offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC756xT, DAC816xT, and DAC856xT data updates can be performed either in *synchronous* or in *asynchronous* mode.

In *asynchronous* mode, the $\overline{\text{LDAC}}$ pin is used as a negative edge-triggered timing signal for simultaneous DAC updates. Multiple single-channel writes can be done in order to set different channel buffers to desired values and then make a falling edge on $\overline{\text{LDAC}}$ pin to simultaneously update the DAC output registers. Data buffers of all channels must be loaded with desired data before an $\overline{\text{LDAC}}$ falling edge. After a high-to-low $\overline{\text{LDAC}}$ transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ pin is triggered. $\overline{\text{LDAC}}$ must be returned high before the next serial command is initiated.

In *synchronous* mode, data are updated with the falling edge of the 24th SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such *synchronous* updates, the $\overline{\text{LDAC}}$ pin is not required, and it must be connected to GND permanently or asserted and held low before sending commands to the device.

Alternatively, all DAC outputs can be updated simultaneously using the built-in software function of LDAC. The LDAC register offers additional flexibility and control by allowing the selection of which DAC channel(s) should be updated simultaneously when the $\overline{\text{LDAC}}$ pin is being brought low. The LDAC register is loaded with a 2-bit word (DB1 and DB0) using command bits C2, C1, and C0 (see Table 17). The default value for each bit, and therefore for each DAC channel, is zero. If the LDAC register bit is set to 1, it overrides the $\overline{\text{LDAC}}$ pin (the $\overline{\text{LDAC}}$ pin is internally tied low for that particular DAC channel) and this DAC channel updates synchronously after the falling edge of the 24th SCLK cycle. However, if the LDAC register bit is set to 0, the DAC channel is controlled by the $\overline{\text{LDAC}}$ pin.

The combination of software and hardware simultaneous update functions is particularly useful in applications when updating a DAC channel, while keeping the other channel unaffected; see Table 11 and Table 17 for more information.

Table 11. DAC-n Selection for LDAC Register Command

DB1, DB0	Value	$\overline{\text{LDAC}}$ Pin Functionality
DB0	0	DAC-A uses $\overline{\text{LDAC}}$ pin
	1	DAC-A operates in synchronous mode
DB1	0	DAC-B uses $\overline{\text{LDAC}}$ pin
	1	DAC-B operates in synchronous mode

8.5 Programming

The DAC756xT, DAC816xT, and DAC856xT devices have a three-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}; see the table) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram (Figure 1) for an example of a typical write sequence.

The DAC756xT, DAC816xT, or DAC856xT input shift register is 24 bits wide, consisting of two *don't care* bits (DB23 to DB22), three command bits (DB21 to DB19), three address bits (DB18 to DB16), and 16 data bits (DB15 to DB0). All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register. DB23 is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register, and any further clocking of data is ignored.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the DAC756xT, DAC816xT, and DAC856xT devices compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data.

After receiving the 24th falling clock edge, the DAC756xT, DAC816xT, and DAC856xT devices decode the three command bits, three address bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept low or brought high. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to begin the next cycle properly; see the Serial Write Operation timing diagram (Figure 1).

A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. A new write sequence starts at the next falling edge of $\overline{SYNC}$. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible.

8.5.1 $\overline{SYNC}$ Interrupt

In a normal write sequence, the $\overline{SYNC}$ line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24th falling edge. However, if $\overline{SYNC}$ is brought high before the 23rd falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 93).

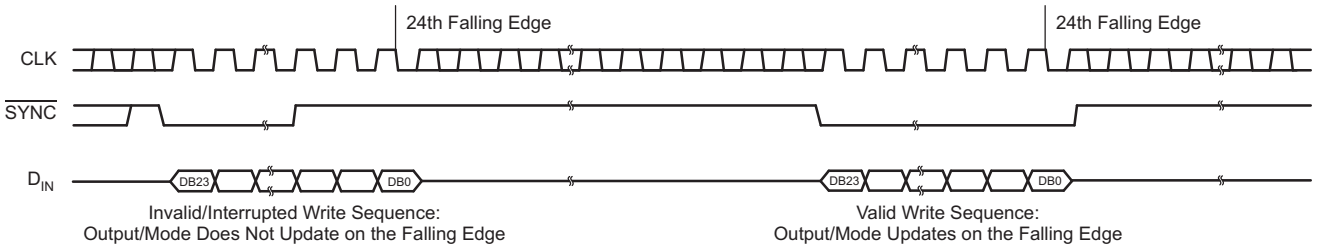


Figure 93. $\overline{SYNC}$ Interrupt Facility

Programming (continued)

8.5.2 DAC Register Configuration

When the DAC registers are being written to, the DAC756xT, DAC816xT, and DAC856xT devices receive all 24 bits of data, ignore DB23 and DB22, and decode the next three bits (DB21 to DB19) in order to determine the DAC operating or control mode (see Table 12). Bits DB18 to DB16 are used to address the DAC channels (see Table 13).

Table 12. Commands for the DAC756xT, DAC816xT, and DAC856xT Devices

C2 (DB21)	C1 (DB20)	C0 (DB19)	Command
0	0	0	Write to input register n (Table 13)
0	0	1	Software LDAC, update DAC register n (Table 13)
0	1	0	Write to input register n (Table 13) and update all DAC registers
0	1	1	Write to input register n and update DAC register n (Table 13)
1	0	0	Set DAC power up or -down mode
1	0	1	Software reset
1	1	0	Set LDAC registers
1	1	1	Enable or disable the internal reference

Table 13. Address Select for the DAC756xT, DAC816xT, and DAC856xT Devices

A2 (DB18)	A1 (DB17)	A0 (DB16)	Channel (n)
0	0	0	DAC-A
0	0	1	DAC-B
0	1	0	Gain (only use with command 000)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	DAC-A and DAC-B

When writing to the DAC input registers the next 16, 14, or 12 bits of data that follow are decoded by the DAC to determine the equivalent analog output (see Table 14 through Table 16) . The data format is straight binary, with all 0s corresponding to 0-V output and all 1s corresponding to full-scale output. For all documentation purposes, the data format and representation used here is a true 16-bit pattern (that is, FFFFh data word for full scale) that the DAC756xT, DAC816xT, and DAC856xT devices require.

Table 14. DAC856xT Data Input Register Format

		COMMAND			ADDRESS			DATA															
X(1)	X	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DB23																							DB0

(1) *X* denotes *don't care* bits.

Table 15. DAC816xT Data Input Register Format

		COMMAND			ADDRESS			DATA															
X	X	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
DB23																							DB0

Table 16. DAC756xT Data Input Register Format

		COMMAND			ADDRESS			DATA															
X	X	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
DB23																							DB0

In additon to DAC input register updates, the DAC756xT, DAC816xT, and DAC856xT devices support a number of functional mode commands (such as write to LDAC register, power down DACs and so on). The complete set of functional mode commands is shown in Table 17.

Table 17. Command Matrix for the DAC756xT, DAC816xT, and DAC856xT Devices

DB23-DB22	Command			Address			Data						DESCRIPTION
	C2	C1	C0	A2	A1	A0	DB15-DB6	DB5	DB4	DB3-DB2	DB1	DB0	
X(1)	0	0	0	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input registers
X	0	1	0	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register and update all DACs
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register and update all DACs
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	1	1	0	0	0	16-, 14-, or 12-bit DAC data						Write to DAC-A input register and update DAC-A
				0	0	1	16-, 14-, or 12-bit DAC data						Write to DAC-B input register and update DAC-B
				1	1	1	16-, 14-, or 12-bit DAC data						Write to DAC-A and DAC-B input register and update all DACs
X	0	0	1	0	0	0	X						Update DAC-A
				0	0	1	X						Update DAC-B
				1	1	1	X						Update all DACs
X	0	0	0	0	1	0	X				0	0	Gain: DAC-B gain = 2, DAC-A gain = 2 (default with internal V_{REF})
											0	1	Gain: DAC-B gain = 2, DAC-A gain = 1
											1	0	Gain: DAC-B gain = 1, DAC-A gain = 2
											1	1	Gain: DAC-B gain = 1, DAC-A gain = 1 (power-on default)
X	1	0	0	X			X	0	0	X	0	1	Power up DAC-A
											1	0	Power up DAC-B
											1	1	Power up DAC-A and DAC-B
X	1	0	0	X			X	0	1	X	0	1	Power down DAC-A; 1 kΩ to GND
											1	0	Power down DAC-B; 1 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 1 kΩ to GND
X	1	0	0	X			X	1	0	X	0	1	Power down DAC-A; 100 kΩ to GND
											1	0	Power down DAC-B; 100 kΩ to GND
											1	1	Power down DAC-A and DAC-B; 100 kΩ to GND
X	1	0	0	X			X	1	1	X	0	1	Power down DAC-A; Hi-Z
											1	0	Power down DAC-B; Hi-Z
											1	1	Power down DAC-A and DAC-B; Hi-Z
X	1	0	1	X			X				X	0	Reset DAC-A and DAC-B input register and update all DACs
											X	1	Reset all registers and update all DACs (Power-on-reset update)
X	1	1	0	X			X				0	0	$\overline{\text{LDAC}}$ pin active for DAC-B and DAC-A
											0	1	$\overline{\text{LDAC}}$ pin active for DAC-B; inactive for DAC-A
											1	0	$\overline{\text{LDAC}}$ pin inactive for DAC-B; active for DAC-A
											1	1	$\overline{\text{LDAC}}$ pin inactive for DAC-B and DAC-A
X	1	1	1	X			X				X	0	Disable internal reference and reset DACs to gain = 1
											X	1	Enable internal reference and reset DACs to gain = 2

(1) *X* denotes *don't care* bits.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DAC Internal Reference

The internal reference of the DAC756xT, DAC816xT, and DAC856xT devices does not require an external load capacitor for stability because it is stable without any capacitive load. However, for improved noise performance, an external load capacitor of 150 nF or larger connected to the V_{REFIN}/V_{REFOUT} output is recommended. Figure 94 shows the typical connections required for operation of the DAC756xT, DAC816xT, and DAC856xT internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

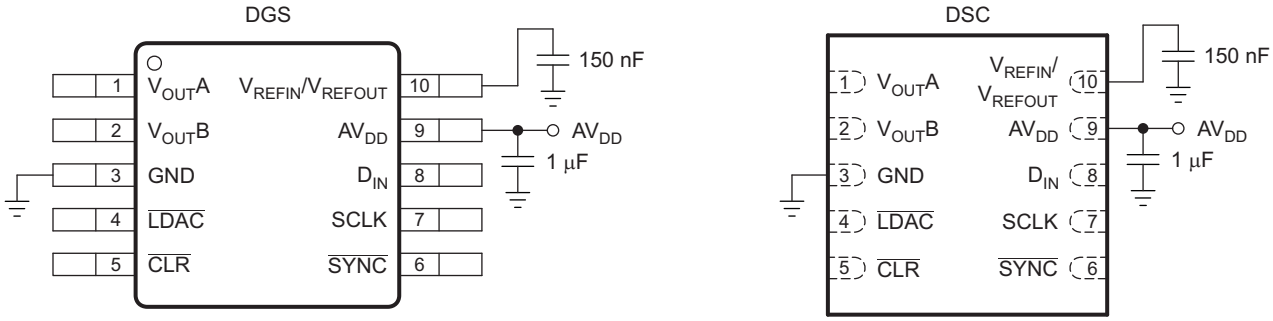


Figure 94. Typical Connections for Operating the DAC756xT, DAC816xT, and DAC856xT Internal Reference

9.1.1.1 Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5 mV above the reference output voltage in an unloaded condition. For loaded conditions, see the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7 V to 5.5 V, the variation at V_{REFIN}/V_{REFOUT} is typically 50 µV/V; see Figure 7.

9.1.1.2 Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the box method described by Equation 3:

$$\left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}}\right) \times 10^{6} \left(\frac{ppm}{°C}\right) \quad (3)$$

where:

- V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.
- V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.
- V_{REF} = 2.5 V, target value for reference output voltage.
- T_{RANGE} = the characterized range from –40°C to 125°C (165°C range)

The internal reference features an exceptional typical drift coefficient of 4 ppm/°C from –40°C to 125°C. Characterizing a large number of units, a maximum drift coefficient of 10 ppm/°C is observed. Temperature drift results are summarized in Figure 3.

Application Information (continued)

9.1.1.3 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise and noise spectral density performance are listed in the *Electrical Characteristics*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at the V_{REFIN}/V_{REFOUT} pin, both unloaded and with an external 4.7-µF load capacitor, is shown in Figure 6. Internal reference noise impacts the DAC output noise when the internal reference is used.

9.1.1.4 Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 95. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are shown in Figure 4. Force and sense lines should be used for applications that require improved load regulation.

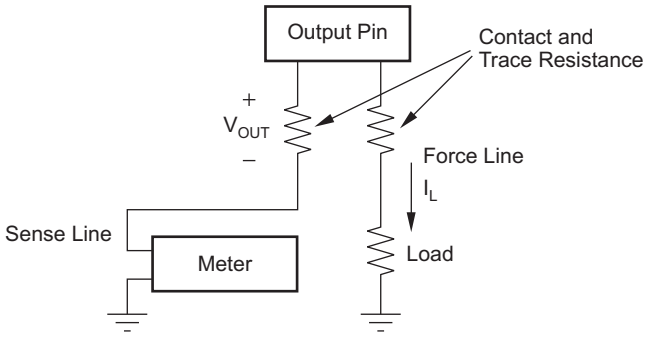


Figure 95. Accurate Load Regulation of the DAC756xT, DAC816xT, and DAC856xT Internal Reference

9.1.1.4.1 Long-Term Stability

Long-term stability or aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses. The typical drift value for the internal reference is listed in the *Electrical Charateristics* and measurement results are shown in Figure 5. This parameter is characterized by powering up multiple devices and measuring them at regular intervals.

9.1.1.5 Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at 25°C, cycling the device through the operating temperature range, and returning to 25°C. Hysteresis is expressed by Equation 4:

$$V_{HYST} = \left[\frac{V_{REF\_PRE} - V_{REF\_POST}}{V_{REF\_NOM}} \right] \times 10^6 (ppm/°C) \quad (4)$$

where:

- V_{HYST} = thermal hysteresis.
- V_{REF_PRE} = output voltage measured at 25°C pre-temperature cycling.
- V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to 125°C, and returns to 25°C.
- V_{REF_NOM} = 2.5 V, target value for reference output voltage.

9.1.2 DAC Noise Performance

Output noise spectral density at the V_{OUT}-n pin versus frequency is depicted in Figure 45 and Figure 46 for full-scale, mid-scale, and zero-scale input codes. The typical noise density for mid-scale code is 90 nV/√Hz at 1 kHz. High-frequency noise can be improved by filtering the reference noise. Integrated output noise between 0.1 Hz and 10 Hz is close to 2.5 μV_{PP} (mid-scale), as shown in Figure 47.

9.2 Typical Applications

9.2.1 Combined Voltage and Current Analog Output Module Using the XTR300

The design features two independent outputs that can source and sink voltage and current over the standard industrial output ranges. The possible outputs of the design include: –24 mA to 24 mA, 4 mA–20 mA, 0 mA to 24 mA, 0 V to 5 V, 0 V to 10 V, –5 V to5 V, and –10 V to 10 V.

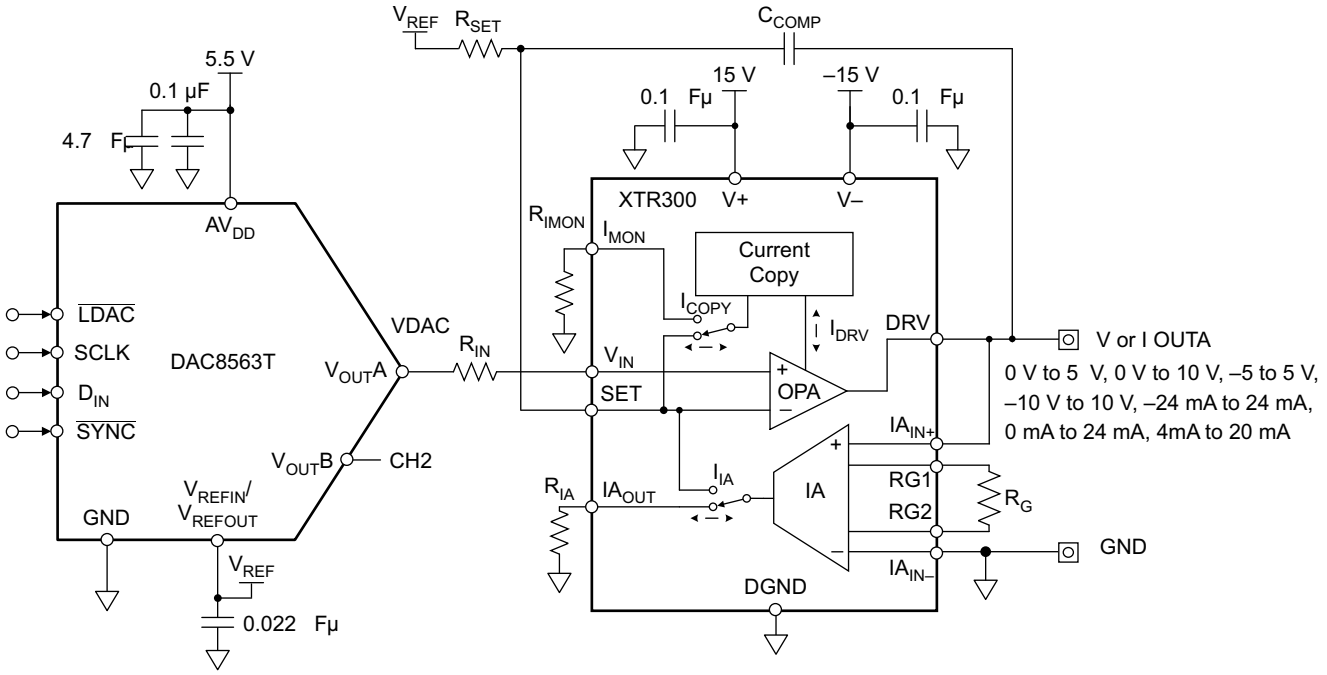


Figure 96. DAC8563T and XTR300 Discrete Analog Output Module

9.2.1.1 Design Requirements

The design uses a DAC and a current-or-voltage output driver to create a discrete analog output design that can output either voltage or current from the same pin while focusing on high-accuracy specifications. The choice of the DAC8563T device takes advantage of its 16-bit resolution as well as its low typical offset error of 1 mV and gain error of 0.01% FSR. The choice of the XTR300 device is based on its strong dc performance, having a typical error of 400 µV and 0.04% FSR gain error. The XTR300 device allows a variety of both current and voltage outputs on the same pin while providing load monitoring and error status pins.

The power-on reset-to-midscale feature of the DAC8563T makes the bipolar output of the XTR300 power up at 0 V or 0 A. If using a unipolar output, the recommended device to achieve a system power-on output of 0 V, 0 A or 4 mA is the DAC8562T device.

A recommendation for minimizing the introduction of errors into the system is to use ±0.01% tolerance RG and RSET resistors. The bypass capacitors on AV_{DD}, VREF, V+ and V– should have values between 100 nF and 10 µF. Smaller capacitors filter fast low-energy transients, whereas the large capacitors filter the slow high-energy transients. If there is an expectation of both types of signals in the system, the recommendation is to use a pair of small and large values as shown on the AV_{DD} pin of the DAC8563T device in Figure 96.

9.2.1.2 Detailed Design Procedure

When configured for voltage mode, the output of the instrumentation amplifier (IA), internal to the XTR300 device, is routed to the SET pin. The SET output provides feedback for the IA based on the IA input voltage. The feedback from the IA provides high-impedance remote sensing of the voltage at the output load. Using the output voltage can overcome errors from PCB traces and protection component impedances. The DAC provides a unipolar input voltage to the VIN pin of the XTR300 device. The XTR300 device offsets the V_{DAC} range by a negative V_{REF} and amplifies the difference by a value set by the R_G and R_{SET} resistors, as shown in Equation 5.

Typical Applications (continued)

$$V_{OUT} = \frac{R_G}{2} \times \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \quad (5)$$

When configured for current mode, the XTR300 routes the internal output of its current copy circuitry to the SET pin. This provides feedback for the internal OPA driver based on 1 / 10th of the output current, resulting in a voltage-to-current transfer function. Generating bipolar current outputs from the single-ended DAC output voltage, VDAC, requires the application of an offset to the XTR300 SET pin. Connect the R_{SET} resistor from the SET pin to V_{REF} to apply the offset and obtain the transfer function shown in Equation 6.

$$I_{OUT} = 10 \times \left(\frac{V_{DAC} - V_{REF}}{R_{SET}} \right) \quad (6)$$

The desired output ranges for VDAC and V_{REF} voltages determine the R_{SET} and R_G resistor values, calculated using Equation 7 and Equation 8. The system design requires a V_{DAC} voltage range of 0.04 V to 4.96 V in order to operate the DAC8563T in the specified linear output range from codes 512 to 65 024.

$$R_{SET} = 10 \times \left(\frac{V_{DAC} - V_{REF}}{I_{OUT}} \right) = 10 \times \left(\frac{4.96\ V - 2.5\ V}{0.024\ A} \right) = 1025\ \Omega \quad (7)$$

$$R_G = \frac{2 \times V_{OUT\_MAX} \times R_{SET}}{V_{DAC} - V_{REF}} = \frac{2 \times 10\ V \times 1020\ \Omega}{4.96\ V - 2.5\ V} = 8292\ \Omega \quad (8)$$

I_{MON} and IA_{OUT} accomplish load monitoring. The sizing of R_{IMON} and R_{IA} determine the monitoring output voltage across the resistors. Size the resistors according to Equation 9 and Equation 10 and the expected output load current I_{DRV}.

$$R_{IMON} = \frac{10 \times V_{IMON}}{I_{DRV}} \quad (9)$$

$$R_{IA} = \frac{10 \times V_{IA}}{I_{IA}} \quad (10)$$

For more detailed information about the design procedure of this circuit and how to isolate it, see *Two-Channel Source/Sink Combined Voltage & Current Output, Isolated, EMC/EMI Tested Reference Design* (TIDU434).

Typical Applications (continued)

9.2.1.3 Application Curves

Figure 97 shows the transfer function for the bipolar ±10 V voltage range. This design also supports output voltage ranges of 0–5 V, 0–10 V and ±5 V. Figure 98 shows the transfer function for the unipolar 0–24 mA current range. This design also supports output current ranges of ±24 mA and 4 mA–20 mA.

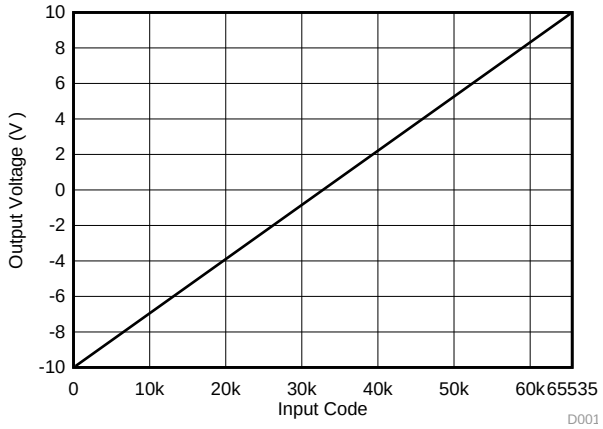


Figure 97. Output Voltage vs Input Code

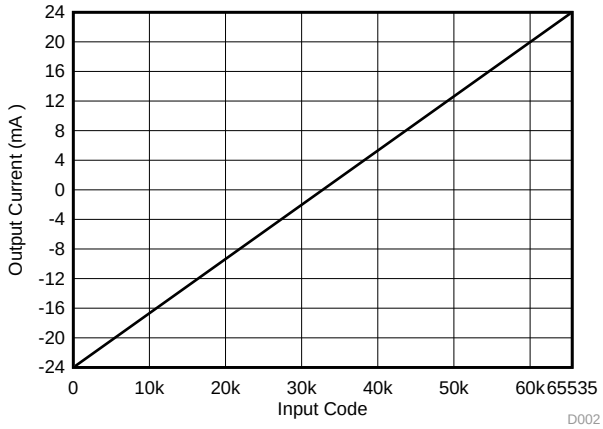


Figure 98. Output Current vs Input Code

Typical Applications (continued)

9.2.2 Up to ±15-V Bipolar Output Using the DAC8562T

The DAC8562T is designed to be operate from a single power supply providing a maximum output range of AV_{DD} volts. However, the DAC can be placed in the configuration shown in Figure 99 in order to be designed into bipolar systems. Depending on the ratio of the resistor values, the output of the circuit can range anywhere from ±5 V to ±15 V. The design example below shows that the DAC is configured to have its internal reference enabled and the DAC8562T internal gain set to 2, however, an external 2.5-V reference could also be used (with DAC8562T internal gain set to 2).

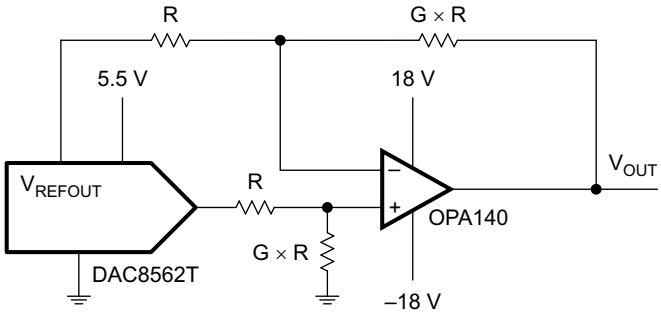


Figure 99. Bipolar Output Range Circuit Using DAC8562T

The transfer function shown in Equation 11 can be used to calculate the output voltage as a function of the DAC code, reference voltage and resistor ratio:

$$V_{OUT} = G \times V_{REFOUT}\left(2 \times \frac{D_{IN}}{65{,}536} - 1\right) \tag{11}$$

where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register, ranging from 0 to 65,535 for DAC8562T (16 bit).

V_{REFOUT} = reference output voltage with the internal reference enabled from the DAC V_{REFIN}/V_{REFOUT} pin

G = ratio of the resistors

An example configuration to generate a ±10-V output range is shown below in Equation 6 with G = 4 and V_{REFOUT} = 2.5 V:

$$V_{OUT} = 20 \times \frac{D_{IN}}{65{,}536} - 10\ V \tag{12}$$

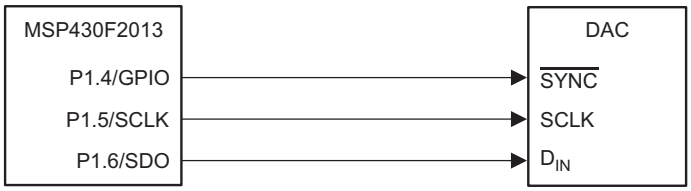
In this example, the range is set to ±10 V by using a resistor ratio of four, V_{REFOUT} of 2.5 V, and DAC8562T internal gain of 2. The resistor sizes must be selected keeping in mind the current sink or source capability of the DAC8562T internal reference. Using larger resistor values, for example, R = 10 kΩ or larger, is recommended. The operational amplifier is selectable depending on the requirements of the system.

The DAC8562TEVM and DAC7562TEVM boards have the option to evaluate the bipolar output application by installing the components on the pre-placed footprints. For more information see either the DAC8562EVM or DAC7562EVM product folder.

9.3 System Examples

9.3.1 MSP430 Microprocessor Interfacing

Figure 100 shows a serial interface between the DAC756xT, DAC816xT, or DAC856xT device and a typical MSP430 USI port such as the one found on the MSP430F2013. The port is configured in SPI master mode by setting bits 3, 5, 6, and 7 in USICTL0. The USI counter interrupt is set in USICTL1 to provide an efficient means of SPI communication with minimal software overhead. The serial clock polarity, source, and speed are controlled by settings in the USI clock control register (USICKCTL). The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on port 1; in this case, port line P1.4 is used. When data are to be transmitted to the DAC756xT, DAC816xT, or DAC856xT device, P1.4 is taken low. The USI transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P1.4 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P1.4 is taken high following the completion of the third write cycle.

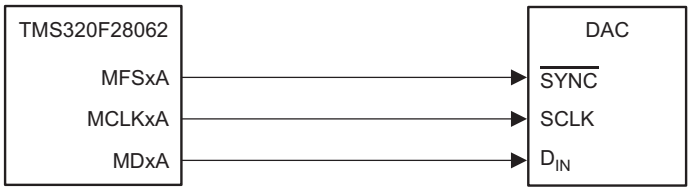


NOTE: Additional pins omitted for clarity.

Figure 100. DAC756xT, DAC816xT, or DAC856xT Device to MSP430 Interface

9.3.2 TMS320 McBSP Microprocessor Interfacing

Figure 101 shows an interface between the DAC756xT, DAC816xT, or DAC856xT device and any TMS320 series DSP from Texas Instruments with a multi-channel buffered serial port (McBSP). Serial data are shifted out on the rising edge of the serial clock and are clocked into the DAC756xT, DAC816xT, or DAC856xT device on the falling edge of the SCLK signal.

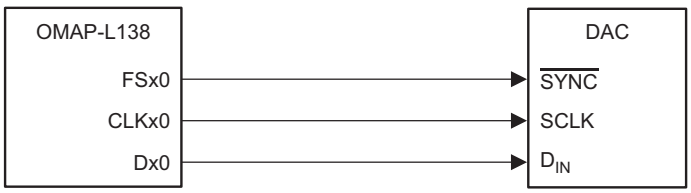


NOTE: Additional pins omitted for clarity.

Figure 101. DAC756xT, DAC816xT, or DAC856xT Device to TMS320 McBSP Interface

9.3.3 OMAP-L1x Processor Interfacing

Figure 102 shows a serial interface between the DAC756xT, DAC816xT, or DAC856xT device and the OMAP-L138 processor. The transmit clock CLKx0 of the L138 drives SCLK of the DAC756xT, DAC816xT, or DAC856xT device, and the data transmit (Dx0) output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from the frame sync transmit (FSx0) line, similar to the TMS320 interface.



NOTE: Additional pins omitted for clarity.

Figure 102. DAC756xT, DAC816xT, or DAC856xT Device to OMAP-L1x Processor

10 Power Supply Recommendations

These devices can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AV_{DD} should be well-regulated and low-noise. In order to further minimize noise from the power supplies, a strong recommendation is to include a pair of 100-pF and 1-nF capacitors and a 0.1-µF to 1-µF bypass capacitor. The current consumption of the AV_{DD} pin, the short-circuit current limit, and the load current for these devices are listed in the *Electrical Characteristics* table. Choose the power supplies for these devices to meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC756xT, DAC816xT, and DAC856xT devices offer single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. As a result of the single ground pin of the DAC756xT, DAC816xT, and DAC856xT devices, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system. The power applied to AV_{DD} should be well-regulated and low noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, AV_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a pair of 100-pF to 1-nF capacitors and a 0.1-µF to 1-µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed essentially to provide low-pass filtering for the supply and remove the high-frequency noise.

11.2 Layout Example

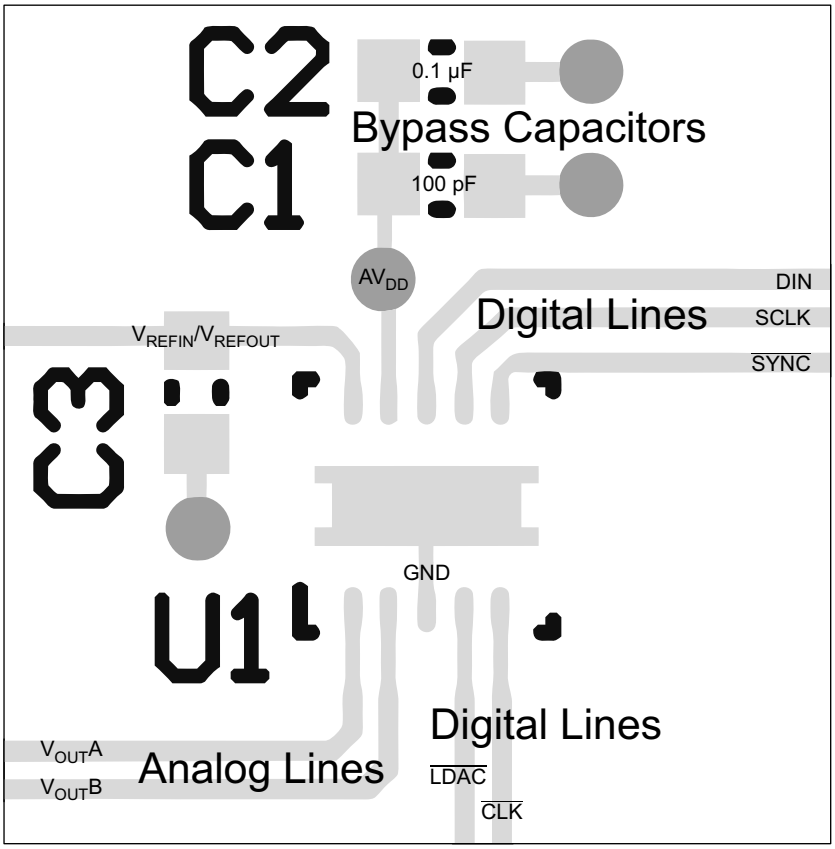


Figure 103. DACxx6xT Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 18. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC7562T	Click here	Click here	Click here	Click here	Click here
DAC7563T	Click here	Click here	Click here	Click here	Click here
DAC8162T	Click here	Click here	Click here	Click here	Click here
DAC8163T	Click here	Click here	Click here	Click here	Click here
DAC8562T	Click here	Click here	Click here	Click here	Click here
DAC8563T	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

SPI, QSPI are trademarks of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7562TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75T2	Samples
DAC7562TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75T2	Samples
DAC7562TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562T	Samples
DAC7562TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7562T	Samples
DAC7563TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75T3	Samples
DAC7563TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75T3	Samples
DAC7563TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7563T	Samples
DAC7563TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7563T	Samples
DAC8162TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81T2	Samples
DAC8162TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81T2	Samples
DAC8162TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162T	Samples
DAC8162TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8162T	Samples
DAC8163TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81T3	Samples
DAC8163TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	81T3	Samples
DAC8163TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163T	Samples
DAC8163TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8163T	Samples
DAC8562TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	85T2	Samples
DAC8562TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	85T2	Samples
DAC8562TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562T	Samples
DAC8562TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8562T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8563TDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	85T3	Samples
DAC8563TDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	85T3	Samples
DAC8563TDSCR	ACTIVE	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563T	Samples
DAC8563TDSCT	ACTIVE	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8563T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

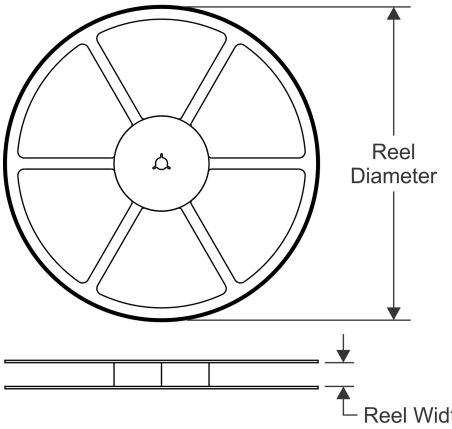
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

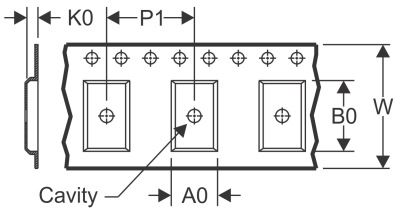
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

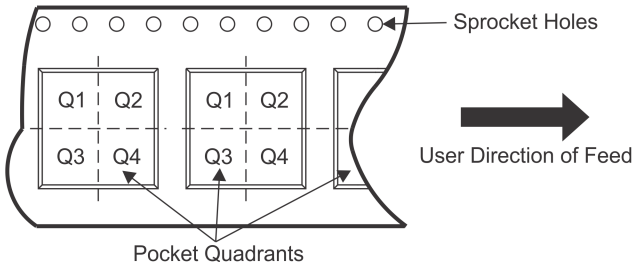


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

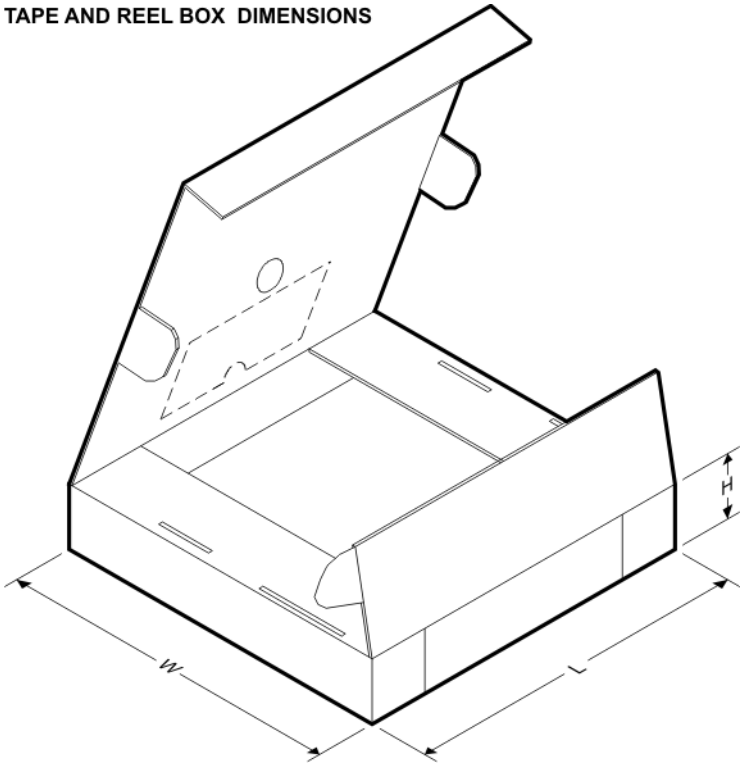


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7562TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7562TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7562TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7562TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7563TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC7563TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC7563TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8162TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8162TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8163TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8163TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8163TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8562TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8562TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8562TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8563TDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8563TDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
DAC8563TDSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8563TDSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7562TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC7562TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC7562TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC7562TDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC7563TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC7563TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC7563TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC7563TDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8162TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC8162TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC8162TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0

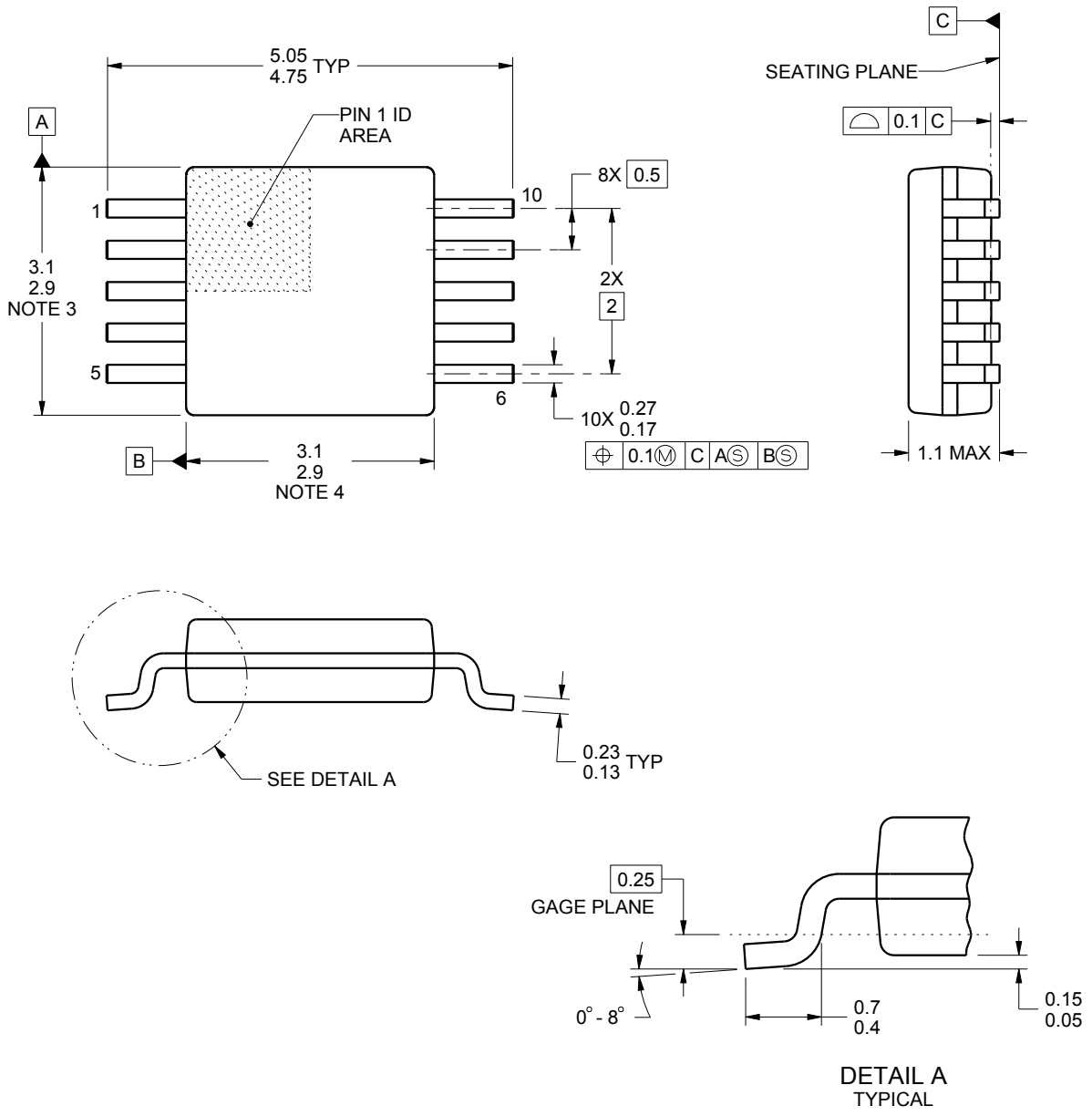
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8162TDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8163TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC8163TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC8163TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8163TDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8562TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC8562TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC8562TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8562TDSCT	WSON	DSC	10	250	210.0	185.0	35.0
DAC8563TDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
DAC8563TDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
DAC8563TDSCR	WSON	DSC	10	3000	367.0	367.0	35.0
DAC8563TDSCT	WSON	DSC	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

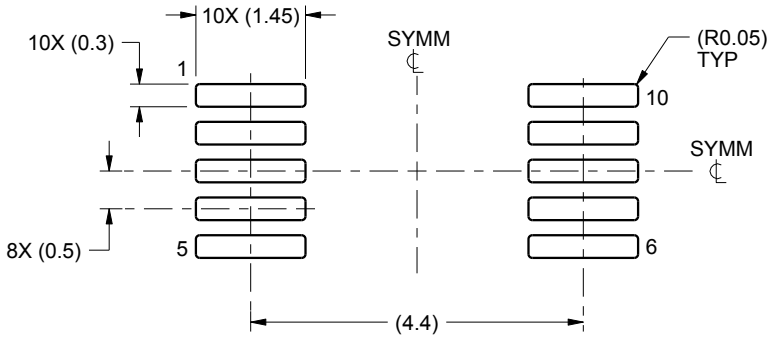
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

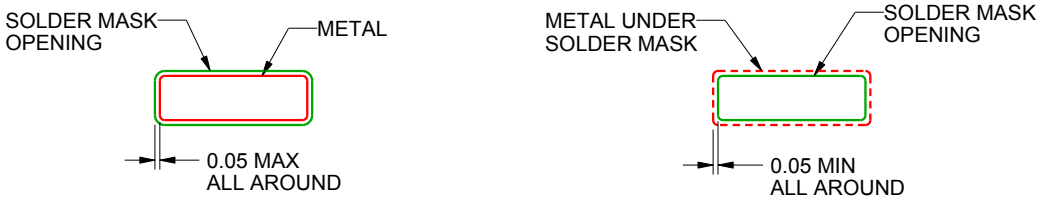


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

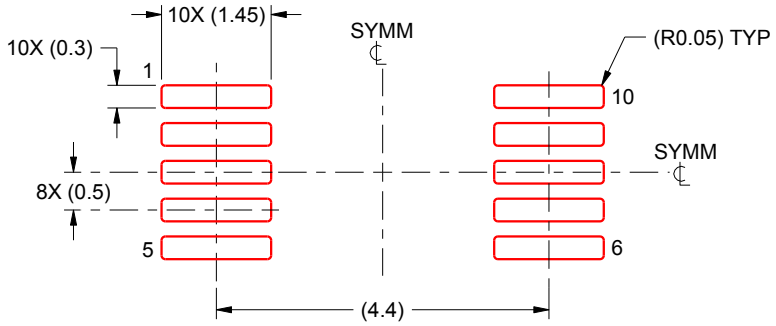


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

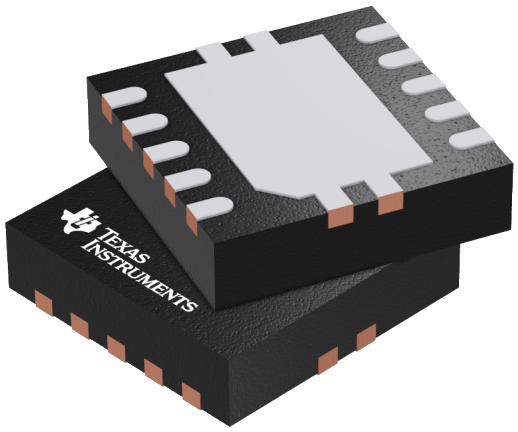
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DSC 10

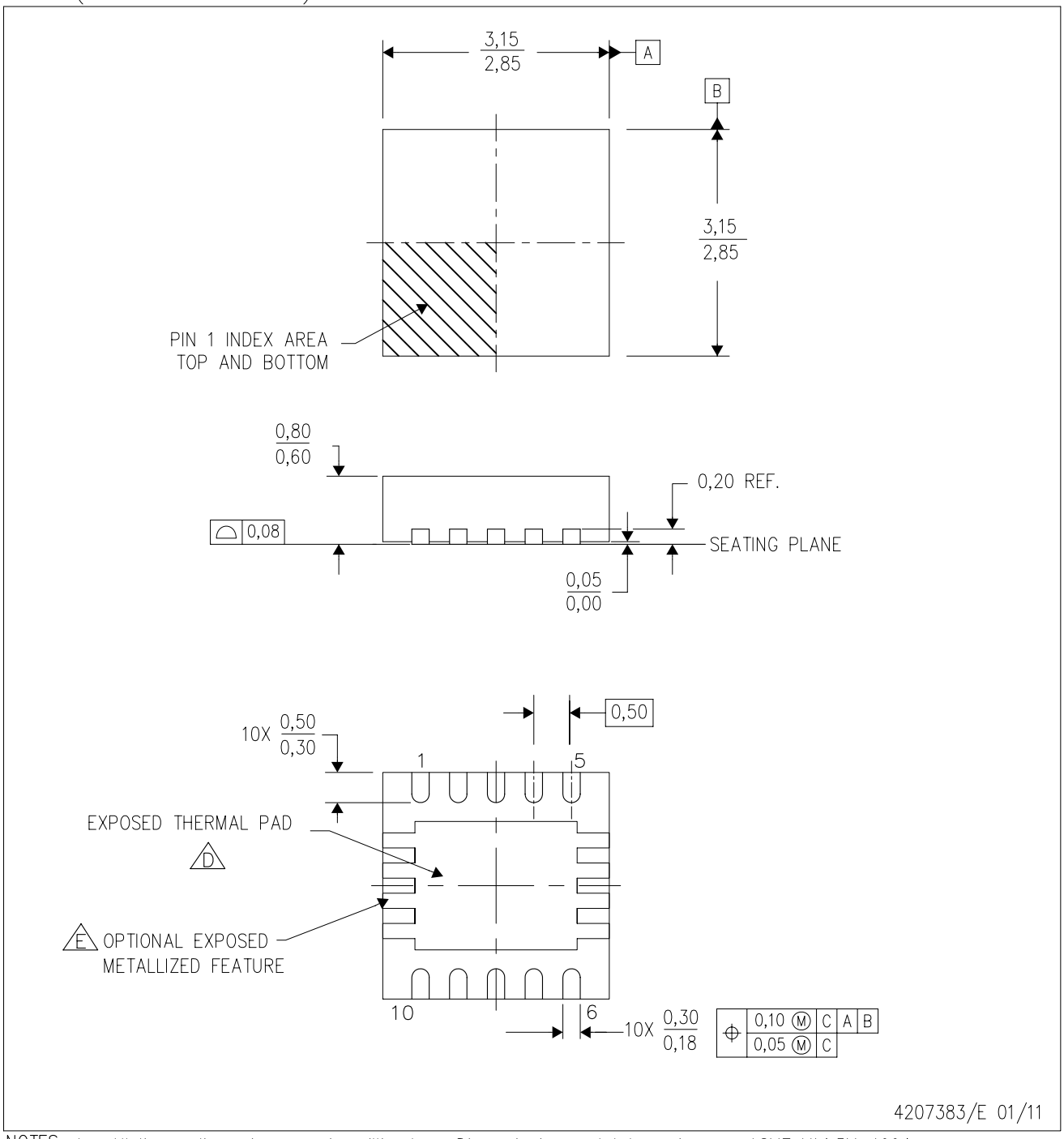
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

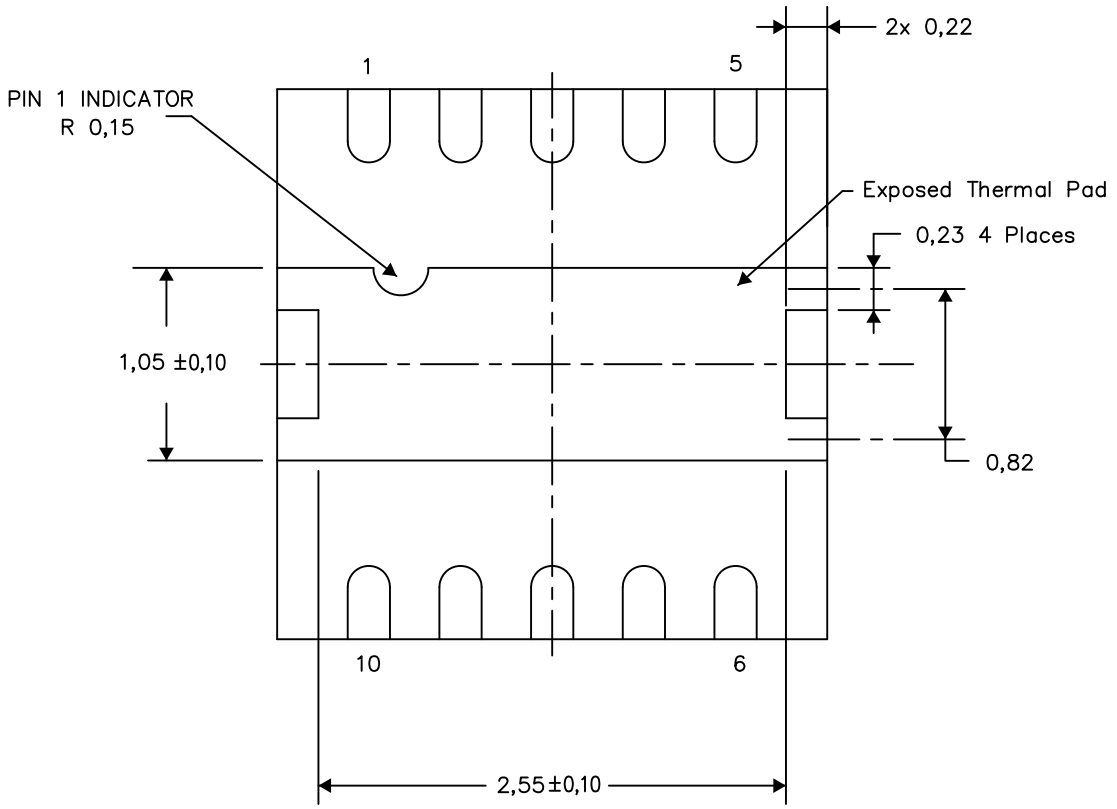
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



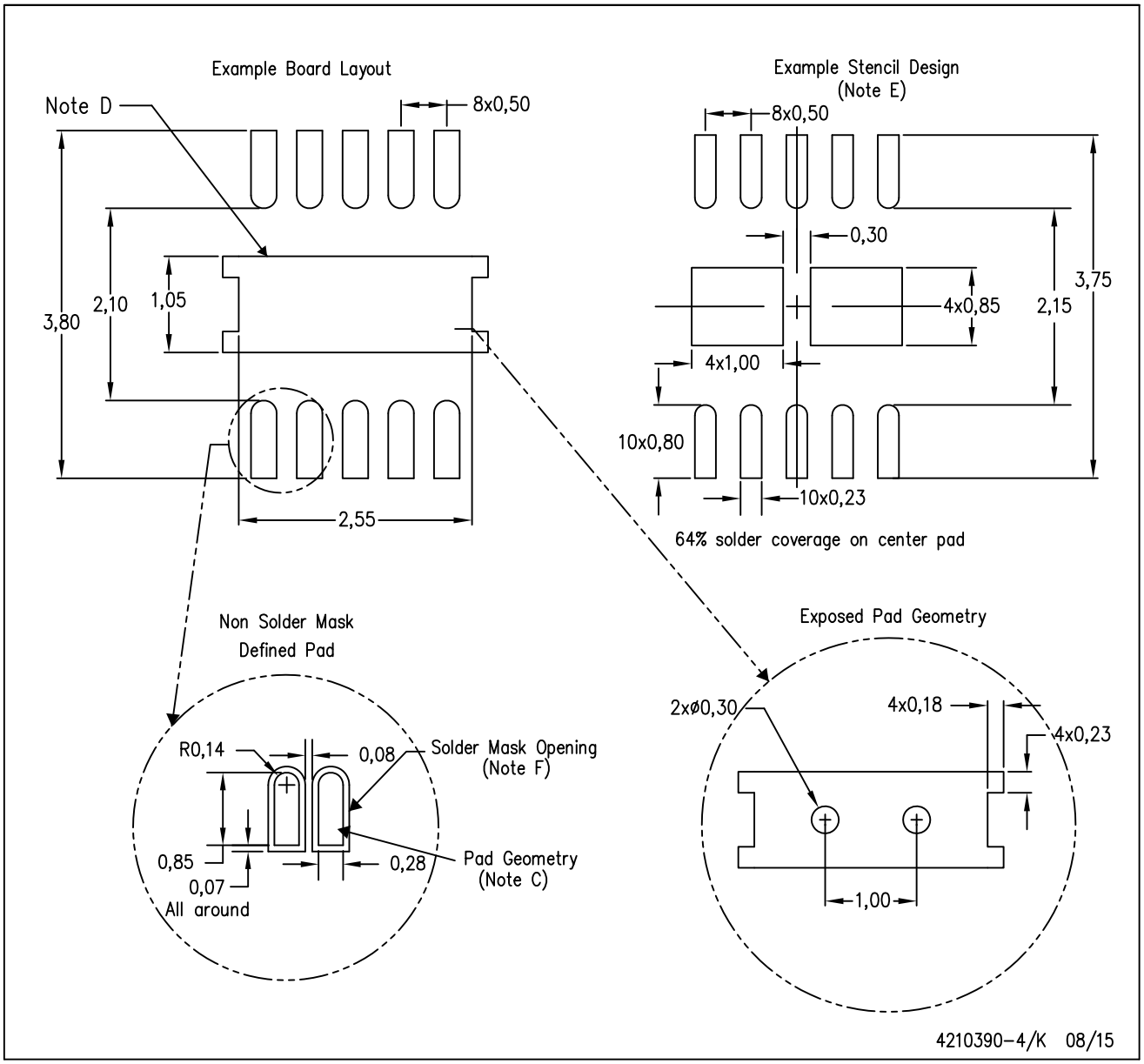
Bottom View

Exposed Thermal Pad Dimensions

4210391–4/Q 08/15

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

12-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER with 2.5V, 2ppm/°C Internal Reference

Check for Samples: DAC7564

FEATURES

- **Relative Accuracy: 0.5LSB**
- **Glitch Energy: 0.15nV-s**
- **Internal Reference:**
  - **2.5V Reference Voltage (enabled by default)**
  - **0.004% Initial Accuracy (typ)**
  - **2ppm/°C Temperature Drift (typ)**
  - **5ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero-Scale**
- **Ultra-Low Power Operation: 1mA at 5V**
- **Wide Power-Supply Range: +2.7V to +5.5V**
- **12-Bit Monotonic Over Temperature Range**
- **Settling Time: 10µs to ±0.024% Full-Scale Range (FSR)**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **1.8V to 5.5V Logic Compatibility**
- **Temperature Range: –40°C to +105°C**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control, PLCs**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

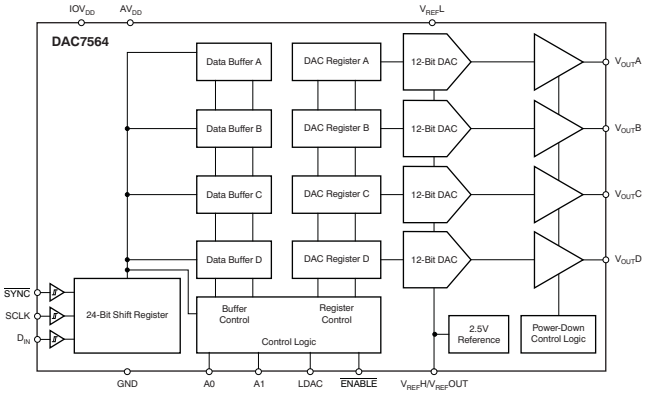
RELATED DEVICES	16-BIT	14-BIT	12-BIT
Pin and Functionally Compatible	DAC8564	DAC8164	DAC7564
Functionally Compatible	DAC8565	DAC8165	DAC7565

DESCRIPTION

The DAC7564 is a low-power, voltage-output, four-channel, 12-bit digital-to-analog converter (DAC). The device includes a 2.5V, 2ppm/°C internal reference (enabled by default), giving a full-scale output voltage range of 2.5V. The internal reference has an initial accuracy of 0.02% and can source up to 20mA at the $V_{REF}H/V_{REF}OUT$ pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC7564 uses a versatile 3-wire serial interface that operates at clock rates up to 50MHz. The interface is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC7564 incorporates a power-on-reset circuit that ensures the DAC output powers up at zero-scale and remains there until a valid code is written to the device. The device contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 1.3µA at 5V. Power consumption is 2.9mW at 3V, reducing to 1.5µW in power-down mode. The low power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment.

The DAC7564 is drop-in and functionally compatible with the DAC8164 and DAC8564, and functionally compatible with the DAC7565, DAC8165 and DAC8565. All these devices are available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI, QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	REFERENCE DRIFT (ppm/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7564A	±1	±0.5	25	TSSOP-16	PW	–40°C to +105°C	DAC7564
DAC7564C	±1	±0.5	5	TSSOP-16	PW	–40°C to +105°C	DAC7564

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		DAC7564	UNIT
AV_{DD} to GND		–0.3 to +6	V
Digital input voltage to GND		–0.3 to $+V_{DD}$ + 0.3	V
V_{OUT} to GND		–0.3 to $+V_{DD}$ + 0.3	V
V_{REF} to GND		–0.3 to $+V_{DD}$ + 0.3	V
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
Junction temperature range (T_J max)		+150	°C
Power dissipation		$(T_J \text{ max} – T_A)/\theta_{JA}$	W
Thermal impedance, θ_{JA}		+118	°C/W
Thermal impedance, θ_{JC}		+29	°C/W
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1500	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER	TEST CONDITIONS		DAC7564 MIN	DAC7564 TYP	DAC7564 MAX	UNIT
STATIC PERFORMANCE(1)						
Resolution			12			Bits
Relative accuracy	Measured by the line passing through codes 30 and 4050	DAC7564A, DAC7564C		±0.5	±1	LSB
Differential nonlinearity	12-bit monotonic			±0.1	±0.5	LSB
Offset error	Measured by the line passing through codes 30 and 4050			±5	±8	mV
Offset error drift				±1		µV/°C
Full-scale error				±0.2	±0.5	% of FSR
Gain error				±0.05	±0.2	% of FSR
Gain temperature coefficient	AV_{DD} = 5V			±1		ppm of FSR/°C
	AV_{DD} = 2.7V			±2		
PSRR Power-supply rejection ratio	Output unloaded			1		mV/V
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		V_{REF}	V
Output voltage settling time	To ±0.024% FSR, 0020h to 3FD0h, R_L = 2kΩ, 0pF < C_L < 200pF			8	10	µs
	R_L = 2kΩ, C_L = 500pF			12		
Slew rate				2.2		V/µs
Capacitive load stability	R_L = ∞			470		pF
	R_L = 2kΩ			1000		
Code change glitch impulse	1LSB change around major carry			0.15		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high			0.15		nV-s
Channel-to-channel dc crosstalk	Full-scale swing on adjacent channel			0.25		LSB
Channel-to-channel ac crosstalk	1kHz full-scale sine wave, outputs unloaded			–100		dB
DC output impedance	At mid-code input			1		Ω
Short-circuit current				50		mA
Power-up time	Coming out of power-down mode, AV_{DD} = 5V			2.5		µs
	Coming out of power-down mode, AV_{DD} = 3V			5		
AC PERFORMANCE(2)						
SNR	T_A = +25°C, BW = 20kHz, V_{DD} = 5V, f_{OUT} = 1kHz. First 19 harmonics removed for SNR calculation.			81		dB
THD				–75		dB
SFDR				79		dB
SINAD				74		dB
DAC output noise density	T_A = +25°C, at mid-code input, f_{OUT} = 1kHz			120		nV/√Hz
DAC output noise	T_A = +25°C, at mid-code input, 0.1Hz to 10Hz			6		$µV_{PP}$
REFERENCE						
Internal reference current consumption	AV_{DD} = 5.5V			360		µA
	AV_{DD} = 3.6V			348		µA
External reference current	External V_{REF} = 2.5V, if internal reference is disabled, all four channels active			80		µA
Reference input range $V_{REF}H$ voltage	$V_{REF}L$ < $V_{REF}H$, AV_{DD} – ($V_{REF}H$ + $V_{REF}L$) /2 > 1.2V		0		AV_{DD}	V
Reference input range $V_{REF}L$ voltage	$V_{REF}L$ < $V_{REF}H$, AV_{DD} – ($V_{REF}H$ + $V_{REF}L$) /2 > 1.2V		0		AV_{DD}/2	V
Reference input impedance				31		kΩ

(1) Linearity calculated using a reduced code range of 30 to 4050; output unloaded.
(2) Ensured by design or characterization; not production tested.

ELECTRICAL CHARACTERISTICS (continued)

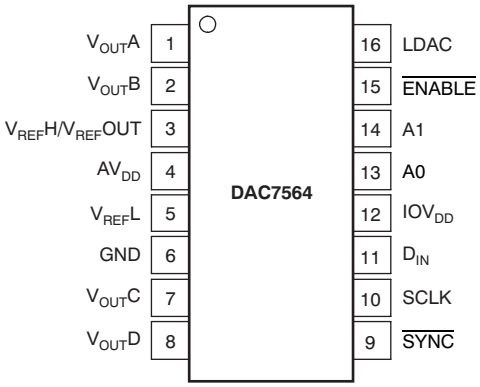
At AV_{DD} = 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	DAC7564 MIN	DAC7564 TYP	DAC7564 MAX	UNIT
REFERENCE OUTPUT						
Output voltage		T_A = +25°C	2.4975	2.5	2.5025	V
Initial accuracy		T_A = +25°C	–0.1	±0.004	0.1	%
Output voltage temperature drift		DAC7564A(3)		5	25	ppm/°C
		DAC7564C(4)		2	5	
Output voltage noise		f = 0.1Hz to 10Hz		12		μV_{PP}
Output voltage noise density (high-frequency noise)		T_A = +25°C, f = 1MHz, C_L = 0µF		50		nV/√Hz
		T_A = +25°C, f = 1MHz, C_L = 1µF		20		
		T_A = +25°C, f = 1MHz, C_L = 4µF		16		
Load regulation, sourcing(5)		T_A = +25°C		30		µV/mA
Load regulation, sinking(5)		T_A = +25°C		15		µV/mA
Output current load capability(6)				±20		mA
Line regulation		T_A = +25°C		10		µV/V
Long-term stability/drift (aging)(5)		T_A = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis(5)		First cycle		100		ppm
		Additional cycles		25		
LOGIC INPUTS(6)						
Input current				±1		µA
$V_{IN}L$	Logic input LOW voltage	2.7V ≤ IOV_{DD} ≤ 5.5V			0.3 × IOV_{DD}	V
		1.8V ≤ IOV_{DD} ≤ 2.7V			0.1 × IOV_{DD}	
$V_{IN}H$	Logic input HIGH voltage	2.7V ≤ IOV_{DD} ≤ 5.5V	0.7 × IOV_{DD}			V
		1.8V ≤ IOV_{DD} ≤ 2.7V	0.95 × IOV_{DD}			
Pin capacitance					3	pF
POWER REQUIREMENTS						
AV_{DD}			2.7		5.5	V
IOV_{DD}			1.8		5.5	V
IOI_{DD} (6)				10	20	µA
I_{DD} (7)	Normal mode	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1	1.6	mA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		0.95	1.5	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.3	3.5	µA
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		0.5	2.5	
Power Dissipation (7)	Normal mode	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		3.6	8.8	mW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		2.6	5.4	
	All power-down modes	AV_{DD} = IOV_{DD} = 3.6V to 5.5V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		4.7	19	µW
		AV_{DD} = IOV_{DD} = 2.7V to 3.6V $V_{IN}H$ = IOV_{DD} and $V_{IN}L$ = GND		1.4	9	
TEMPERATURE RANGE						
Specified performance			–40		+105	°C

(3) Reference is trimmed and tested at room temperature, and is characterized from –40°C to +120°C.
(4) Reference is trimmed and tested at two temperatures (+25°C and +105°C), and is characterized from –40°C to +120°C.
(5) Explained in more detail in the *Application Information* section of this data sheet.
(6) Ensured by design or characterization; not production tested.
(7) Input code = 2048, reference current included, no load.

PIN CONFIGURATIONS

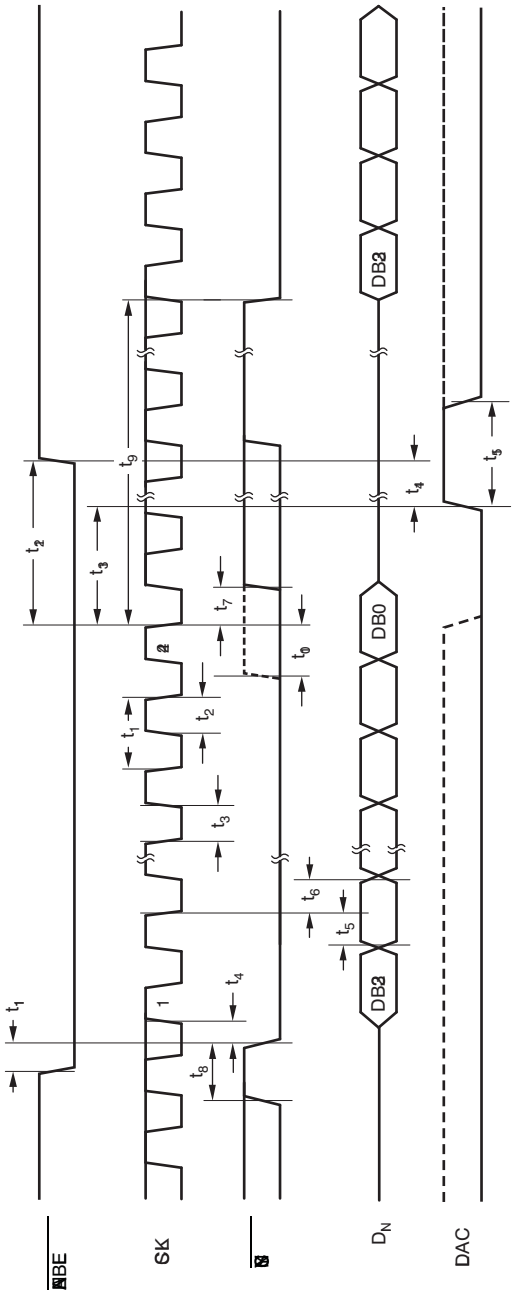
PW PACKAGE
TSSOP-16
(Top View)



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$V_{OUT}A$	Analog output voltage from DAC A
2	$V_{OUT}B$	Analog output voltage from DAC B
3	$V_{REF}H$/ $V_{REF}OUT$	Positive reference input / reference output 2.5V if internal reference used.
4	AV_{DD}	Power-supply input, 2.7V to 5.5V
5	$V_{REF}L$	Negative reference input
6	GND	Ground reference point for all circuitry on the part
7	$V_{OUT}C$	Analog output voltage from DAC C
8	$V_{OUT}D$	Analog output voltage from DAC D
9	$\overline{SYNC}$	Level-triggered control input (active low). This input is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 24th clock. If $\overline{SYNC}$ is taken high before the 24th clock edge, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC7564. Schmitt-Trigger logic input.
10	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.
11	D_{IN}	Serial data input. Data are clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
12	IOV_{DD}	Digital input-output power supply
13	A0	Address 0—sets device address; see Table 5.
14	A1	Address 1—sets device address; see Table 5.
15	$\overline{ENABLE}$	The enable pin (active low) connects the SPI interface to the serial port
16	LDAC	Load DACs; rising edge triggered, loads all DAC registers

SERIAL WRITE OPERATION



TIMING REQUIREMENTS(1) (2)

At AV_{DD} = IOV_{DD}= 2.7V to 5.5V and –40°C to +105°C range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	DAC7564 MIN	DAC7564 TYP	DAC7564 MAX	UNIT
t_1 (3) SCLK cycle time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_2 SCLK HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_3 SCLK LOW time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_4 $\overline{SYNC}$ to SCLK rising edge setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_5 Data setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	5			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5			
t_6 Data hold time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	4.5			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	4.5			
t_7 SCLK falling edge to $\overline{SYNC}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_8 Minimum $\overline{SYNC}$ HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_9 24th SCLK falling edge to $\overline{SYNC}$ falling edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	130			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	130			
t_{10} $\overline{SYNC}$ rising edge to 24th SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	15			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	15			
t_{11} $\overline{ENABLE}$ falling edge to $\overline{SYNC}$ falling edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	15			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	15			
t_{12} 24th SCLK falling edge to $\overline{ENABLE}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_{13} 24th SCLK falling edge to LDAC rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	50			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	50			
t_{14} LDAC rising edge to $\overline{ENABLE}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_{15} LDAC HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
	IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			

(1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See the *Serial Write Operation* timing diagram.
(3) Maximum SCLK frequency is 50MHz at IOV_{DD} = V_{DD} = 3.6V to 5.5V and 25MHz at IOV_{DD} = AV_{DD} = 2.7V to 3.6V.

TYPICAL CHARACTERISTICS: Internal Reference

At T_A = +25°C, unless otherwise noted.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (Grade C)

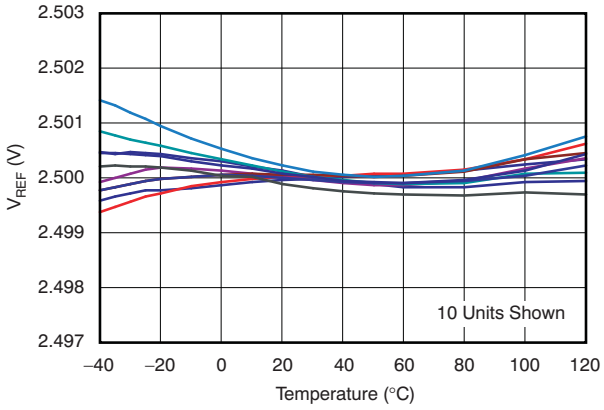


Figure 1.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (Grade A)

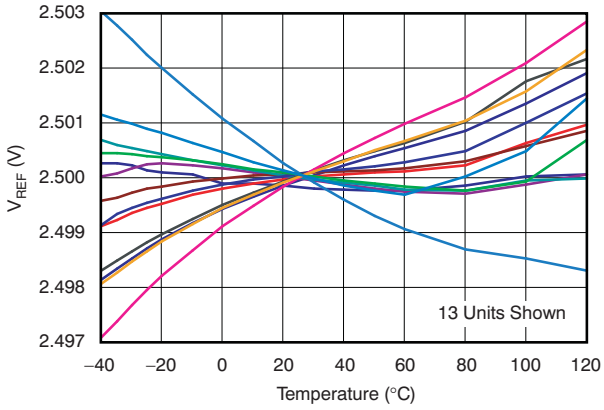


Figure 2.

REFERENCE OUTPUT TEMPERATURE DRIFT (–40°C to +120°C, Grade C)

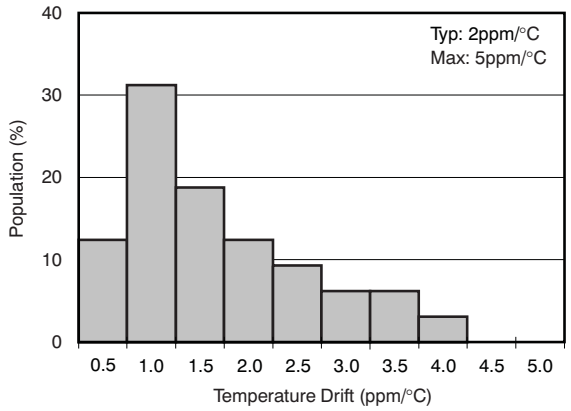


Figure 3.

REFERENCE OUTPUT TEMPERATURE DRIFT (–40°C to +120°, Grade A)

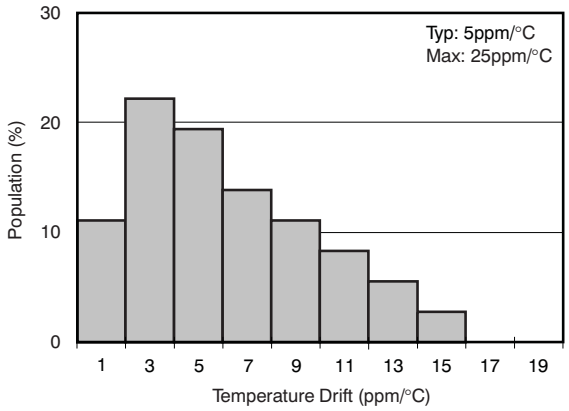


Figure 4.

REFERENCE OUTPUT TEMPERATURE DRIFT (0°C to +120°C, Grade C)

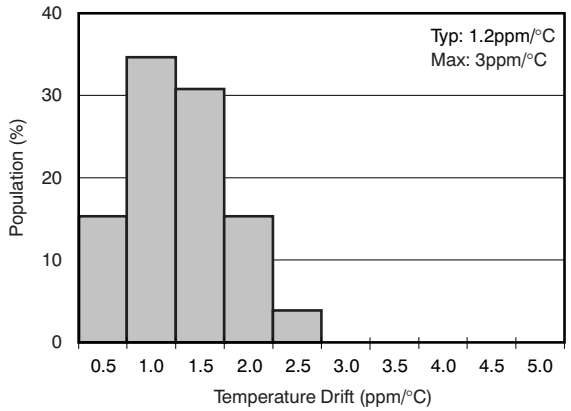


Figure 5.

LONG-TERM STABILITY/DRIFT (1)

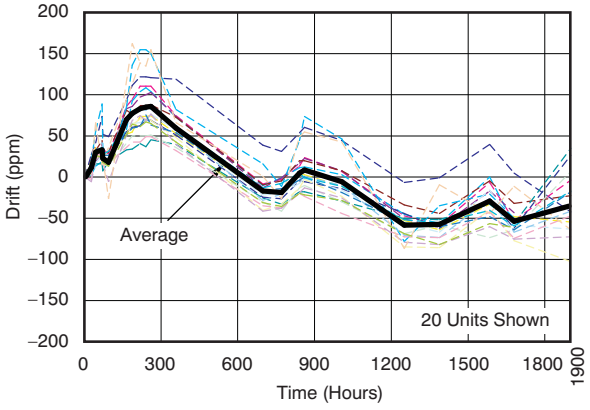


Figure 6.

(1) Explained in more detail in the *Application Information* section of this data sheet.

TYPICAL CHARACTERISTICS: Internal Reference (continued)

At T_A = +25°C, unless otherwise noted.

INTERNAL REFERENCE NOISE DENSITY vs FREQUENCY

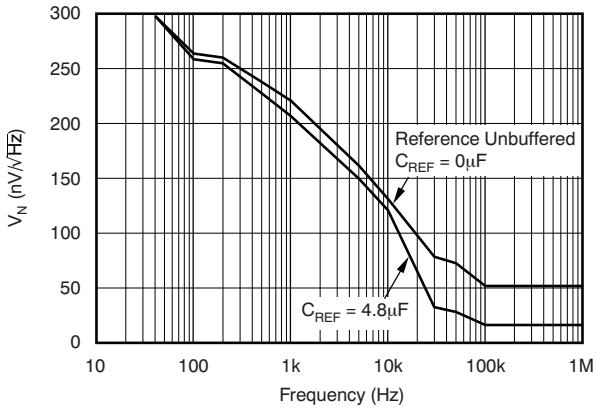


Figure 7.

INTERNAL REFERENCE NOISE 0.1Hz TO 10Hz

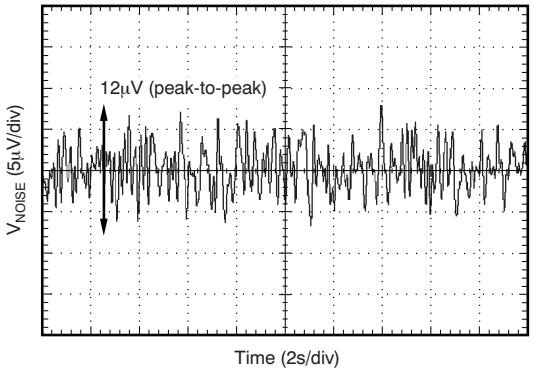


Figure 8.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT (Grade C)

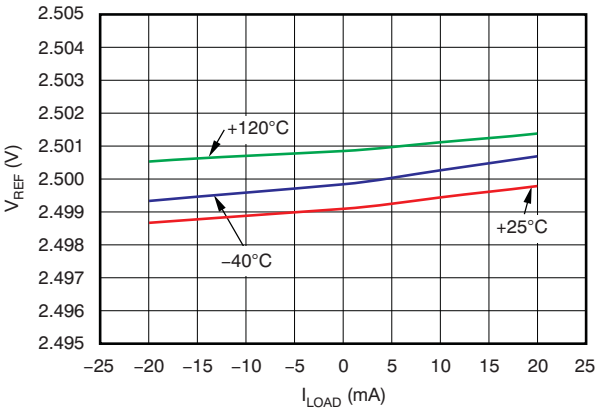


Figure 9.

INTERNAL REFERENCE VOLTAGE vs LOAD CURRENT (Grade A)

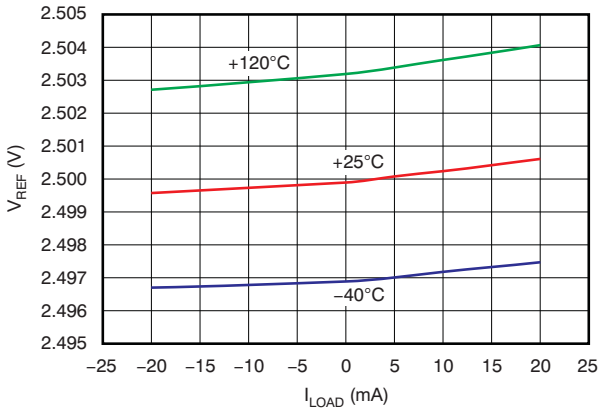


Figure 10.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grade C)

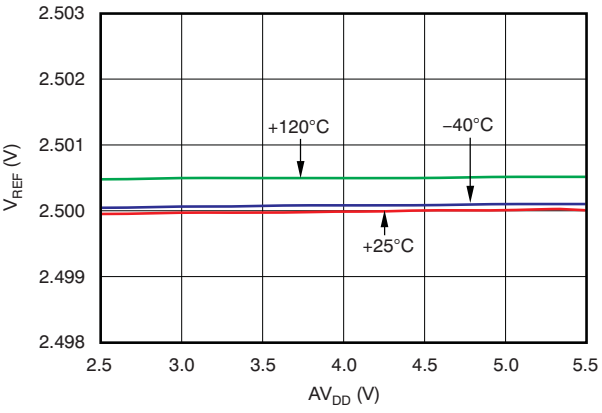


Figure 11.

INTERNAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE (Grade A)

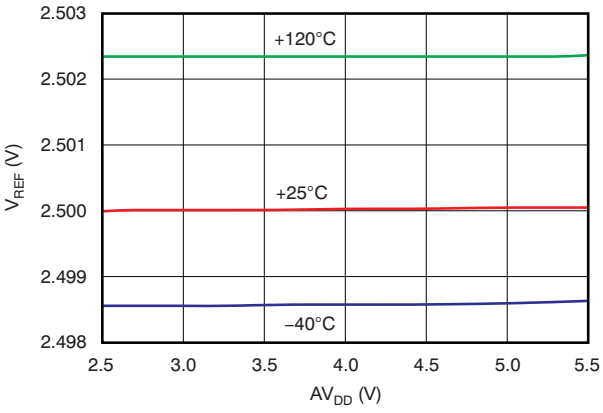


Figure 12.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

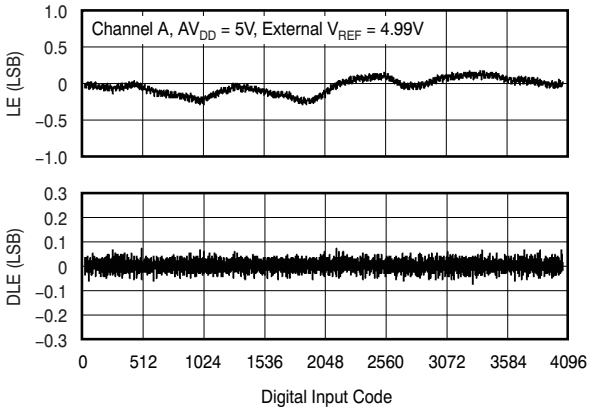


Figure 13.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

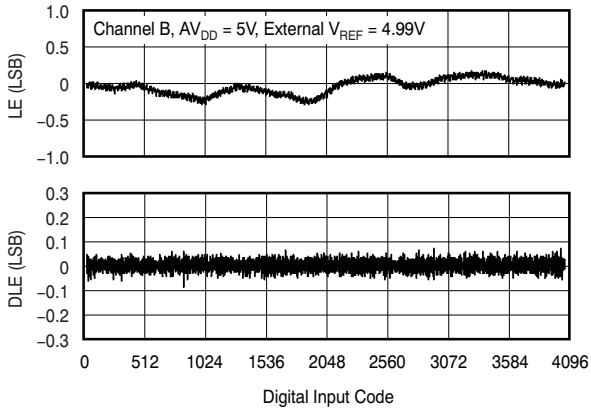


Figure 14.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

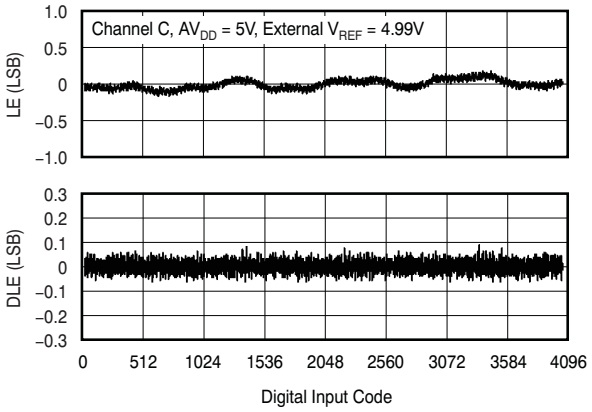


Figure 15.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

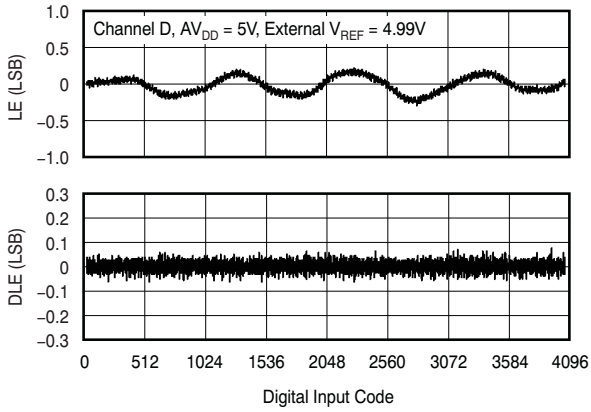


Figure 16.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

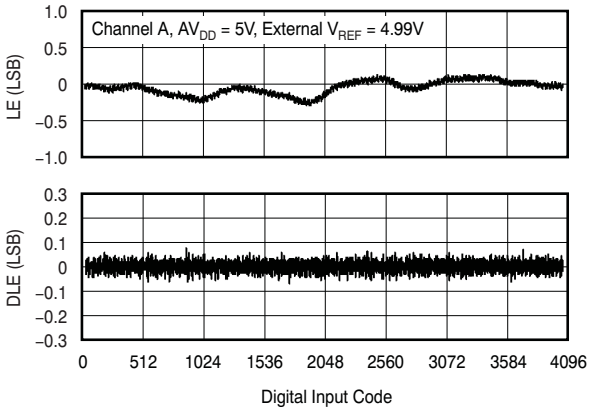


Figure 17.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

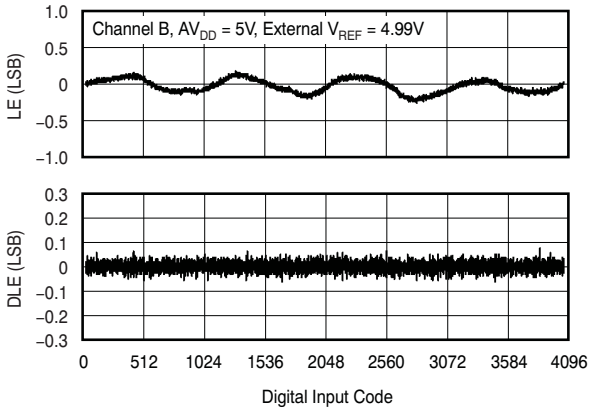


Figure 18.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

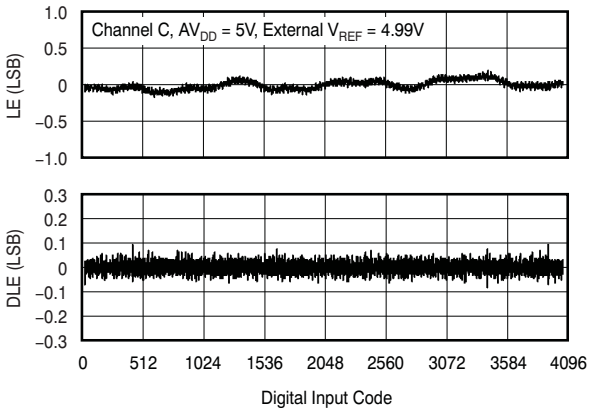


Figure 19.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

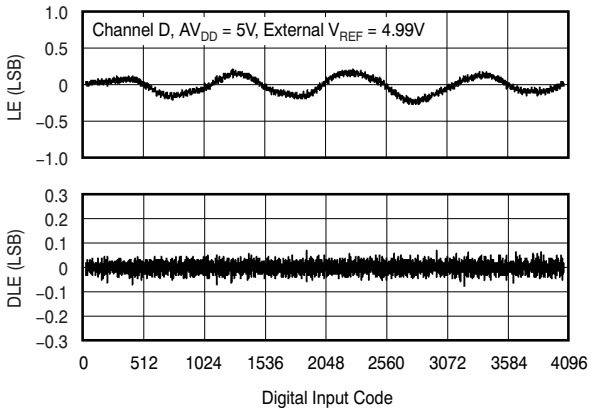


Figure 20.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

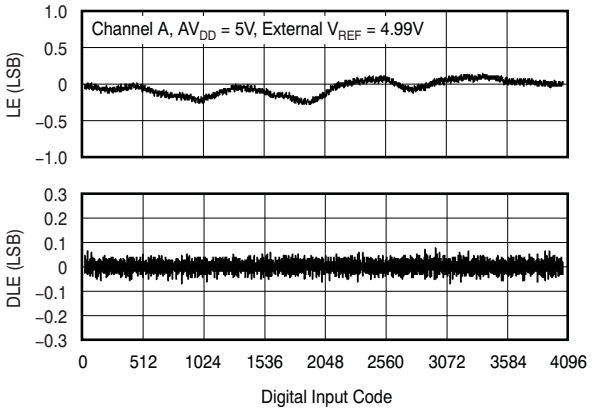


Figure 21.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

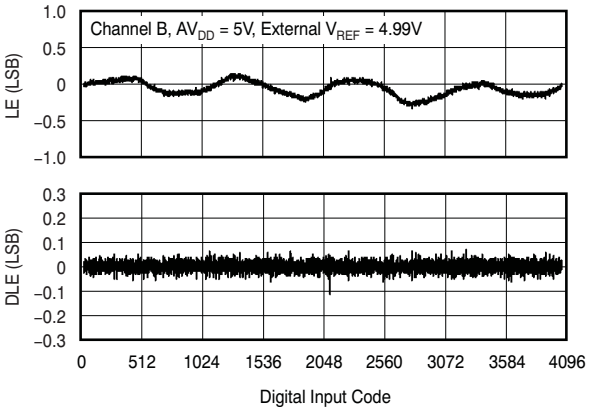


Figure 22.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

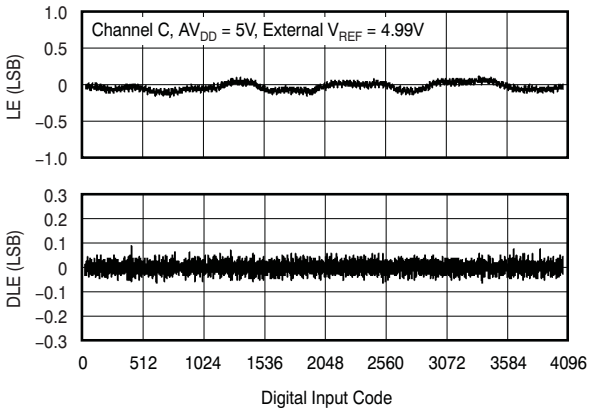


Figure 23.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

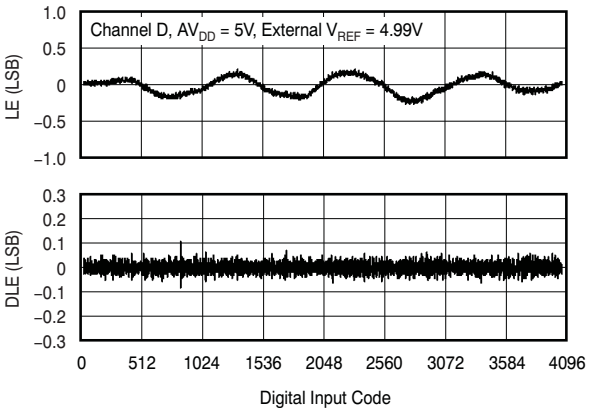


Figure 24.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

OFFSET ERROR vs TEMPERATURE

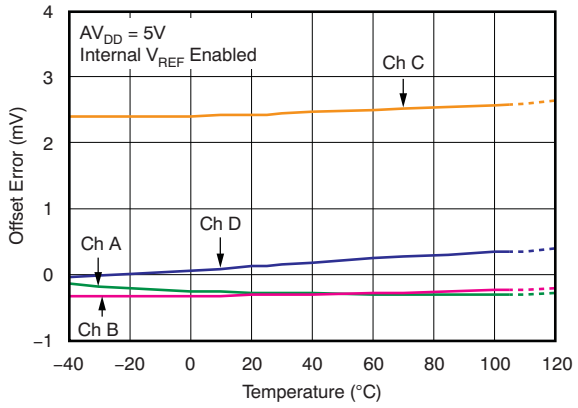


Figure 25.

FULL-SCALE ERROR vs TEMPERATURE

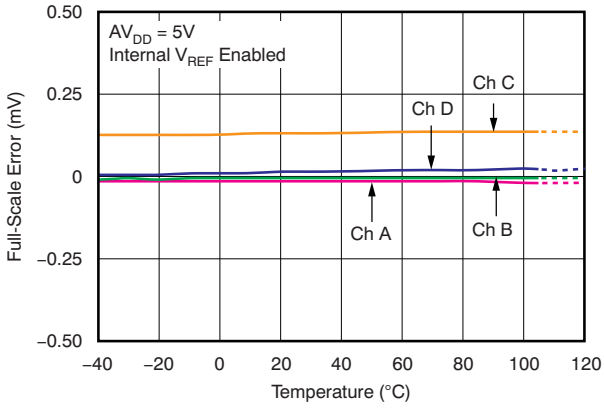


Figure 26.

SOURCE AND SINK CURRENT CAPABILITY

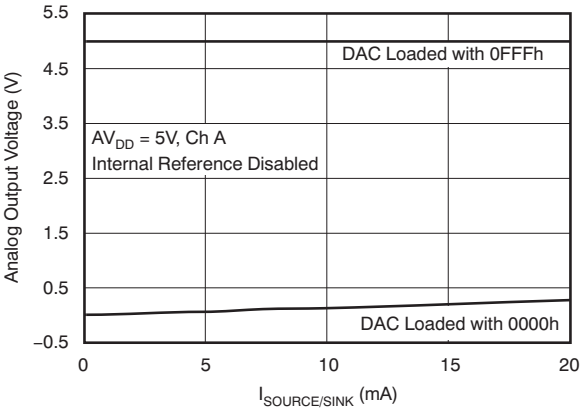


Figure 27.

SOURCE AND SINK CURRENT CAPABILITY

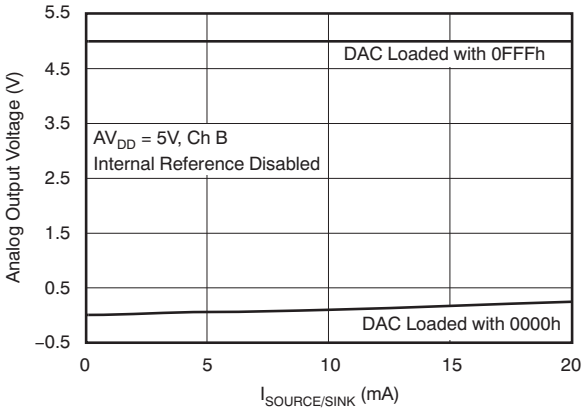


Figure 28.

SOURCE AND SINK CURRENT CAPABILITY

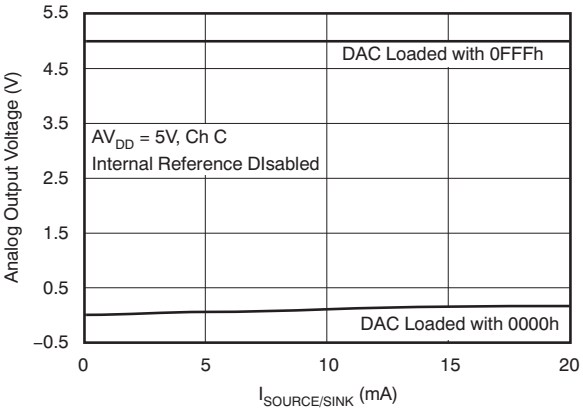


Figure 29.

SOURCE AND SINK CURRENT CAPABILITY

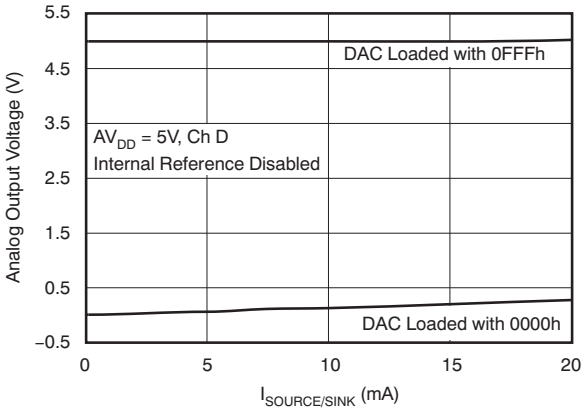


Figure 30.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

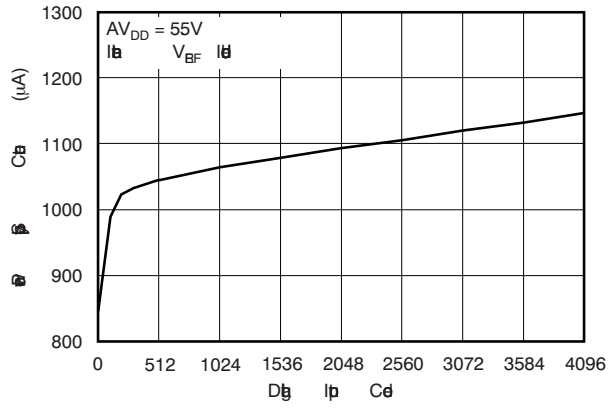


Figure 31.

POWER-SUPPLY CURRENT vs TEMPERATURE

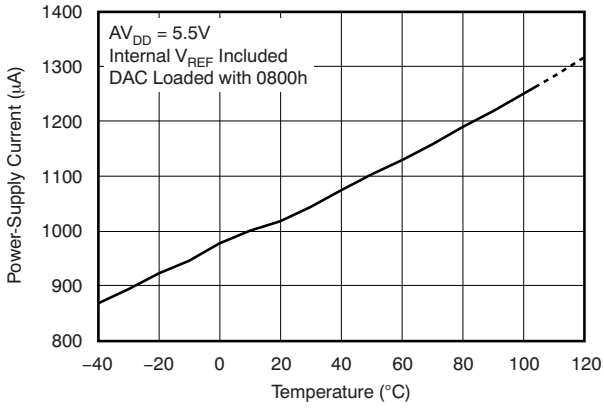


Figure 32.

POWER-SUPPLY CURRENT vs POWER-SUPPLY VOLTAGE

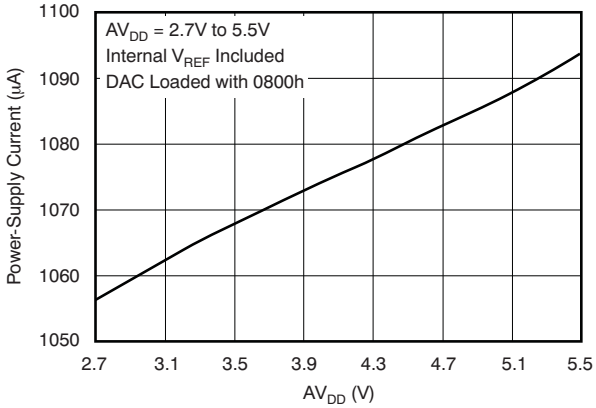


Figure 33.

POWER-DOWN CURRENT vs POWER-SUPPLY VOLTAGE

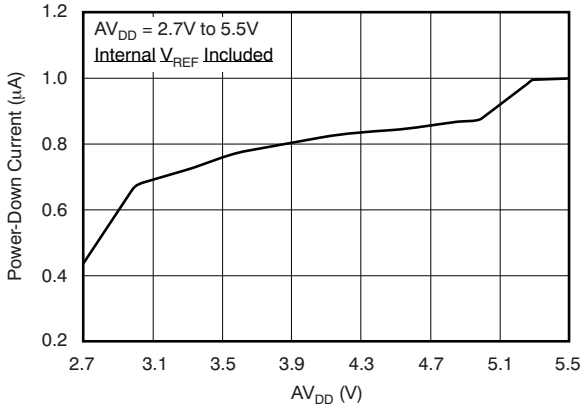


Figure 34.

POWER-DOWN CURRENT vs TEMPERATURE

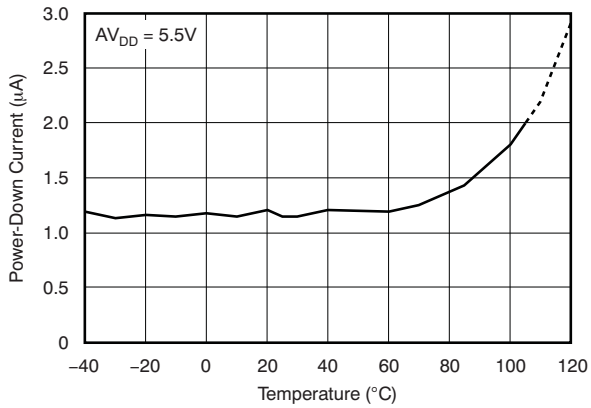


Figure 35.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

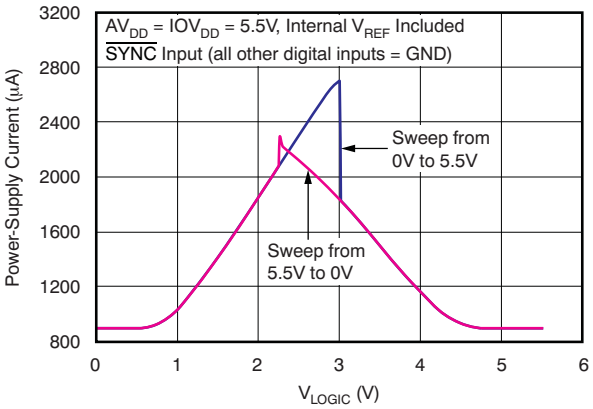


Figure 36.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

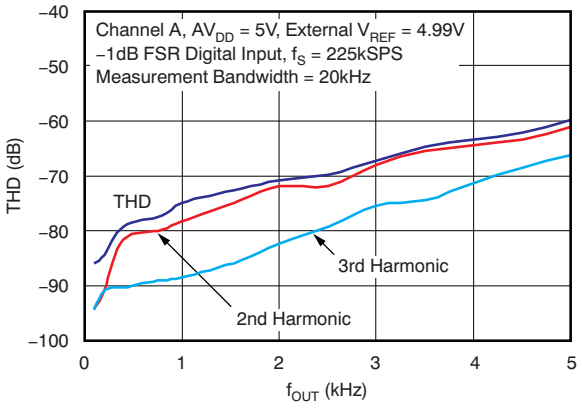


Figure 37.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

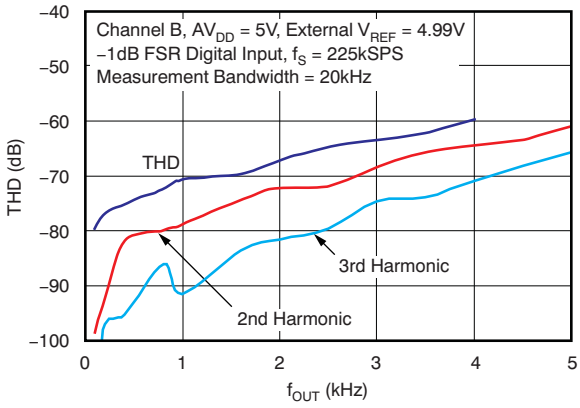


Figure 38.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

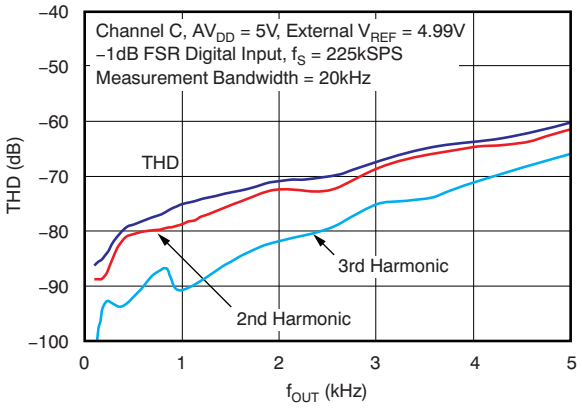


Figure 39.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

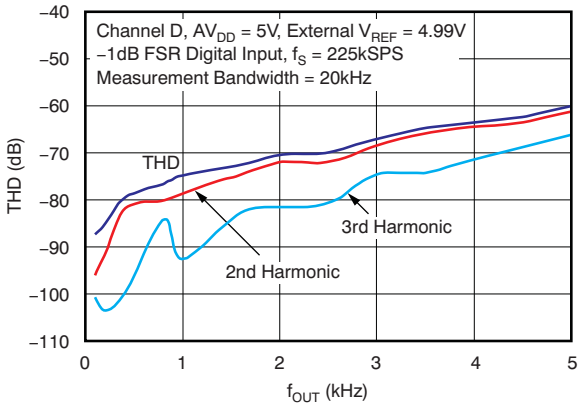


Figure 40.

POWER-SUPPLY CURRENT HISTOGRAM

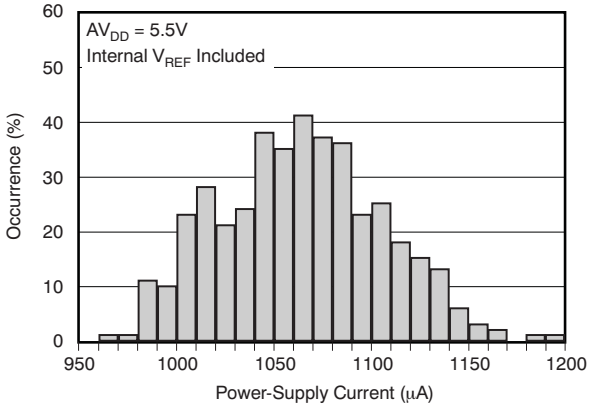


Figure 41.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

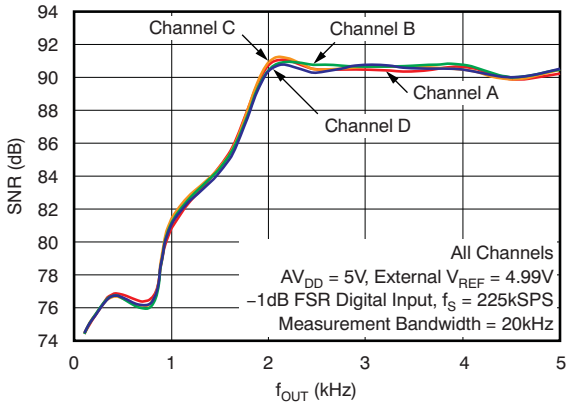


Figure 42.

POWER SPECTRAL DENSITY

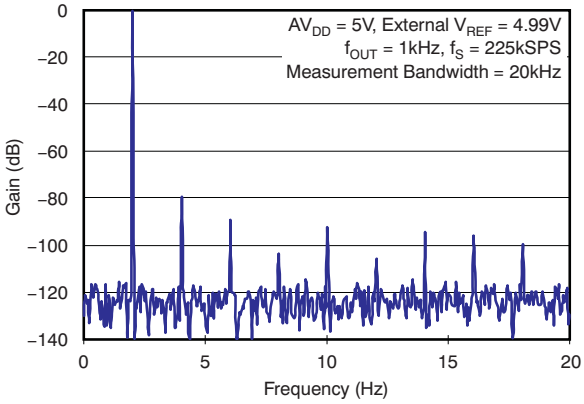


Figure 43.

FULL-SCALE SETTLING TIME: 5V RISING EDGE

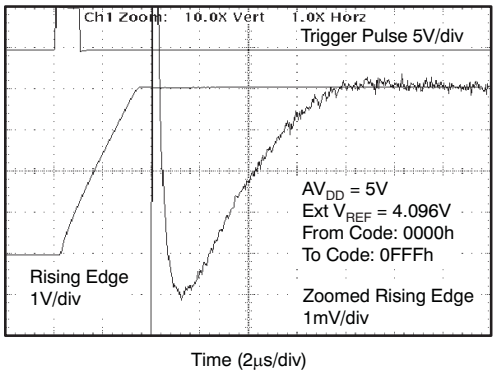


Figure 44.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

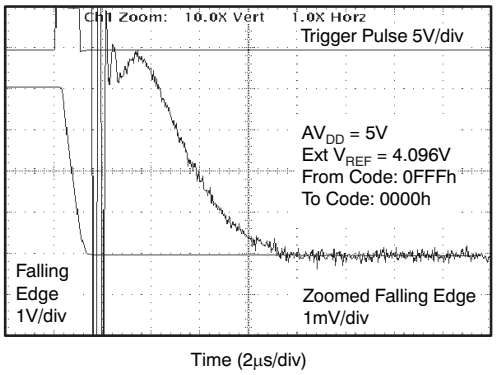


Figure 45.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

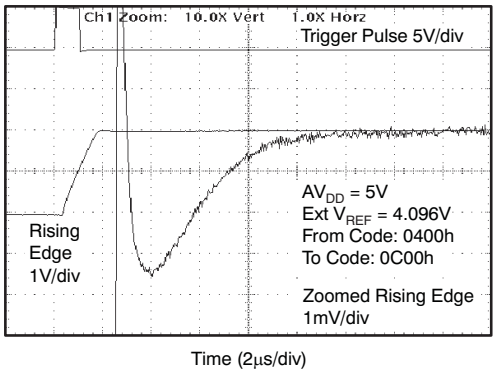


Figure 46.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

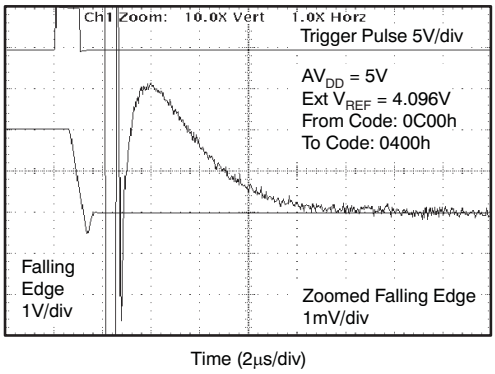


Figure 47.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE

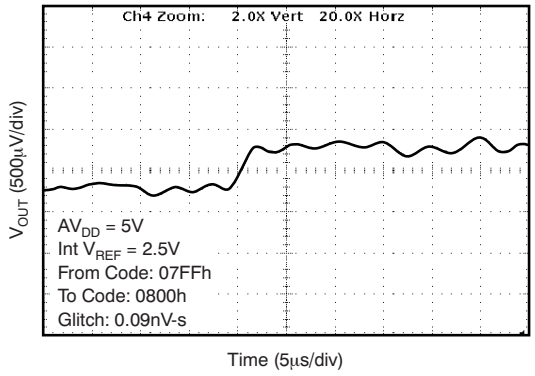


Figure 48.

GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE

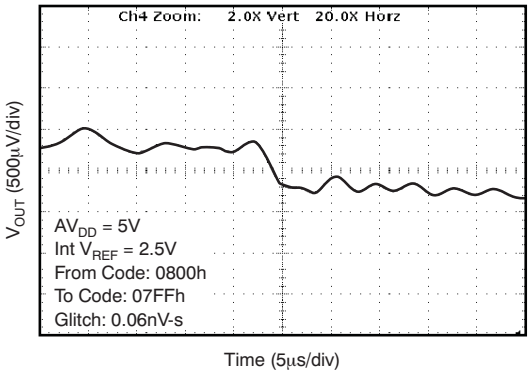


Figure 49.

GLITCH ENERGY: 5V, 4LSB STEP, RISING EDGE

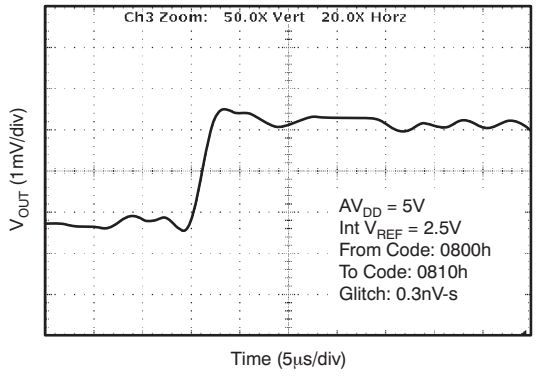


Figure 50.

GLITCH ENERGY: 5V, 4LSB STEP, FALLING EDGE

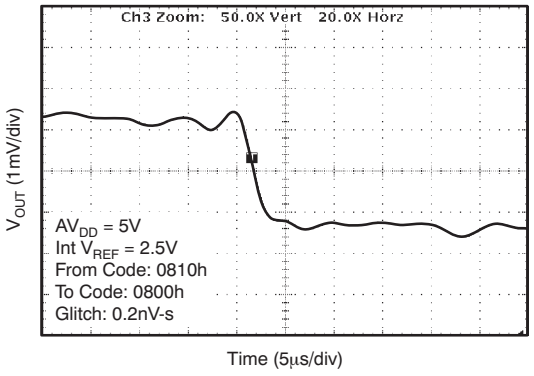


Figure 51.

GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE

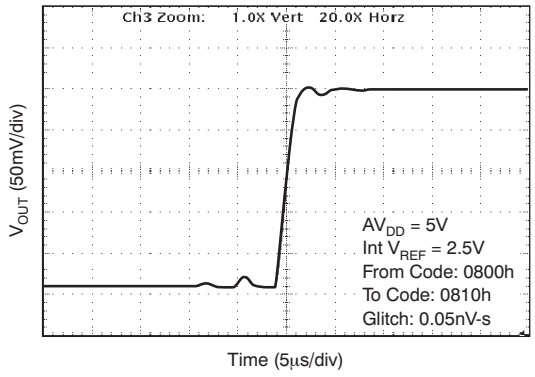


Figure 52.

GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE

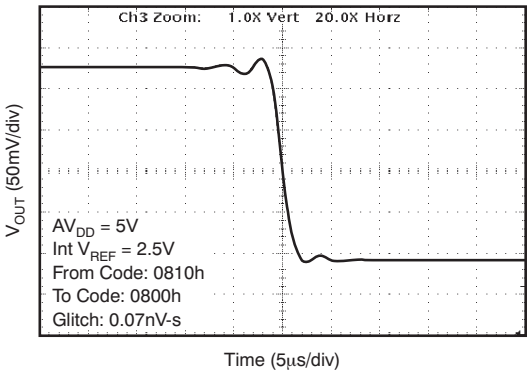


Figure 53.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 5V (continued)

At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

DAC OUTPUT NOISE DENSITY vs FREQUENCY (1)

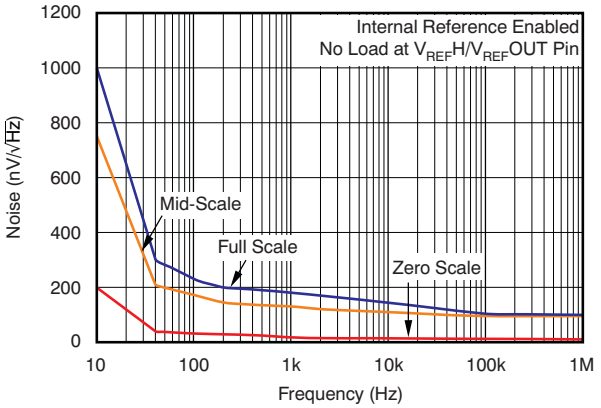


Figure 54.

DAC OUTPUT NOISE DENSITY vs FREQUENCY (2)

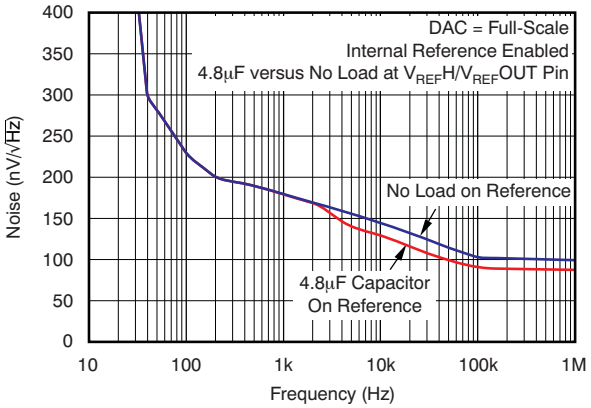


Figure 55.

DAC OUTPUT NOISE 0.1Hz TO 10Hz

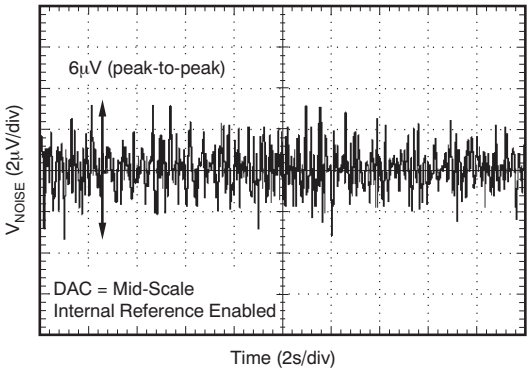


Figure 56.

(1) Explained in more detail in the *Application Information* section of this data sheet.
(2) See the *Application Information* section for more information.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 3.6V

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

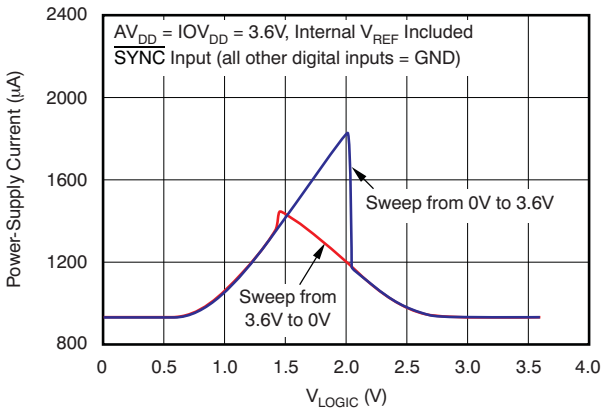


Figure 57.

POWER-SUPPLY CURRENT vs TEMPERATURE

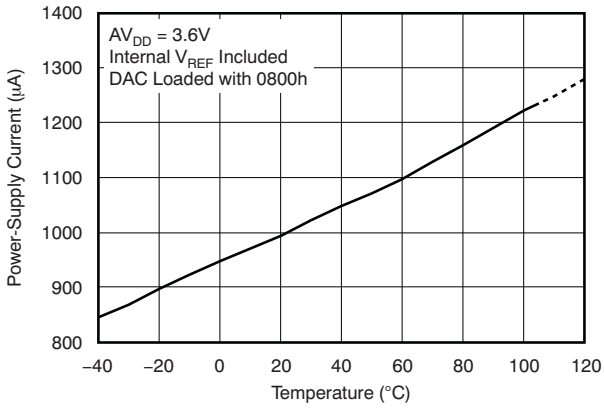


Figure 58.

POWER-SUPPLY CURRENT HISTOGRAM

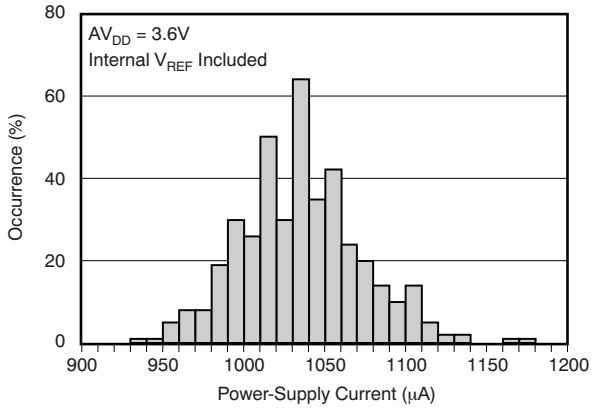


Figure 59.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

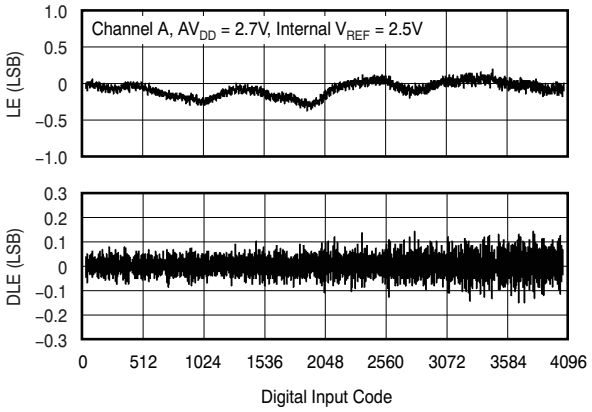


Figure 60.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

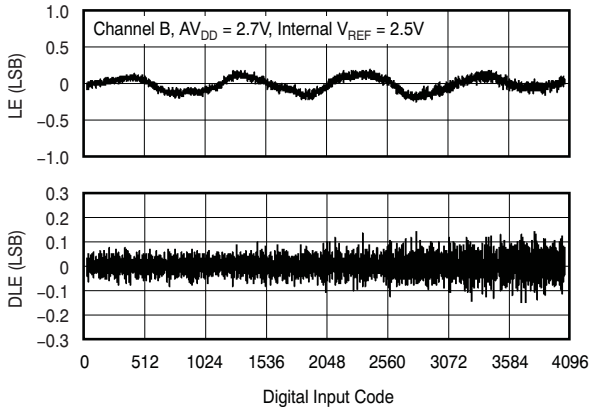


Figure 61.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

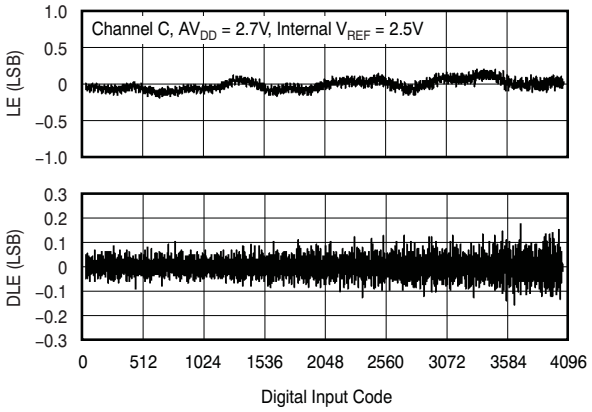


Figure 62.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (–40°C)

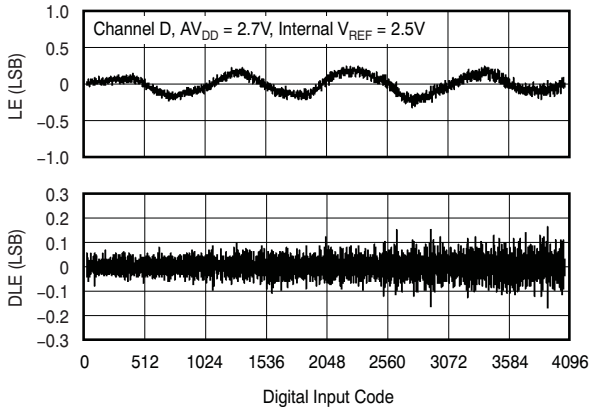


Figure 63.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

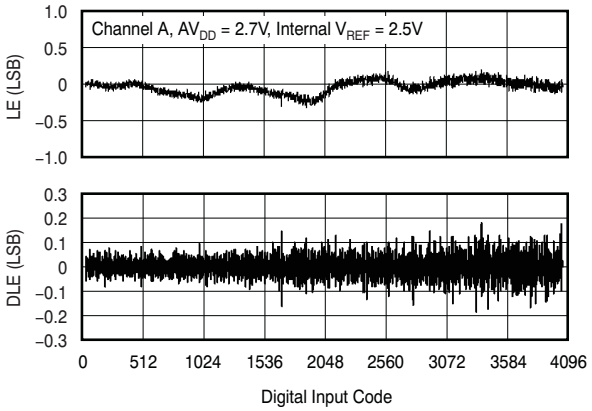


Figure 64.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

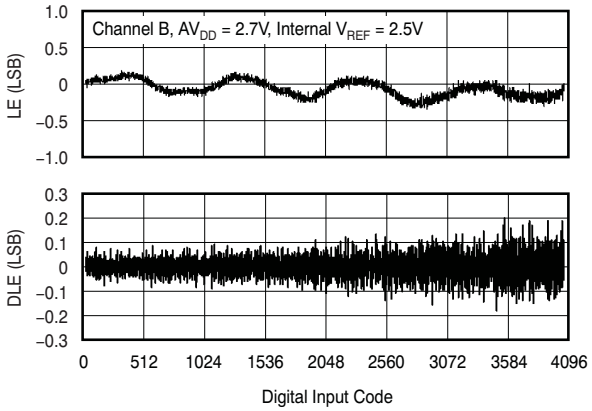


Figure 65.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

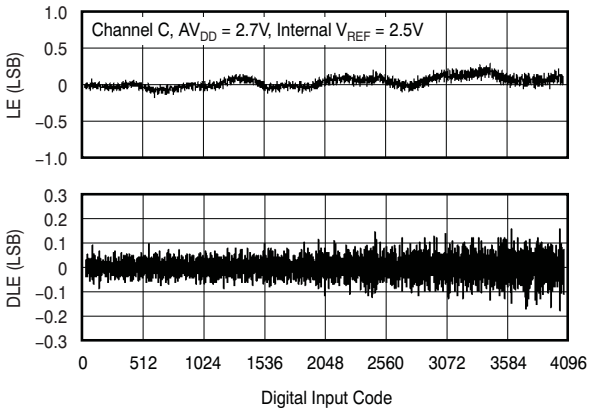


Figure 66.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+25°C)

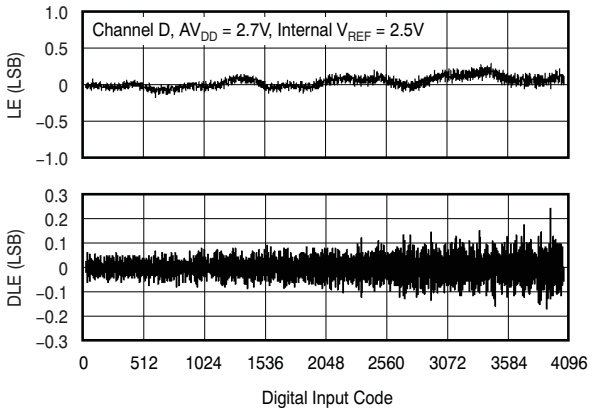


Figure 67.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

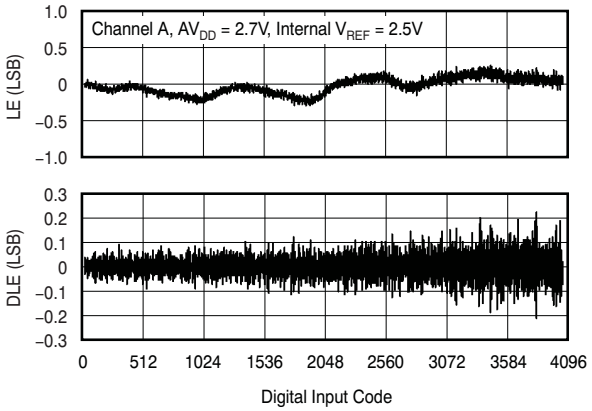


Figure 68.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

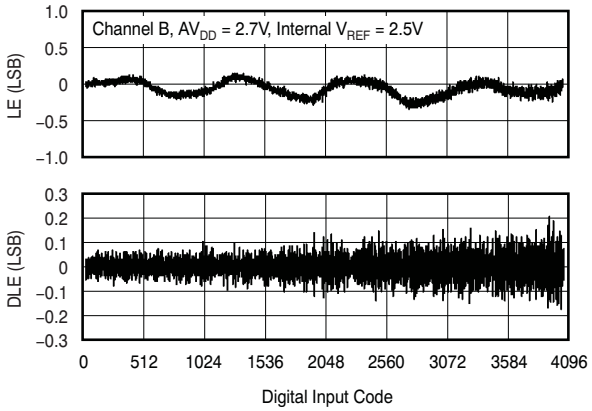


Figure 69.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

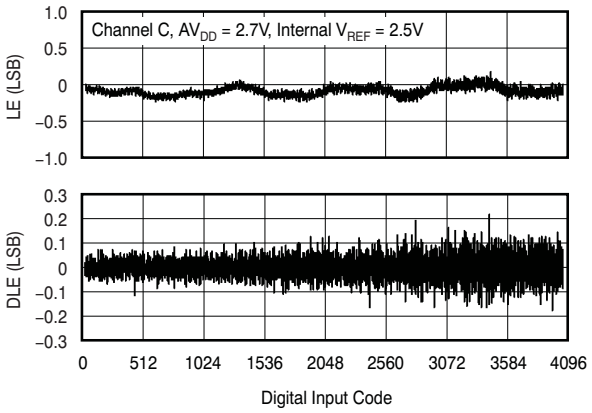


Figure 70.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (+105°C)

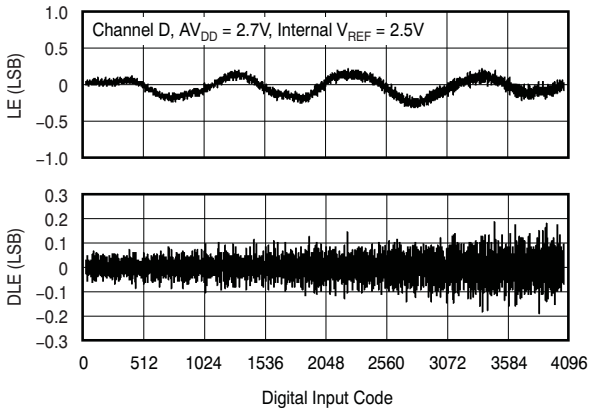


Figure 71.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

OFFSET ERROR vs TEMPERATURE

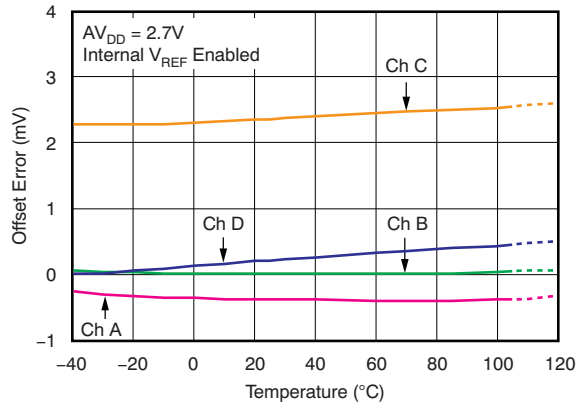


Figure 72.

FULL-SCALE ERROR vs TEMPERATURE

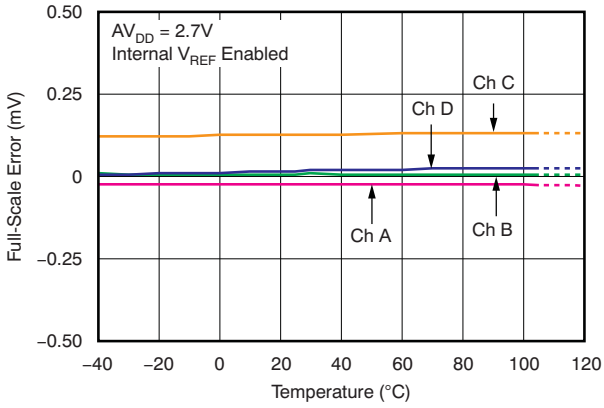


Figure 73.

SOURCE AND SINK CURRENT CAPABILITY

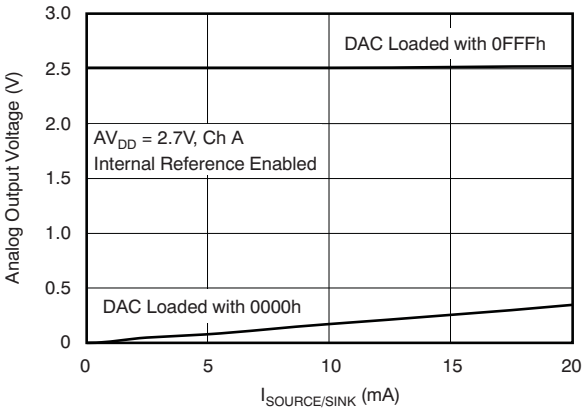


Figure 74.

SOURCE AND SINK CURRENT CAPABILITY

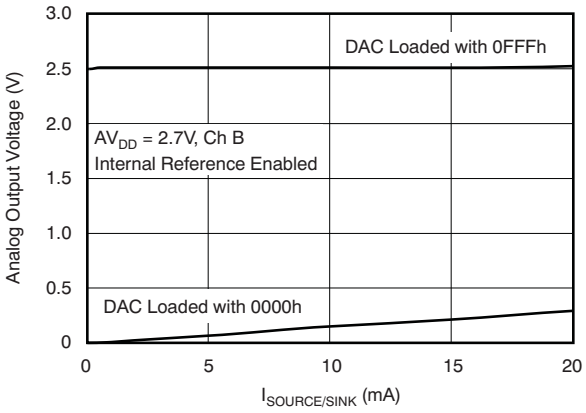


Figure 75.

SOURCE AND SINK CURRENT CAPABILITY

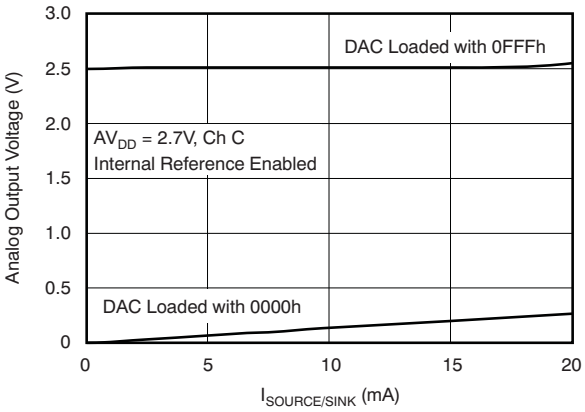


Figure 76.

SOURCE AND SINK CURRENT CAPABILITY

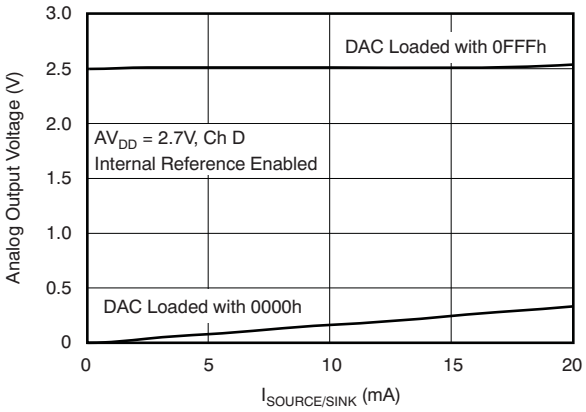


Figure 77.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs DIGITAL INPUT CODE

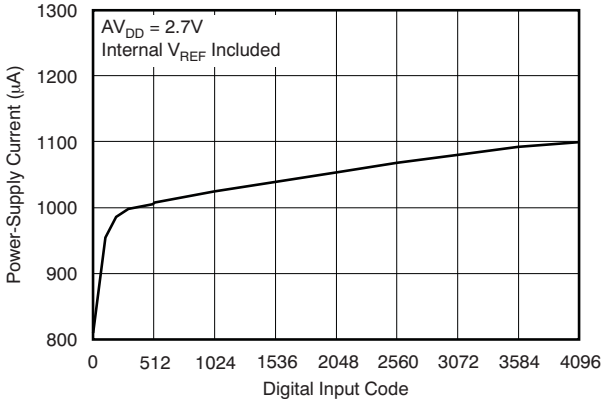


Figure 78.

POWER-SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

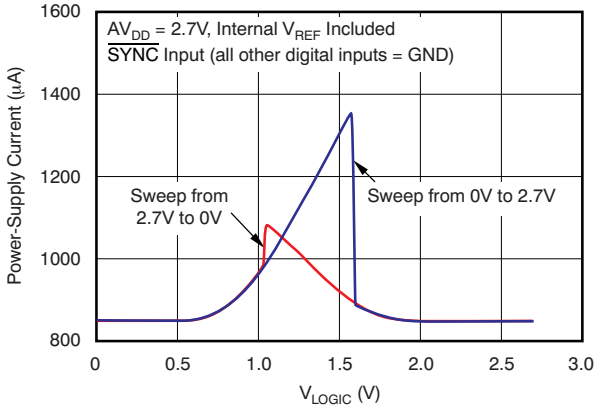


Figure 79.

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

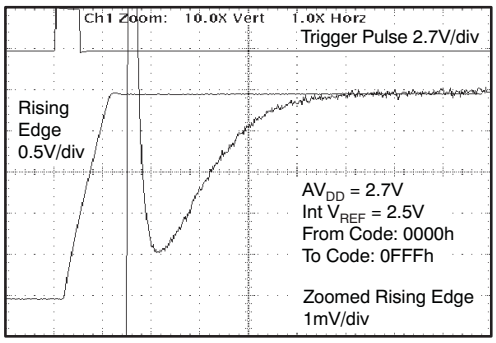


Figure 80.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

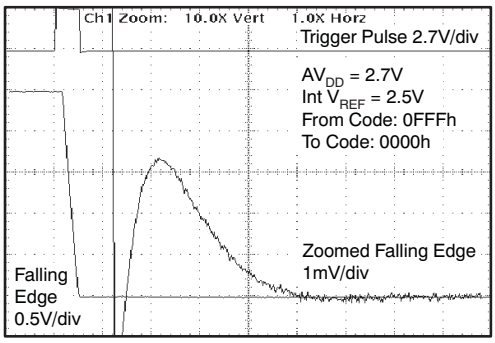


Figure 81.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

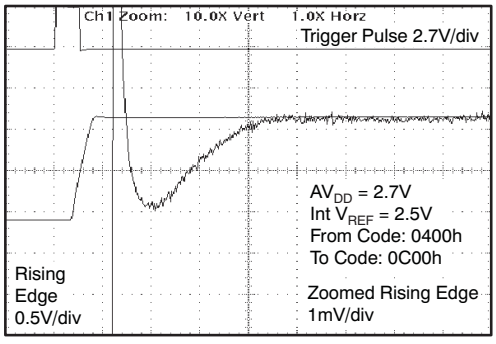


Figure 82.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

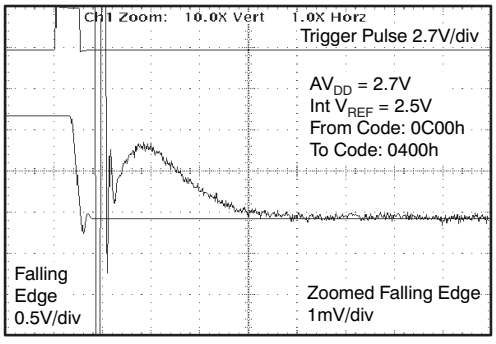


Figure 83.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

GLITCH ENERGY: 2.7V, 1LSB STEP, RISING EDGE

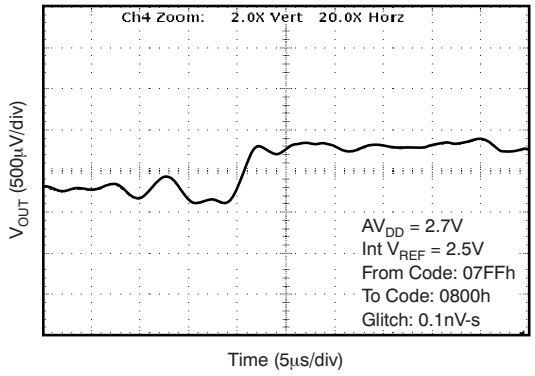


Figure 84.

GLITCH ENERGY: 2.7V, 1LSB STEP, FALLING EDGE

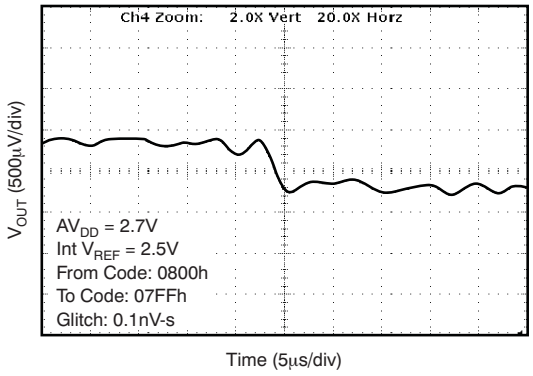


Figure 85.

GLITCH ENERGY: 2.7V, 4LSB STEP, RISING EDGE

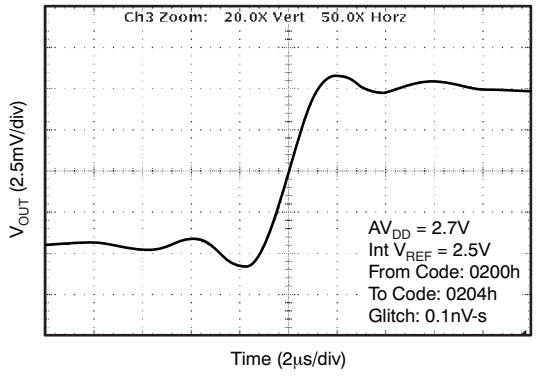


Figure 86.

GLITCH ENERGY: 2.7V, 4LSB STEP, FALLING EDGE

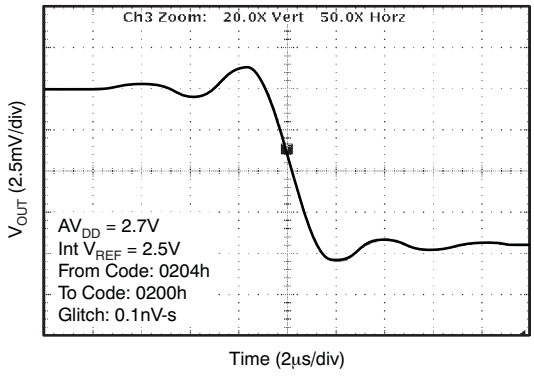


Figure 87.

GLITCH ENERGY: 2.7V, 16LSB STEP, RISING EDGE

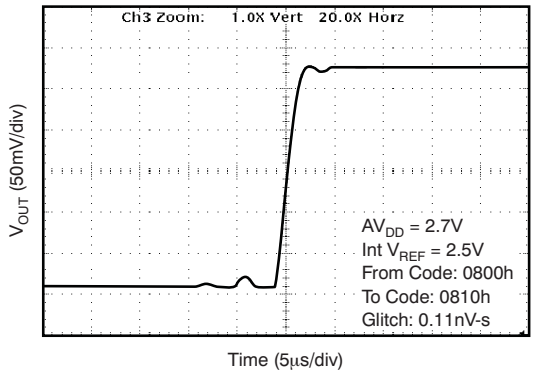


Figure 88.

GLITCH ENERGY: 2.7V, 16LSB STEP, FALLING EDGE

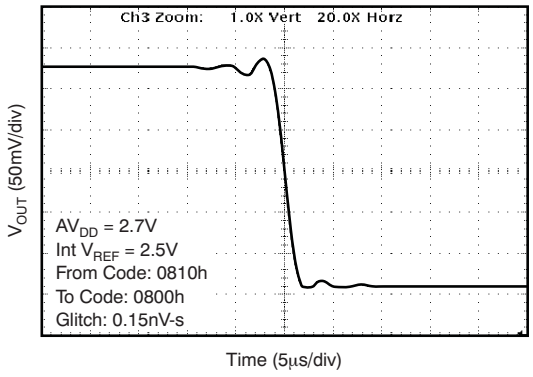


Figure 89.

TYPICAL CHARACTERISTICS: DAC at AV_{DD} = 2.7V (continued)

At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

POWER-SUPPLY CURRENT vs TEMPERATURE

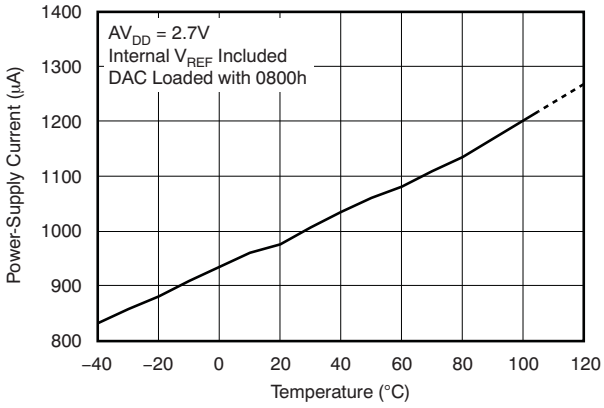


Figure 90.

POWER-DOWN CURRENT vs TEMPERATURE

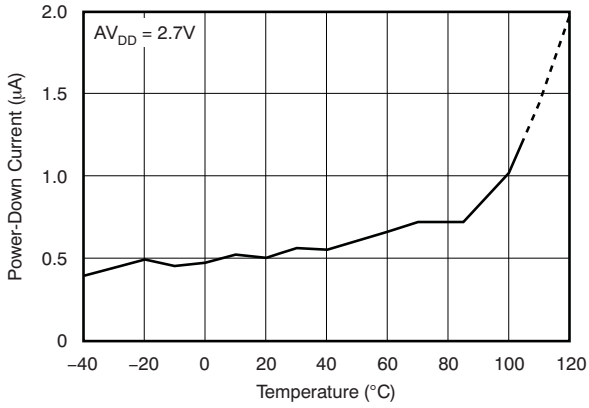


Figure 91.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC7564 architecture consists of a string DAC followed by an output buffer amplifier. Figure 92 shows a block diagram of the DAC architecture.

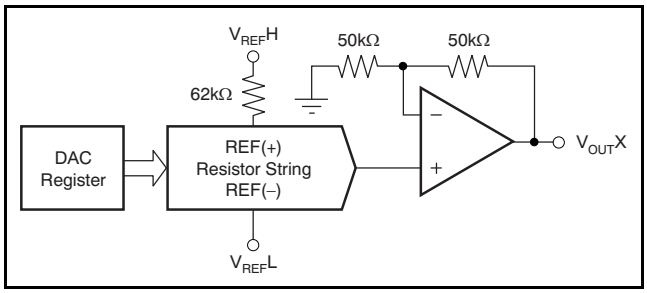


Figure 92. DAC7564 Architecture

The input coding to the DAC7564 is straight binary, so the ideal output voltage is given by Equation 1.

$$V_{OUT}X = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times \frac{D_{IN}}{4096} \quad (1)$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095. X represents channel A, B, C, or D.

RESISTOR STRING

The resistor string section is shown in Figure 93. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

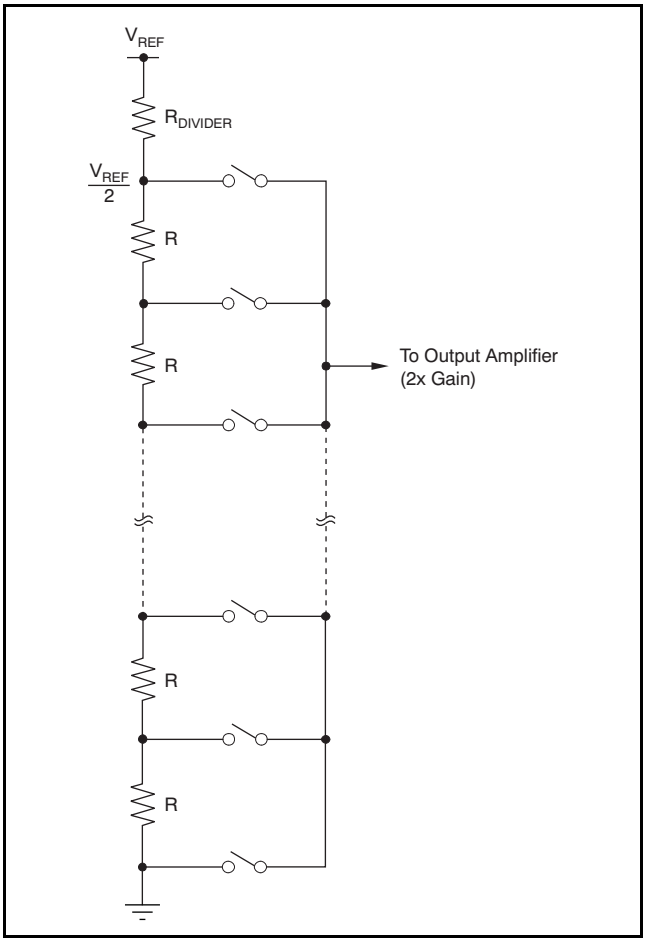


Figure 93. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 2.2V/µs, with a full-scale settling time of 8µs with the output unloaded.

INTERNAL REFERENCE

The DAC7564 includes a 2.5V internal reference that is enabled by default. The internal reference is externally available at the $V_{REF}H/V_{REF}OUT$ pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC7564 is a bipolar transistor-based, precision bandgap voltage reference. Figure 94 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} - V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is gained up and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

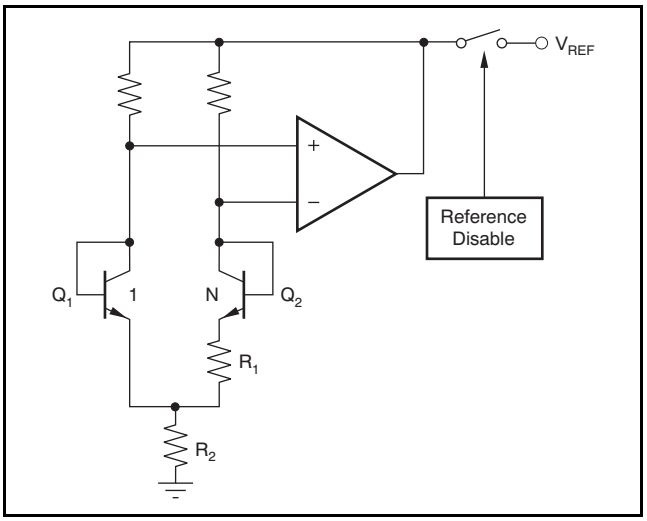


Figure 94. Simplified Schematic of the Bandgap Reference

Enable/Disable Internal Reference

The internal reference in the DAC7564 is enabled by default and operates in automatic mode; however, the reference can be disabled for debugging, evaluation purposes, or when using an external reference. A serial command that requires a 24-bit write sequence (see the *Serial Interface* section) must be used to disable the internal reference, as shown in Table 1. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the $V_{REF}H/V_{REF}OUT$ pin (3-state output). Do not attempt to drive the $V_{REF}H/V_{REF}OUT$ pin externally and internally at the same time indefinitely.

To then enable the internal reference, either perform a power-cycle to reset the device, or write the 24-bit serial command shown in Table 2. These actions put the internal reference back into the default mode. In the default mode, the internal reference powers down automatically when all DACs power down in any of the power-down modes (see the *Power-Down Modes* section); the internal reference powers up automatically when any DAC is powered up.

The DAC7564 also provides the option of keeping the internal reference powered on all the time, regardless of the DAC(s) state (powered up or down). To keep the internal reference powered on, regardless of the DAC(s) state, write the 24-bit serial command shown in Table 3.

Table 1. Write Sequence for Disabling Internal Reference (internal reference always powered down—012000h)

DB23							DB16			DB13													DB0
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	X	X	X	X
										Data Bits													

Table 2. Write Sequence for Enabling Internal Reference (internal reference powered up to default mode—010000h)

DB23							DB16																DB0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
										Data Bits													

Table 3. Write Sequence for Enabling Internal Reference (internal reference always powered up—011000h)

DB23							DB16				DB12												DB0
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	X	X	X	X
										Data Bits													

SERIAL INTERFACE

The DAC7564 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The DAC7564 input shift register is 24 bits wide, consisting of eight control bits (DB23 to DB16) and 12 data bits (DB15 to DB4). Bits DB0, DB1, DB2, and DB3 are ignored by the DAC and should be treated as *don't care* bits. All 24 bits of data are loaded into the DAC under the control of the serial clock input, SCLK. DB23 (MSB) is the first bit that is loaded into the DAC shift register, and is followed by the rest of the 24-bit word pattern, left-aligned. This configuration means that the first 24 bits of data are latched into the shift register and any further clocking of data is ignored. The DAC7564 receives all 24 bits of data and decodes the first eight bits in order to determine the DAC operating/control mode. The 12 bits of data that follow are decoded by the DAC to determine the equivalent analog output, while the last four bits (DB3, DB2, DB1, and DB0) are ignored. The data format is straight binary with all '0's corresponding to 0V output and all '1's corresponding to full-scale output (that is, V_{REF} – 1 LSB). For all documentation purposes, the data format and representation used here is a true 12-bit pattern (that is, 0FFFh for full-scale), even if the usable 12 bits of data are extracted from a left-justified, 16-bit data format that the DAC7564 requires.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC7564 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data. After 24 bits are locked into the shift register, the eight MSBs are used as control bits and the following 12 LSBs are used as data. After receiving the 24th falling clock edge, the DAC7564 decodes the eight control bits and 12 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new write sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs. After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle. To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. Refer to the Typical Characteristics section for Figure 36, Figure 57, and Figure 79 (*Supply Current vs Logic Input Voltage*).

IOV_{DD} AND VOLTAGE TRANSLATORS

The IOV_{DD} pin powers the digital input structures of the DAC7564. For single-supply operation, it can be tied to AV_{DD}. For dual-supply operation, the IOV_{DD} pin provides interface flexibility with various CMOS logic families and should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC7564 use AV_{DD} as the supply voltage. The external logic high inputs translate to AV_{DD} by level shifters. These level shifters use the IOV_{DD} voltage as a reference to shift the incoming logic HIGH levels to AV_{DD}. IOV_{DD} is ensured to operate from 2.7V to 5.5V regardless of the AV_{DD} voltage, assuring compatibility with various logic families. Although specified down to 2.7V, IOV_{DD} operates at as low as 1.8V with degraded timing and temperature performance. For lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND voltages.

INPUT SHIFT REGISTER

The input shift register (SR) of the DAC7564 is 24 bits wide, as shown in Table 4, and consists of eight control bits (DB23 to DB16), 12 data bits (DB15 to DB4), and four *don't care* bits. The first two control bits (DB23 and DB22) are the address match bits. The DAC7564 offers hardware-enabled addressing capability, allowing a single host to talk to up to four DAC7564s through a single SPI bus without any glue logic, enabling up to 16-channel operation. The state of DB23 should match the state of pin A1; similarly, the state of DB22 should match the state of pin A0. If there is no match, the control command and the data (DB21...DB0) are ignored by the DAC7564. That is, if there is no match, the DAC7564 is not addressed. Address matching can be overridden by the broadcast update.

Table 4. Data Input Register Format

DB23											DB12
A1	A0	LD1	LD0	0	DAC Select 1	DAC Select 0	PD0	D11	D10	D9	D8
DB11											DB0
D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

LD1 (DB21) and LD0 (DB20) control the loading of each analog output with the specified 12-bit data value or power-down command. Bit DB19 must always be '0'. The DAC channel select bits (DB18, DB17) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC7564 channels as well as the power-down mode of the internal reference.

The DAC7564 supports a number of different load commands. The load commands include broadcast commands to address all the DAC7564s on an SPI bus. The load commands are summarized as follows:

DB21 = 0 and DB20 = 0: Single-channel store. The data buffer corresponding to a DAC selected by DB18 and DB17 updates with the contents of SR data (or power-down).

DB21 = 0 and DB20 = 1: Single-channel update. The data buffer and DAC register corresponding to a DAC selected by DB18 and DB17 update with the contents of SR data (or power-down).

DB21 = 1 and DB20 = 0: Simultaneous update. A channel selected by DB18 and DB17 updates with the SR data; simultaneously, all the other channels update with previously stored data (or power-down) from data buffers.

DB21 = 1 and DB20 = 1: Broadcast update. All the DAC7564s on the SPI bus respond, regardless of address matching. If DB18 = 0, SR data are ignored and any channels from all DAC7564s update with previously stored data (or power-down). If DB18 = 1, SR data (or power-down) update any channels of all DAC7564s in the system. This broadcast update feature allows the simultaneous update of up to 16 channels.

Refer to Table 5 for more information.

Table 5. Control Matrix for the DAC7564

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13-DB4	DB3-DB0	DESCRIPTION
A1	A0	LD 1	LD 0	0	DAC Sel 1	DAC Sel 0	PD0	MSB	MSB-1	MSB-2...LSB	Don't Care	
(Address Select)												
0/1	0/1	See Below										This address selects one of four possible devices on a single SPI data bus based on the address pin(s) state of each device.
A0 and A1 should correspond to the package address set via pins 13 and 14		0	0	0	0	0	0	Data			X	Write to buffer A with data
		0	0	0	0	1	0	Data			X	Write to buffer B with data
		0	0	0	1	0	0	Data			X	Write to buffer C with data
		0	0	0	1	1	0	Data			X	Write to buffer D with data
		0	0	0	(00, 01, 10, or 11)		1	See Table 6		0	X	Write to buffer (selected by DB17 and DB18) with power-down command
		0	1	0	(00, 01, 10, or 11)		0	Data			X	Write to buffer with data and load DAC (selected by DB17 and DB18)
		0	1	0	(00, 01, 10, or 11)		1	See Table 6		0	X	Write to buffer with power-down command and load DAC (selected by DB17 and DB18)
		1	0	0	(00, 01, 10, or 11)		0	Data			X	Write to buffer with data (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers
		1	0	0	(00, 01, 10, or 11)		1	See Table 6		0	X	Write to buffer with power-down command (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers
Broadcast Modes												
X	X	1	1	0	0	X	X	X			X	Simultaneously update all channels of all DAC7564 devices in the system with data stored in each channels data buffer
X	X	1	1	0	1	X	0	Data			X	Write to all devices and load all DACs with SR data
X	X	1	1	0	1	X	1	See Table 6		0	X	Write to all devices and load all DACs with power-down command in SR

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line stays low for at least 24 falling edges of SCLK and the addressed DAC register updates on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 95).

POWER-ON RESET TO ZERO-SCALE

The DAC7564 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain that way until a valid write sequence and load command are made to the respective DAC channel. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before power is applied to the device. The internal reference is powered on by default and remains that way until a valid reference-change command is executed.

No device pin should be brought high before power is applied to the device. The internal reference is powered on by default and remains that way until a valid reference-change command is executed.

LDAC FUNCTIONALITY

The DAC7564 offers both a software and hardware simultaneous update function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC7564 data updates are *synchronized* with the falling edge of the 24th SCLK cycle, which follows a falling edge of $\overline{\text{SYNC}}$. For such *synchronous* updates, the LDAC pin is not required and it must be connected to GND permanently. The LDAC pin is used as a positive edge triggered timing signal for *asynchronous* DAC updates. To do an LDAC operation, single-channel store(s) should be done (loading DAC buffers) by setting LD0 and LD1 to '0'. Multiple single-channel updates can be done in order to set different channel buffers to desired values and then make a rising edge on LDAC. Data buffers of all channels must be loaded with desired data before an LDAC rising edge. After a low-to-high LDAC transition, all DACs are simultaneously updated with the contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the LDAC trigger.

ENABLE PIN

For normal operation, the enable pin must be driven to a logic low. If the enable pin is driven high, the DAC7564 stops listening to the serial port. However, SCLK, $\overline{\text{SYNC}}$, and D_{IN} must not be kept floating, but must be at some logic level. This feature can be useful for applications that share the same serial port.

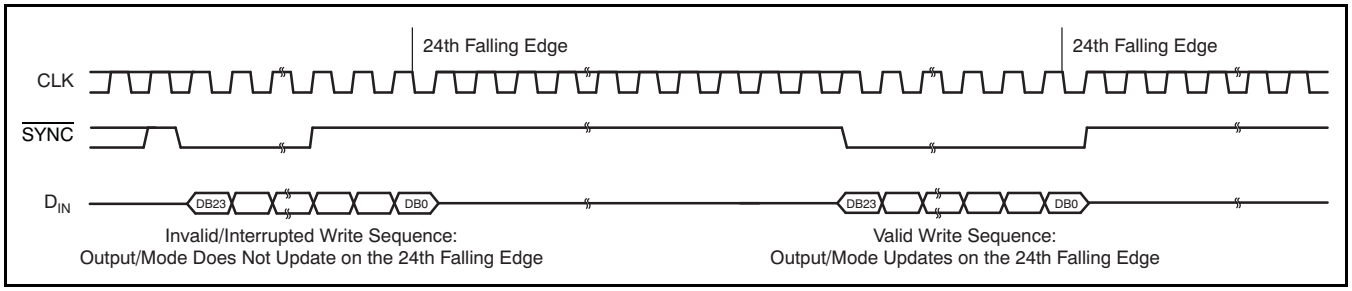


Figure 95. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-DOWN MODES

The DAC7564 has two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference, see the *Enable/Disable Internal Reference* section.

DAC Power-Down Commands

The DAC7564 uses four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register. Table 6 shows how to control the operating mode with data bits PD0 (DB16), PD1 (DB15), and PD2 (DB14).

Table 6. DAC Operating Modes

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	DAC OPERATING MODES
0	X	X	Normal operation
1	0	1	Output typically 1kΩ to GND
1	1	0	Output typically 100kΩ to GND
1	1	1	Output high-impedance

The DAC7564 treats the power-down condition as data; all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC7564s in a system; it is also possible to simultaneously power-down a channel while updating data on other channels.

When the PD0 bit is set to '0', the device works normally with its typical current consumption of 1mA at 5.5V with an input code = 2048. The reference current is included with the operation of all four DACs. However, for the three power-down modes, the supply current falls to 1.3μA at 5.5V (0.5μA at 3.6V). Not only does the supply current fall, but the output stage also switches internally from the output of the amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 6, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open circuited (High-Z). The output stage is shown in Figure 96. In other words, DB16, DB15, and DB14 = '111' represent a power-down condition with Hi-Z output impedance for a selected channel. '101' represents a power-down condition with 1kΩ output impedance, and '110' represents a power-down condition with 100kΩ output impedance.

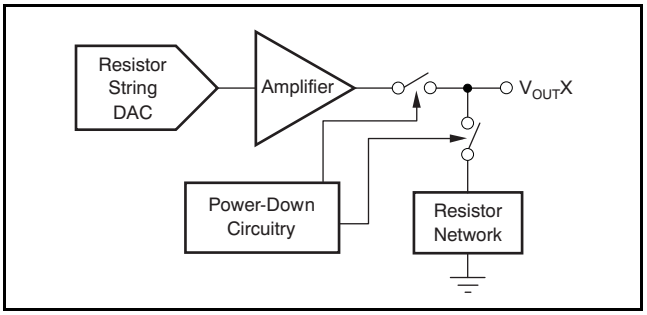


Figure 96. Output Stage During Power-Down

All analog channel circuitries are shut down when the power-down mode is exercised. However, the contents of the DAC register are unaffected when in power down. The time required to exit power-down is typically 2.5μs for V_{DD} = 5V, and 5μs for V_{DD} = 3V. See the Typical Characteristics for more information.

OPERATING EXAMPLES: DAC7564

For the following examples, ensure that DAC pins A0 and A1 are both connected to ground. Pins A0 and A1 must always match data bits DB22 and DB23 within the SPI write sequence/protocol. X = *don't care*; value can be either '0' or '1'.

Example 1: Write to Data Buffer A Through Buffer D; Load DAC A Through DAC D Simultaneously

- 1st: Write to data buffer A:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	0	0	0	D11	D10	D9	D8-D0	X

- 2nd: Write to data buffer B:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	0	1	0	D11	D10	D9	D8-D0	X

- 3rd: Write to data buffer C:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	1	0	0	D11	D10	D9	D8-D0	X

- 4th: Write to data buffer D and simultaneously update all DACs:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	1	0	0	1	1	0	D11	D10	D9	D8-D0	X

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle).

Example 2: Load New Data to DAC A Through DAC D Sequentially

- 1st: Write to data buffer A and load DAC A: DAC A output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	0	0	0	D11	D10	D9	D8-D0	X

- 2nd: Write to data buffer B and load DAC B: DAC B output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	0	1	0	D11	D10	D9	D8-D0	X

- 3rd: Write to data buffer C and load DAC C: DAC C output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	1	0	0	D11	D10	D9	D8-D0	X

- 4th: Write to data buffer D and load DAC D: DAC D output settles to specified value upon completion:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	1	1	0	D11	D10	D9	D8-D0	X

After completion of each write cycle, DAC analog output settles to the voltage specified.

Example 3: Power-Down DAC A and DAC B to 1kΩ and Power-Down DAC C and DAC D to 100kΩ Simultaneously

- 1st: Write power-down command to data buffer A: DAC A to 1kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	0	0	1	0	1	X	X	X

- 2nd: Write power-down command to data buffer B: DAC B to 1kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	0	1	1	0	1	X	X	X

- 3rd: Write power-down command to data buffer C: DAC C to 100kΩ.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	0	0	1	0	1	1	0	X	X	X

- 4th: Write power-down command to data buffer D: DAC D to 100kΩ and simultaneously update all DACs.

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	1	0	0	1	1	1	1	0	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power-down to each respective specified mode upon completion of the fourth write sequence.

Example 4: Power-Down DAC A Through DAC D to High-Impedance Sequentially

- 1st: Write power-down command to data buffer A and load DAC A: DAC A output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	0	0	1	1	1	X	X	X

- 2nd: Write power-down command to data buffer B and load DAC B: DAC B output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	0	1	1	1	1	X	X	X

- 3rd: Write power-down command to data buffer C and load DAC C: DAC C output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	1	0	1	1	1	X	X	X

- 4th: Write power-down command to data buffer D and load DAC D: DAC D output = Hi-Z:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12-DB4	DB3-DB0
0	0	0	1	0	1	1	1	1	1	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first, second, third, and fourth write sequences, respectively.

Example 5: Power-Down All Channels Simultaneously while Reference is Always Powered Up

- 1st: Write sequence for enabling the DAC7564 internal reference all the time:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	0	0	0	0	0	1	0	0	0	1	X	X

- 2nd: Write sequence to power-down all DACs to high-impedance:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	1	1	0	1	0	1	1	1	X	X	X	X

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the first and second write sequences, respectively.

Example 6: Write a Specific Value to All DACs while Reference is Always Powered Down

- 1st: Write sequence for disabling the DAC7564 internal reference all the time (after this sequence, the DAC7564 requires an external reference source to function):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	0	0	0	0	0	1	0	0	1	0	X	X

- 2nd: Write sequence to write specified data to all DACs:

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	1	1	0	1	0	0	D11	D10	D9	D8	D7–D0	X

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the fourth write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the fourth write cycle). Reference is always powered-down.

Example 7: Write a Specific Value to DAC A, while Reference is Placed in Default Mode and All Other DACs are Powered Down to High-Impedance

- 1st: Write sequence for placing the DAC7564 internal reference into default mode. Alternately, this step can be replaced by performing a power-on reset (see the *Power-On Reset* section):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	0	0	0	0	0	1	0	0	0	0	X	X

- 2nd: Write sequence to power-down all DACs to high-impedance (after this sequence, the DAC7564 internal reference powers down automatically):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	1	1	0	1	0	1	1	1	X	X	X	X

- 3rd: Write sequence to power-up DAC A to a specified value (after this sequence, the DAC7564 internal reference powers up automatically):

DB23 (A1)	DB22 (A0)	DB21 (LD1)	DB20 (LD0)	DB19	DB18 (DAC Sel 1)	DB17 (DAC Sel 0)	DB16 (PD0)	DB15	DB14	DB13	DB12	DB11-DB4	DB3-DB0
0	0	0	1	0	0	0	0	D11	D10	D9	D8	D7–D0	X

The DAC B, DAC C, and DAC D analog outputs simultaneously power-down to high-impedance, and DAC A settles to the specified value upon completion.

APPLICATION INFORMATION

INTERNAL REFERENCE

The internal reference of the DAC7564 does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 150nF or larger connected to the $V_{REF}H/V_{REF}OUT$ output is recommended. Figure 97 shows the typical connections required for operation of the DAC7564 internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

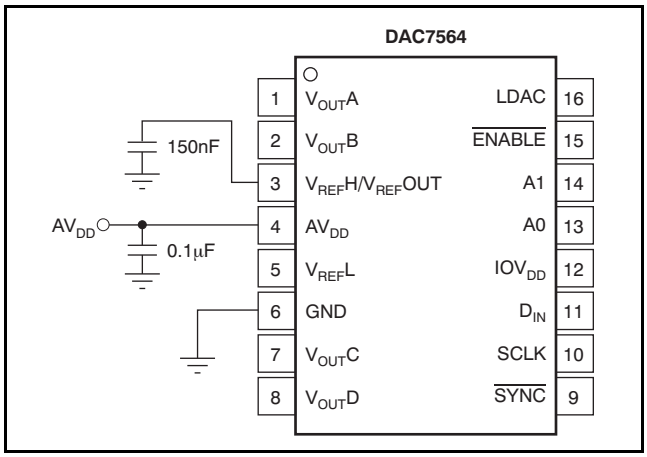


Figure 97. Typical Connections for Operating the DAC7564 Internal Reference

Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at $V_{REF}H/V_{REF}OUT$ is less than 10µV/V; see the Typical Characteristics.

Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the *box* method described by Equation 2:

$$\text{Drift Error} = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \text{ (ppm/°C)} \quad (2)$$

Where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.

V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.

V_{REF} = 2.5V, target value for reference output voltage.

The internal reference (grade C only) features an exceptional typical drift coefficient of 2ppm/°C from –40°C to +120°C. Characterizing a large number of units, a maximum drift coefficient of 5ppm/°C (grade C only) is observed. Temperature drift results are summarized in the Typical Characteristics.

Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in Figure 8, *Internal Reference Noise*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at $V_{REF}H/V_{REF}OUT$ without any external components is depicted in Figure 7, *Internal Reference Noise Density vs Frequency*. Another noise density spectrum is also shown in Figure 7. This spectrum was obtained using a 4.8µF load capacitor at $V_{REF}H/V_{REF}OUT$ for noise filtering. Internal reference noise impacts the DAC output noise; see the *DAC Noise Performance* section for more details.

Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 98. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are summarized in the Typical Characteristics. Force and sense lines should be used for applications that require improved load regulation.

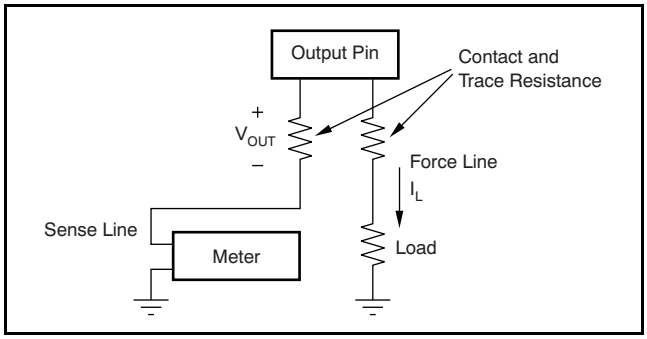


Figure 98. Accurate Load Regulation of the DAC7564 Internal Reference

Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses (see Figure 6, the typical long-term stability curve). The typical drift value for the internal reference is 50ppm from 0 hours to 1900 hours. This parameter is characterized by powering-up and measuring 20 units at regular intervals for a period of 1900 hours.

Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at +25°C, cycling the device through the operating temperature range, and returning to +25°C. Hysteresis is expressed by Equation 3:

$$V_{HYST} = \left(\frac{|V_{REF\_PRE} - V_{REF\_POST}|}{V_{REF\_NOM}} \right) \times 10^6 \text{ (ppm/°C)} \quad (3)$$

Where:

V_{HYST} = thermal hysteresis.

V_{REF_PRE} = output voltage measured at +25°C pre-temperature cycling.

V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to +120°C, and returns to +25°C.

DAC NOISE PERFORMANCE

Typical noise performance for the DAC7564 with the internal reference enabled is shown in Figure 54 to Figure 56. Output noise spectral density at the V_{OUT} pin versus frequency is depicted in Figure 54 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 120nV/$\sqrt{Hz}$ at 1kHz and 100nV/$\sqrt{Hz}$ at 1MHz. High-frequency noise can be improved by filtering the reference noise as shown in Figure 55, where a 4.8µF load capacitor is connected to the $V_{REF}H/V_{REF}OUT$ pin and compared to the no-load condition. Integrated output noise between 0.1Hz and 10Hz is close to 6µV_{PP} (midscale), as shown in Figure 56.

BIPOLAR OPERATION USING THE DAC7564

The DAC7564 is designed for single-supply operation, but a bipolar output range is also possible using the circuit in either Figure 99 or Figure 100. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated with Equation 4:

$$V_O = \left[V_{REF} \times \left[\frac{D}{4096} \right] \times \left[\frac{R_1 + R_2}{R_1} \right] - V_{REF} \times \left[\frac{R_2}{R_1} \right] \right] \quad (4)$$

where *D* represents the input code in decimal (0–4095).

With $V_{REF}H$ = 5V, $R_1 = R_2$ = 10kΩ.

$$V_O = \left[\frac{10 \times D}{4096} \right] - 5V \quad (5)$$

This result has an output voltage range of ±5V with 0000h corresponding to a –5V output and 0FFFh corresponding to a +5V output, as shown in Figure 99. Similarly, using the internal reference, a ±2.5V output voltage range can be achieved, as Figure 100 shows.

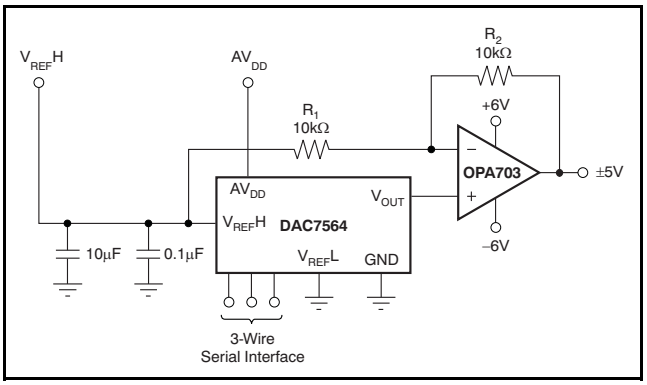


Figure 99. Bipolar Output Range Using External Reference at 5V

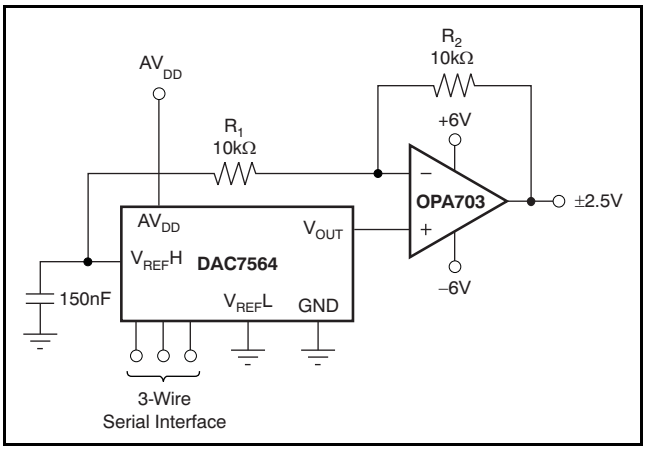


Figure 100. Bipolar Output Range Using Internal Reference

MICROPROCESSOR INTERFACING

DAC SPI Interfacing

Care must be taken with the digital control signals that are applied directly to the DAC, especially with the SYNC pin. The SYNC pin must not be toggled without having a full SCLK pulse in between. If this condition is violated, the SPI interface locks up in an erroneous state, causing the DAC to behave incorrectly and have errors. The DAC can be recovered from this faulty state by writing a valid SPI command or using the SYNC pin correctly; communication will then be restored. Avoid glitches and transients on the SYNC line to ensure proper operation.

DAC7564 to an 8051 Interface

Figure 101 shows a serial interface between the DAC7564 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC7564, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051; in this case, port line P3.3 is used. When data are to be transmitted to the DAC7564, P3.3 is taken low. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC7564 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this requirement into account, and *mirror* the data as needed.

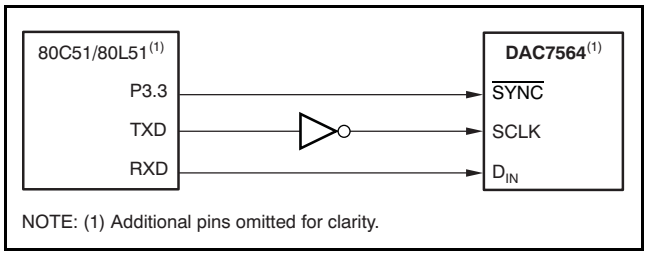


Figure 101. DAC7564 to 80C51/80L51 Interface

DAC7564 to Microwire Interface

Figure 102 shows an interface between the DAC7564 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DAC7564 on the rising edge of the SK signal.

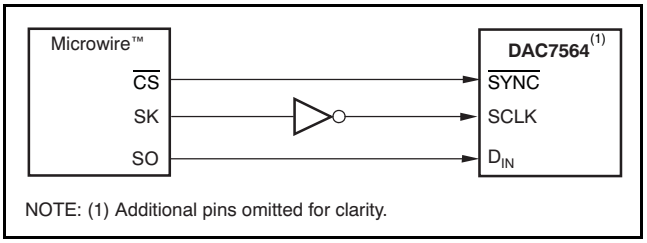


Figure 102. DAC7564 to Microwire Interface

DAC7564 to 68HC11 Interface

Figure 103 shows a serial interface between the DAC7564 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC7564, while the MOSI output drives the serial data line of the DAC. The SYNC signal derives from a port line (PC7), similar to the 8051 diagram.

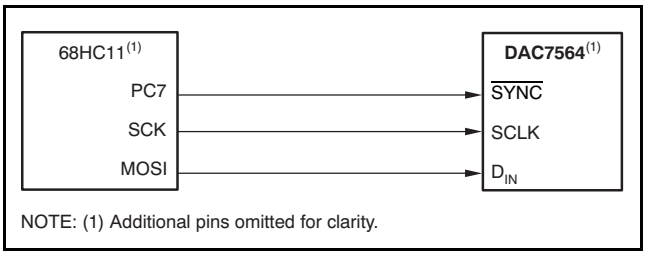


Figure 103. DAC7564 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is held low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC7564, PC7 is left low after the first eight bits are transferred; then, a second and third serial write operation are performed to the DAC. PC7 is taken high at the end of this procedure.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC7564 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

As a result of the single ground pin of the DAC7564, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor and 0.1µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply and remove the high-frequency noise.

PARAMETER DEFINITIONS

With the increased complexity of many different specifications listed in product data sheets, this section summarizes selected specifications related to digital-to-analog converters.

STATIC PERFORMANCE

Static performance parameters are specifications such as differential nonlinearity (DNL) or integral nonlinearity (INL). These are dc specifications and provide information on the accuracy of the DAC. They are most important in applications where the signal changes slowly and accuracy is required.

Resolution

Generally, the DAC resolution can be expressed in different forms. Specifications such as IEC 60748-4 recognize the numerical, analog, and relative resolution. The numerical resolution is defined as the number of digits in the chosen numbering system necessary to express the total number of steps of the transfer characteristic, where a step represents both a digital input code and the corresponding discrete analogue output value. The most commonly-used definition of resolution provided in data sheets is the numerical resolution expressed in bits.

Least Significant Bit (LSB)

The least significant bit (LSB) is defined as the smallest value in a binary coded system. The value of the LSB can be calculated by dividing the full-scale output voltage by 2^n, where *n* is the resolution of the converter.

Most Significant Bit (MSB)

The most significant bit (MSB) is defined as the largest value in a binary coded system. The value of the MSB can be calculated by dividing the full-scale output voltage by 2. Its value is one-half of full-scale.

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity (INL) is defined as the maximum deviation between the real transfer function and a straight line passing through the endpoints of the ideal DAC transfer function. DNL is measured in LSBs.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is defined as the maximum deviation of the real LSB step from the ideal 1LSB step. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. If the DNL is less than 1LSB, the DAC is said to be monotonic.

Full-Scale Error

Full-scale error is defined as the deviation of the real full-scale output voltage from the ideal output voltage while the DAC register is loaded with the full-scale code. Ideally, the output should be V_{DD} – 1 LSB. The full-scale error is expressed in percent of full-scale range (%FSR).

Offset Error

The offset error is defined as the difference between actual output voltage and the ideal output voltage in the linear region of the transfer function. This difference is calculated by using a straight line defined by two codes. Since the offset error is defined by a straight line, it can have a negative or positve value. Offset error is measured in mV.

Zero-Code Error

The zero-code error is defined as the DAC output voltage, when all '0's are loaded into the DAC register. Zero-scale error is a measure of the difference between actual output voltage and ideal output voltage (0V). It is expressed in mV. It is primarily caused by offsets in the output amplifier.

Gain Error

Gain error is defined as the deviation in the slope of the real DAC transfer characteristic from the ideal transfer function. Gain error is expressed as a percentage of full-scale range (%FSR).

Full-Scale Error Drift

Full-scale error drift is defined as the change in full-scale error with a change in temperature. Full-scale error drift is expressed in units of %FSR/°C.

Offset Error Drift

Offset error drift is defined as the change in offset error with a change in temperature. Offset error drift is expressed in µV/°C.

Zero-Code Error Drift

Zero-code error drift is defined as the change in zero-code error with a change in temperature. Zero-code error drift is expressed in µV/°C.

Gain Temperature Coefficient

The gain temperature coefficient is defined as the change in gain error with changes in temperature. The gain temperature coefficient is expressed in ppm of FSR/°C.

Power-Supply Rejection Ratio (PSRR)

Power-supply rejection ratio (PSRR) is defined as the ratio of change in output voltage to a change in supply voltage for a full-scale output of the DAC. The PSRR of a device indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is measured in decibels (dB).

Monotonicity

Monotonicity is defined as a slope whose sign does not change. If a DAC is monotonic, the output changes in the same direction or remains at least constant for each step increase (or decrease) in the input code.

DYNAMIC PERFORMANCE

Dynamic performance parameters are specifications such as settling time or slew rate, which are important in applications where the signal rapidly changes and/or high frequency signals are present.

Slew Rate

The output slew rate (SR) of an amplifier or other electronic circuit is defined as the maximum rate of change of the output voltage for all possible input signals.

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right)$$

Where $\Delta V_{OUT}(t)$ is the output produced by the amplifier as a function of time *t*.

Output Voltage Settling Time

Settling time is the total time (including slew time) for the DAC output to settle within an error band around its final value after a change in input. Settling times are specified to within ±0.003% (or whatever value is specified) of full-scale range (FSR).

Code Change/Digital-to-Analog Glitch Energy

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nanovolts-second (nV-s), and is measured when the digital input code changes by 1LSB at the major carry transition.

Digital Feedthrough

Digital feedthrough is defined as impulse seen at the output of the DAC from the digital inputs of the DAC. It is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus; that is, from all '0's to all '1's and vice versa.

Channel-to-Channel DC Crosstalk

Channel-to-channel dc crosstalk is defined as the dc change in the output level of one DAC channel in response to a change in the output of another DAC channel. It is measured with a full-scale output change on one DAC channel, while monitoring another DAC channel remains at midscale; it is expressed in LSB.

Channel-to-Channel AC Crosstalk

AC crosstalk in a multi-channel DAC is defined as the amount of ac interference experienced on the output of a channel at a frequency (f) (and its harmonics), when the output of an adjacent channel changes its value at the rate of frequency (f). It is measured with one channel output oscillating with a sine wave of 1kHz frequency while monitoring the amplitude of 1kHz harmonics on an adjacent DAC channel output (kept at zero scale); it is expressed in dB.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is defined as the ratio of the root mean-squared (RMS) value of the output signal divided by the RMS values of the sum of all other spectral components below one-half the output frequency, not including harmonics or dc. SNR is measured in dB.

Total Harmonic Distortion (THD)

Total harmonic distortion + noise is defined as the ratio of the RMS values of the harmonics and noise to the value of the fundamental frequency. It is expressed in a percentage of the fundamental frequency amplitude at sampling rate f_S.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range (SFDR) is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from dc to the full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of the DAC. SFDR is specified in decibels relative to the carrier (dBc).

Signal-to-Noise plus Distortion (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing any internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DAC Output Noise Density

Output noise density is defined as internally-generated random noise. Random noise is characterized as a spectral density (nV/$\sqrt{Hz}$). It is measured by loading the DAC to midscale and measuring noise at the output.

DAC Output Noise

DAC output noise is defined as any voltage deviation of DAC output from the desired value (within a particular frequency band). It is measured with a DAC channel kept at midscale while filtering the output voltage within a band of 0.1Hz to 10Hz and measuring its amplitude peaks. It is expressed in terms of peak-to-peak voltage (V_{pp}).

Full-Scale Range (FSR)

Full-scale range (FSR) is the difference between the maximum and minimum analog output values that the DAC is specified to provide; typically, the maximum and minimum values are also specified. For an *n*-bit DAC, these values are usually given as the values matching with code 0 and 2^n.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2008) to Revision B	Page
• Changed Output Voltage parameter min/max values from 2.4995 and 2.5005 to 2.4975 and 2.5025, respectively	4
• Changed Initial Accuracy parameter min/max values from –0.02 and 0.02 to –0.1 and 0.1, respectively	4
• Changed values for SCLK High TIme parameter from 20 and 10 to 10 and 20.	7
• Added *DAC SPI Interfacing* subsection to *Microprocessor Interfacing* section	39

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7564IAPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7564	Samples
DAC7564IAPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7564	Samples
DAC7564ICPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7564	Samples
DAC7564ICPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7564	Samples
DAC7564ICPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7564	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

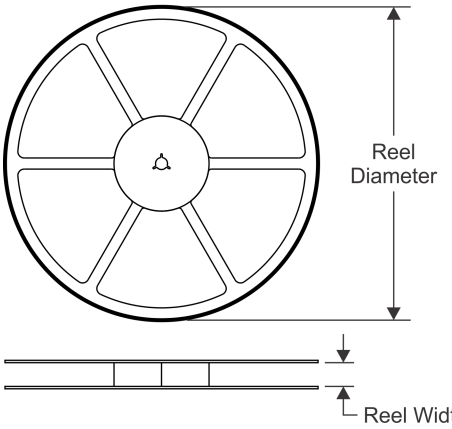
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

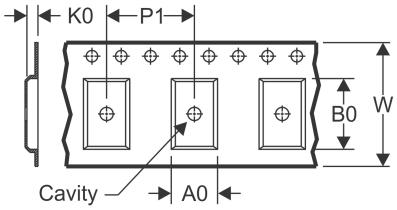
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

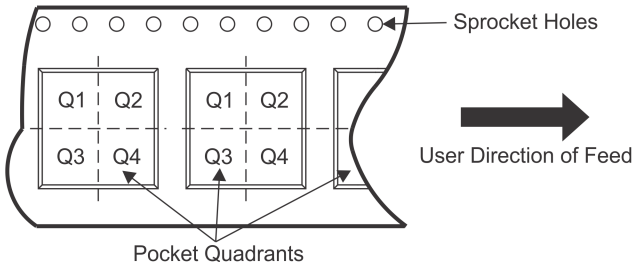


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

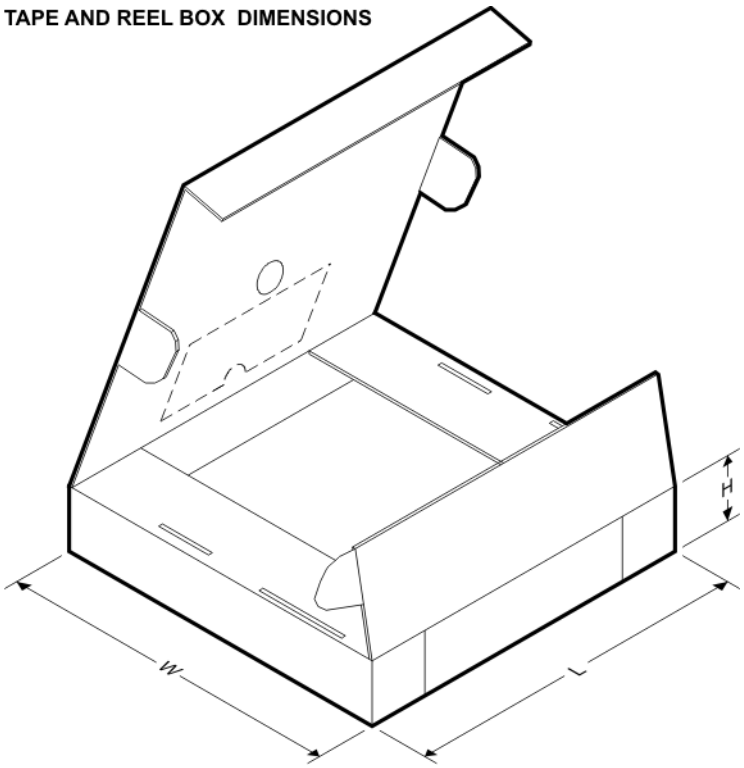
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7564IAPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC7564ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

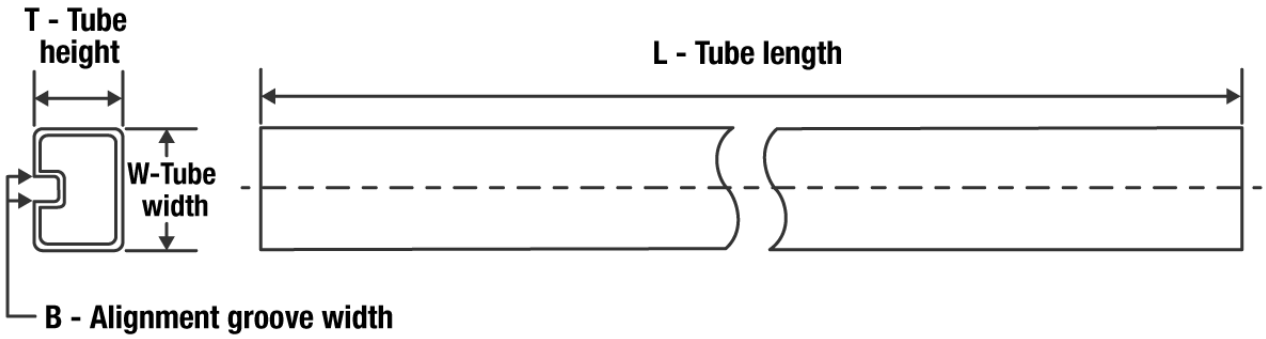
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7564IAPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
DAC7564ICPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

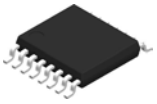
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7564IAPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC7564ICPW	PW	TSSOP	16	90	530	10.2	3600	3.5

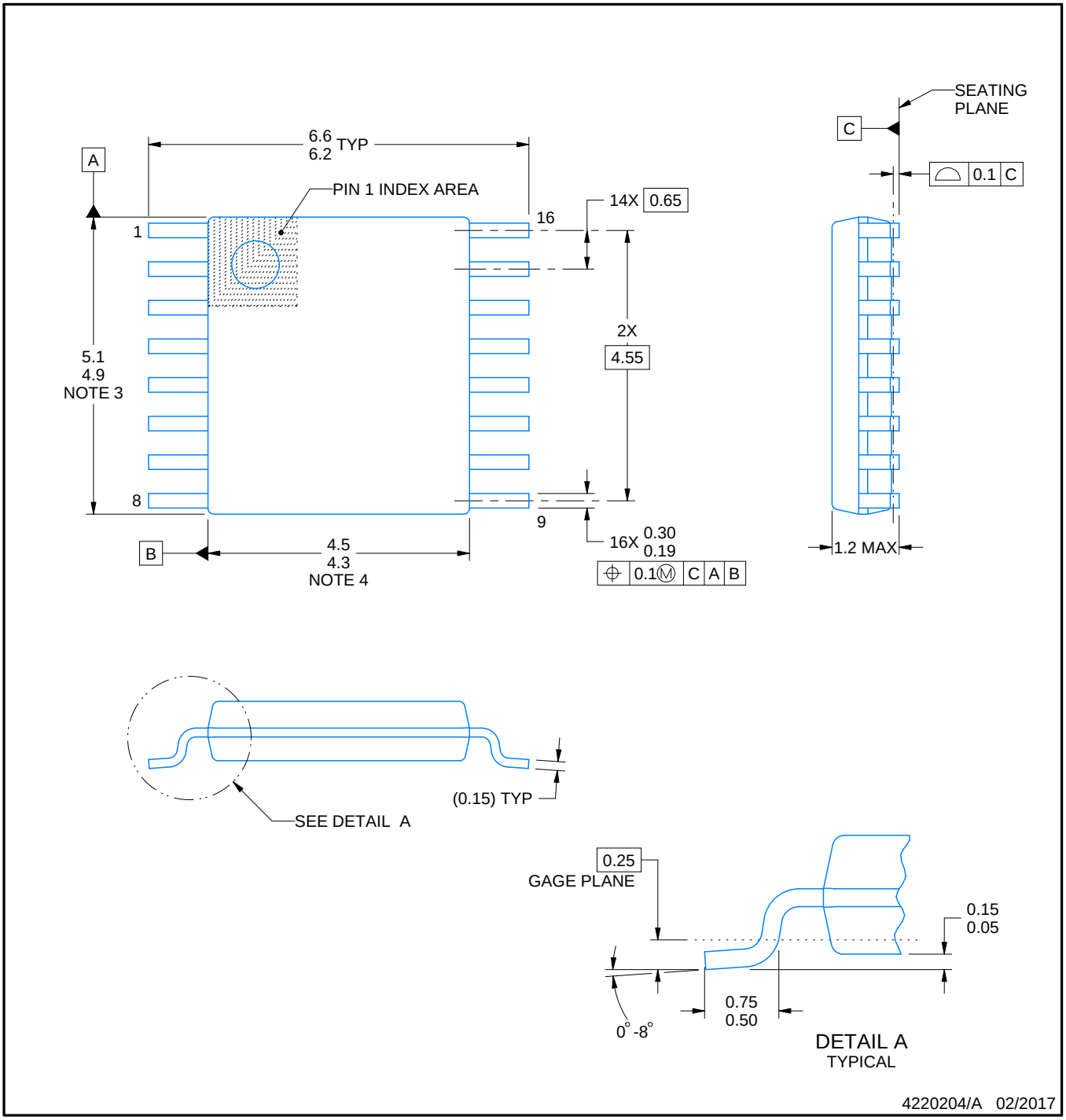
PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

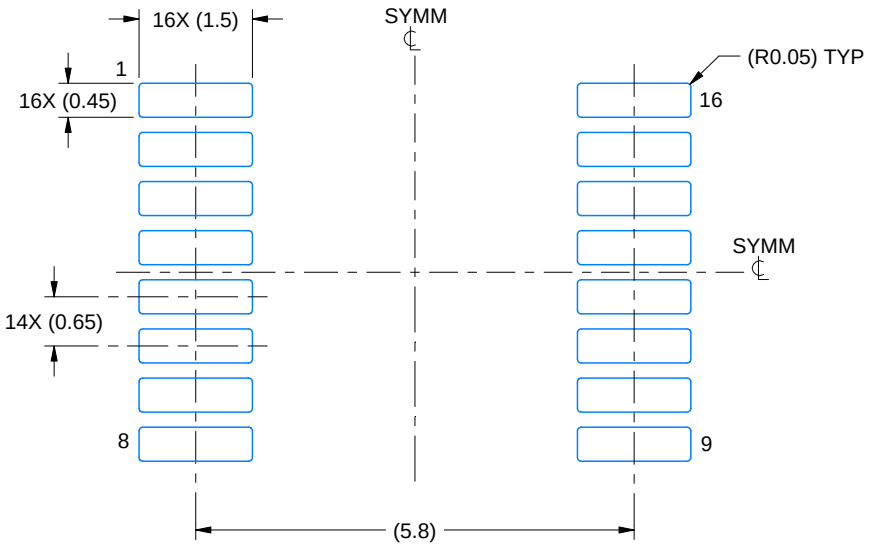
SMALL OUTLINE PACKAGE





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



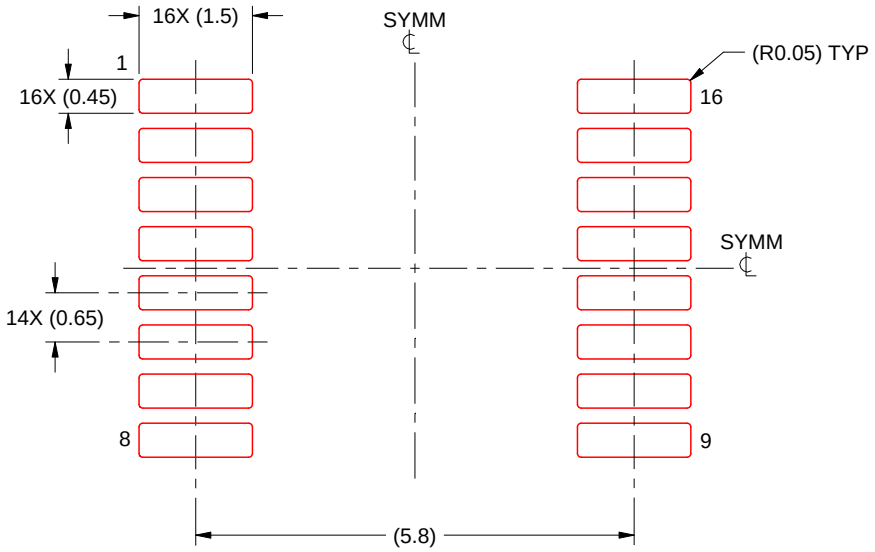
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
DRV8243-Q1
SLVSG23A – DECEMBER 2021 – REVISED JANUARY 2022

DRV8243-Q1 Automotive H-Bridge Driver with Integrated Current Sense and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 4.5-V to 35-V (40-V abs. max) operating range
- VQFN-HR package: R_{ON_LS} + R_{ON_HS}: 84 mΩ
- HVSSOP package: R_{ON_LS} + R_{ON_HS}: 98 mΩ
- I_{OUT} Max = 12 A
- PWM frequency operation up to 25 KHz with automatic dead time assertion
- Configurable slew rate and spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated current sense (eliminates shunt resistor)
- Proportional load current output on IPROPI pin
- Configurable current regulation
- Protection and diagnostic features with configurable fault reaction (latched or retry)
  - Load diagnostics in both the off-state and on-state to detect open load and short circuit
  - Voltage monitoring on supply (VM)
  - Over current protection
  - Over temperature protection
  - Fault indication on nFAULT pin
- Supports 3.3-V, 5-V logic inputs
- Low sleep current - 1µA typical at 25°C
- 3 variants - HW (H), SPI (S) or SPI (P)
- Configurable control modes:
  - Single full bridge using PWM or PH/EN mode
  - Two half-bridges using Independent mode
- Device family comparison table

2 Applications

- Automotive brushed DC motors, Solenoids
- Door modules , mirror modules, and seat modules
- Body control module (BCM)
- E-Shifter
- Gas engine systems
- On board charger

3 Description

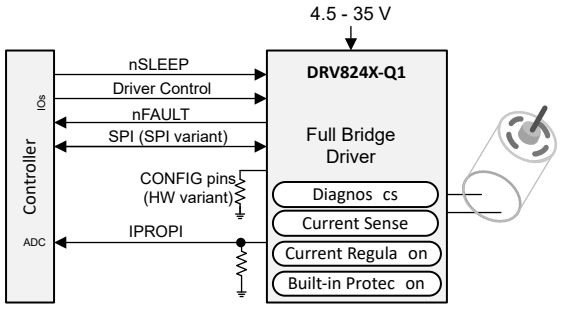
The DRV824x-Q1 family of devices is a fully integrated H-bridge driver intended for a wide range of automotive applications. The device can be configured as a single full-bridge driver or as two independent half-bridge drivers. Designed in a BiCMOS high power process technology node, this monolithic family of devices in a power package offer excellent power handling and thermal capability while providing compact package size, ease of layout, EMI control, accurate current sense, robustness, and diagnostic capability. This family also has identical pin function with scalable R_{ON} (current capability) to support different loads.

The devices integrate a N-channel H-bridge, charge pump regulator, high-side current sensing and regulation, current proportional output, and protection circuitry. A low-power sleep mode is provided to achieve low quiescent current. The devices offer voltage monitoring and load diagnostics as well as protection features against over current and over temperature. Fault conditions are indicated on nFAULT pin. The devices are available in three variants - hardwired interface: HW (H) and two SPI interface variants: SPI(P) and SPI(S), with SPI (P) for externally supplied logic supply and SPI (S) for internally generated logic supply. The SPI interface variants offer more flexibility in device configuration and fault observability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (nominal)
DRV8243-Q1	VQFN-HR (14)	3 mm X 4.5 mm
DRV8243-Q1(2)	HVSSOP (28)	3 mm X 7.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet
(2) Device available for preview only.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (January 2022)	Page
• Updated device status to Mixed Production	1

5 Device Comparison

Table 5-1 summarizes the R_{ON} and package differences between devices in the DRV824X-Q1 family.

Table 5-1. Device Comparison

PART NUMBER(2)	(LS + HS) R_{ON}	I_{OUT} MAX	PACKAGE	BODY SIZE (nominal)	Variants
DRV8243-Q1	84 mΩ	12 A	VQFN-HR (14)	3 mm X 4.5 mm	HW (H), SPI (S)
DRV8243-Q1(3)	98 mΩ	12 A	HVSSOP (28)	3 mm X 7.3 mm	HW (H), SPI (S), SPI (P)
DRV8244-Q1	47 mΩ	21 A	VQFN-HR (16)	3 mm X 6 mm	HW (H), SPI (S)(1)
DRV8244-Q1	60 mΩ	21 A	HVSSOP (28)	3 mm X 7.3 mm	HW (H), SPI (S), SPI (P)
DRV8245-Q1	32 mΩ	32 A	VQFN-HR (16)	3.5 mm X 5.5 mm	HW (H)(1), SPI (S)
DRV8245-Q1	40 mΩ	32 A	HTSSOP (28)	4.4 mm X 9.7 mm	HW (H), SPI (S), SPI (P)

(1) **DRV8245HRXZQ1** and **DRV8244SRYJQ1** exceptions:
   a. Off-state diagnostics (OLP) - This feature is NOT available for use in **DRV8244SRYJQ1** (SPI(S) variant in VQFN-HR (16) package) and **DRV8245HRXZQ1** (HW(H) variant in VQFN-HR (16) package) - recommend to disable OLP in application.
   b. Slew rate setting (SR = 3'b000, 3'b001, 3'b010) for **DRV8244SRYJQ1** (SPI(S) variant in VQFN-HR (16) package) and LVL2 for **DRV8245HRXZQ1** (HW(H) variant in VQFN-HR (16) package) is NOT available in Independent mode operation using low-side recirculation (low-side load) - recommend to use other settings for slew rate control.

(2) This is the product datasheet for the DRV8243-Q1. Please reference other device variant data sheets for additional information.

(3) Device available for preview only.

Table 5-2 summarizes the feature differences between the SPI and HW interface variants in the DRV824X-Q1 family. In general, the SPI variant offers more configurability, bridge control options, diagnostic feedback, redundant driver shutoff, improved Pin FMEA and additional features.

In addition, the SPI variant has two options - **SPI (S) variant and SPI (P) variant**. The SPI (P) variant supports an external, low voltage 5 V supply to the device through the VDD pin for the device logic, whereas in the SPI (S) variant, this supply is internally derived from the VM pin. With this external logic supply, the SPI (P) variant avoids device brown out (reset of device) during VM under voltage transients.

Table 5-2. SPI Variant vs HW Variant Comparison

FUNCTION	HW (H) Variant	SPI (S) Variant	SPI (P) Variant
Bridge control	Pin only	Individual pin **"and/or"** register bit with pin status indication (Refer Register Pin control)	
Sleep function	Available through nSLEEP pin		Not available
External logic supply to the device	Not supported	Not supported	Supported through VDD pin
Clear fault command	Reset pulse on nSLEEP pin	SPI CLR_FAULT command	
Slew rate	6 levels	8 levels	
Over current protection (OCP)	Fixed at the highest setting	3 choices for thresholds, 4 choices for filter time	
ITRIP regulation	5 levels with disable & fixed TOFF time	7 levels with disable & indication, with programmable TOFF time	
Individual fault reaction configuration between retry or latched behavior	Not supported, either all latched or all retry	Supported	
Detailed fault logging and device status feedback	Not supported, nFAULT pin monitoring necessary	Supported, nFAULT pin monitoring optional	
VM over voltage	Fixed	4 threshold choices	
On-state (Active) diagnostics	Not supported	Supported for high-side loads	
Spread spectrum clocking (SSC)	Not supported	Supported	
Additional driver states in PWM mode	Not supported	Supported	
Hi-Z for individual half-bridge in Independent mode	Not supported	Supported (SPI register only)	

Note

There are some functional improvements as well as parametric corrections between the pre-production samples and final production devices. These differences are summarized in the feature changes table and errata table. The sample types can be differentiated visually by their package symbolization. Pre-production samples are pre-fixed with a "P" on the package symbolization. Additionally, for the SPI variant, it is possible to electrically differentiate between the samples by reading the DEVICE_ID register byte (refer to Table 5-5).

Table 5-3 summarizes the feature changes between the pre-production samples and final production devices.

Table 5-3. Feature Changes Between Pre-Production and Production Samples

Feature	Pre-Production Samples	Final Product
Parallel Mode	Parallel mode available	Parallel mode removed. Use the DRV814X equivalent device for this.
Slew Rate	DRV824X: SR = ~[1.6 12* 18* 23 28 33 38 43] V/usec HW only 6 choices only for high-side recirculation *Additional settings in SPI variant only	DRV824X: SR = ~[1.2 4* 6.7* 11.4 17 22 32 41] V/usec for high-side recirculation *Additional settings in SPI variant only
OCP limit in DRV8243	Set at 9 A min	Increased to 12 A
ITRIP regulation levels	VTRIP = [DIS 2.97 2.64 2.31 1.98 1.65] V	VTRIP = [DIS 2.97 2.64 2.31 1.98 1.65* 1.41* 1.18] V *Additional settings in SPI only
SPI variants only - Reg / Pin control	When SPI_IN is unlocked, the input pins, DRVOFF, EN_IN1 and PH_IN2, become don't care and the output is controlled by their equivalent register bits only.	DRVOFF_SEL, EN_IN1_SEL, PH_IN2_SEL introduced to configure the logical combination (AND/OR) of each of the three input pins (DRVOFF, EN/IN1, PH/IN2) with their register bit counterparts, when SPI_IN is unlocked. (Refer Register Pin control)
PWM truth table	[IN1 IN2] = [L L] => HiZ, [H H] => Brake	[IN1 IN2] = [H H] => HiZ, [L L] => Brake. This eliminates risk for direction reversal for a short to GND or Open in PWM mode.
SPI variants only - Register map expansion	As listed in the register map section	Changes allow for efficient diagnostic monitoring, in addition to support extended configurability 1. STATUS2 byte added for DRVOFF_STAT and ACTIVE bit indication 2. OLP_CMP moved to STATUS2 with a redundant ACTIVE bit replacing OLP_CMP in the STATUS1 3. CONFIG4 byte added to accommodate configurability for OCP control and output control through input pins & their equivalent register bits
Spread spectrum clocking	1. SPI variant - Feature enabled by default 2. HW variant - Feature always enabled	1. SPI variant - Feature disabled by default 2. HW variant - Feature always disabled
Over current protection	Fixed thresholds	Added 2 bits of OCP_SEL to lower OCP threshold and 2 bits of OCP_TSEL to change the OCP filter time.
SPI (P) variant	Not available	Additional SPI (P) variant – nSLEEP/VIO pin function changed to external VDD input as logic supply
OLP CMP reference	Can't differentiate between open and short for a half-bridge use case during off-state diagnostics (OLP)	Thresholds swapped in half-bridge operation to enable differentiation between short and open for a half-bridge use case during off-state diagnostics (OLP)
SPI variant only – Frame length error	Processes write commands for 1. length ≥ 16 SCLKs for regular SPI frame or 2. length ≥ 16 + "N" x 16 SCLKs for daisy chain SPI frame, where N = number of peripherals Only shorter lengths are rejected with SPI_ERR	Improved feature to process write commands for 1. length = 16 SCLKs for regular SPI frame or 2. length = 16 + "N" x 16 SCLKs for daisy chain SPI frame, where N = number of peripherals All other lengths are rejected with SPI_ERR

Table 5-4. Errata Fixes Between Pre-Production and Production Samples

Errata	Pre-Production Samples	Final Product
HW (H) variant only - Mean shift in determining the resistance to GND at the CONFIG pins	Recommend to use **1%** resistor on the CONFIG pins to ensure expected behavior	Fixed the mean shift to ensure 10% resistor (datasheet target) is OK for use on the CONFIG pins as per datasheet
Digital input pin - hysteresis is lower than expected	Hysteresis measured: [Min/ Typ/ Max] = [30/ 60/ 90] mV	Fixed to meet datasheet target of: [Min/ Typ/ Max] = [70/ 100/ 150] mV
ITRIP regulation accuracy – lower than expected	VTRIP threshold comparison could be ~ +/- 12%	Fixed to meet datasheet target of < +/- 10%
Over current protection threshold mean shift of high-side FET for DRV8245 closer to the lower threshold	OCP of HSx FET could be as low as 28 A	Fixed the mean value so that min OCP is always > 32 A(datasheet target)

Table 5-5. Differentiating Between Pre-Production and Production Samples

Device	Pre-Production Samples		Final Product	
	Package Symbolization	DEVICE_ID Register	Package Symbolization	DEVICE_ID Register
DRV8243H-Q1	P8243X	Not applicable	8243H	Not applicable
DRV8244H-Q1	P8244X	Not applicable	8244H	Not applicable
DRV8245H-Q1	P8245X	Not applicable	8245H	Not applicable
DRV8243S-Q1	P8243X	0 x 30	8243S	0 x 32
DRV8244S-Q1	P8244X	0 x 40	8244S	0 x 42
DRV8245S-Q1	P8245X	0 x 50	8245S	0 x 52
DRV8243P-Q1	Not available		8243P	0 x 36
DRV8244P-Q1	Not available		8244P	0 x 46
DRV8245P-Q1	Not available		8245P	0 x 56

6 Pin Configuration and Functions

6.1 HW Variant

6.1.1 HVSSOP (28) package

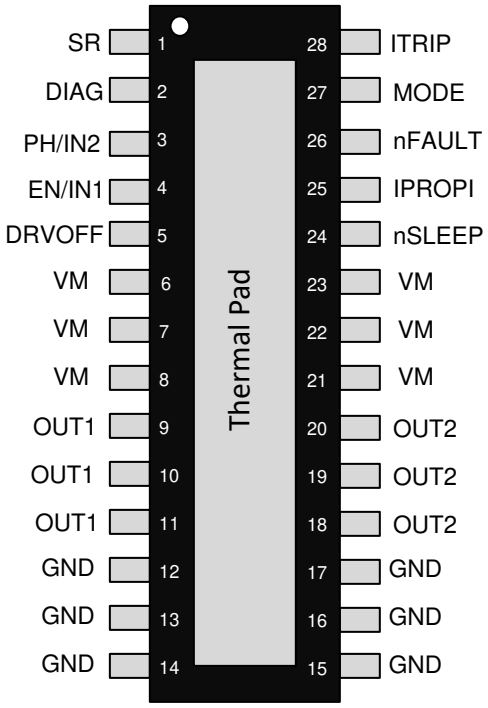


Figure not drawn to scale

Figure 6-1. DRV8243H-Q1 HW variant in HVSSOP (28) package

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SR	I	Device configuration pin for Slew Rate control . For details, refer to Slew Rate in the Device Configuration section.
2	DIAG	I	Device configuration pin for load type indication and fault reaction configuration. For details, refer to DIAG in the Device Configuration section.
3	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
4	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
5	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
6, 7, 8, 21, 22, 23	VM	P	Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
9, 10, 11	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load. Must combine with the rest of OUT1 pins (3 total) to support device current capability.
12, 13, 14, 15, 16, 17	GND	G	Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.
18, 19, 20	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load. Must combine with the rest of OUT2 pins (3 total) to support device current capability.
24	nSLEEP	I	Controller input pin for SLEEP. For details, see the Bridge Control section.
25	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
26	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.

Table 6-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
27	MODE	I	Device configuration pin for MODE. For details, refer to the Device Configuration section.
28	ITRIP	I	Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the Device Configuration section.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.1.2 VQFN-HR (14) package

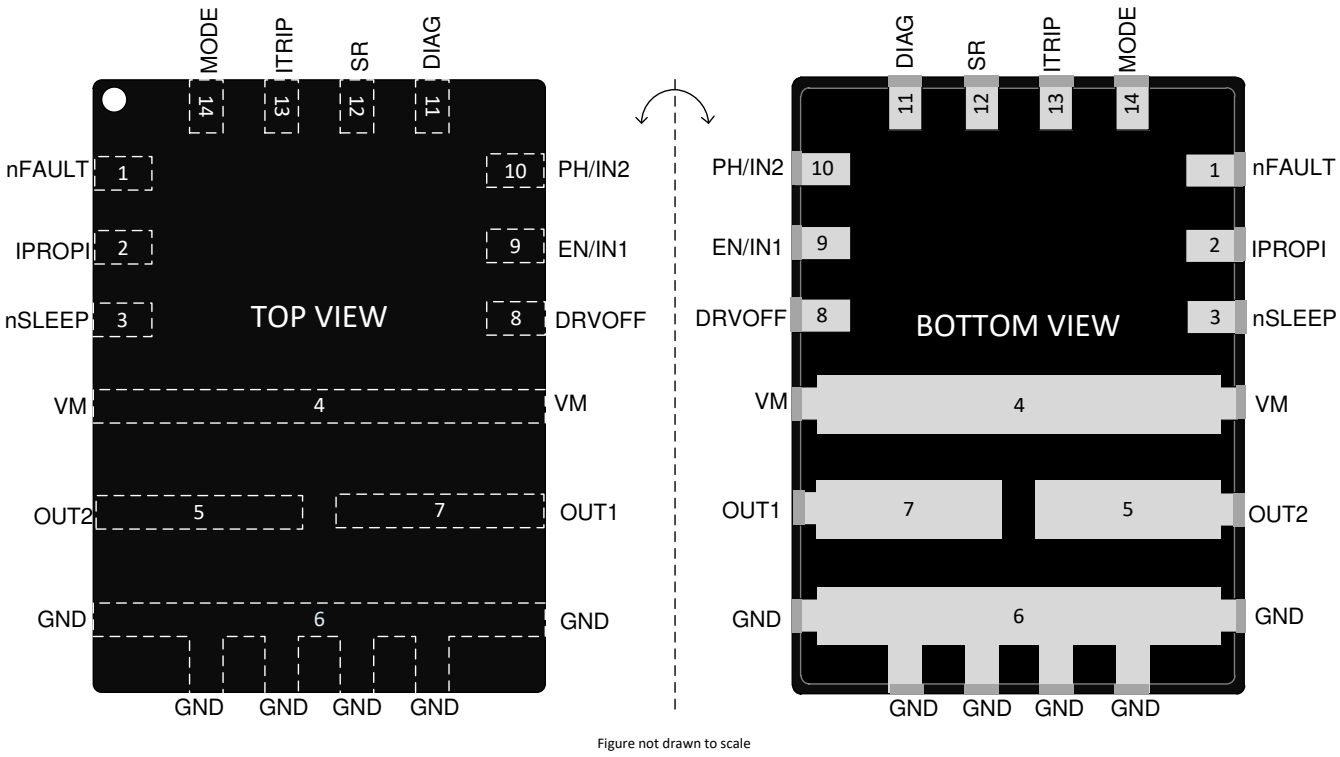


Figure not drawn to scale

Figure 6-2. DRV8243H-Q1 HW variant in VQFN-HR (14) package

Table 6-2. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
2	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
3	nSLEEP	I	Controller input pin for SLEEP . For details, see the Bridge Control section.
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
11	DIAG	I	Device configuration pin for load type indication and fault reaction configuration. For details, refer to DIAG in the Device Configuration section.

Table 6-2. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
12	SR	I	Device configuration pin for Slew Rate control . For details, refer to Slew Rate in the Device Configuration section.
13	ITRIP	I	Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the Device Configuration section.
14	MODE	I	Device configuration pin for MODE. For details, refer to the Device Configuration section.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.2 SPI Variant

6.2.1 HVSSOP (28) package

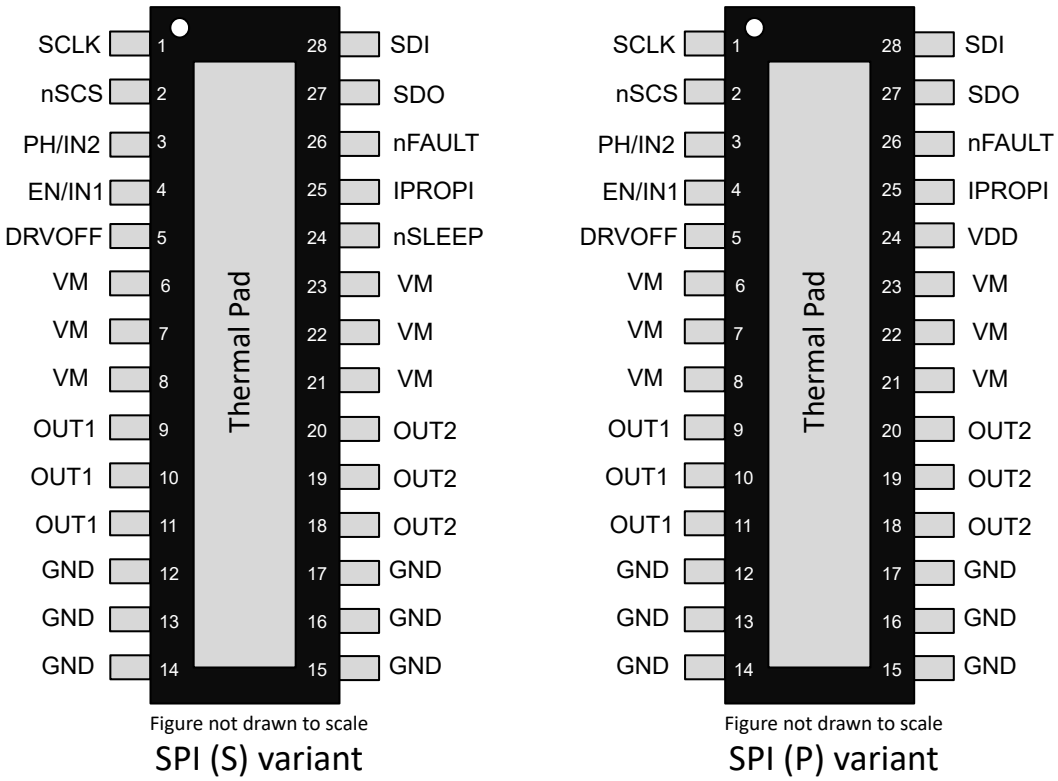


Figure 6-3. DRV8243S-Q1 SPI variant in HVSSOP (28) package

Table 6-3. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI - Serial Clock input.
2	nSCS	I	SPI - Chip Select. An active low on this pin enables the serial interface communication.
3	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
4	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
5	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
6, 7, 8, 21, 22, 23	VM	P	Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
9, 10, 11	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load. Must combine with the rest of OUT1 pins (3 total) to support device current capability.

Table 6-3. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
12, 13, 14, 15, 16, 17	GND	G	Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.
18, 19, 20	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load. Must combine with the rest of OUT2 pins (3 total) to support device current capability.
24	nSLEEP	I	SPI (S) variant: Controller input pin for SLEEP. For details, see the Bridge Control section. Also VIO logic level for SDO.
	VDD	P	SPI (P) variant: Logic power supply to the device.
25	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
26	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
27	SDO	PP	SPI - Serial Data Output. Data is updated at the rising edge of SCLK.
28	SDI	I	SPI - Serial Data Input. Data is captured at the falling edge of SCLK.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.2.2 VQFN-HR (14) package

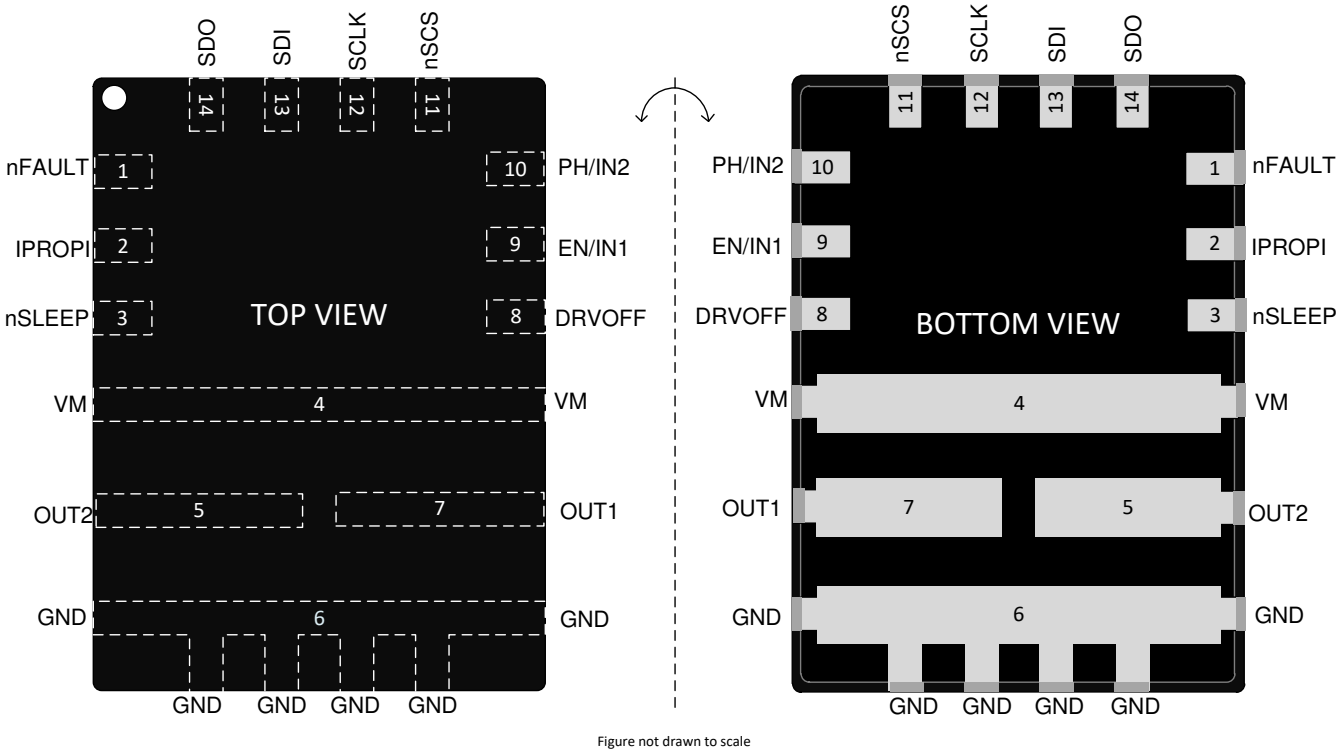


Figure not drawn to scale

Figure 6-4. DRV8243S-Q1 SPI variant in VQFN-HR (14) package

Table 6-4. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
2	IPROPI	O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
3	nSLEEP	I	Controller input pin for SLEEP. For details, see the Bridge Control section. Also VIO logic level for SDO.

Table 6-4. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
11	nSCS	I	SPI - Chip Select. An active low on this pin enables the serial interface communication.
12	SCLK	I	SPI - Serial Clock input.
13	SDI	I	SPI - Serial Data Input. Data is captured at the falling edge of SCLK.
14	SDO	PP	SPI - Serial Data Output. Data is updated at the rising edge of SCLK.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	–0.3	40	V
Power supply transient voltage ramp	VM		2	V/µs
Output pin voltage	OUT1, OUT2	-0.9	V_{VM} + 0.9	V
Output pin current	OUT1, OUT2	Internally limited(2)		A
Driver disable pin voltage	DRVOFF	–0.3	40	V
Logic I/O voltage	EN/IN1, PH/EN2, nFAULT	–0.3	5.75	V
HW variant - Configuration pins voltage	MODE, ITRIP, SR, DIAG	–0.3	5.75	V
Analog feedback pin voltage	IPROPI	–0.3	5.75	V
Sleep pin voltage (Not applicable for SPI (P) variant)	nSLEEP	–0.3	40	V
SPI I/O voltage - SPI variant	SDI, SDO, nSCS, SCLK	–0.3	5.75	V
SPI (P) variant - Logic supply	VDD	-0.3	5.75	V
SPI (P) variant - Logic supply transient voltage ramp	VDD		5	V/µs
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limited by the over current and over temperature protection functions of the device

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	VM, OUT1, OUT2, GND	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5	35(1)	V
V_{VDD}	SPI (P) variant - Logic supply voltage	VDD	4.5	5.5	V
V_{LOGIC}	Logic pin voltage	EN/IN1, PH/EN2, nSLEEP, DRVOFF, nFAULT	0	5.5	V
f_{PWM}	PWM frequency	EN/IN1, PH/EN2	0	25	KHz
V_{CONFIG}	HW variant - Configuration pin voltage	MODE, ITRIP, SR, DIAG	0	5.5	V
V_{IPROPI}	Analog feedback voltage	IPROPI	0	5.5	V
V_{SPI_IOS}	SPI (S) variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	0	V_{nSLEEP} + 0.5	V
	SPI (P) variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	0	V_{VDD} + 0.5	V
T_A	Operating ambient temperature		–40	125	°C
T_J	Operating junction temperature		–40	150	°C

(1) The over current protection function does not support direct output (OUT1, OUT2) shorts less than 1 µH above 28 V.

7.4 Thermal Information

Refer Transient thermal impedance table for application related use case.

THERMAL METRIC(1)		HVSSOP package	VQFN-HR package	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	29.1	22.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	8.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.3	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

4.5 V (falling) ≤ V_{VM} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)
For SPI (P) variant only: 4.5 V ≤ V_{VDD} ≤ 5.5 V (unless otherwise noted)

7.5.1 Power Supply & Initialization

Refer wake up transient waveforms

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VM_REV}	Supply pin voltage during reverse current	I_{VM} = - 5 A, device in unpowered state		1.4		V
I_{VMQ}	VM current in SLEEP state	V_{VM} = 13.5 V, V_{nSLEEP} = 0 V or V_{VDD} < POR_{VDD_FALL}, T_A = 25°C		1		µA
		V_{VM} = 13.5 V, V_{nSLEEP} = 0 V or V_{VDD} < POR_{VDD_FALL}, T_A = 125°C			5.8	µA
I_{VMS}	VM current in STANDBY state	V_{VM} = 13.5 V		3	5	mA
I_{VDD}	VDD current in ACTIVE state	SPI (P) variant			10	mA
t_{RESET}	RESET pulse filter time	Reset signal on nSLEEP pin for HW (H) variant	5		20	µs
t_{SLEEP}	SLEEP command filter time	Sleep signal on nSLEEP pin for HW (H) variant	40		120	µs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SLEEP_SPI}	SLEEP command filter time	Sleep signal on nSLEEP pin for SPI (S) variant	5		20	µs
t_{WAKEUP}	Wake-up command filter time	Wake-up signal on nSLEEP pin for HW (H) and SPI (S) variants		10		µs
t_{COM}	Time for communication to be available after wake-up or power-up through VM or VDD supply pin	Wake-up signal on nSLEEP pin or power cycle - V_{VM} > VM_{POR_RISE} or V_{VDD} > VDD_{POR_RISE}			400	µs
t_{READY}	Time for driver ready to be driven after wake-up through nSLEEP pin or power-up through VM or VDD supply pin	Wake-up signal on nSLEEP pin or power cycle - V_{VM} > VM_{POR_RISE} or V_{VDD} > VDD_{POR_RISE}			1	ms

7.5.2 Logic I/Os

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_nSLEEP}	Input logic low voltage	nSLEEP pin			0.65	V
V_{IH_nSLEEP}	Input logic high voltage	nSLEEP pin	1.55			V
V_{IHYS_nSLEEP}	Input hysteresis	nSLEEP pin		200		mV
V_{IL}	Input logic low voltage	DRVOFF, EN/IN1, PH/IN2 pins			0.7	V
V_{IH}	Input logic high voltage	DRVOFF, EN/IN1, PH/IN2 pins	1.5			V
V_{IHYS}	Input hysteresis	DRVOFF, EN/IN1, PH/IN2 pins		100		mV
R_{PD_nSLEEP}	Internal pull-down resistance on nSLEEP to GND	Measured at min VIL level	100		400	KΩ
R_{PU}	Internal pull-up resistance to VDD (reverse current blocked) on DRVOFF	Measured at min VIH level	200		550	KΩ
R_{PD}	Internal pull-down resistance to GND on EN/IN1 and PH/IN2	Measured at max VIL level	200		500	KΩ
I_{nFAULT_PD}	Sink current to GND on nFAULT pin when asserted low	V_{nFAULT} = 0.3 V	5			mA

7.5.3 SPI I/Os

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PU_nSCS}	Internal pull-up resistance to VDD (reverse current blocked) on nSCS	Measured at min VIH level	200		500	KΩ
R_{PD_SPI}	Internal pull-down resistance to GND on SDI, SCLK	Measured at max VIL level	150		500	KΩ
V_{IL}	Input logic low voltage	SDI, SCLK, nSCS pins			0.7	V
V_{IH}	Input logic high voltage	SDI, SCLK, nSCS pins	1.5			V
V_{IHYS}	Input hysteresis	SDI, SCLK, nSCS pins		100		mV
V_{OL_SDO}	Output logic low voltage	0.5 mA sink into SDO			0.4	V
V_{OH_SDO}	Output logic high voltage for SPI (S) variant	0.5 mA source from SDO, V_{nSLEEP} = 5 V, V_{VM} > 7 V	4.1			V
		0.5 mA source from SDO, V_{nSLEEP} = 3.3 V, V_{VM} > 5 V	2.7			V
	Output logic high voltage for SPI (P) variant	0.5 mA source from SDO, V_{VDD} = 5 V	4.5			V
$V_{OH\_SDO\_NL}$	Output logic high voltage at no load on SDO, valid only for SPI (S) variant	No current from SDO, V_{nSLEEP} = 5 V, V_{VM} > 7 V			5.5	V
		No current from SDO, V_{nSLEEP} = 3.3 V, V_{VM} > 5 V			3.8	V

7.5.4 Configuration Pins - HW Variant Only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6 level setting for ITRIP, SR and DIAG						
$R_{LVL1OF6}$	Level 1 of 6	Connect to GND			10	Ω
$R_{LVL2OF6}$	Level 2 of 6	+/- 10% resistor to GND	7.4	8.2	9	KΩ
$R_{LVL3OF6}$	Level 3 of 6	+/- 10% resistor to GND	19.8	22	24.2	KΩ
$R_{LVL4OF6}$	Level 4 of 6	+/- 10% resistor to GND	42.3	47	51.7	KΩ
$R_{LVL5OF6}$	Level 5 of 6	+/- 10% resistor to GND	90	100	110	KΩ
$R_{LVL6OF6}$	Level 6 of 6	Hi-Z (no connect)	250			KΩ
3 level setting for MODE						
$R_{LVL1OF3}$	Level 1 of 3	Connect to GND			10	Ω
$R_{LVL2OF3}$	Level 2 of 3	+/- 10% resistor to GND	7.4	8.2	9	KΩ
$R_{LVL3OF3}$	Level 3 of 3	Hi-Z (no connect)	100			KΩ

7.5.5 Power FET Parameters

Measured at V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HS_ON}	High-side FET on resistance, HVSSOP package	I_{OUT} = 3 A, T_J = 25°C		49		mΩ
		I_{OUT} = 3 A, T_J = 150°C			93.1	mΩ
	High-side FET on resistance, VQFN-HR package	I_{OUT} = 3 A, T_J = 25°C		42		mΩ
		I_{OUT} = 3 A, T_J = 150°C			79.8	mΩ
R_{LS_ON}	Low-side FET on resistance, HVSSOP package	I_{OUT} = 3 A, T_J = 25°C		49		mΩ
		I_{OUT} = 3 A, T_J = 150°C			93.1	mΩ
	Low-side FET on resistance, VQFN-HR package	I_{OUT} = 3 A, T_J = 25°C		42		mΩ
		I_{OUT} = 3 A, T_J = 150°C			79.8	mΩ
V_{SD}	Low-side & High-side FET source-drain voltage when body diode is forward biased	I_{OUT} = +/- 3 A (both directions)	0.4	0.9	1.5	V
R_{Hi-Z}	OUT resistance to GND in SLEEP or STANDBY state, V_{OUTx} = V_{VM} = 13.5 V	SR = 3'b000 or 3'b001 or 3'b010 or 3'b111 or LVL2 or LVL5	2		5	KΩ
		SR = 3'b011 or LVL3	7		14	KΩ
		SR = 3'b100 or LVL4	5		10.5	KΩ
		SR = 3'b101 or LVL1	4		8.5	KΩ
		SR = 3'b110 or LVL6	2.5		6	KΩ

7.5.6 Switching Parameters with High-Side Recirculation

Load = 1.5mH / 4.7 Ohm, V_{VM} = 13.5 V, refer high-side recirculation waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR_{LSOFF}	Output voltage rise time, 10% - 90%	SR = 3'b000 or LVL2		1.6		V/µs
		SR = 3'b001 (SPI only)		5		V/µs
		SR = 3'b010 (SPI only)		8		V/µs
		SR = 3'b011 or LVL3		13.3		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24.5		V/µs
		SR = 3'b110 or LVL6		36		V/µs
		SR = 3'b111 or LVL5		47		V/µs
t_{PD_LSOFF}	Propagation time during output voltage rise	SR = 3'b000 or LVL2		1		µs
		SR = 3'b001 (SPI only)		0.9		µs
		SR = 3'b010 (SPI only)		0.8		µs
		SR = 3'b011 or LVL3		0.7		µs
		SR = 3'b100 & 3'b101 or LVL4 & LVL1		0.6		µs
		SR = 3'b110 & 3'b111 or LVL6 & LVL5		0.5		µs
t_{DEAD_LSOFF}	Dead time during output voltage rise	All SRs		0.9		µs
SR_{LSON}	Output voltage fall time, 90% - 10%	SR = 3'b000 or LVL2		1.6		V/µs
		SR = 3'b001 (SPI only)		5		V/µs
		SR = 3'b010 (SPI only)		8		V/µs
		SR = 3'b011 or LVL3		13.3		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24.5		V/µs
		SR = 3'b110 or LVL6		36		V/µs
		SR = 3'b111 or LVL5		47		V/µs
t_{PD_LSON}	Propagation time during output voltage fall	SR = 3'b000 or LVL2		0.2		µs
		SR = 3'b001 (SPI only)		0.2		µs
		SR = 3'b010 (SPI only)		0.2		µs
		SR = 3'b011 or LVL3		0.4		µs
		SR = 3'b100 or 3'b101 or LVL4 or LVL1		0.3		µs
		SR = 3'b110 & 3'b111 or LVL6 & LVL5		0.2		µs
t_{DEAD_LSON}	Dead time during output voltage fall	SR = 3'b000 or LVL2		1.5		µs
		SR = 3'b001 or 3'b010 (SPI only)		0.6		µs
		SR = 3'b011 or LVL3		0.7		µs
		All other SRs		0.6		µs
$Match_{SRLS}$	Output voltage rise and fall slew rate matching	All SRs	-20		+20	%

7.5.7 Switching Parameters with Low-Side Recirculation

Load = 1.5 mH / 4.7 Ohm, V_{VM} = 13.5 V, refer low-side recirculation waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR_{HSON}	Output voltage rise time, 10% - 90%	All SRs		8		V/µs
t_{PD_HSON}	Propagation time during output voltage rise	SR = 3'b000 or LVL2		3.1		µs
		SR = 3'b001 (SPI only)		2		µs
		SR = 3'b010 (SPI only)		1.7		µs
		SR = 3'b011 or LVL3		1.2		µs
		All other SRs		0.9		µs
t_{DEAD_HSON}	Dead time during output voltage rise	SR = 3'b000 or LVL2		1.5		µs
		SR = 3'b001 (SPI only)		1		µs
		SR = 3'b010 (SPI only)		0.8		µs
		All other SRs		0.45		µs
SR_{HSOFF}	Output voltage fall time, 90% - 10%	SR = 3'b000 or 3'b001 or 3'b010 or LVL2		43		V/µs
		SR = 3'b011 or LVL3		14		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24		V/µs
		SR = 3'b110 or LVL6		34		V/µs
		SR = 3'b111 or LVL5		43		V/µs
t_{PD_HSOFF}	Propagation time during output voltage fall	All SRs		0.25		µs
t_{DEAD_HSOFF}	Dead time during output voltage fall	All SRs		0.2		µs
t_{BLANK}	Current regulation blanking time after OUT slewing for current sense output to settle (Valid for only for LS recirculation)	All SRs		3.4		µs

7.5.8 IPROPI & ITRIP Regulation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{IPROPI}	Current scaling factor, HVSSOP package			3020		A/A
	Current scaling factor, VQFN-HR package			3070		A/A
A_{I_ERR}	Current scaling factor error	I_{OUT} > 0.8 A to 4.3 A	-5		+5	%
		I_{OUT} = 0.2 A to 0.8 A	-20		+20	%
		I_{OUT} = 0.1 A to 0.2 A	-50		+50	%
$A_{I\_ERR\_M}$	Current matching between the two half-bridges	I_{OUT} > 0.8 A	-2		+2	%
$Offset_{IPROPI}$	Offset current on IPROPI at no load current	I_{OUT} = 0 A			15	µA
BW_{IPROPI}	Bandwidth of the IPROPI internal sense circuit	No external capacitor on IPROPI.	400			KHz
V_{IPROPI_LIM}	Internal clamping voltage on IPROPI		4.5		5.5	V
V_{ITRIP_LVL}	Voltage limit on V_{IPROPI} to trigger TOFF cycle for ITRIP regulation	ITRIP = 3'b001 or LVL2	1.06	1.18	1.3	V
		ITRIP = 3'b010 (SPI only)	1.27	1.41	1.55	V
		ITRIP = 3'b011 (SPI only)	1.49	1.65	1.82	V
		ITRIP = 3'b100 or LVL3	1.78	1.98	2.18	V
		ITRIP = 3'b101 or LVL4	2.08	2.31	2.54	V
		ITRIP = 3'b110 or LVL5	2.38	2.64	2.9	V
		ITRIP = 3'b111 or LVL6	2.67	2.97	3.27	V
t_{OFF}	ITRIP regulation - off time	TOFF = 2'b00 (SPI only)	16	20	25	µs
		TOFF = 2'b01 (SPI). Only choice for HW	24	30	36	µs
		TOFF = 2'b10 (SPI only)	33	40	48	µs
		TOFF = 2'b11 (SPI only)	41	50	61	µs

7.5.9 Over Current Protection (OCP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP_HS}	Over current protection threshold on the high side	OCP_SEL = 2'b00 (SPI), Only choice for HW	12		24	A
		OCP_SEL = 2'b10 (SPI only)	9		18	A
		OCP_SEL = 2'b01 (SPI only)	6		14	A
I_{OCP_LS}	Over current protection threshold on the low side	OCP_SEL = 2'b00 (SPI), Only choice for HW	12		24	A
		OCP_SEL = 2'b10 (SPI only)	9		18	A
		OCP_SEL = 2'b01 (SPI only)	6		14	A
t_{OCP}	Over current protection deglitch time	TOCP_SEL = 2'b00 (SPI), Only choice for HW	4.5	6	7.3	µs
	Over current protection deglitch time	TOCP_SEL = 2'b01 (SPI only)	2.2	3	4.1	µs
	Over current protection deglitch time	TOCP_SEL = 2'b10 (SPI only)	1.1	1.5	2.3	µs
	Over current protection deglitch time	TOCP_SEL = 2'b11 (SPI only)	0.15	0.2	0.4	µs

7.5.10 Over Temperature Protection (TSD)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature		155	170	185	°C
T_{HYS}	Thermal shutdown hysteresis			30		°C
t_{TSD}	Thermal shutdown deglitch time		10	12	19	µs

7.5.11 Voltage Monitoring

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VMOV}	VM over voltage threshold while rising	VMOV_SEL = 2'b00 (SPI), Only choice in HW variant	33.6		37	V
		VMOV_SEL = 2'b01 (SPI only)	28		31	V
		VMOV_SEL = 2'b10 (SPI only)	18		21	V
V_{VMOV_HYS}	VM over voltage hysteresis			0.6		V
t_{VMOV}	VM over voltage deglitch time		10	12	19	µs
V_{VMUV}	VM under voltage threshold while falling		4.2		4.5	V
V_{VMUV_HYS}	VM under voltage hysteresis			200		mV
t_{VMUV}	VM under voltage deglitch time		10	12	19	µs
VM_{POR_FALL}	VM voltage at which device goes into POR	Applicable for HW & SPI (S) variant			3.6	V
VM_{POR_RISE}	VM voltage at which device comes out of POR	Applicable for HW & SPI (S) variant			3.9	V
VDD_{POR_FALL}	VDD voltage at which device goes into POR	Applicable for SPI (P) variant			3.5	V
VDD_{POR_RISE}	VDD voltage at which device comes out of POR	Applicable for SPI (P) variant			3.8	V

7.5.12 Load Monitoring

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off-state diagnostics (OLP)						
R_{S_GND}	Resistance on OUT to GND that will be detected as short, All modes				1	KΩ
R_{S_VM}	Resistance on OUT to VM that will be detected as short , All modes				1	KΩ
R_{OPEN_FB}	Resistance between OUTx that will be detected as open, PH/EN or PWM mode		1.5			KΩ
R_{OPEN_LS}	Resistance on OUT to GND that will be detected as open , Independent mode	Valid for low-side load	2			KΩ
R_{OPEN_HS}	Resistance on OUT to VM that will be detected as open, Independent mode	Valid for high-side load, V_{VM} = 13.5 V	10			KΩ
V_{OLP_REFH}	OLP Comparator Reference High			2.65		V
V_{OLP_REFL}	OLP Comparator Reference Low			2		V
R_{OLP_PU}	Internal pull-up resistance on OUT to VDD during OLP	$V_{OUTx} = V_{OLP\_REFH} + 0.1V$		1		KΩ
R_{OLP_PD}	Internal pull-down resistance on OUT to GND during OLP	$V_{OUTx} = V_{OLP\_REFL} - 0.1V$		1		KΩ
SPI variant only - On-state diagnostics (OLA)						
I_{PD_OLA}	Internal sink current on OUT to GND during dead-time in high-side recirculation	SR = 3'b000 or 3'b001 or 3'b010 or 3'b111 or LVL2 or LVL5	2.5		5	mA
		SR = 3'b011 or LVL3	0.8		2	mA
		SR = 3'b100 or LVL4	1.2		2.5	mA
		SR = 3'b101 or LVL1	1.5		3	mA
		SR = 3'b110 or LVL6	2.2		4	mA
V_{OLA_REF}	Comparator Reference with respect to VM used for OLA			0.25		V

7.5.13 Fault Retry Setting

Refer to retry setting waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RETRY}	Automatic driver retry time	Fault reaction set to RETRY	4.1	5	6.1	ms
t_{CLEAR}	Fault free operation time to auto-clear from over current event	Fault reaction set to RETRY	85		200	µs
t_{CLEAR_TSD}	Fault free operation time to auto-clear from over temperature event	Fault reaction set to RETRY	4.2		6.7	ms

7.5.14 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

Table 7-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability - full-bridge

PART NUMBER	PACKAGE	$R_{\theta JA}$ [°C/W](1)				Current [A](2)					
		without PWM(3)								with PWM(4)	
		0.1 sec	1 sec	10 sec	DC	0.1 sec	1 sec	10 sec	DC	10 sec	DC
DRV8243-Q1	VQFN-HR	7.3	13	17.5	34.2	7.5	5.6	4.8	3.5	4.4	3.0
DRV8243-Q1	HVSSOP	5.8	10.5	15.3	32.4	7.8	5.8	4.8	3.3	4.4	2.9

(1) Based on thermal simulations using 40 mm x 40 mm x 1.6 mm 4 layer PCB – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 minimum mm via pitch.
(2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C
(3) Only conduction losses (I^2R) considered
(4) Switching loss roughly estimated by the following equation:

$$P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times V_{VM}/SR, \text{ where } V_{VM} = 13.5\ V,\ f_{PWM} = 20\ KHz,\ SR = 23\ V/\mu s \quad (1)$$

7.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period(1)	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{HI_nSCS}	SDO minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{EN_SDO}	SDO enable delay time(1)			35	ns
t_{DIS_SDO}	SDO disable delay time(1)			100	ns

(1) SPI (S) variant: SDO delay times are valid only with SDO external load of 5 pF. With a 20 pF load on SDO, there is an additional delay on SDO, which results in a 25% increase in SCLK minimum time, limiting the SCLK to a maximum of 8 MHz. There is NO such limitation for the SPI (P) variant.

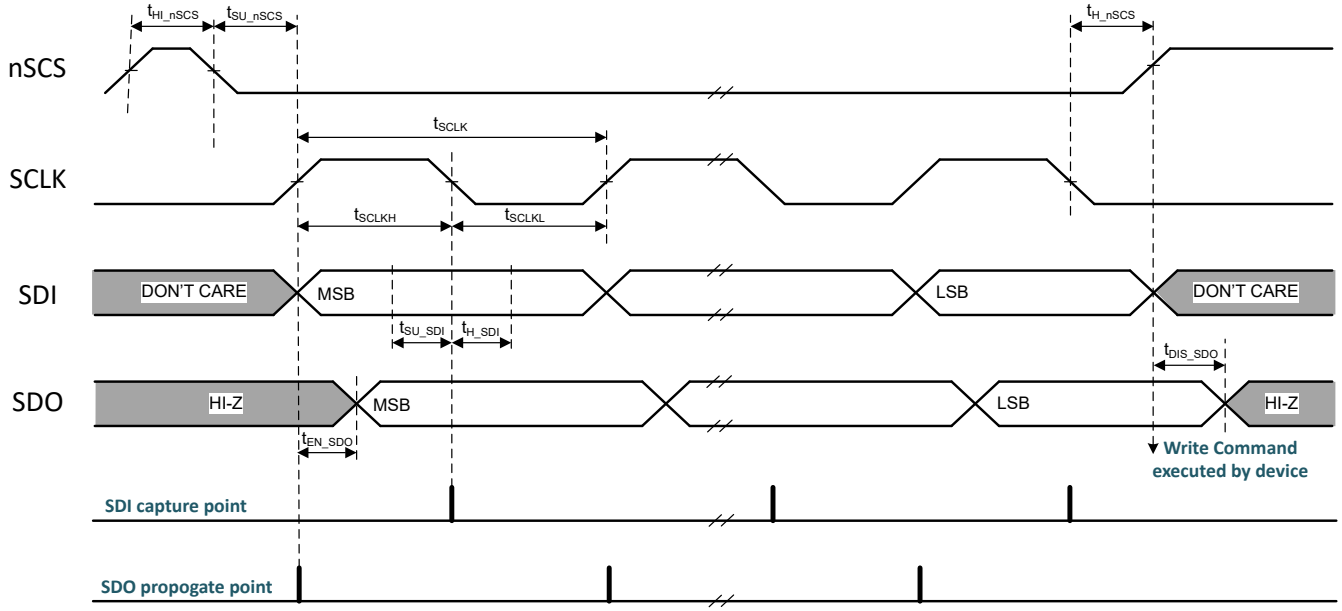


Figure 7-1. SPI Peripheral-Mode Timing Definition

7.7 Switching Waveforms

This section illustrates the switching transients for an inductive load due to external PWM or internal ITRIP regulation.

7.7.1.1 High-Side Recirculation

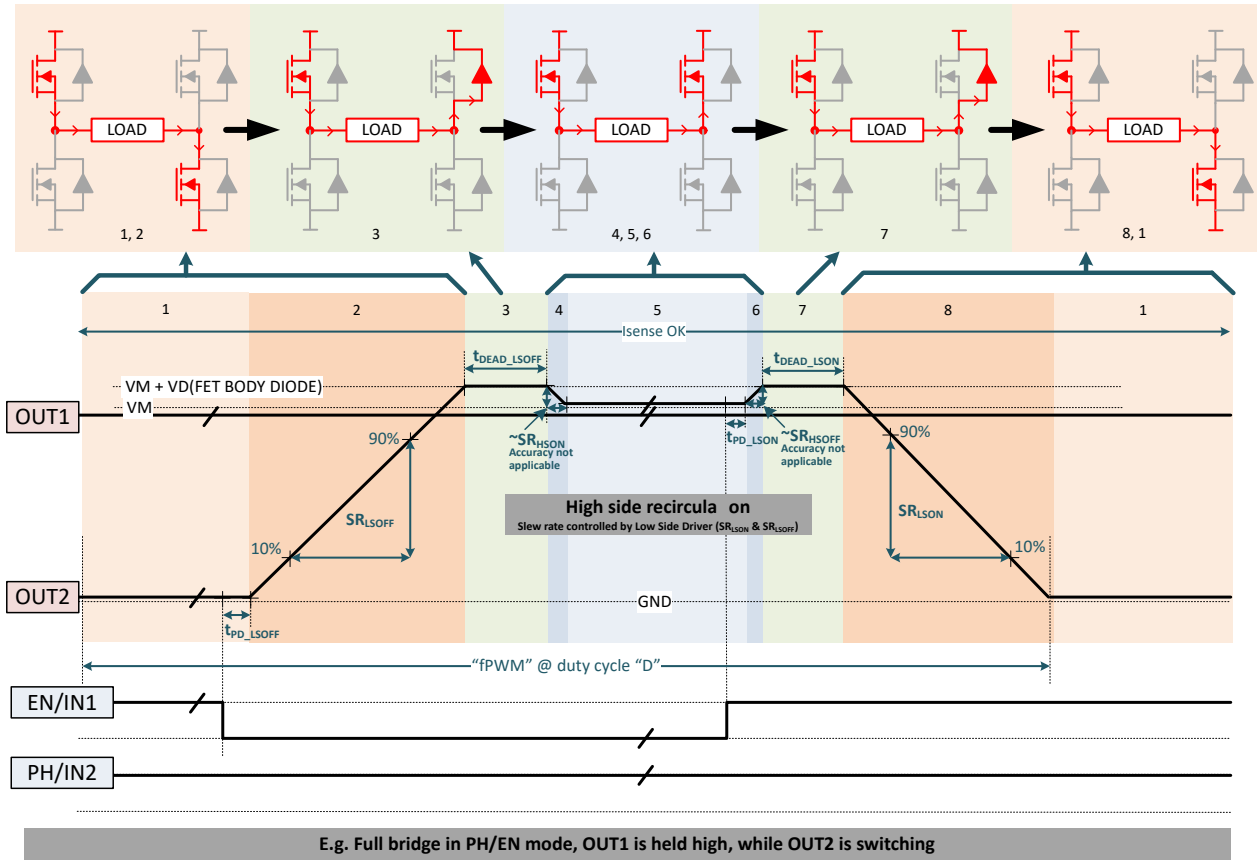


Figure 7-2. Output Switching Transients for a H-Bridge with High-Side Recirculation

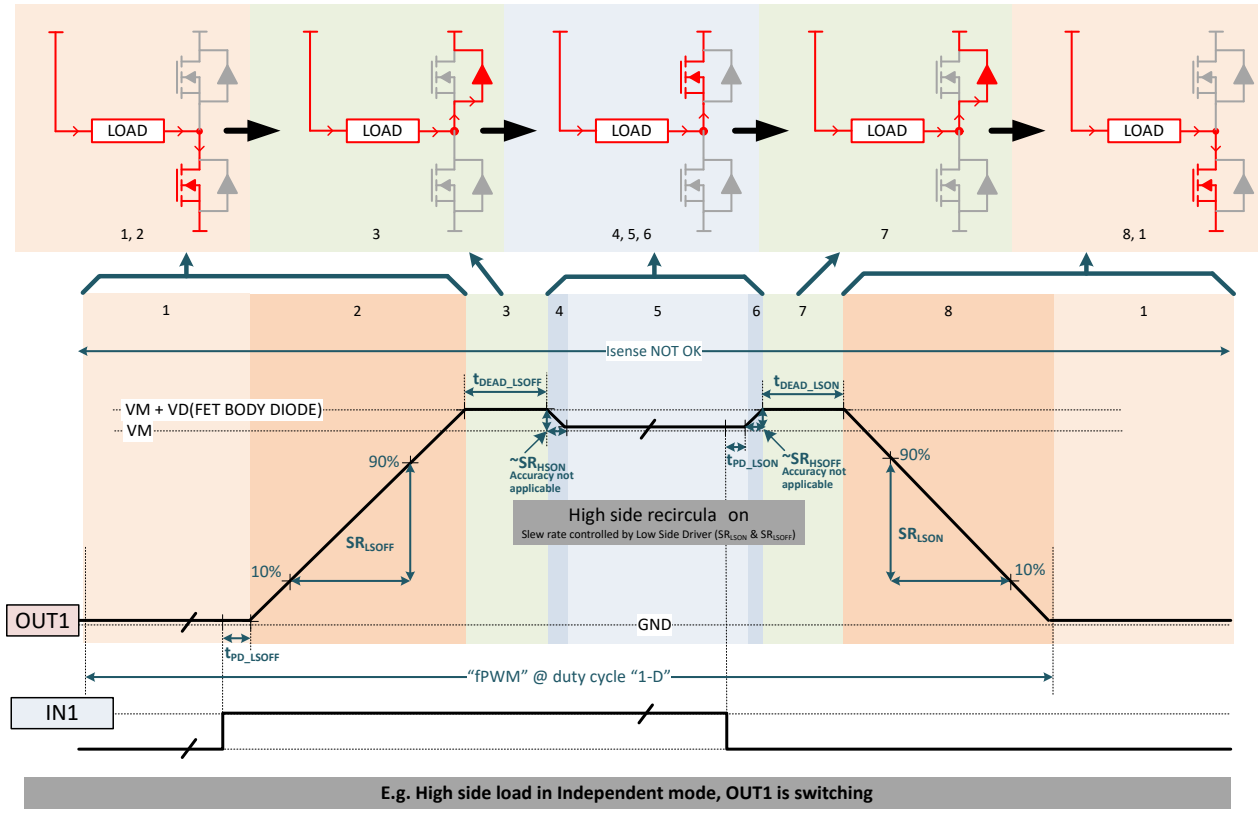


Figure 7-3. Output Switching Transients for a Half-Bridge with High-Side Recirculation

7.7.1.2 Low-Side Recirculation

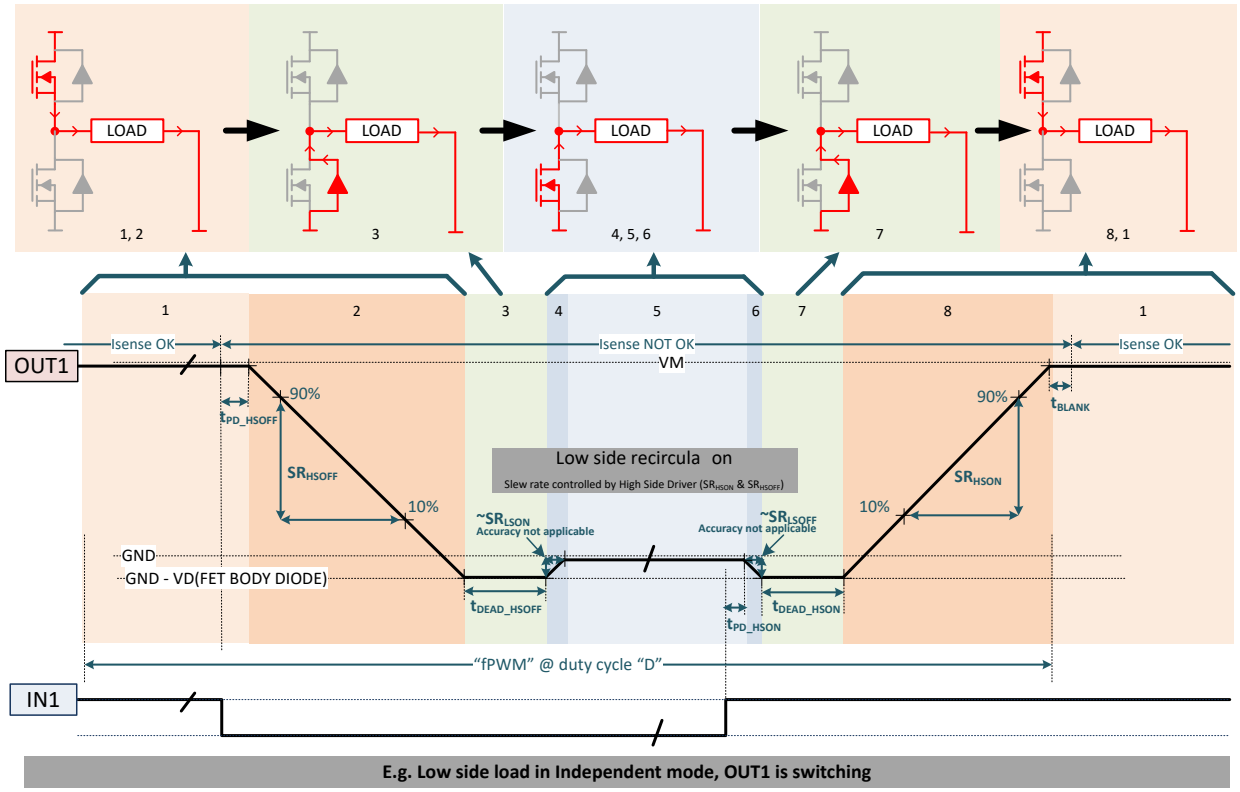


Figure 7-4. Output Switching Transients for a half-bridge with Low-Side Recirculation

7.7.2 Wake-up Transients

7.7.2.1 HW Variant

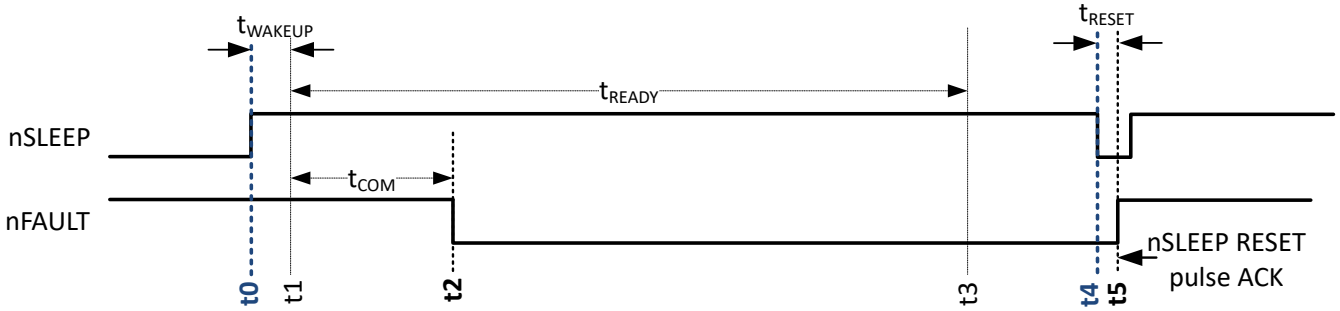


Figure 7-5. Wake-up from SLEEP State to STANDBY State Transition for HW Variant

Hand shake between controller and device during wake-up as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t2): **Controller – Issue nSLEEP reset pulse** to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgement of nSLEEP reset pulse. Device in STANDBY state

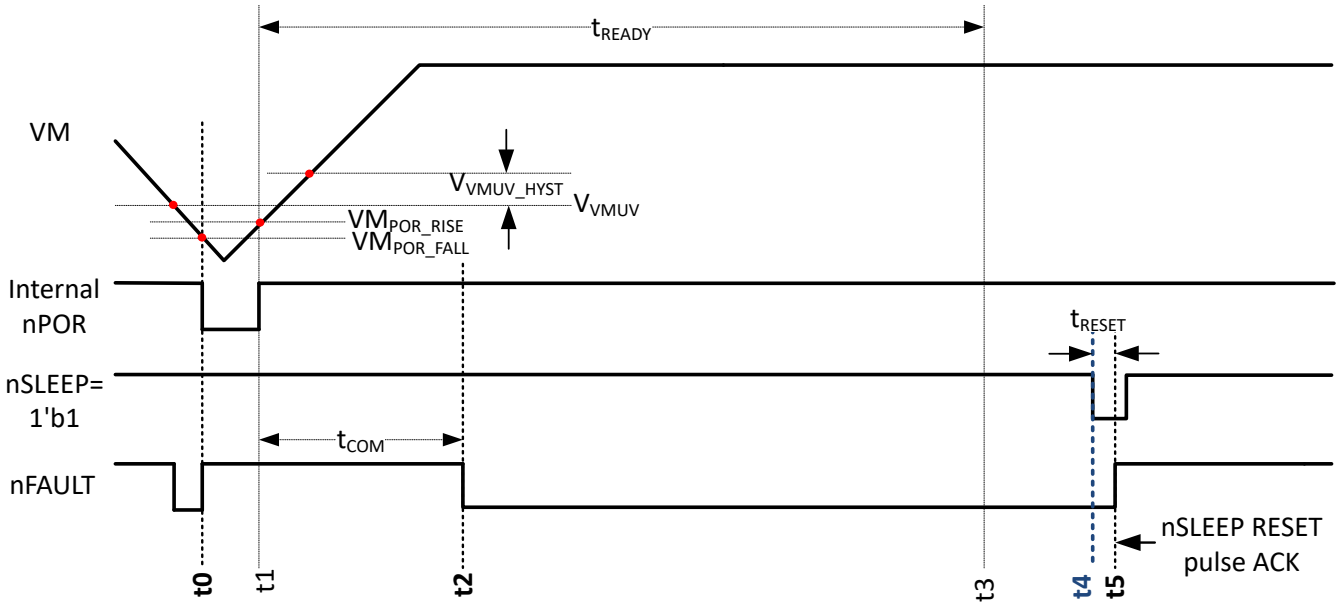


Figure 7-6. Power-up to STANDBY State Transition for HW Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t1: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t2): **Controller – Issue nSLEEP reset pulse** to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgement of nSLEEP reset pulse. Device in STANDBY state

7.7.2.2 SPI Variant

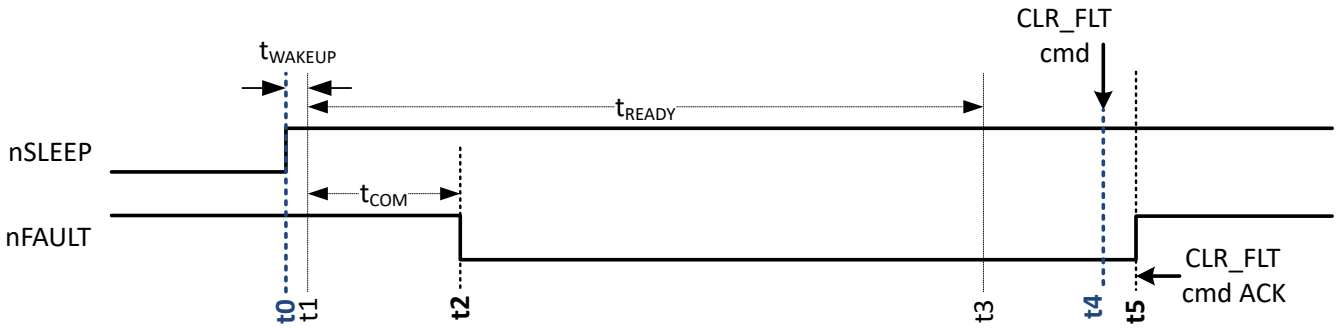


Figure 7-7. Wake-up from SLEEP State to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during a wake-up transient as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgement of nSLEEP reset pulse. Device in STANDBY state

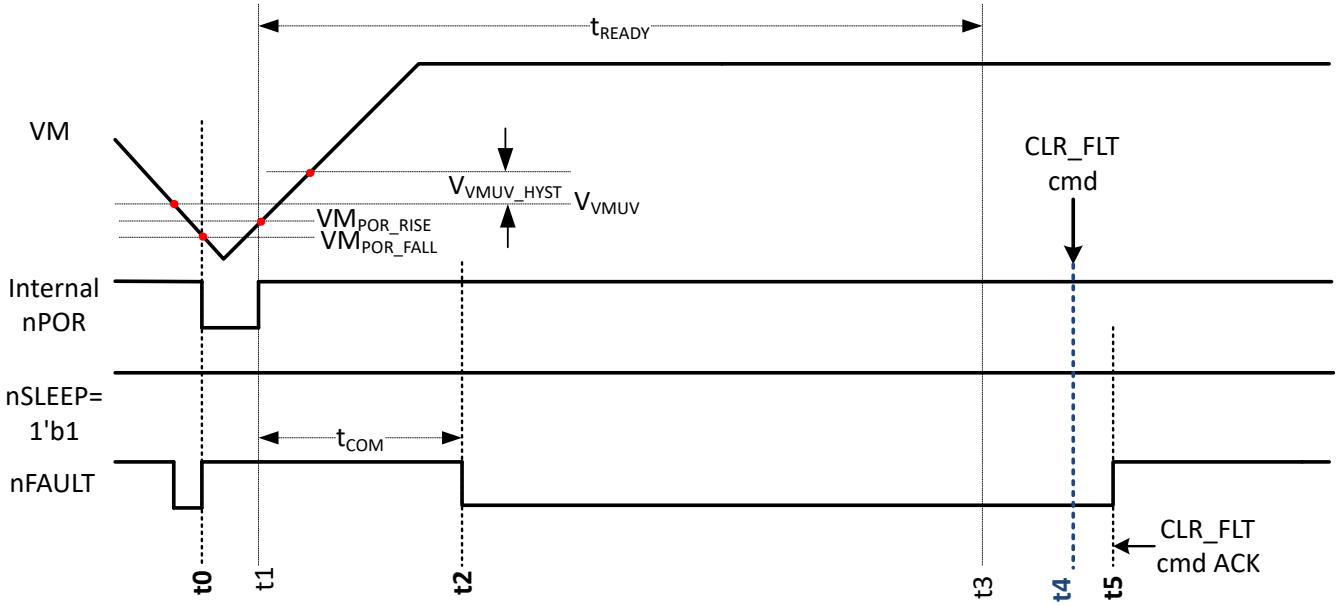


Figure 7-8. Power-up to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t1: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgement of nSLEEP reset pulse. Device in STANDBY state

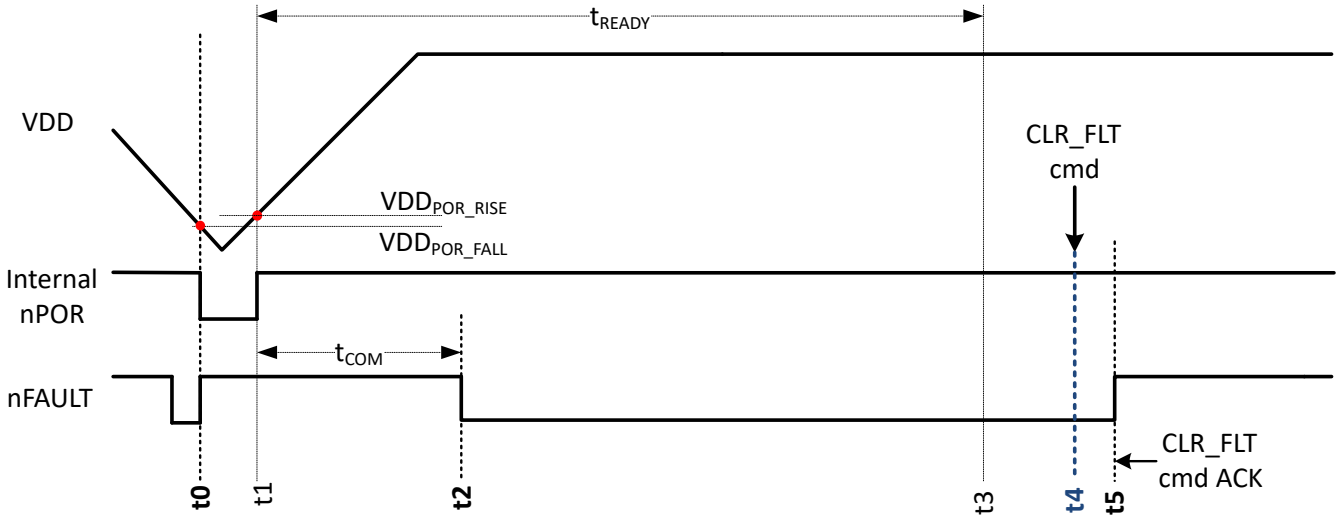


Figure 7-9. Power-up to STANDBY State Transition for SPI (P) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgement of nSLEEP reset pulse. Device in STANDBY state

7.7.3 Fault Reaction Transients

7.7.3.1 Retry setting

Valid for both SPI and HW variants

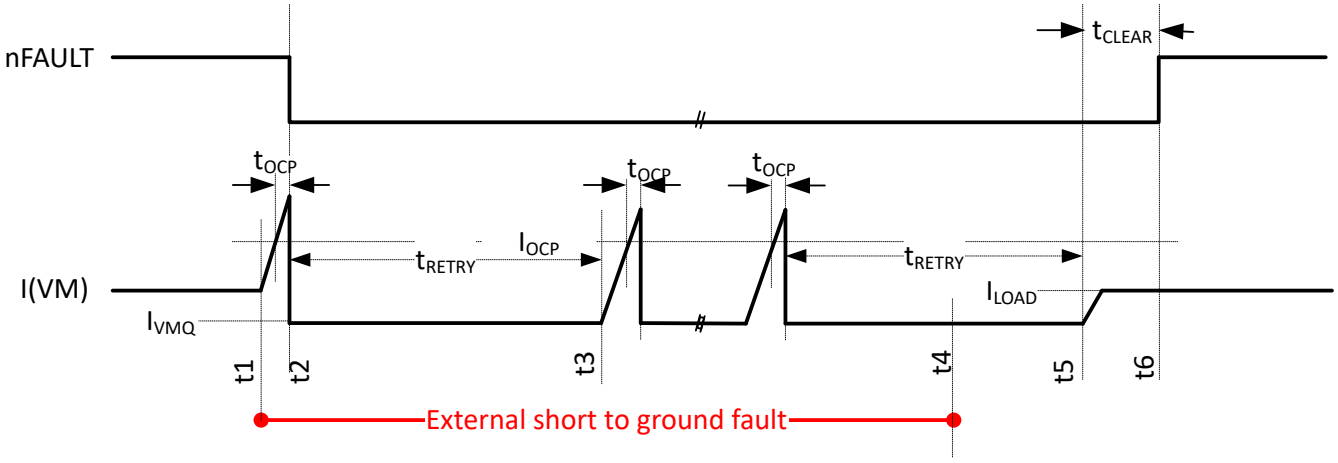


Figure 7-10. Fault reaction with RETRY setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with RETRY setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP}, output disabled, nFAULT asserted low to indicate fault.
- t3: Device automatically attempts retry (auto retry) after t_{RETRY}. Each time output is briefly turned on to confirm short occurrence and then immediately disabled after t_{OCP}. nFAULT remains asserted low through out. Cycle repeats till driver is disabled by the user or external short is removed, as illustrated further. Note that, in case of a TSD (Thermal Shut Down) event, automatic retry time depends on the cool off based on thermal hysteresis.
- t4: The external short is removed.
- t5: Device attempts auto retry. But this time, no fault occurs and device continues to keep the output enabled.
- t6: After a fault free operation for a period of t_{CLEAR} is confirmed, nFAULT is de-asserted.
- SPI variant only – Fault status remains latched till a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

7.7.3.2 Latch setting

Valid for both SPI and HW variants

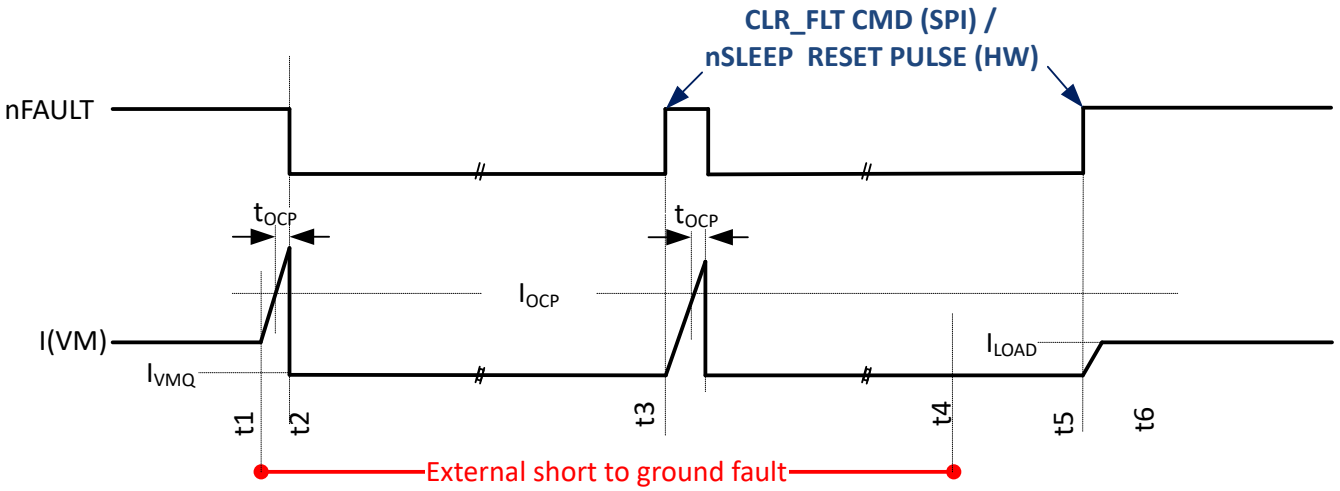


Figure 7-11. Fault reaction with Latch setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with LATCH setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP}, output disabled, nFAULT asserted low to indicate fault.
- t3: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. OCP fault is detected again and output is disabled with nFAULT asserted low.
- t4: The external short is removed.
- t5: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. Normal operation resumes.
- SPI variant only – Fault status remains latched till a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

7.8 Typical Characteristics

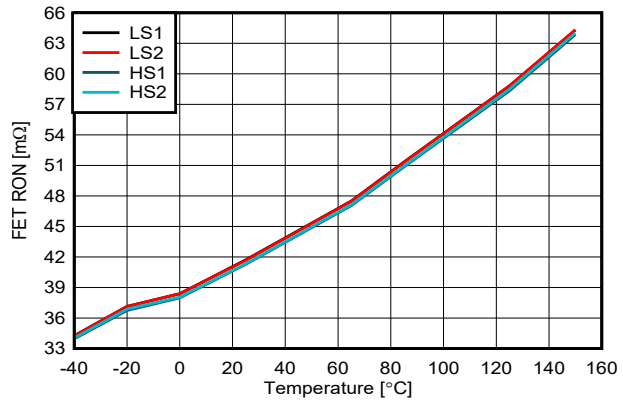


Figure 7-12. R_{HS_ON} & R_{LS_ON} for VQFN-HR(16) vs Temperature at V_{VM} = 13.5 V

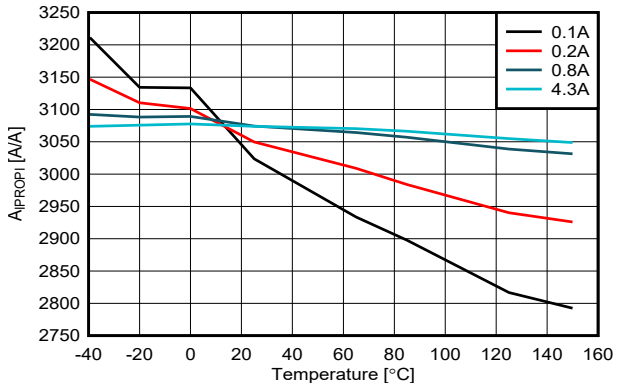


Figure 7-13. A_{IPROPI} Gain vs Temperature at V_{VM} = 13.5 V

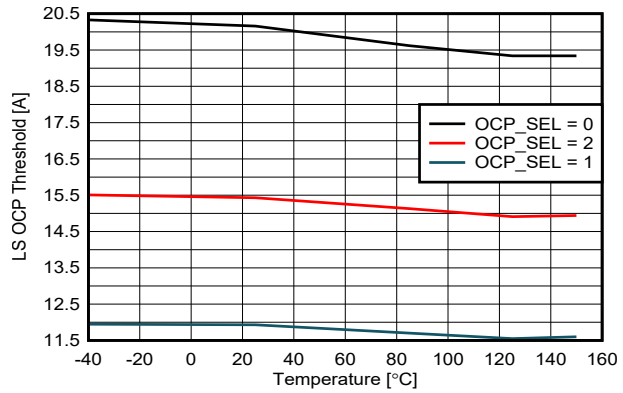


Figure 7-14. LS OCP Threshold vs Temperature at V_{VM} = 13.5 V

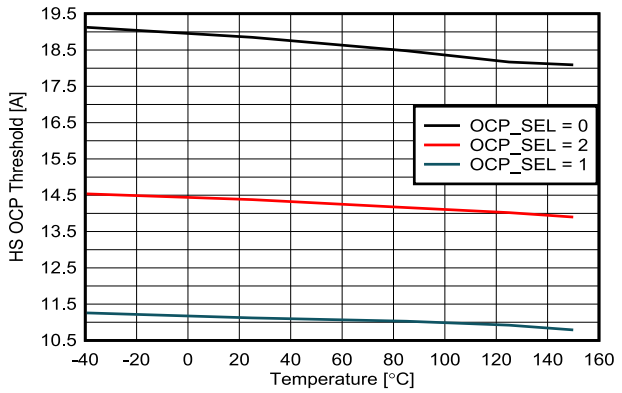


Figure 7-15. HS OCP Threshold vs Temperature at V_{VM} = 13.5 V

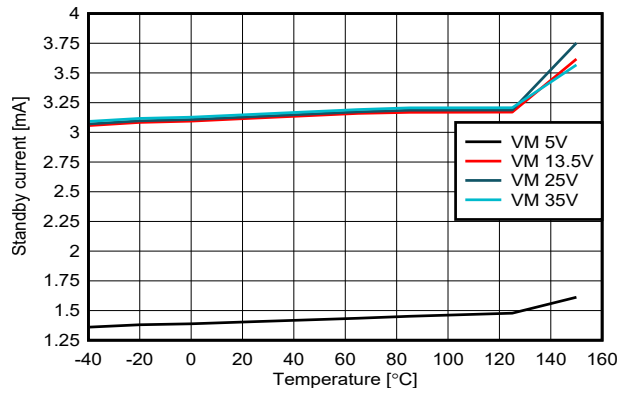


Figure 7-16. Current on VM in STANDBY state vs Temperature

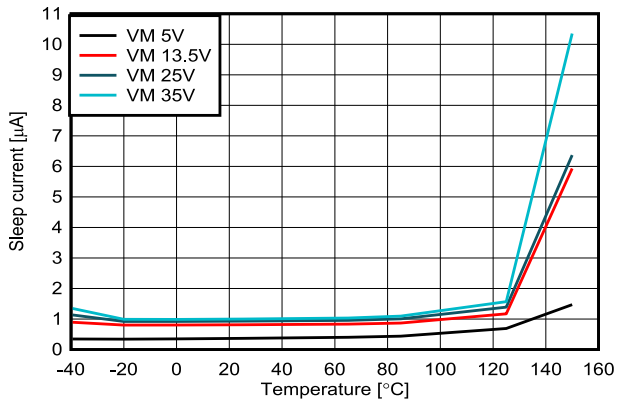


Figure 7-17. Current on VM in SLEEP state vs Temperature

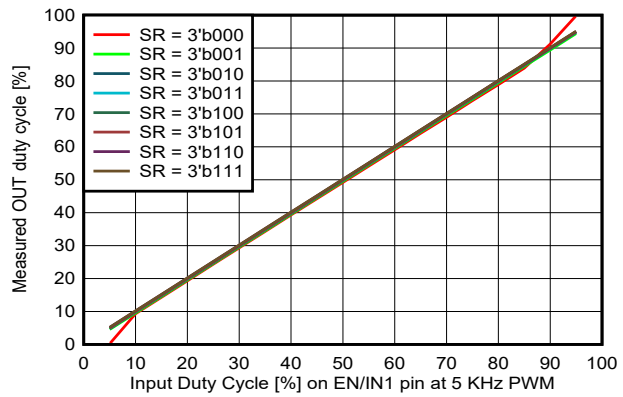


Figure 7-18. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 5 KHz at V_{VM} = 13.5 V for HS recirculation

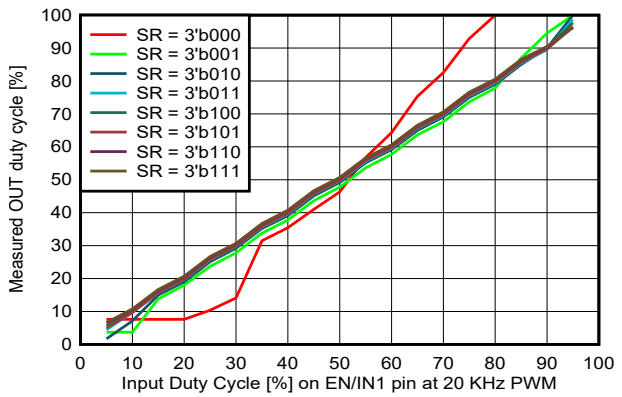


Figure 7-19. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 20 KHz at V_{VM} = 13.5 V for HS recirculation

8 Detailed Description

8.1 Overview

The DRV824x-Q1 family of devices are brushed DC motor drivers that operate from 4.5 to 35-V supporting a wide range of output load currents for various types of motors and loads. The devices integrate an H-bridge output power stage that can be operated in different control modes set by the MODE function. This allows for driving a single bidirectional brushed DC motor or two unidirectional brushed DC motors. The devices integrate a charge pump regulator to support efficient high-side N-channel MOSFETs with 100% duty cycle operation. The devices operate from a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The devices also provide a low power mode to minimize current draw during system inactivity.

The devices are available in two interface variants -

1. HW variant - Hardwired interface variant is available for easy device configuration. Due to the limited number of available pins in the device, this variant offers fewer configuration and fault reporting capability compared to the SPI variant.
2. SPI variant - A standard 4-wire serial peripheral interface (SPI) with daisy chain capability allows flexible device configuration and detailed fault reporting to an external controller. The feature differences of the SPI and HW variants can be found in the device comparison section. The SPI interface is available in two device variant choices, as stated below:
   a. SPI (S) variant - The power supply for the digital block is provided by an internal LDO regulator sourced from VM supply. The nSLEEP pin is a high impedance input pin.
   b. SPI (P) variant - This allows for an external supply input to the digital block of the device through a VDD pin. The nSLEEP pin is replaced by this VDD supply pin. This prevents device reset (brown out) during a VM under voltage condition.

The DRV824x family of devices provide a load current sense output using current mirrors on the high-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the high-side MOSFETs (current sourced out of the OUTx pin). This current can be converted to a proportional voltage using an external resistor (R_{IPROPI}). Additionally, the devices also support a fixed off-time PWM chopping scheme for limiting current to the load. The current regulation level can be configured through the ITRIP function.

A variety of protection features and diagnostic functions are integrated into the device. These include supply voltage monitors (VMOV & VMUV), , off-state (Passive) diagnostics (OLP), on-state (Active) diagnostics (OLA) - SPI variant only, overcurrent protection (OCP) for each power FET and over-temperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. The SPI variant has additional communication protection features such as frame errors and lock features for configuration register bits and driver control bits.

8.2 Functional Block Diagram

8.2.1 HW Variant

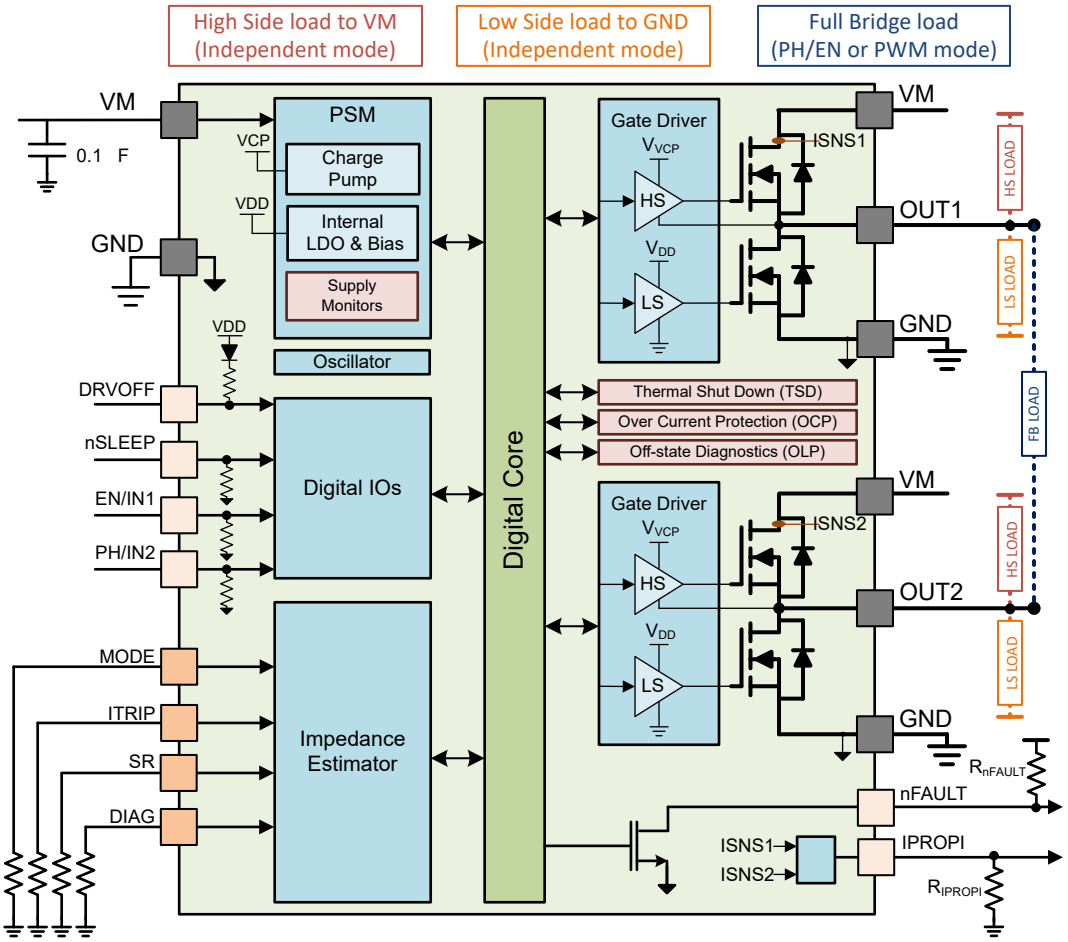


Figure 8-1. Functional Block Diagram - HW Variant

8.2.2 SPI Variant

There are two variants for the SPI interface - SPI (S) variant and SPI (P) variant as shown below.

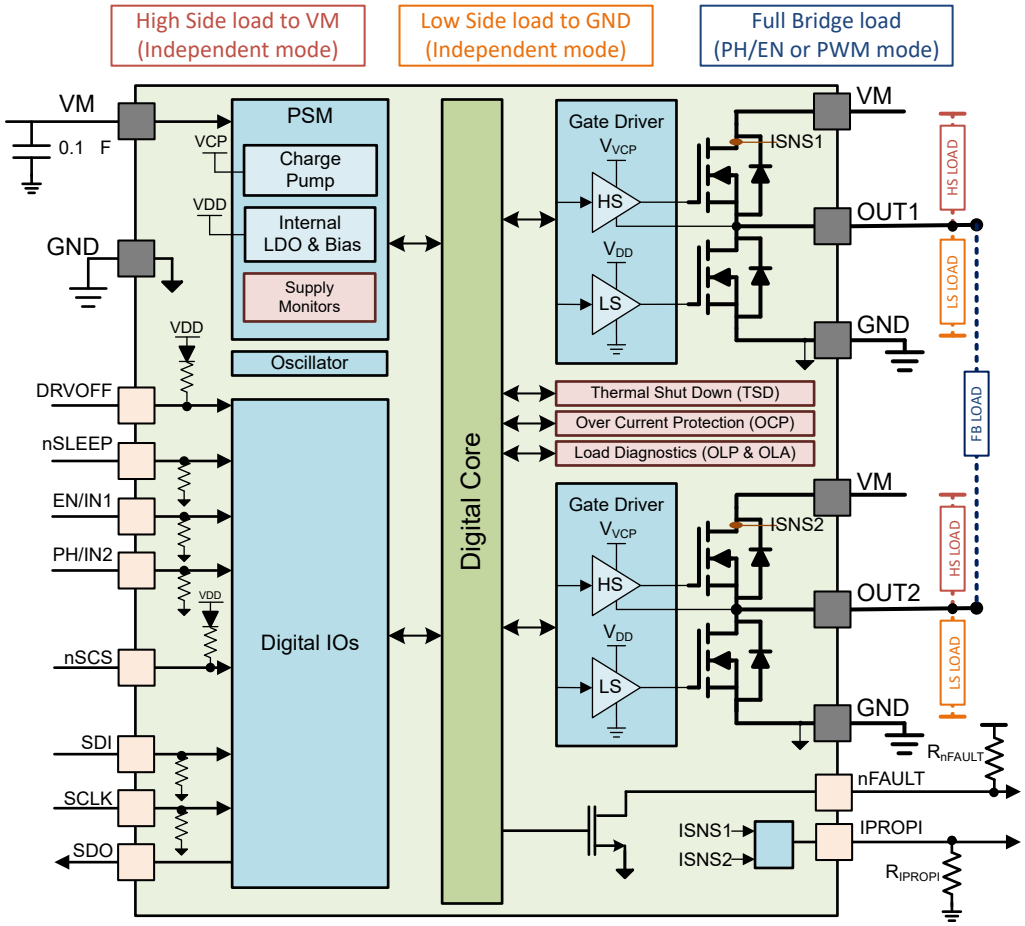


Figure 8-2. Functional Block Diagram - SPI (S) Variant

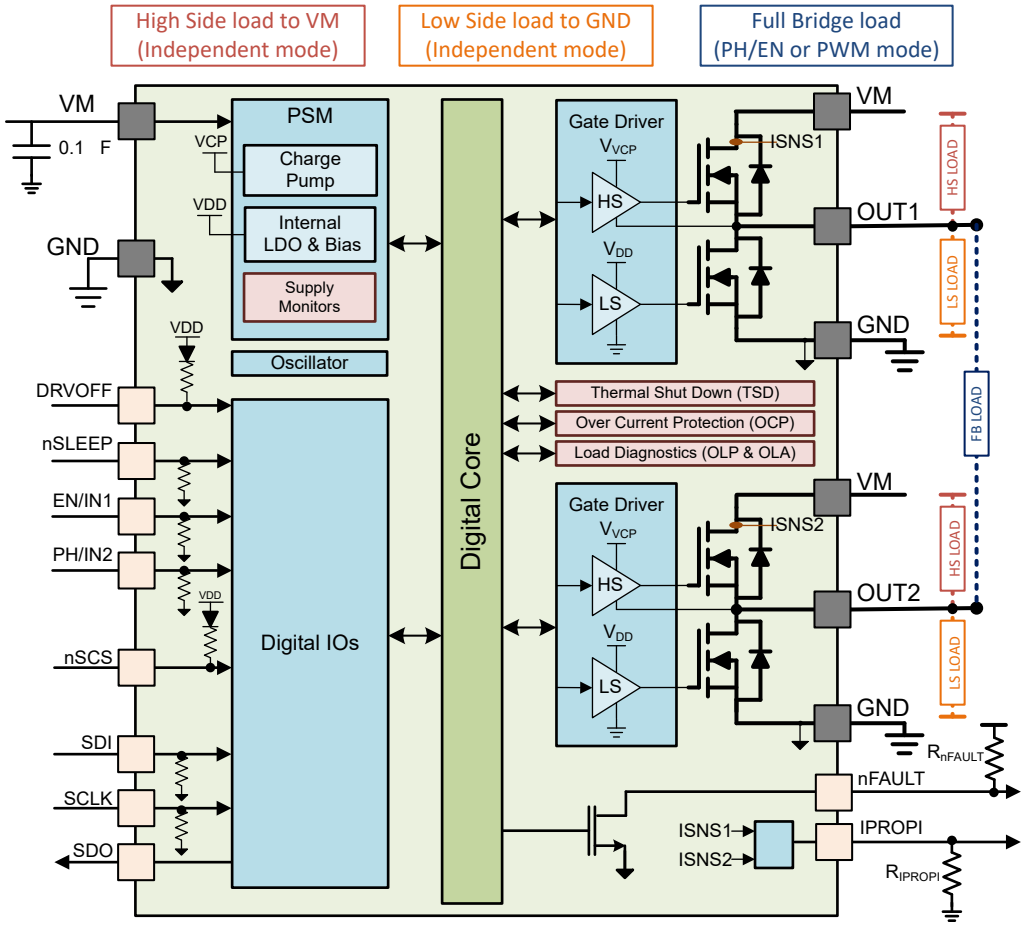


Figure 8-3. Functional Block Diagram - SPI (P) Variant

8.3 Feature Description

8.3.1 External Components

Section 8.3.1.1 and Section 8.3.1.2 contain the recommended external components for the device.

8.3.1.1 HW Variant

Table 8-1. External Components Table for HW Variant

Component	PIN	Recommendation
C_{VM1}	VM	0.1 µF, low ESR ceramic capacitor to GND rated for VM
C_{VM2}	VM	Local bulk capacitor to GND, 10 µF or higher, rated for VM to handle load transients. Refer the section on bulk capacitor sizing.
R_{IPROPI}	IPROPI	Typically 500 - 5000 Ω 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C_{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section.
R_{nFAULT}	nFAULT	Typically 1KΩ - 10 KΩ, 0.063 W pull-up resistor to controller supply.
R_{MODE}	MODE	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer MODE table.
R_{SR}	SR	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer SR section.
R_{ITRIP}	ITRIP	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer ITRIP table.
R_{DIAG}	DIAG	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer DIAG section.

8.3.1.2 SPI Variant

Table 8-2. External Components Table for SPI Variant

Component	PIN	Recommendation
C_{VM1}	VM	0.1 µF, low ESR ceramic capacitor to GND rated for VM
C_{VM2}	VM	Local bulk capacitor to GND, 10 µF or higher, rated for VM to handle load transients. Refer the section on bulk capacitor sizing.
R_{IPROPI}	IPROPI	Typically 500 - 5000 Ω 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C_{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section.
R_{nFAULT}	nFAULT	Typically 1KΩ - 10 KΩ, 0.063 W pull-up resistor to controller supply. If nFAULT signaling is not used, this pin can be short to GND or left open.
C_{VDD}	VDD	0.1 µF, 6.3 V, low ESR ceramic capacitor to GND. This is applicable for the SPI (P) variant only.

8.3.2 Bridge Control

The DRV824x-Q1 family of devices provides three separate modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the MODE setting. MODE is a 3-level setting based on the MODE pin for the HW variant or S_MODE bits in the CONFIG3 register for the SPI variant as summarized in Table 8-3:

Table 8-3. Mode table

MODE pin	S_MODE bits	Device Mode	Description
$R_{LVL1OF3}$	2'b00	PH/EN mode	full-bridge mode where EN/IN1 is the PWM input, PH/EN2 is the direction input
$R_{LVL2OF3}$	2'b01	Independent mode	Independent control for 2 half-bridges
$R_{LVL3OF3}$	2'b10, 2b'11	PWM mode	full-bridge mode where EN/IN1 and PH/EN2 control the PWM respectively depending on the direction

In the HW variant, MODE pin is latched during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant of the device, the mode setting can be changed anytime the SPI communication is available by writing to the S_MODE bits. This change is immediately reflected.

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied. By default, the nSLEEP and DRVOFF pins have an internal pull-down and pull-up resistor respectively, to ensure the outputs are Hi-Z if no inputs are present. Both the EN/IN1 and PH/IN2 pins also have internal pull down resistors. The sections below show the truth table for each control mode.

The device automatically generates the optimal dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage feedback. No external timing is required. This scheme ensures minimum dead time, while guaranteeing no shoot-through current.

Note

1. The SPI variant also provides additional control through the SPI_IN register bits. Refer to - Register - Pin control.
2. For the SPI (P) variant, ignore the nSLEEP column in the control table as there is no nSLEEP pin. Internally, nSLEEP = 1, always. The control table is valid when VDD > VDD_{POR} level.

8.3.2.1 PH/EN mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 is the PWM input and PH/IN2 is the direction input. For load illustration, refer the Load Summary section.

Table 8-4. Control table - PH/EN mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1				
1	1	1	1				
1	0	0	X	H	H	ISNS1 or ISNS2(1)	ACTIVE
1	0	1	0	L(2)	H	ISNS2	ACTIVE
1	0	1	1	H	L(2)	ISNS1	ACTIVE

(1) Current sourcing out of the device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

8.3.2.2 PWM mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 provides the PWM input in one direction, while PH/IN2 provides the PWM in the other direction. For load illustration, refer the Load Summary section.

Table 8-5. Control table - PWM mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1			No current	STANDBY
1	1	1	1			No current	STANDBY
1	0	0	0	H	H	ISNS1 or ISNS2(1)	ACTIVE
1	0	0	1	L(2)	H	ISNS2	ACTIVE
1	0	1	0	H	L(2)	ISNS1	ACTIVE

Table 8-5. Control table - PWM mode (continued)

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
1	0	1	1	Hi-Z	Hi-Z	No current	STANDBY

(1) Current sourcing out of device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

For the SPI variant, by setting the PWM_EXTEND bit in the CONFIG2 register, there are additional Hi-Z states that are possible, when a forward ([EN/IN1 PH/IN2] = [1 0]) or reverse ([EN/IN1 PH/IN2] = [0 1]) command is followed by a Hi-Z command ([EN/IN1 PH/IN2] = [1 1]). In this condition of Hi-Z (coasting), only the half-bridge involved with the PWM is Hi-Z, while the HS FET on the other half-bridge is kept ON. The determination on which half-bridge to Hi-Z is made based on the previous cycle. This is summarized in Table 8-6.

Table 8-6. PWM EXTEND table (PWM_EXTEND bit = 1'b1)

PREVIOUS STATE		CURRENT STATE			Device State Transition
OUT1	OUT2	OUT1	OUT2	IPROPI	
Hi-Z	Hi-Z	Hi-Z	Hi-Z	No current	Remains in STANDBY, no change
H	H	Hi-Z	Hi-Z	No current	ACTIVE to STANDBY
L	H	Hi-Z	H	ISNS2	ACTIVE to STANDBY
H	L	H	Hi-Z	ISNS1	ACTIVE to STANDBY

Note

For the pre-production samples, the truth table is modified as shown in Table 8-7:

Table 8-7. Control Table Differences - PWM Mode in Pre-Production Samples

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
1	0	1	1	H	H	ISNS1 or ISNS2	ACTIVE
1	0	0	0	Hi-Z	Hi-Z	No current	STANDBY

With this change, as an example, the PWM cycle for a forward → brake (HS recirculation) → forward, inputs will be as follows:

- Pre-production samples: [EN/IN1 PH/IN2] = [1 0] → [1 1] → [1 0]
- Final product: [EN/IN1 PH/IN2] = [1 0] → [0 0] → [1 0]

8.3.2.3 Independent mode

In this mode, the two half-bridges are configured to be used as two independent half-bridges. The Table 8-8 shows the logic table for bridge control. For load illustration, refer the Load Summary section.

Table 8-8. Control table - Independent mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1			No current	STANDBY
1	1	1	1			No current	STANDBY
1	0	0	0	L	L	No current	ACTIVE
1	0	0	1	L	H(2)	ISNS2(1)	ACTIVE
1	0	1	0	H(2)	L	ISNS1(1)	ACTIVE
1	0	1	1	H(2)	H(2)	ISNS1 + ISNS2(1)	ACTIVE

For the SPI variant, it is possible to have independent Hi-Z control of both half-bridges through equivalent bits, S_DRVOFF & S_DRVOFF2 in the SPI_IN register, when the **SPI_IN register has been unlocked**. Table 8-9

shows the logic table for bridge control using the pin & register combined inputs. Refer to - Register - Pin control for details on the combined inputs shown in Table 8-9.

Table 8-9. Control table - Independent mode for SPI variant, when SPI_IN is unlocked

nSLEEP	DRVOFF1 *combined*	DRVOFF2 *combined*	EN_IN1 *combined*	PH_IN2 *combined*	OUT1	OUT2	IPROPI	Device State
0	X	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	1	0	1			No current	STANDBY
1	1	1	1	1			No current	STANDBY
1	1	0	X	0	Hi-Z	L	No current	ACTIVE
1	1	0	X	1	Hi-Z	H(2)	ISNS2(1)	ACTIVE
1	0	1	0	X	L	Hi-Z	No current	ACTIVE
1	0	1	1	X	H(2)	Hi-Z	ISNS1(1)	ACTIVE
1	0	0	0	0	L	L	No current	ACTIVE
1	0	0	0	1	L	H(2)	ISNS2(1)	ACTIVE
1	0	0	1	0	H(2)	L	ISNS1(1)	ACTIVE
1	0	0	1	1	H(2)	H(2)	ISNS1 + ISNS2(1)	ACTIVE

(1) Current sourcing out of device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "L" for a fixed time

In this mode, the device behavior is as listed below:

- Load current can be sensed only for current from VM → OUTx → Load. So current sense is not possible for high-side loads
- The current on IPROPI pin is the sum of the high-side sense current from both the half-bridges. This limits the ITRIP current regulation feature as a combined current regulation, rather than as truly independent.
- Slew rate configurability is limited for low-side recirculation (low-side loads)
- Active state open load diagnostics (OLA) is possible only for high-side loads
- For the HW variant, it is NOT possible to have independent Hi-Z control of each half-bridge. Asserting DRVOFF pin high will Hi-Z both the half-bridges.

8.3.2.4 Register - Pin Control - SPI Variant Only

The SPI variant allows control of the bridge through the specific register bits, S_DRVOFF, S_DRVOFF2, S_EN_IN1, S_PH_IN2 in the SPI_IN register, provided the **SPI_IN register has been unlocked**. The user can unlock this register by writing the right combination to the SPI_IN_LOCK bits in the COMMAND register.

Additionally, the user can configure between an AND / OR logic combination of each of external input pin with their equivalent register bit in the SPI_IN register. This logical configuration is done through the equivalent selects bits in the CONFIG4 register:

- DRVOFF_SEL, EN_IN1_SEL and PH_IN2_SEL

The control of the output is similar to the truth tables described in the section before, but with these logically combined inputs. These combined inputs are listed as follows:

- Combined input = Pin input **OR** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 1'b0
- Combined input = Pin input **AND** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 1'b1
- In Independent mode:
  - DRVOFF2 combined = DRVOFF pin **OR** S_DRVOFF2 bit, if DRVOFF_SEL bit = 1'b0
  - DRVOFF2 combined = DRVOFF pin **AND** S_DRVOFF2 bit, if DRVOFF_SELbit = 1'b1

Note that external nSLEEP pin is still needed for sleep function.

This logical combination offers more configurability to the user as shown in the table below.

Table 8-10. Register - Pin Control Examples

Example	CONFIG4: xxx_SEL Bit	PIN status	SPI_IN Bit Status	Comment
DRVOFF as redundant shutoff	DRVOFF_SEL = 1'b0	DRVOFF active	S_DRVOFF active	Either DRVOFF pin = 1 or S_DRVOFF bit = 1 will shutoff the output
Pin only control	DRVOFF_SEL = 1'b1	DRVOFF active	S_DRVOFF = 1'b1	Only DRVOFF pin function is available
Register only control	PH_IN2_SEL bit = 1'b0	PH/IN2 - short to GND or float	S_PH_IN2 active	PH (direction) will be controlled by the register bit alone

Note

This logical combination is NOT supported in the pre-production samples. In this case, when the SPI_IN register is unlocked, the output is controlled from the equivalent register bits and the input pins are ignored. In other words, if SPI_IN unlocked, *xxx_combined = S_xxx register bits,* else *xxx_combined = Input pin*.

8.3.3 Device Configuration

This section describes the various device configurations to enable the user to configure the device to suit their use case.

8.3.3.1 Slew Rate (SR)

The SR pin (HW variant) or S_SR bits in the CONFIG3 register (SPI variant) determines the slew rate of the driver. This enables the user to optimize the PWM switching losses while meeting the EM conformance requirements. For the HW variant, SR is a 6-level **setting** as summarized in the table below. SPI variant has additional 2 levels.

Table 8-11. SR Table

SR Pin	S_SR Register Bits	SR_{LSOFF}, SR_{LSON} [V/µsec](1)	SR_{HSOFF} [V/µsec](2)	SR_{HSON} [V/µsec](2)
$R_{LVL2OF6}$	3'b000	1.2	40	10
Not available	3'b001	4	40	10
Not available	3'b010	6.7	40	10
$R_{LVL3OF6}$	3'b011	11.4	15	10
$R_{LVL4OF6}$	3'b100	17	20	10
$R_{LVL1OF6}$	3'b101	22	26	10
$R_{LVL6OF6}$	3'b110	32	37	10
$R_{LVL5OF6}$	3'b111	41	48	10

(1) Applicable for high-side recirculation
(2) Applicable for low-side recirculation (only in the Independent mode operation using low-side load)

Note

The SPI variant also offers an **optional** spread spectrum clocking (SSC) feature that spreads the internal oscillator frequency +/- 12% around its mean with a period triangular function of ~1.3 MHz to reduce emissions at higher frequencies.

In the HW variant, the SR pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked. Also there is **no** spread spectrum clocking (SSC) feature.

In the SPI variant, the slew rate setting can be changed at any time when SPI communication is available by writing to the S_SR bits. This change is immediately reflected.

Note

For the pre-production samples, the SR settings are as shown in Table 8-12 the table below. Also, in the HW variant, SSC feature is always enabled.

Table 8-12. Pre-Production Samples - SR Table

SR Pin	S_SR Register Bits	SR_{LSOFF}, SR_{LSON} [V/µsec](1)	SR_{HSOFF} [V/µsec](2)	SR_{HSON} [V/µsec](2)
$R_{LVL1OF6}$	3'b000	23	23	8
$R_{LVL2OF6}$	3'b001	1.6	1.6	1.6
$R_{LVL3OF6}$	3'b010	33	33	8
$R_{LVL4OF6}$	3'b011	38	38	8
$R_{LVL5OF6}$	3'b100	43	43	8
$R_{LVL6OF6}$	3'101	28	28	8
Not available	3'b110	18	18	8
Not available	3'b111	12	12	8

8.3.3.2 IPROPI

The device integrates a current sensing feature with a proportional analog current output on the IPROPI pin that can be used for load current regulation. This eliminates the need of an external sense resistor or sense circuitry reducing system size, cost, and complexity.

The device senses the load current by using a shunt-less high-side current mirror topology. This way the device can only sense an uni-directional high-side current from VM → OUTx → Load through the high-side FET when it is fully turned ON (linear mode). The IPROPI pin outputs an analog current proportional to this sensed current scaled by A_{IPROPI} as follows:

$I_{IPROPI} = (I_{HS1} + I_{HS2}) / A_{IPROPI}$

The IPROPI pin must be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage V_{IPROPI}. This allows for the load current to be measured as a voltage-drop across the R_{IPROPI} resistor with an analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

The current expressed on IPROPI is the sum of the currents flowing out of the OUTx pins from VM. This implies that:

- In full-bridge operation using PWM or PH/EN mode, the current expressed on IPROPI pin is always from one of the half-bridges that is sourcing the current from VM to the load.
- In independent mode, the current expressed on IPROPI pin could be from either half-bridges or both of them. It is **not** possible to observe only one half-bridge current independently.

8.3.3.3 ITRIP Regulation

The device offers an optional internal load current regulation feature using fixed TOFF time method. This is done by comparing the voltage on the IPROPI pin against a reference voltage determined by ITRIP setting. TOFF time is fixed at 30 µsec for HW variant, while it is configurable between or 20 to 50 µsec for the SPI variant using TOFF_SEL bits in the CONFIG3 register.

The ITRIP regulation, when enabled, comes into action only when the HS FET is enabled and current sensing is possible. In this scenario, when the voltage on the IPROPI pin exceeds the reference voltage set by the ITRIP setting, the internal current regulation loop forces the following action:

- In PH/EN or PWM mode, OUT1 = H, OUT2 = H (high-side recirculation) for the fixed TOFF time
  - Cycle skipping: Due to minimum duty cycle limitations (especially at low slew rate settings and high VM), load current will contiue to increase even with ITRIP regulation. In order to prevent this current walk away, a cycle skipping scheme is implemented, where, if IOUT sensed is still greater than ITRIP at the end of

TOFF time, then the recirculation time is extended by an additional TOFF period. This recirculation time addition will continue till IOUT sensed is less than ITRIP at the end of the TOFF period.

- In Independent mode, If OUTx = H, then toggle OUTx = L for the fixed TOFF time, else no action on OUTx

Note

The user inputs always takes **precedence** over the internal control. That means that if the inputs change during the TOFF time, the remainder of the TOFF time is ignored and the outputs will follow the inputs as commanded.

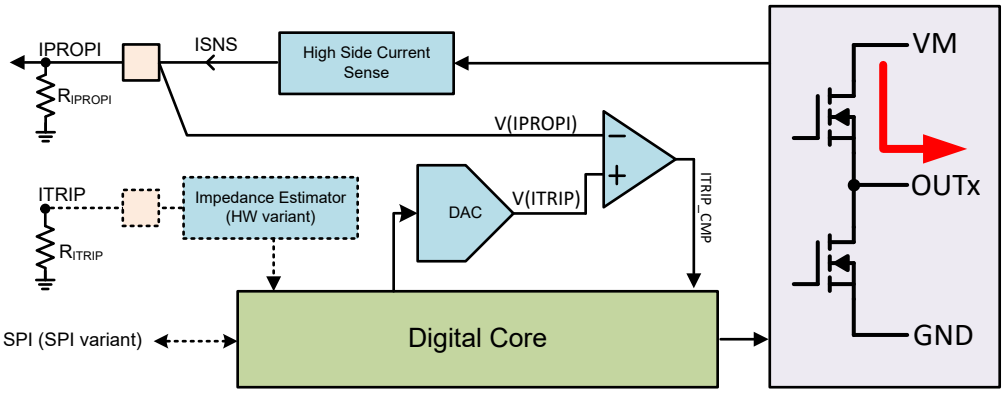


Figure 8-4. ITRIP Implementation

Current limit is set by the following equation:

$$\text{ITRIP regulation level} = V_{ITRIP} / R_{IPROPI} \times A_{IPROPI} \quad (2)$$

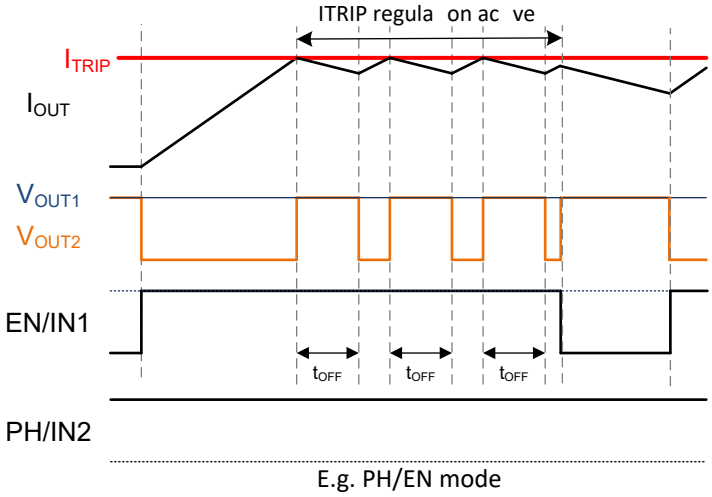


Figure 8-5. Fixed TOFF ITRIP Current Regulation

In Independent mode, since ITRIP regulation is based on summation of the two half-bridge currents on IPROPI pin, it is **not** possible to have completely independent current regulation for the two half-bridges simultaneously.

The ITRIP comparator output (ITRIP_CMP) is ignored during output slewing to avoid false triggering of the comparator output due to current spikes from the load capacitance. Additionally, in the event of transition from low-side recirculation, an additional blanking time t_{BLANK} is needed for the sense loop to stabilize before the ITRIP comparator output is valid.

ITRIP is a 6-level **setting** for the HW variant. The SPI variant offers two more settings. This is summarized in the table below:

Table 8-13. ITRIP Table

ITRIP Pin	S_ITRIP Register Bits	V_{ITRIP} [V]
$R_{LVL1OF6}$	3'b000	Regulation Disabled
$R_{LVL2OF6}$	3'b001	1.18
Not available	3'b010	1.41
Not available	3'b011	1.65
$R_{LVL3OF6}$	3'b100	1.98
$R_{LVL4OF6}$	3'b101	2.31
$R_{LVL5OF6}$	3'b110	2.64
$R_{LVL6OF6}$	3'b111	2.97

In the HW variant of the device, the ITRIP pin changes are **transparent** and changes are reflected immediately.

In the SPI variant of the device, the ITRIP setting can be changed at any time when SPI communication is available by writing to the S_ITRIP bits. This change is immediately reflected in the device behavior.

SPI variant only - If the ITRIP regulation levels are reached, the ITRIP_CMP bit in the STATUS1 register is set. There is no nFAULT pin indication. This bit can be cleared with a CLR_FLT command.

Note

For pre-production samples, the ITRIP settings are as shown in the table below.

Table 8-14. Pre-Production Samples - ITRIP Table

ITRIP Pin	S_ITRIP Register Bits	V_{ITRIP} [V]
$R_{LVL1OF6}$	3'b000	Regulation Disabled
$R_{LVL2OF6}$	3'b001	1.65
$R_{LVL3OF6}$	3'b010	1.98
$R_{LVL4OF6}$	3'b011	2.31
$R_{LVL5OF6}$	3'b100	2.64
$R_{LVL6OF6}$	3'b101, 3'b110, 3'b111	2.97

8.3.3.4 DIAG

The DIAG is a pin (HW variant) or register (SPI variant) setting that is used in both ACTIVE and STANDBY operation of the device, as follows:

- STANDBY state
  - In PH/EN or PWM modes: Enable or disable Off-state diagnostics (OLP).
  - Enable or disable Off-state diagnostics (OLP), as well as select the OLP combinations when enabled. Refer to the tables in the Off-state diagnostics (OLP) section for details on this.
- ACTIVE state
  - Mask ITRIP regulation function if the load type is indicated as high-side load.
  - SPI variant only - Mask active open load detection (OLA) if the load type is indicated as low-side. load
  - HW variant only - Configure fault reaction between retry and latch settings

8.3.3.4.1 HW variant

For the HW variant, the DIAG pin is a 6-level **setting**. Depending on the mode, its configurations are summarized in the table below.

Table 8-15. DIAG table for the HW variant, PH/EN or PWM mode

DIAG pin	STANDBY state	ACTIVE state
	Off-state diagnostics	Fault reaction
$R_{LVL1OF6}$	Disabled	Retry
All other levels	Enabled(1)	Latch

Table 8-16. DIAG table for the HW variant, Independent mode

DIAG pin	STANDBY state	ACTIVE state		
	Off-state diagnostics	Load Configuration	Fault reaction	IPROPI / ITRIP
$R_{LVL1OF6}$	Disabled	Low-side load	Retry	Available
$R_{LVL2OF6}$	Enabled(1)	Low-side load	Latch	Available
$R_{LVL3OF6}$	Enabled(1)	High-side load	Latch	Disabled
$R_{LVL4OF6}$	Enabled(1)	High-side load	Retry	Disabled
$R_{LVL5OF6}$	Disabled	Low-side load	Latch	Available
$R_{LVL6OF6}$	Enabled(1)	Low-side load	Retry	Available

(1) Refer to the tables in the Off-state diagnostics (OLP) section for combination details

Note

HW variant only - Option to disable off-state diagnostics for a high-side load use case is not supported. In this case, setting DRVOFF pin high and IN pin low is only way to disable off-state diagnostics.

In the HW variant, the DIAG pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

8.3.3.4.2 SPI variant

For the SPI variant, S_DIAG is a 2-bit setting in the CONFIG2 register. Depending on the mode, its configurations are summarized in the table below.

Table 8-17. DIAG table for the SPI variant, PH/EN or PWM mode

S_DIAG bits	STANDBY state	ACTIVE state
	Off-state diagnostics	On-state diagnostics
2'b00	Disabled	Available
2'b01, 2'b10, 2'b11	Enabled(1)	Available

Table 8-18. DIAG table for the SPI variant, Independent mode

S_DIAG bits	STANDBY state	ACTIVE state		
	Off-state diagnostics	Load Configuration	On-state diagnostics	IPROPI / ITRIP
2'b00	Disabled	Low-side load	Disabled	Available
2'b01	Enabled(1)	Low-side load	Disabled	Available
2'b10	Disabled	High-side load	Available	Disabled
2'b11	Enabled(1)	High-side load	Available	Disabled

(1) Refer to the tables in the Off-state diagnostics (OLP) section for combination details

In the SPI variant of the device, the settings can be changed anytime when SPI communication is available by writing to the S_DIAG bits. This change is immediately reflected.

8.3.4 Protection and Diagnostics

The driver is protected against over-current and over-temperature events to ensure device robustness. Additionally, the device also offers load monitoring (on-state and off-state), over/ under voltage monitoring on VM pin to signal any unexpected voltage conditions. Fault signaling is done through a low-side open drain nFAULT pin which gets pulled to GND by I_{nFAULT_PD} current on detection of a fault condition. Transition to SLEEP state automatically de-asserts nFAULT.

Note

In the SPI variant, nFAULT pin logic level is the inverted copy of the FAULT bit in the FAULT SUMMARY register. Only exception is when off-state diagnostics are enabled and SPI_IN register is locked (Refer OLP section) .

For the SPI variant, whenever nFAULT is asserted low, the device logs the fault into the FAULT SUMMARY and STATUS registers. These registers can be cleared only by

- CLR FLT command or
- SLEEP command through the nSLEEP pin

It is possible to get all the useful diagnostic information for periodic software monitoring in a single 16 bit SPI frame by:

- Reading the STATUS1 register during ACTIVE state
- Reading the STATUS2 register during STANDBY state

All the diagnosable fault events can be uniquely identified by reading the STATUS registers.

8.3.4.1 Over Current Protection (OCP)

- Device state: ACTIVE
- Mechanism & thresholds: An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold, I_{OCP}, for longer than t_{OCP}, then an over current fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Reaction is based on mode selection:
    - PH/EN or PWM mode - Both OUTx is Hi-Z
    - Independent mode - The affected half-bridge OUTx is Hi-Z
  - For a short to GND fault (over current detected on the high-side FET), the IPROPI pin continues to be pulled up to V_{IPROPI_LIM} even if the FET has been disabled. For the HW variant, this helps differentiate a short to GND fault during ACTIVE state from other fault types, as the IPROPI pin is pulled high while the nFAULT pin is asserted low.
- Reaction configurable between latch setting and retry setting based on t_{RETRY} and t_{CLEAR}
- User can add a small 6.3V capacitor in the range of 10 nF to 100 nF on the IPROPI pin to avoid a race condition with ITRIP regulation in case of a load short condition when ITRIP regulation is enabled.
  - In case of a load short where there is enough inductance in the short, ITRIP regulation could trigger ahead of the OCP detection, resulting in the device missing the OCP detection. To ensure that OCP detection wins this race condition, a small capacitor (10 nF - 100 nF) on the IPROPI pin is recommended. This capacitance slows down the ITRIP regulation loop enough to allow the OCP detection circuit to work as intended.

The SPI variant offers configurable I_{OCP} levels and t_{OCP} filter times. Refer CONFIG4 register for these settings.

8.3.4.2 Over Temperature Protection (TSD)

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: The device has several temperature sensors spread around the die. If any of the sensors detect an over temperature event, set by T_{TSD} for a time greater than t_{TSD}, then an over temperature fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z
- Reaction configurable between latch setting and retry setting based on T_{HYS} and t_{CLEAR_TSD}

8.3.4.3 Off-State Diagnostics (OLP)

The user can determine the impedance on the OUTx node using off-state diagnostics in the STANDBY state when the power FETs are off. With this diagnostics, it is possible to detect the following fault conditions passively in the STANDBY state:

- Output short to VM or GND < 100 Ω
- Open load > 1K Ω for full-bridge load or low-side load
- Open load > 10K Ω for high-side load, VM = 13.5 V

Note

It is NOT possible to detect a **load short** with this diagnostic. However, the user can deduce this logically if an over current fault (OCP) occurs during ACTIVE operation, but OLP diagnotics do not report any fault in the STANDBY state. Occurrence of both OCP in the ACTIVE state and OLP in the STANDBY state would imply a terminal short (short on OUT node).

- The user can configure the following combinations
  - Internal pull up resistor (R_{OLP_PU}) on OUTx
  - Internal pull down resistor (R_{OLP_PD}) on OUTx
  - Comparator reference level
  - Comparator input selection (OUT1 or OUT2)
- This combination is determined by the controller inputs (pins only for the HW variant) or equivalent bits in the SPI_IN register for the SPI variant if the SPI_IN register has been unlocked.
- HW variant - When off-state diagnostics are enabled, comparator output (OLP_CMP) is available on nFAULT pin.
- SPI variant - The off-state diagnostics comparator output (OLP_CMP) is available on OLP_CMP bit in STATUS2 register. Additionally, if the SPI_IN register has been locked, this comparator output is also available on the nFAULT pin when off-state diagnostics are enabled.
- The user is expected to toggle through all the combinations and record the comparator output after its output is settled.
- Based on the input combinations and comparator output, the user can determine if there is a fault on the output.

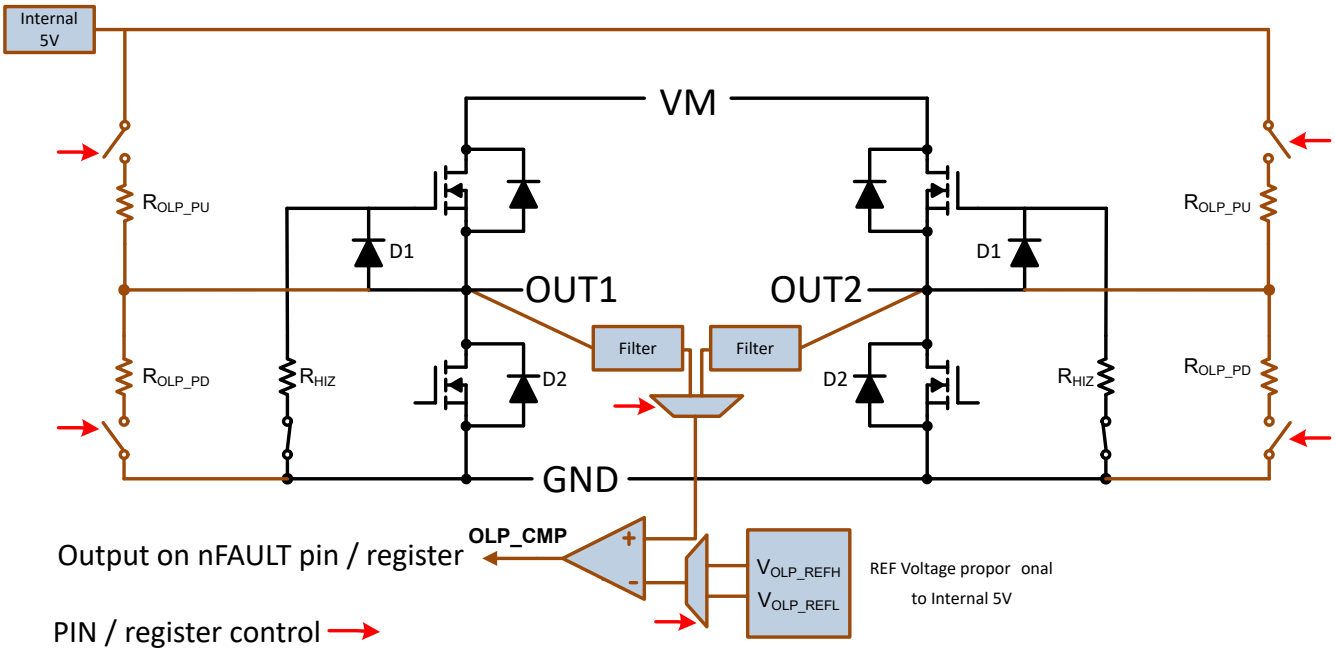


Figure 8-6. Off-State Diagnostics for full-bridge Load (PH/EN or PWM Mode)

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a full-bridge load in PH/EN or PWM modes is shown in Table 8-19.

Table 8-19. Off-State Diagnostics Table - PH/EN or PWM Mode (full-bridge)

User Inputs				OLP Set-Up				OLP CMP Output			
nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	GND Short	VM Short
1	1	1	0	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFH}	OUT1	L	H	L	H
1	1	0	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFL}	OUT2	H	L	L	H
1	1	1	1	R_{OLP_PD}	R_{OLP_PU}	V_{OLP_REFL}	OUT2	H	H	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load in Independent mode is shown in Table 8-20.

Table 8-20. Off-State Diagnostics Table for Low-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short
LVL2, LVL6	2'b01	1	1	1	don't care	R_{OLP_PU}	Hi-Z	V_{OLP_REFH}	OUT1	L	H	H
LVL3, LVL4	2'b11	1	1	1	don't care	R_{OLP_PD}	Hi-Z	V_{OLP_REFL}	OUT1	L	L	H
LVL2, LVL6	2'b01	1	1	0	1	Hi-Z	R_{OLP_PU}	V_{OLP_REFH}	OUT2	L	H	H
LVL3, LVL4	2'b11	1	1	0	1	Hi-Z	R_{OLP_PD}	V_{OLP_REFL}	OUT2	L	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a high-side load in Independent mode is shown in Table 8-21.

Table 8-21. Off-State Diagnostics Table for High-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short
LVL2, LVL6	2'b01	1	1	1	don't care	R_{OLP_PU}	Hi-Z	V_{OLP_REFH}	OUT1	H	H	L
LVL3, LVL4	2'b11	1	1	1	don't care	R_{OLP_PD}	Hi-Z	V_{OLP_REFL}	OUT1	H	L	L
LVL2, LVL6	2'b01	1	1	0	1	Hi-Z	R_{OLP_PU}	V_{OLP_REFH}	OUT2	H	H	L
LVL3, LVL4	2'b11	1	1	0	1	Hi-Z	R_{OLP_PD}	V_{OLP_REFL}	OUT2	H	L	L

Note

For the pre-production samples, it is NOT possible to differentiate between an open fault and a load short in the Independent mode.

8.3.4.4 On-State Diagnostics (OLA) - SPI Variant Only

- Device state: ACTIVE - high-side recirculation

- Mechanism and threshold: On-state diagnostics (OLA) can detect an open load detection in the ACTIVE state during high-side recirculation. This includes high-side load connected directly to VM or through a high-side FET on the other half-bridge. During a PWM switching transition, the inductive load current re-circulates into VM through the HS body diode when the LS FET is turned OFF. The device looks for a voltage spike on OUTx above VM during the brief dead time, before the HS FET is turned ON. To observe the voltage spike, this load current needs to be higher than the pull down current (I_{PD_OLA}) on the output asserted by the FET driver. Absence of this voltage spike for "3" consecutive re-circulation switching cycles indicates a loss of load inductance or increase in load resistance and is detected as an OLA fault.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between latch setting and retry setting. In retry setting, OLA fault is automatically cleared with the detection of "3" consecutive voltage spikes during re-circulation switching cycles.

This monitoring is optional and can be disabled.

Note

OLA is not supported for low-side loads (low-side recirculation).

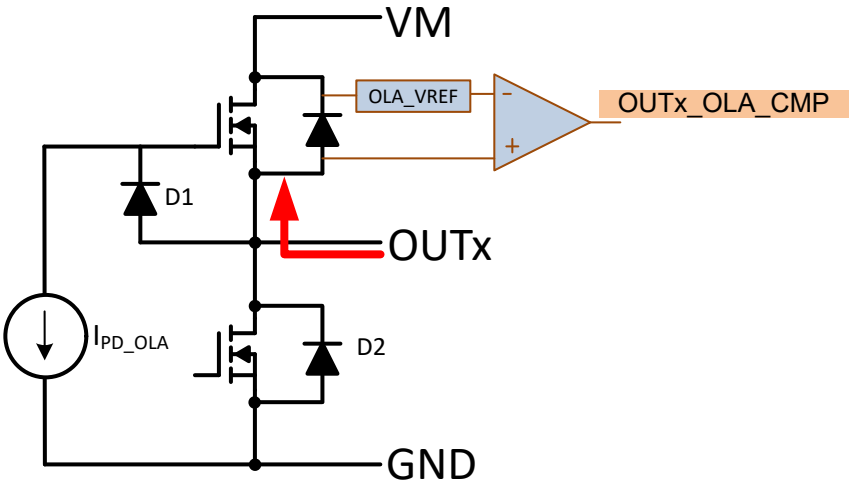


Figure 8-7. On-State Diagnostics

8.3.4.5 VM Over Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin exceeds the threshold, set by V_{VMOV} for a time greater than t_{VMOV}, then an VM over voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between retry and latch setting

In the SPI variant, this monitoring is optional and can be disabled. Also the thresholds are configurable. Refer CONFIG1 register.

8.3.4.6 VM Under Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin drops below the threshold, set by V_{VMUV} for a time greater than t_{VMUV}, then an VM under voltage fault is detected.
- Action:

  - nFAULT pin is asserted low
  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z
- HW and SPI (S) variant: Reaction fixed to retry setting
- Only for SPI (P) variant: Reaction configurable between retry and latch setting
- Note that retry time is only dependent on recovery of VM under voltage condition and is independent of t_{RETRY} / t_{CLEAR} times

8.3.4.7 Power On Reset (POR)

- Device state: ALL
- Mechanism & thresholds: If logic supply drops below VDD_{POR_FALL} for a time greater than t_{POR}, then a power on reset will occur that will hard reset the device.
- Action:
  - nFAULT pin is de-asserted
  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z.
  - When this supply recovers above the VDD_{POR_RISE} level, the device will go through a wake-up initialization and nFAULT pin will be asserted low to notify the user on this reset (Refer Wake-up transients).
- HW and SPI (S) variant: These thresholds translate to VM_{POR_FALL} and VM_{POR_RISE} as the logic supply is internally derived from the VM supply
- Only for SPI (P) variant: These thresholds directly map to the VDD pin voltage (VDD_{POR_FALL} and VDD_{POR_RISE})
- Fault reaction: Always retry, retry time depends on the external supply condition to initiate a device wake-up

8.3.4.8 Event Priority

In the ACTIVE state, in a scenario where two or more events occur simultaneously, the device assigns control of the driver based on the following priority table.

Table 8-22. Event Priority Table

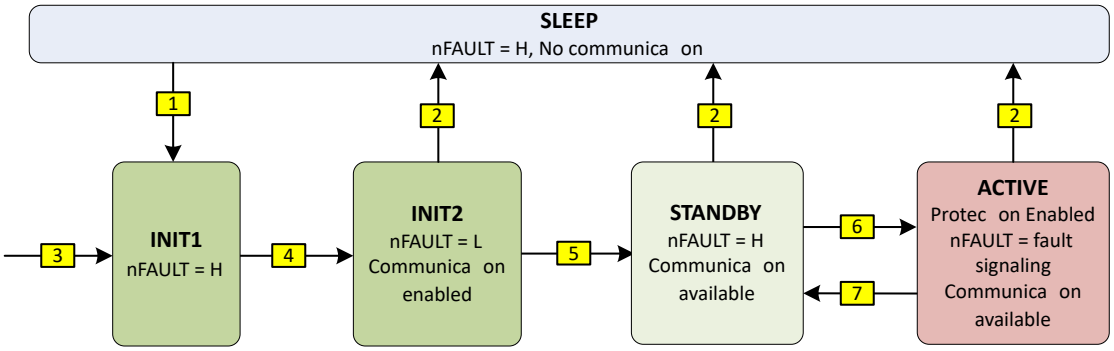
Event	Priority
User SLEEP command	1
User input: DRVOFF	2
Over temperature detection (TSD)	3
Over current detection (OCP)(1)	4
VM under voltage detection (VMUV)	5
User input: EN/IN1 and/or PH/IN2	6
Internal PWM control from ITRIP regulation	7
VM over voltage detection (VMOV)(2)	8
On-state fault detection (OLA - SPI variant only)(2)	9

(1) If the device is waiting for an OCP event to be confirmed (waiting for t_{OCP}) when any of events with lower priority than OCP occur, then the device may delay servicing the other events up to a maximum time of t_{OCP} to enable detection of the OCP event.
(2) Priority is "don't care" in this case as this fault event does not cause a change in OUTx

8.4 Device Functional States

The device has three functional states:

- SLEEP
- STANDBY
- ACTIVE



1. nSLEEP = 1 for t > t_{WAKE}
2. nSLEEP = 0 for t > t_{SLEEP}
3. Power on reset
4. End of t_{COM}
5. CLR_FLT or HW RESET pulse from from controller & End of t_{READY}
6. DRVOFF = 0 & [IN1/EN IN2/PH] != [1 1], if PWM mode
7. DRVOFF = 1 or [IN1/EN IN2/PH] = [1 1], if PWM mode

Note

For pre-production samples, [IN1/EN IN2/PH] = [0 0], if PWM mode

Figure 8-8. Illustrative State Diagram

These states are described in the following section.

8.4.1 SLEEP State

This state occurs when nSLEEP pin is asserted low for a time > t_{SLEEP} or voltage on the VDD pin is < VDD_{POR_FALL}.

This is the deep sleep low power (I_{SLEEP}) state of the device where all functions except a wake-up command are not serviced. The drivers are in Hi-Z. The internal power supply rails (5 V and others) are powered off. nFAULT pin is de-asserted in this state. The device can enter this state from either the STANDBY or the ACTIVE state, when the nSLEEP pin is asserted low for time longer than t_{SLEEP} (HW variant) or for t_{SLEEP_SPI} (SPI (S) variant).

8.4.2 STANDBY State

The device is in this state when nSLEEP pin is asserted high or the voltage on the VDD pin is > VDD_{POR_RISE} with DRVOFF = 1'b0 for all modes and additionally, in PWM mode when both IN1/EN & IN2/PH are 1'b1 [Note: 1'b0 for pre-production samples]. In this state, the device is powered up ($I_{STANDBY}$), with the driver Hi-Z and nFAULT de-asserted. The device is ready to transition to ACTIVE state or SLEEP state when commanded so. Off-state diagnostics (OLP), if enabled, are done in this state.

8.4.3 Wake-up to STANDBY State

The device starts transition from SLEEP state to STANDBY state

- if the nSLEEP pin goes high for a duration longer than t_{WAKE}, or
- if VM supply > VM_{POR_RISE} or VDD supply > VDD_{POR_RISE} such that internal POR is released to indicate a power-up.

The device goes through an initialization sequence to load its internal registers and wake-up all the blocks in the following sequence:

- At a certain time, t_{COM} from wake-up, the device is capable of communication. This is indicated by asserting the nFAULT pin low.
- This is followed by the time t_{READY}, when the device wake-up is complete.
- At this point, once the device receives a nSLEEP reset pulse (HW variant) or a CLR FAULT command through SPI (SPI variant) as an acknowledgment of the wake-up from the controller, the device enters the STANDBY state. This is indicated by the de-assertion of the nFAULT pin. The driver is held in Hi-Z till this point.

- From here on, the device is ready to drive the bridge based on the truth tables for the specific mode configured.

Refer to the wake-up transients waveforms for the illustration.

8.4.4 ACTIVE State

The device is fully functional in this state with the drivers controlled by other inputs as described in prior sections. All protection features are fully functional with fault signaling on nFAULT pin. SPI communication is available.The device can transition into this state only from the STANDBY state.

8.4.5 nSLEEP Reset Pulse (HW Variant Only)

This is a special communication signal from the controller to the device through the nSLEEP pin available only for the HW variant. This is used to:

- Acknowledge the nFAULT asserted during the SLEEP/ Power up transition to STANDBY state
- Clear a latched fault when the fault reaction is configured to the LATCHED setting, without forcing the device into SLEEP or affecting any of the other functions (Equivalent to the CLR_FAULT command in the SPI variant)

This pulse on nSLEEP must be greater than the nSLEEP deglitch time of t_{RESET} time, but shorter than t_{SLEEP} time, as shown in case # 3, in Table 8-23 below.

Table 8-23. nSLEEP Timing (HW Variant Only)

Case #	Window Start Time	Window End Time	Command Interpretation	
			Clear Fault	Sleep
1	0	t_{RESET} min	No	No
2	t_{RESET} min	t_{RESET} max	Interdeterminate	No
3	t_{RESET} max	t_{SLEEP} min	Yes	No
4	t_{SLEEP} min	t_{SLEEP} max	Yes	Interdeterminate
5	t_{SLEEP} max	No limit	Yes	Yes

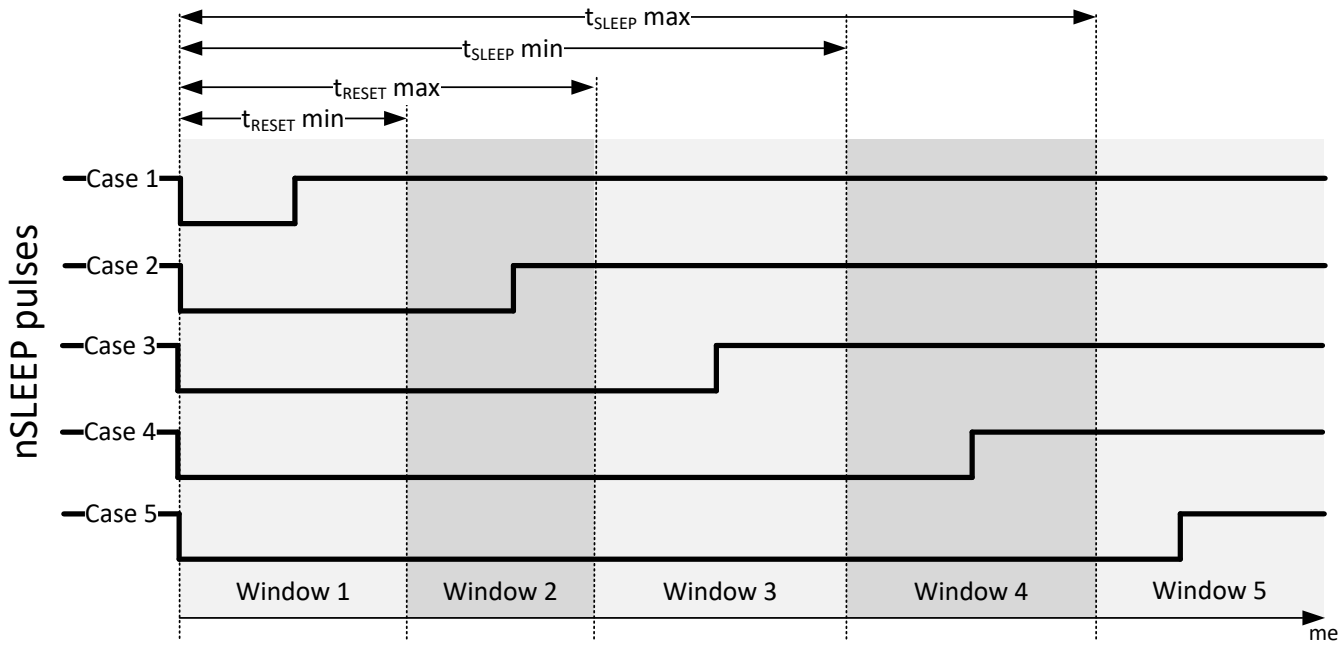


Figure 8-9. nSLEEP Pulse Scenarios

8.5 Programming - SPI Variant Only

8.5.1 SPI Interface

The SPI variant has full-duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. The SPI operates in peripheral mode and connects to a controller. The serial data input (SDI) word consists of a 16-bit word, with an 8-bit command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of the FAULT_SUMMARY byte (S1), followed by a report byte (R1). The report byte is either the register data being accessed by read command or null for a write command. The data sequence between the MCU and the SPI peripheral driver is shown in Figure 8-10.

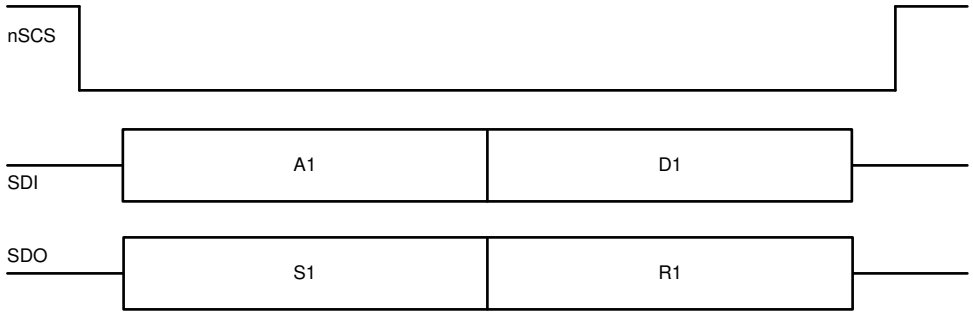


Figure 8-10. SPI Data - Standard "16-bit" Frame

A valid frame must meet the following conditions:

- SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- nSCS pin should be pulled high between words.
- When nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by the device on the subsequent falling edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chain frame with "n" number of peripheral devices, 16 + (n x 16) SCLK cycles must occur for a valid transaction. Else, a frame error (SPI_ERR) is reported and the data is ignored if it is a WRITE operation.

8.5.2 Standard Frame

The SDI input data word is 2 bytes long and consists of the following format:

- Command byte (first byte)
  - MSB bit indicates frame type (bit B15 = 0 for standard frame).
  - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
  - Followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (second byte)
  - Second byte indicates data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 8-24. SDI - Standard Frame Format

	Command Byte								Data Byte							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 2 bytes long and consists of the following format:

- Status byte (first byte)

  - 2 MSB bits are forced high (B15, B14 = 1)
  - Following 6 bits are from the FAULT SUMMARY register (B13:B8)
- Report byte (second byte)
  - The second byte (B7:B0) is either the data currently in the register being read for a read operation (W0 = 1), or, existing data in the register being written to for a write command (W0 = 0)

Table 8-25. SDO - Standard Frame Format

	Status Byte								Report Byte							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	VMOV	VMUV	OCP	TSD	SPI_ERR	D7	D6	D5	D4	D3	D2	D1	D0

Note

For the pre-production samples, B8 in the above SDO format is OLA bit (not SPI_ERR as shown).

8.5.3 SPI Interface for Multiple Peripherals

Multiple devices can be connected to the controller with and without the daisy chain. For connecting a 'n' number of devices to a controller without using a daisy chain, 'n' number of I/O resources from controller has to utilized for nSCS pins as shown in Figure 8-11. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple devices. Figure 8-12

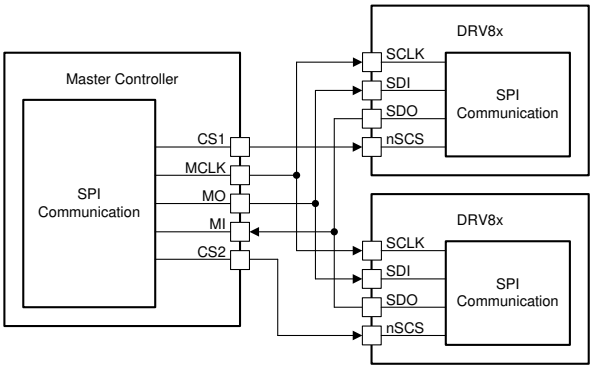


Figure 8-11. SPI Operation Without Daisy Chain

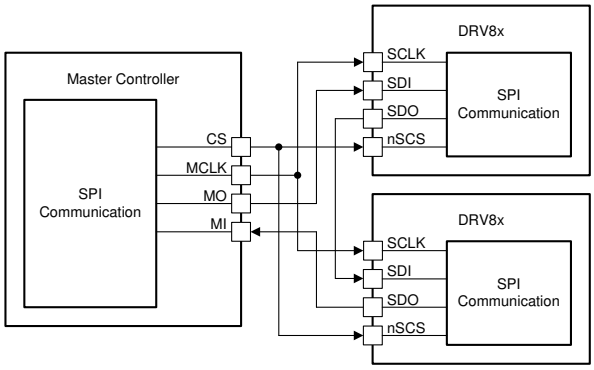


Figure 8-12. SPI Operation With Daisy Chain

8.5.3.1 Daisy Chain Frame for Multiple Peripherals

The device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 8-13 shows the topology with waveforms, where, number of peripherals connected in a daisy chain "n" is set to 3. A maximum of up to 63 devices can be connected in this manner.

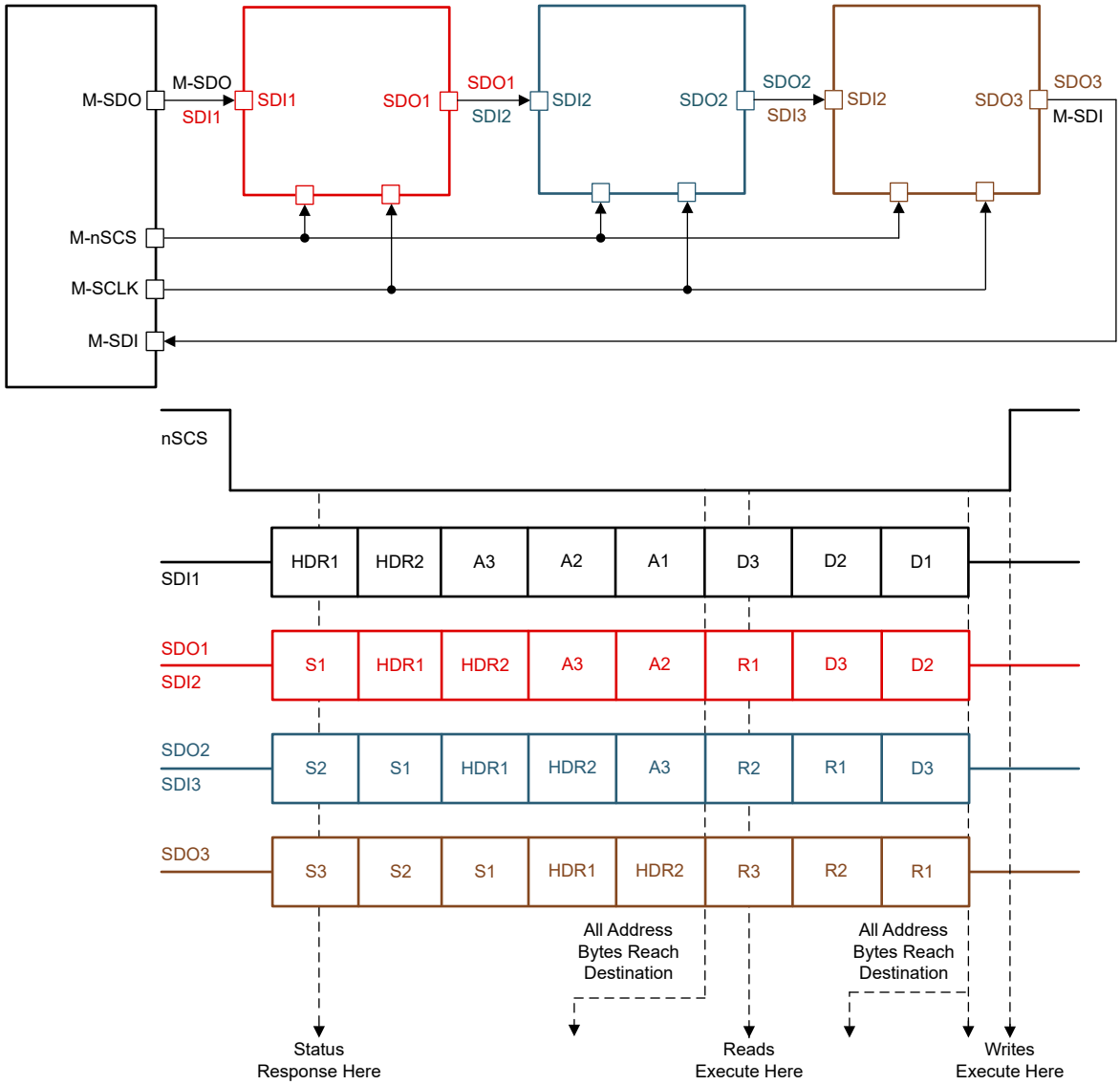


Figure 8-13. Daisy Chain SPI Operation

The SDI sent by the controller in this case would be in the following format (see SDI1 in Figure 8-13):

- 2 bytes of header (HDR1, HDR2)
- "n" bytes of command byte starting with furthest peripheral in the chain (for this example, this is A3, A2, A1)
- "n" bytes of data byte starting with furthest peripheral in the chain (for this example, this is D3, D2, D1)
- Total of 2 x "n" + 2 bytes

While the data is being transmitted through the chain, the controller receives it in the following format (see SDO3 in Figure 8-13):

- 3 bytes of status byte starting with furthest peripheral in the chain (for this example, this is S3, S2, S1)
- 2 bytes of header that were transmitted before (HDR1, HDR2)
- 3 bytes of report byte starting with furthest peripheral in the chain (for this example, this is R3, R2, R1)

The Header bytes are special bytes asserted at the beginning of a daisy chain SPI communication. **Header bytes must start with 1 and 0 for the two leading bits.**

The first header byte (HDR1) contains information of the total number of peripheral devices in the daisy chain. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in Figure 8-14. Up to 63 devices can be connected in series per daisy chain connection. Number of peripheral = 0 is not permitted and will result in a SPI_ERR flag.

The second header byte (HDR2) contains a global CLR FAULT command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. The 5 trailing bits of the HDR2 register are marked as SPARE (don't care bits). These can be used by the MCU to determine integrity of the daisy chain connection.

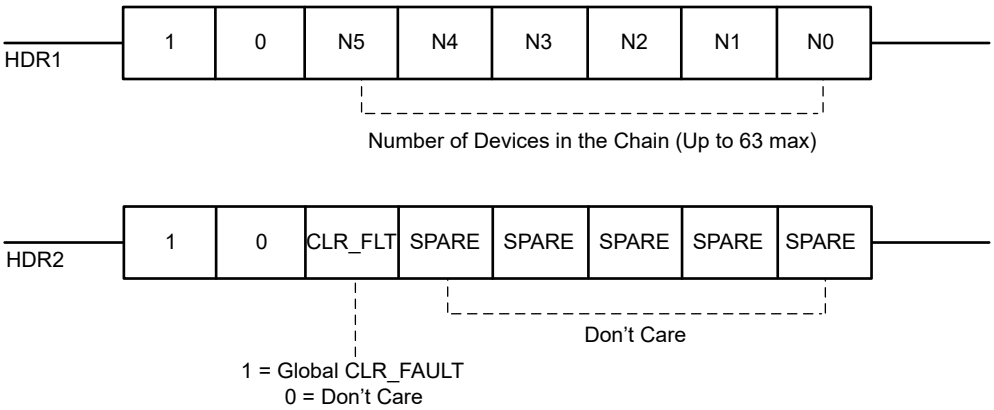


Figure 8-14. Header bytes

In addition, the device recognizes bytes that start with 1 and 1 for the two leading bits as a "pass" byte. These "pass" bytes are NOT processed by the device, but they are simply transmitted out on SDO in the following byte.

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two status bytes before receiving the two header bytes.

From the two status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The command, data, status and report bytes remain the same as described in the standard frame format.

8.6 Register Map - SPI Variant Only

This section describes the user configurable registers in the device.

Note

While the device allows register writes at any time SPI communication is available, it is recommended to exercise caution while updating registers in the ACTIVE state while the load is being driven. This is especially important for settings such as S_MODE and S_DIAG which control the critical device configuration. In order to prevent accidental register writes, the device offers a locking mechanism through the REG_LOCK bits in the COMMAND register to lock the contents of all configurable registers. Best practice would be to write all the configurable registers during initialization and then lock these settings. Run-time register writes for output control are handled by the SPI_IN register, which offers its own separate locking mechanism through the SPI_IN_LOCK bits.

8.6.1 User Registers

The following table lists all the registers that can be accessed by the user. All register addresses NOT listed in this table should be considered as "reserved" locations and access is blocked to this space. Accessing them will cause a SPI_ERR.

Table 8-26. User Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type (2)	Addr
DEVICE_ID	DEV_ID[5]	DEV_ID[4]	DEV_ID[3]	DEV_ID[2]	DEV_ID[1]	DEV_ID[0]	REV_ID[1]	REV_ID[0]	R	00h
FAULT_SUMMARY	SPI_ERR(3)	POR	FAULT	VMOV	VMUV	OCP	TSD	OLA (3)	R	01h
STATUS1	OLA1	OLA2	ITRIP_CMP	ACTIVE	OCP_H1	OCP_L1	OCP_H2	OCP_L2	R	02h
STATUS2	DRVOFF_STAT	N/A(4)	N/A(4)	ACTIVE	N/A(4)	N/A(4)	N/A(4)	OLP_CMP	R	03h
COMMAND	CLR_FLT	N/A(4)	N/A(4)	SPI_IN_LOCK[1]	SPI_IN_LOCK[0] (1)	N/A(4)	REG_LOCK[1]	REG_LOCK[0] (1)	R/W	08h
SPI_IN	N/A(4)	N/A(4)	N/A(4)	N/A(4)	S_DRVOFF (1)	S_DRVOFF2 (1)	S_EN_IN1	S_PH_IN2	R/W	09h
CONFIG1	EN_OLA	VMOV_SEL[1]	VMOV_SEL[0]	SSC_DIS(1)	OCP_RETRY	TSD_RETRY	VMOV_RETRY	OLA_RETRY	R/W	0Ah
CONFIG2	PWM_EXTEND	S_DIAG[1]	S_DIAG[0]	N/A(4)	N/A(4)	S_ITRIP[2]	S_ITRIP[1]	S_ITRIP[0]	R/W	0Bh
CONFIG3	TOFF[1]	TOFF[0] (1)	N/A(4)	S_SR[2]	S_SR[1]	S_SR[0]	S_MODE[1]	S_MODE[0]	R/W	0Ch
CONFIG4	TOCP_SEL[1]	TOCP_SEL[0]	N/A(4)	OCP_SEL[1]	OCP_SEL[0]	DRVOFF_SEL(1)	EN_IN1_SEL	PH_IN2_SEL	R/W	0Dh

(1) Defaulted to 1b on reset, others are defaulted to 0b on reset
(2) R = Read Only, R/W = Read/Write
(3) OLA replaced by SPI_ERR in the first SDO byte response, common to all SPI frames. Refer SDO - Standard frame format.
(4) N/A = Not available (read back of this bit will be 0b)

Note

For the pre-production samples, the register map has the following differences:

Table 8-27. Pre-Production Samples - Register Map Differences

Address	Name	Bit	Pre-production samples
02h	STATUS1	4	OLP_CMP
03h	STATUS2	All	Not defined
0Dh	CONFIG4	All	Not defined

8.6.1.1 DEVICE_ID register (Address = 00h)

Return to the User Register table.

Device	Pre-production samples	Final Product
DRV8243S-Q1	30h	32h
DRV8244S-Q1	40h	42h
DRV8245S-Q1	50h	52h
DRV8243P-Q1	Not available	36h
DRV8244P-Q1	Not available	46h
DRV8245P-Q1	Not available	56h

8.6.1.2 FAULT_SUMMARY Register (Address = 01h) [reset = 40h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	SPI_ERR	R	0b	1b indicates that a SPI communication fault has occurred in the previous SPI frame.
6	POR	R	1b	1b indicates that a power-on-reset has been detected.
5	FAULT	R	0b	Logic OR of SPI_ERR, POR, VMOV, VMUV, OCP, TSD & OLA
4	VMOV	R	0b	1b indicates that a VM over voltage has been detected. Refer VMOV_SEL to change thresholds or disable diagnostic, VMOV_RETRY to configure fault reaction.
3	VMUV	R	0b	1b indicates that a VM under voltage has been detected.
2	OCP	R	0b	1b indicates that an over current has been detected in either one or more power FETs. Refer OCP_SEL, TOCP_SEL to change thresholds & filter times. Refer OCP_RETRY to configure fault reaction.
1	TSD	R	0b	1b indicates that an over temperature has been detected. Refer TSD_RETRY to configure fault reaction.
0	OLA	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state. Refer to EN_OLA to disable diagnostic, OLA_RETRY to configure fault reaction.

8.6.1.3 STATUS1 Register (Address = 02h) [reset = 00h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	OLA1	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT1
6	OLA2	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT2
5	ITRIP_CMP	R	0b	1b indicates that load current has reached the ITRIP regulation level.

Bit	Field	Type	Reset	Description
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state
3	OCP_H1	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT1
2	OCP_L1	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT1
1	OCP_H2	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT2
0	OCP_L2	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT2

8.6.1.4 STATUS2 Register (Address = 03h) [reset = 80h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	DRVOFF_STAT	R	1b	This bit shows the status of the DRVOFF pin. 1b implies the pin status is high.
6, 5	N/A	R	0b	Not available
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state (Copy of bit4 in STATUS1)
3, 2, 1	N/A	R	0b	Not available
0	OLP_CMP	R	0b	This bit is the output of the off-state diagnostics (OLP) comparator.

8.6.1.5 COMMAND Register (Address = 08h) [reset = 09h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	CLR_FLT	R/W	0b	Clear Fault command - Write 1b to clear all faults reported in the fault registers and de-assert the nFAULT pin
6-5	N/A	R	0b	Not available
4-3	SPI_IN_LOCK	R/W	01b	Write 10b to **unlock** the SPI_IN register Write 01b or 00b or 11b to **lock** the SPI_IN register SPI_IN register is **locked** by default.
2	N/A	R	0b	Not available
1-0	REG_LOCK	R/W	01b	Write 10b to **lock** the CONFIG registers Write 01b or 00b or 11b to **unlock** the CONFIG registers CONFIG registers are **unlocked** by default.

8.6.1.6 SPI_IN Register (Address = 09h) [reset = 0Ch]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-4	N/A	R	0b	Not available
3	S_DRVOFF	R/W	1b	Register bit equivalent of DRVOFF pin when SPI_IN is unlocked. Refer Register Pin control section. In Independent mode, this bit shuts off half-bridge 1.
2	S_DRVOFF2	R/W	1b	Register bit to shut off half-bridge 2 in Independent mode when SPI_IN is unlocked. Refer Register Pin control section
1	S_EN_IN1	R/W	0b	Register bit equivalent of EN/IN1 pin when SPI_IN is unlocked. Refer Register Pin control section
0	S_PH_IN2	R/W	0b	Register bit equivalent of PH/IN2 pin when SPI_IN is unlocked. Refer Register Pin control section

8.6.1.7 CONFIG1 Register (Address = 0Ah) [reset = 10h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	EN_OLA	R/W	0b	Write 1b to enable open load detection in the active state. In Independent mode, OLA is always disabled for low-side load. Refer DIAG section.
6-5	VMOV_SEL	R/W	0b	Determines the thresholds for the VM over voltage diagnostics 00b = VM > 35 V 01b = VM > 28 V 10b = VM > 18 V 11b = VMOV disabled
4	SSC_DIS	R/W	1b	0b: Enables the spread spectrum clocking feature
3	OCP_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over current, else the fault reaction is latched
2	TSD_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over temperature, else the fault reaction is latched
1	VMOV_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of VMOV, else the fault reaction is latched. **Note** For the SPI (P) variant, this bit also controls the fault reaction for a VM under voltage detection.

Bit	Field	Type	Reset	Description
0	OLA_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of open load during active, else the fault reaction is latched.

8.6.1.8 CONFIG2 Register (Address = 0Bh) [reset = 00h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	PWM_EXTEND	R/W	0b	Write 1b to access additional Hi-Z (coast) states in the PWM mode - refer PWM EXTEND table
6-5	S_DIAG	R/W	0b	Load type indication - refer to DIAG table
4-3	N/A	R	0b	Not available
2-0	S_ITRIP	R/W	0b	ITRIP level configuration - refer ITRIP table

8.6.1.9 CONFIG3 Register (Address = 0Ch) [reset = 40h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-6	TOFF	R/W	1b	TOFF time used for ITRIP current regulation 00b = 20 µsec 01b = 30 µsec 10b = 40 µsec 11b = 50 µsec
5	N/A	R	0b	Not available
4-2	S_SR	R/W	0b	Slew Rate configuration - refer to Section 8.3.3.1
1-0	S_MODE	R/W	0b	Device mode configuration - refer MODE table

8.6.1.10 CONFIG4 Register (Address = 0Dh) [reset = 04h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-6	TOCP_SEL	R/W	0b	Filter time for over current detection configuration 00b = 6 µsec 01b = 3 µsec 10b = 1.5 µsec 11b = Minimum (~0.2 µsec)
5	N/A	R	0b	Not available
4-3	OCP_SEL	R/W	0b	Threshold for over current detection configuration 00b = 100% setting 01b, 11b = 50% setting 10b = 75% setting
2	DRVOFF_SEL	R/W	1b	DRVOFF pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND
1	EN_IN1_SEL	R/W	0b	EN/IN1 pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND
0	PH_IN2_SEL	R/W	0b	PH/IN2 pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV824x-Q1 family of devices can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver and dual unidirectional current control applications requiring two half-bridge drivers.

9.1.1 Load Summary

Table 9-1 summarizes the utility of the device features for different type of inductive loads.

Table 9-1. Load Summary Table

LOAD TYPE	Configuration		Device Feature		
	Device	Recirculation Path	Slew Rate	Current sense	ITRIP regulation
Bi-directional motor or solenoid(1)	DRV824x in PH/EN or PWM mode	High-side	Full range	Continuous	Useful
2 Uni-directional motors or low-side solenoids (one side connected to GND)	DRV824x in Independent mode (2)	Low-side	Limited(4)	Discontinuous(3),	Individual load regulation not possible
2 High-side solenoids (one side connected to VM)	DRV824x in Independent mode (2)	High-side	Full range	Not available, need external solution	

(1) Solenoid - clamping or quick demagnetization possible, but clamping level will be VM dependent
(2) Independent Hi-Z only supported in the SPI variant
(3) Not sensed during recirculation and during OUTx voltage slew times including t_{blank}
(4) Rising edge slew rate capped at 8 V/µsec for higher settings

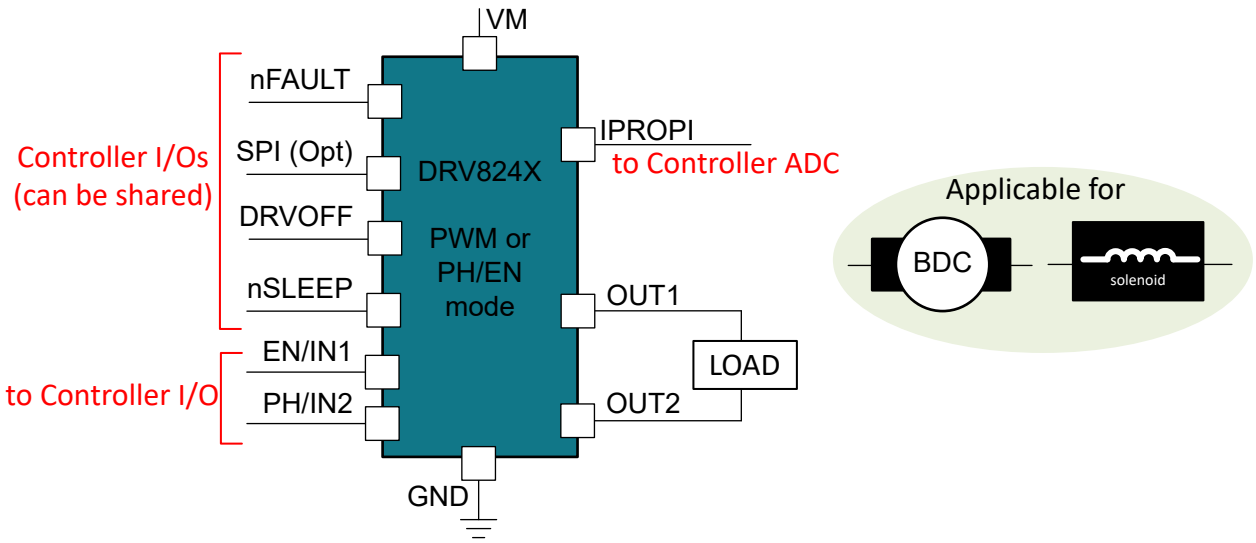


Figure 9-1. Illustration Showing a Full-Bridge Topology With DRV824X-Q1 in PWM or PH/EN Mode

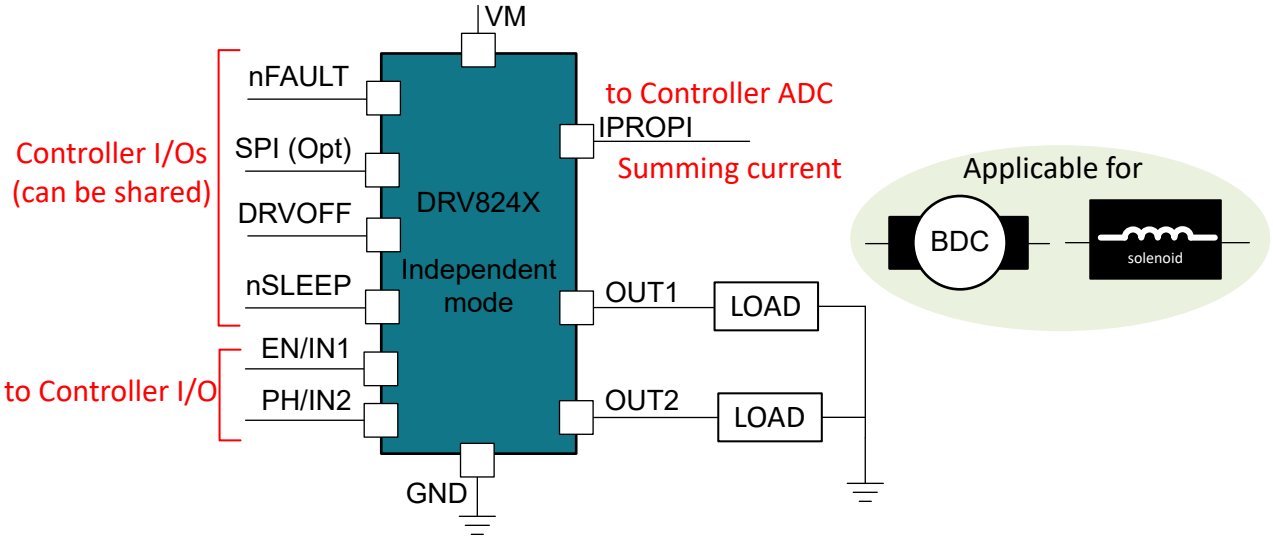


Figure 9-2. Illustration Showing Half-Bridge Topology to Drive Two Low-side Loads Independently With DRV824X-Q1 Device in INDEPENDENT Mode

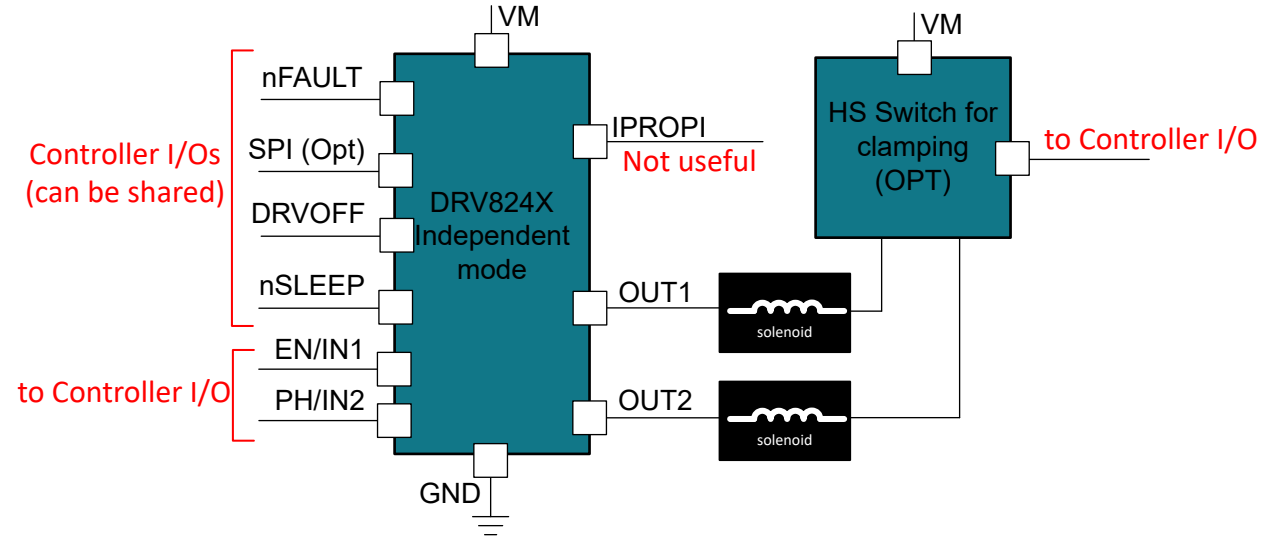


Figure 9-3. Illustration Showing a Half-Bridge Topology to Drive Two High-side Loads Independently With DRV824X-Q1 Device in INDEPENDENT Mode

9.2 Typical Application

The figures below show the typical application schematic for driving a brushed DC motor or any inductive load in various modes. There are several optional connections shown in these schematics, which are listed as follows:

- nSLEEP pin
  - SPI (S) variant - This pin can be tied off high in the application if SLEEP function is not needed.
  - SPI (P) variant - N/A
  - HW (H) variant - Pin control is **mandatory** even if SLEEP function is not needed. The controller needs to issue a reset pulse during wake-up to acknowledge wake-up or power-up.
- DRVOFF pin
  - Both SPI (P) and SPI (S) variants - This pin can be tied off low in the application if shutoff through **pin** function is not needed. The equivalent register bit can be used.
- EN/IN1 pin

  - Both SPI (P) and SPI (S) variants - This pin can be tied off low or left floating if register only control is needed.
- PH/IN2 pin
  - Both SPI (P) and SPI (S) variants - This pin can be tied off low or left floating if register only control is needed.
- IPROPI pin
  - All variants - Monitoring of this output is optional. Also IPROPI pin can be tied low if ITRIP feature & IPROPI function is not needed.
- nFAULT pin
  - Both SPI (P) and SPI (S) variants - Monitoring of this output is optional. All diagnostic information can be read from the STATUS registers.
- SPI input pins
  - Both SPI (S) and SPI (P) variants - Inputs (SDI, nSCS, SCLK) are compatible with 3.3 V / 5 V levels.
- SPI SDO pin
  - SPI (S) variant - SDO tracks the nSLEEP pin voltage.
  - SPI (P) variant - SDO tracks the VDD pin voltage. To interface with a 3.3 V level controller input, a level shifter or a current limiting series resistor is recommended.
- CONFIG pins
  - HW (H) variant - Resistor is not needed for short to GND and Hi-Z level selections
    - LVL1 and LVL3 for MODE pin
    - LVL1 and LVL6 for SR, ITRIP, DIAG pins

9.2.1 HW Variant

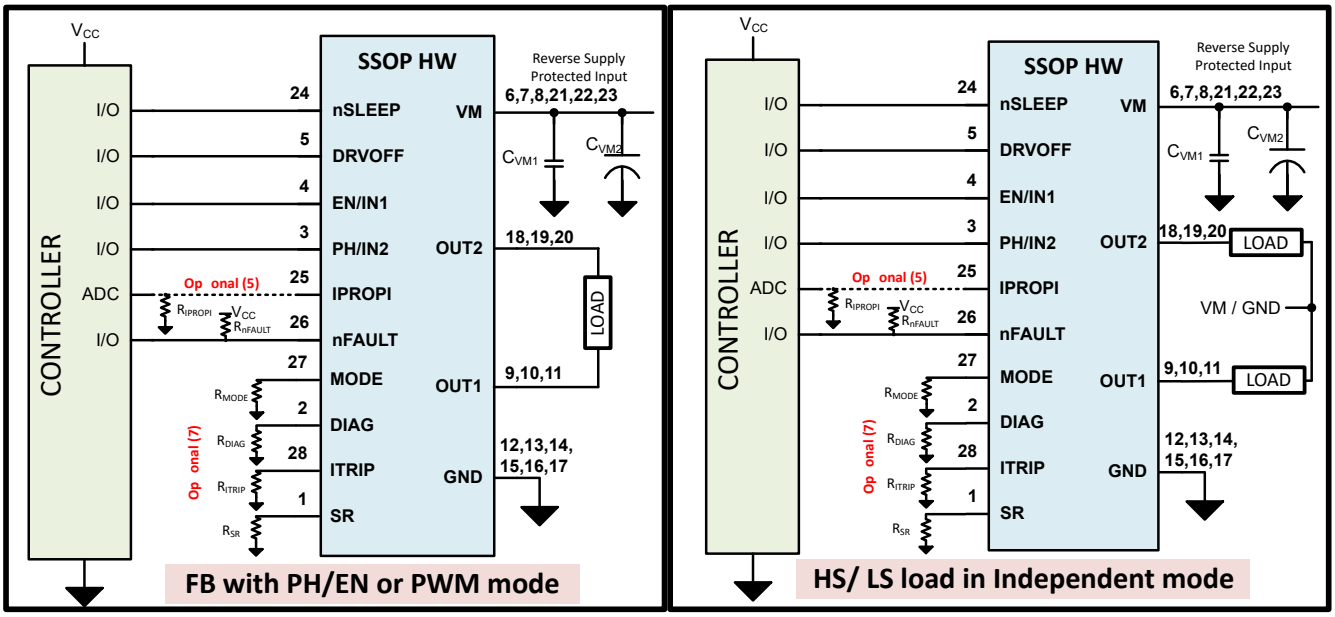


Figure 9-4. Typical Application Schematic - HW Variant in HVSSOP Package

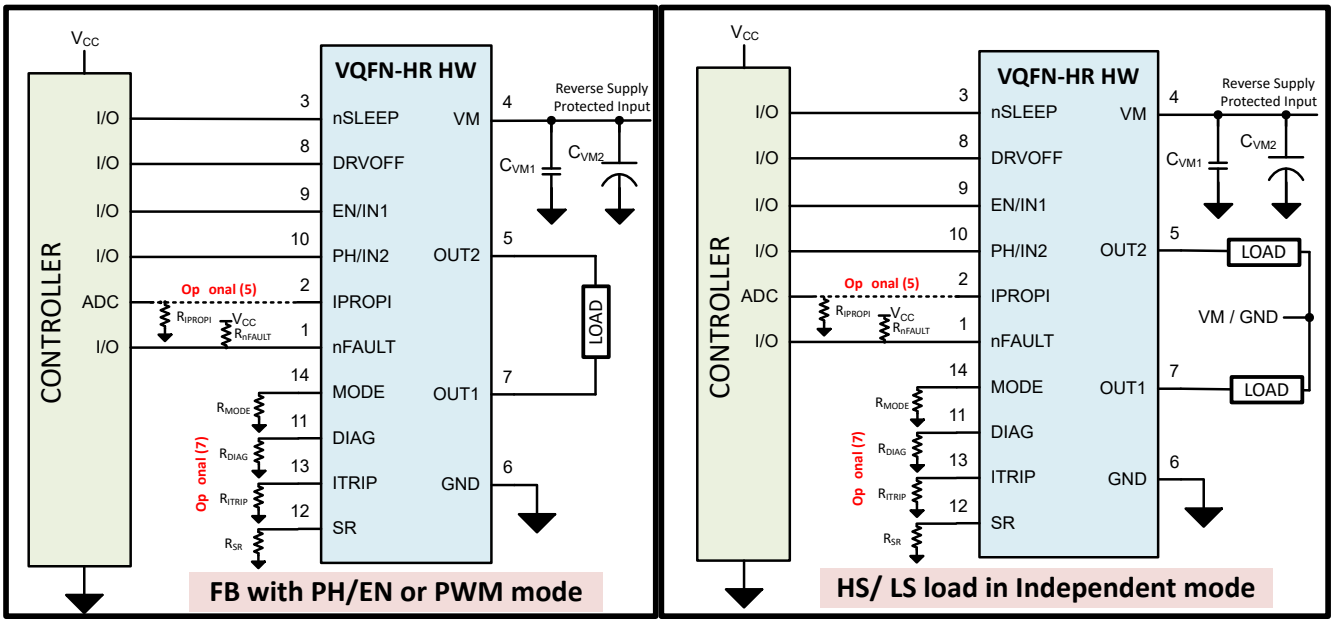


Figure 9-5. Typical Application Schematic - HW Variant in VQFN-HR Package

9.2.2 SPI Variant

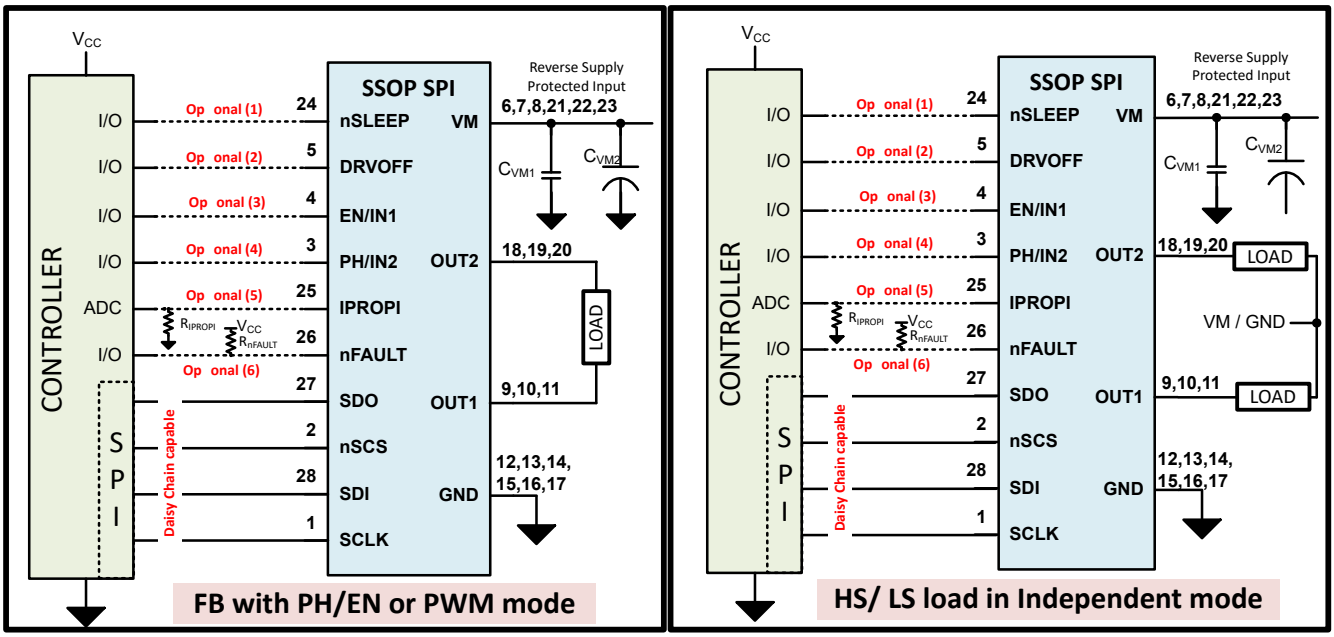


Figure 9-6. Typical Application Schematic - SPI (S) Variant in HVSSOP Package

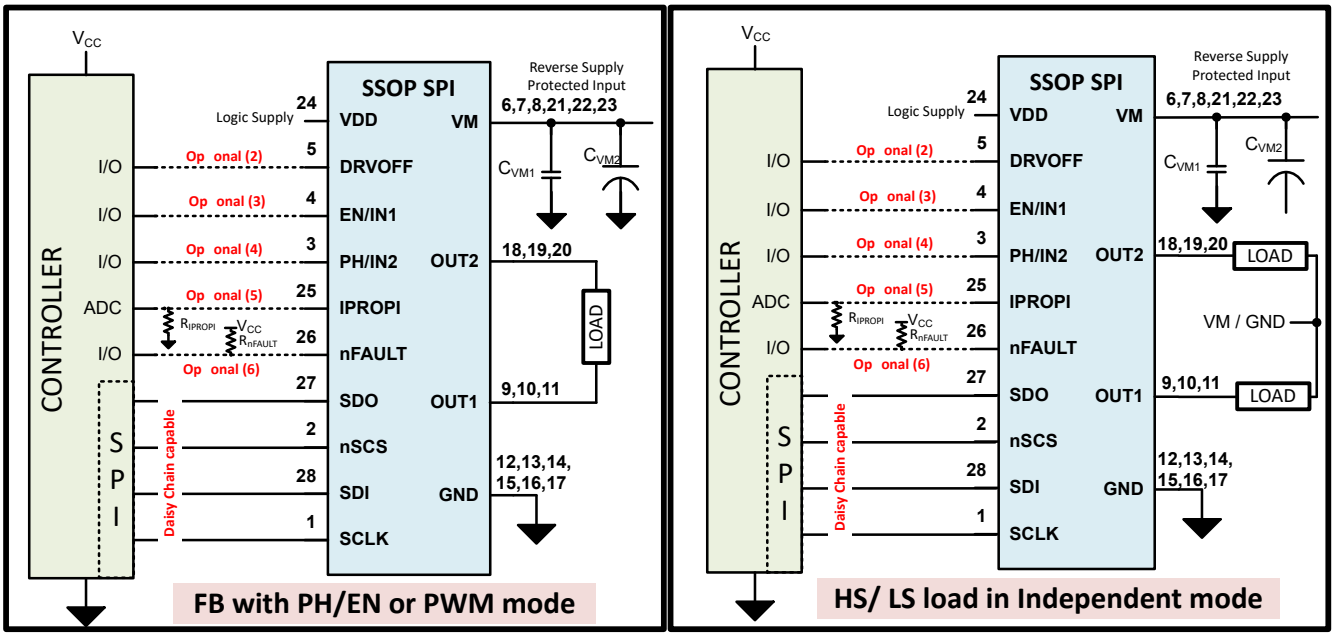


Figure 9-7. Typical Application Schematic - SPI (P) Variant in HVSSOP Package

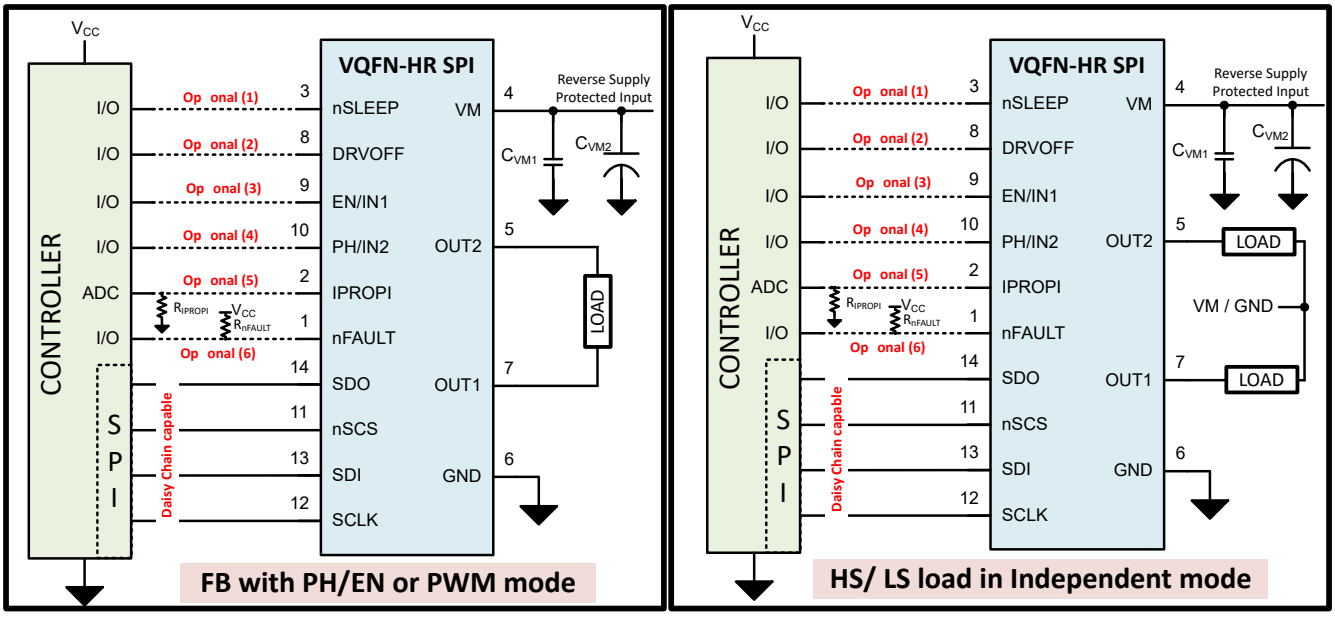


Figure 9-8. Typical Application Schematic - SPI (S) Variant in VQFN-HR Package

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply (VM) range from 4.5 V to 40 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. Also, an appropriately sized bulk capacitor must be placed on the VM pin.

10.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

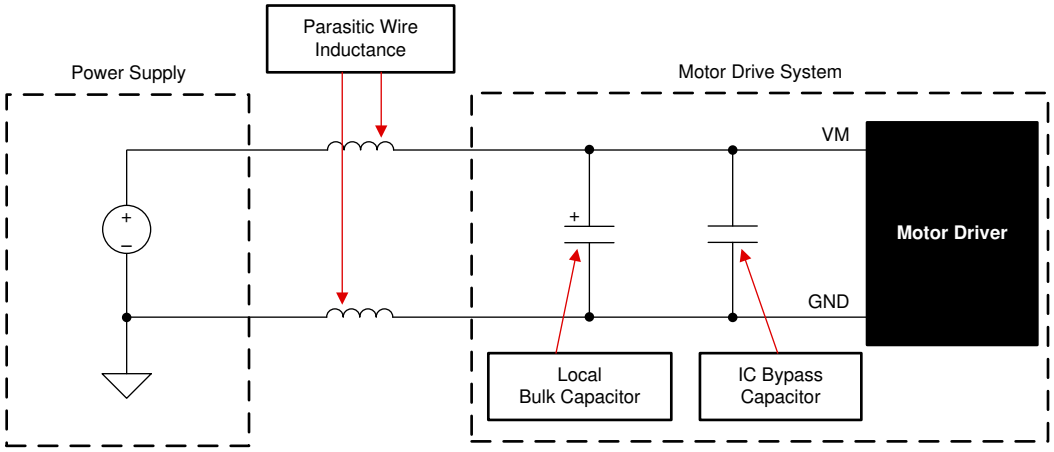


Figure 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

Each VM pin must be bypassed to ground using low-ESR ceramic bypass capacitors with recommended values of 0.1 µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

For the SPI (P) device variant, VDD pin may be bypassed to ground using low-ESR ceramic 6.3 V bypass capacitor with recommended values of 0.1 µF.

11.2 Layout Example

The following figure shows a layout example for a 4 cm X 4 cm x 1.6 mm, 4 layer PCB for a leaded package device. The 4 layers uses 2 oz copper on top/ bottom signal layers and 1 oz copper on internal supply layers, with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 mm minimum via pitch. The same layout can be adopted for the non-leaded VQFN-HR package as well. The Section 7.5.14 for the 4 cm X 4 cm X 1.6 mm is based on a similar layout.

Note: The layout example shown is for a full bridge topology using DRV824xQ1 device in SSOP package.

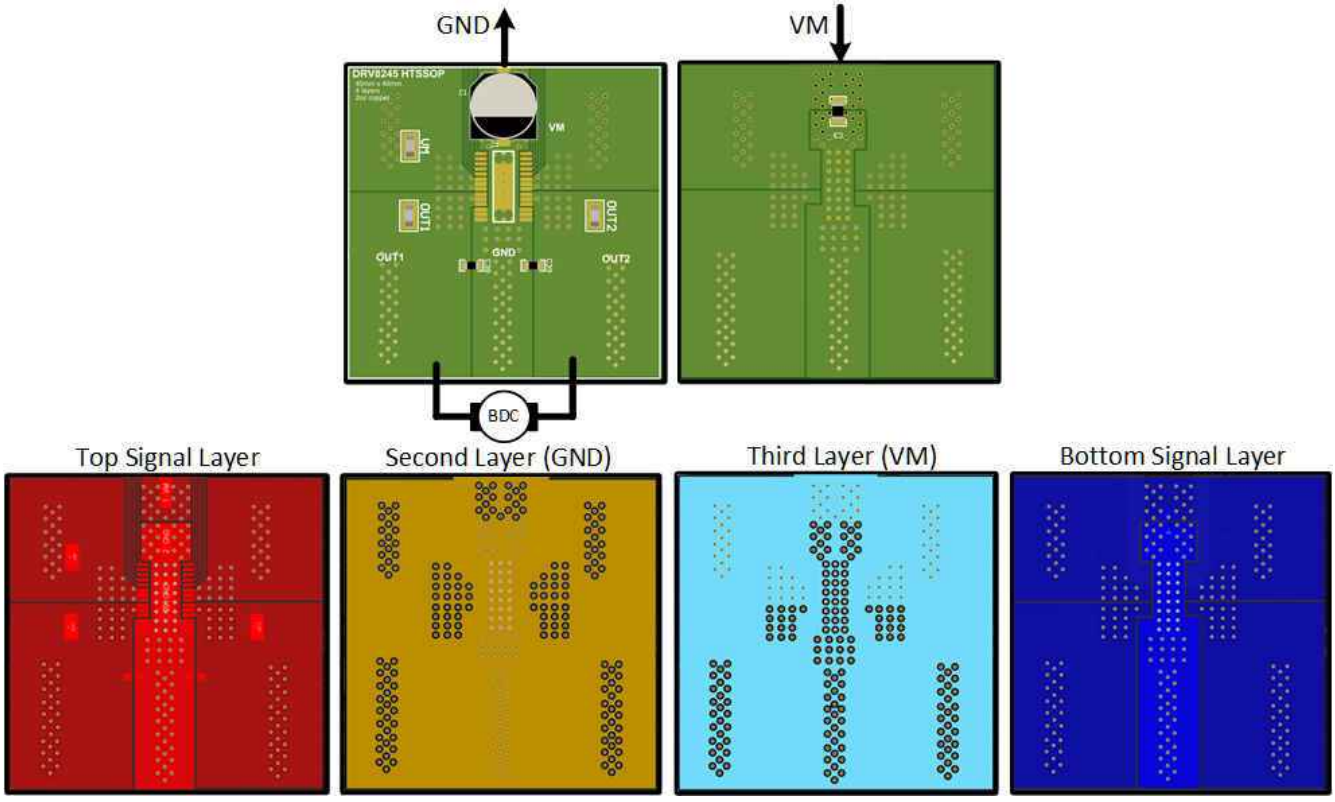


Figure 11-1. Layout example: 4cm x 4 cm x 1.6mm, 4 layer PCB

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Full Bridge Driver Junction Temperature Estimator (Excel-based worksheet)*
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

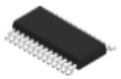
All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and order-able information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

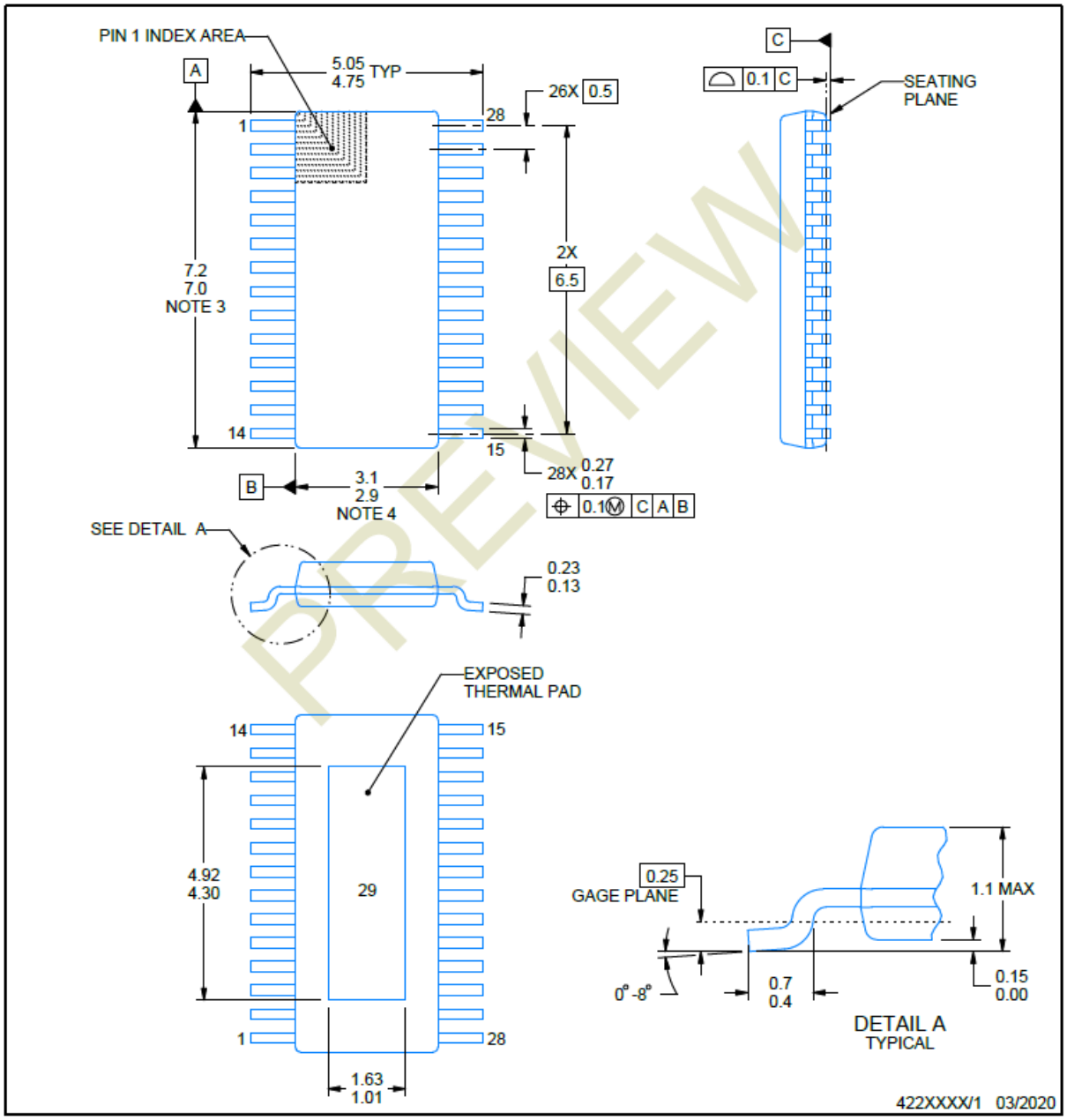
PACKAGE OUTLINE

DGQ0028A



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

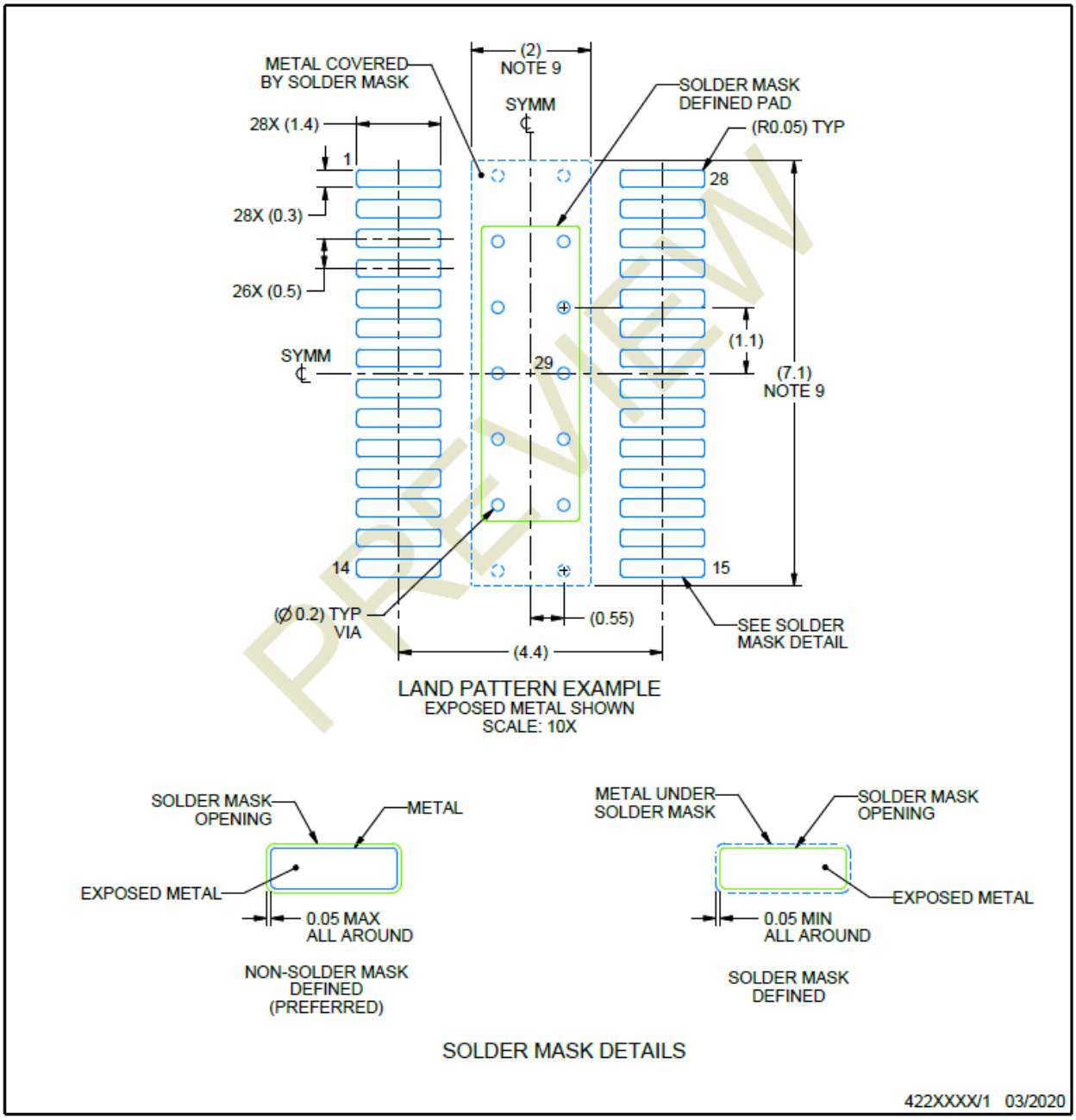
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. No JEDEC registration as of March 2020.

EXAMPLE BOARD LAYOUT

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



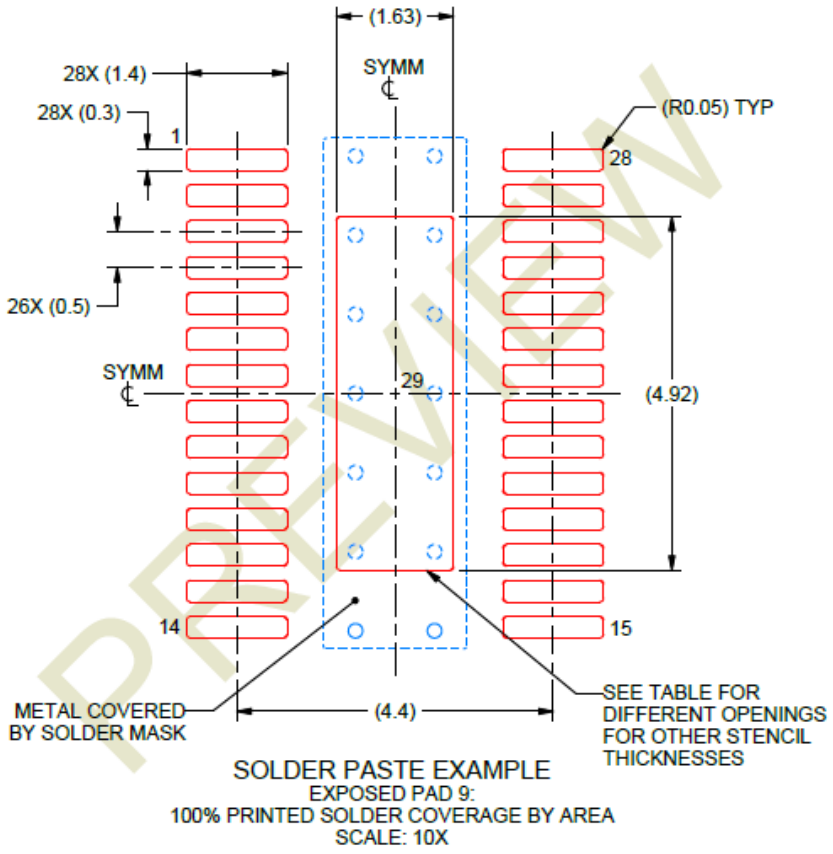
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGQ0028A — **PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.82 X 5.50
0.125	1.63 X 4.92 (SHOWN)
0.15	1.49 X 4.49
0.175	1.38 X 4.16

422XXXX/1 03/2020

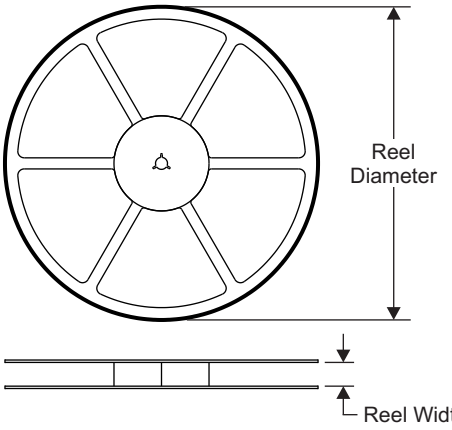
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

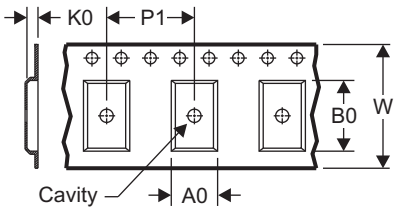
Figure 13-1. DGQ28A: HVSSOP(28) Package Drawing

13.1 Tape and Reel Information

REEL DIMENSIONS

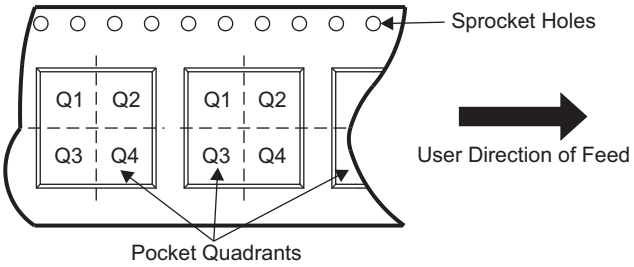


TAPE DIMENSIONS



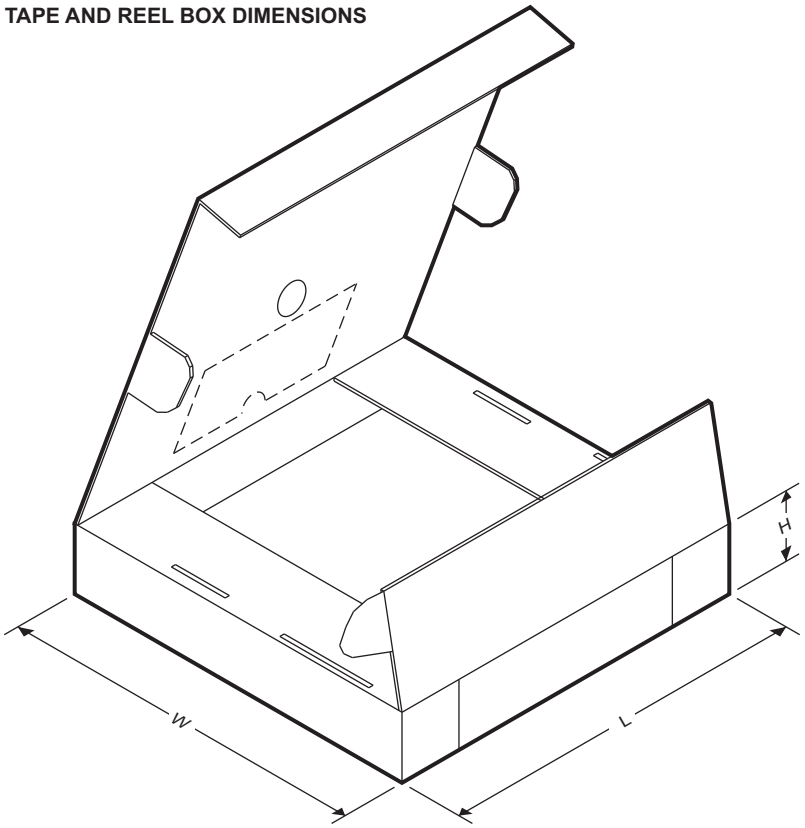
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDRV8243SDGQQ1	HVSSOP	DGQ	28	3000	330	16.4	5.50	7.40	1.45	8.00	16.00	Q1
PDRV8243PDGQQ1	HVSSOP	DGQ	28	3000	330	16.4	5.50	7.40	1.45	8.00	16.00	Q1
PDRV8243HDGQQ1	HVSSOP	DGQ	28	3000	330	16.4	5.50	7.40	1.45	8.00	16.00	Q1
PDRV8243SRXYQ1	VQFN-HR	RXY	14	5000	180	12.4	2.45	2.75	1.2	4	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDRV8243SDGQQ1	HVSSOP	DGQ	28	3000	356	356	35
PDRV8243PDGQQ1	HVSSOP	DGQ	28	3000	356	356	35
PDRV8243HDGQQ1	HVSSOP	DGQ	28	3000	356	356	35
PDRV8243SRXYQ1	VQFN-HR	RXY	14	5000	210	185	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8243HQRXYRQ1	ACTIVE	VQFN-HR	RXY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8243H	Samples
PDRV8243SDGQQ1	ACTIVE	HVSSOP	DGQ	28	1	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

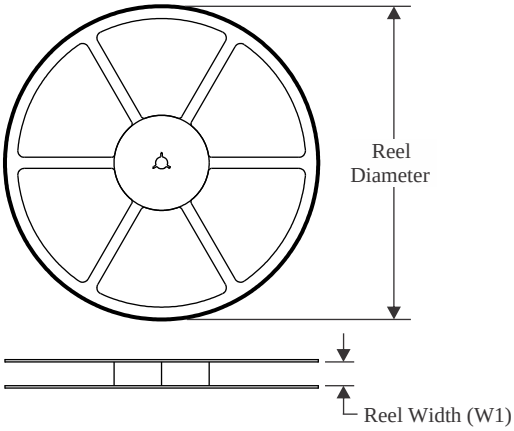
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

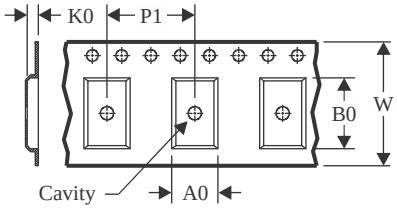
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

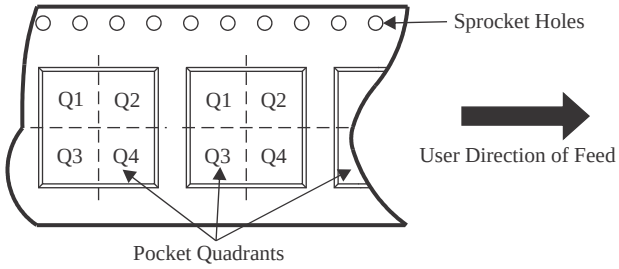


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

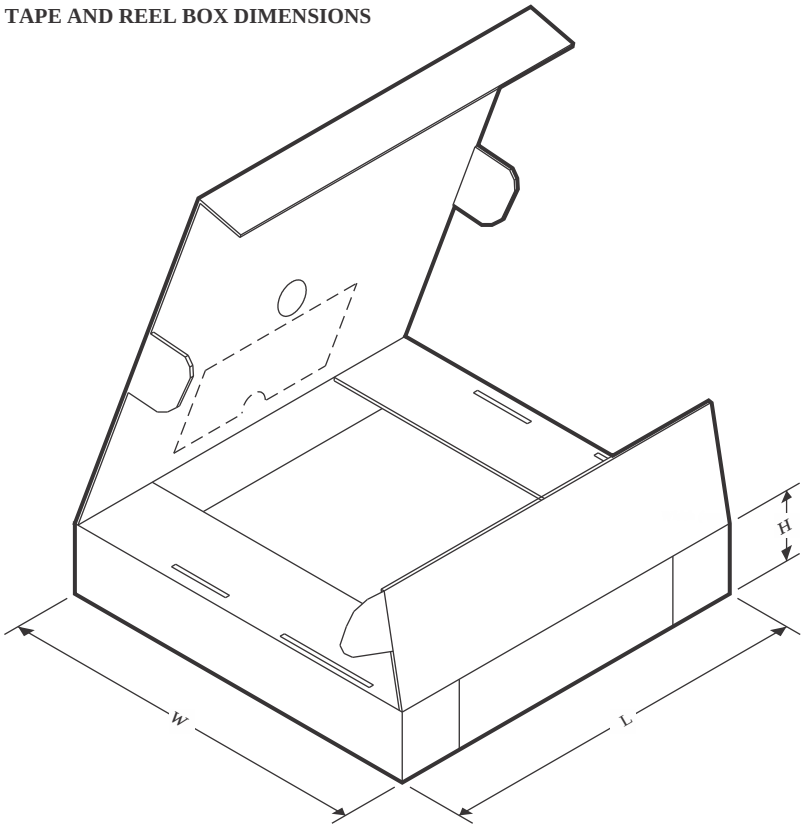
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8243HQRXYRQ1	VQFN-HR	RXY	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

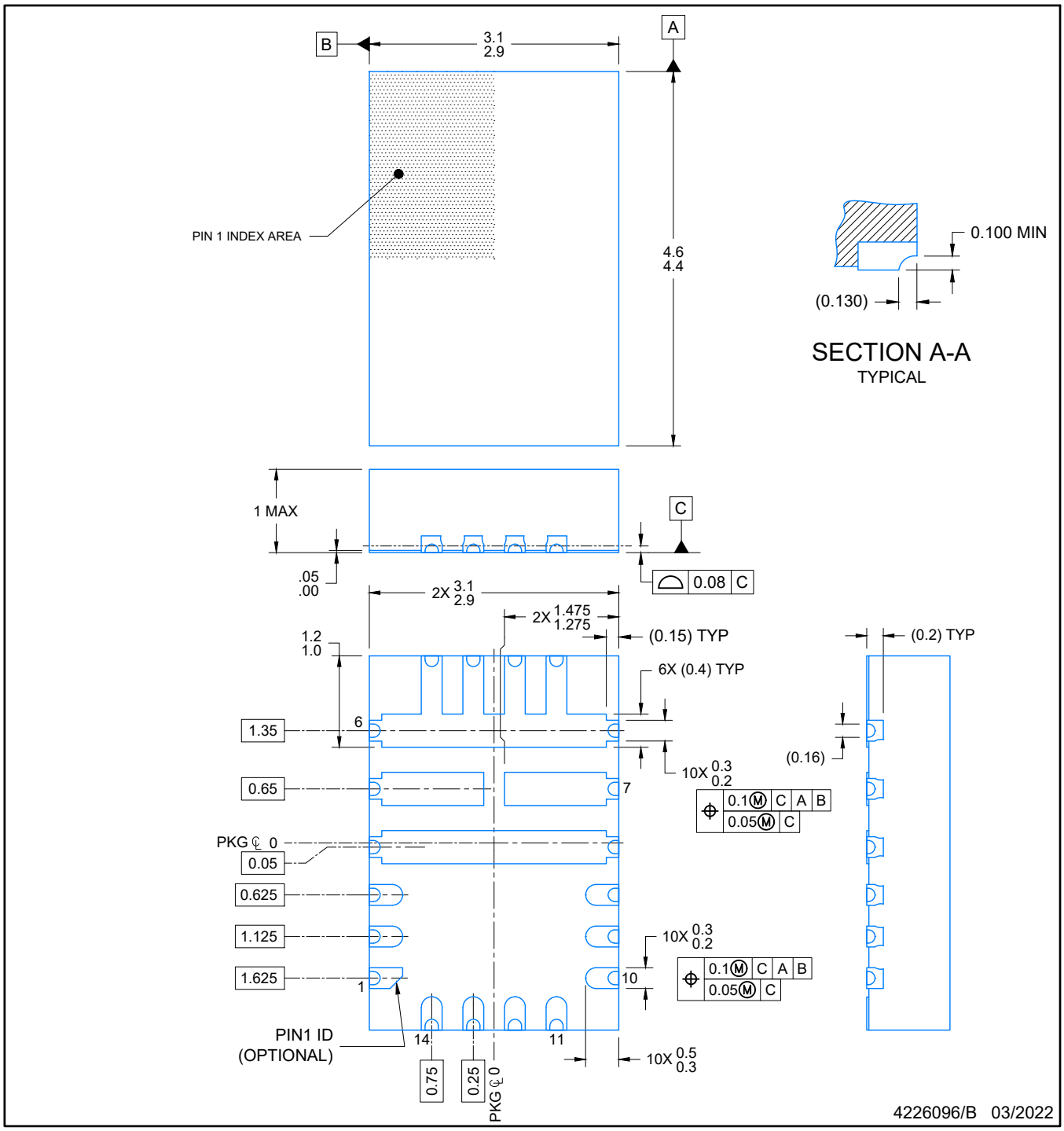
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8243HQRXYRQ1	VQFN-HR	RXY	14	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RXY0014A

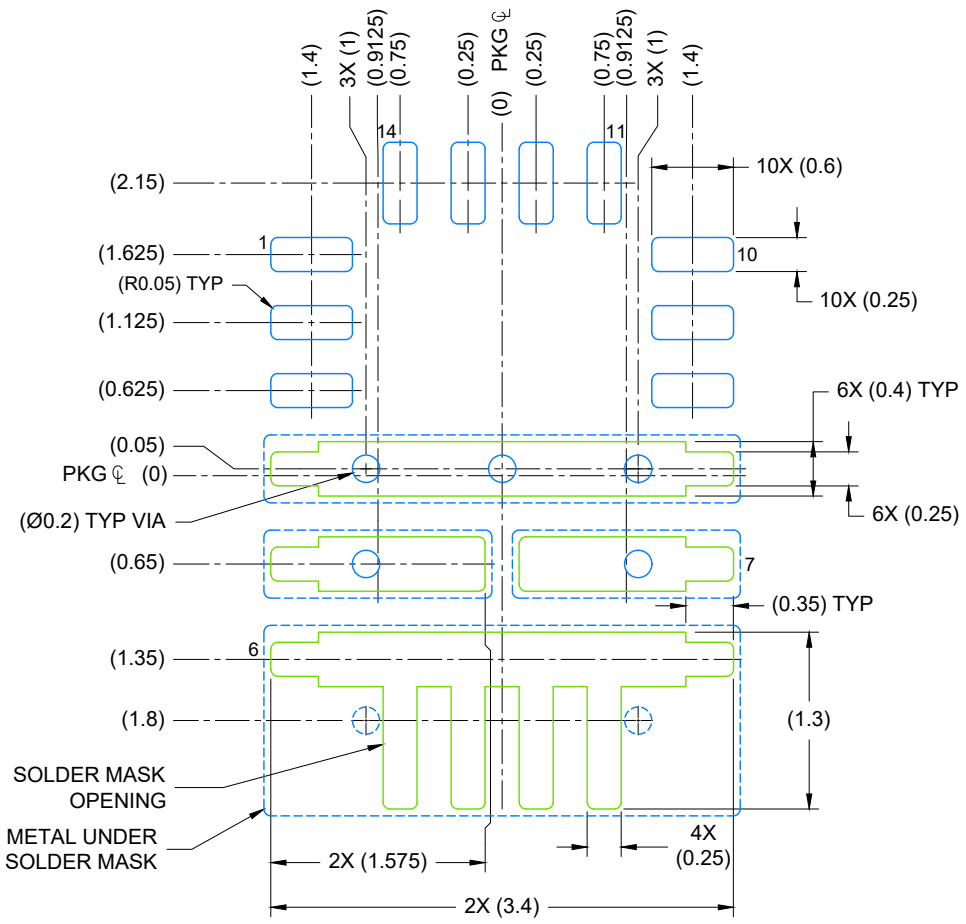
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

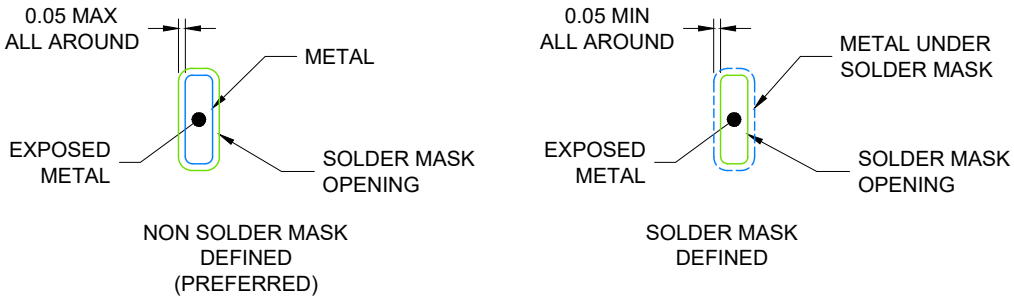
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X

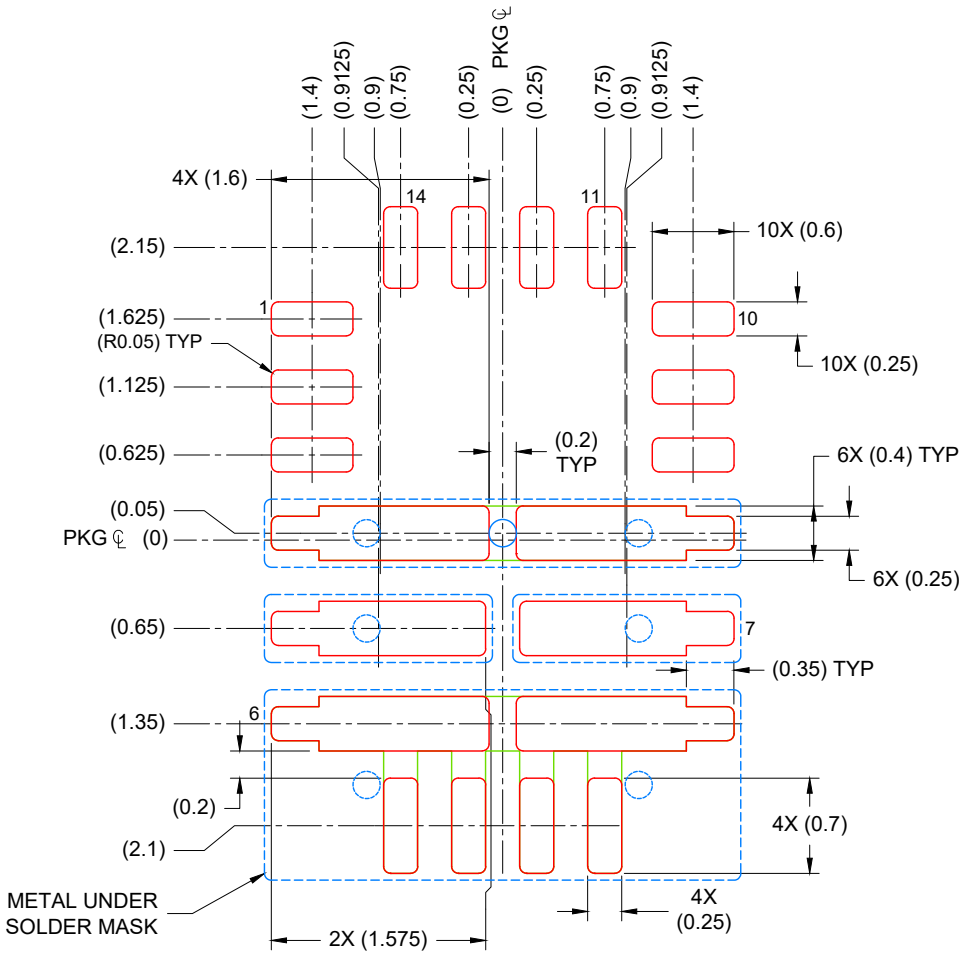


SOLDER MASK DETAILS

4226096/B 03/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 18X

4226096/B 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

DRV8300U: 100-V Three-Phase BLDC Gate Driver

1 Features

- 100-V Three Phase Half-Bridge Gate driver
  - Drives N-Channel MOSFETs (NMOS)
  - Gate Driver Supply (GVDD): 5-20 V
  - MOSFET supply (SHx) support upto 100 V
- Integrated Bootstrap Diodes (DRV8300UD devices)
- Supports Inverting and Non-Inverting INLx inputs
- Bootstrap gate drive architecture
  - 750-mA source current
  - 1.5-A sink current
- Supports up to 15S battery powered applications
- Higher BSTUV (8V typ) and GVDDUV (7.6V typ) threshold to support standard MOSFETs
- Low leakage current on SHx pins (<55 µA)
- Absolute maximum BSTx voltage upto 125-V
- Supports negative transients upto -22-V on SHx
- Built-in cross conduction prevention
- Adjustable deadtime through DT pin for QFN package variants
- Fixed deadtime insertion of 200 nS for TSSOP package variants
- Supports 3.3-V and 5-V logic inputs with 20 V Abs max
- 4 nS typical propogation delay matching
- Compact QFN and TSSOP packages
- Efficient system design with Power Blocks
- Integrated protection features
  - BST undervoltage lockout (BSTUV)
  - GVDD undervoltage (GVDDUV)

2 Applications

- E-Bikes, E-Scooters, and E-Mobility
- Fans, Pumps, and Servo Drives
- Brushless-DC (BLDC) Motor Modules and PMSM
- Cordless Garden and Power Tools, Lawnmowers
- Cordless Vacuum Cleaners
- Drones, Robotics, and RC Toys
- Industrial and Logistics Robots

3 Description

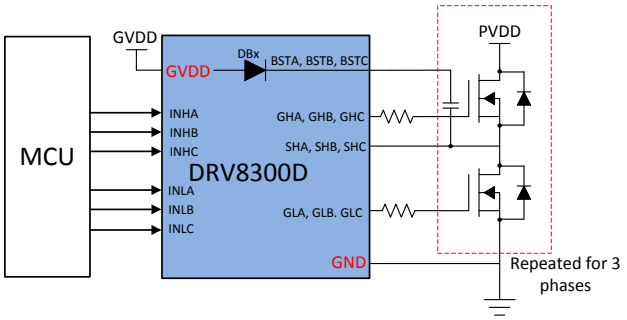
DRV8300U is 100-V three half-bridge gate drivers, capable of driving high-side and low-side N-channel power MOSFETs. The DRV8300UD generates the correct gate drive voltages using an integrated bootstrap diode and external capacitor for the high-side MOSFETs. GVDD is used to generate gate drive voltage for the low-side MOSFETs. The Gate Drive architecture supports peak up to 750-mA source and 1.5-A sink currents.

The phase pins SHx is able to tolerate the significant negative voltage transients; while high side gate driver supply BSTx and GHx is able to support to higher positive voltage transients (125-V) abs max voltage which improves robustness of the system. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency. Undervoltage protection is provided for both low and high side through GVDD and BST undervoltage lockout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8300UDPW	TSSOP (20)	6.40 mm × 4.40 mm
DRV8300UDIPW(2)	TSSOP (20)	6.40 mm × 4.40 mm
DRV8300UDRGE(2)	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Device available for preview only



Simplified Schematic for DRV8300UD

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2022	*	Initial Release

5 Device Comparison Table

Device Variants	Package	Integrated Bootstrap Diode	GLx polarity with respect to INLx Input	Deadtime
DRV8300UD	20-Pin TSSOP	Yes	Inverted	Fixed
DRV8300UDI(1)		Yes	Non-Inverted	Fixed
DRV8300UD(1)	24-Pin VQFN	Yes	Non-Inverted or Inverted	Variable

(1) Device available for preview only

Table 5-1. DRV8300 vs DRV8300U comparison

Parameters	DRV8300	DRV8300U
GVDDUV rising	4.6-V (typ)	8.3-V (typ)
GVDDUV falling	4.35-V (typ)	8-V (typ)
BSTUV rising	4.2-V (typ)	8-V (typ)
BSTUV falling	4-V (typ)	7.6-V(typ)

6 Pin Configuration and Functions

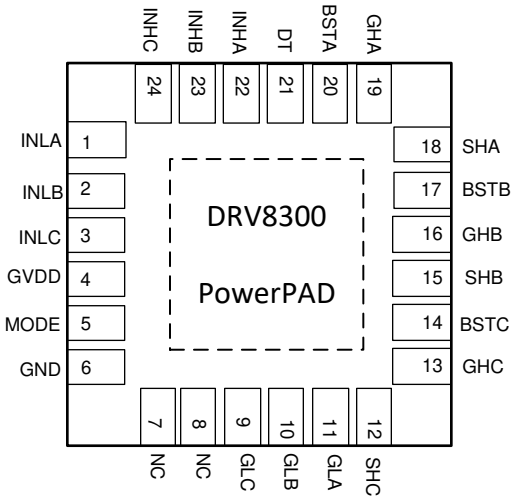


Figure 6-1. DRV8300UD RGE Package 24-Pin VQFN With Exposed Thermal Pad Top View

Table 6-1. Pin Functions—24-Pin DRV8300U Devices

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
DT	21	I	Deadtime input pin. Connect resistor to ground for variable deadtime, fixed deadtime when left it floating
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	22	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	23	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	24	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	1	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	2	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	3	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	5	I	Mode Input controls polarity of GLx compared to INLx inputs. Mode pin floating: GLx output polarity same(Non-Inverted) as INLx input Mode pin to GVDD: GLx output polarity inverted compared to INLx input
NC	7, 8	NC	No internal connection. This pin can be left floating or connected to system ground.
GND	6	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	4	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

(1) PWR = power, I = input, O = output, NC = no connection

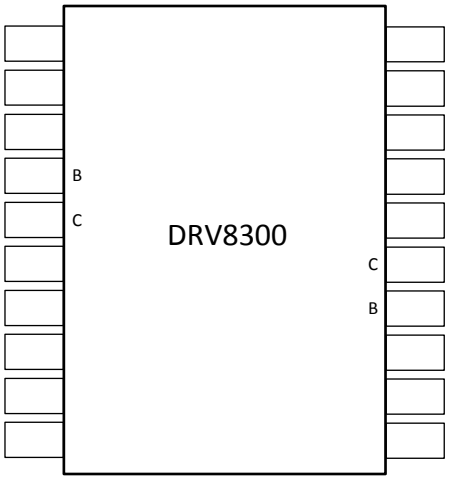


Figure 6-2. DRV8300UD, DRV8300UDI PW Package 20-Pin TSSOP Top View

Table 6-2. Pin Functions—20-Pin DRV8300U Devices

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	1	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	2	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	3	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	4	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	5	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	6	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
GND	8	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	7	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

1. PWR = power, I = input, O = output, NC = no connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	21.5	V
Bootstrap pin voltage	BSTx	-0.3	125	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	21.5	V
Logic pin voltage	INHx, INLx, MODE, DT	-0.3	V_{GVDD}+0.3	V
High-side gate drive pin voltage	GHx	-22	125	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	22	V
Transient 500-ns high-side gate drive pin voltage	GHx with respect to SHx	-5	22	V
Low-side gate drive pin voltage	GLx	-0.3	V_{GVDD}+0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx	-5	V_{GVDD}+0.3	V
High-side source pin voltage	SHx	-22	110	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	8.7		20	V
V_{SHx}	High-side source pin voltage	SHx	-2		85	V
V_{SHx}	Transient 2µs high-side source pin voltage	SHx	-22		85	V
V_{BST}	Bootstrap pin voltage	BSTx	5		105	V
V_{BST}	Bootstrap pin voltage	BSTx with respect to SHx	5		20	V
V_{IN}	Logic input voltage	INHx, INLx, MODE, DT	0		GVDD	V
f_{PWM}	PWM frequency	INHx, INLx	0		200	kHz
V_{SHSL}	Slew rate on SHx pin (DRV8300UD and DRV8300UDI)				2	V/ns
C_{BOOT} (1)	Capacitor between BSTx and SHx (DRV8300UD and DRV8300UDI)				1	µF
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Current flowing through boot diode (D_{BOOT}) needs to be limited for C_{BOOT} > 1µF

7.4 Thermal Information

THERMAL METRIC(1)		DRV8300U		UNIT
		PW (TSSOP)	RGE (VQFN)	
		20 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.4	49.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	26.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.4	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, BSTx)						
I_{GVDD}	GVDD standby mode current	INHx = INLX = 0; V_{BSTx} = V_{GVDD}	400	800	1400	µA
	GVDD active mode current	INHx = INLX = Switching @20kHz; V_{BSTx} = V_{GVDD}; NO FETs connected	400	825	1400	µA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 85V; V_{GVDD} = 0V	2	4	7	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	INHx = Switching@20kHz	30	105	220	µA
IL_{BS_DC}	Bootstrap pin active mode leakage static current	INHx = High	30	85	150	µA
IL_{SHx}	High-side source pin leakage current	INHx = INLX = 0; V_{BSTx} - V_{SHx} = 12V; V_{SHx} = 0 to 85V	30	55	80	µA
LOGIC-LEVEL INPUTS (INHx, INLx, MODE)						
V_{IL_MODE}	Input logic low voltage	Mode pin			0.6	V
V_{IL}	Input logic low voltage	INLx, INHx pins			0.8	V
V_{IH_MODE}	Input logic high voltage	Mode pin	3.7			V
V_{IH}	Input logic high voltage	INLx, INHx pins	2.0			V
V_{HYS_MODE}	Input hysteresis	Mode pin	1600	2000	2400	mV
V_{HYS}	Input hysteresis	INLx, INHx pins	40	100	260	mV
I_{IL_INLx}	INLx Input logic low current	V_{PIN} (Pin Voltage) = 0 V; INLx in non-inverting mode	-1	0	1	µA
		V_{PIN} (Pin Voltage) = 0 V; INLx in inverting mode	5	20	30	µA
I_{IH_INLx}	INLx Input logic high current	V_{PIN} (Pin Voltage) = 5 V; INLx in non-inverting mode	5	20	30	µA
		V_{PIN} (Pin Voltage) = 5 V; INLx in inverting mode	0	0.5	1.5	µA
I_{IL}	INHx, MODE Input logic low current	V_{PIN} (Pin Voltage) = 0 V;	-1	0	1	µA
I_{IH}	INHx, MODE Input logic high current	V_{PIN} (Pin Voltage) = 5 V;	5	20	30	µA
R_{PD_INHx}	INHx Input pulldown resistance	To GND	120	200	280	kΩ
R_{PD_INLx}	INLx Input pulldown resistance	To GND, INLx in non-inverting mode	120	200	280	kΩ
R_{PU_INLx}	INLx Input pullup resistance	To INT_5V, INLx in inverting mode	120	200	280	kΩ
R_{PD_MODE}	MODE Input pulldown resistance	To GND	120	200	280	kΩ
GATE DRIVERS (GHx, GLx, SHx, SLx)						

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GHx_LO}	High-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
V_{GLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
I_{DRIVEP_HS}	High-side peak source gate current	GHx-SHx = 12V	400	750	1200	mA
I_{DRIVEN_HS}	High-side peak sink gate current	GHx-SHx = 0V	850	1500	2100	mA
I_{DRIVEP_LS}	Low-side peak source gate current	GLx = 12V	400	750	1200	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	GLx = 0V	850	1500	2100	mA
t_{PD}	Input to output propagation delay	INHx, INLx to GHx, GLx; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	70	125	180	ns
t_{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{PD_match}	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t_{R_GLx}	GLx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{R_GHx}	GHx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{F_GLx}	GLx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{F_GHx}	GHx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{DEAD}	Gate drive dead time	DT pin floating	150	215	280	ns
		DT pin connected to GND	150	215	280	ns
		40 kΩ between DT pin and GND	150	200	260	ns
		400 kΩ between DT pin and GND	1500	2000	2600	ns
t_{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		40	70	150	ns
BOOTSTRAP DIODES(DRV8300UD, DRV8300UDI)						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA	0.45	0.7	0.85	V
		I_{BOOT} = 100 mA	2	2.3	3.1	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 80 mA	11	15	25	Ω
PROTECTION CIRCUITS						
V_{GVDDUV}	Gate Driver Supply undervoltage lockout (GVDDUV)	Supply rising	8	8.3	8.6	V
		Supply falling	7.8	8	8.25	V
V_{GVDDUV_HYS}	Gate Driver Supply UV hysteresis	Rising to falling threshold	295	330	360	mV
t_{GVDDUV}	Gate Driver Supply undervoltage deglitch time		5	10	13	µs

8.7 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BSTUV}	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply rising	7.5	8	8.7	V
	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply falling	6.9	7.6	8.4	V
V_{BSTUV_HYS}	Bootstrap UV hysteresis	Rising to falling threshold	250	400	850	mV
t_{BSTUV}	Bootstrap undervoltage deglitch time		5.5	10	22	µs

7.6 Timing Diagrams

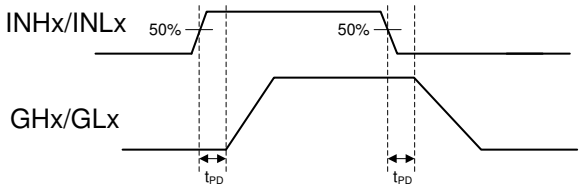


Figure 7-1. Propagation Delay(t_{PD})

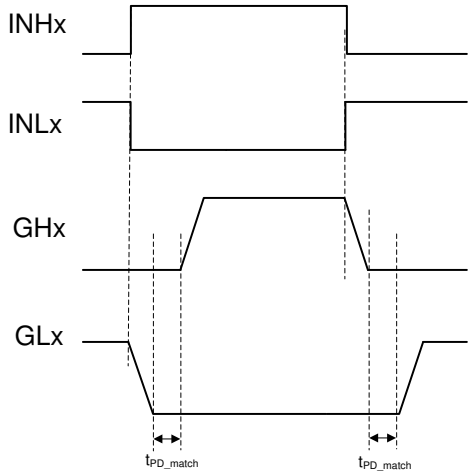


Figure 7-2. Propagation Delay Match (t_{PD_match})

7.7 Typical Characteristics

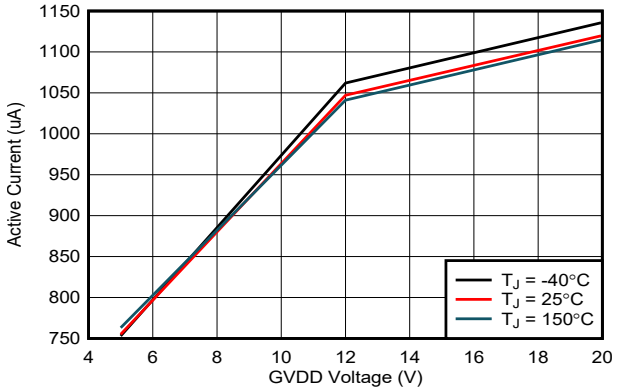


Figure 7-3. Supply Current Over GVDD Voltage

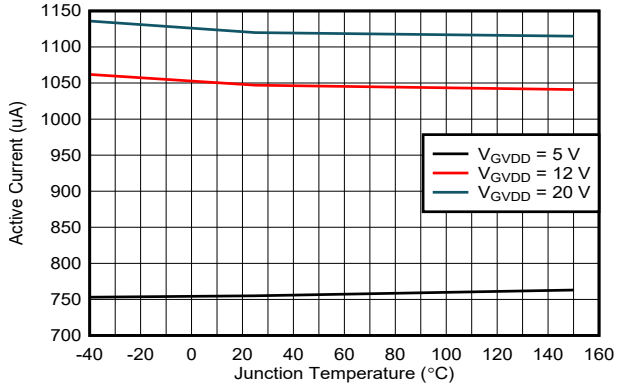


Figure 7-4. Supply Current Over Temperature

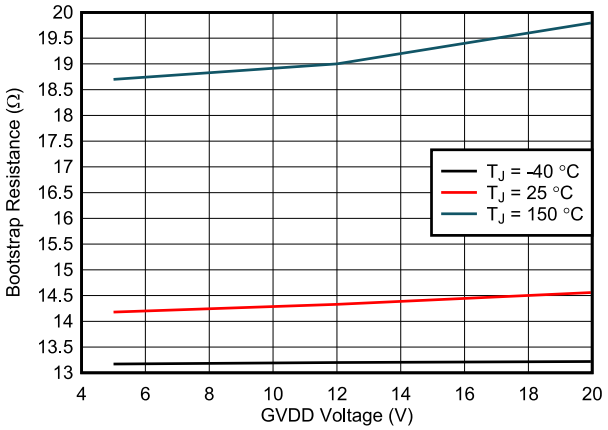


Figure 7-5. Bootstrap Resistance Over GVDD Voltage

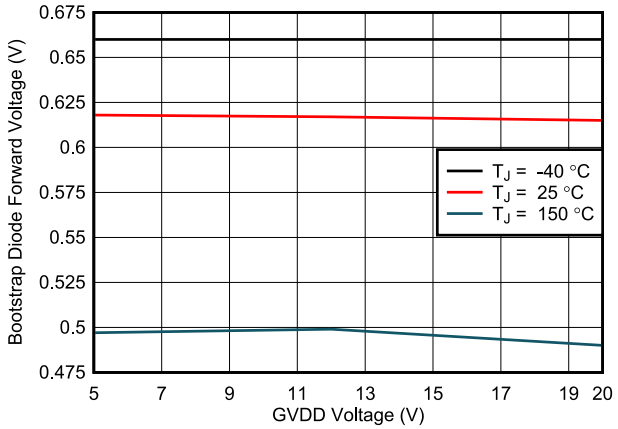


Figure 7-6. Bootstrap Diode Forward Voltage over GVDD Voltage

8 Detailed Description

8.1 Overview

The DRV8300U family of devices is a gate driver for three-phase motor drive applications. These devices decrease system component count, saves PCB space and cost by integrating three independent half-bridge gate drivers and optional bootstrap diodes.

DRV8300U supports external N-channel high-side and low-side power MOSFETs and can drive 750-mA source, 1.5-A sink peak currents with total combined 30-mA average output current. The DRV8300U family of devices are available in 0.5-mm pitch QFN and 0.65-mm pitch TSSOP surface-mount packages. The QFN size is 4 × 4 mm (0.5-mm pin pitch) for the 24-pin package, and TSSOP body size is 6.5 × 4.4 mm (0.65-mm pin pitch) for the 20-pin package.

8.2 Functional Block Diagram

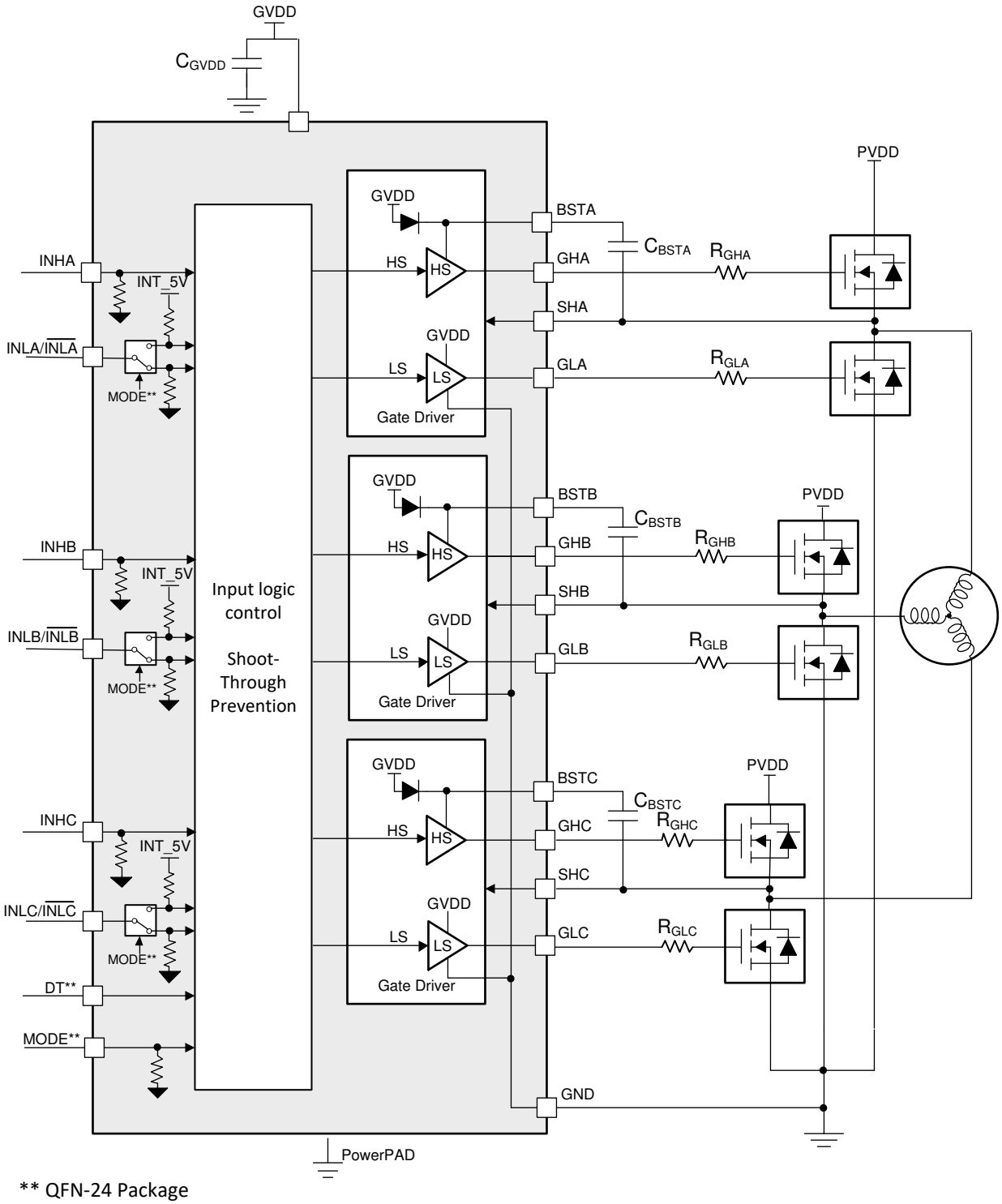


Figure 8-1. Block Diagram for DRV8300UD

8.3 Feature Description

8.3.1 Three BLDC Gate Drivers

The DRV8300U integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using bootstrap capacitor and GVDD supply. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

8.3.1.1 Gate Drive Timings

8.3.1.1.1 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.1.2 Deadtime and Cross-Conduction Prevention

In the DRV8300U, high-side and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at same time. The DRV8300U turns OFF high-side and low-side output to prevent shoot through when the both high-side and low-side inputs are at logic HIGH at same time.

The DRV8300U also provides option to insert additional deadtime to prevent the external high-side and low-side MOSFET from switching on at the same time. In the devices with DT pin (QFN package), deadtime can be linearly adjusted between 200 ns to 2000 ns by configuring resistor value between DT and GND. When the DT pin is left floating, fixed deadtime of 200 nS (typical value) is inserted. The value of resistor can be calculated using Equation 1.

$$R_{DT}\ (k\Omega) = \frac{\text{DT (ns)}}{5} \quad (1)$$

In the devices without DT pin (TSSOP package), fixed deadtime of 200 ns (typical value) is inserted to prevent high and low side gate output turning ON at same time.

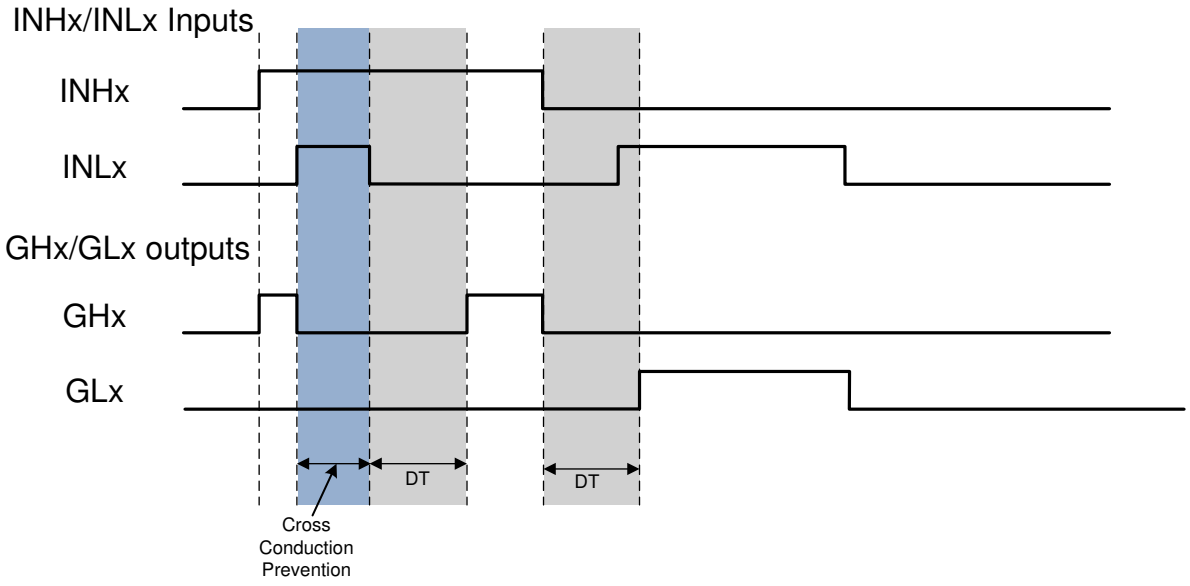


Figure 8-2. Cross Conduction Prevention and Deadtime Insertion

8.3.1.2 Mode (Inverting and non inverting INLx)

The DRV8300U has flexibility of accepting different kind of inputs on INLx. In the devices with MODE pin (QFN package), the DRV8300U provides option of configuring the GLx outputs to be inverted or non-inverted compared to polarity of signal on INLx pins. When the MODE pin is left floating, the INLx is configured to be in non-inverting mode and GLx output is in phase with respect to INLx (see Figure 8-3), whereas when the MODE pin is connected to GVDD, GLx output is out of phase with respect to INLx (see Figure 8-4). In devices without MODE pin (TSSOP package device), there are different device option available for inverting and non inverting inputs (see Section 5).

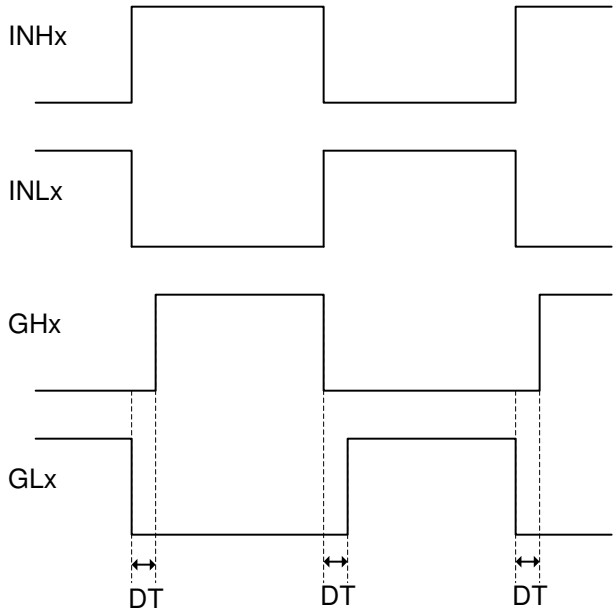


Figure 8-3. Non-Inverted INLx inputs

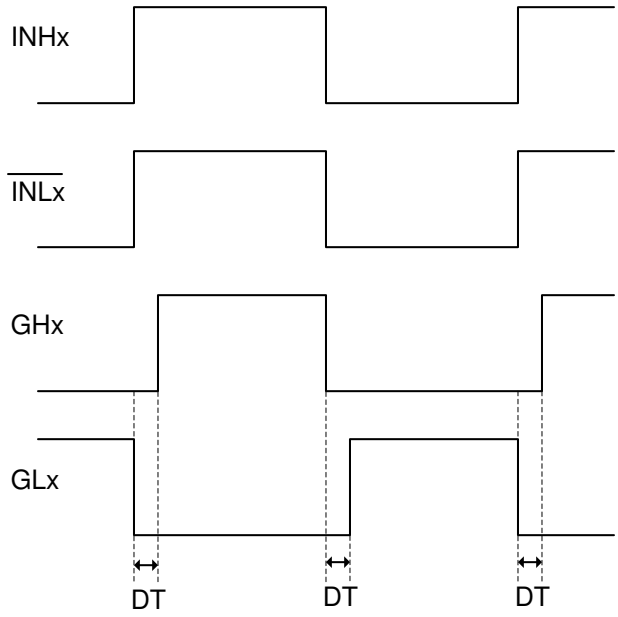


Figure 8-4. Inverted INLx inputs

8.3.2 Pin Diagrams

Figure 8-5 shows the input structure for the logic level pins INHx, INLx. INHx and non-inverted INLx has passive pull down, so when inputs are floating the output the gate driver will be pulled low. Figure 8-6 shows the input structure for the inverted INLx pins. The inverted INLx has passive pull up, so when inputs are floating the output of the low-side gate driver will be pulled low.

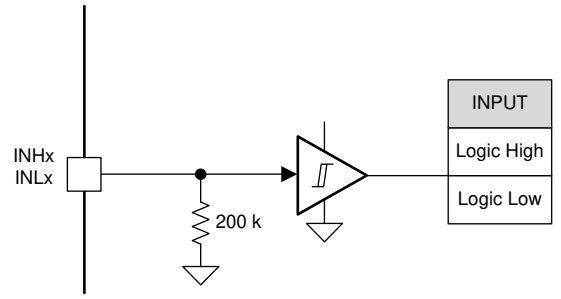


Figure 8-5. INHx and non-inverted INLx Logic-Level Input Pin Structure

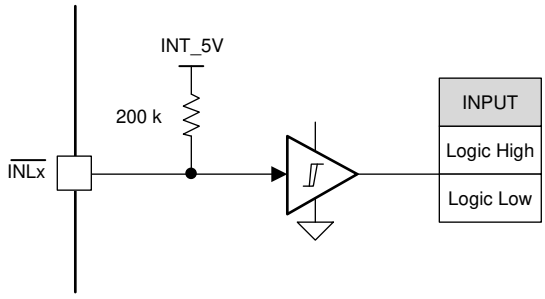


Figure 8-6. Inverted INLx Logic-Level Input Pin Structure

8.3.3 Gate Driver Protective Circuits

The DRV8300U is protected against BSTx undervoltage and GVDD undervoltage events.

Table 8-1. Fault Action and Response

FAULT	CONDITION	GATE DRIVER	RECOVERY
V_{BSTx} undervoltage (BSTUV)	$V_{BSTx} < V_{BSTUV}$	GHx - Hi-Z	Automatic: $V_{BSTx} > V_{BSTUV}$ and low to high PWM edge detected on INHx pin
GVDD undervoltage (GVDDUV)	$V_{GVDD} < V_{GVDDUV}$	Hi-Z	Automatic: $V_{GVDD} > V_{GVDDUV}$

8.3.3.1 V_{BSTx} Undervoltage Lockout (BSTUV)

The DRV8300U has separate voltage comparator to detect undervoltage condition for each phases. If at any time the voltage on the BSTx pin falls lower than the V_{BSTUV} threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge is detected on INHx input of the same phase that BSTUV condition was detected. BSTUV protection ensures that high-side MOSFETs are not driven when the BSTx pins has lower value.

8.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDDUV} threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again when the GVDDUV condition clears. GVDDUV protection ensures that external MOSFETs are not driven when the GVDD input is at lower value.

8.4 Device Functional Modes

The DRV8300U is in operating (active) mode, whenever the GVDD and BST pins are higher than the UV threshold (GVDD > $V_{GVDDUV}$and V_{BSTX} > V_{BSTUV}). In active mode, the gate driver output GHx and GLX will follow respective inputs INHx and INLx.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8300U family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 9.2* section highlight how to use and configure the DRV8300U.

9.2 Typical Application

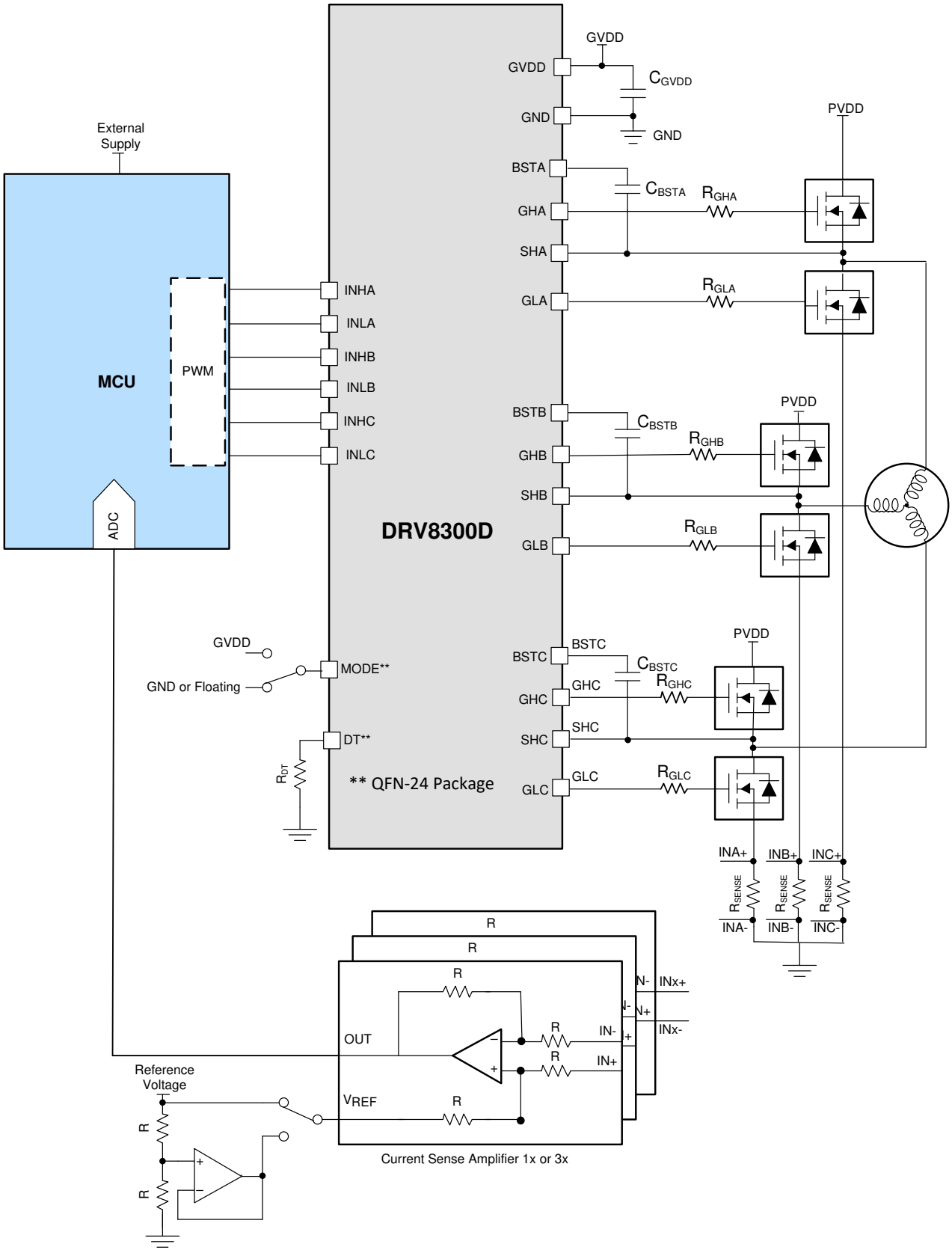


Figure 9-1. Application Schematic

9.2.1 Design Requirements

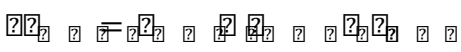
Table 9-1 lists the example design input parameters for system design.

Table 9-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
MOSFET	-	CSD19532Q5B
Gate Supply Voltage	V_{GVDD}	12 V
Gate Charge	Q_G	48 nC

9.2.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 2 calculates the maximum allowable voltage drop across the bootstrap capacitor:



(2)

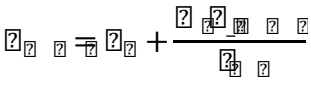
=12 V – 0.85 V – 4.5 V = 6.65 V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with Equation 3:



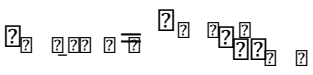
(3)

=48 nC + 220 µA/20 kHz = 50 nC + 11 nC = 59 nC

where

- Q_G is the total MOSFET gate charge
- I_{LBS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

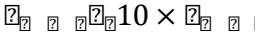
The minimum bootstrap capacitor an then be estimated as below assuming 1V ΔV_{BSTx}:



(4)

= 59 nC / 1 V = 59 nF

The calculated value of minimum bootstrap capacitor is 59 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.



(5)

= 10*100 nF= 1 µF

For this example application choose 1 µF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

9.2.3 Application Curves

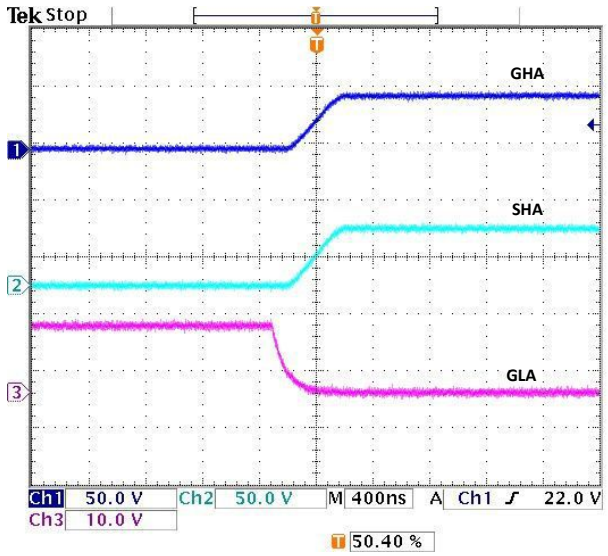


Figure 9-2. Gate voltages, SHx rising with 15 ohm gate resistor and CSD19532Q5B MOSFET

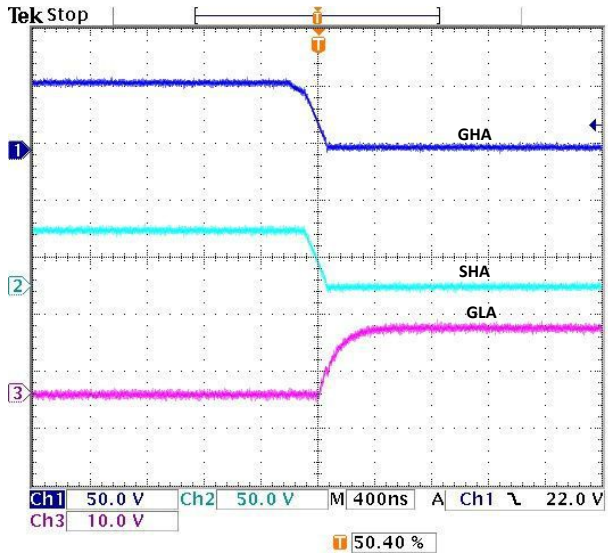


Figure 9-3. Gate voltages, SHx falling with 15 ohm gate resistor and CSD19532Q5B MOSFET

10 Power Supply Recommendations

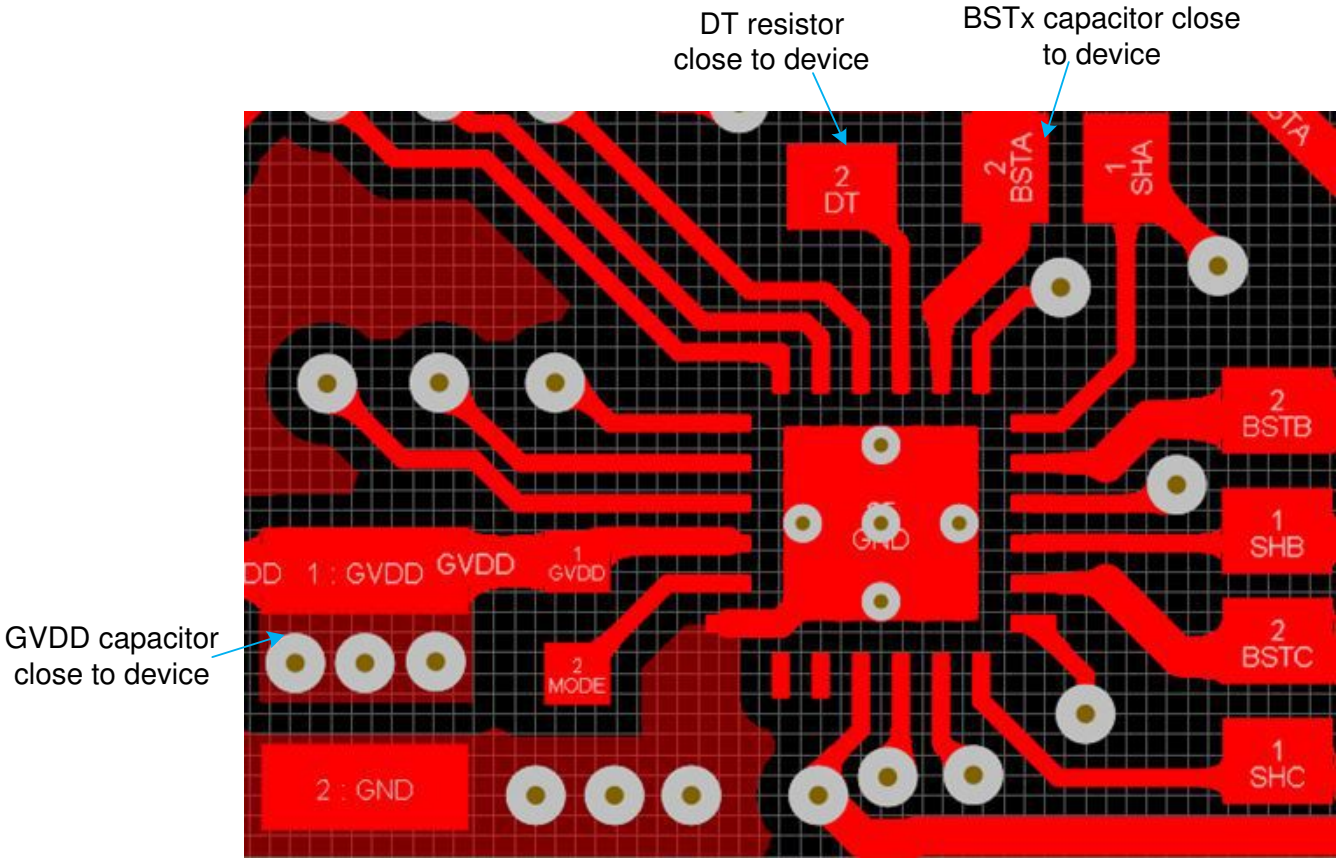
The DRV8300U is designed to operate from an input voltage supply (GVDD) range from 4.8 V to 20 V. A local bypass capacitor should be placed between the GVDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surfacemount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, capacitor across the BSTx to SHx is recommended, it should be high enough capacitance value capacitor to deliver GHx pulses

11 Layout

11.1 Layout Guidelines

- Low ESR/ESL capacitors must be connected close to the device between GVDD and GND and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- In order to avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.
- In order to avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the trace length and number of vias wherever possible. Minimum 10 mil and typical 15 mil trace width is recommended.
- Resistance between DT and GND must be place as close as possible to device
- Place the gate driver as close to the MOSFETs as possible. Confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area by reducing trace length. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs.
- In QFN package device variants, NC pins can be connected to GND to increase ground conenction between thermal pad and external ground plane.
- Refer to sections *General Routing Techniques and MOSFET Placement and Power Stage Routing* in Application Report

11.2 Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8300UDPWR	ACTIVE	TSSOP	PW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8300UD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

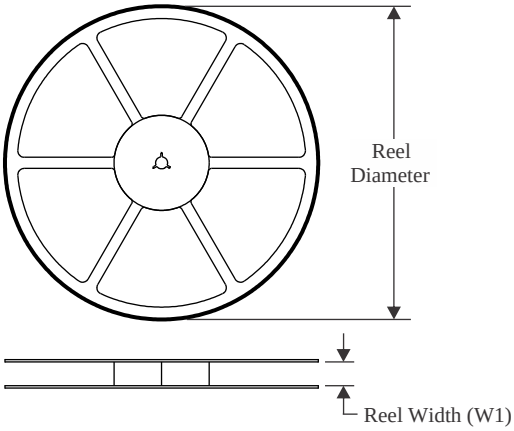
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

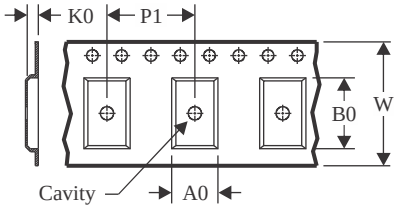
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

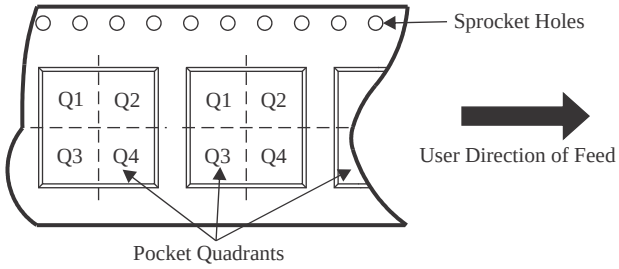


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

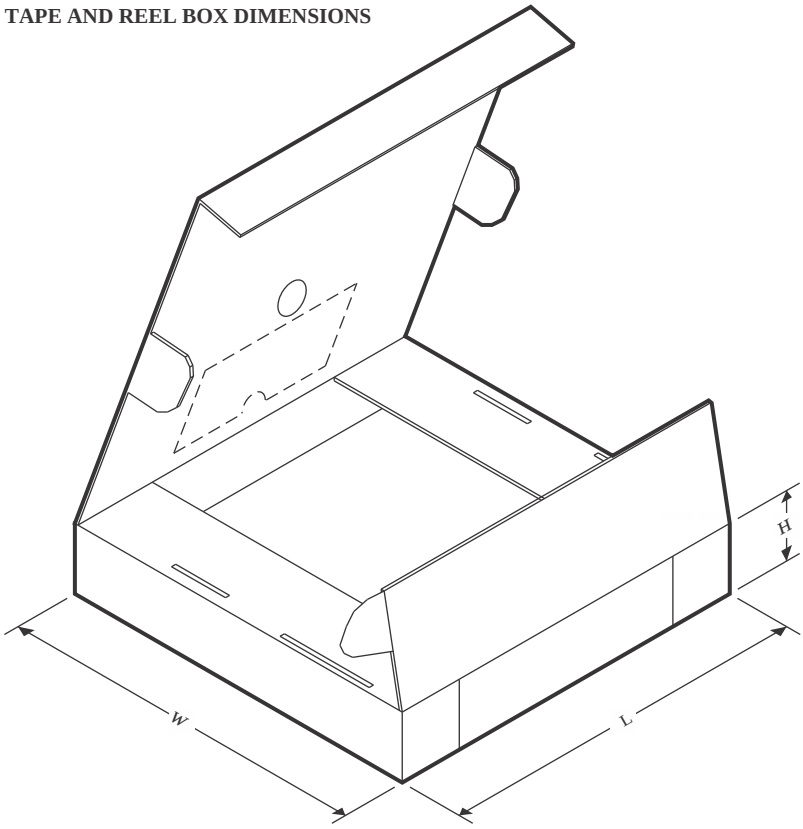
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8300UDPWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

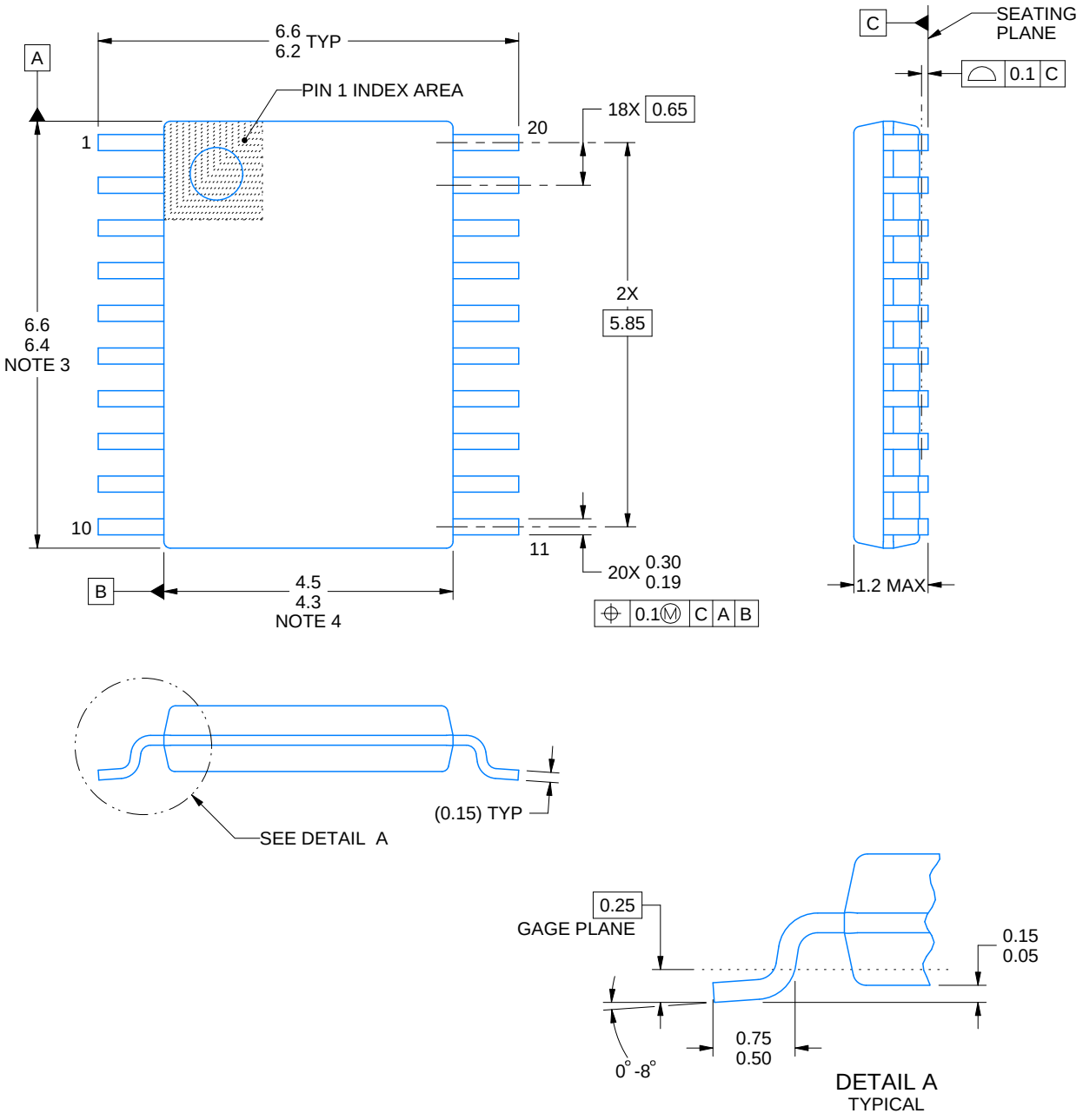
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8300UDPWR	TSSOP	PW	20	3000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

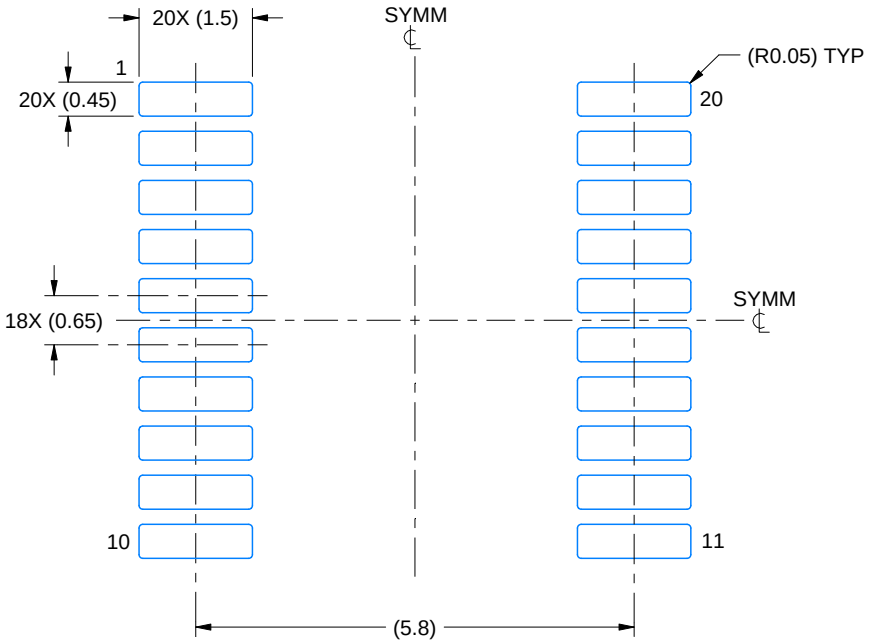
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

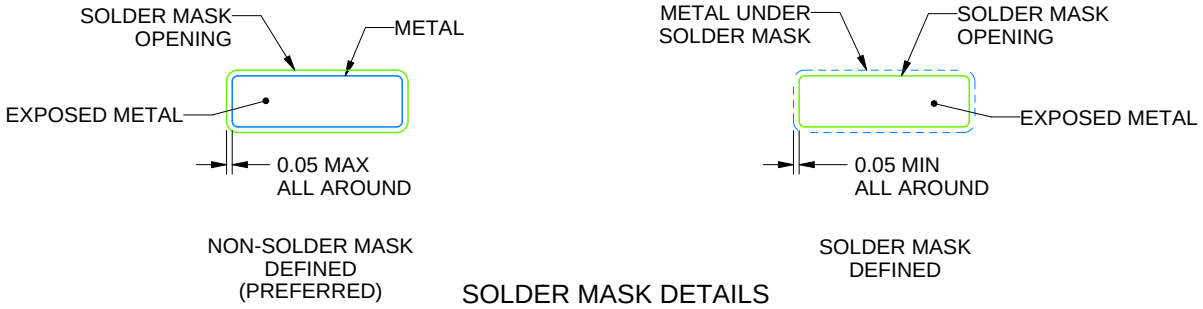


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

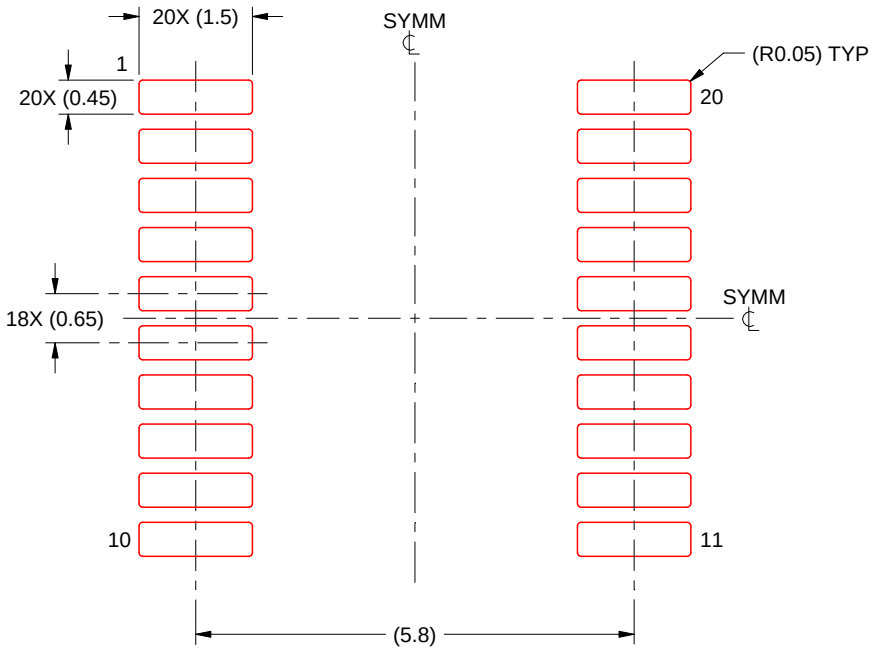


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

DRV8424/25 Stepper Drivers With Integrated Current Sense, 1/256 Microstepping, STEP/DIR Interface and smart tune Technology

1 Features

- PWM microstepping stepper motor driver
  - Simple STEP/DIR interface
  - Up to 1/256 microstepping indexer
- Integrated current sense functionality
  - No sense resistors required
  - ±5% full-scale current accuracy
- Smart tune decay technology, fixed slow, and mixed decay options
- 4.5 to 33-V operating supply voltage range
- Low $R_{DS(ON)}$:
  - DRV8424: 330 mΩ HS + LS at 24 V, 25°C
  - DRV8425: 550 mΩ HS + LS at 24 V, 25°C
- High current capacity per bridge
  - DRV8424: 4 A peak, 2.5 A full-scale, 1.8 A rms
  - DRV8425: 3.2 A peak, 2 A full-scale, 1.4 A rms
- Pin to pin compatible with -
  - DRV8426: 33-V, 900 mΩ HS + LS
  - DRV8436: 48-V, 900 mΩ HS + LS
  - DRV8434: 48-V, 330 mΩ HS + LS
- Configurable off-time PWM chopping
  - 7-µs, 16-µs, 24-µs, or 32-µs.
- Supports 1.8-V, 3.3-V, 5.0-V Logic Inputs
- Low-Ccrrent sleep mode (2 µA)
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Printers and scanners
- ATM and money handling machines
- Textile machines
- Stage lighting equipment
- Office and home automation
- Factory automation and robotics
- Medical applications
- 3D printers

3 Description

The DRV8424/25 are stepper motor drivers for industrial and consumer applications. The device is fully integrated with two N-channel power MOSFET H-bridge drivers, a microstepping indexer, and integrated current sensing. The DRV8424 is capable of driving up to 2.5-A full-scale output current; and the DRV8425 is capable of driving up to 2-A full-scale output current (dependent on PCB design).

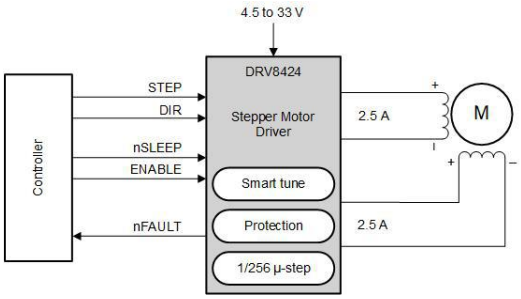
The DRV8424/25 use an internal current sense architecture to eliminate the need for two external power sense resistors, saving PCB area and system cost. The devices use an internal PWM current regulation scheme selectable between smart tune, slow and mixed decay options. Smart tune automatically adjusts for optimal current regulation, compensates for motor variation and aging effects and reduces audible noise from the motor.

A simple STEP/DIR interface allows an external controller to manage the direction and step rate of the stepper motor. The device can be configured in full-step to 1/256 microstepping. A low-power sleep mode is provided using a dedicated nSLEEP pin. Protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8424PWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8424RGER	VQFN (24)	4.0mm x 4.0mm
DRV8425PWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8425RGER	VQFN (24)	4.0mm x 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2020) to Revision B (May 2021)	Page
• Fixed typo in *Description*	1
• Fixed typo in Table 7-6	18
• Removed duplicate package drawings	45

Changes from Revision * (May 2020) to Revision A (October 2020)	Page
• Changed Device Status to "Production Data"	1

Device Comparison Table

PART NUMBER	$R_{DS(ON)}$ (HS + LS) (mΩ)	Full-Scale Current Per Bridge (A)
DRV8424	330	2.5
DRV8425	550	2

5 Pin Configuration and Functions

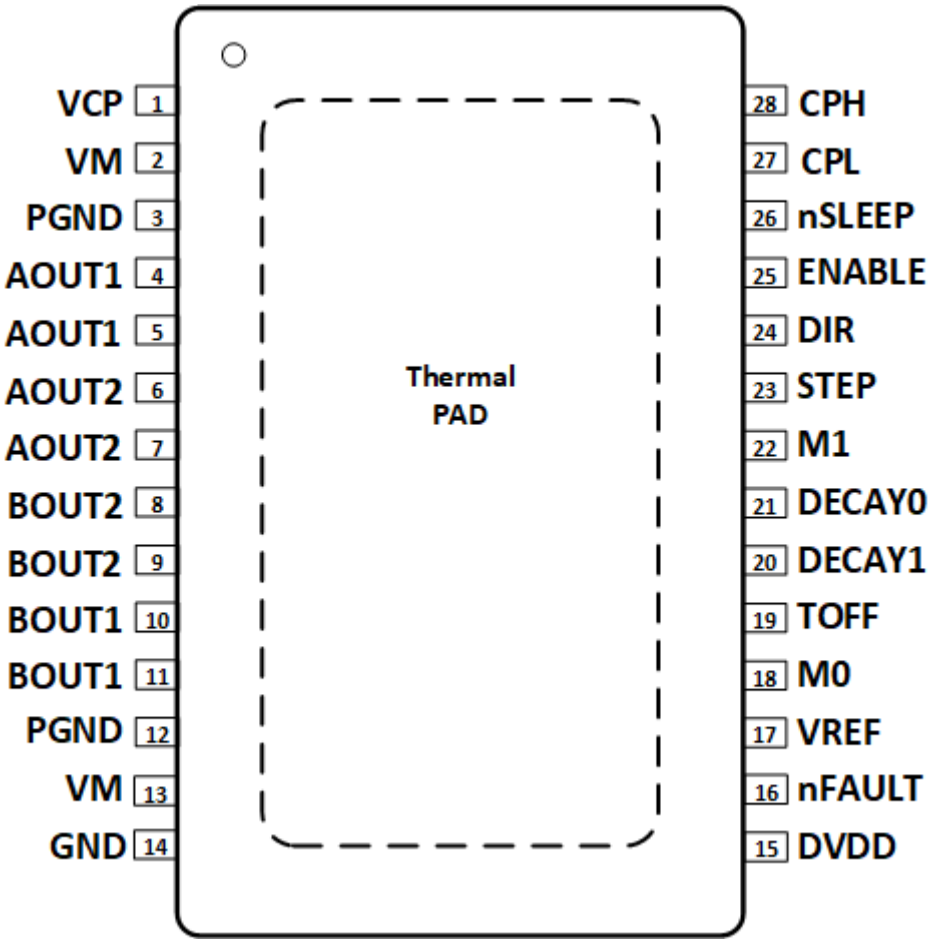


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View

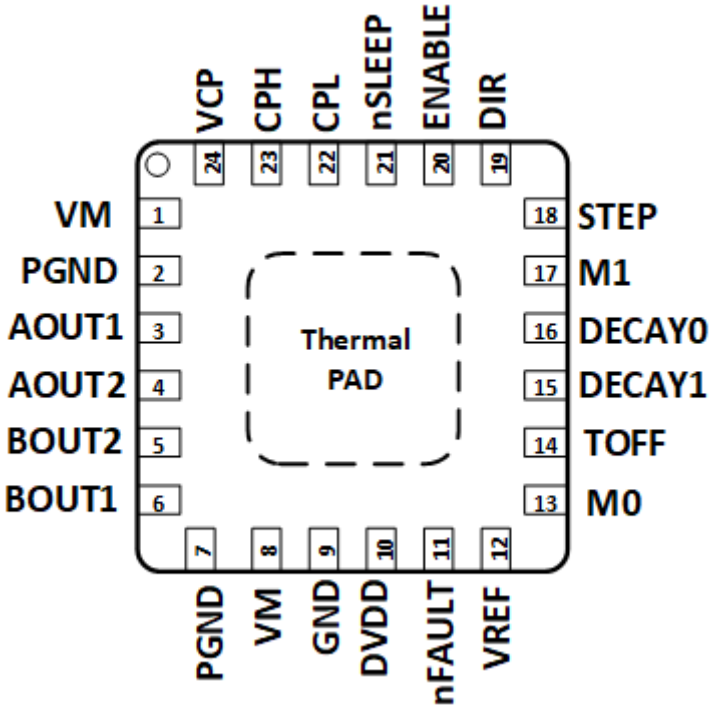


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View

Table 5-1. Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	4, 5	3	O	Output	Winding A output. Connect to stepper motor winding.
AOUT2	6, 7	4	O	Output	Winding A output. Connect to stepper motor winding.
PGND	3, 12	2, 7	—	Power	Power ground. Connect to system ground.
BOUT2	8, 9	5	O	Output	Winding B output. Connect to stepper motor winding
BOUT1	10, 11	6	O	Output	Winding B output. Connect to stepper motor winding
CPH	28	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	22			
DIR	24	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
ENABLE	25	20	I	Input	Logic low to disable device outputs; logic high to enable; internal pullup to DVDD. Also determines the type of OCP and OTSD response.
DVDD	15	10	O	Power	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	14	9	—	Power	Device ground. Connect to system ground.
VREF	17	12	I	Input	Current set reference input. Maximum value 3.3 V for DRV8424 and 2.64V for DRV8425. DVDD can be used to provide VREF through a resistor divider.
M0	18	13	I	Input	Microstepping mode-setting pins. Sets the step mode; internal pulldown resistor.
M1	22	17			
DECAY0	21	16	I	Input	Decay-mode setting pins. Sets the decay mode (see the Section 7.3.6 section).
DECAY1	20	15			

Table 5-1. Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
STEP	23	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
VCP	1	24	—	Power	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
TOFF	19	14	I	Input	Sets the Decay mode off time during current chopping; four level pin. Also sets the ripple current in smart tune ripple control mode.
nFAULT	16	11	O	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	26	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, DECAY0, DECAY1, TOFF, M0, M1)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	33	V
V_I	Logic level input voltage	0	5.5	V
V_{VREF}	VREF voltage (DRV8424)	0.05	3.3	V
V_{VREF}	VREF voltage (DRV8425)	0.05	2.64	V
f_{STEP}	Applied STEP signal (STEP)	0	500(1)	kHz
I_{FS}	Motor full-scale current (xOUTx) (DRV8424)	0	2.5(2)	A
I_{FS}	Motor full-scale current (xOUTx) (DRV8425)	0	2(2)	A
I_{rms}	Motor RMS current (xOUTx) (DRV8424)	0	1.8(2)	A
I_{rms}	Motor RMS current (xOUTx) (DRV8425)	0	1.4(2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		DRV8424/25		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	17.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.7	17.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
t_{EN}	Enable time	ENABLE = 0/1 to output transition			5	µs
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 33 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{CP}	VCP operating voltage	6 V < V_{VM} < 33 V		V_{VM} + 5		V
$f_{(CP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
TRI-LEVEL INPUTS (M0, DECAY0, DECAY1, ENABLE)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
QUAD-LEVEL INPUTS (M1, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_{IL}	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance (DRV8424)	T_J = 25 °C, I_O = -1 A		165	200	mΩ
		T_J = 125 °C, I_O = -1 A		250	300	mΩ
		T_J = 150 °C, I_O = -1 A		280	350	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (DRV8424)	T_J = 25 °C, I_O = 1 A		165	200	mΩ
		T_J = 125 °C, I_O = 1 A		250	300	mΩ
		T_J = 150 °C, I_O = 1 A		280	350	mΩ

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ONH)}$	High-side FET on resistance (DRV8425)	T_J = 25 °C, I_O = -1 A		275	330	mΩ
		T_J = 125 °C, I_O = -1 A		410	500	mΩ
		T_J = 150 °C, I_O = -1 A		460	580	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance (DRV8425)	T_J = 25 °C, I_O = 1 A		275	330	mΩ
		T_J = 125 °C, I_O = 1 A		410	500	mΩ
		T_J = 150 °C, I_O = 1 A		460	580	mΩ
t_{SR}	Output slew rate	V_{VM} = 24 V, I_O = 1 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain	VREF = 3.3 V	1.254	1.32	1.386	V/A
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			8.25	µA
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 2.5 A, 10% to 20% current setting	–8		12	%
		I_O = 2.5 A, 20% to 40% current setting	–7		7	
		I_O = 2.5 A, 40% to 100% current setting	–5		5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 2.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET, DRV8424	4			A
I_{OCP}	Overcurrent protection	Current through any FET, DRV8425	3.2			A
t_{OCP}	Overcurrent deglitch time			1.8		µs
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Indexer Timing Requirements

Typical limits are at T_J = 25°C and V_{VM} = 24 V. Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500(1)	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, STEP rising to DIR or MODEx change	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

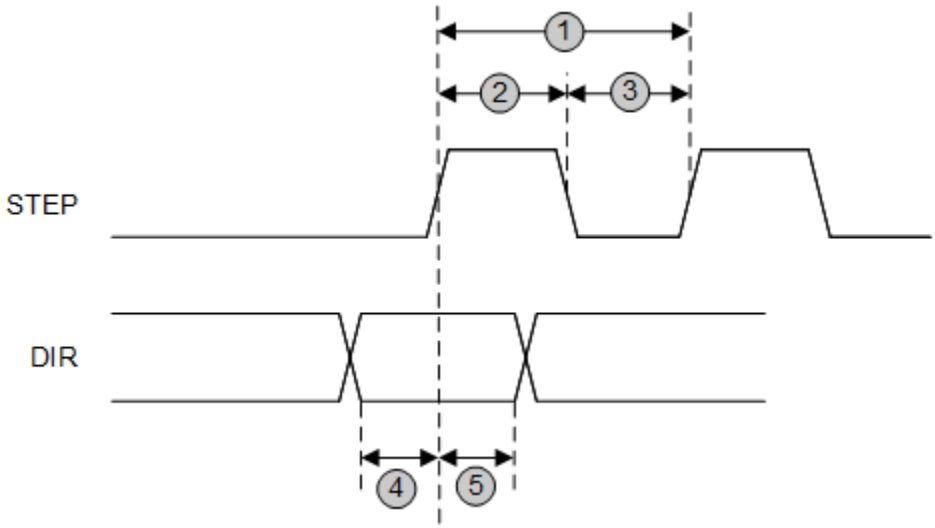


Figure 6-1. STEP and DIR Timing Diagram

6.7 Typical Characteristics

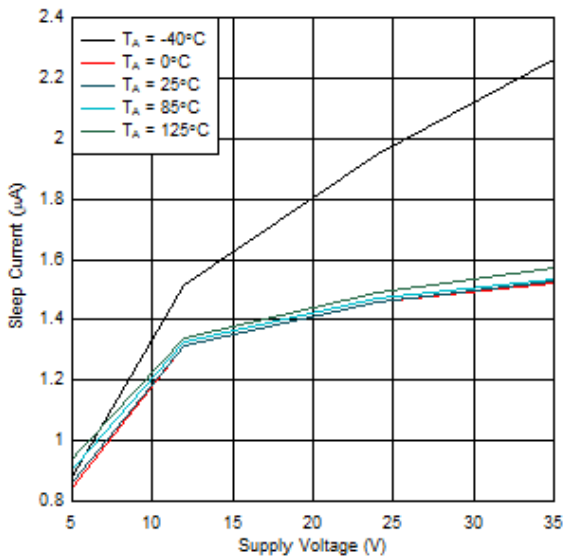


Figure 6-2. Sleep Current over Supply Voltage

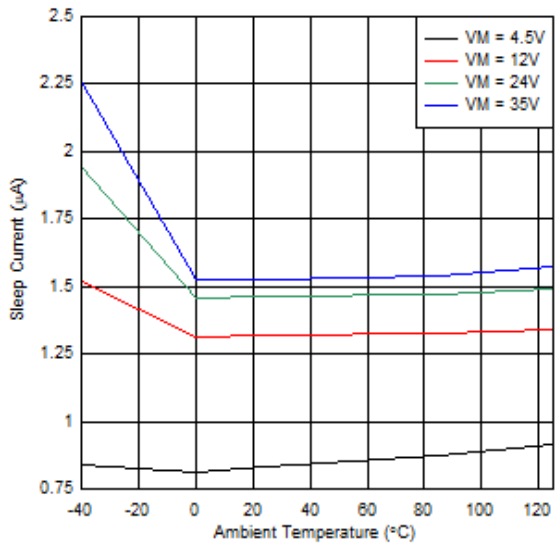


Figure 6-3. Sleep Current over Temperature

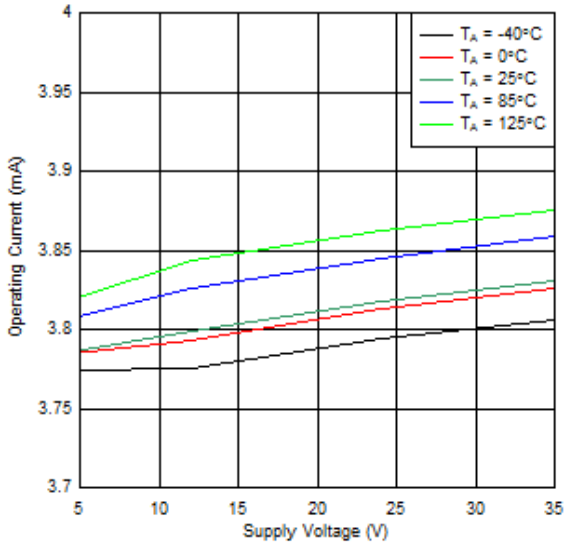


Figure 6-4. Operating Current over Supply Voltage

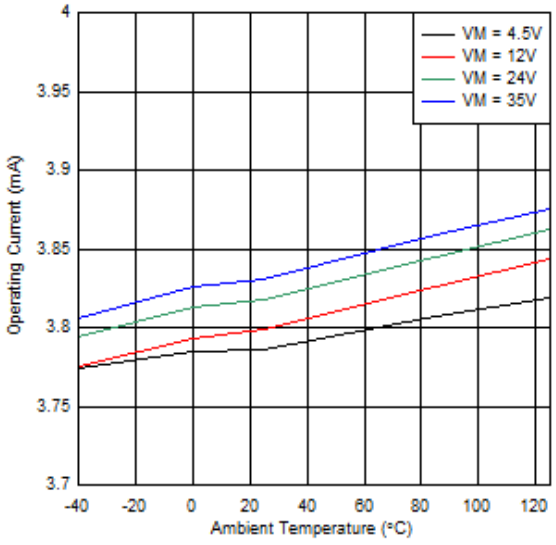


Figure 6-5. Operating Current over Temperature

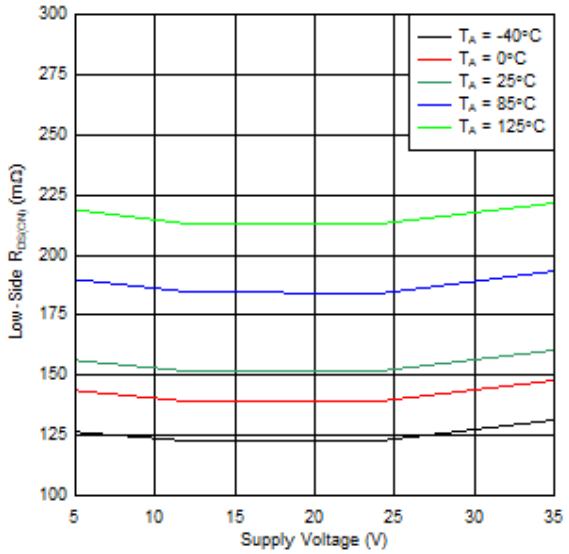


Figure 6-6. Low-Side $R_{DS(ON)}$ over Supply Voltage

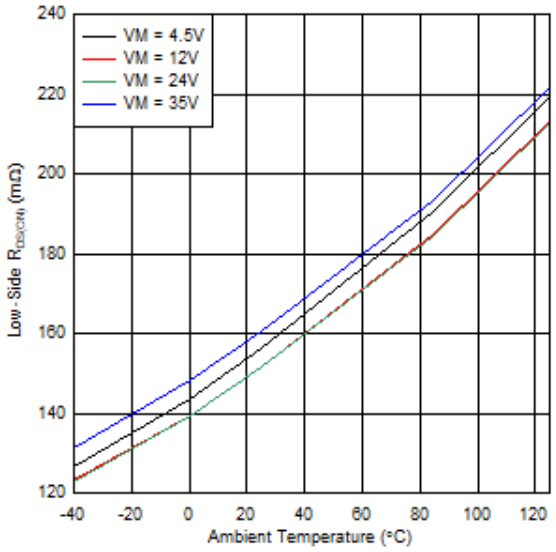


Figure 6-7. Low-Side $R_{DS(ON)}$ over Temperature

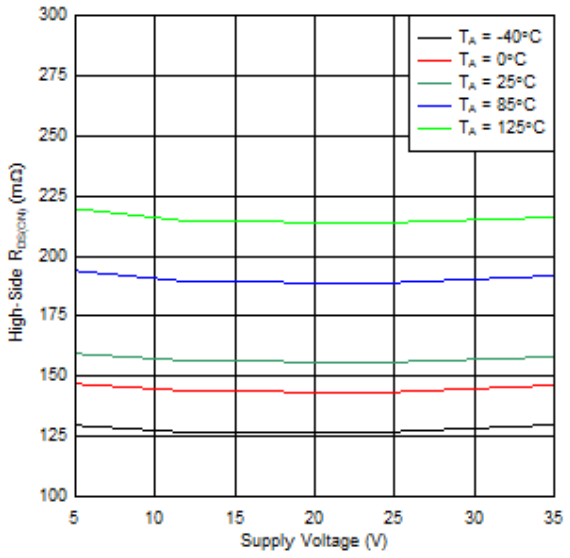


Figure 6-8. High-Side $R_{DS(ON)}$ over Supply Voltage

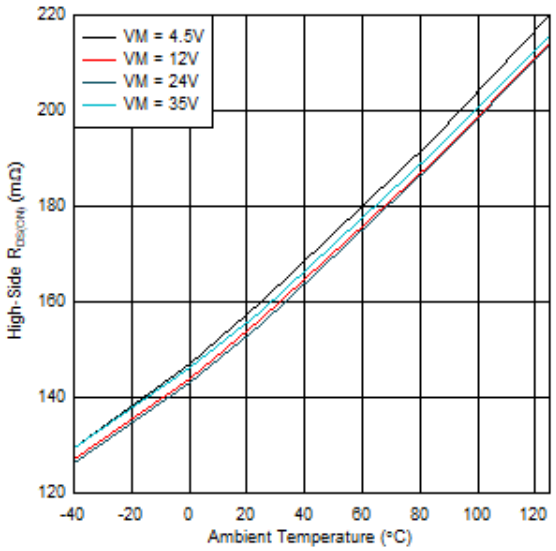


Figure 6-9. High-Side $R_{DS(ON)}$ over Temperature

7 Detailed Description

7.1 Overview

The DRV8424/25 devices are integrated motor-driver solutions for bipolar stepper motors. The devices provide the maximum integration by integrating two N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and a microstepping indexer. The DRV8424 and DRV8425 are pin-to-pin compatible with the DRV8426, DRV8436, and the DRV8434. The DRV8424 and DRV8425 are capable of supporting wide supply voltage of 4.5 to 33 V. DRV8424 provides an output current up to 4-A peak, 2.5-A full-scale, or 1.8-A root mean square (rms), while the DRV8425 provides an output current up to 3.2-A peak, 2-A full-scale, or 1.4-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8424/25 devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, like slow decay, mixed decay and fast decay. The DRV8424/25 comes with smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme to minimize distortion of the motor winding current while minimizing frequency content and significantly reducing design efforts. Along with this seamless, effortless automatic smart tune, DRV8424/25 also provides the traditional decay modes like slow-mixed and mixed decay as well.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

7.2 Functional Block Diagram

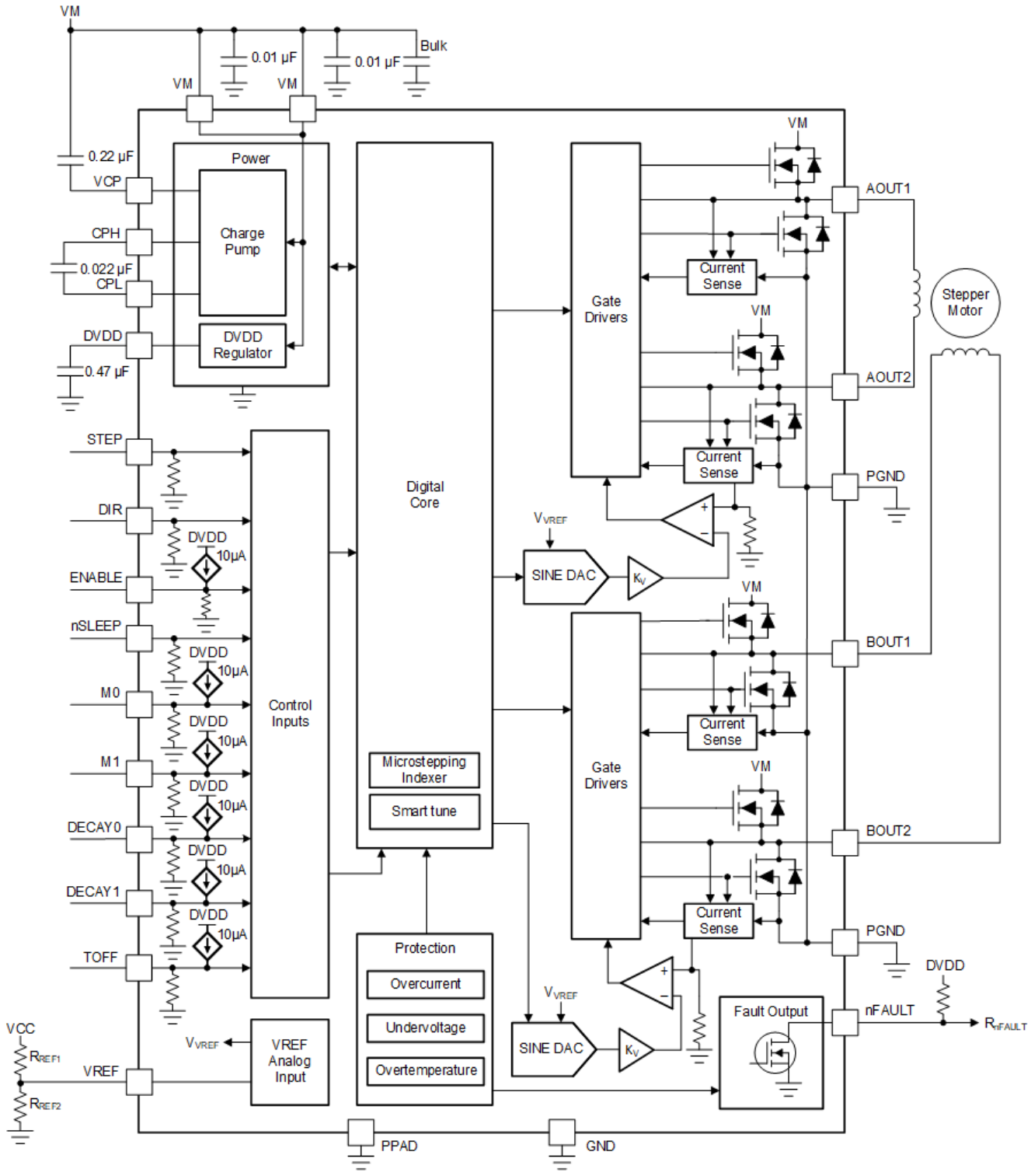


Figure 7-1.

7.3 Feature Description

Table 7-1 lists the recommended external components for the DRV8424/25 devices.

Table 7-1. DRV8424/25 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{CP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the DRV8424/25 device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8424, the peak current rating is 4A per bridge; and for the DRV8425, the peak current rating is 3.2A per bridge.

7.3.1.2 RMS Current Rating

The RMS (average) current is determined by the thermal considerations of the IC. The RMS current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8424, the rms current rating is 1.75A per bridge; and for the DRV8425, the RMS current rating is 1.4A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$ for a sinusoidal current waveform, and I_{RMS} for a square wave current waveform (full step).

Table 7-2. Current Ratings

	DRV8424	DRV8425
Peak Current Rating	4 A	3.2 A
RMS Current Rating	1.8 A	1.4 A
Full-Scale Current Rating	2.5 A	2 A

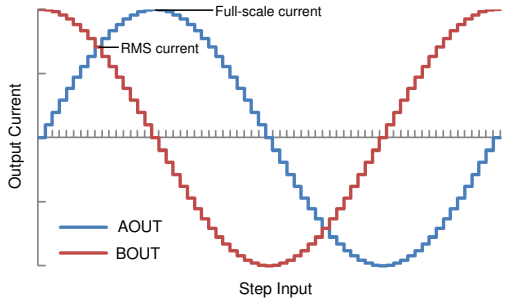


Figure 7-2. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

The DRV8424/25 devices have drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. Figure 7-3 shows a block diagram of the circuitry.

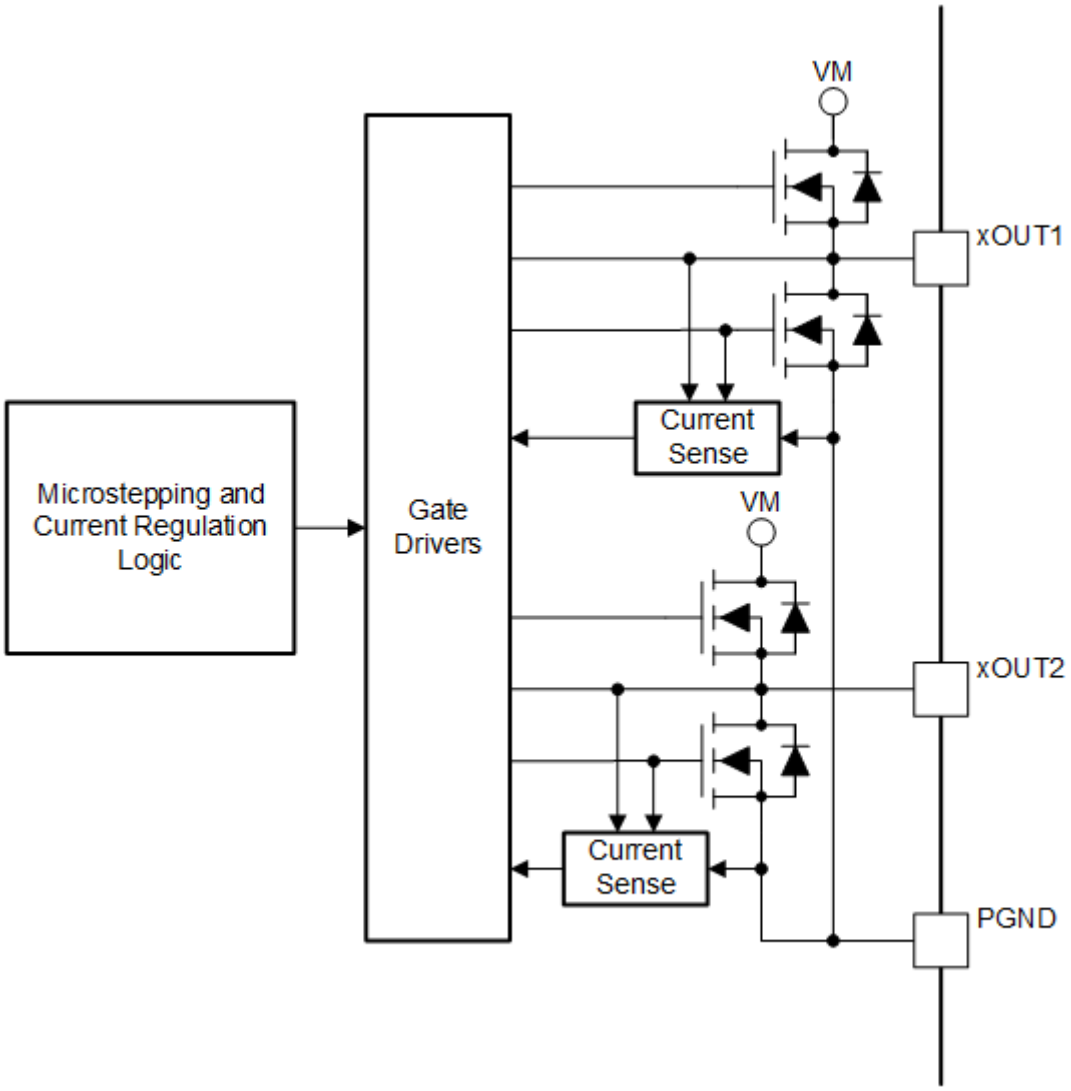


Figure 7-3. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8424/25 devices allow a number of different step modes. The M0 and M1 pins are used to configure the step mode as shown in Table 7-3. The settings can be changed on the fly.

Table 7-3. Microstepping Indexer Settings

MODE0	MODE1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step

Table 7-3. Microstepping Indexer Settings (continued)

MODE0	MODE1	STEP MODE
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

Table 7-4 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

Note

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

Table 7-4. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25

Table 7-4. Relative Current and Step Directions (continued)

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 7-5 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

Table 7-5. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 7-6 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

Table 7-6. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3V for DRV8424 and 2.64V for DRV8425.

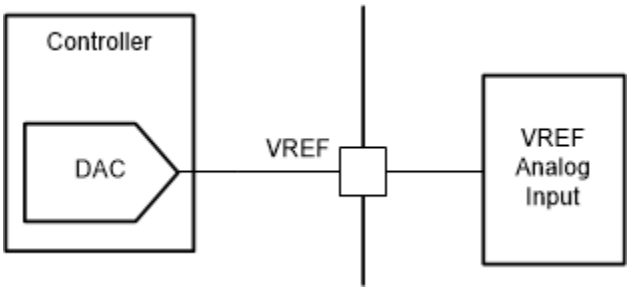


Figure 7-4. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

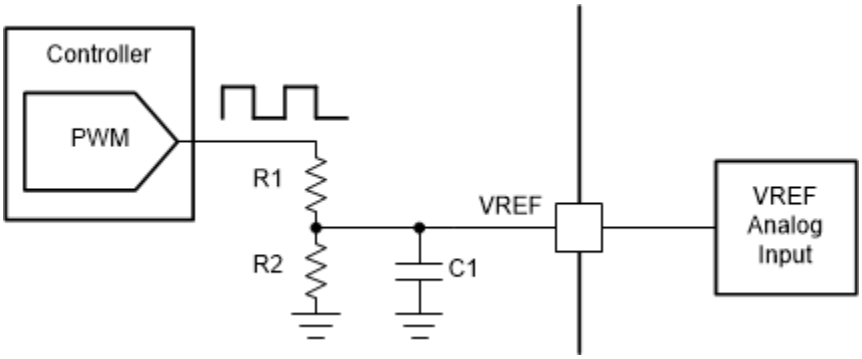


Figure 7-5. Controlling VREF With a PWM Resource

7.3.5 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

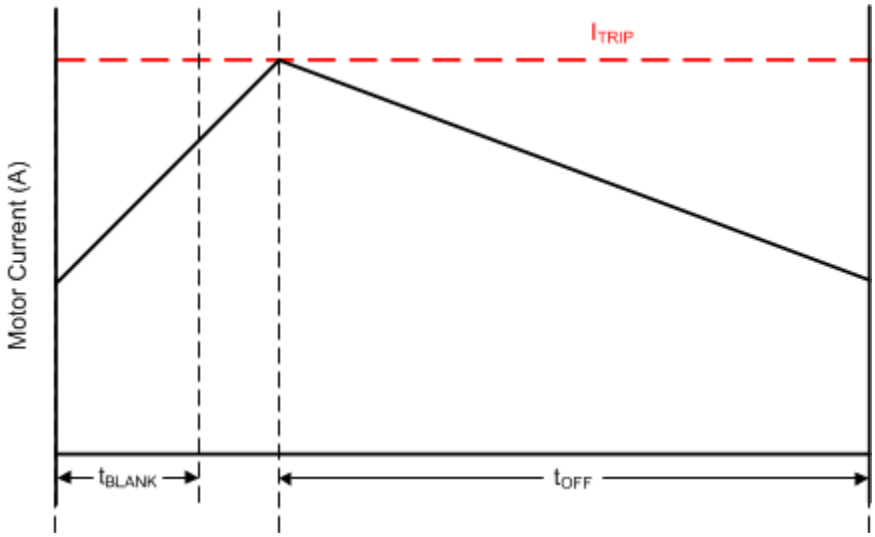


Figure 7-6. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin.

The full-scale regulation current (I_{FS}) can be calculated as I_{FS} (A) = V_{REF} (V) / K_V (V/A) = V_{REF} (V) / 1.32 (V/A).

7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-7, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7-7, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-7, Item 3.

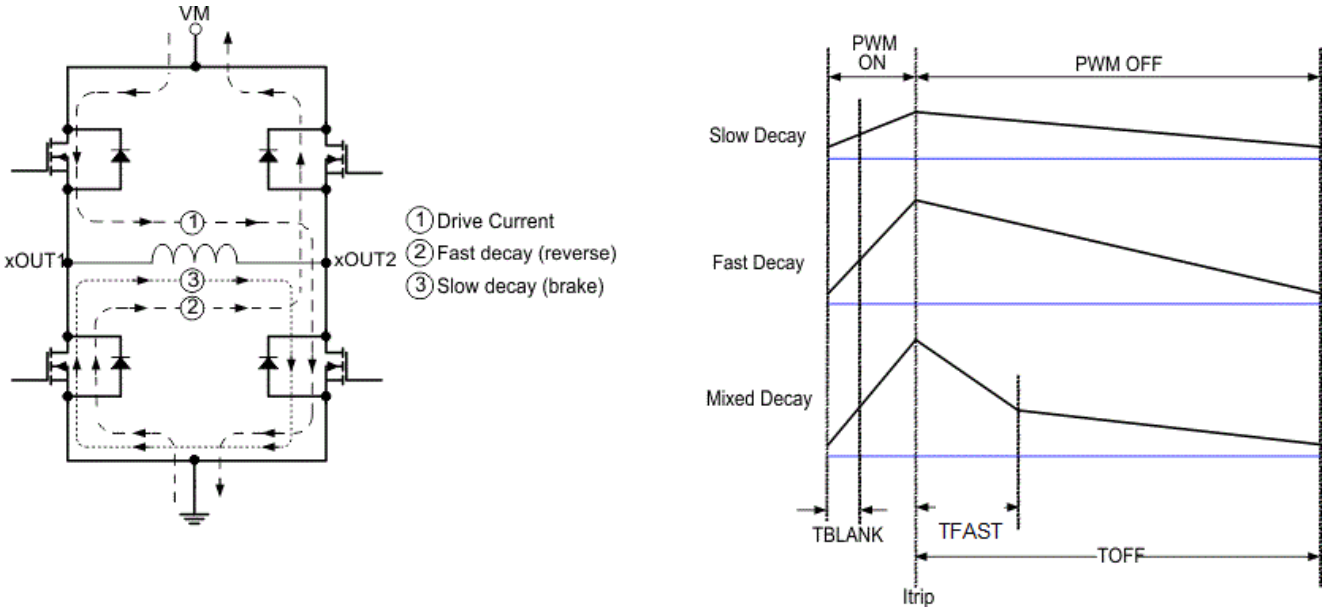


Figure 7-7. Decay Modes

The decay mode of the DRV8424/25 is selected by the DECAY0 and DECAY1 pins as shown in Table 7-7. If DECAY1 pin is Hi-Z, irrespective of the DECAY0 pin voltage, the decay mode will be smart tune dynamic decay. The decay modes can be changed on the fly. After a decay mode change, the new decay mode is applied after a 10 µs de-glitch time.

Table 7-7. Decay Mode Settings

DECAY0	DECAY1	INCREASING STEPS	DECREASING STEPS
0	0	Smart tune Dynamic Decay	Smart tune Dynamic Decay
0	1	Smart tune Ripple Control	Smart tune Ripple Control
1	0	Mixed decay: 30% fast	Mixed decay: 30% fast
1	1	Slow decay	Mixed decay: 30% fast
Hi-Z	0	Mixed decay: 60% fast	Mixed decay: 60% fast
Hi-Z	1	Slow decay	Slow decay

Figure 7-8 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

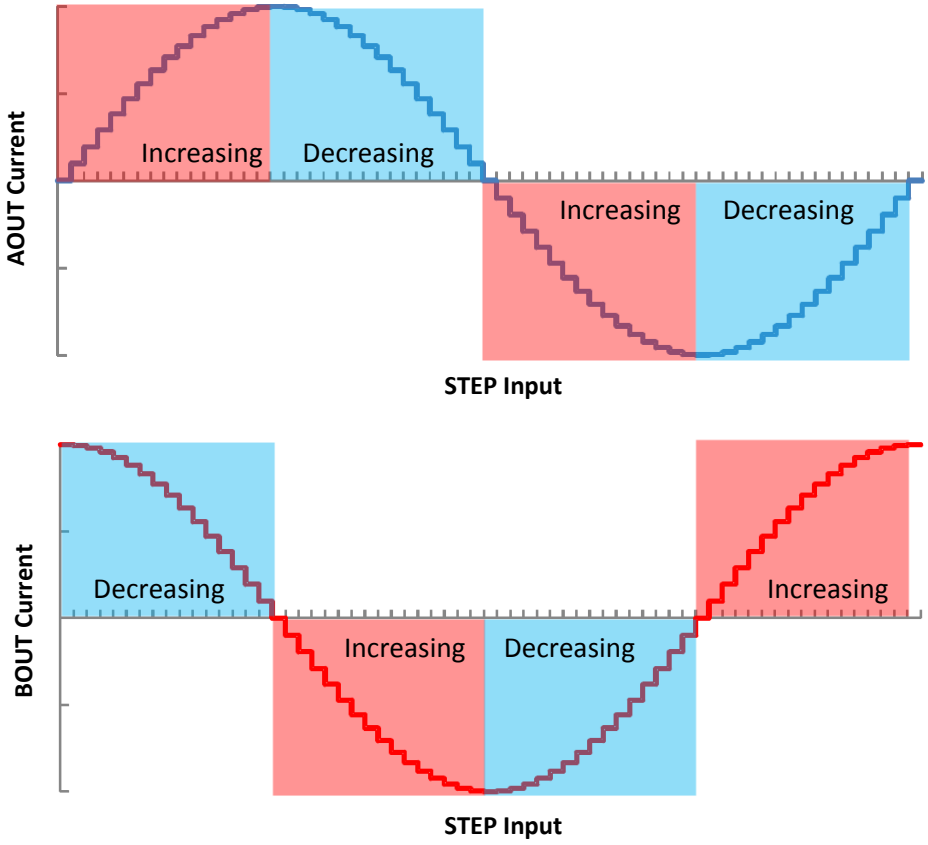


Figure 7-8. Definition of Increasing and Decreasing Steps

7.3.6.1 Slow Decay for Increasing and Decreasing Current

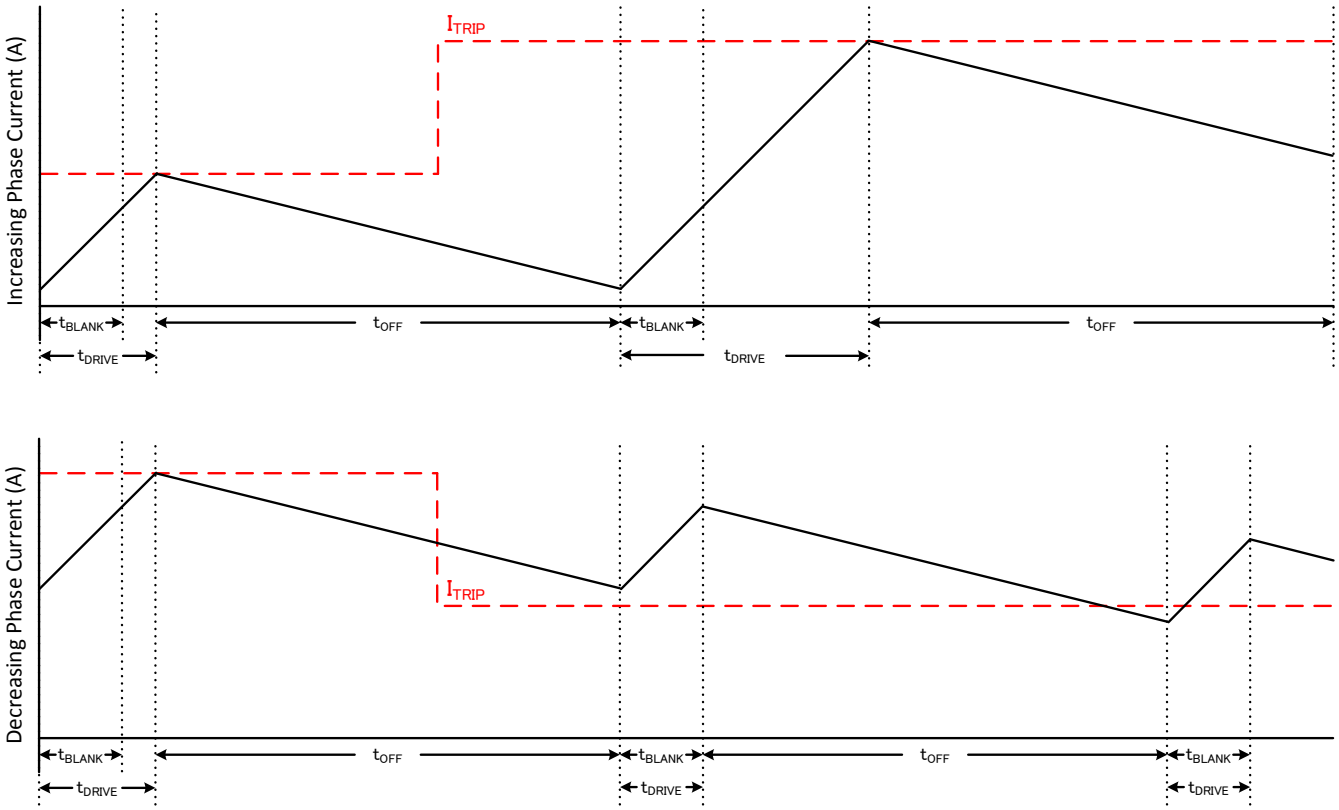


Figure 7-9. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new ITRIP level because the current decreases very slowly.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

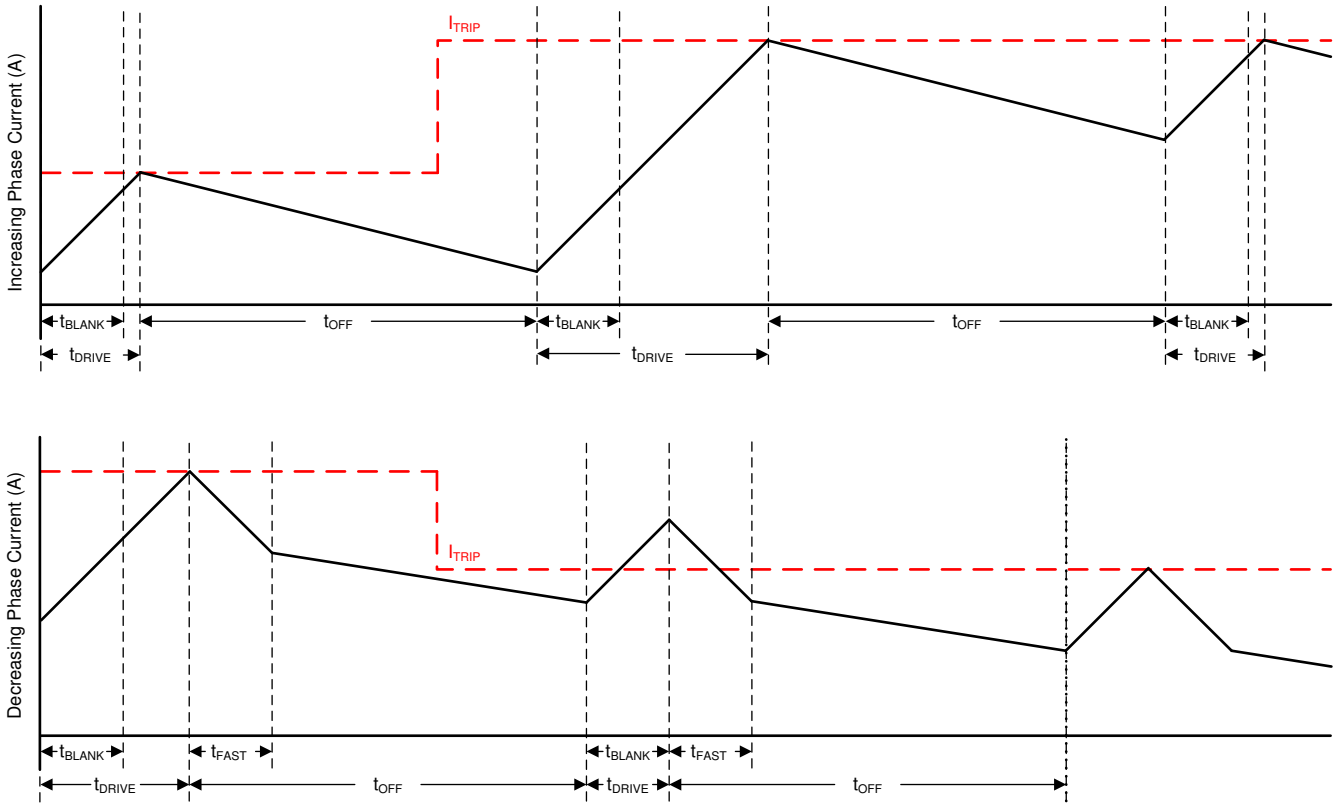


Figure 7-10. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.3 Mixed Decay for Increasing and Decreasing Current

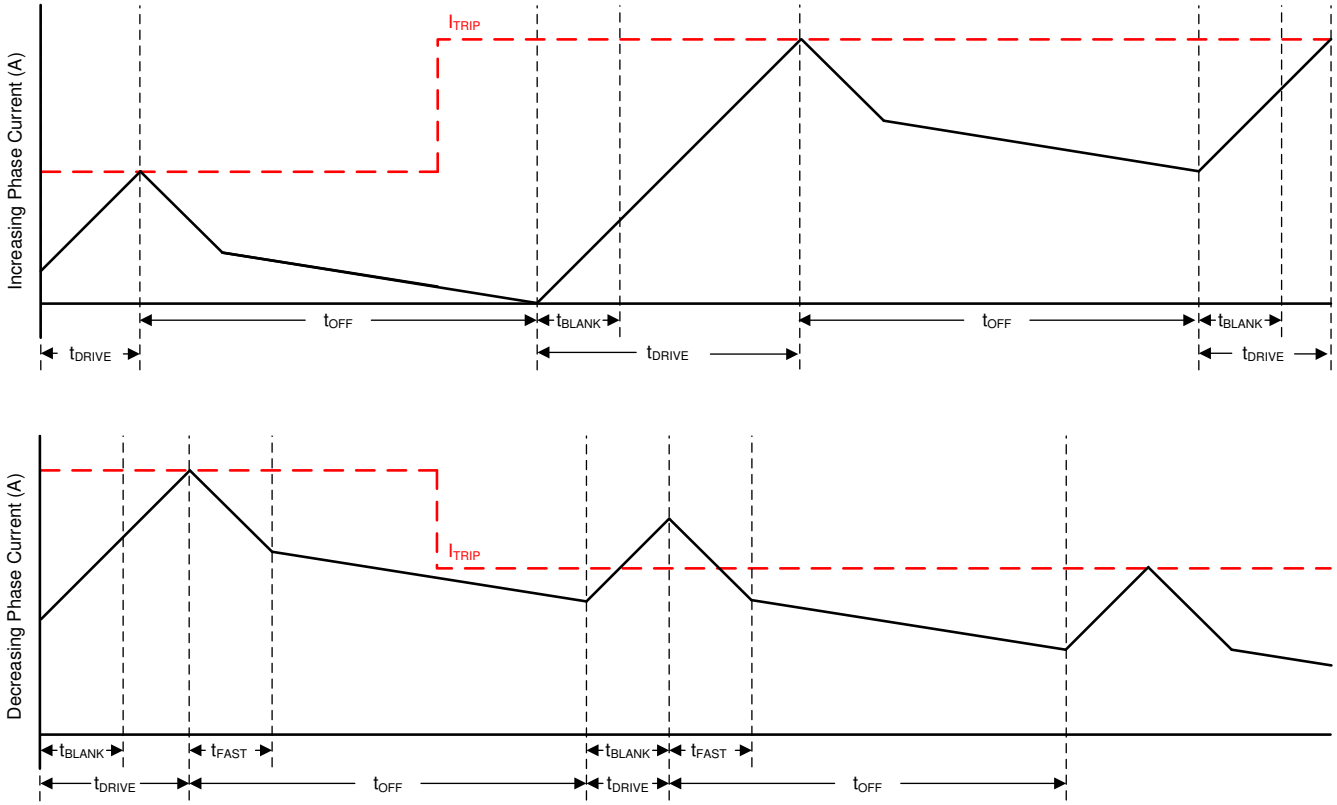


Figure 7-11. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

7.3.6.4 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

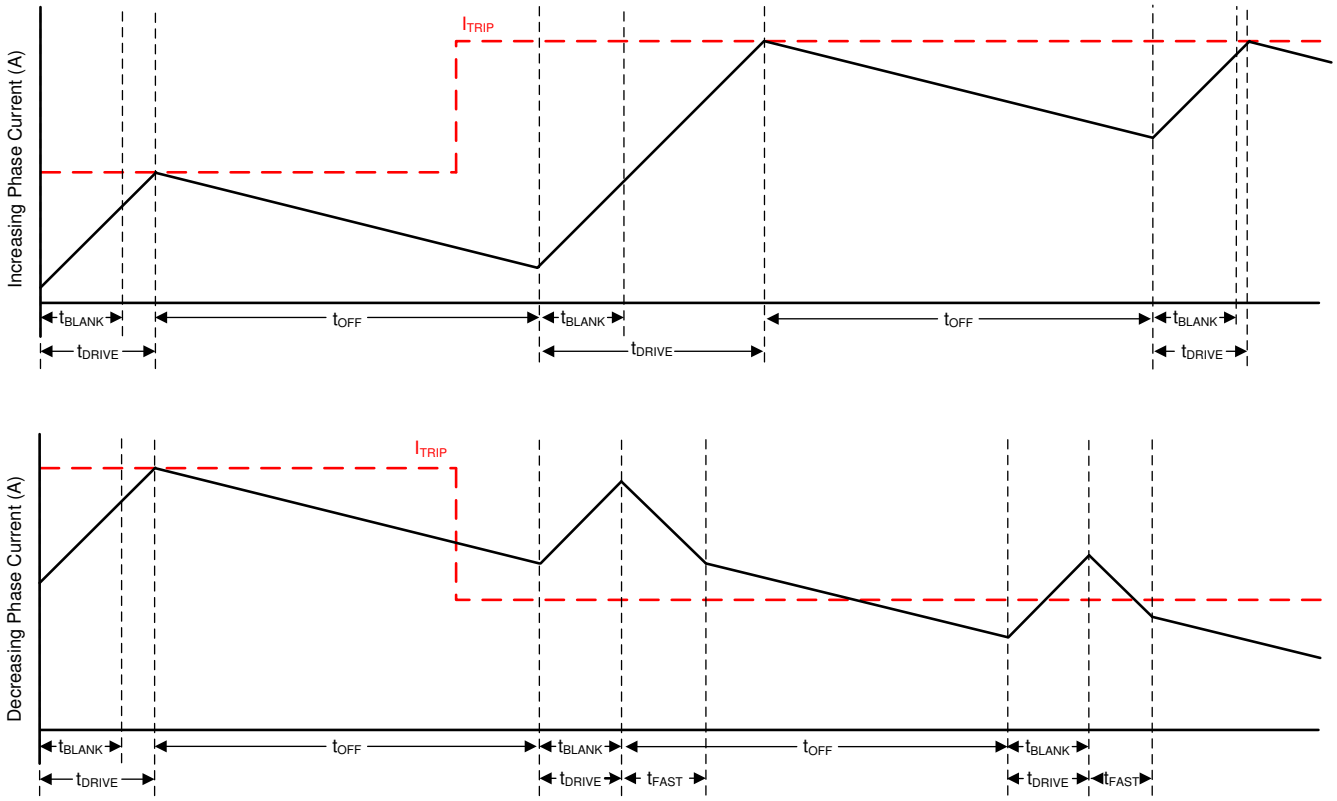


Figure 7-12. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.3.6.5 Smart tune Ripple Control

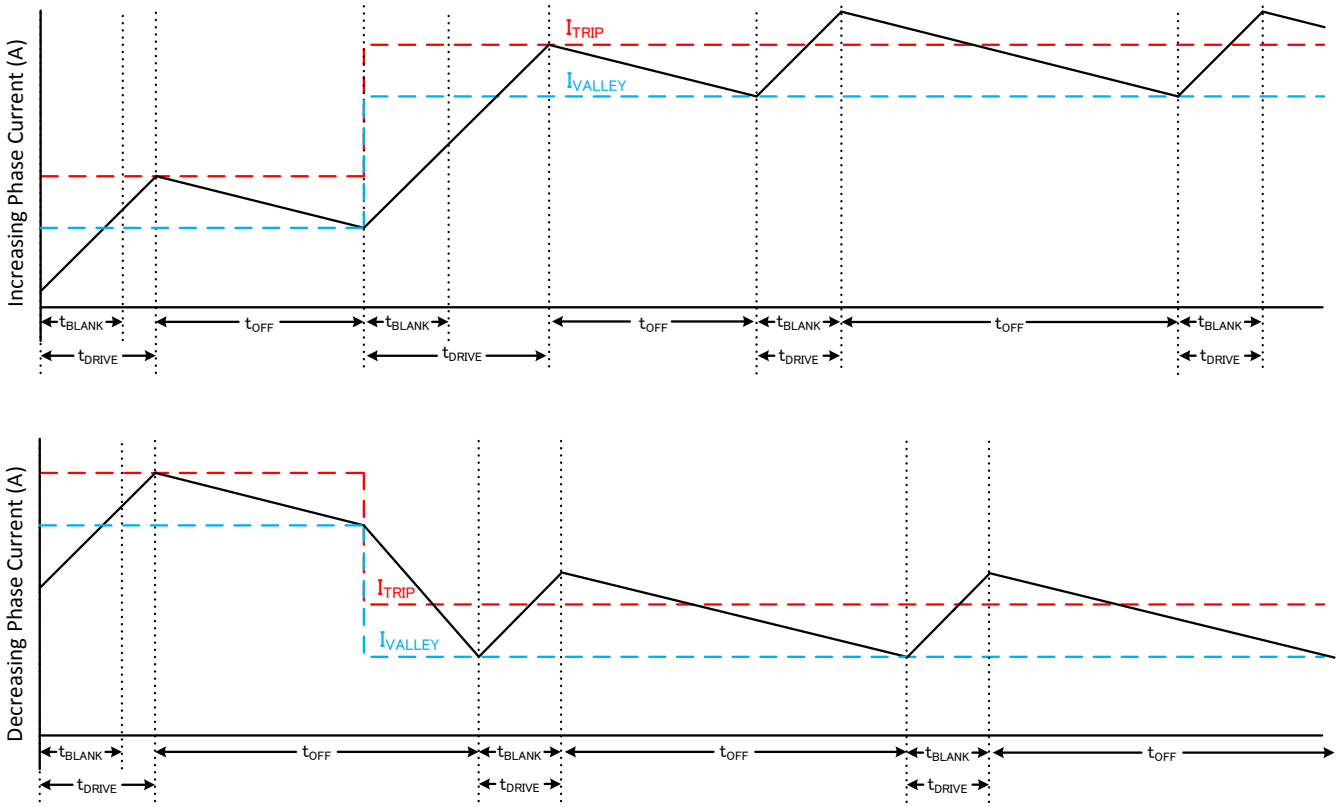


Figure 7-13. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

The ripple current in this decay mode is programmed by the TOFF pin. The ripple current is dependent on the ITRIP of a particular microstep level.

Table 7-8. Current Ripple Settings

TOFF	Current Ripple at a specific microstep level
0	19mA + 1% of ITRIP
1	19mA + 2% of ITRIP
Hi-Z	19mA + 4% of ITRIP
330kΩ to GND	19mA + 6% of ITRIP

The ripple control method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation. Select a low ripple current setting to ensure that the PWM frequency is not in the audible range. However, higher values of ripple current reduces the PWM frequency and therefore the switching loss.

7.3.6.6 PWM OFF Time

The TOFF pin configures the PWM OFF time for all decay modes except smart tune ripple control, as shown in Table 7-7. The OFF time settings can be changed on the fly. After a OFF time setting change, the new OFF time is applied after a 10 µs de-glitch time.

Table 7-9. OFF Time Settings

TOFF	OFF Time
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

7.3.6.7 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

7.3.7 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

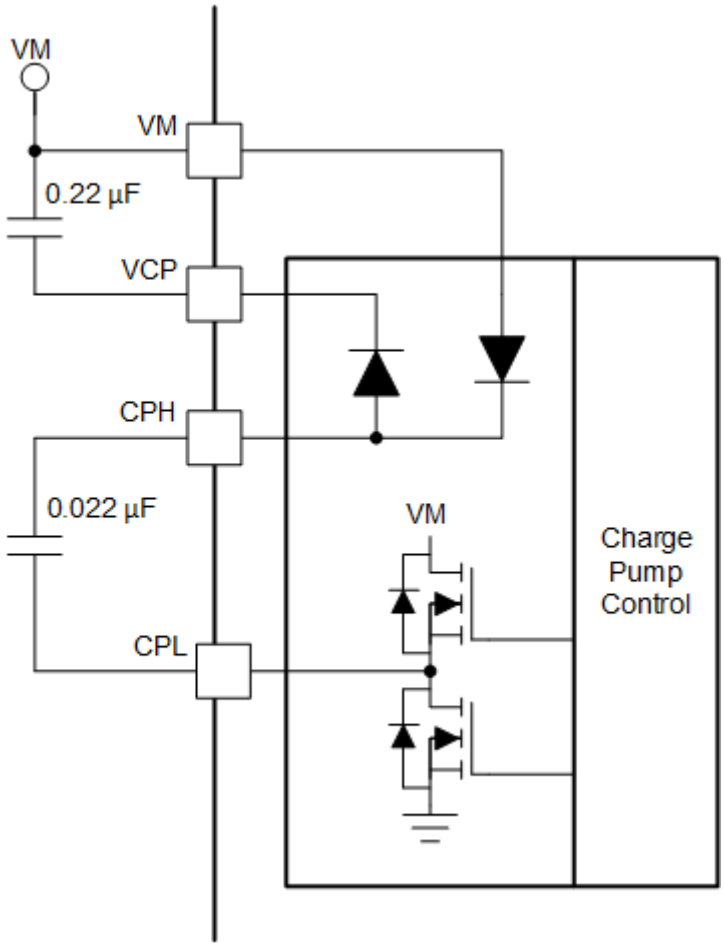


Figure 7-14. Charge Pump Block Diagram

7.3.8 Linear Voltage Regulators

A linear voltage regulator is integrated in the DRV8424/25 devices. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2mA, the output voltage drops significantly.

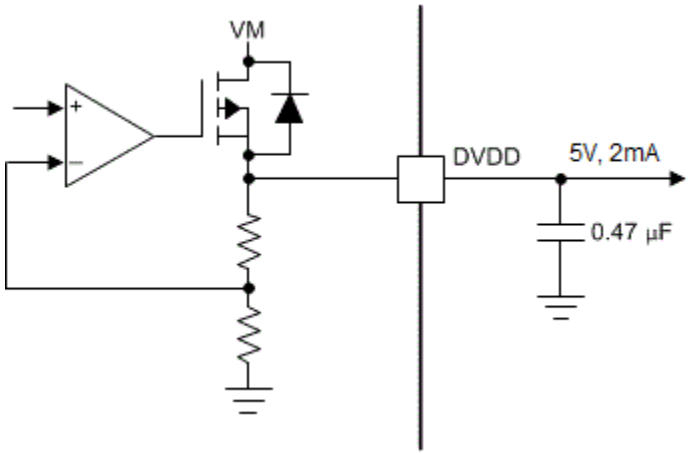


Figure 7-15. Linear Voltage Regulator Block Diagram

Figure 7-16. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, Mx, DECAYx or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.9 Logic Level, tri-level and quad-level Pin Diagrams

Figure 7-17 shows the input structure for M0, DECAY0, DECAY1 and ENABLE pins.

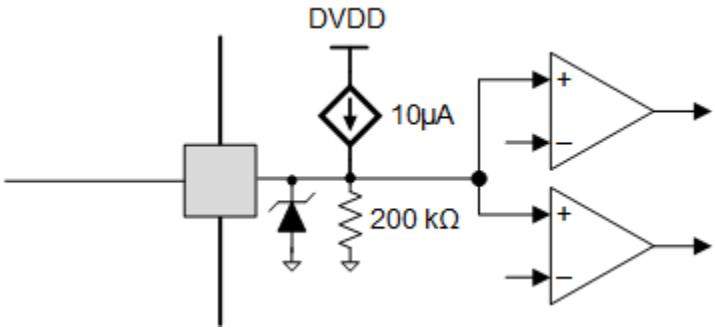


Figure 7-17. Tri-Level Input Pin Diagram

Figure 7-17 shows the input structure for M1 and TOFF pins.

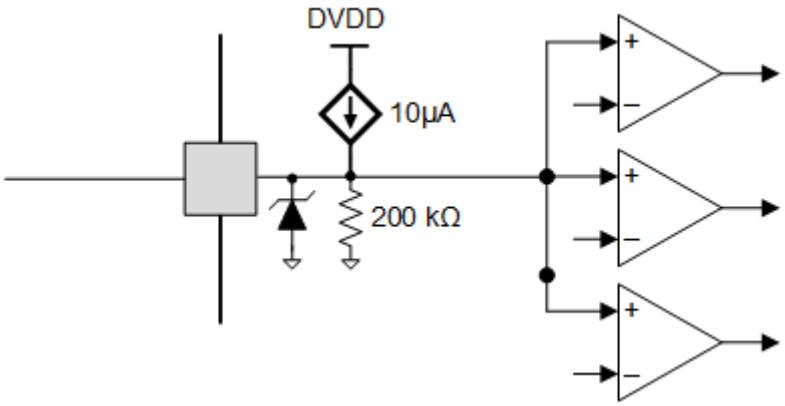


Figure 7-18. Quad-Level Input Pin Diagram

Figure 7-19 shows the input structure for STEP, DIR and nSLEEP pins.

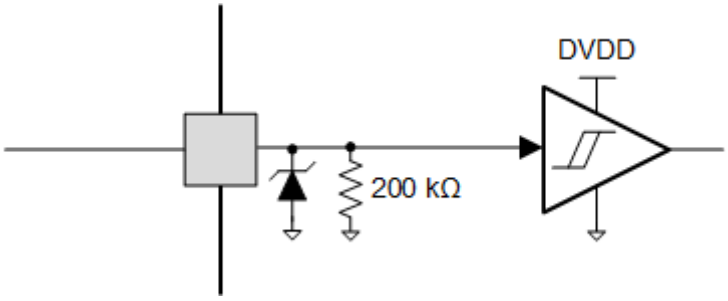


Figure 7-19. Logic-Level Input Pin Diagram

7.3.10 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

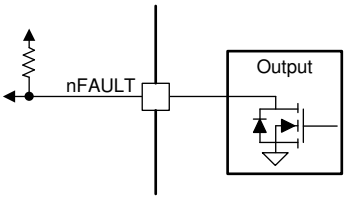


Figure 7-20. nFAULT Pin

7.3.11 Protection Circuits

The DRV8424/25 devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.11.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.11.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in both H-bridges are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry. The operating modes can be changed on the fly.

7.3.11.3.1 Latched Shutdown

The ENABLE pin of the DRV8424/25 has to be made Hi-Z to select latched shutdown mode. In this mode, after an OCP event, the outputs are disabled and the nFAULT pin is driven low. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.11.3.2 Automatic Retry

The ENABLE pin of the DRV8424/25 has to be HIGH (>2.7V) to select automatic retry mode. In this mode, after an OCP event the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.11.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled during this condition. The thermal shutdown protection can operate in two different modes: latched shutdown and automatic retry. The operating modes can be changed on the fly.

7.3.11.4.1 Latched Shutdown

The ENABLE pin of the DRV8424/25 has to be made Hi-Z to select latched shutdown mode. In this mode, after an OTSD event, the relevant outputs are disabled and the nFAULT pin is driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.11.4.2 Automatic Retry

The ENABLE pin of the DRV8424/25 has to be HIGH (>2.7V) to select automatic retry mode. In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

7.3.11.5 Fault Condition Summary

Table 7-10. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	—	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	—	nFAULT	Disabled	Operating	Operating	Operating	Automatic: VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	ENABLE = Hi-Z	nFAULT	Disabled	Operating	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}

Table 7-10. Fault Condition Summary (continued)

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
Thermal Shutdown (OTSD)	$T_J > T_{TSD}$	ENABLE = Hi-Z	nFAULT	Disabled	Disabled	Operating	Operating	Latched
		ENABLE = 1	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: $T_J < T_{OTSD} - T_{HYS\_OTSD}$

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The DRV8424/25 device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the DRV8424/25 device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The DRV8424/25 device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the DRV8424/25. When the ENABLE pin is low, the output drivers are disabled in the Hi-Z state.

7.4.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.4 nSLEEP Reset Pulse

A latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7-21). This reset pulse does not affect the status of the charge pump or other functional blocks.

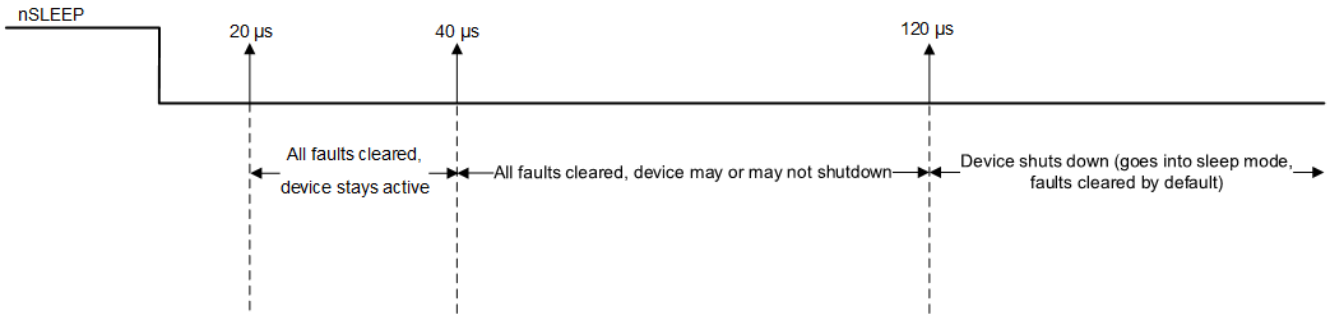


Figure 7-21. nSLEEP Reset Pulse

7.4.5 Functional Modes Summary

Table 7-11 lists a summary of the functional modes.

Table 7-11. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 33 V	nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 33 V	nSLEEP pin = 1 ENABLE pin = 1 or Hi-Z	Operating	Operating	Operating	Operating	Operating

Table 7-11. Functional Modes Summary (continued)

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Disabled	4.5 V < VM < 33 V	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8424 is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8424.

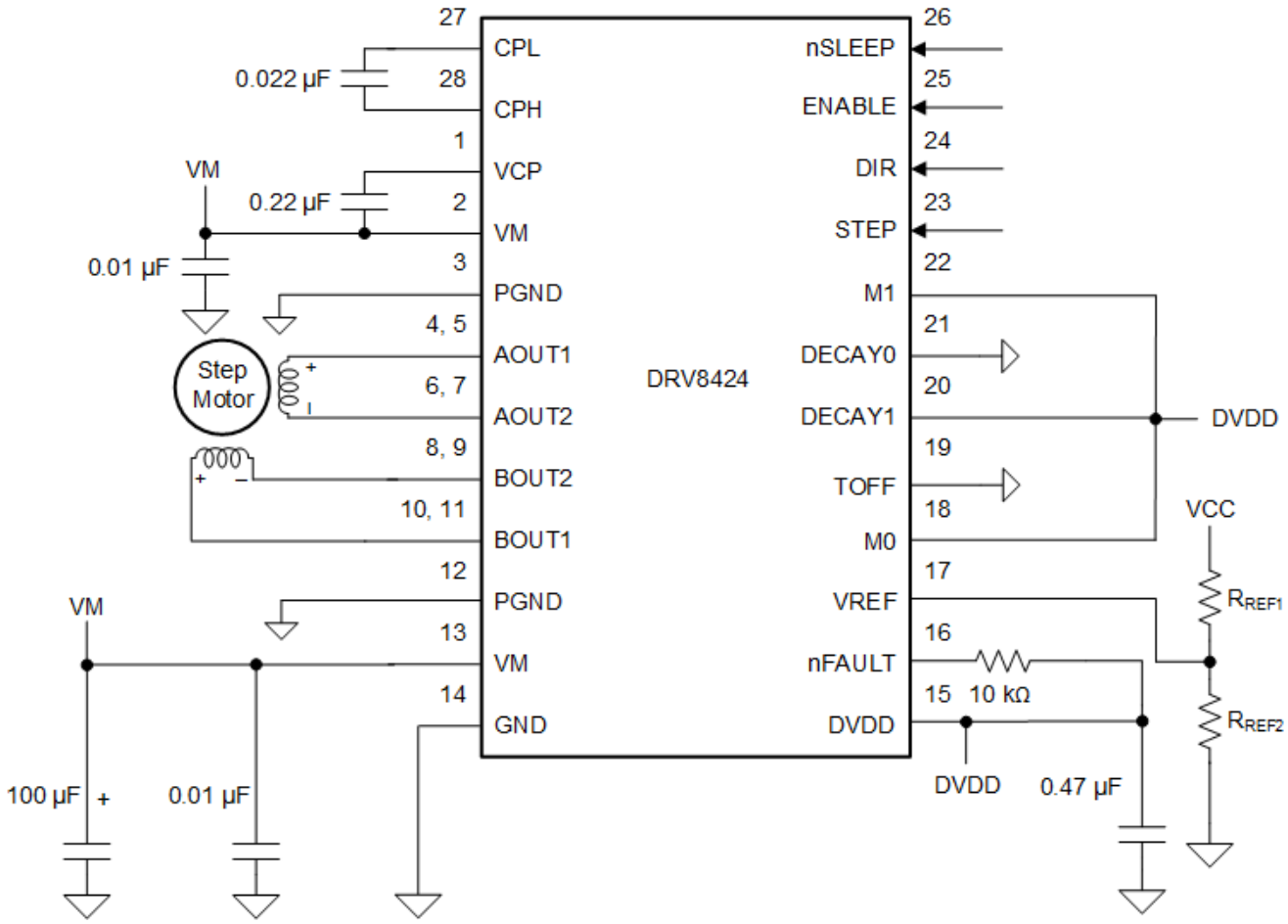


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for a typical application.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	1.5 Ω/phase

Table 8-1. Design Parameters (continued)

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor winding inductance	L_L	2 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	18.75 rpm
Target full-scale current	I_{FS}	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8424/25 device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 1 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps}/\text{s}) = \frac{\text{v}\ (\text{rpm}) \times 360\ (^\circ/\text{rot})}{\theta_{step}\ (^\circ/\text{step}) \times n_m\ (\text{steps}/\text{microstep}) \times 60\ (\text{s}/\text{min})} \quad (1)$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor. For example, the motor in this application is required to rotate at 1.8°/step for a target of 18.75 rpm at 1/8 microstep mode. Using Equation 1, f_{step} can be calculated as 500 Hz.

The microstepping level is set by the M0 and M1 pins and can be any of the settings listed in Table 8-2. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed.

Table 8-2. Microstepping Indexer Settings

MODE0	MODE1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

8.2.2.2 Current Regulation

When an output load is connected to the VM supply, the load current can be regulated to the I_{TRIP} level. The I_{TRIP} current level for OUT1 and OUT2 outputs is controlled by the VREF12 pin, and the I_{TRIP} level for OUT3 and OUT4 outputs is controlled by the VREF34 pin. The I_{TRIP} current can be calculated as I_{TRIP} (A) = VREF (V) / 1.32 (V/A). The VREF voltage can be programmed by connecting resistor dividers from DVDD pin to ground. Both VREF pins can be tied together to program the same ITRIP current for all four output channels.

8.2.2.3 Decay Modes

The DRV8424/25 device supports six different decay modes, as shown in Table 7-7. When a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8424/25 places the winding in one of the six decay modes for t_{OFF}. After t_{OFF}, a new drive phase starts.

8.2.3 Application Curves

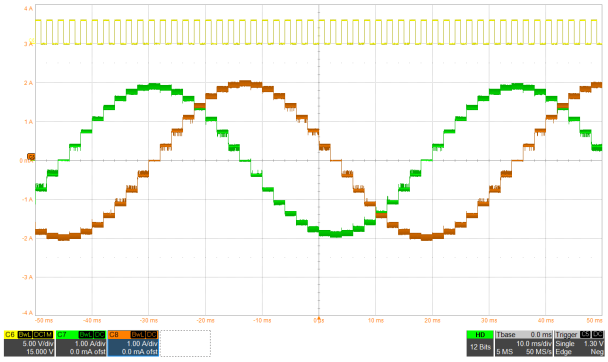


Figure 8-2. 1/8 Microstepping With smart tune Ripple Control Decay

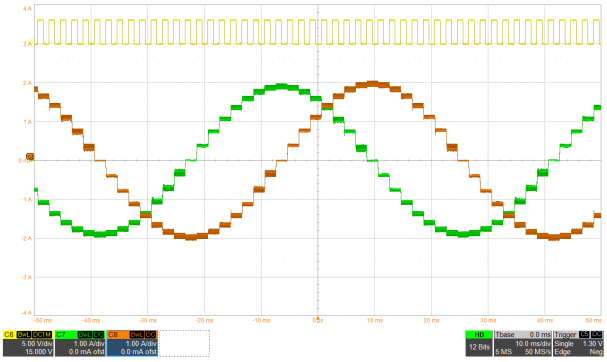


Figure 8-3. 1/8 Microstepping With smart tune Dynamic Decay

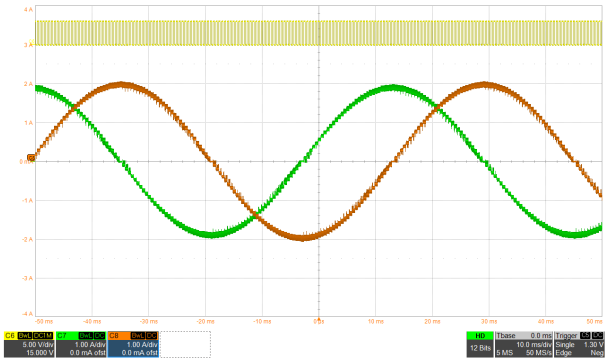


Figure 8-4. 1/32 Microstepping With smart tune Ripple Control Decay

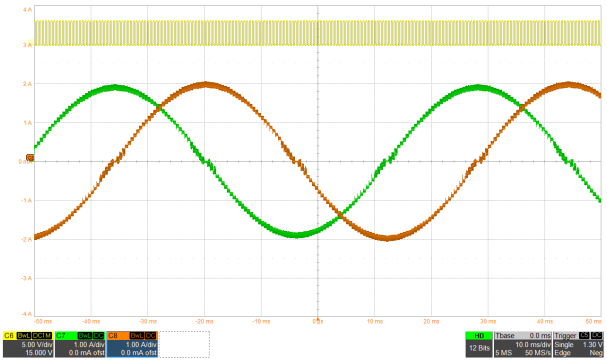


Figure 8-5. 1/32 Microstepping With smart tune Dynamic Decay

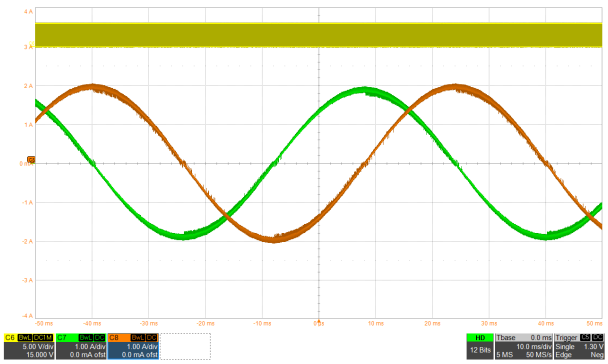


Figure 8-6. 1/256 Microstepping With smart tune Ripple Control Decay

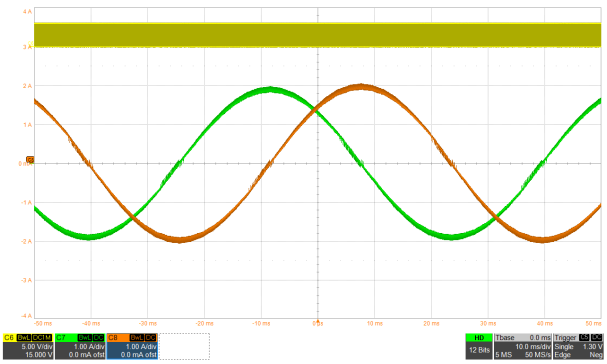


Figure 8-7. 1/256 Microstepping With smart tune Dynamic Decay

8.2.4 Thermal Application

This section presents the power dissipation calculation and junction temperature estimation of the device.

8.2.4.1 Power Dissipation

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

8.2.4.1.1 Conduction Loss

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of the other half-bridge. The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 2.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (2)$$

The conduction loss for the typical application shown in Table 8-2 is calculated in Equation 3.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (2\text{-A} / \sqrt{2})^2 \times (0.165\text{-}\Omega + 0.165\text{-}\Omega) = 1.32\text{-W} \quad (3)$$

Note

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side on-resistance of the FETs. For more accurate calculation, consider the dependency of on-resistance of FETs with device temperature.

8.2.4.1.2 Switching Loss

The power loss due to the PWM switching frequency depends on the slew rate (t_{SR}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 4 and Equation 5.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE\_PWM} \times f_{PWM} \quad (4)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL\_PWM} \times f_{PWM} \quad (5)$$

Both t_{RISE_PWM} and t_{FALL_PWM} can be approximated as V_{VM}/ t_{SR}. After substituting the values of various parameters, and assuming 30-kHz PWM frequency, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (2\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.051\text{-W} \quad (6)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (2\text{-A} / \sqrt{2}) \times (24\text{-V} / 240\ \text{V/µs}) \times 30\text{-kHz} = 0.051\text{-W} \quad (7)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.051\text{-W} + 0.051\text{-W}) = 0.204\text{-W} \quad (8)$$

Note

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (t_{SR}). This parameter is expected to change based on the supply-voltage, temperature and device to device variation.

The switching loss is directly proportional to the PWM switching frequency. The PWM frequency in an application will depend on the supply voltage, inductance of the motor coil, back emf voltage and OFF time or the ripple current (for smart tune ripple control decay mode).

8.2.4.1.3 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (9)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (10)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variation.

8.2.4.1.4 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 11.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 1.32\text{-W} + 0.204\text{-W} + 0.12\text{-W} = 1.644\text{-W} \quad (11)$$

8.2.4.2 Device Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as $T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 31 °C/W for the HTSSOP package and 40.7 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°C + (1.644\text{-W} \times 31°C/W) = 75.96\ °C \quad (12)$$

The junction temperature for the VQFN package is calculated as shown below -

$$T_J = 25°C + (1.644\text{-W} \times 40.7°C/W) = 91.91\ °C \quad (13)$$

9 Power Supply Recommendations

The DRV8424/25 device is designed to operate from an input voltage supply (VM) range from 4.5 V to 33 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8424/25 device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

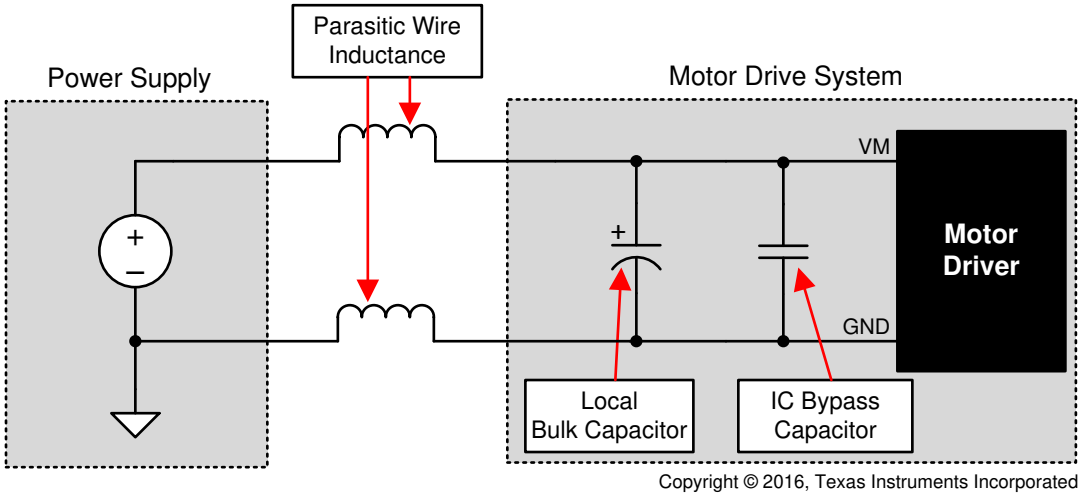


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.2 Layout Example

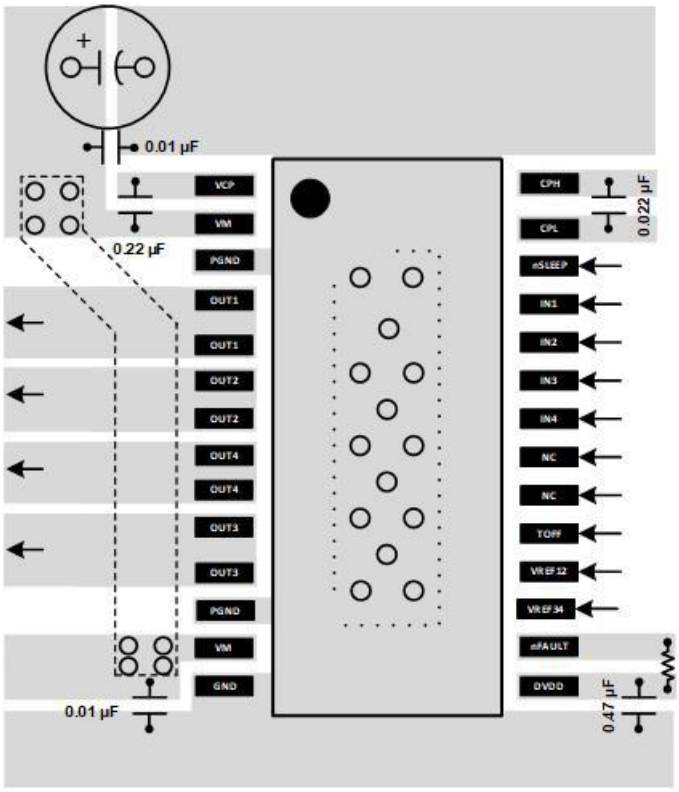


Figure 10-1. HTSSOP Layout Example

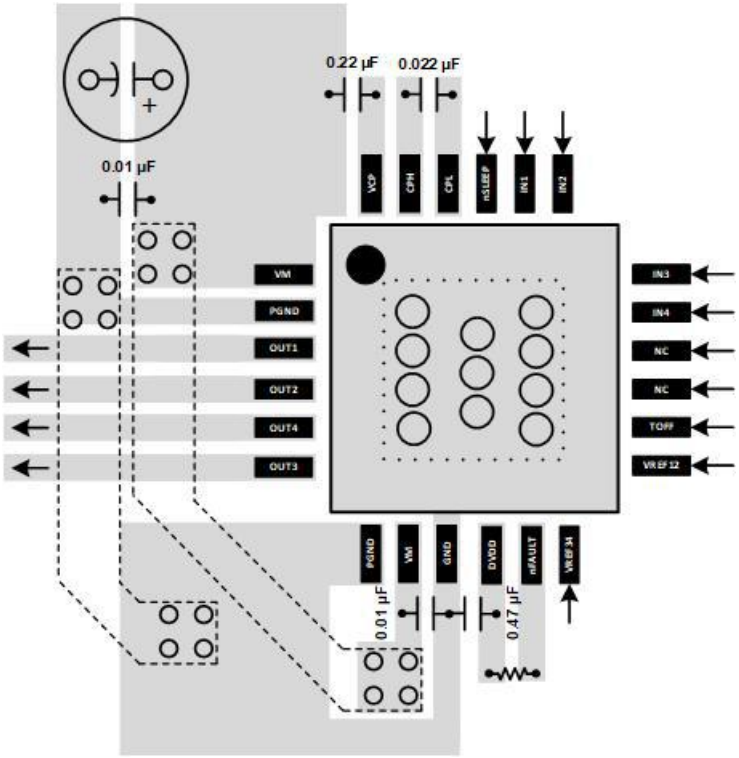


Figure 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8424	Click here	Click here	Click here	Click here	Click here
DRV8425	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

12 Mechanical, Packaging, and Orderable Information

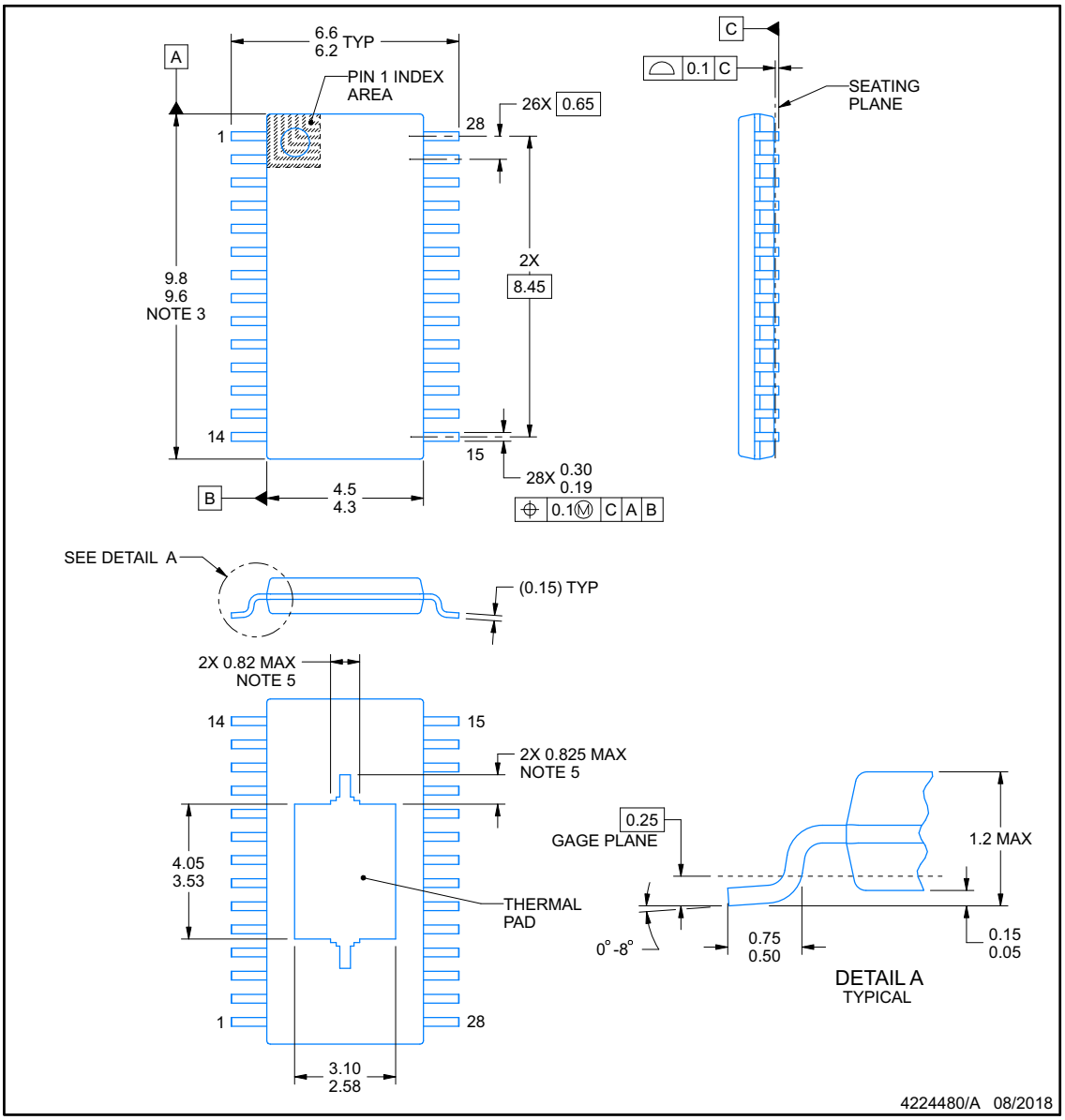
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

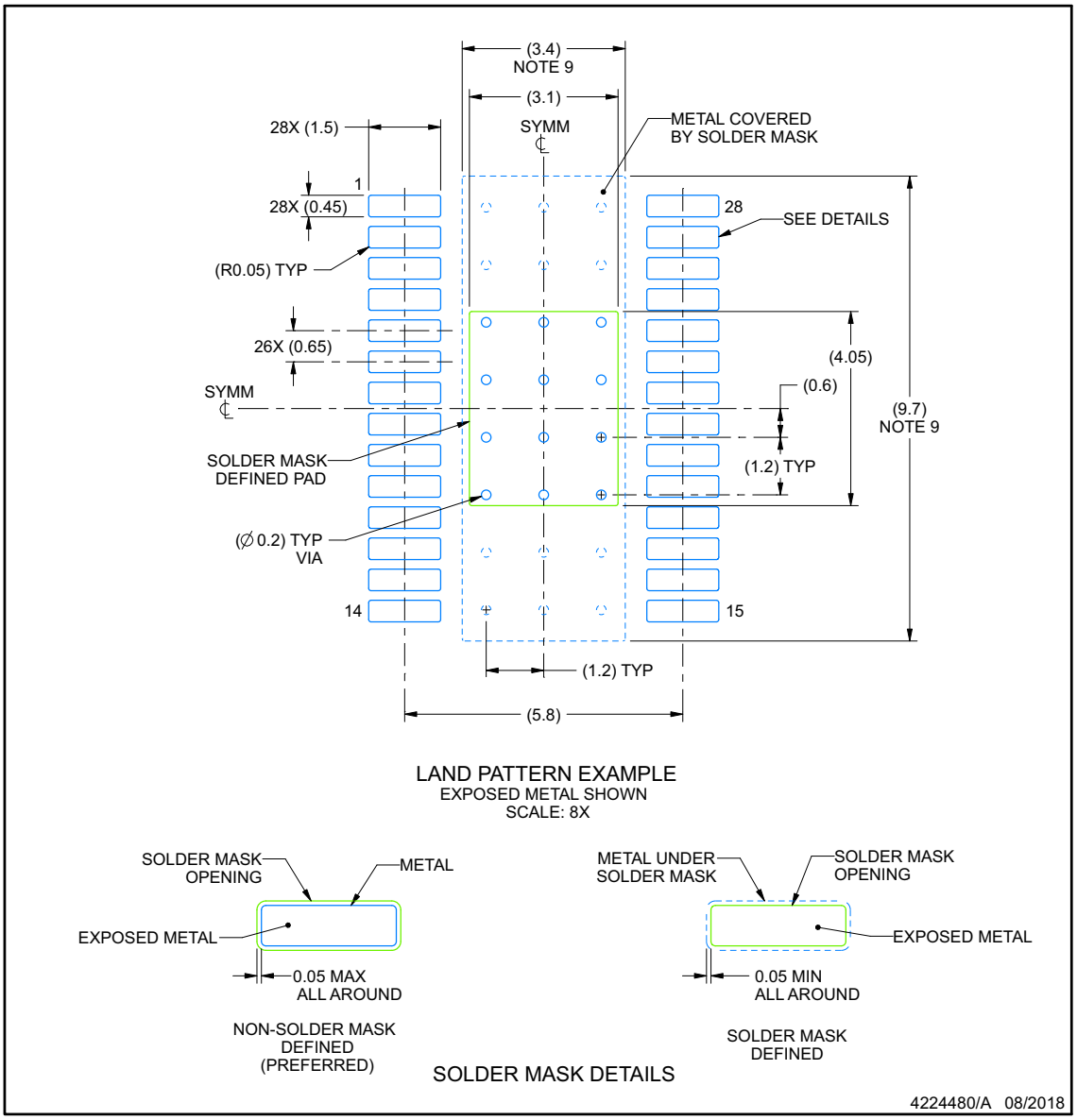
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



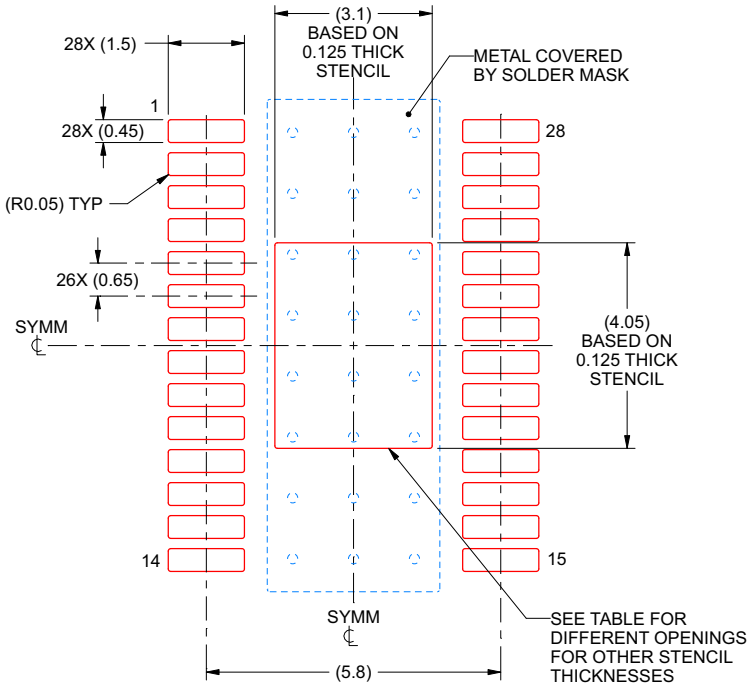
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8424PWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8424	Samples
DRV8424RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8424	Samples
DRV8425PWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8425	Samples
DRV8425RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 8425	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

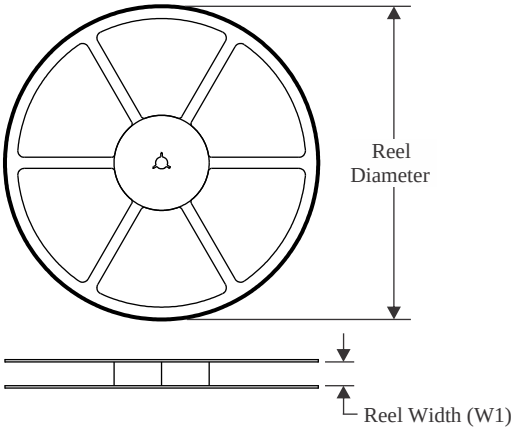
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

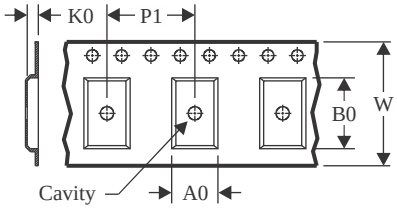
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

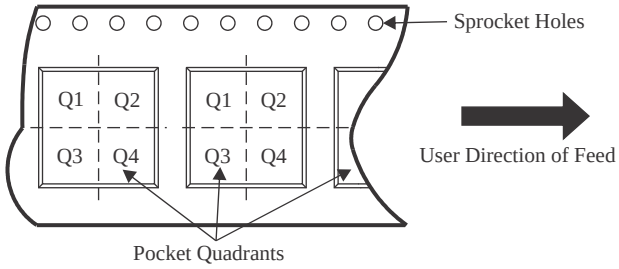


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

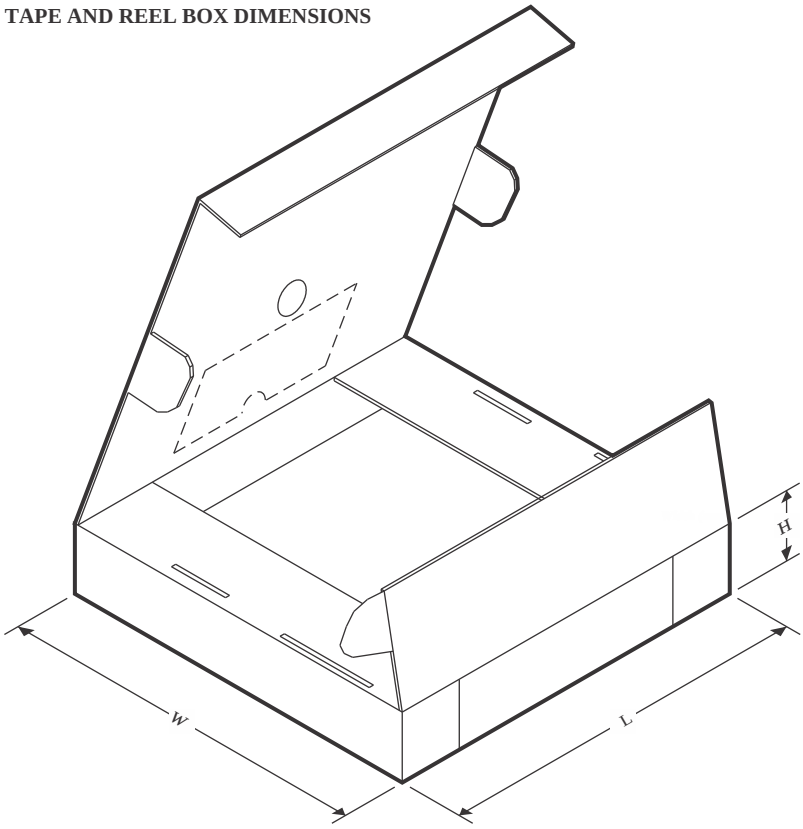
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8424PWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8424RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8425PWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8425RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



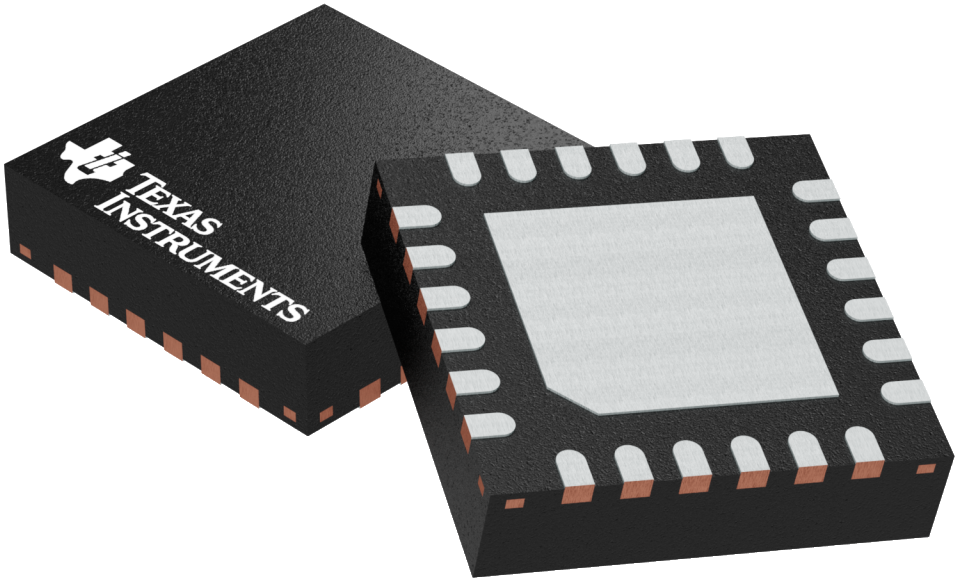
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8424PWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8424RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8425PWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8425RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



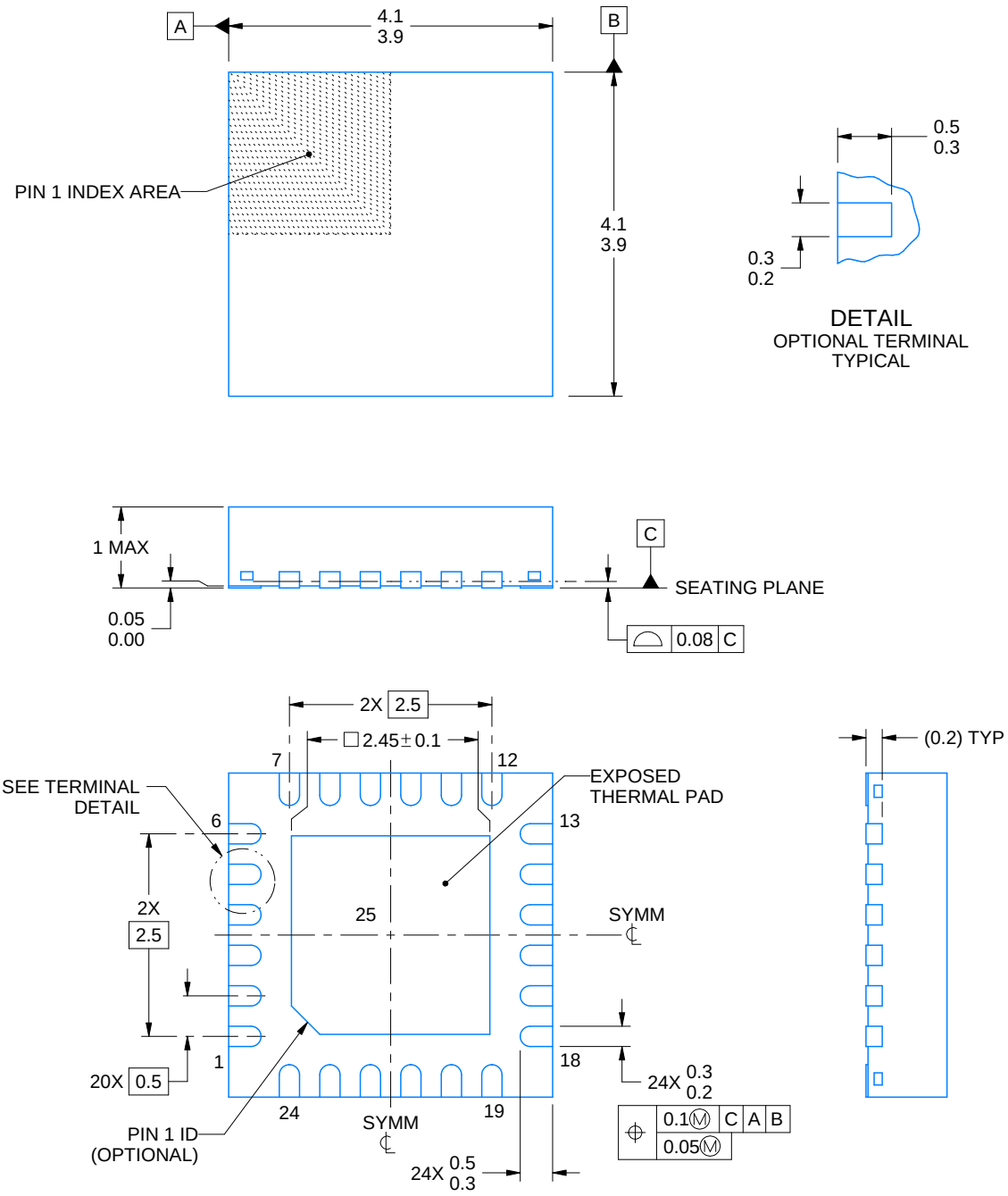
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGE0024B

PACKAGE OUTLINE

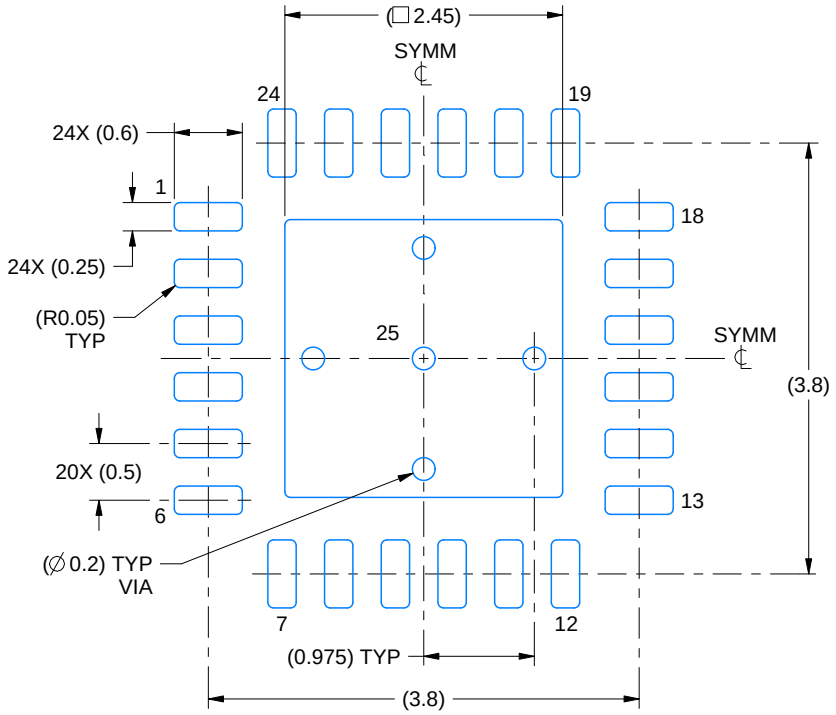
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

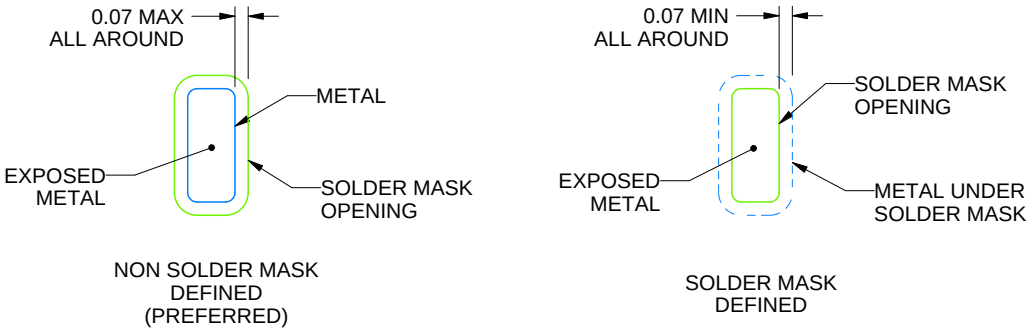


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

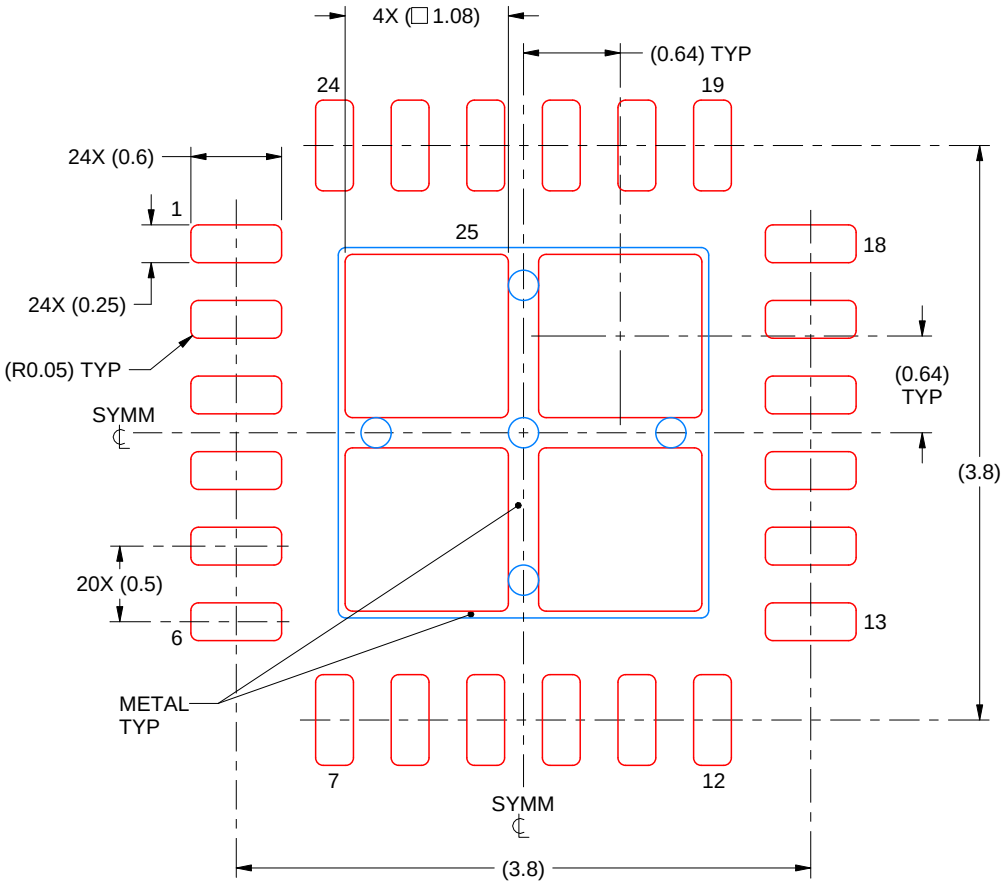


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

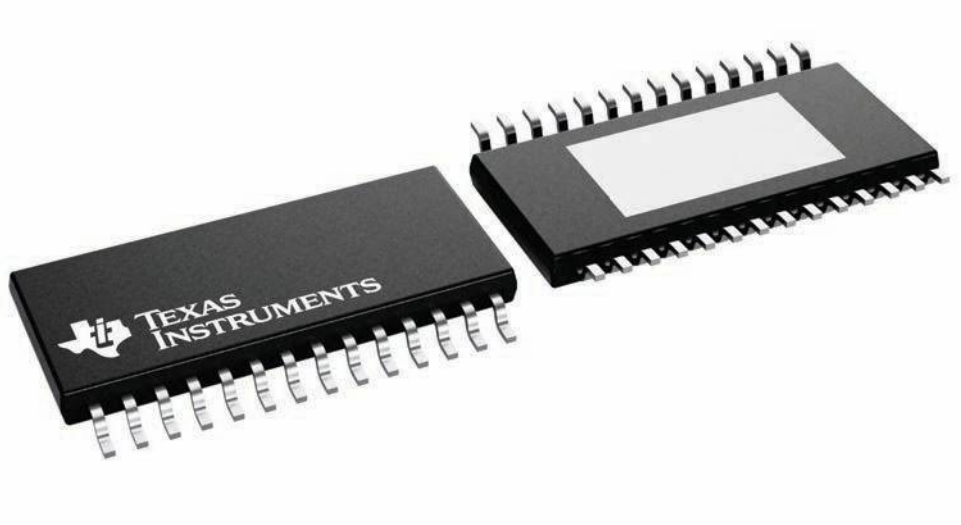
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

DRV8962 Four-channel Half-Bridge Driver with Current Sense Outputs

1 Features

- Four-channel half-bridge driver
  - **Independent control** of each half-bridge
- **4.5 V to 65 V** operating supply voltage range
- Low $R_{DS(ON)}$: **50 mΩ** for each FET (24 V, 25 °C)
- High current capacity:
  - DDW package: Up to **5-A per output**
  - DDV package: Up to **10-A per output**
- Can drive various types of loads -
  - Up to four solenoid loads
  - One stepper motor
  - Two brushed-DC motors
  - One or two thermoelectric coolers (TEC)
  - One 3-phase brushless-DC motor
  - One 3-phase permanent magnet synchronous motor (PMSM)
- Integrated current sense and regulation
  - Current sensing across high-side MOSFETs
  - Sense output (**IPROPI**) for each half-bridge
  - **± 4%** sense accuracy at maximum current
  - Optional external sense resistor
- Pin-to-pin compatible with:
  - DRV8952: 48V, four-channel half-bridge driver
- Separate logic supply voltage (**VCC**)
- Programmable output rise/fall time
- Programmable fault recovery method
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (3 µA)
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Factory Automation, Stepper Drives and Robotics
- Medical Imaging, Diagnostics and Equipment
- Stage Lighting
- PLCs
- TEC Drivers
- BLDC Motor Modules
- Brushed-DC and Stepper Motor drivers

3 Description

The DRV8962 is a wide-voltage, high-power, four-channel half-bridge driver for a wide variety of industrial applications. The device supports up to 65-V supply voltage, and integrated MOSFETs with 50 mΩ on-resistance allow up to 5-A current on each output with the DDW package; and up to 10-A current per output with the DDV package.

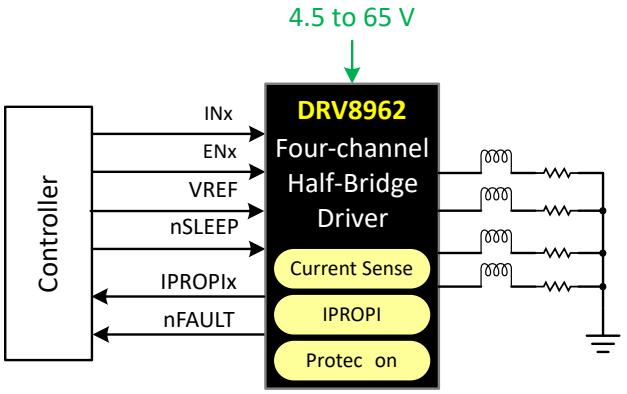
The device can be used for driving up to four solenoid loads, one stepper motor, two brushed-DC motors, one BLDC or PMSM motor and up to two thermoelectric coolers (Peltier elements). The output stage of the device consists of N-channel power MOSFETs configured as four independent half-bridges, charge pump regulator, current sensing and regulation circuits, current sense outputs and protection circuitry.

Integrated current sensing across the high-side MOSFETs allows the device to regulate the current when the load is connected from output to ground. A regulation current limit can be set with an adjustable external voltage reference (VREF). Additionally, the device provides four proportional current output pins, one for each half-bridge high-side FET. Optional external sense resistors can also be connected from the PGND pins to the system ground.

A low-power sleep mode is provided to achieve ultra-low quiescent current. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output over current (OCP), and device overtemperature (OTSD).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DRV8962DDWR	HTSSOP (44), bottom exposed pad	14 mm x 6.1 mm
DRV8962DDVR	HTSSOP (44), top exposed pad	14 mm x 6.1 mm



DRV8962 Simplified Schematic

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
	*	Initial Release

5 Pin Configuration and Functions

The DRV8962 is available in thermally-enhanced, 44-Pin HTSSOP packages.

- The DDW package contains a PowerPAD™ on the bottom side of the device.
- The DDV package contains a PowerPAD™ on the top side of the device for thermal coupling to a heatsink.

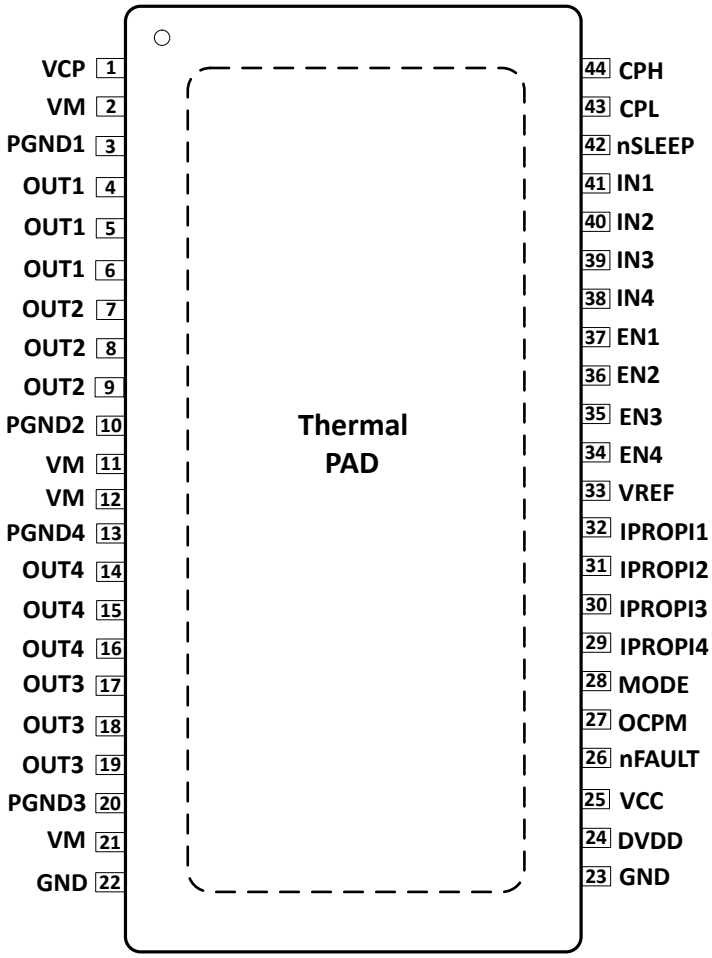


Figure 5-1. DDW Package, Top View

ADVANCE INFORMATION

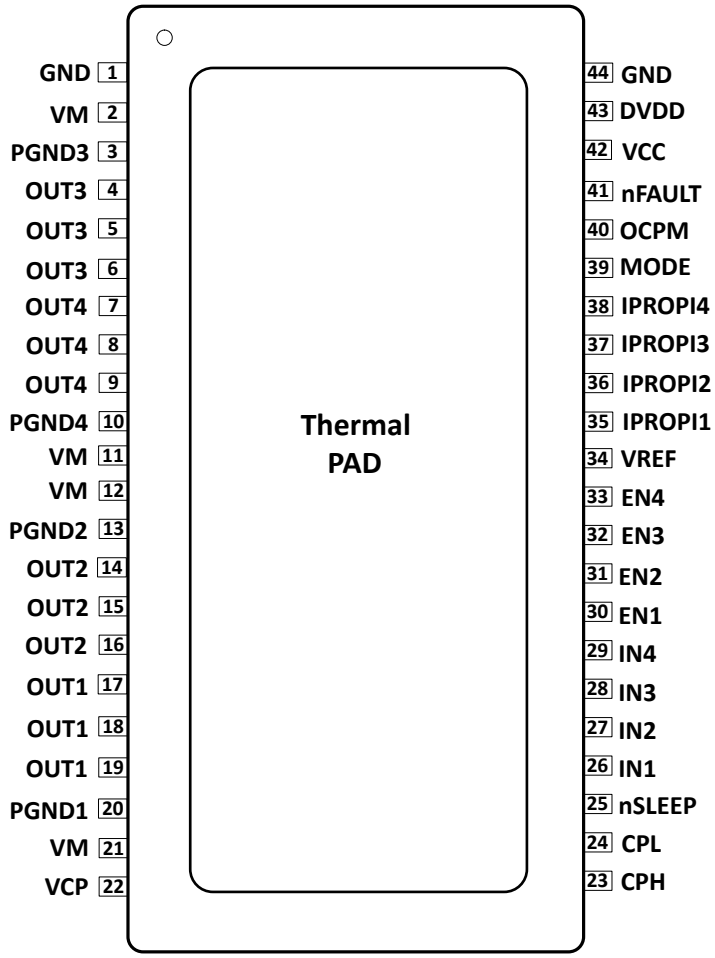


Figure 5-2. DDV Package, Top View

PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
VCP	1	22	Power	Charge pump output. Connect a X7R, 1-µF, 16-V ceramic capacitor from VCP to VM.
VM	2, 11, 12, 21	2, 11, 12, 21	Power	Power supply. Connect to motor supply voltage and bypass to PGND pins with 0.01-µF ceramic capacitors plus a bulk capacitor rated for VM.
PGND1	3	20	Power	Power ground for half-bridge 1. Connect to system ground.
PGND2	10	13	Power	Power ground for half-bridge 2. Connect to system ground.
PGND3	20	3	Power	Power ground for half-bridge 3. Connect to system ground.
PGND4	13	10	Power	Power ground for half-bridge 4. Connect to system ground.
OUT1	4, 5, 6	17, 18, 19	Output	Connect to load terminal.
OUT2	7, 8, 9	14, 15, 16	Output	Connect to load terminal.
OUT3	17, 18, 19	4, 5, 6	Output	Connect to load terminal.
OUT4	14, 15, 16	7, 8, 9	Output	Connect to load terminal.
IPROPI1	32	35	Output	Current sense output for half-bridge 1.
IPROPI2	31	36	Output	Current sense output for half-bridge 2.
IPROPI3	30	37	Output	Current sense output for half-bridge 3.
IPROPI4	29	38	Output	Current sense output for half-bridge 4.

PIN			TYPE	DESCRIPTION
NAME	DDW	DDV		
EN1	37	30	Input	Enable input of half-bridge 1.
EN2	36	31	Input	Enable input of half-bridge 2.
EN3	35	32	Input	Enable input of half-bridge 3.
EN4	34	33	Input	Enable input of half-bridge 4.
IN1	41	26	Input	PWM input for half-bridge 1.
IN2	40	27	Input	PWM input for half-bridge 2.
IN3	39	28	Input	PWM input for half-bridge 3.
IN4	38	29	Input	PWM input for half-bridge 4.
GND	22, 23	1, 44	Power	Device ground. Connect to system ground.
CPH	44	23	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM rated ceramic capacitor from CPH to CPL.
CPL	43	24		
VREF	33	34	Input	Voltage reference input for setting current regulation threshold. DVDD can be used to provide VREF through a resistor divider.
DVDD	24	43	Power	Internal LDO output. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCC	25	42	Power	Supply voltage for internal logic blocks. When separate logic supply voltage is not available, tie the VCC pin to the DVDD pin.
nFAULT	26	41	Open Drain	Fault indication output. Pulled logic low with fault condition. Open drain output requires an external pullup resistor.
MODE	28	39	Input	This pin programs the output rise/fall time.
OCPM	27	40	Input	Determines the fault recovery method. Depending on the OCPM voltage, fault recovery can be either latch-off or auto-retry type.
nSLEEP	42	25	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. A narrow nSLEEP reset pulse clears latched faults.
PAD	-	-	-	Thermal pad.

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	70	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 5.75	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
IPROPI pin voltage (IPROPI)	-0.3	DVDD + 0.3	V
Control pin voltage	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 µs	-2.5	2.5	V
Continuous OUTx pin voltage	–1	V_{VM} + 1	V
Transient 100 ns OUTx pin voltage	–3	V_{VM} + 3	V
Peak drive current	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

- Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to network ground terminal GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	Corner pins	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	65	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
f_{PWM}	Applied PWM signal	0	200	kHz
I_{DDW}	Current per output, DDW Package	0	5	A

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{DDV}	Current per output, DDV Package	0	10	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC		DDW	DDV	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.2	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.1	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	18.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	N/A	°C/W

ADVANCE INFORMATION

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No load, VCC = External 5V		4	7	mA
		nSLEEP = 1, No load, VCC = DVDD		6	9	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 65 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 65 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, EN1, EN2, EN3, EN4, MODE, OCPM, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = DVDD			50	µA
t_1	ENx high to OUTx high delay	INx = 1			2	µs
t_2	ENx low to OUTx low delay	INx = 1			2	µs
t_3	ENx high to OUTx low delay	INx = 0			2	µs
t_4	ENx low to OUTx high delay	INx = 0			2	µs
t_5	INx high to OUTx high delay			600		ns
t_6	INx low to OUTx low delay			600		ns
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -5 A		50	60	mΩ
		T_J = 125 °C, I_O = -5 A		75	90	mΩ
		T_J = 150 °C, I_O = -5 A		85	105	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		50	60	mΩ
		T_J = 125 °C, I_O = 5 A		75	90	mΩ
		T_J = 150 °C, I_O = 5 A		85	105	mΩ
t_{RF}	Output rise/fall time	I_O = 5 A, MODE = 1, between 10% and 90%		70		ns
		I_O = 5 A, MODE = 0, between 10% and 90%		140		ns
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns

ADVANCE INFORMATION

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror gain			212		µA/A
A_{ERR}	Current mirror scaling error	10% to 20% rated current	-8.5		8.5	%
		20% to 40% rated current	-5		5	
		40% to 100% rated current	-4		4	
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			100	nA
t_{OFF}	PWM off-time			16		µs
t_{DEG}	Current regulation deglitch time			0.5		µs
t_{BLK}	Current Regulation Blanking time			1.5		µs
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.35	4.45	
VCC_{UVLO}	VCC UVLO lockout	VCC falling	2.7	2.8	2.9	V
		VCC rising	2.8	2.9	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET, DDW Package	8			A
		Current through any FET, DDV Package	16			A
t_{OCP}	Overcurrent detection delay			2		µs
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

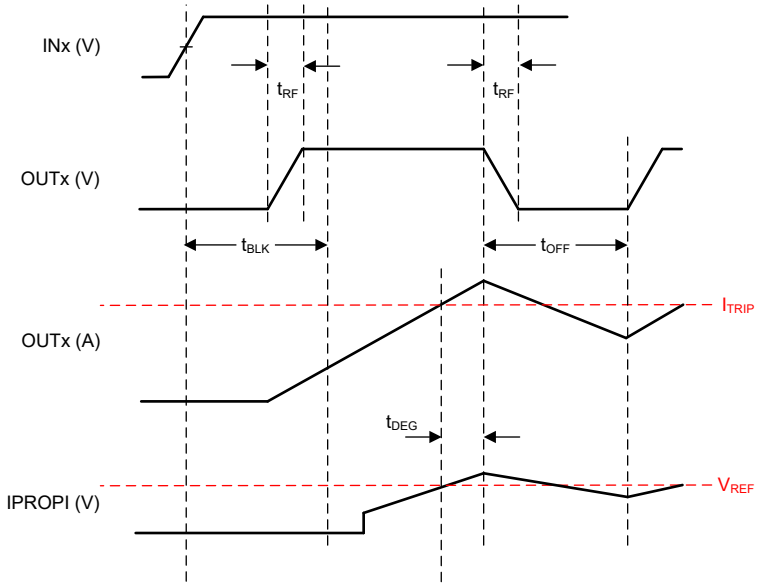


Figure 6-1. IPROPI Timing Diagram

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

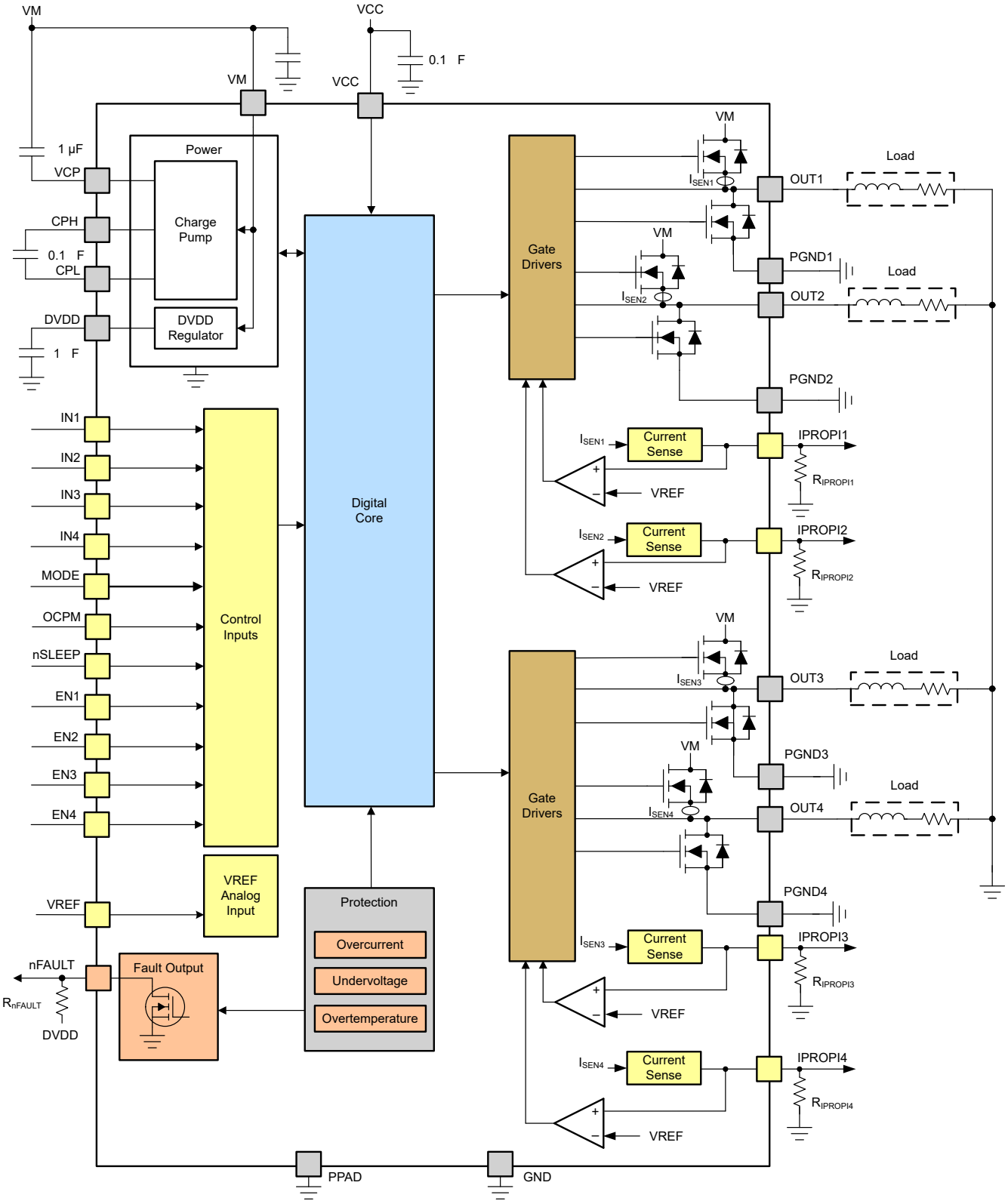
The DRV8962 is a four-channel half-bridge driver that operates from 4.5 V to 65 V and supports a wide range of load currents for various types of loads. The device integrates four half-bridge output power stages. The device integrates a charge pump regulator to support efficient high-side N-channel MOSFETs and 100% duty cycle operation. The DRV8962 can operate from a single power supply input (VM). Alternatively, the VCC pin can be connected to a second power supply to provide power to the internal logic blocks. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

The device is available in two packages - a 44-pin HTSSOP (DDW) package with exposed pad at the bottom of the package; and another 44-pin HTSSOP (DDV) package with exposed pad on the top of the package. The DDW package provides up to 5-A current per output. When used with a low thermal resistance heat sink installed on the top of the DDV package, the DRV8962 can deliver up to 10-A per output. The DRV8962 DDW package is pin-to-pin compatible with the DRV8952, which is rated for 48 V maximum operating voltage. The actual current that can be delivered depends on the ambient temperature, supply voltage, and PCB thermal design.

The DRV8962 provides current sense outputs. The IPROPI pins source a small current that is proportional to the current in the high-side MOSFETs. The current from the IPROPI pins can be converted to a proportional voltage using an external resistor (R_{IPROPI}). The integrated current sensing allows the DRV8962 to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect changes in load. The sense accuracy of the IPROPI output is ± 4% for 40% to 100% of rated current. External power sense resistors can also be connected if higher accuracy sensing is required. The current regulation level can be configured during operation through the VREF pin to limit the load current according to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), over current protection (OCP), and over temperature shutdown (OTSD). Fault conditions are indicated on the nFAULT pin.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

The following table shows the recommended values of the external components for the DRV8962.

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND1	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM	PGND3	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM3}	VM	PGND1	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 6.3-V or 10-V rated ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{REF1}	VREF	DVDD	Resistors to set current regulation threshold.
R_{REF2}	VREF	GND	
$R_{IPROPIx}$	IPROPIx	GND	For details, see Section 7.5.3

7.4 Independent Half-bridge Operation

- The DRV8962 can drive four half-bridge loads simultaneously.
- The MODE pin configures the typical output rise and fall times to 70 ns or 140 ns.
- The ENx pins enable or disable (Hi-Z) the outputs.
- The INx pins control the state (high or low) of the outputs
  - The INx pins can accept static or pulse-width modulated (PWM) signals.
  - The INx and ENx inputs can be powered before VM is applied.
- The truth table does not take into account the internal current regulation feature.
- The device automatically handles the dead time generation when switching between the high-side and low-side MOSFET of a half-bridge.

Table 7-2. Independent Half-Bridge Operation Truth Table

nSLEEP	INx	ENx	OUTx	DESCRIPTION
0	X	X	Hi-Z	Sleep mode, all half-bridges disabled (Hi-Z)
1	X	0	Hi-Z	Individual outputs disabled (Hi-Z)
1	0	1	L	OUTx Low-side ON
1	1	1	H	OUTx High-side ON

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. The following table is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 7-3. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
1	1	PWM	1	Forward PWM, slow decay
PWM	1	1	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

ADVANCE INFORMATION

7.5 Current Sensing and Regulation

The DRV8962 integrates current sensing across the high-side MOSFETs, current regulation, and current sense feedback. These features allow the device to sense the load current when the load is connected between output nodes and ground, without connecting an external sense resistor or sense circuitry; reducing system size, cost, and complexity. The current sense proportional outputs (IPROPI) allow the device to give detailed feedback to the controller about the load current.

7.5.1 Current Sensing and Feedback

The DRV8962 supports four IPROPI outputs, one for each half-bridge. The IPROPI outputs represent the current of each high-side MOSFET, as shown below -

$$I_{PROPI} = I_{HS} \times A_{IPROPI} \quad (1)$$

Where I_{HS} is the current flowing through the high-side MOSFET and A_{IPROPI} is the current mirror gain.

Each IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin. This allows the current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. The device implements an internal clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events. The IPROPI voltage should be less than the maximum recommended value of VREF, which is 3.3V.

The corresponding IPROPI voltage to the output current can be calculated as shown below -

$$V_{IPROPI}\,(V) = I_{PROPI}\,(A) \times R_{IPROPI}\,(\Omega) \quad (2)$$

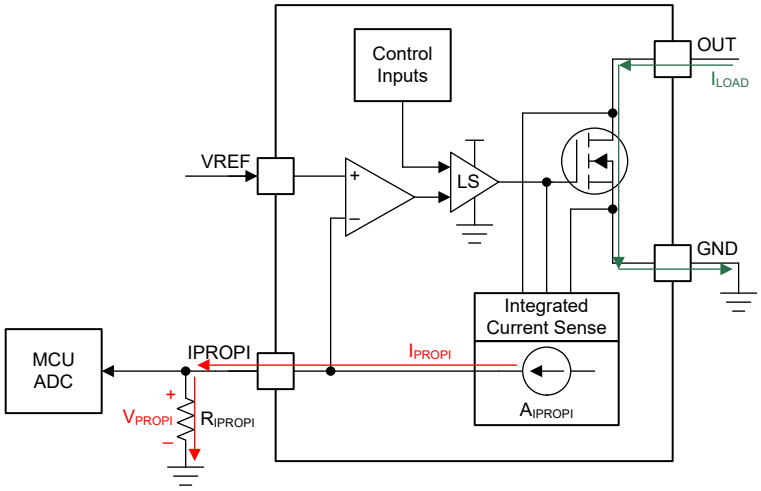


Figure 7-1. Integrated Current Sensing

The A_{ERR} parameter in the Electrical Characteristics table is the error associated with the A_{IPROPI} gain. It indicates the combined effect of offset error added to the I_{OUT} current and gain error.

7.5.2 Current Sensing with External Resistor

The IPROPI output accuracy is ±4% for 40% to 100% of rated current. If more accurate current sensing is desired, external sense resistors can also be used between the PGND pins and the system ground to sense the load currents, as shown below.

ADVANCE INFORMATION

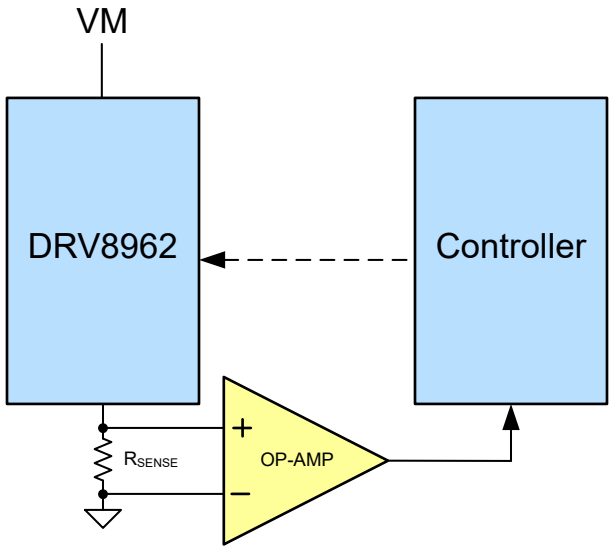


Figure 7-2. Current Sensing with External Resistor

The voltage drop across the external sense resistor should not exceed 300 mV.

Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to ensure good matching. Low-inductance sense resistors should be used to prevent voltage spikes and ringing. For optimal performance, the sense resistor should be a surface-mount resistor rated for high enough power.

7.5.3 Current Regulation

The current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP} \times A_{IPROPI} = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, to set I_{TRIP} at 5 A with V_{VREF} at 3.3 V, R_{IPROPI} has to be -

$R_{IPROPI} = V_{VREF} / (I_{TRIP} \times A_{IPROPI}) = 3.3 / (5 \times 212 \times 10^{-6}) = 3.09\ k\Omega$

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND (if current feedback is not required). If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold.

The DRV8962 can simultaneously drive up to four resistive or inductive loads. When an output load is connected to ground, the load current can be regulated to the I_{TRIP} level. The PWM off-time (t_{OFF}) is fixed at 16 µs. The fixed off-time mode allows for a simple current chopping scheme without involvement from the external controller. Fixed off-time mode will support 100% duty cycle current regulation.

Another way of controlling the load current is the cycle-by-cycle control mode, where PWM pulse width of the INx input pins have to be controlled. This allows for additional control of the current chopping scheme by the external controller.

Few scenarios of driving high-side and low-side loads are described below -

- **Resistive loads connected to ground:**

The regulated current will not exceed I_{TRIP}. If I_{TRIP} is higher than the (VM / R_{LOAD}), the load current is regulated at VM / R_{LOAD} level while INx = 1 (shown in Figure 7-3).

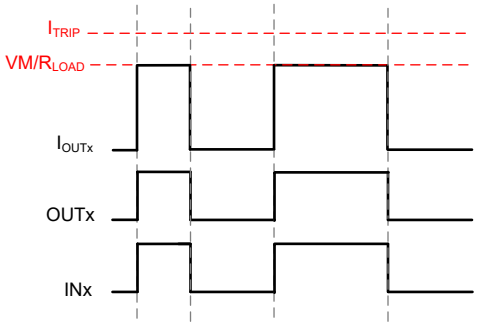


Figure 7-3. Resistive Load Connected to ground, Cycle-by-cycle control

- **Inductive loads connected to ground:**

It should be ensured that the current decays enough every cycle to prevent runaway and triggering overcurrent protection.

- For the scenario shown in Figure 7-4, with INx = 1, the low-side MOSFET is turned on for t_{OFF} duration after I_{OUT} exceeds I_{TRIP}. After t_{OFF}, the high side MOSFET is again turned on till I_{OUT} exceeds I_{TRIP} again.

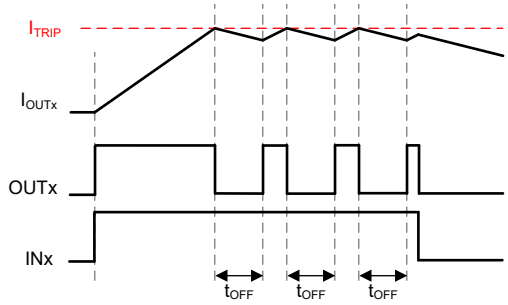


Figure 7-4. Inductive Load Connected to ground, fixed off-time current chopping

If, after the t_{OFF} time has elapsed the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration. The OFF time extension will continue till sensed current is less than I_{TRIP} at the end of t_{OFF} time.

- Loads can also be controlled using the cycle-by-cycle method. When INx = 1, the current through the load builds up; and when INx = 0, the current through the load decays. By properly choosing the duty cycle of the INx pulse, current can be regulated to a target value. Various such scenarios are shown in Figure 7-5 and Figure 7-6.

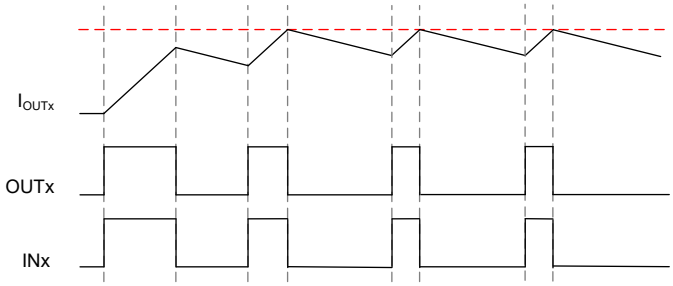


Figure 7-5. Inductive Load Connected to ground, Cycle-by-cycle control

The next scenario requires INx pin duty cycle adjustment (T has to be less than T_{OFF}) to ensure that the current does not run away.

ADVANCE INFORMATION

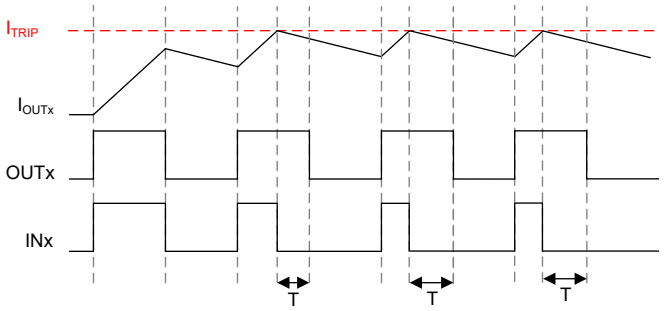


Figure 7-6. Inductive Load Connected to ground, Cycle-by-cycle control

- **Loads connected to VM:**

Such loads can be controlled by controlling the INx pin pulse width: INx = 0 builds up the current, and INx = 1 decays the current, as shown in Figure 7-7 and Figure 7-8.

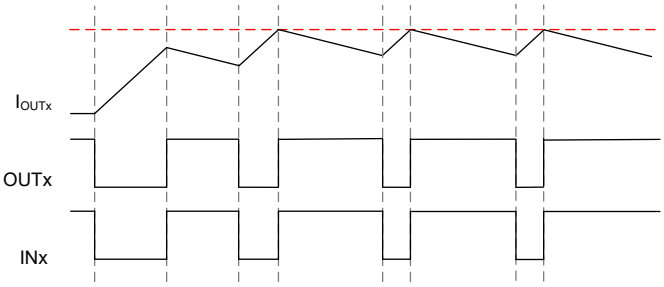


Figure 7-7. Inductive Load Connected to VM, Cycle-by-cycle control

This scenario requires INx pin duty cycle adjustment to ensure that the current does not run away.

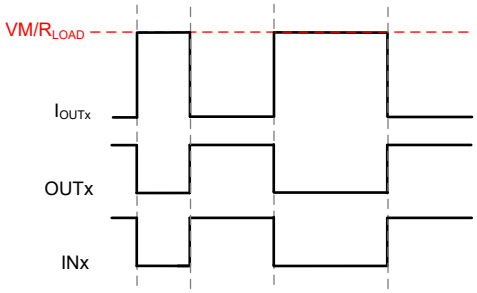


Figure 7-8. Resistive Load Connected to ground, Cycle-by-cycle control

7.6 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

ADVANCE INFORMATION

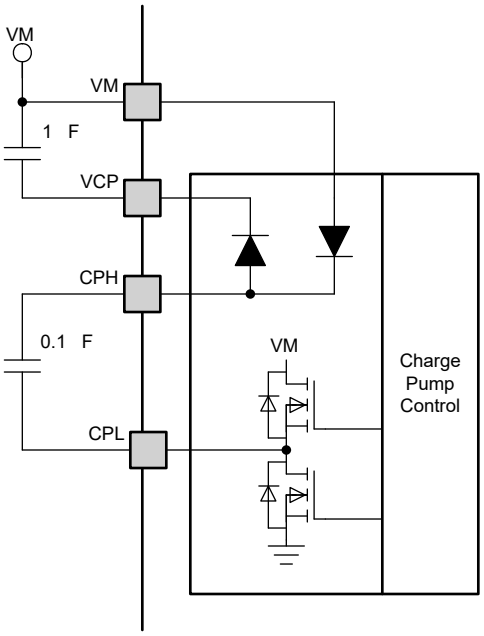


Figure 7-9. Charge Pump Block Diagram

7.7 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1 µF ceramic capacitor. The DVDD output is nominally 5-V.

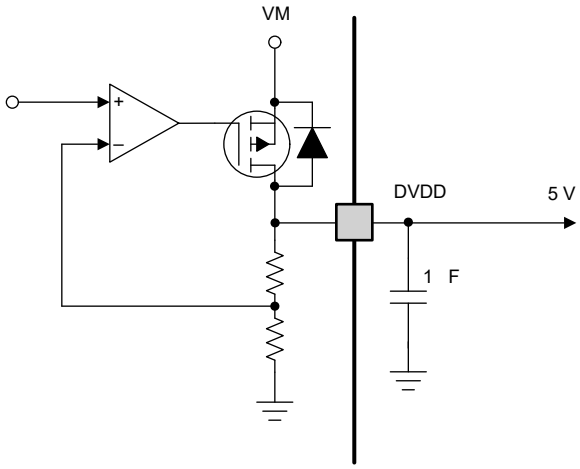


Figure 7-10. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.8 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3.05 V and 5.5 V and should be well regulated. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

ADVANCE INFORMATION

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8962. This is beneficial in high voltage applications, and when ambient temperature is high. Bypass the VCC pin to ground using a 0.1 µF ceramic capacitor.

7.9 Logic Level Pin Diagram

The pin diagram below shows the input structure for INx, ENx, MODE, OCPM and nSLEEP pins.

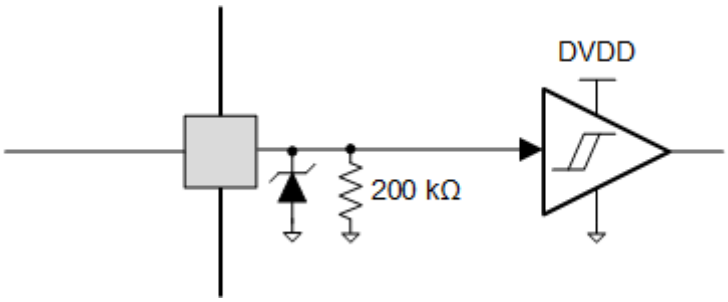


Figure 7-11. Logic-Level Input Pin Diagram

7.10 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO threshold voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump is disabled

Normal operation resumes (driver operation and nFAULT released) when the VM voltage recovers above the UVLO rising threshold voltage.

7.10.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active

Normal operation resumes (driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.10.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)
- Charge pump is disabled

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

7.10.4 Overcurrent Protection (OCP)

Analog current-limit circuit on each MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- Only the half-bridge experiencing the overcurrent will be disabled
- nFAULT is driven low

ADVANCE INFORMATION

- Charge pump remains active

Overcurrent conditions on both high and low side MOSFETs; meaning a short to ground or short to supply will result in an overcurrent fault detection.

Once the overcurrent condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically (driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.10.5 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs in the Half-bridges are disabled
- nFAULT is driven low
- Charge pump is disabled

Once the thermal shutdown condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

7.10.6 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

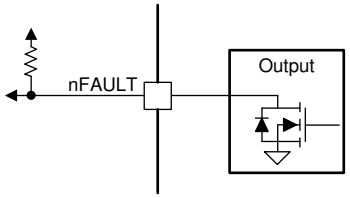


Figure 7-12. nFAULT Pin

7.10.7 Fault Condition Summary

Table 7-4. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	Half-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Reset	VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	-	Disabled	Disabled	Reset	VCC > VCC_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}, OCPM = 0	nFAULT	Disabled	Operating	Operating	Latched: nSLEEP reset pulse
	I_{OUT} > I_{OCP}, OCPM = 1	nFAULT	Disabled	Operating	Operating	Automatic retry: t_{RETRY}

ADVANCE INFORMATION

Table 7-4. Fault Condition Summary (continued)

FAULT	CONDITION	ERROR REPORT	Half-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
Thermal Shutdown (OTSD)	$T_J > T_{TSD}$, OCPM = 0	nFAULT	Disabled	Disabled	Operating	Latched: nSLEEP reset pulse
	$T_J > T_{TSD,}$ OCPM = 1	nFAULT	Disabled	Disabled	Operating	Automatic: $T_J < T_{OTSD}$ - T_{HYS_OTSD}

7.11 Device Functional Modes

7.11.1 Sleep Mode

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.11.2 Operating Mode

This mode is enabled when -

- nSLEEP is high
- VM > UVLO

The t_{WAKE} time must elapse before the device is ready for inputs.

7.11.3 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

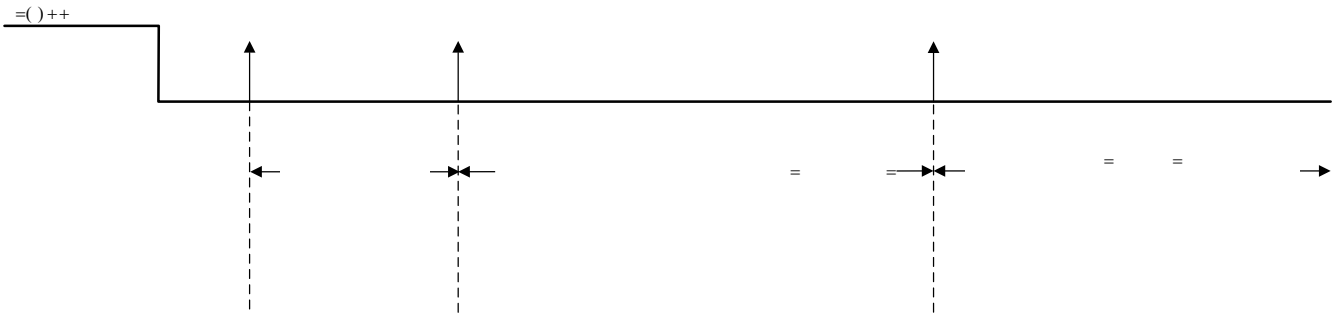


Figure 7-13. nSLEEP Reset Pulse

7.11.4 Functional Modes Summary

Table 7-5 lists a summary of the functional modes.

Table 7-5. Functional Modes Summary

CONDITION		CONFIGURATION	Half-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 65 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled
Operating	4.5 V < VM < 65 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8962 can be used to drive the following types of loads -

- Up to four solenoid loads
- One stepper motor
- Two brushed-DC motors
- One 3-phase sinewave Brushless-DC motor
- One 3-phase Permanent magnet synchronous motor (PMSM)
- One or two thermoelectric coolers (TEC)

8.1.1 Driving Solenoid Loads

The DRV8962 can drive four solenoid loads at the same time. For loads connected to ground, the IPROPI pins output the load current information; and the load current can be regulated to an I_{TRIP} level determined by the voltage on the VREF pin.

The DRV8962 supports independent IN and EN pins for each of the four half-bridges. All the four half-bridges also have separate PGND pins.

8.1.1.1 Solenoid Driver Typical Application

Figure 8-1 shows a schematic of the DRV8962 driving four loads connected to ground.

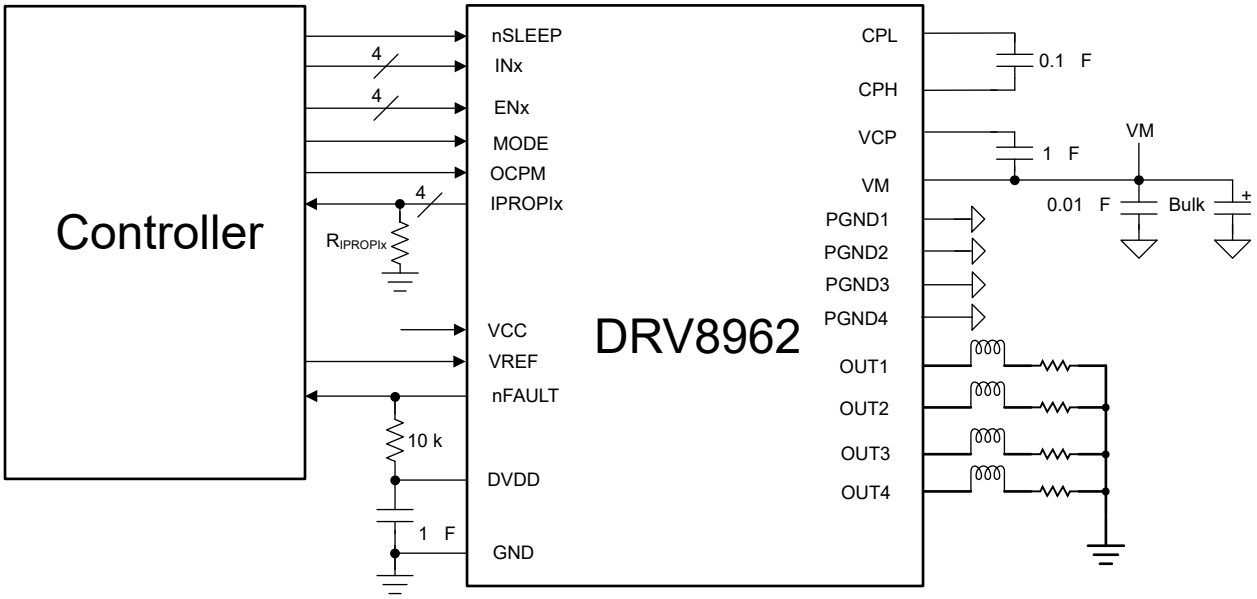


Figure 8-1. Driving Solenoids with DRV8962

8.1.1.2 Thermal Calculations

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

ADVANCE INFORMATION

Total power dissipation for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

8.1.1.2.1 Power Loss Calculations

The total power dissipation in each half-bridge can be calculated as -

$$P_{HB} = P_{HS} + P_{LS} = [R_{DS(ON)} \times I_L{}^2] + [((2 \times V_D \times t_D) + (VM \times t_{RF})) \times I_L \times f_{PWM}]$$

Where,

- $R_{DS(ON)}$ = ON resistance of each FET
  - For DRV8962, it is typically 50 mΩ at 25 °C, and 85 mΩ at 150 °C.
- f_{PWM} = PWM switching frequency
- VM = Supply voltage to the driver
- I_L = Load current
- D = PWM duty cycle (between 0 and 1)
- t_{RF} = Output voltage rise/ fall time
  - For DRV8962, the rise/fall time is either 70 ns or 140 ns
- V_D = FET body diode forward bias voltage
  - For DRV8962, it is 1 V
- t_D = dead time
  - For DRV8962, it is 300 ns

So, total power dissipation in the DRV8962 is -

$$P_{TOT} = n \times P_{HB} + P_Q$$

Where n is the number of half-bridges switching at the same time, and P_Q is the quiescent power loss.

For this example, let us assume -

- All four half-bridges are switching
- VM = 24 V
- I_L = 4 A
- Ambient temperature (T_A) = 25 °C
- t_{RF} = 70 ns
- Input PWM frequency = 20 kHz

When the VCC pin is connected to an external power supply, the quiescent current is 4 mA, and therefore P_Q will be (24 V x 4 mA) = 96 mW.

$$P_{HB} = [50\ m\Omega \times 4^2] + [((2 \times 1\ V \times 300\ ns) + (24\ V \times 70\ ns)) \times 4\ A \times 20\ KHz] = 0.982\ W$$

$$P_{TOT} = (4 \times 0.982) + 0.096 = 4.024\ W$$

8.1.1.2.2 Junction Temperature Estimation

The estimated junction temperature will be: $T_J = T_A + (P_{TOT} \times \theta_{JA})$

The junction-to-ambient thermal resistance θ_{JA} is 22.2 °C/W for the DDW package on a JEDEC standard PCB, and close to 5 °C/W for the DDV package if a suitable heat sink is used.

Therfore, the first estimate of the junction temperature is -

$$T_J = T_A + (P_{TOT} \times \theta_{JA}) = 25 + (4.024 \times 22.2) = 114.3\ °C$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

For example,

ADVANCE INFORMATION

- At 114.3 °C junction temperature, the on-resistance will likely increase by a factor of 1.35 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss (loss due to $R_{DS(ON)}$) for each half-bridge was 0.8 W.
- New estimate of conduction loss will therefore be 0.8 W x 1.35 = 1.08 W.
- New estimate of the total power loss will accordingly be 5.144 W.
- New estimate of junction temperature for the DDW package will be 139.2 °C.
- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

The following plot estimates the current that can be delivered from each output of the DDW package as a function of the ambient temperature and the number of half-bridges (N) switching at any time, with the following assumptions:

- VM = 24 V
- t_{RF} = 70 ns
- f_{PWM} = 20 kHz
- T_J = 150 °C

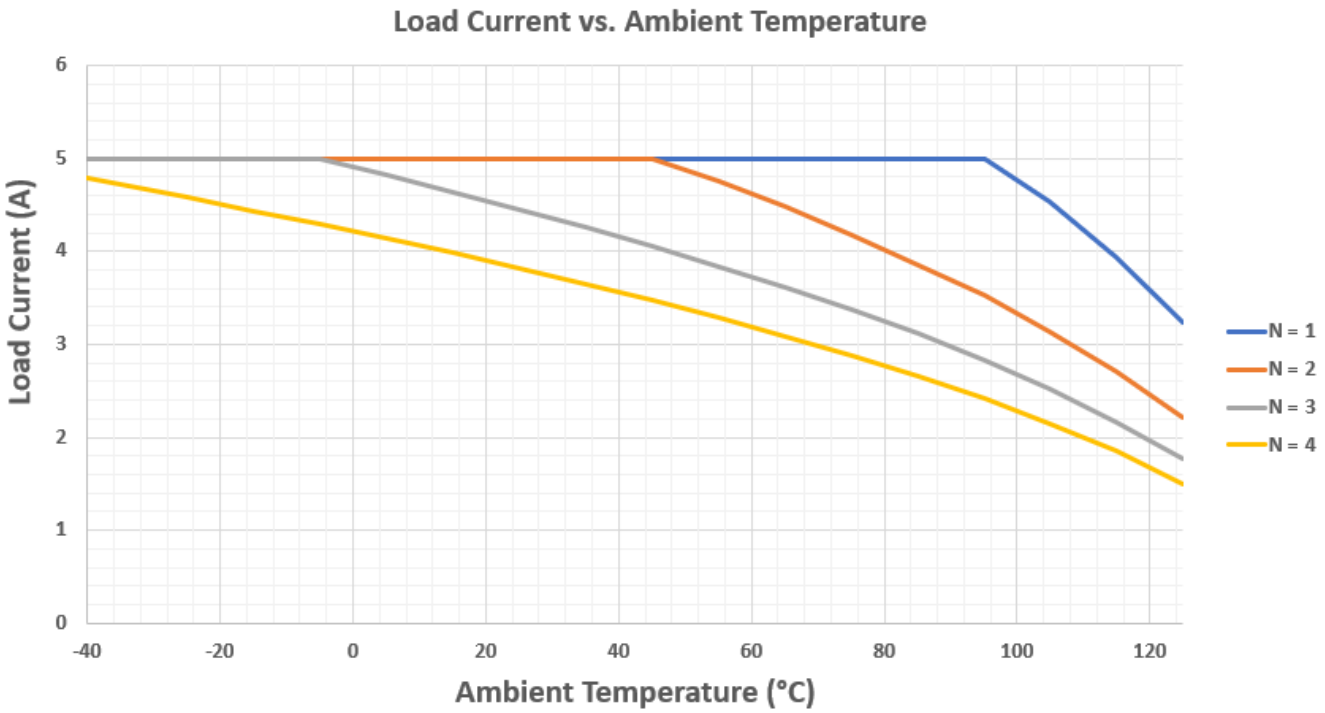


Figure 8-2. Load Current per Half-bridge vs. Ambient Temperature

8.1.2 Driving Stepper Motors

The DRV8962 can drive one stepper motor using the PWM input interface.

8.1.2.1 Stepper Driver Typical Application

The following schematic shows the DRV8962 driving a stepper motor.

ADVANCE INFORMATION

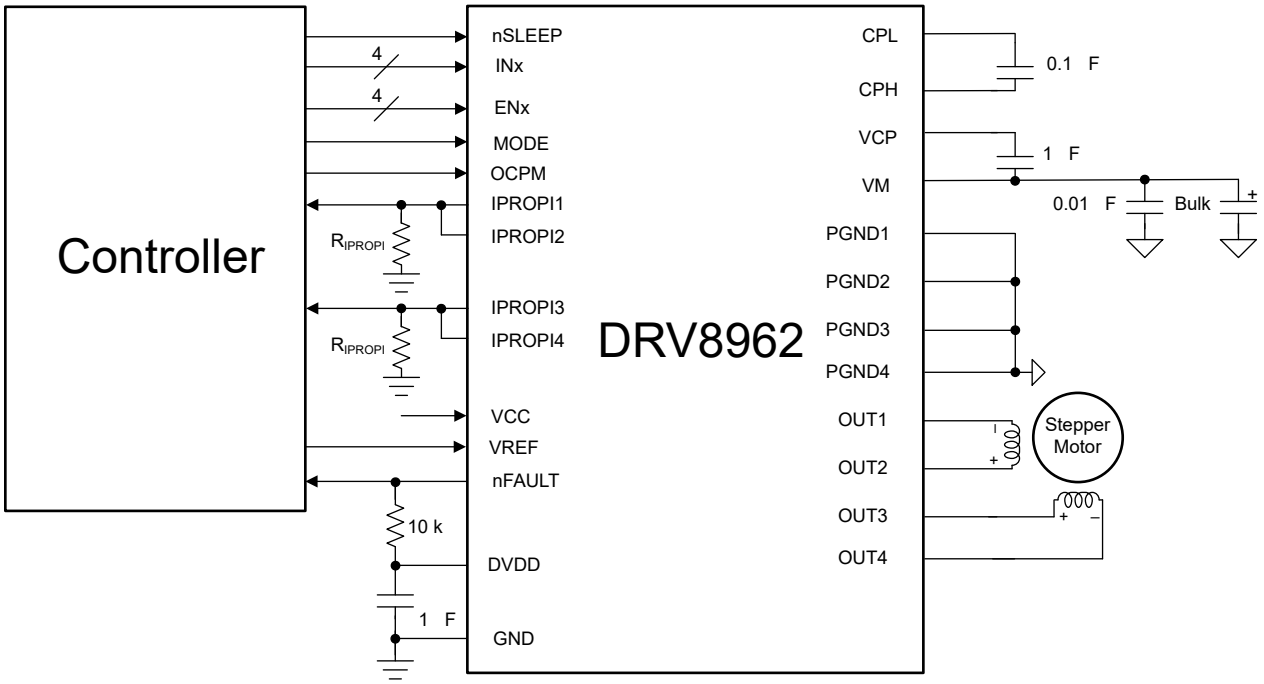


Figure 8-3. Driving Stepper Motor with DRV8962

The full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the VREF voltage and the resistor connected from IPROPI pin to ground.

I_{FS} x A_{IPROPI} = V_{VREF} / R_{IPROPI}

The maximum allowable voltage on the VREF pins is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

Note

The I_{FS} current must also follow Equation 4 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{4}$$

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}), determine the frequency of the input waveform as follows -

$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (^\circ/rot)}{\theta_{step}\ (^\circ/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \tag{5}$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the DRV8962. 1/ f_{step} = t_{STEP} on the diagram below. Equation 6 shows an example calculation for a 120 rpm target speed and 1/2 step.

$$f_{step}\ (steps/s) = \frac{120\ rpm \times 360^\circ/rot}{1.8^\circ/step \times 1/2\ steps/microstep \times 60\ s/min} = 800\,Hz \tag{6}$$

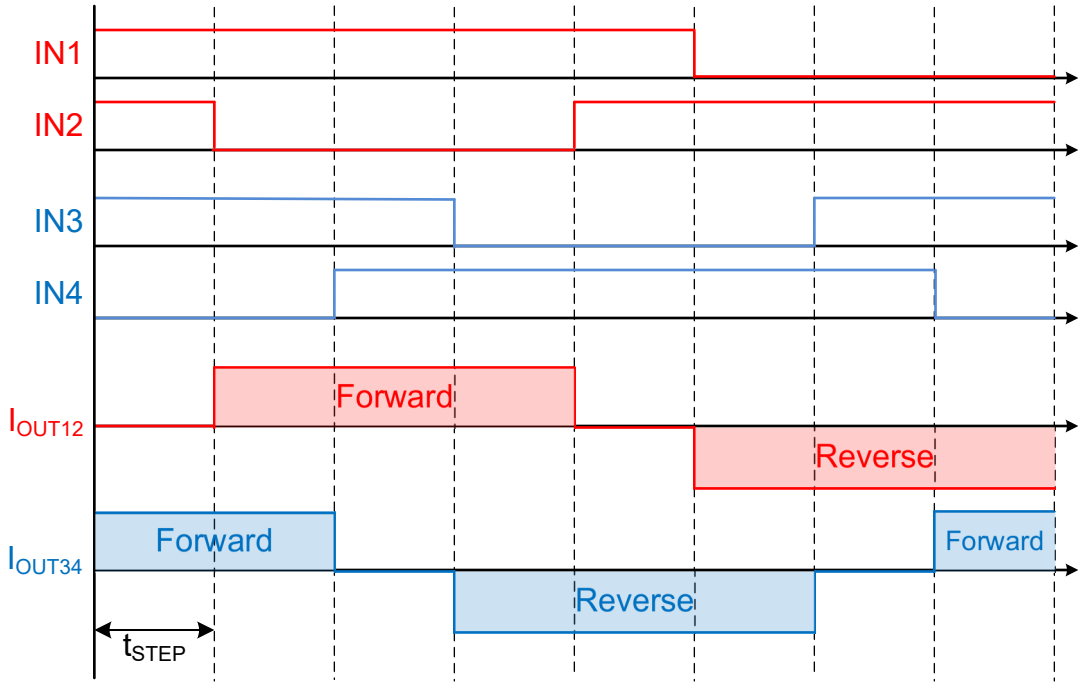


Figure 8-4. Example 1/2 Stepping Operation

Connect the IPROPI outputs corresponding to the same H-bridge together. IPROPI1 and IPROPI2, when connected together, reprsent the current of coil A of the stepper (connected between OUT1 and OUT2) during drive and slow-decay (high-side recirculation) modes. Similarly, IPROPI3 and IPROPI4, connected together, will reprsent coil B current.

When two IPROPI pins are connected together, the effective current mirror gain will be 424 µA/A typical. The resistor from the combined IPROPI pin to ground should be selected accordingly.

8.1.2.2 Power Loss Calculations

The following calculations assume a use case where the supply voltage is 24 V, full-scale current is 5 A, rise/fall time is 140 ns and input PWM frequency is 30-kHz.

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in Equation 7.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) \quad (7)$$

The conduction loss for the typical application shown in Section 8.1.2.1 is calculated in Equation 8.

$$P_{COND} = 2 \times (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \times (5\text{-A} / \sqrt{2})^2 \times (0.1\text{-}\Omega) = 2.5\text{-W} \quad (8)$$

The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in Equation 9 and Equation 10.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (9)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (10)$$

After substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

ADVANCE INFORMATION

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (140\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (11)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (100\text{ ns}) \times 30\text{-kHz} = 0.178\text{-W} \quad (12)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.178\text{-W} + 0.178\text{-W}) = 0.712\text{-W} \quad (13)$$

Note

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

When the VCC pin is connected to an external voltage, the quiescent current is typically 4 mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (14)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 4\text{-mA} = 0.096\text{-W} \quad (15)$$

Note

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in Equation 16.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.5\text{-W} + 0.712\text{-W} + 0.096\text{-W} = 3.308\text{-W} \quad (16)$$

8.1.2.3 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.2 °C/W for the DDW package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (3.308\text{-W} \times 22.2\ °C/W) = 98.4\ °C \quad (17)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

For example,

- At 98.4 °C junction temperature, the on-resistance will likely increase by a factor of 1.25 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss was 2.5 W.
- New estimate of conduction loss will therefore be 2.5 W x 1.25 = 3.125 W.
- New estimate of the total power loss will accordingly be 3.933 W.
- New estimate of junction temperature for the DDW package will be 112.3 °C.

ADVANCE INFORMATION

- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

When using the DDV package, if a heat sink with less than 4 °C/W thermal resistance is chosen, the junction to ambient thermal resistance can be lower than 5 °C/W. The initial estimate of the junction temperature with the DDV package in this application will therefore be -

$$T_J = 25°C + (3.308\text{-W} \times 5\ °C/W) = 41.5\ °C \quad (18)$$

As the DDV package results in low thermal resistance, it can deliver 10 A full-scale current.

8.1.3 Driving Brushed-DC Motors

The DRV8962 can be used to drive one or two brushed-DC motors.

8.1.3.1 Brushed-DC Driver Typical Application

The schematic below shows the DRV8962 driving two brushed-DC motors.

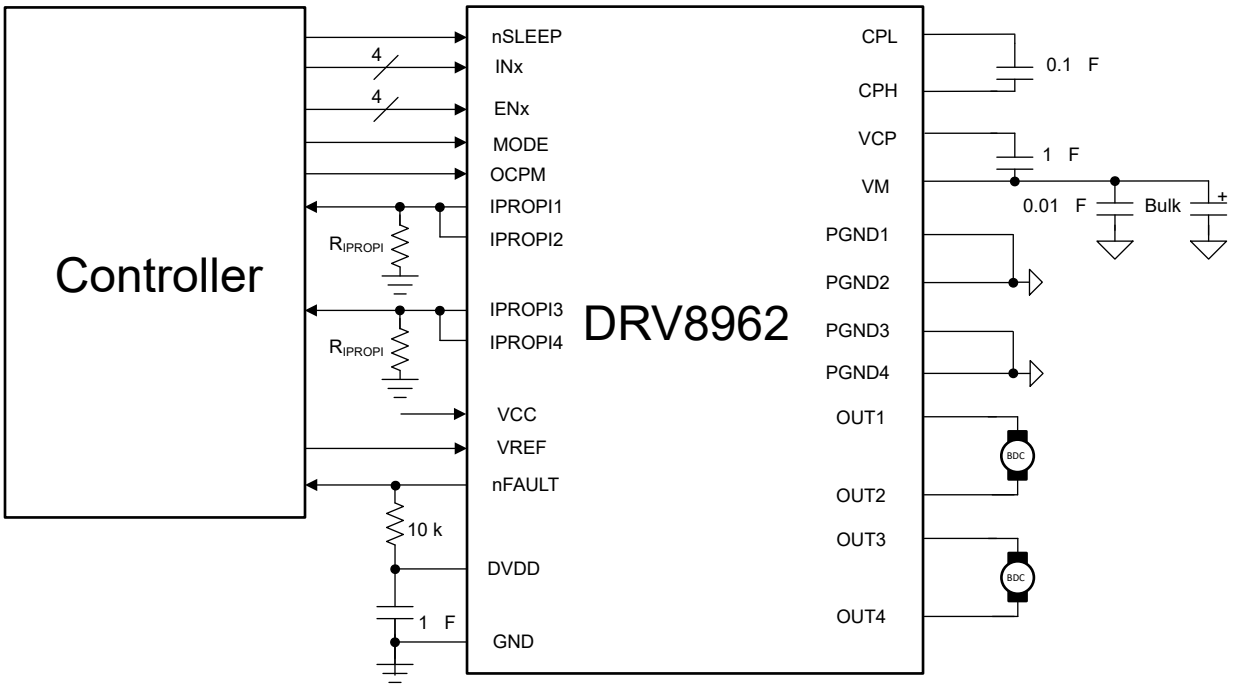


Figure 8-5. Driving two Brushed-DC Motors with DRV8962

The following truth table describes how to control brushed-DC motors -

Table 8-1. Brushed-DC Motor Truth Table

Function	EN1	EN2	IN1	IN2	OUT1	OUT2
Forward	1	1	1	PWM	H	H/L
Reverse	1	1	PWM	1	H/L	H
Brake	1	1	1	1	H	H
Brake*	1	1	0	0	L	L
Coast*	0	X	X	X	Z	X
Coast*	X	0	X	X	X	Z

* IPROPI pins will not output proportional current in these conditions.

ADVANCE INFORMATION

8.1.3.2 Power Loss Calculation

For a H-bridge with high-side recirculation, power dissipation for each FET can be approximated as follows:

- $P_{HS1} = R_{DS(ON)} \times I_L^2$
- $P_{LS1} = 0$
- $P_{HS2} = [R_{DS(ON)} \times I_L^2 \times (1-D)] + [2 \times V_D \times I_L \times t_D \times f_{PWM}]$
- $P_{LS2} = [R_{DS(ON)} \times I_L^2 \times D] + [VM \times I_L \times t_{RF} \times f_{PWM}]$

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

Substituting the following values in the equations above -

- VM = 24 V
- I_L = 4 A
- $R_{DS(ON)}$ = 50 mΩ
- D = 0.5
- V_D = 1 V
- t_D = 300 ns
- t_{RF} = 70 ns
- f_{PWM} = 20 kHz

The losses in each FET can be calculated as follows -

$P_{HS1} = 50\ m\Omega \times 4^2 = 0.8\ W$

$P_{LS1} = 0$

$P_{HS2} = [50\ m\Omega \times 4^2 \times (1-0.5)] + [2 \times 1\ V \times 4\ A \times 300\ ns \times 20\ KHz] = 0.448\ W$

$P_{LS2} = [\ 50\ m\Omega \times 4^2 \times 0.5] + [24 \times 4\ A \times 70\ ns \times 20\ kHz] = 0.534\ W$

Quiescent Current Loss $P_Q = 24\ V \times 4\ mA = 0.096\ W$

$P_{TOT} = 2 \times (P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2}) + P_Q = 2 \times (0.8 + 0 + 0.448 + 0.534) + 0.096 = 3.66\ W$

8.1.3.3 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.2 °C/W for the DDW package.

Assuming 25°C ambient temperature, the junction temperature for the DDW package is calculated as shown below -

$$T_J = 25°C + (3.66\text{-W} \times 22.2\ °C/W) = 106.3\ °C \quad (19)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature, as explained in Section 8.1.1.2.2 and Section 8.1.2.3.

The DDV package with heat sink mounted on top will be able to deliver up to 10A current to both brushed-DC motors.

8.1.3.4 Driving Single Brushed-DC Motor

The outputs of DRV8962 can be connected in parallel to increase the drive current. Figure 8-6 shows the schematic of DRV8962 driving a single brushed-DC motor.

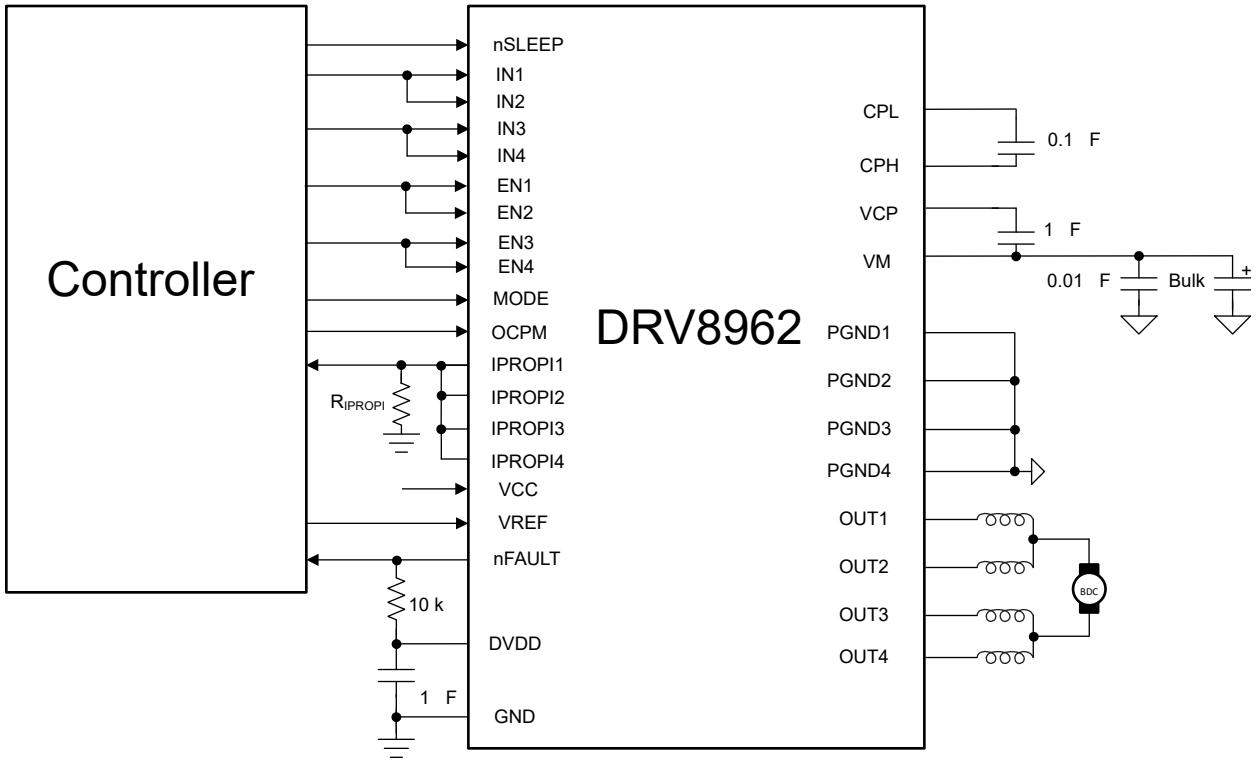


Figure 8-6. Driving Single Brushed-DC motor with DRV8962

In this mode, a minimum of 30 nH to 100 nH inductance or a ferrite bead is required after the output pins before connecting the two channels together. This will help to prevent any shoot through between two paralleled channels during switching transient due to mismatch of paralleled channels (for example, asymmetric PCB layout, etc).

8.1.4 Driving Thermoelectric Coolers (TEC)

Thermoelectric coolers (TEC) work according to the Peltier effect. When a voltage is applied across the TEC, a DC current flows through the junction of the semiconductors, causing a temperature difference. Heat is transferred from one side of the TEC to the other. This creates a “hot” and a “cold” side of the TEC element. If the DC current is reversed, the hot and cold sides reverse as well.

A common way of modulating the current through the TEC is to use PWM driving and make the average current change by varying the ON and OFF duty cycles. To allow both heating and cooling from a single supply, a H-bridge topology is required. The DRV8962 can drive two H-bridges to drive two TECs bi-directionally with up to 5-A current. Pair of half-bridges can also be paralleled together to drive a single TEC with up to 10-A current.

The DRV8962 also features integrated current sensing and current sense output (IPROPI) with ± 4% accuracy to eliminate the need for two external shunt resistors in a closed-loop control topology, saving bill-of-materials cost and space. Figure 8-7 shows the schematic of two TECs connected to a DRV8962 driver.

ADVANCE INFORMATION

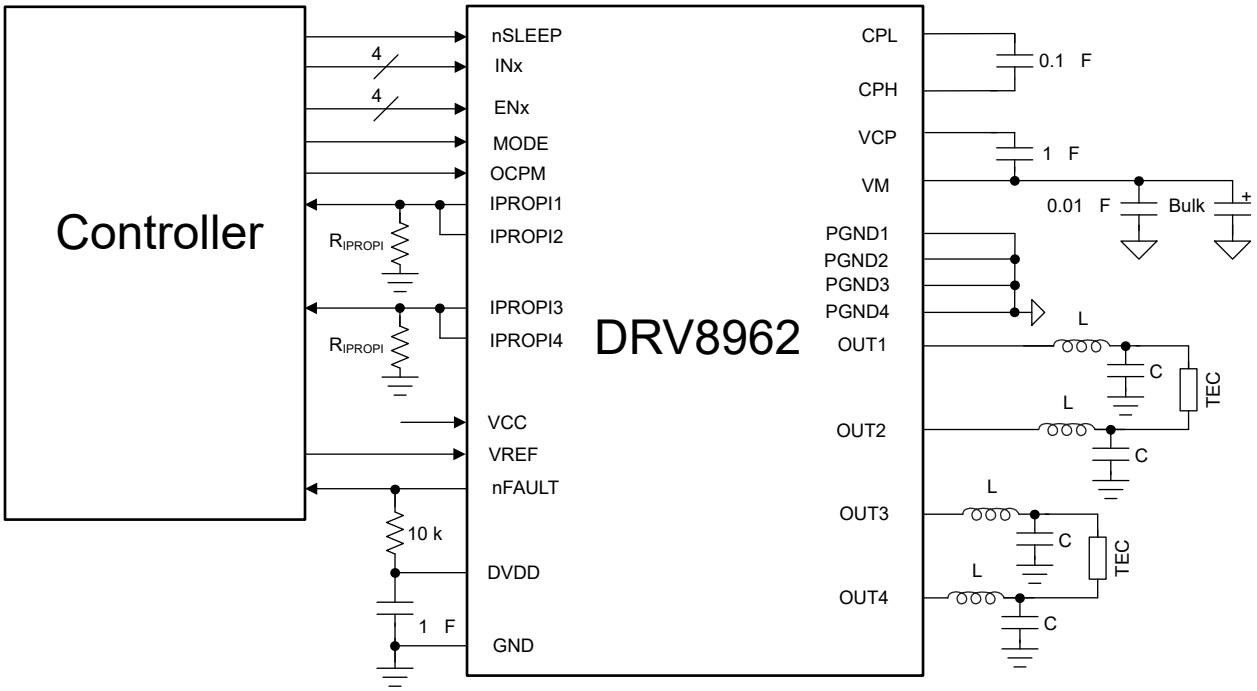


Figure 8-7. Driving two TECs

Figure 8-8 shows the schematic to drive one TEC with higher current.

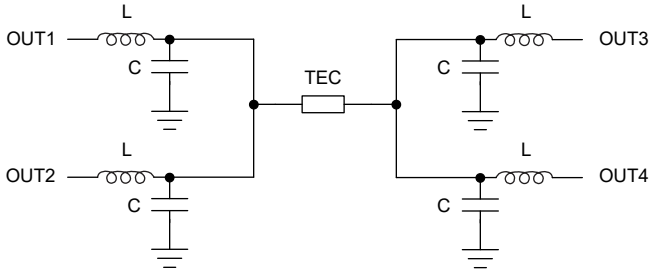


Figure 8-8. Driving one TEC with higher current

The LC filters connected to the output nodes convert the PWM output from the DRV8962 into a low-ripple DC voltage across the TEC. The filters are required to minimize the ripple current, because fast transients (e.g., square wave power) can shorten the life of the TEC. The maximum ripple current is recommended to be less than 10% of maximum current. The maximum temperature differential across the TEC, which decreases as ripple current increases, is calculated with the following equation:

$$\Delta T = \Delta T_{MAX} / (1 + N^2) \quad (20)$$

Where ΔT is actual temperature differential, ΔT_{MAX} is maximum possible temperature differential specified in the TEC datasheet, N is the ratio between ripple and maximum current. N should not be greater than 0.1.

The choice of the input PWM frequency is a trade-off between switching loss and use of smaller inductors and capacitors. High PWM frequency also means that the voltage across the TEC can be tightly controlled, and the LC components can potentially be cheaper.

The transfer function of a second order low-pass filter is shown in :

$$H(j\omega) = 1 / (1 - (\omega / \omega_0)^2 + j\omega / Q\omega_0) \quad (21)$$

Where,

ω_0 = 1 / √(LC), resonant frequency of the filter

Q = quality factor

ω = DRV8962 input PWM frequency

The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the PWM frequency. With this assumption, Equation 20 may be simplified to -

H in dB = -40 log (f_S/f_0)

Where f_0 = 1/ 2π√(LC) and f_S is the input PWM switching frequency.

- If L = 10 µH and C = 22 µF, the resonant frequency is 10.7 kHz.
- This resonant frequency corresponds to 39 dB of attenuation at 100 kHz switching frequency.
- For VM = 48 V, 39 dB attenuation means that the amount of ripple voltage across the TEC element will be approximately 550 mV.
- For a TEC element with a resistance of 1.5 Ω, the ripple current through the TEC will therefore be 366 mA.
- At the 5-A maximum output current of the DRV8962, 366 mA corresponds to 7.32% ripple current.
- This will cause about 0.5% reduction of the maximum temperature differential of the TEC element, as per Equation 20.

Adjust the LC values according to the supply voltage and DC current through the TEC element. The DRV8962 supports up to 200 kHz input PWM frequency. The power loss in the device at any given ambient temperature must be carefully considered before selecting the input PWM frequency.

Closing the loop on current is important in some TEC based heating and cooling systems. The DRV8962 can achieve this without the need for external current shunt resistors. Internal current mirrors are used to monitor the currents in each half-bridge and this information is available on IPROPI pins. A microcontroller can monitor and adjust the PWM duty based on the IPROPI pin voltage. When driving two TECs, connect the IPROPI pins of the corresponding half-bridges together to measure the H-bridge current. For example, for the schematic shown in Figure 8-7, IPROPI1 and IPROPI2 are tied together, and IPROPI3 and IPROPI4 are also together. When driving only one TEC as shown in Figure 8-8, tie all the IPROPI pins together.

Additionally, the DRV8962 can regulate the current internally by providing an external voltage reference (VREF) to the device to adjust the current regulation trip point. The current loop would then be closed within the H-bridge itself.

8.1.5 Driving Brushless DC Motors

The DRV8962 can also be used to drive a three-phase brushless DC (BLDC) motor. The DRV8962 supports independent control of three phases required to drive the BLDC motor. One of the four half-bridges of the DRV8962 can be disabled while driving a BLDC motor, by connecting the corresponding EN pin to ground. Shows a schematic of the DRV8962 driving a BLDC motor.

ADVANCE INFORMATION

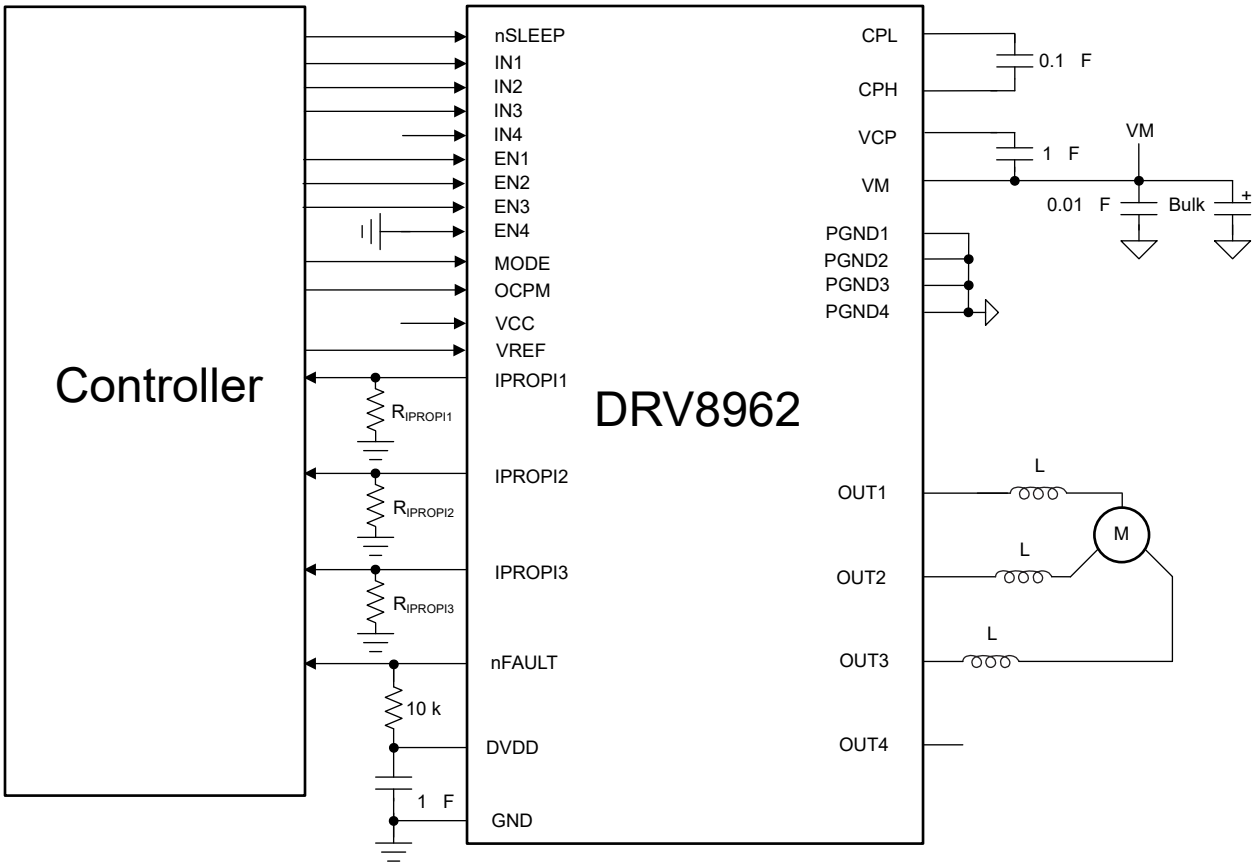


Figure 8-9. Driving BLDC Motor with DRV8962

The three half-bridges required to drive a BLDC motor can be controlled by six inputs - EN1, EN2, EN3 and IN1, IN2, IN3.

- When EN1 is low, OUT1 becomes high-impedance, allowing current to flow through the internal body diodes of the high-side and low-side FETs.
- When EN1 is high and IN1 is low, OUT1 is driven low with its low-side FET enabled.
- When EN1 is high and IN1 is high, OUT1 is driven high with its high-side FET enabled.
- Likewise is true for OUT2 and OUT3.
- EN4 can be grounded to permanently disable OUT4.

A minimum of 30 nH to 100 nH inductance or a ferrite bead has to be connected after the output pins. This will help to prevent any shoot through due to mismatch between channels (for example, process variation, unsymmetrical PCB layout, etc).

The IPROPI pins output a current proportional to the current flowing through the high-side FET of each half-bridge. The IPROPI output accuracy at maximum rated current is ± 4%.

$I_{IPROPI} = I_{HS} \times A_{IPROPI}$

Each IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC).

$V_{IPROPI} = IPROPI \times R_{IPROPI}$

If higher accuracy of current sensing is required, external sense resistors can be placed between the PGND pins and system ground. The voltage drop across the external sense resistor should not exceed 300 mV.

9 Package Thermal Considerations

9.1 DDW Package

Thermal pad of the DDW package is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. Refer to the Section 11.1 section for more details.

9.2 DDV Package

The DDV package is designed to interface directly to a heat sink using a thermal interface compound in between, (e.g., Ceramique from Arctic Silver, TIMTronics 413, etc.). The heat sink absorbs heat from the DRV8962 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. A concept digram of the heatsink on top of the DDV package is shown in Figure 9-1.

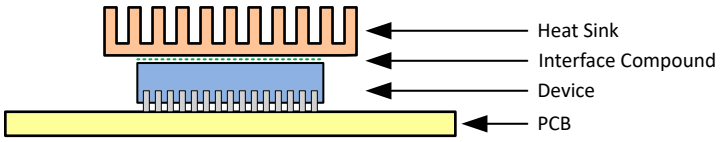


Figure 9-1. Heat sink on DDV Package

Care must be taken when mounting the heatsinks, ensuring good contact with thermal pads and not exceeding the mechanical stress capability of the parts to avoid breakage. The DDV package is capable of tolerating up to 90 Newton load. In production, it is recommended to apply less than 45 Newton load torque.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ of the DDV Package (thermal resistance from junction to exposed pad)
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

$R_{\theta JA} = R_{\theta JC}$ + thermal interface resistance + heat sink resistance

The thermal resistance of the thermal interface material can be determined from the area of the exposed metal package and manufacturer's value for the area thermal resistance (expressed in °Cmm^2/W). For example, a typical white thermal grease with a 0.0254 mm (0.001 inch) thick layer has 4.52 °Cmm^2/W thermal resistance. The DDV package has an exposed area of 28.7 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the interface material as 0.157°C/W.

Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured. The following are the various important parameters in selecting a heatsink.

1. Thermal resistance
2. Airflow
3. Volumetric resistance
4. Fin density
5. Fin spacing
6. Width
7. Length

The thermal resistance is one parameter that changes dynamically depending on the airflow available.

Airflow is typically measured in LFM (linear feet per minute) or CFM (cubic feet per minute). LFM is a measure of velocity, whereas CFM is a measure of volume. Typically, fan manufacturers use CFM because fans are rated according to the quantity of air it can move. Velocity is more meaningful for heat removal at the board level, which is why the derating curves provided by most power converter manufacturers use this.

Typically, airflow is either classified as natural or forced convection.

ADVANCE INFORMATION

- Natural convection is a condition with no external induced flow and heat transfer depends on the air surrounding the heatsink. The effect of radiation heat transfer is very important in natural convection, as it can be responsible for approximately 25% of the total heat dissipation. Unless the component is facing a hotter surface nearby, it is imperative to have the heatsink surfaces painted to enhance radiation.
- Forced convection occurs when the flow of air is induced by mechanical means, usually a fan or blower.

Limited thermal budget and space make the choice of a particular type of heatsink very important. This is where the volume of the heatsink becomes relevant. The volume of a heatsink for a given flow condition can be obtained by using the following equation:

$Volume_{(heatsink)}$ = volumetric resistance (Cm^3 °C/W)/thermal resistance θ_{SA} (°C/W)

An approximate range of volumetric resistance is given in the following table:

Available Airflow (LFM)	Volumetric Resistance (Cm^3 °C/W)
NC	500 – 800
200	150 - 250
500	80 - 150
1000	50 - 80

The next important criterion for the performance of a heatsink is the width. It is linearly proportional to the performance of the heatsink in the direction perpendicular to the airflow. An increase in the width of a heatsink by a factor of two, three, or four increase the heat dissipation capability by a factor of two, three, or four. Similarly, the square root of the fin length used is approximately proportional to the performance of the heatsink in the direction parallel to the airflow. In case of an increase in the length of the heatsink by a factor of two, three, or four only increases the heat dissipation capability by a factor of 1.4, 1.7, or 2.

If the board has sufficient space, it is always beneficial to increase the width of a heatsink rather than the length of the heatsink. This is only the beginning of an iterative process before the correct and the actual heatsink design is achieved.

The heat sink must be supported mechanically at each end of the IC. This mounting ensures the correct pressure to provide good mechanical, thermal and electrical contact. The heat sink should be connected to GND or left floating.

9.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

10 Power Supply Recommendations

The DRV8962 is designed to operate from an input voltage supply (VM) range from 4.5 V to 65 V. A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of DRV8962. In addition, a bulk capacitor must be included on VM.

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps with a change in voltage. When adequate bulk capacitance is used, the voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

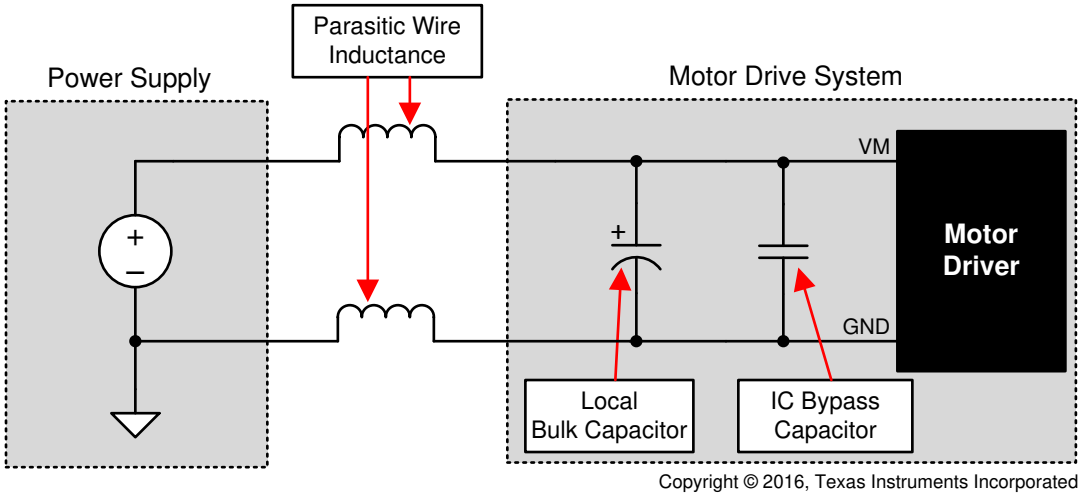


Figure 10-1. Example Setup of System With External Power Supply

10.2 Power Supplies

The DRV8962 needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the half-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.
- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by built-in charge pump requiring external capacitors.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

- The VM pins should be bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins should be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- Bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the DDW package must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

11.2 Layout Example

Follow the layout example of the DRV8962 EVM. The design files can be downloaded from the DRV8962EVM product folder.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Related Documentation

- Texas Instruments, *How to Drive Unipolar Stepper Motors with DRV8xxx* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *What Motor Drivers should be considered for driving TEC*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

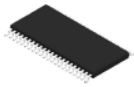
ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

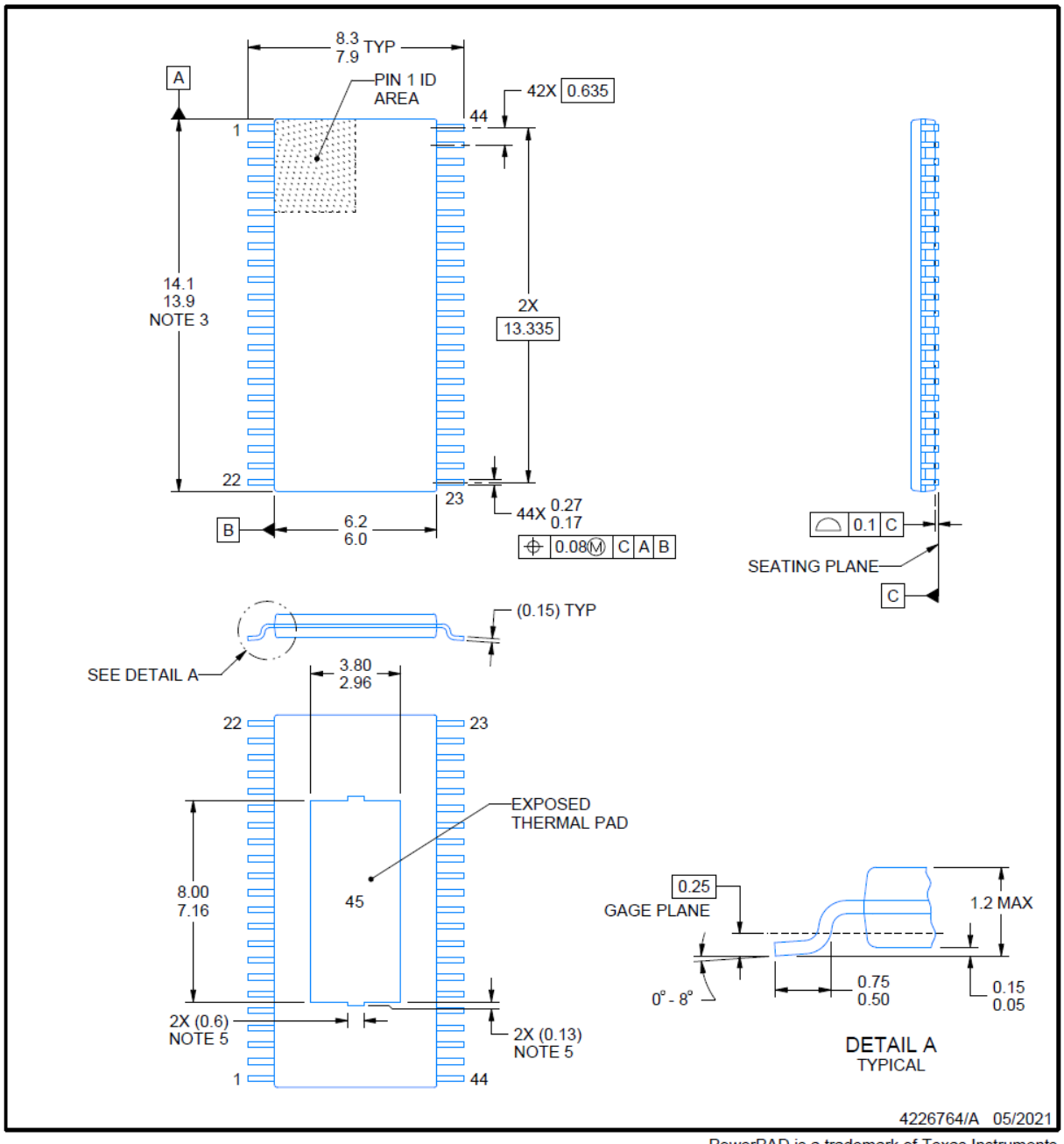
PACKAGE OUTLINE

DDW0044E



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

ADVANCE INFORMATION

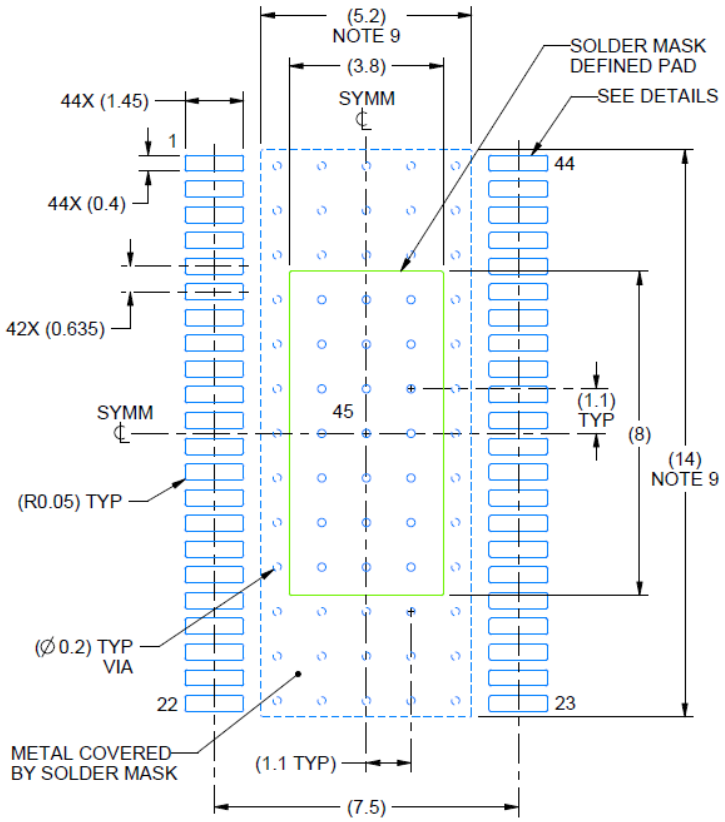
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

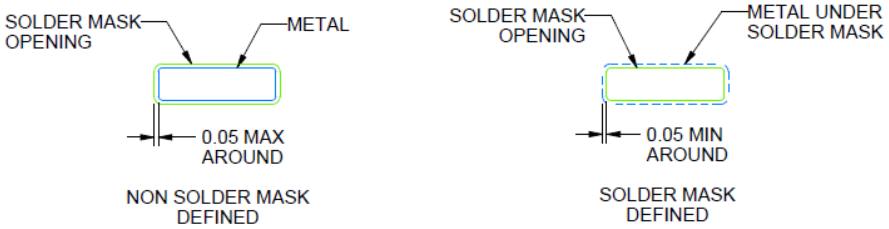
DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4226764/A 05/2021

NOTES: (continued)

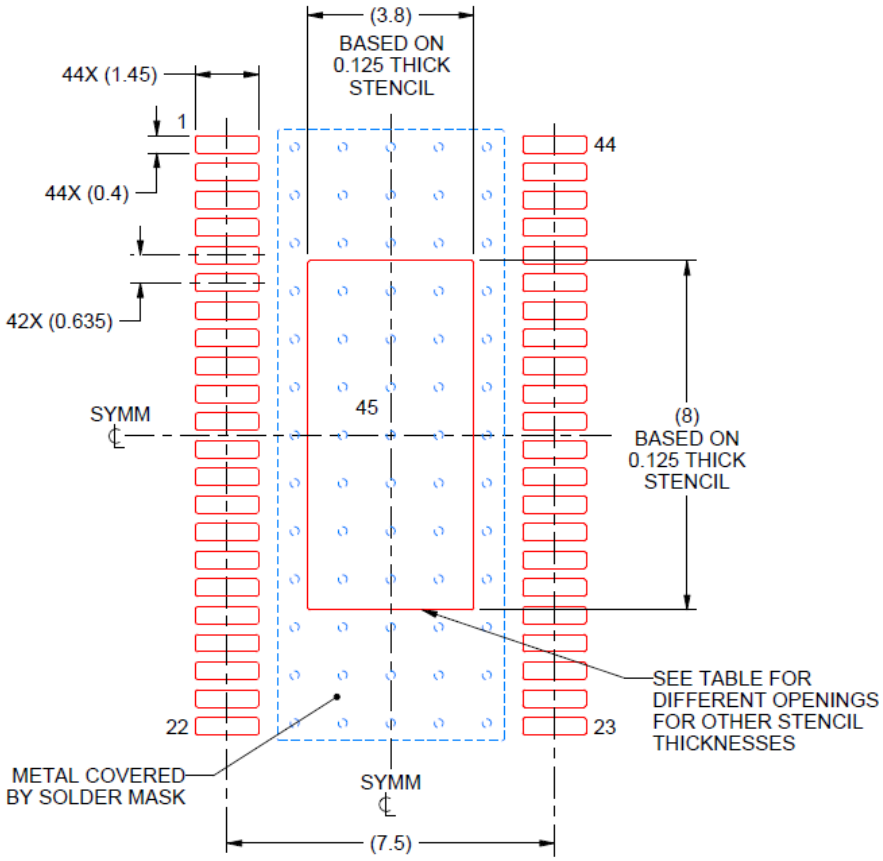
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

4226764/A 05/2021

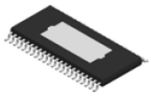
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

ADVANCE INFORMATION

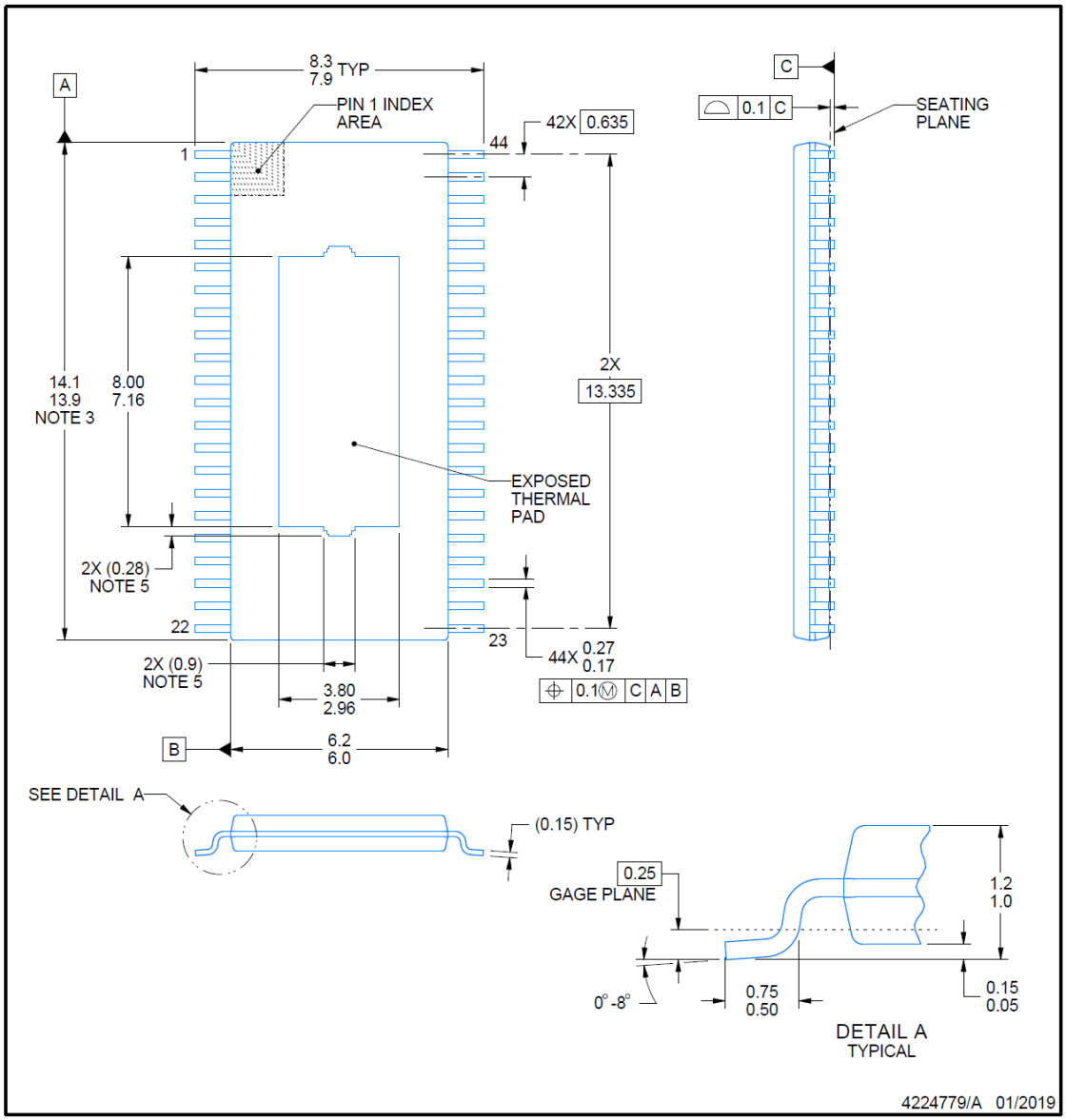
PACKAGE OUTLINE



DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

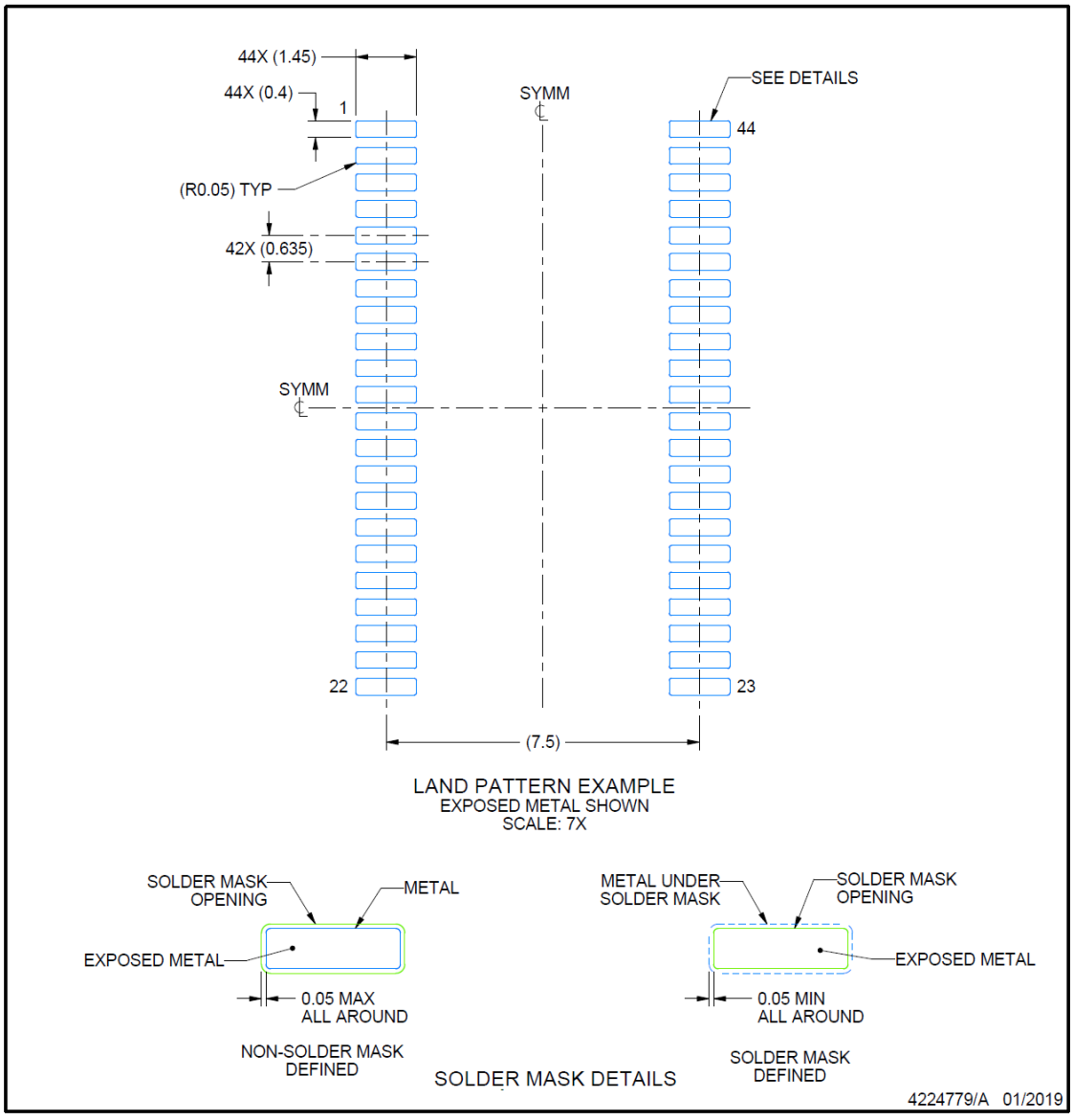
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DDV0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

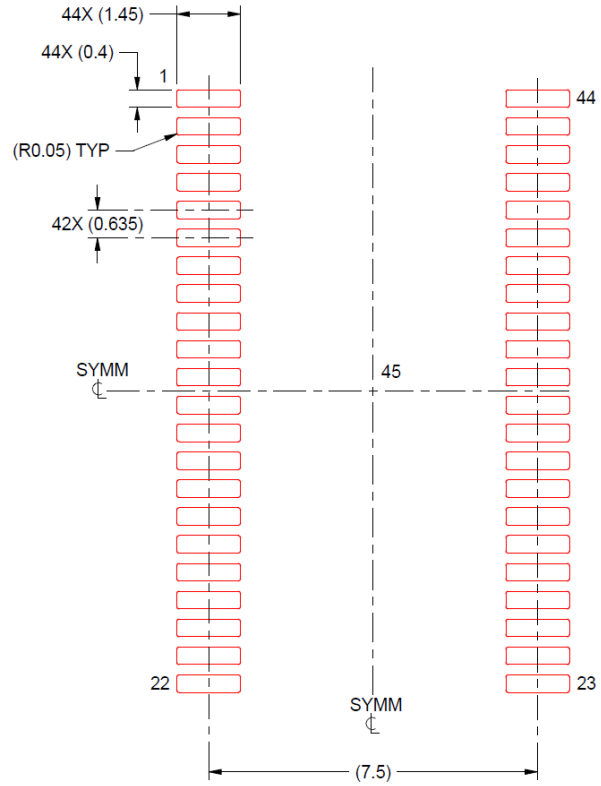
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDV0044E — **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

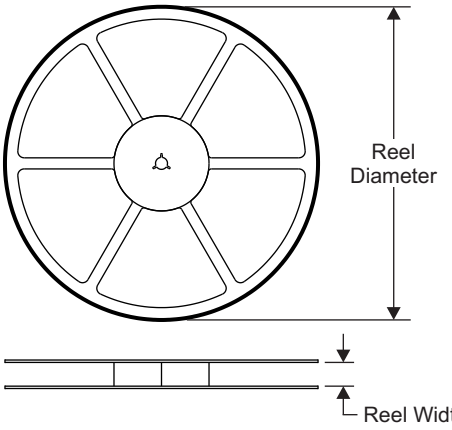
4224779/A 01/2019

NOTES: (continued)

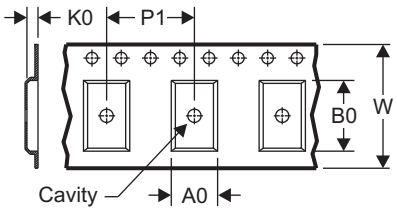
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

13.1 Tape and Reel Information

REEL DIMENSIONS

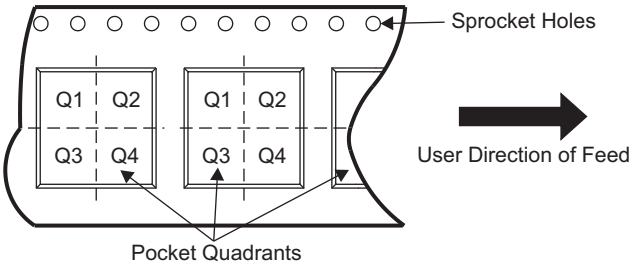


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

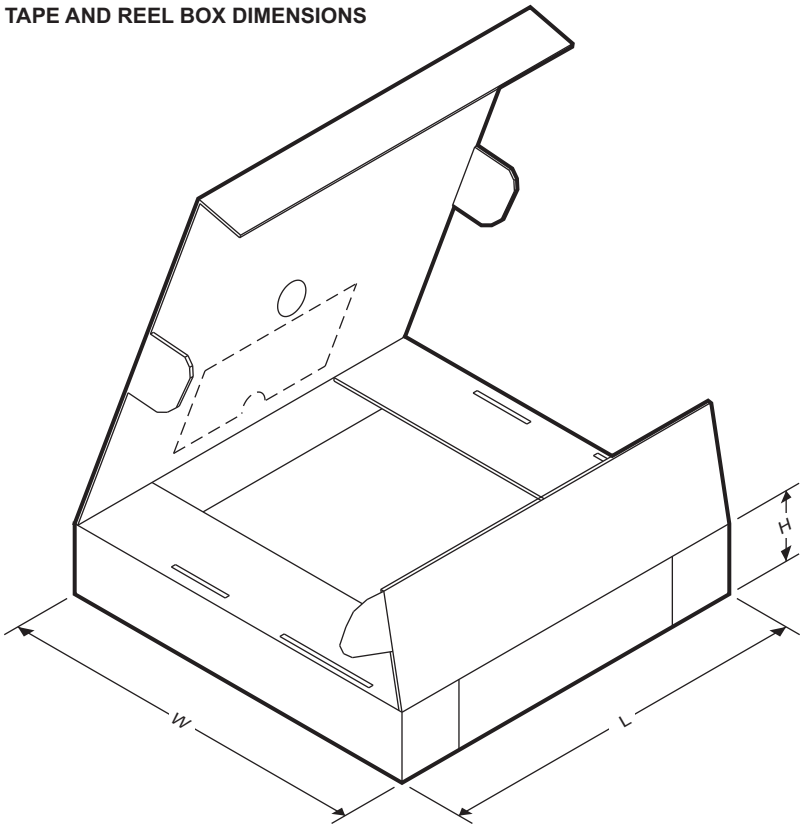


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8962DDWR	HTSSOP	DDW	44	2500	330	24.4	8.9	14.7	1.4	12	24	Q1
DRV8962DDVR	HTSSOP	DDV	44	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8962DDWR	HTSSOP	DDW	44	2500	367.0	367.0	45.0
DRV8962DDVR	HTSSOP	DDV	44	2500	367.0	367.0	45.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV8962DDWR	ACTIVE	HTSSOP	DDW	44	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

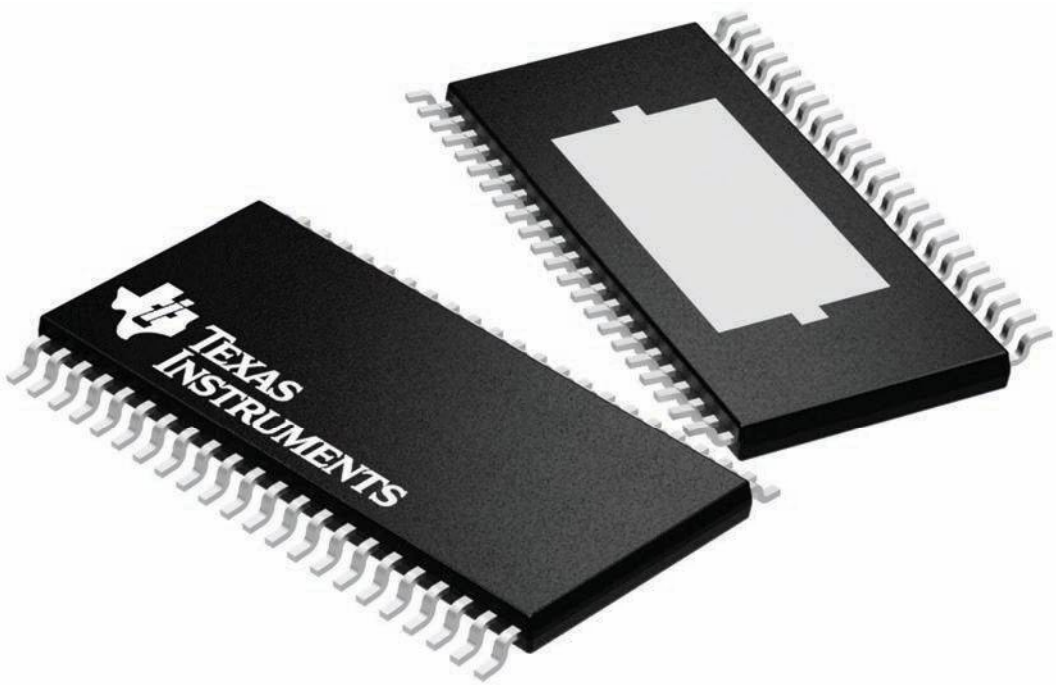
DDW 44

PowerPAD TSSOP - 1.2 mm max height

6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

ESD752 and ESD7x2 24-V, 2-Channel, ESD Protection With 5.7 A of 8/20 µs Surge Protection in a SOT-23 and SOT-323 / SC-70 Package

1 Features

- Robust surge protection:
  - IEC 61000-4-5 (8/20 µs): 5.7 A
- IEC 61000-4-2 level 4 ESD protection:
  - ±30-kV or ±20-kV contact discharge
  - ±30-kV or ±20-kV air-gap discharge
- 24 V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD and surge protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 3 pF or 1.7 pF (typical)
- SOT-23 (DBZ) small, standard, common footprint
- SOT-323 / SC-70 (DCK) very small, standard, space saving, common footprint
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial control networks:
  - Smart distribution system (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4
  - 4/20 mA circuits
  - PLC surge protection
  - ADC surge protection

3 Description

The ESD752 and ESD7x2 are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The ESD752 and ESD7x2 are rated to dissipate contact ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 level 4 standard (±30-kV or ±20-kV contact and ±30-kV or ±20-kV airgap). The low dynamic resistance and low clamping voltage ensures system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

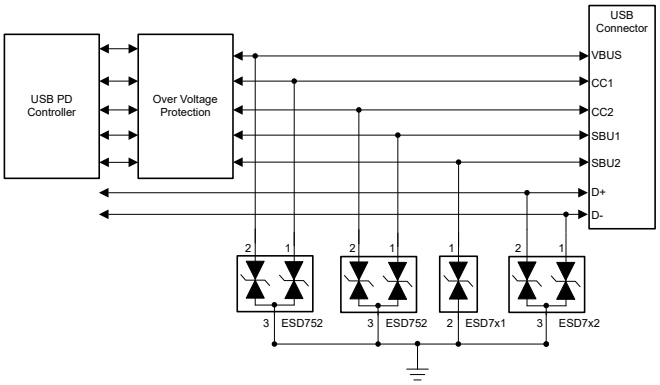
These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The I_{PP} = 5.7 A (8/20 µs surge waveform) capability of the ESD752 makes it suitable for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 3 pF or 1.7 pF line capacitance of the ESD752 and ESD7x2 are suitable for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

The ESD752 and ESD7x2 are offered in two leaded packages for easy flow through routing.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD752	DCK (SOT-323 / SC-70, 3)	2.00 mm × 1.25 mm
	DBZ (SOT-23, 3)	2.92 mm × 1.30 mm
ESD7x2	DBZ (SOT-23, 3)	2.92 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



USB Power Delivery Typical Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (August 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

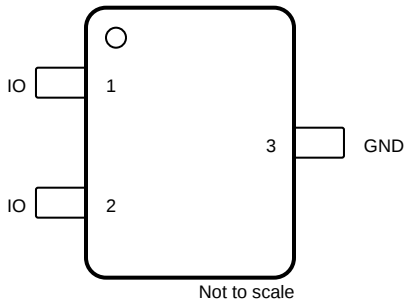


Figure 5-1. DCK and DBZ Package, 3-Pin SOT-323 / SC-70 and SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	—	Connect to ground.

(1) I/O = Input or Output,

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		DEVICE	MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD752		210	W
	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C	ESD752		5.7	A
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	°C
T_{stg}	Storage temperature		-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

6.3 ESD Ratings—IEC Specification

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD752	±30000	V
		IEC 61000-4-2 Air Discharge, all pins		±30000	

6.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	−24		24	V
T_A	Operating free-air temperature	−55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD752		ESD7x2	UNIT
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	
		3 PINS	3PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.5	283.0	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.1	164.1	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	131.1	105.1	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.0	67.1	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	130.2	104.4	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		ESD752	–24		24	V
V_{BRF}	Forward breakdown voltage(2)	I_{IO} = 10 mA, IO to GND	ESD752	25.5		35.5	V
V_{BRR}	Reverse breakdown voltage(2)	I_{IO} = –10 mA, IO to GND	ESD752	–35.5		–25.5	V
V_{CLAMP}	Clamping voltage(4)	I_{PP} = 5.7 A, t_p = 8/20 µs, IO to GND	ESD752		37		V
	Clamping voltage(5)	I_{PP} = 16 A, TLP, IO to GND or GND to IO			35		
V_{Hold}	Holding voltage after snapback(3)	TLP	ESD752		30		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND	ESD752	-50	5	50	nA
R_{DYN}	Dynamic resistance(5)	IO to GND	ESD752		0.35		Ω
		GND to IO			0.35		
C_L	Line capacitance(6)	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV	ESD752		3	5	pF

(1) Measurements made on both IO channels.
(2) V_{BRF} and V_{BRR} are defined as the voltage when ± 10 mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.
(3) V_{HOLD} is defined as the lowest voltage on the TLP plot once the trigger threshold is reached and the device snapbacks and begins clamping the voltage.
(4) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(5) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.
(6) Measured from IO to GND on both channels.

6.7 Typical Characteristics

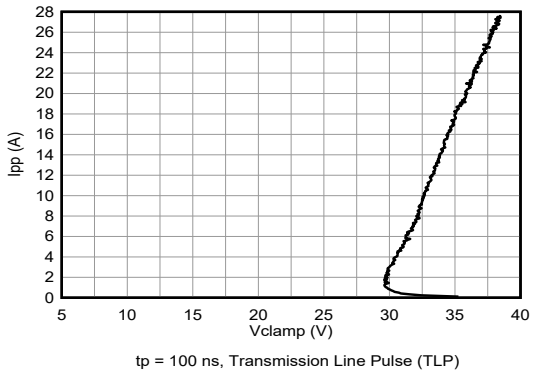


Figure 6-1. Positive TLP Curve

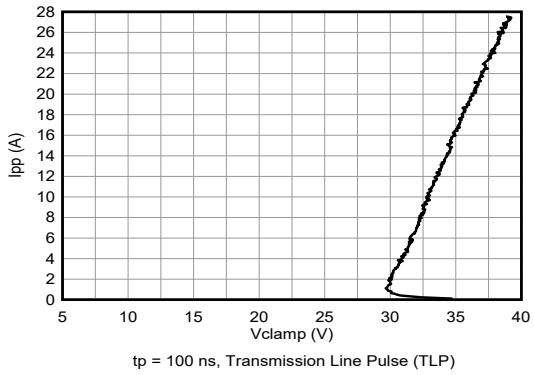


Figure 6-2. Negative TLP Curve

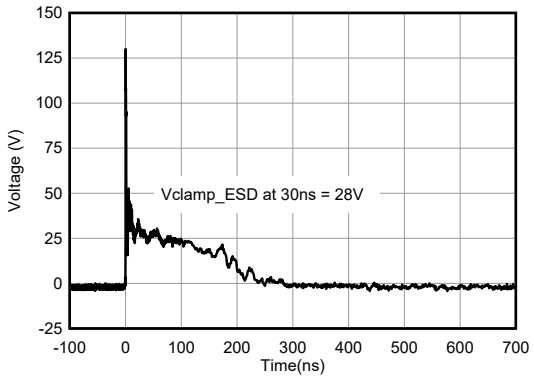


Figure 6-3. +8-kV Clamped IEC Waveform

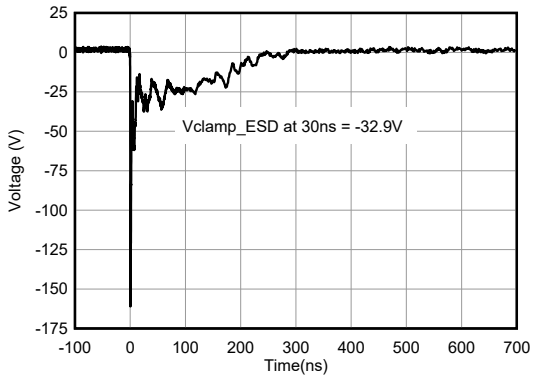


Figure 6-4. −8-kV Clamped IEC Waveform

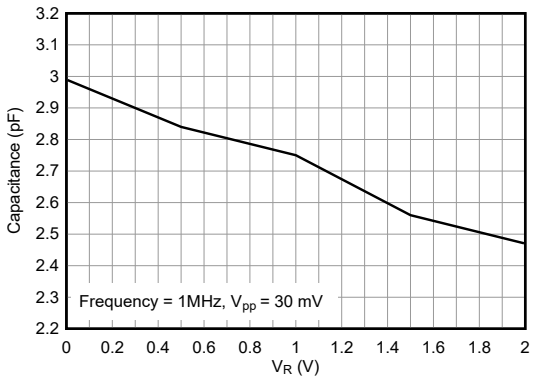


Figure 6-5. Capacitance vs. Bias Voltage

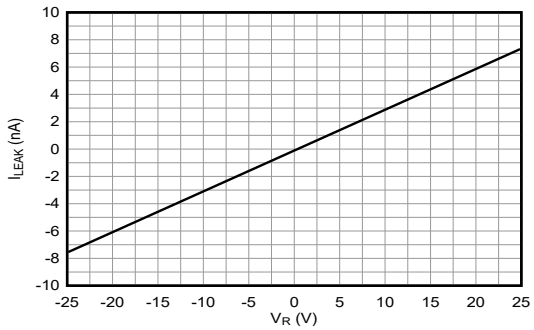


Figure 6-6. Leakage Current vs. Bias Voltage Across Temperature

6.7 Typical Characteristics (continued)

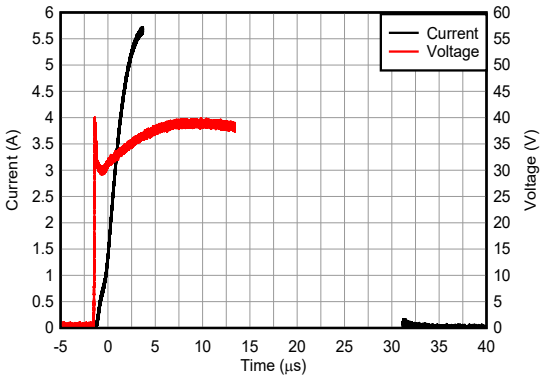


Figure 6-7. 8/20 µs Surge Response at 5.7 A

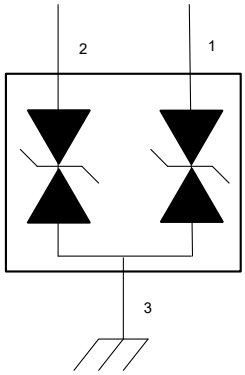
7 Detailed Description

7.1 Overview

The ESD752 and ESD7x2 are dual-channel ESD TVS diodes in SOT-23 and SOT-323 (SC-70) leaded packages which are convenient for automatic optical inspection. This product offers IEC 61000-4-2 ±30-kV or ±20-kV air-gap, ±30-kV or ±20-kV contact ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The I_{PP} = 5.7 A (8/20 µs surge waveform) capability of the ESD752 makes it suitable for protecting VBUS. The ESD752 device is also a good fit for protecting industrial IOs requiring 5.7 A or less of surge current protection. The 3 pF or 1.7 pF line capacitance of these ESD protection diodes are suitable for USB-PD slower speed signals and industrial IO applications.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD752 and ESD7x2 are bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to ±30-kV or ±20-kV contact and ±30-kV or ±20-kV air-gap respectively as specified in the IEC 61000-4-2 standard. The ESD752 and ESD7x2 can also handle up to 5.7 A or 1.5 A of surge current (IEC 61000-4-5 8/20 µs) respectively. The I/O capacitance of 3 pF or 1.7 pF are suitable for USB power delivery slower speed signals and industrial applications. These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the ESD752 clamping voltage is only 37 V when the device is taking 5.7 A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 and SOT-323 (SC-70) packages are good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

These devices are qualified to operate from –55°C to +150°C.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.7 A and 1.5 A (8/20 µs waveform) for the ESD752 and ESD7x2 respectively. An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between the I/O pins is 3 pF and 1.7 pF for the ESD752 and ESD7x2 respectively. These capacitances are suitable for USB power delivery slower speed signals and industrial applications.

7.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.35 Ω for the ESD752 device, and 0.57 Ω for the ESD7x2 device, which prevents system damage during ESD events.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 24 V.

7.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of ± 24 V.

7.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 5.7 A for 8/20 µs surge waveform), 35 V (I_{PP} = 16 A for TLP), 36 V (I_{PP} = 1.5 A for 8/20 µs surge waveform), and 38 V (I_{PP} = 16 A for TLP) for the ESD752 and ESD7x2, respectively.

7.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and SC-70 (DCK) leaded packages for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD752 and ESD7x2 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below V_{RWM}, and activate when the voltage between IO and GND goes above V_{BR}. During IEC 61000-4-2 ESD events, transient voltages as high as ±30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD752 and ESD7x2 are dual channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

8.2 Typical Application

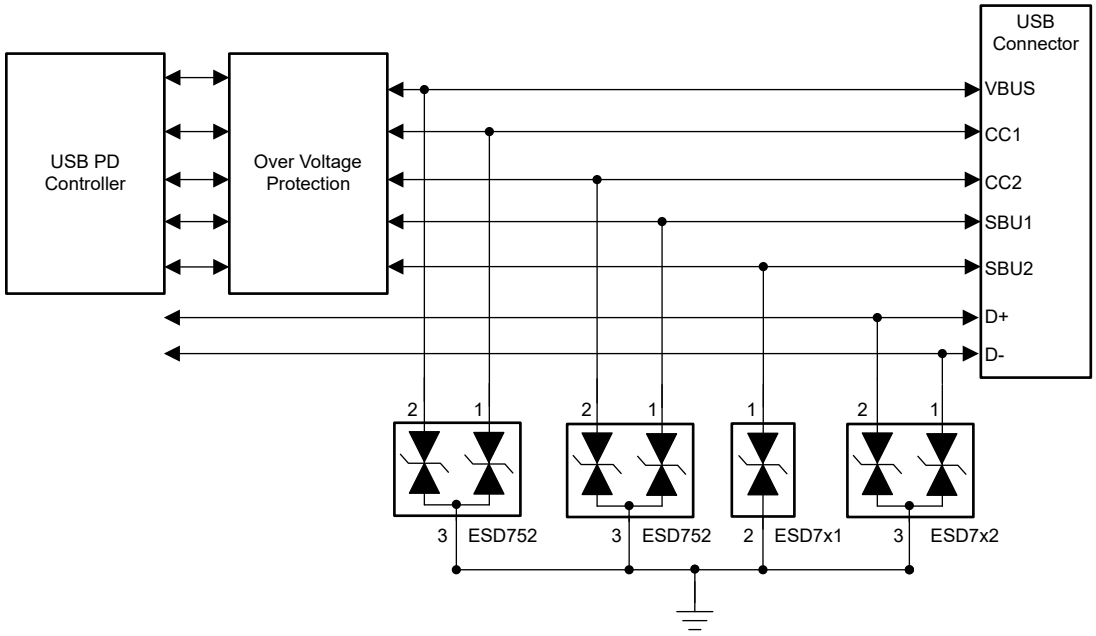


Figure 8-1. USB Power Delivery Typical Application

8.2.1 Application

8.2.2 Design Requirements

For this design example, the ESD752 and ESD7x2 are used to provide ESD protection on a USB-PD connector. Table 8-1 lists the known design parameters for this application.

Table 8-1. Design Parameters for the USB Power Delivery Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20 V
V_{IO} signal range	+ 3.3 V
V_{RWM}	± 24 V
Short to VBUS event on V_{IO}	± 20 V
Data rate	Up to 480 Mbps

8.2.3 Detailed Design Procedure

The ESD752 and ESD7x2 has a V_{RWM} of ± 24 V to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic ensures both positive and negative polarity are protected. The low 1.7 pF capacitance of the ESD7x2 device ensures data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD752 has an I_{PP} = 5.7 A (8/20 µs) surge current capability making it suitable for protecting the VBUS power rail.

8.2.4 Application Curves

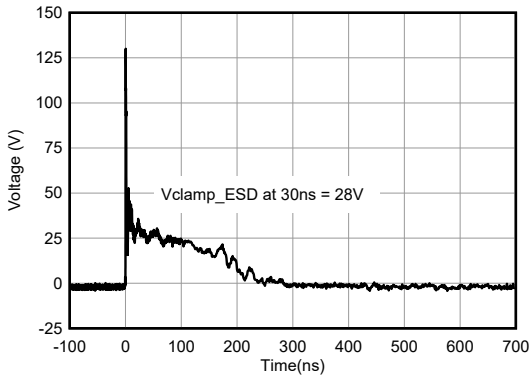


Figure 8-2. +8-kV Clamped IEC Waveform

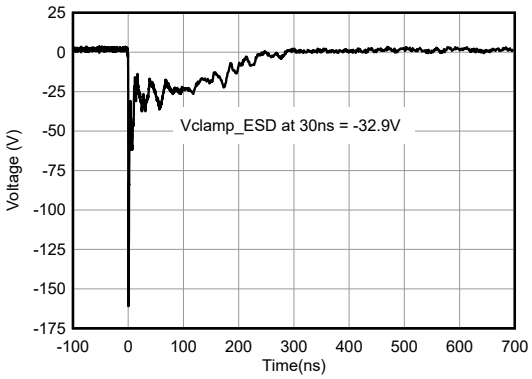


Figure 8-3. −8-kV Clamped IEC Waveform

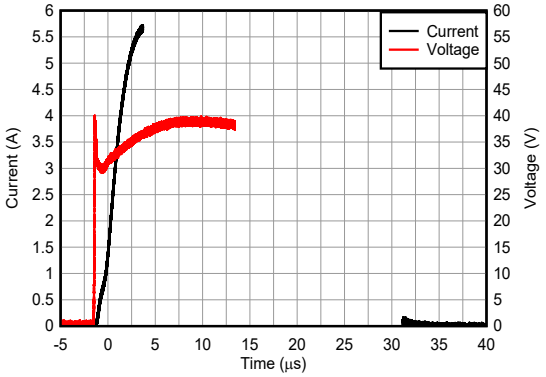


Figure 8-4. 8/20 µs Surge Response at 5.7 A

9 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This is a typical example of a dual channel IO routing.

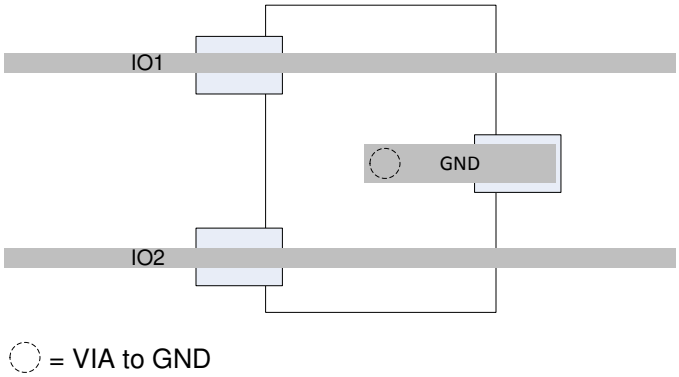


Figure 10-1. Routing with DBZ and DCK Package

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD752DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8	Samples
PESD752DBZR	ACTIVE	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-55 to 150		Samples
PESD752DCKR	ACTIVE	SC70	DCK	3	3000	TBD	Call TI	Call TI	-55 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

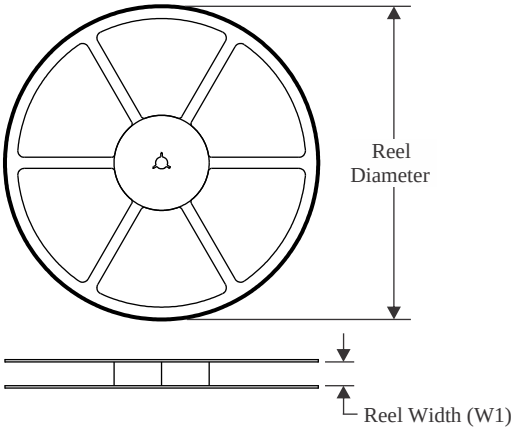
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

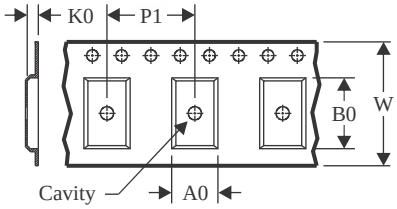
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

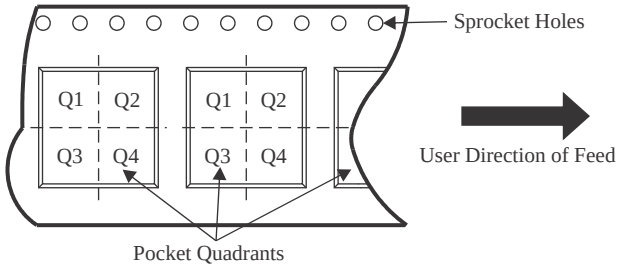


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

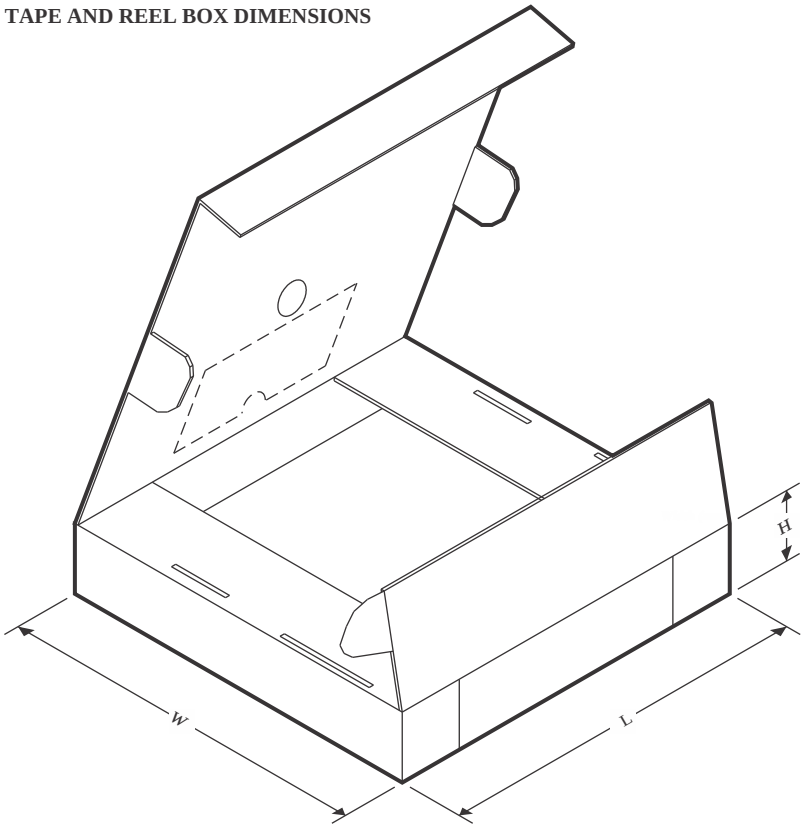
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD752DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



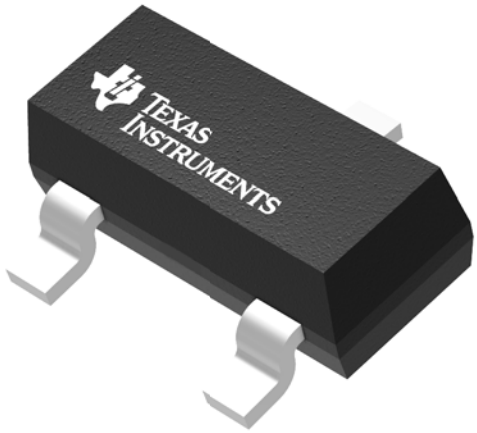
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD752DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



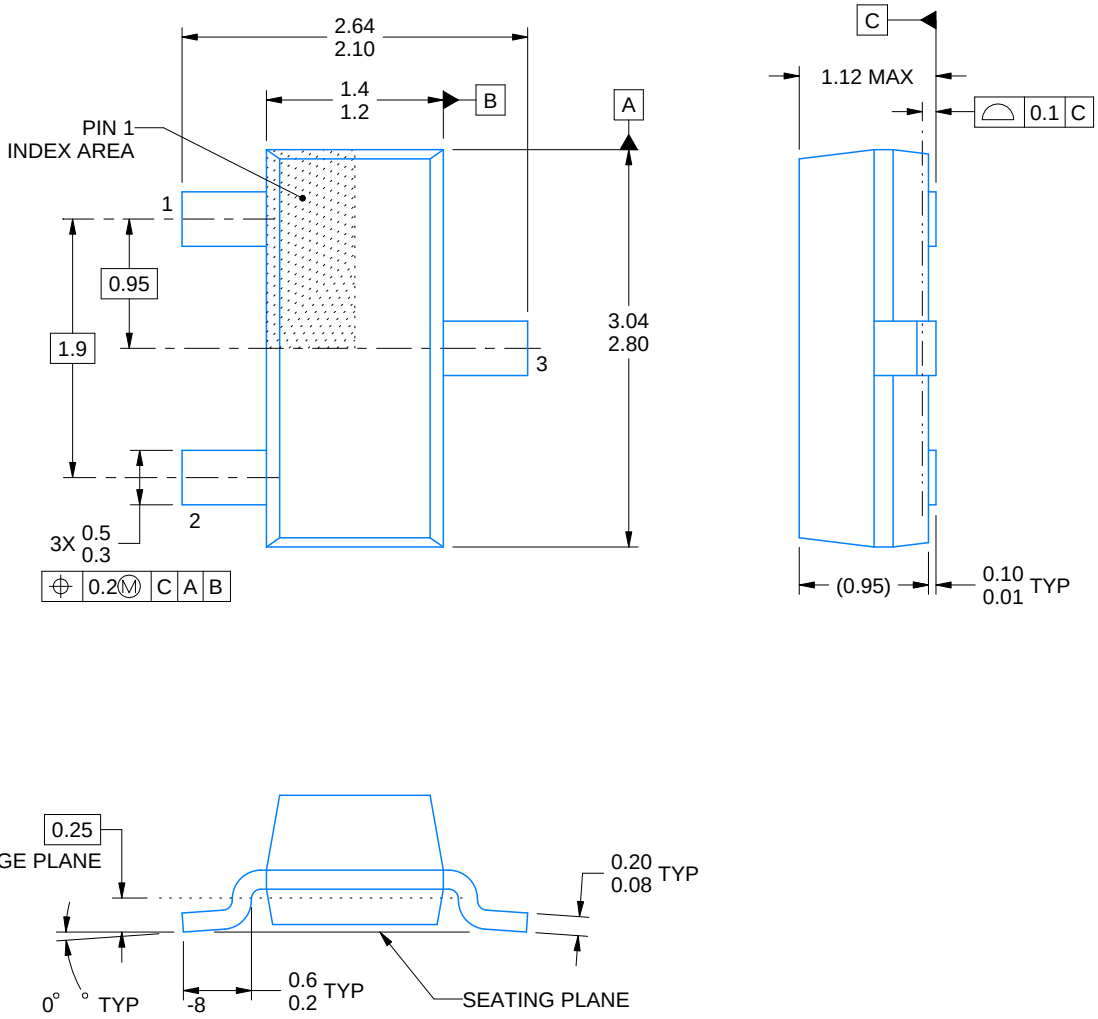
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

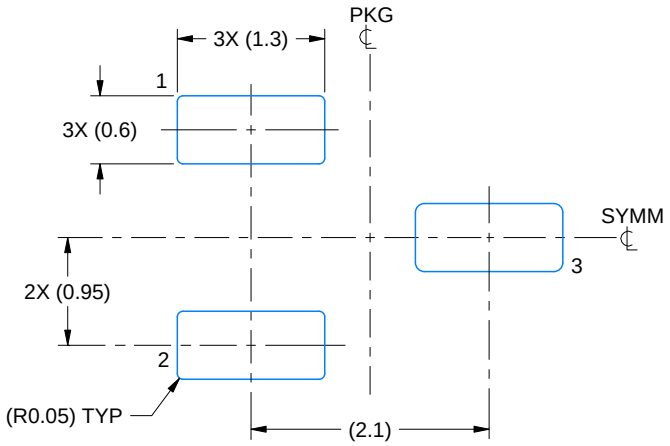
SMALL OUTLINE TRANSISTOR



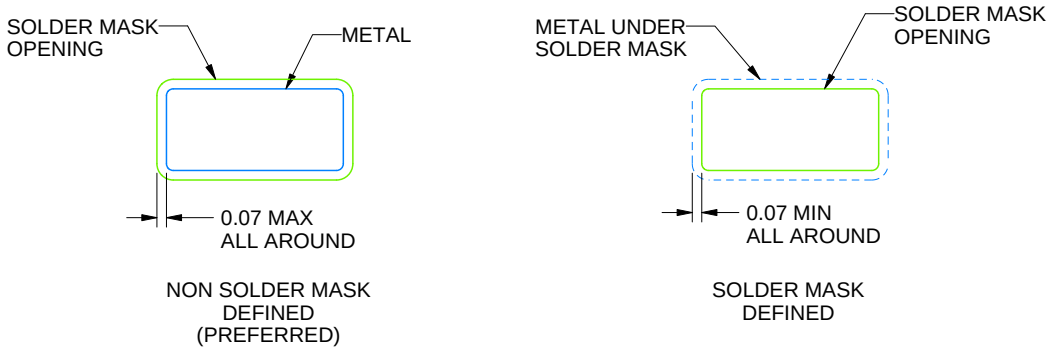
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

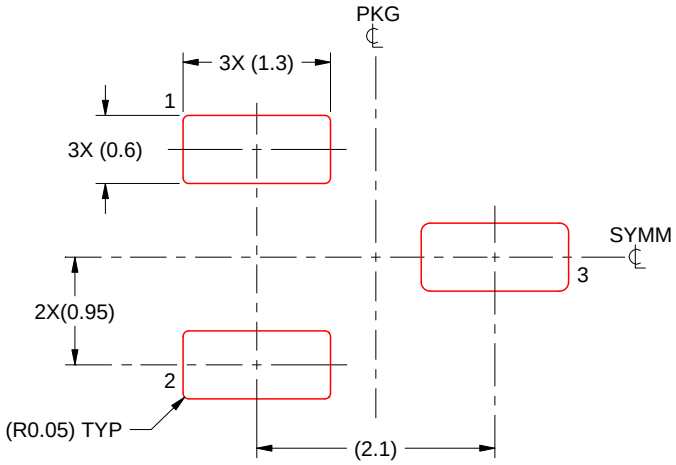


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

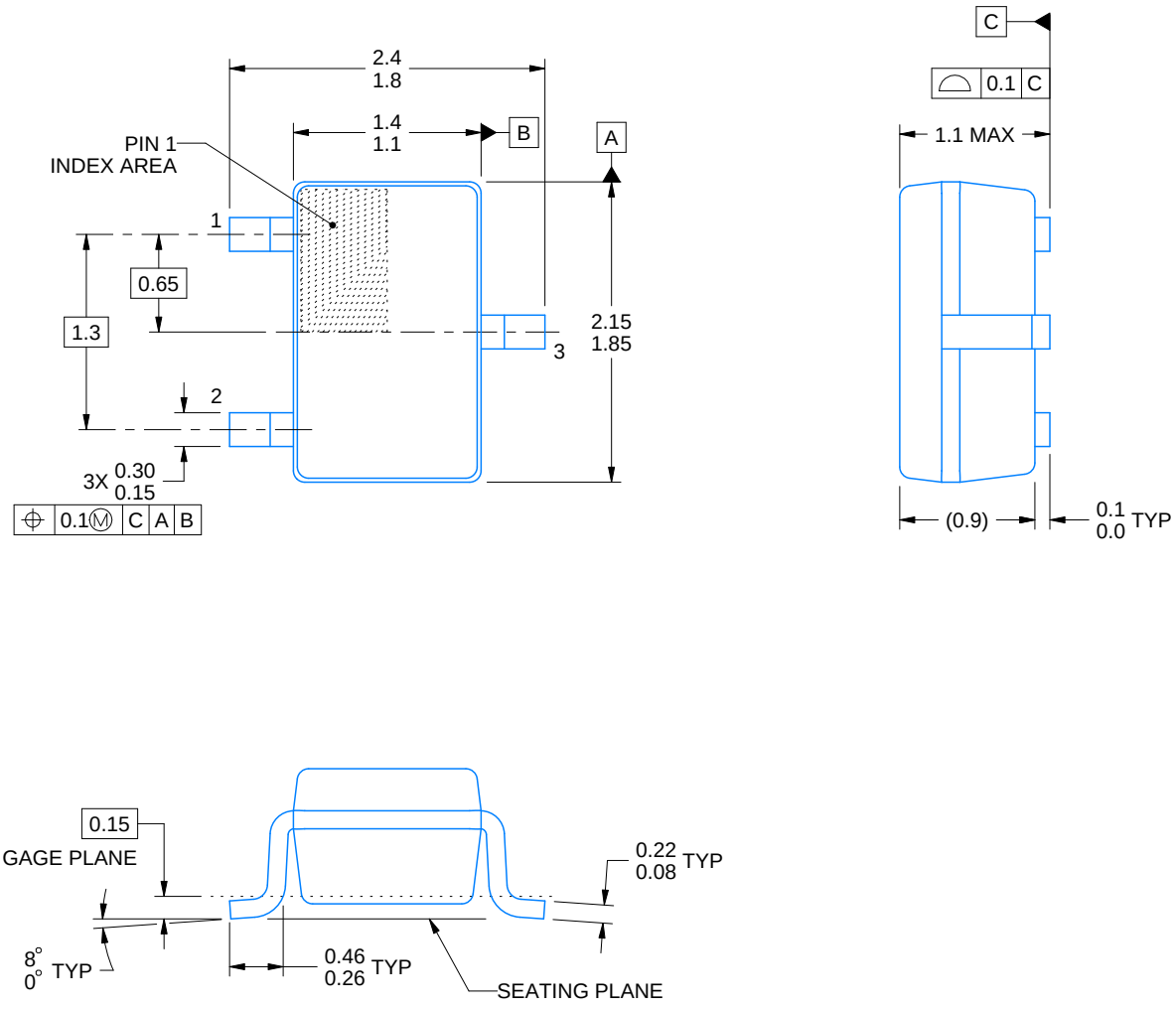
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

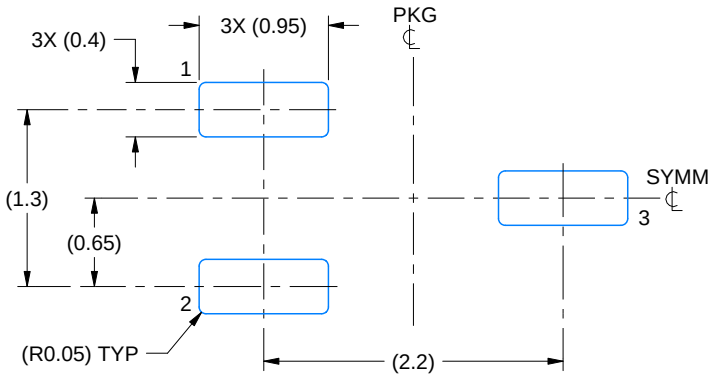
SMALL OUTLINE TRANSISTOR SC70



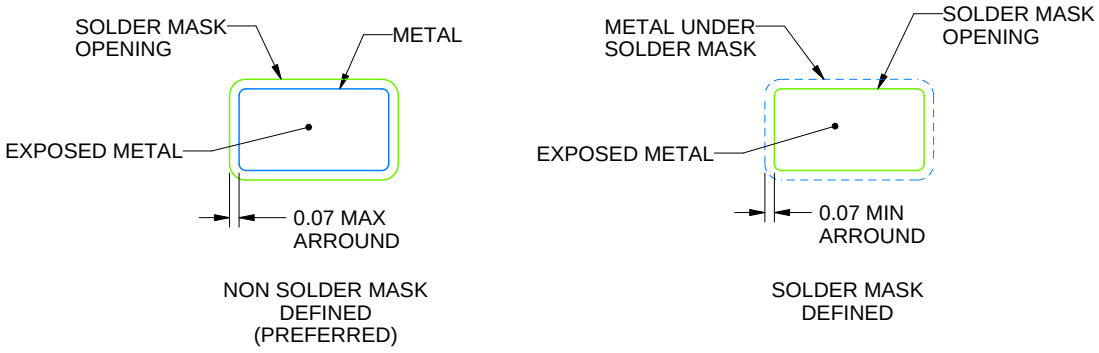
4220745/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4220745/C 06/2021

NOTES: (continued)

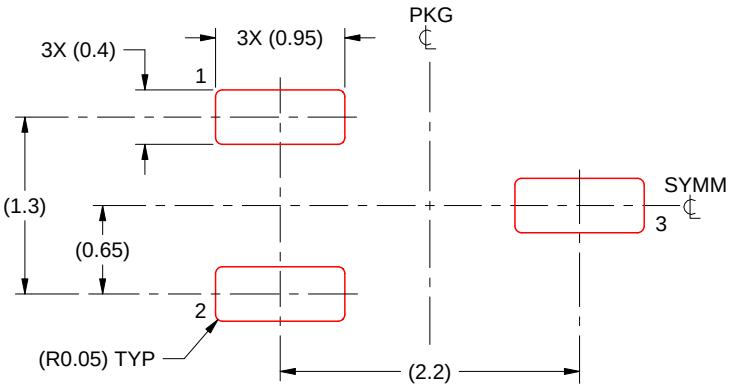
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

INA186 Bidirectional, Low-Power, Zero-Drift, Wide Dynamic Range, Current-Sense Amplifier With Enable

1 Features

- Wide common-mode voltage range, V_{CM}: –0.2 V to +40 V
- Low input bias currents, I_{IB}: 500 pA (typical) (enables microamp current measurement)
- Low power:
  - Low supply voltage, V_S: 1.7 V to 5.5 V
  - Low quiescent current, I_Q: 48 µA (typical)
- Accuracy:
  - Common-mode rejection ratio: 120 dB (minimum)
  - Gain error, E_G: ±1% (maximum)
  - Gain drift: 10 ppm/°C (maximum)
  - Offset voltage, V_{OS}: ±50 µV (maximum)
  - Offset drift: 0.5 µV/°C (maximum)
- Bidirectional current sensing capability
- Gain options:
  - INA186A1: 25 V/V
  - INA186A2: 50 V/V
  - INA186A3: 100 V/V
  - INA186A4: 200 V/V
  - INA186A5: 500 V/V

2 Applications

- Standard notebook PC
- Smartphone
- Consumer battery charger
- Baseband unit (BBU)
- Merchant network and server PSU
- Battery test

3 Description

The INA186 is a low-power, voltage-output, current-sense amplifier (also called a current-shunt monitor). This device is commonly used for overcurrent protection, precision current measurement for system optimization, or in closed-loop feedback circuits. The INA186 can sense drops across shunts at common-mode voltages from –0.2 V to +40 V, independent of the supply voltage.

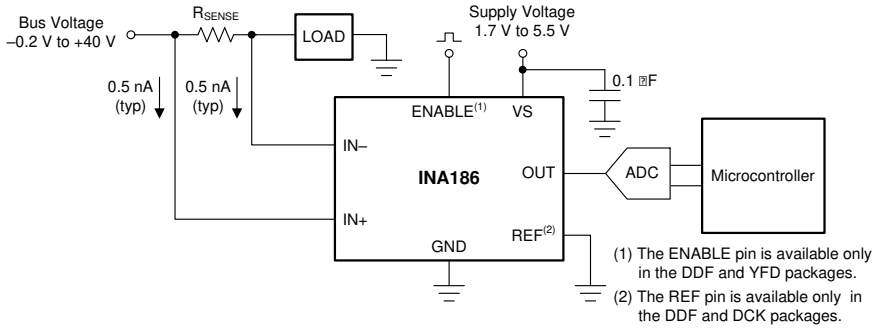
The low input bias current of the INA186 permits the use of larger current-sense resistors, thus providing accurate current measurements in the microamp range. The low offset voltage of the zero-drift architecture extends the dynamic range of the current measurement. This feature allows for smaller sense resistors with lower power loss, while still providing accurate current measurements.

The INA186 operates from a single 1.7-V to 5.5-V power supply, and draws a maximum of 90 µA of supply current . Five fixed gain options are available: 25 V/V, 50 V/V, 100 V/V, 200 V/V, or 500 V/V. The device is specified over the operating temperature range of –40°C to +125°C, and offered in SC70, SOT-23-THIN, and DSBGA packages. The SC70 and SOT-23 (DDF) packages support bidirectional current measurement, whereas the DSBGA package only supports current measurement in one direction.

Table 3-1. Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA186	SC70 (6)	2.00 mm × 1.25 mm
	SOT-23 (8)	2.90 mm × 1.60 mm
	DSBGA (6)	1.17 mm × 0.765 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Typical Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2019) to Revision B (July 2021)	Page
• Added the YFD (DSBGA) package and associated content to data sheet	1
• Changed *Overview* section	11
• Added ENABLE pin information to the *Functional Block Diagram*	11
• Added REF pin information to the *Bidirectional Current Monitoring* section	12
• Changed graphics in the *Basic Connections* section	18
• Added REF pin information to the R_{SENSE} *and Device Gain Selection* section	19
• Added the YFD (DSBGA) layout example to *Layout Examples*	25

Changes from Revision * (April 2019) to Revision A (November 2019)	Page
• Added DDF (SOT-23) package and associated content to data sheet	1

5 Pin Configuration and Functions

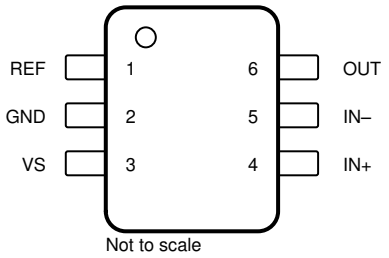


Figure 5-1. DCK Package 6-Pin SC70 Top View

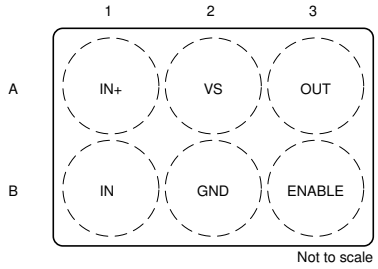


Figure 5-2. YFD Package 6-Pin DSBGA Top View

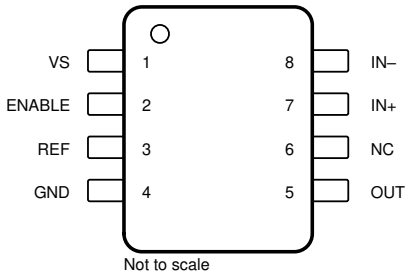


Figure 5-3. DDF Package 8-Pin SOT-23 Top View

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DCK (SC70)	DDF (SOT-23)	YFD (DSBGA)		
ENABLE	—	2	B3	Digital input	Enable Pin. When this pin is driven to VS, the device is on and functions as a current sense amplifier. When this pin is driven to GND, the device is off, the supply current is reduced, and the output is placed in a high-impedance state. This pin must be driven externally, or connected to VS if not used. DDF and YFD packages only.
GND	2	4	B2	Analog	Ground
IN–	5	8	B1	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	4	7	A1	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
NC	—	6	—	—	No internal connection. Can be left floating, grounded, or connected to supply.
OUT	6	5	A3	Analog output	OUT pin. This pin provides an analog voltage output that is the gained up voltage difference from the IN+ to the IN– pins, and is offset by the voltage applied to the REF pin.
REF	1	3	—	Analog input	Reference input. Enables bidirectional current sensing with an externally applied voltage. DCK and DDF packages only. Devices without a REF pin have the REF node grounded internally.
VS	3	1	A2	Analog	Power supply, 1.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
V_{IN+}, $V_{IN–}$	Analog inputs	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–42	42	V
		V_{IN+}, $V_{IN–}$, with respect to GND(3)	GND – 0.3	42	
V_{ENABLE}	ENABLE		GND – 0.3	6	V
	REF, OUT(3)		GND – 0.3	(V_S) + 0.3	V
	Input current into any pin(3)			5	mA
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	GND – 0.2		40	V
V_{IN+}, $V_{IN–}$	Input pin voltage range	GND – 0.2		40	V
V_S	Operating supply voltage	1.7		5.5	V
V_{REF}	Reference pin voltage range	GND		V_S	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA186			UNIT
		YFD (DSBGA)	DCK (SC70)	DDF (SOT23)	
		6 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.4	170.7	137.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	132.7	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.7	65.3	57.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	45.7	5.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.3	65.2	56.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25°C, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, $V_{REF} = V_S / 2$, and $V_{ENABLE} = V_S$ (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection ratio	V_{SENSE} = 0 mV, V_{IN+} = –0.1 V to 40 V, T_A = –40°C to +125°C	120	150		dB
V_{OS}	Offset voltage, RTI(1)	V_S = 1.8 V, V_{SENSE} = 0 mV		–3	±50	µV
dV_{OS}/dT	Offset drift, RTI	V_{SENSE} = 0 mV, T_A = –40°C to +125°C		0.05	0.5	µV/°C
PSRR	Power-supply rejection ratio, RTI	V_{SENSE} = 0 mV, V_S = 1.7 V to 5.5 V		–1	±10	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV		0.5	3	nA
I_{IO}	Input offset current	V_{SENSE} = 0 mV		±0.07		nA
OUTPUT						
G	Gain	A1 devices		25		V/V
		A2 devices		50		
		A3 devices		100		
		A4 devices		200		
		A5 devices		500		
E_G	Gain error	V_{OUT} = 0.1 V to V_S – 0.1 V		–0.04%	±1%	
	Gain error drift	T_A = –40°C to +125°C		2	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.1 V to V_S – 0.1 V		±0.01%		
RVRR	Reference voltage rejection ratio	V_{REF} = 100 mV to V_S – 100 mV, T_A = –40°C to +125°C		±2	±10	µV/V
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT						
V_{SP}	Swing to V_S power-supply rail	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		(V_S) – 20	(V_S) – 40	mV
V_{SN}	Swing to GND	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = –10 mV, V_{REF} = 0 V		(V_{GND}) + 0.05	(V_{GND}) + 1	mV
V_{ZL}	Zero current output voltage	V_S = 1.8 V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C, V_{SENSE} = 0 mV, V_{REF} = 0 V		(V_{GND}) + 2	(V_{GND}) + 10	mV
FREQUENCY RESPONSE						
BW	Bandwidth	A1 devices, C_{LOAD} = 10 pF		45		kHz
		A2 devices, C_{LOAD} = 10 pF		37		
		A3 devices, C_{LOAD} = 10 pF		35		
		A4 devices, C_{LOAD} = 10 pF		33		
		A5 devices, C_{LOAD} = 10 pF		27		
SR	Slew rate	V_S = 5.0 V, V_{OUT} = 0.5 V to 4.5 V		0.3		V/µs
t_S	Settling time	From current step to within 1% of final value		30		µs
NOISE, RTI(1)						
	Voltage noise density			75		nV/√Hz
ENABLE						
I_{EN}	Leakage input current	0 V ≤ V_{ENABLE} ≤ V_S		1	100	nA
V_{IH}	High-level input voltage	DDF Package	0.7 × V_S		6	V
V_{IL}	Low-level input voltage		0		0.3 × V_S	V
V_{HYS}	Hysteresis			300		mV
V_{IH}	High-level input voltage	YFD package	1.35		5.5	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{HYS}	Hysteresis			100		mV
I_{ODIS}	Output leakage disabled	V_S = 5.0 V, V_{OUT} = 0 V to 5.0 V, V_{ENABLE} = 0 V		1	5	µA
POWER SUPPLY						
I_Q	Quiescent current	V_S = 1.8 V, V_{SENSE} = 0 mV		48	65	µA
		V_S = 1.8 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C			90	µA

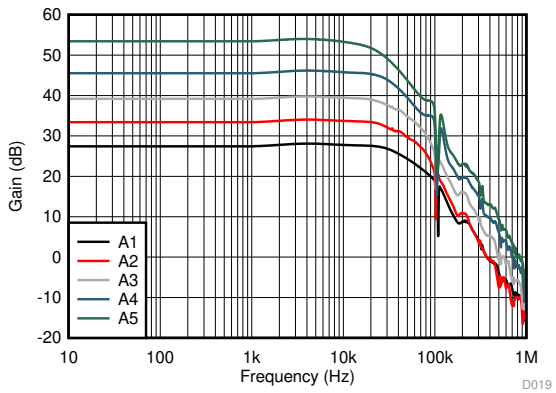
at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, and V_{ENABLE} = V_S (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{QDIS}	Quiescent current disabled	V_{ENABLE} = 0 V, V_{SENSE} = 0 mV		10	100	nA

(1) RTI = referred-to-input.

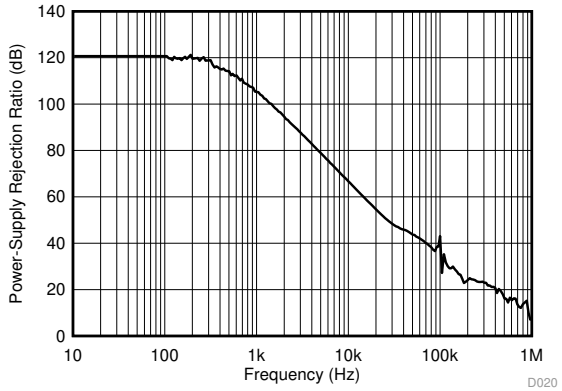
6.6 Typical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



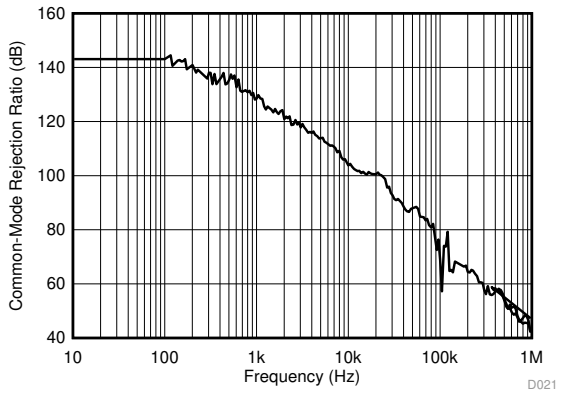
V_S = 5 V

Figure 6-1. Gain vs. Frequency



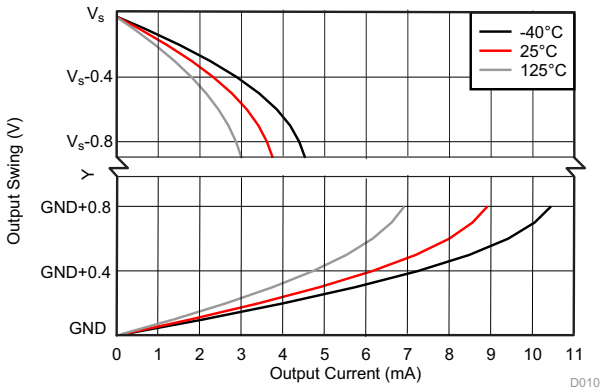
V_S = 5 V

Figure 6-2. Power-Supply Rejection Ratio vs. Frequency



A3 devices

Figure 6-3. Common-Mode Rejection Ratio vs. Frequency

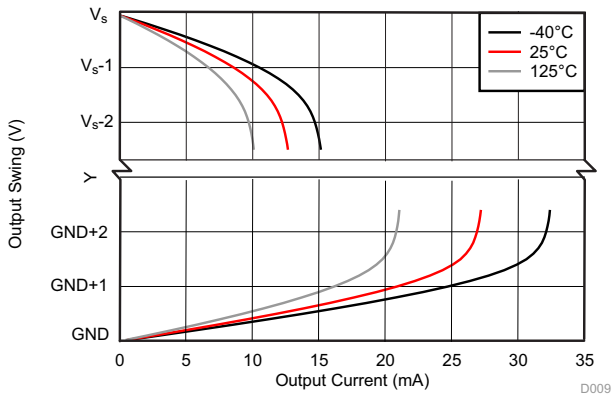


V_S = 1.8 V

Figure 6-4. Output Voltage Swing vs. Output Current

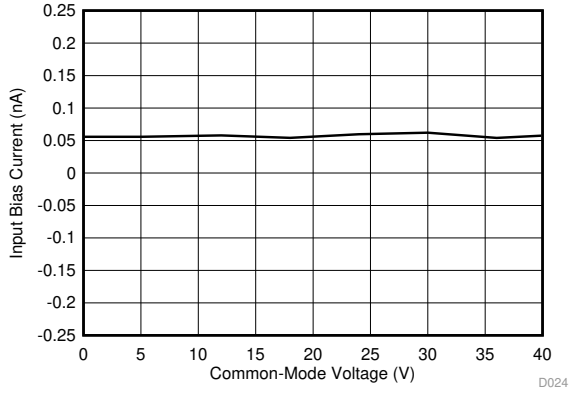
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



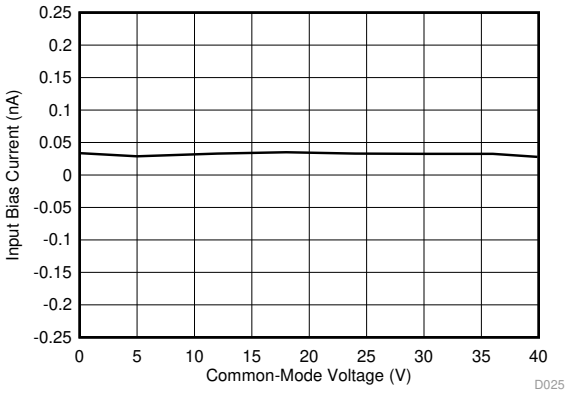
V_S = 5.0 V

Figure 6-5. Output Voltage Swing vs. Output Current



V_S = 5.0 V

Figure 6-6. Input Bias Current vs. Common-Mode Voltage



V_{ENABLE} = 0 V

Figure 6-7. Input Bias Current vs. Common-Mode Voltage (Shutdown)

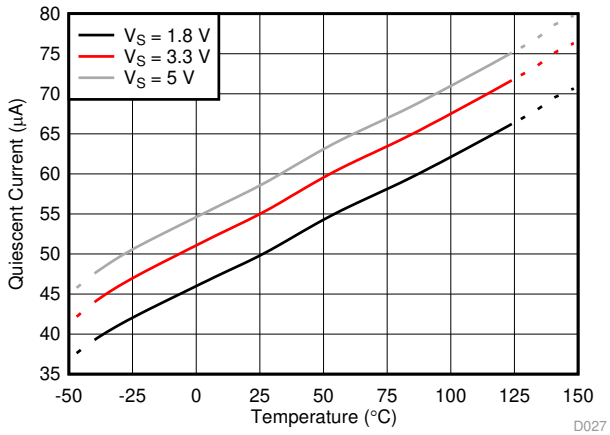
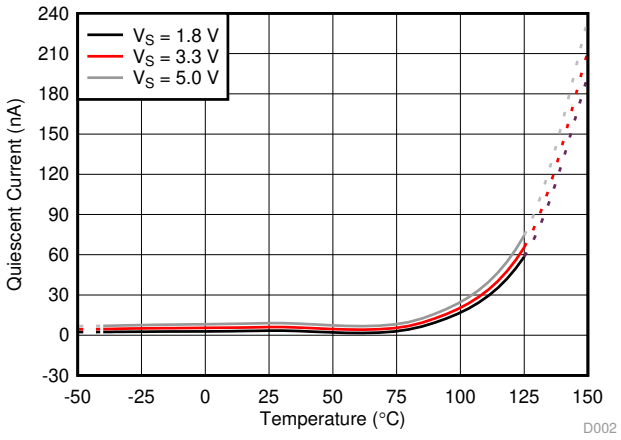
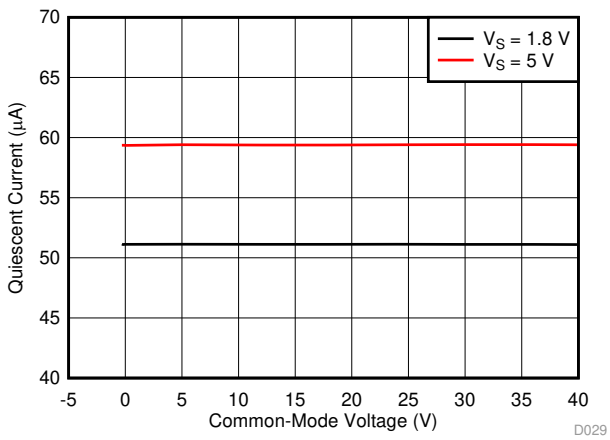


Figure 6-8. Quiescent Current vs. Temperature (Enabled)



V_{ENABLE} = 0 V

Figure 6-9. Quiescent Current vs. Temperature (Disabled)

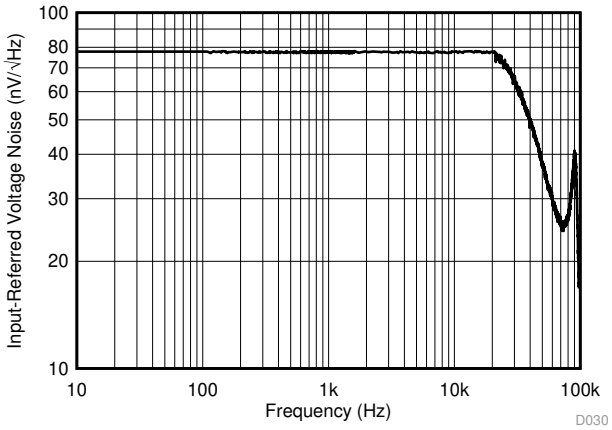


V_S = 5.0 V

Figure 6-10. Quiescent Current vs. Common-Mode Voltage

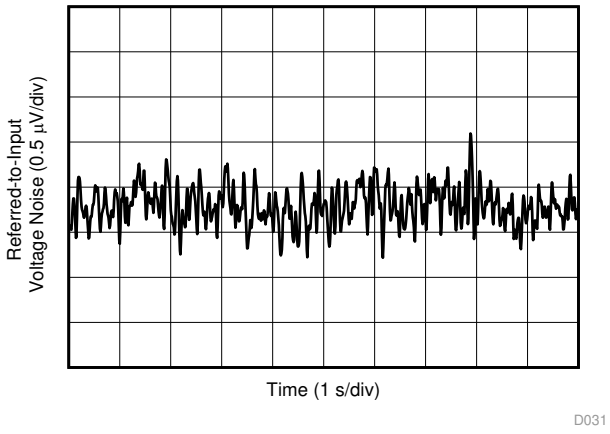
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



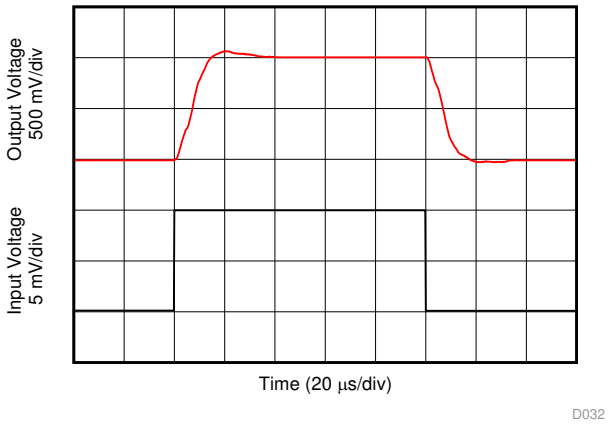
A3 devices

Figure 6-11. Input-Referred Voltage Noise vs. Frequency



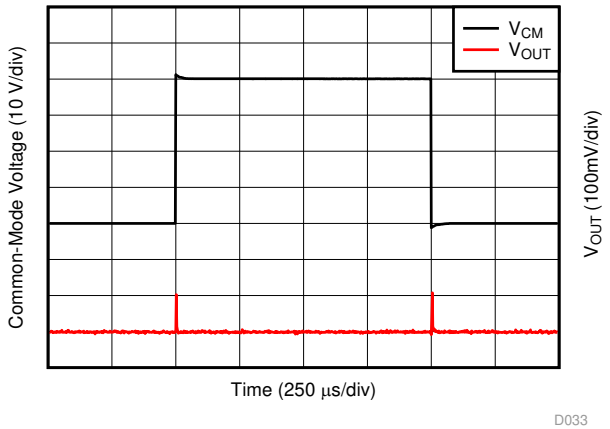
A3 devices

Figure 6-12. 0.1-Hz to 10-Hz Voltage Noise (Referred-To-Input)



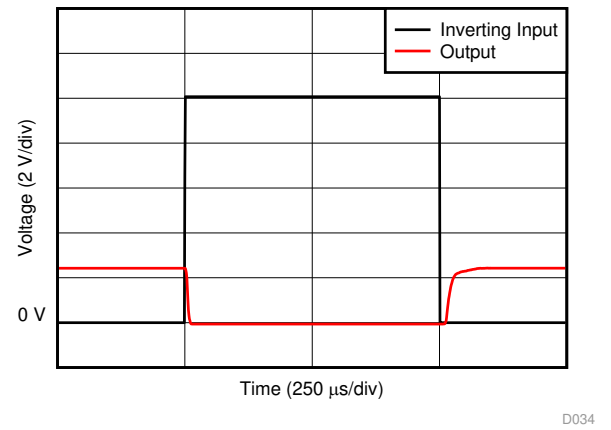
V_S = 5.0 V, A3 devices

Figure 6-13. Step Response (10-mV_{PP} Input Step)



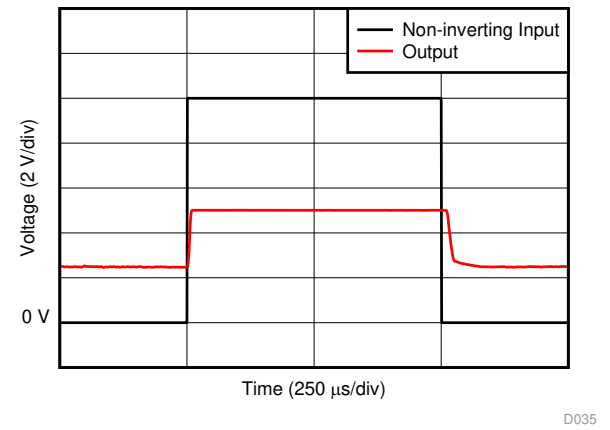
A3 devices

Figure 6-14. Common-Mode Voltage Transient Response



A3 devices

Figure 6-15. Inverting Differential Input Overload

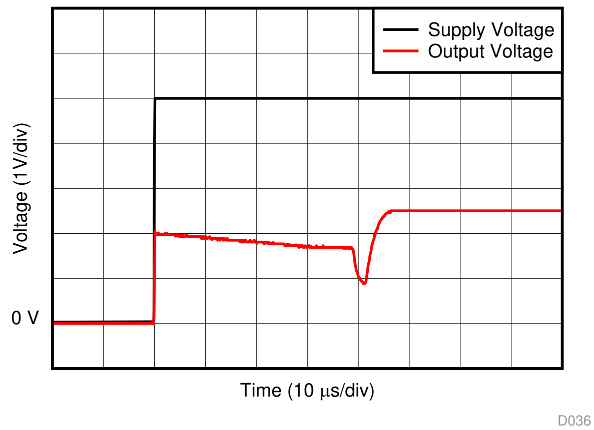


V_S = 5.0 V, A3 devices

Figure 6-16. Noninverting Differential Input Overload

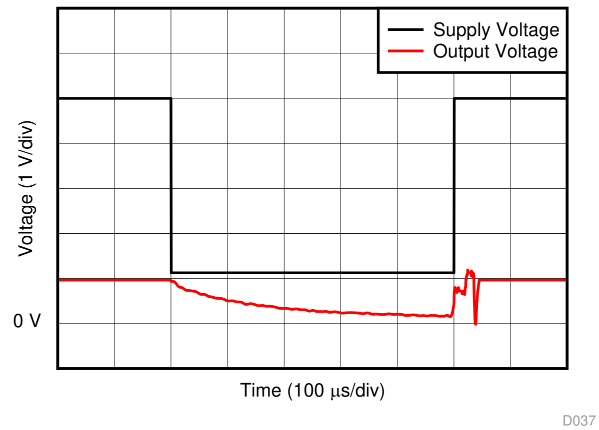
6.6 Typical Characteristics (continued)

at T_A = 25°C, $V_{SENSE} = V_{IN+} – V_{IN-}$, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, $V_{REF} = V_S / 2$, $V_{ENABLE} = V_S$, and for all gain options (unless otherwise noted)



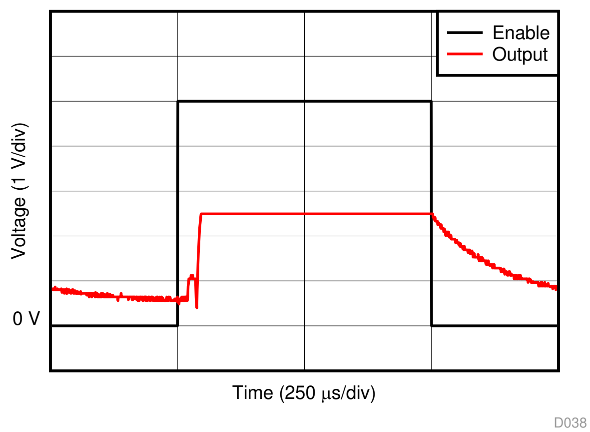
V_S = 5.0 V, A3 devices

Figure 6-17. Start-Up Response



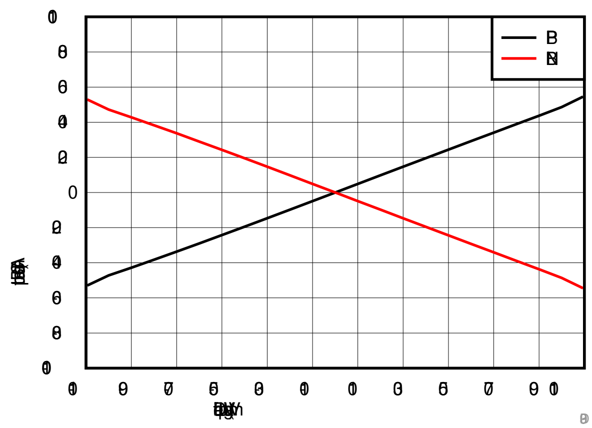
V_S = 5.0 V, A3 devices

Figure 6-18. Brownout Recovery



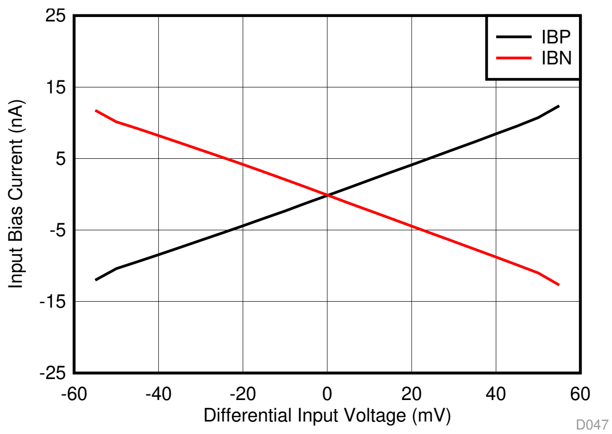
V_S = 5.0 V, A3 devices

Figure 6-19. Enable and Disable Response



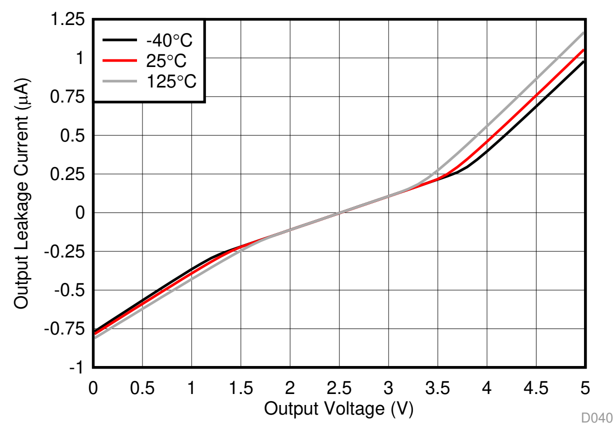
V_S = 5.0 V, V_{REF} = 2.5 V, A1 devices

Figure 6-20. IB+ and IB– vs. Differential Input Voltage



V_S = 5.0 V, V_{REF} = 2.5 V, A2, A3, A4, A5 devices

Figure 6-21. IB+ and IB– vs. Differential Input Voltage

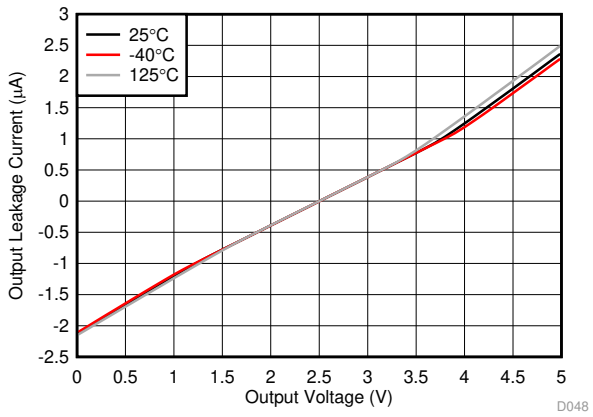


V_S = 5.0 V, V_{ENABLE} = 0 V, V_{REF} = 2.5 V

Figure 6-22. Output Leakage vs. Output Voltage (A1, A2, and A3 Devices)

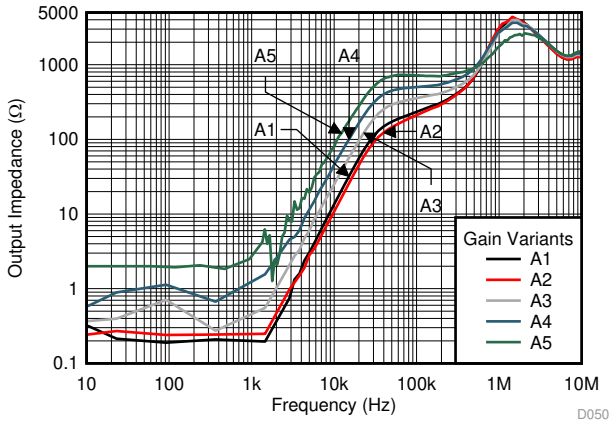
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = V_{IN+} – V_{IN-}, V_S = 1.8 V to 5.0 V, V_{IN+} = 12 V, V_{REF} = V_S / 2, V_{ENABLE} = V_S, and for all gain options (unless otherwise noted)



V_S = 5.0 V, V_{ENABLE} = 0 V, V_{REF} = 2.5 V

Figure 6-23. Output Leakage vs. Output Voltage (A4 and A5 Devices)



V_S = 5.0 V, V_{CM} = 0 V

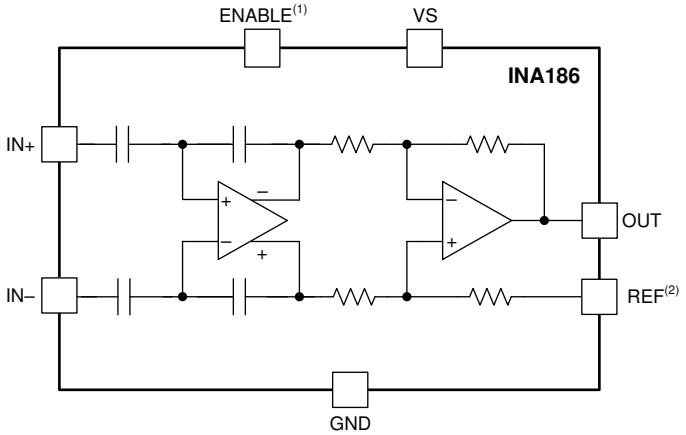
Figure 6-24. Output Impedance vs. Frequency

7 Detailed Description

7.1 Overview

The INA186 is a low bias current, low offset, 40-V common-mode, current-sensing amplifier. The DDF SOT-23 and YFD DSBGA packages also come with an enable pin. The INA186 is a specially designed, current-sensing amplifier that accurately measures voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage. Current is measured on input voltage rails as high as 40 V at V_{IN+} and $V_{IN–}$, with a supply voltage, V_S, as low as 1.7 V. When disabled, the output goes to a high-impedance state, and the supply current draw is reduced to less than 0.1 µA. The INA186 is intended for use in both low-side and high-side current-sensing configurations where high accuracy and low current consumption are required.

7.2 Functional Block Diagram



1. The ENABLE pin is available only in the DDF and YFD packages.
2. YFD packages without a REF pin have this node internally connected to GND.

7.3 Feature Description

7.3.1 Precision Current Measurement

The INA186 allows for accurate current measurements over a wide dynamic range. The high accuracy of the device is attributable to the low gain error and offset specifications. The offset voltage of the INA186 is less than ±50 µV. In this case, the low offset improves the accuracy at light loads when V_{IN+} approaches $V_{IN–}$. Another advantage of low offset is the ability to use a lower-value shunt resistor that reduces the power loss in the current-sense circuit, and improves the power efficiency of the end application.

The maximum gain error of the INA186 is specified at ±1%. As the sensed voltage becomes much larger than the offset voltage, the gain error becomes the dominant source of error in the current-sense measurement. When the device monitors currents near the full-scale output range, the total measurement error approaches the value of the gain error.

7.3.2 Low Input Bias Current

The INA186 is different from many current-sense amplifiers because this device offers very low input bias current. The low input bias current of the INA186 has three primary benefits.

The first benefit is the reduction of the current consumed by the device . Classical current-sense amplifier topologies typically consume tens of microamps of current at the inputs. For these amplifiers, the input current is the result of the resistor network that sets the gain and additional current to bias the input amplifier. To reduce the bias current to near zero, the INA186 uses a capacitively coupled amplifier on the input stage, followed by a difference amplifier on the output stage.

The second benefit of low bias current is the ability to use input filters to reject high-frequency noise before the signal is amplified. In a traditional current-sense amplifier, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias currents, input filters have little effect on the measurement accuracy of the INA186.

The third benefit of low bias current is the ability to use a larger current-sense resistor. This ability allows the device to accurately monitor currents as low as 1 µA.

7.3.3 Low Quiescent Current With Output Enable

The device features low quiescent current (I_Q), while still providing sufficient small-signal bandwidth to be usable in most applications. The quiescent current of the INA186 is only 48 µA (typical), while providing a small-signal bandwidth of 35 kHz in a gain of 100. The low I_Q and good bandwidth allow the device to be used in many portable electronic systems without excessive drain on the battery. Because many applications only need to periodically monitor current, the INA186 features an enable pin that turns off the device until needed. When in the disabled state, the INA186 typically draws 10 nA of total supply current.

7.3.4 Bidirectional Current Monitoring

The INA186 devices that feature a REF pin can sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage. Likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. Use Equation 1 to calculate the output voltage of the current-sense amplifier.

$$V_{OUT} = (I_{LOAD} \times R_{SENSE} \times GAIN) + V_{REF} \quad (1)$$

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the selected device.
- V_{REF} is the voltage applied to the REF pin.

7.3.5 High-Side and Low-Side Current Sensing

The INA186 supports input common-mode voltages from –0.2 V to +40 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S). With the ability to operate with common-mode voltages greater or less than V_S, Figure 7-1 shows an example on how the INA186 can be used in high-side and low-side current-sensing applications.

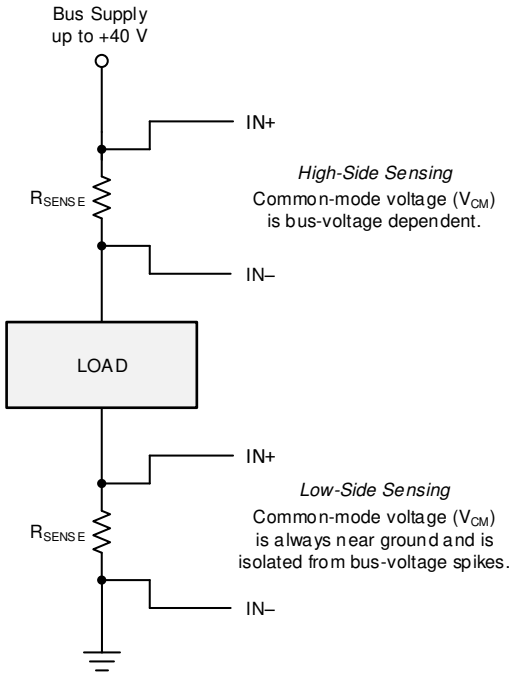


Figure 7-1. High-Side and Low-Side Sensing Connections

7.3.6 High Common-Mode Rejection

The INA186 uses a capacitively coupled amplifier on the front end. Therefore, dc common-mode voltages are blocked from downstream circuits, resulting in very high common-mode rejection. Typically, the common-mode rejection of the INA186 is approximately 150 dB. The ability to reject changes in the dc common-mode voltage allows the INA186 to monitor both high-voltage and low-voltage rail currents with very little change in the offset voltage.

7.3.7 Rail-to-Rail Output Swing

The INA186 allows linear current-sensing operation with the output close to the supply rail and ground. The maximum specified output swing to the positive rail is V_S – 40 mV, and the maximum specified output swing to GND is only GND + 1 mV. The close-to-rail output swing is useful to maximize the usable output range, particularly when operating the device from a 1.8-V supply.

7.4 Device Functional Modes

7.4.1 Normal Operation

The INA186 is in normal operation when the following conditions are met:

- The power-supply voltage (V_S) is between 1.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +40 V.
- The maximum differential input signal times the gain plus V_{REF} is less than the positive swing voltage V_{SP}.
- The ENABLE pin is driven or connected to V_S.
- The minimum differential input signal times the gain plus V_{REF} is greater than the zero load swing to GND, V_{ZL} (see *Rail-to-Rail Output Swing*).

For devices that do not feature a REF pin that value for V_{REF} will be zero. During normal operation, this device produces an output voltage that is the *amplified* representation of the difference voltage from IN+ to IN– plus the voltage applied to the REF pin.

7.4.2 Unidirectional Mode

This device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is connected. Figure 7-2 shows the most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground. When the current flows from the bus supply to the load, the input voltage from IN+ to IN– increases and causes the output voltage at the OUT pin to increase.

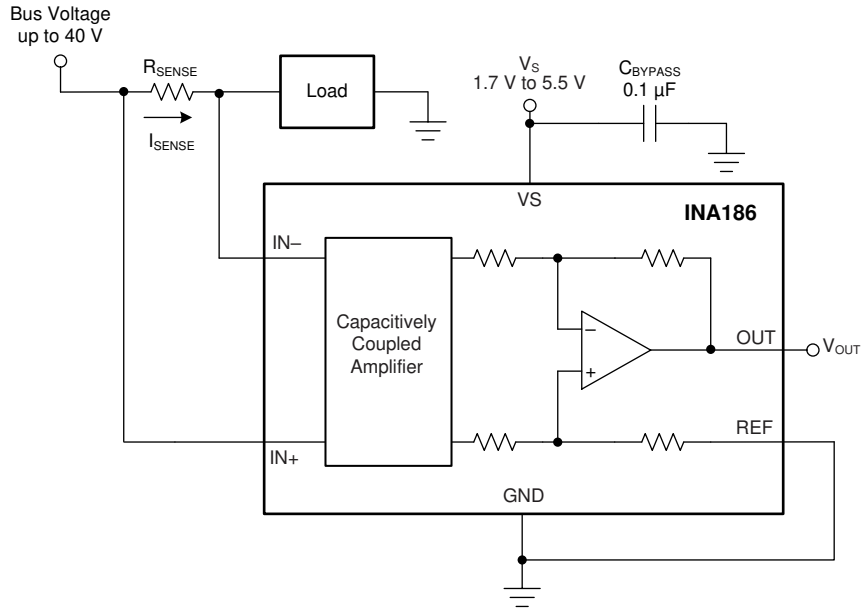


Figure 7-2. Typical Unidirectional Application

The linear range of the output stage is limited by how close the output voltage can approach ground under zero input conditions. The zero current output voltage of the INA186 is very small and for most unidirectional applications the REF pin is simply grounded. However, if the measured current multiplied by the current sense resistor and device gain is less than the zero current output voltage, then bias the REF pin to a convenient value above the zero current output voltage to get the output into the linear range of the device. To limit common-mode rejection errors, buffer the reference voltage connected to the REF pin.

A less-frequently used output biasing method is to connect the REF pin to the power-supply voltage, V_S. This method results in the output voltage saturating at 40 mV less than the supply voltage when no differential input voltage is present. This method is similar to the output saturated low condition with no differential input voltage when the REF pin is connected to ground. The output voltage in this configuration only responds to currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when

the negative differential input signal increases, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed V_S.

Another use for the REF pin in unidirectional operation is to level shift the output voltage. Figure 7-3 shows an application where the device ground is set to a negative voltage so currents biased to negative supplies, as seen in optical networking cards, can be measured. The GND of the INA186 can be set to negative voltages, as long as the inputs do not violate the common-mode range specification and the voltage difference between VS and GND does not exceed 5.5 V. In this example, the output of the INA186 is fed into a positive-biased analog-to-digital converter (ADC). By grounding the REF pin, the voltages at the output will be positive and not damage the ADC. To make sure the output voltage never goes negative, the supply sequencing must be the positive supply first, followed by the negative supply.

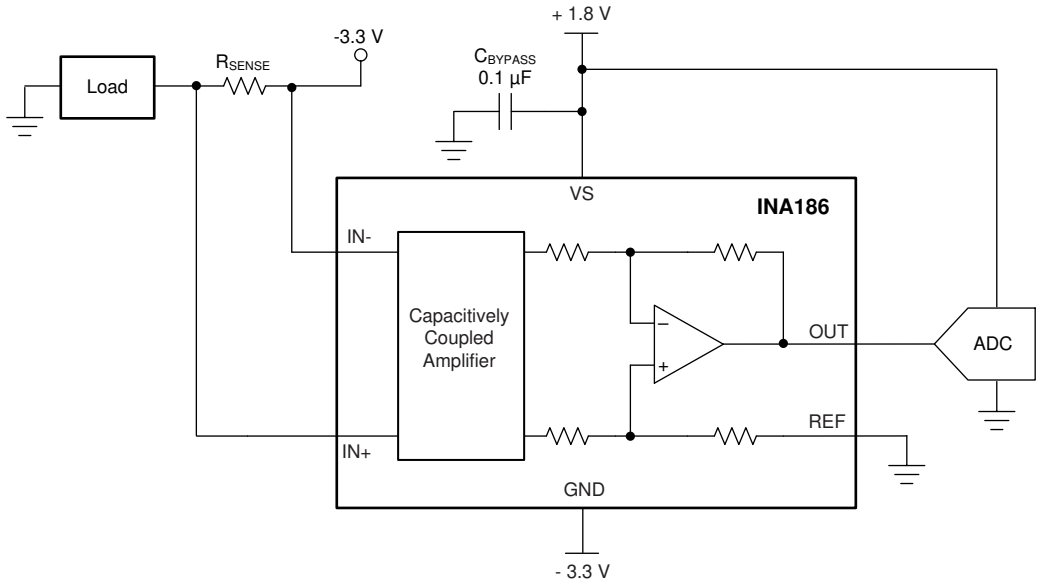


Figure 7-3. Using the REF Pin to Level-Shift Output Voltage

7.4.3 Bidirectional Mode

The INA186 is a bidirectional current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flowing through the resistor can change directions.

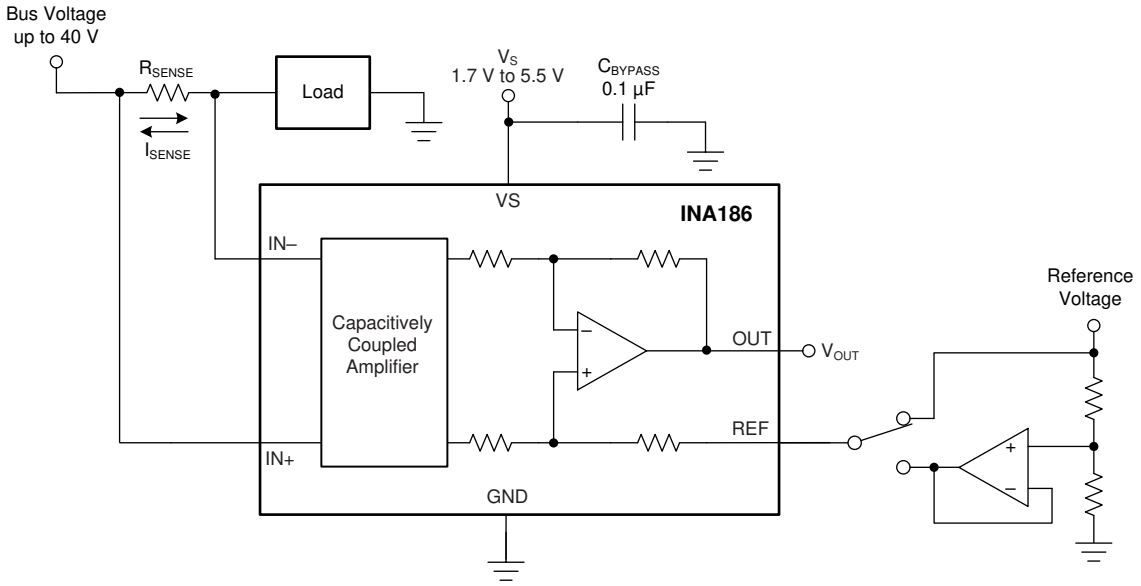


Figure 7-4. Bidirectional Application

By applying a voltage to the REF pin, Figure 7-4 shows how you can measure this current flowing in both directions. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at $V_S/2$ for equal signal range in both current directions. In some cases, V_{REF} is set at a voltage other than $V_S/2$; for example, when the bidirectional current and corresponding output signal do not need to be symmetrical.

7.4.4 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INA186 drives its output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a time-limited fault event, then the output of the INA186 returns to the expected value approximately 80 µs after the fault condition is removed.

7.4.5 Shutdown

The INA186 features an active-high ENABLE pin that shuts down the device when pulled to ground. When the device is shut down, the quiescent current is reduced to 10 nA (typical), and the output goes to a high-impedance state. In a battery-powered application, the low quiescent current extends the battery lifetime when the current measurement is not needed. When the ENABLE pin is driven to the supply voltage, the device turns back on. The typical output settling time when enabled is 130 µs.

The output of the INA186 goes to a high-impedance state when disabled. Figure 7-5 shows how to connect multiple outputs of the INA186 together to a single ADC or measurement device.

When connected in this way, enable only one INA186 at a time, and make sure all devices have the same supply voltage.

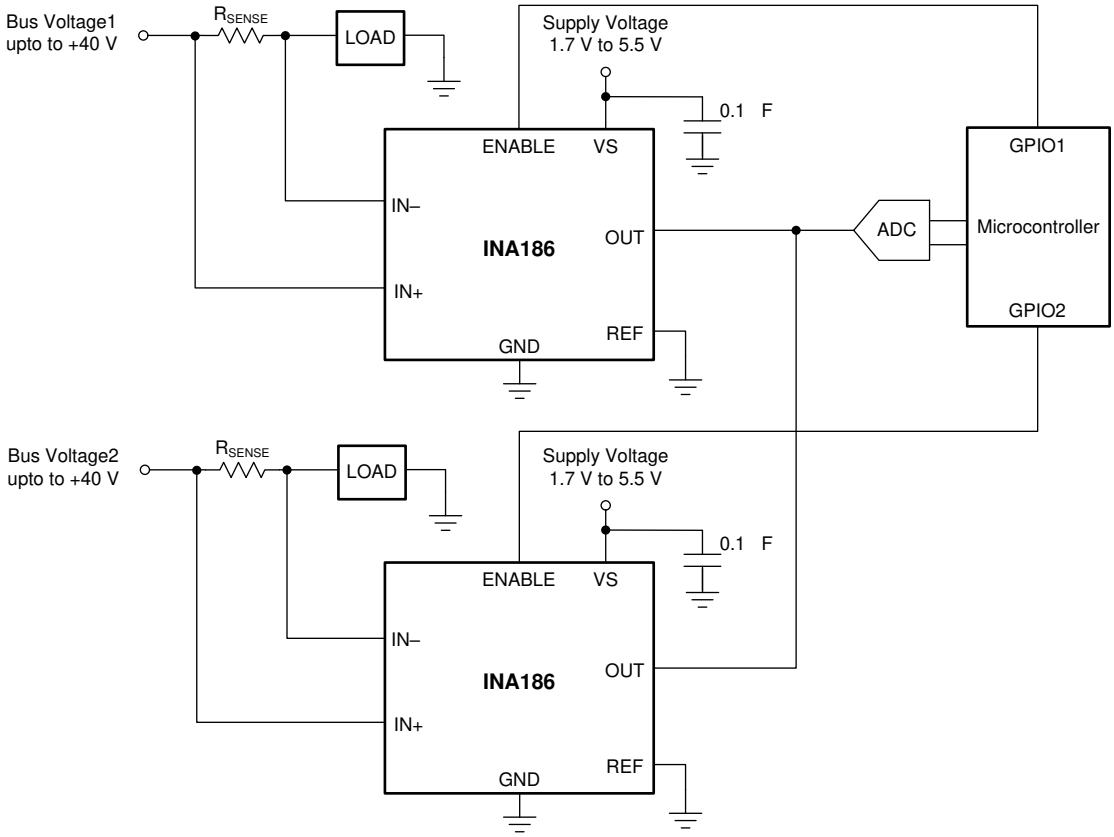


Figure 7-5. Multiplexing Multiple Devices With the ENABLE Pin

8 Application and Implementation

Note

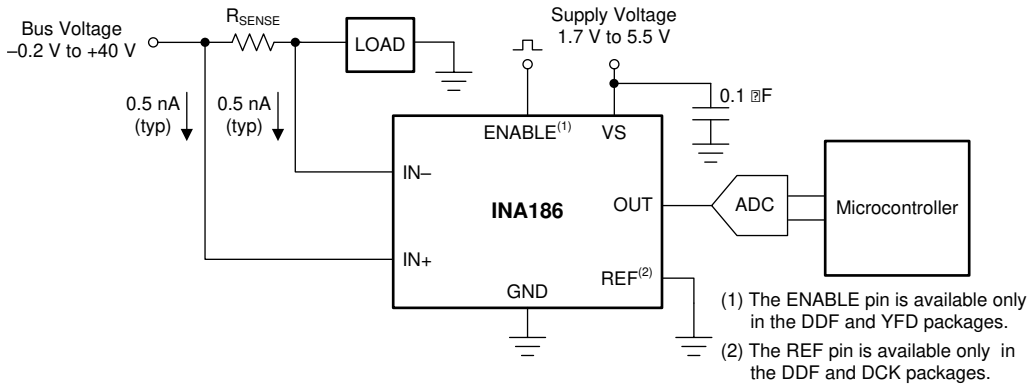
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA186 amplifies the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground. The high common-mode rejection of the INA186 makes it usable over a wide range of voltage rails while still maintaining an accurate current measurement.

8.1.1 Basic Connections

Figure 8-1 shows the basic connections of the INA186. Place the device as close as possible to the current sense resistor and connect the input pins (IN+ and IN–) to the current sense resistor through kelvin connections. If present, the ENABLE pin must be controlled externally or connected to VS if not used.



A. To help eliminate ground offset errors between the device and the analog-to-digital converter (ADC), connect the REF pin to the ADC reference input. When driving SAR ADCs, filter or buffer the output of the INA186 before connecting directly to the ADC.

Figure 8-1. Basic Connections

8.1.2 R_{SENSE} and Device Gain Selection

The accuracy of any current-sense amplifier is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. Equation 2 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (2)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that will flow through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing-to-rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 3 provides the maximum values of R_{SENSE} and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} - V_{REF} \quad (3)$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.
- V_{REF} is the externally applied voltage on the REF pin. This voltage is zero for devices without a REF pin.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small the sense resistor value can be for a given application. Equation 4 provides the limit on the minimum value of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} - V_{REF} \quad (4)$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SN} is the negative output swing of the device (see *Rail-to-Rail Output Swing*).
- V_{REF} is the externally applied voltage on the REF pin. This voltage is zero for devices without a REF pin.

In addition to adjusting R_{SENSE} and the device gain, the voltage applied to the REF pin can be slightly increased above GND to avoid negative swing limitations.

8.1.3 Signal Conditioning

When performing accurate current measurements in noisy environments, the current-sensing signal is often filtered. The INA186 features low input bias currents. Therefore, adding a differential mode filter to the input without sacrificing the current-sense accuracy is possible. Filtering at the input is advantageous because this action attenuates differential noise before the signal is amplified. Figure 8-2 provides an example of how to use a filter on the input pins of the device.

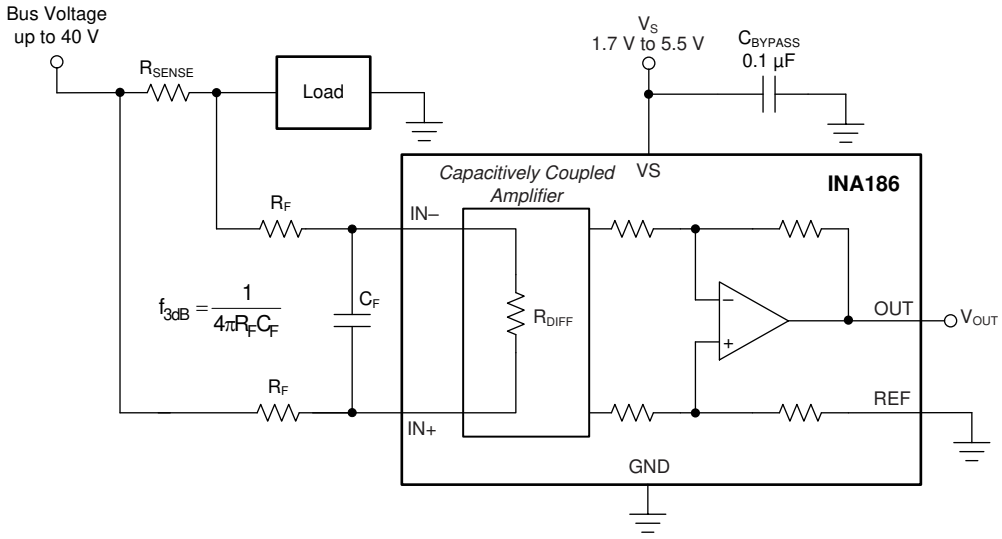


Figure 8-2. Filter at the Input Pins

Figure 8-2 shows the differential input impedance (R_{DIFF}) limits the maximum value for R_F. Figure 8-3 shows the value of R_{DIFF} is a function of the device temperature.

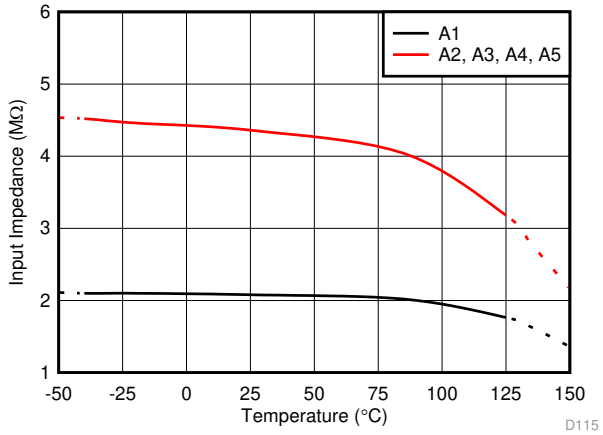


Figure 8-3. Differential Input Impedance vs. Temperature

As the voltage drop across the sense resistor (V_{SENSE}) increases, the amount of voltage dropped across the input filter resistors (R_F) also increases. The increased voltage drop results in additional gain error. The error caused by these resistors is calculated by the resistor divider equation shown in Equation 5.

$$\text{Error}(\%) = \left(1 - \frac{R_{DIFF}}{R_{SENSE} + R_{DIFF} + (2 \times R_F)}\right) \times 100 \tag{5}$$

where:

- R_{DIFF} is the differential input impedance.
- R_F is the added value of the series filter resistance.

The input stage of the INA186 uses a capacitive feedback amplifier topology in order to achieve high dc precision. As a result, periodic high-frequency shunt voltage (or current) transients of significant amplitude (10 mV or greater) and duration (hundreds of nanoseconds or greater) may be amplified by the INA186, even though the transients are greater than the device bandwidth. Use a differential input filter in these applications to minimize disturbances at the INA186 output.

The high input impedance and low bias current of the INA186 provide flexibility in the input filter design without impacting the accuracy of current measurement. For example, set R_F = 100 Ω and C_F = 22 nF to achieve a low-pass filter corner frequency of 36.2 kHz. These filter values significantly attenuate most unwanted high-frequency signals at the input without severely impacting the current sensing bandwidth or precision. If a lower corner frequency is desired, increase the value of C_F.

Filtering the input filters out differential noise across the sense resistor. If high-frequency, common-mode noise is a concern, add an RC filter from the OUT pin to ground. The RC filter helps filter out both differential and common mode noise, as well as internally generated noise from the device. The value for the resistance of the RC filter is limited by the impedance of the load. Any current drawn by the load manifests as an external voltage drop from the INA186 OUT pin to the load input. To select the optimal values for the output filter, use Output Impedance vs. Frequency and see the *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* application report

8.1.4 Common-Mode Voltage Transients

With a small amount of additional circuitry, the INA186 can be used in circuits subject to transients that exceed the absolute maximum voltage ratings. The most simple way to protect the inputs from negative transients is to add resistors in series with the IN– and IN+ pins. Use resistors that are 1 kΩ or less, and limit the current in the ESD structures to less than 5 mA. For example, using 1-kΩ resistors in series with the INA186 allows voltages as low as –5 V, while limiting the ESD current to less than 5 mA. Use the circuits shown in Figure 8-4 and Figure 8-5 if protection from high-voltage or more-negative, common-voltage transients is needed. When implementing these circuits, use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode (see Figure 8-4). Keep these resistors as small as possible; most often, use around 100 Ω. See *Signal Conditioning* for information on how larger values can be used with an effect on gain. This circuit limits only short-term transients; therefore, many applications are satisfied with a 100-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

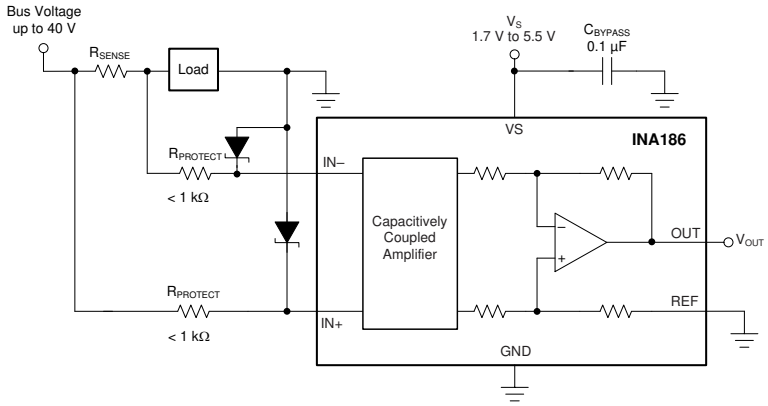


Figure 8-4. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in Figure 8-5. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in Figure 8-4 and Figure 8-5, the total board area required by the INA186 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an VSSOP-8 package.

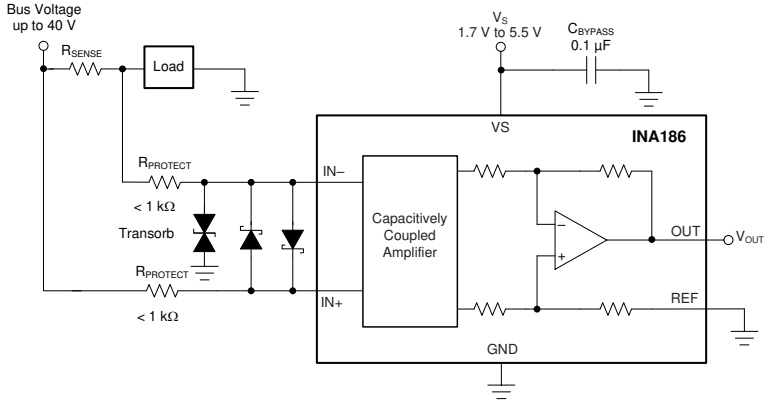


Figure 8-5. Transient Protection Using a Single Transzorb and Input Clamps

For more information, see the *Current Shunt Monitor With Transient Robustness* reference design.

8.2 Typical Applications

The low input bias current of the INA186 allows accurate monitoring of small-value currents. To accurately monitor currents in the microamp range, increase the value of the sense resistor to increase the sense voltage so that the error introduced by the offset voltage is small. Figure 8-6 shows the circuit configuration for monitoring low-value currents. As a result of the differential input impedance of the INA186, limit the value of R_{SENSE} to 1 kΩ or less for best accuracy.

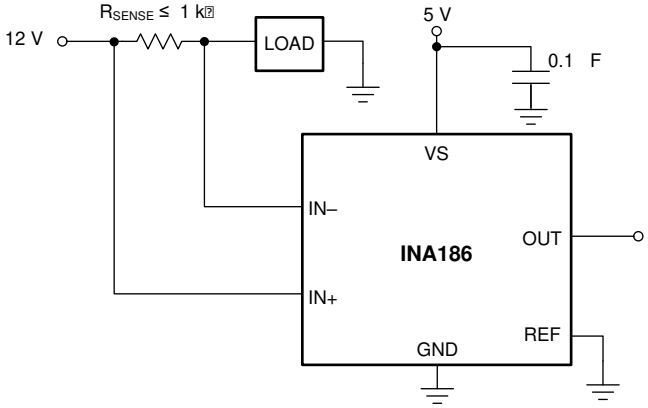


Figure 8-6. Microamp Current Measurement

8.2.1 Design Requirements

Table 8-1 lists the design requirements for the circuit shown in Figure 8-6.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	12 V
Minimum sense current (I_{MIN})	1 µA
Maximum sense current (I_{MAX})	150 µA
Device gain (GAIN)	25 V/V
Reference voltage (V_{REF})	0 V

8.2.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based on choice of gain, value of the maximum current the be sensed (I_{MAX}), and the power-supply voltage (V_S). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP}. Using Equation 6, for the given design parameters the maximum value for R_{SENSE} is calculated to be 1.321 kΩ.

$$R_{SENSE} < \frac{V_{SP}}{I_{MAX} \times GAIN} \tag{6}$$

However, because this value exceeds the maximum recommended value for R_{SENSE}, a resistance value of 1 kΩ must be used. When operating at the minimum current value, I_{MIN} the output voltage must be greater than the swing to GND (V_{SN}), specification. For this example, the output voltage at the minimum current is calculated using Equation 7 to be 25 mV, which is greater than the value for V_{SN}.

$$V_{OUTMIN} = I_{MIN} \times R_{SENSE} \times GAIN \tag{7}$$

8.2.3 Application Curve

Figure 8-7 shows the output of the device under the conditions given in Table 8-1 and with R_{SENSE} = 1 kΩ.

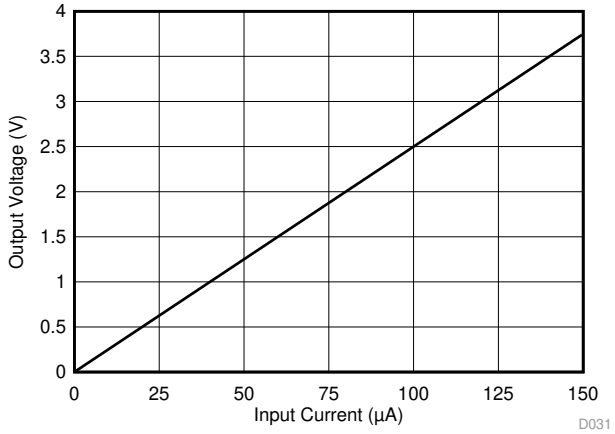


Figure 8-7. Typical Application DC Transfer Function

9 Power Supply Recommendations

The input circuitry of the INA186 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 40 V. However, the output voltage range of the OUT pin is limited by the voltage on the VS pin. The INA186 also withstands the full differential input signal range up to 40 V at the IN+ and IN– input pins, regardless of whether the device has power applied at the VS pin. There is no sequencing requirement for V_S and V_{IN+} or $V_{IN–}$.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current-sense resistor to the device, keep the trace lengths as short as possible. The input filter capacitor C_F should be placed as close as possible to the input pins of the device.

10.2 Layout Examples

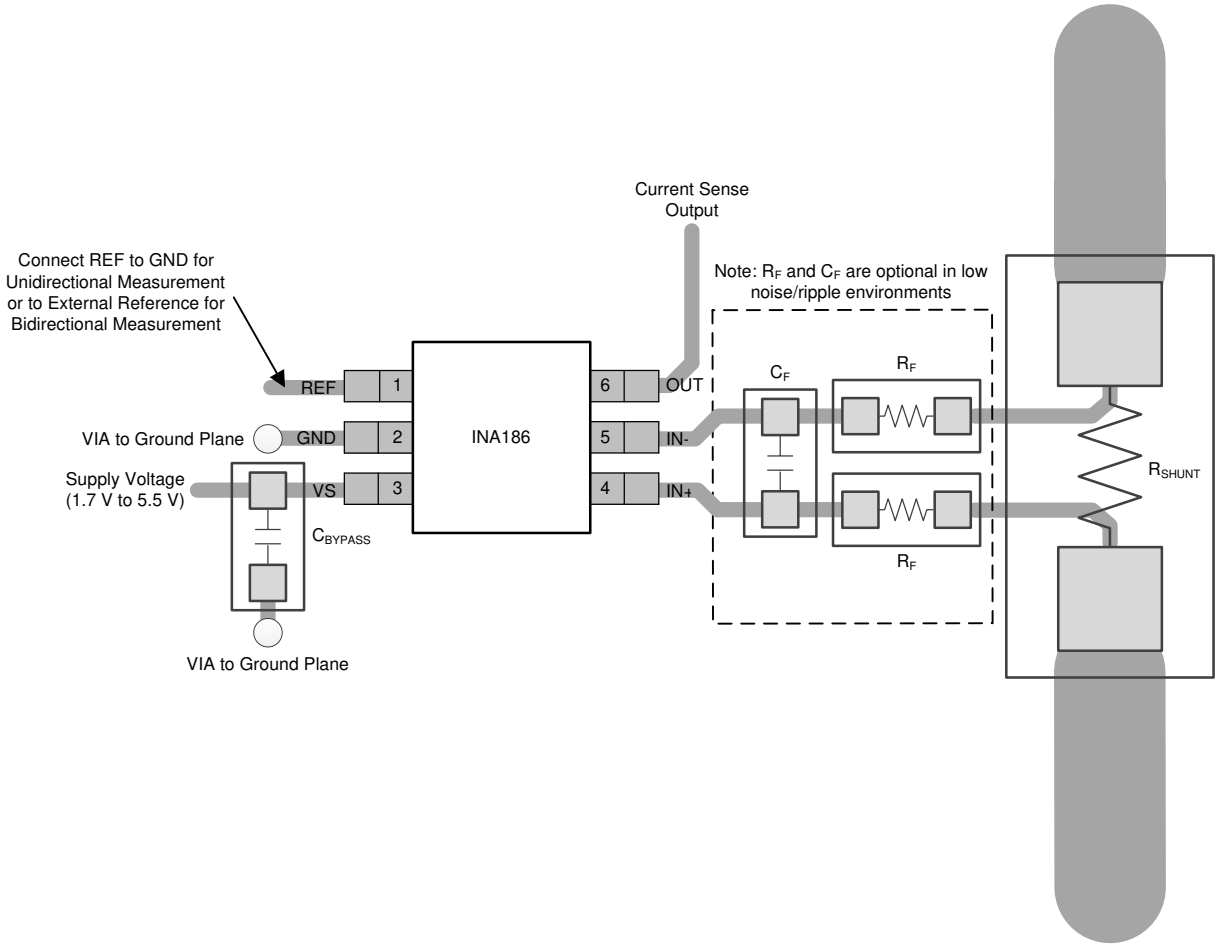


Figure 10-1. Recommended Layout for SC70 (DCK) Package

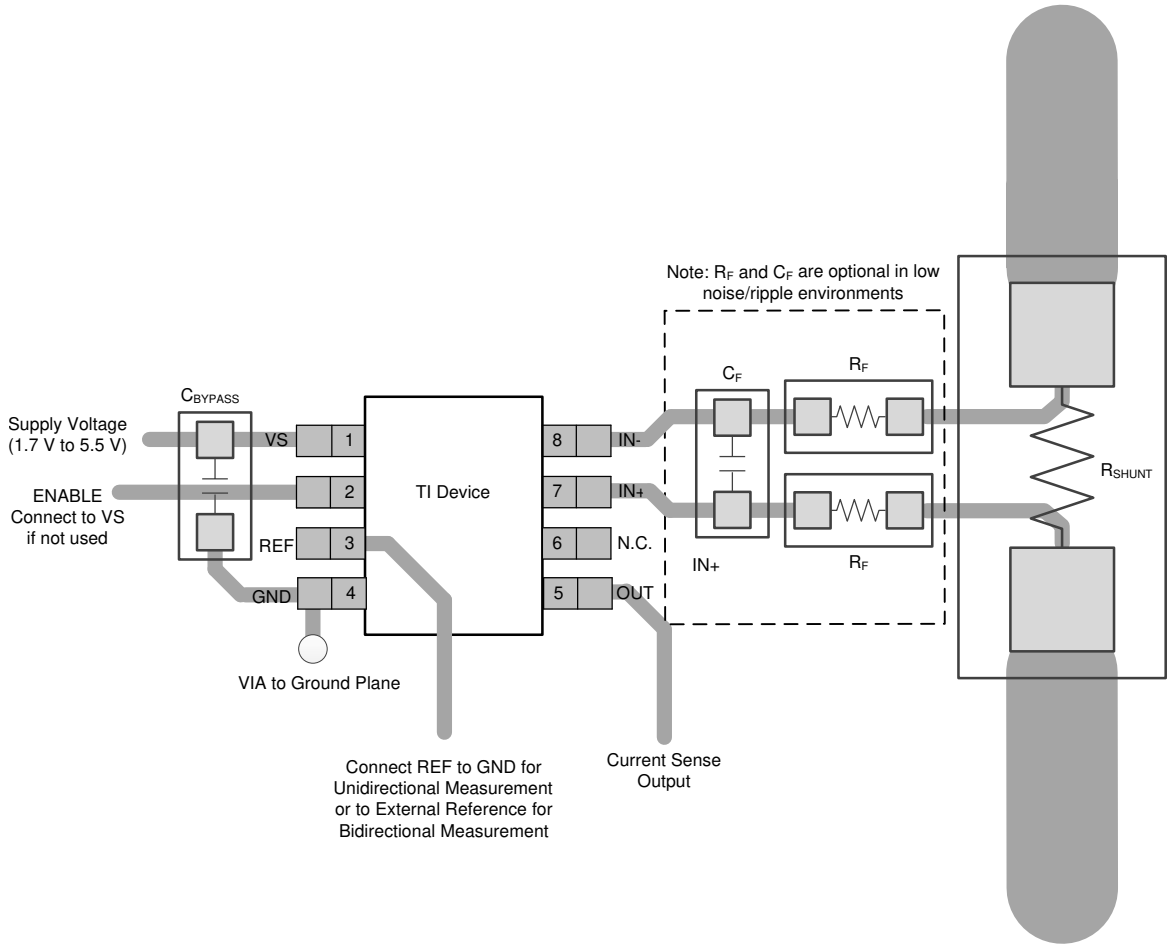


Figure 10-2. Recommended Layout for SOT-23 (DDF) Package

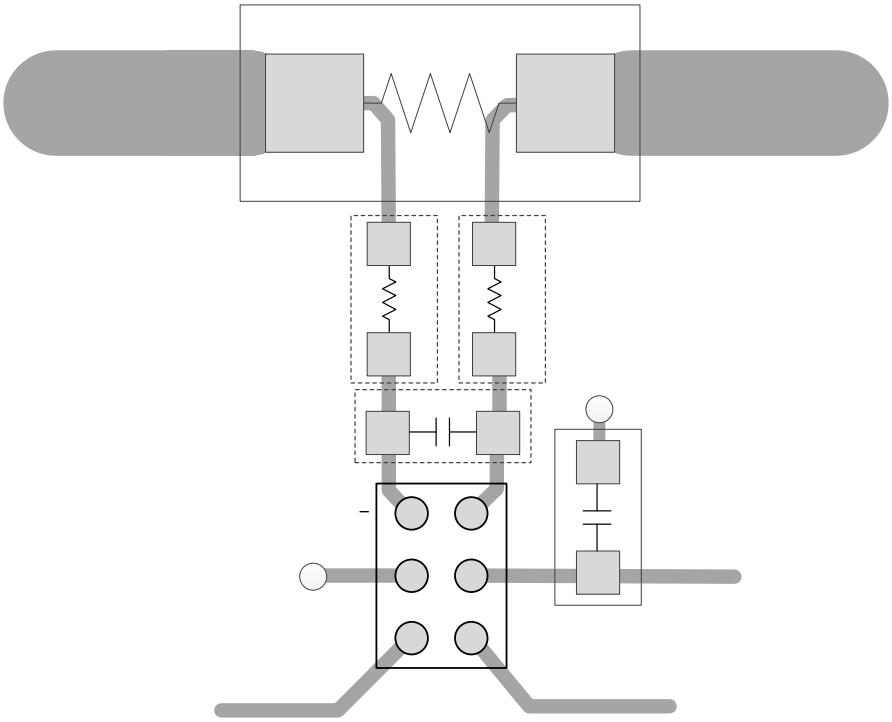


Figure 10-3. Recommended Layout DSBGA (YFD) Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *INA186EVM* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

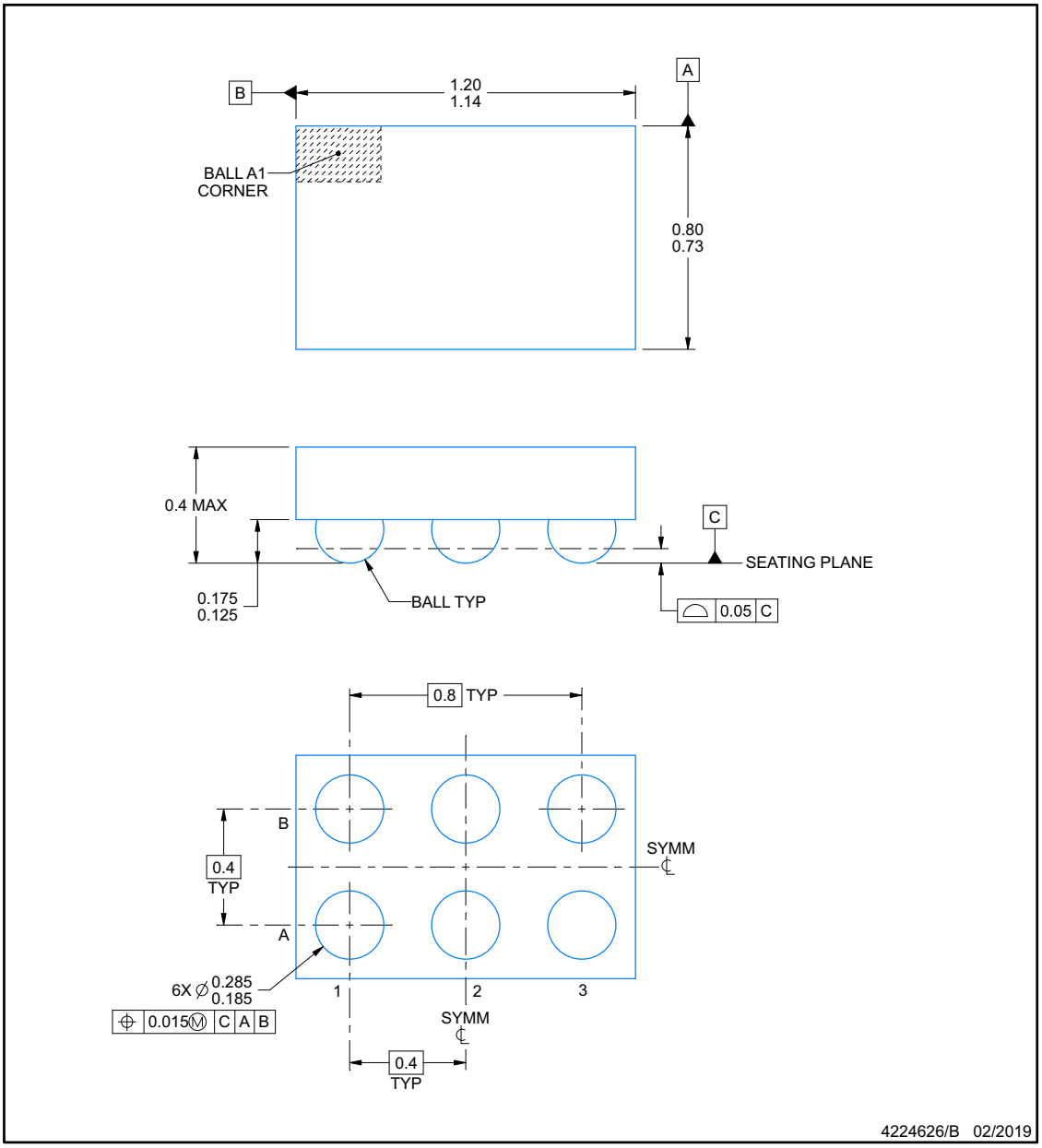
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YFD0006-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



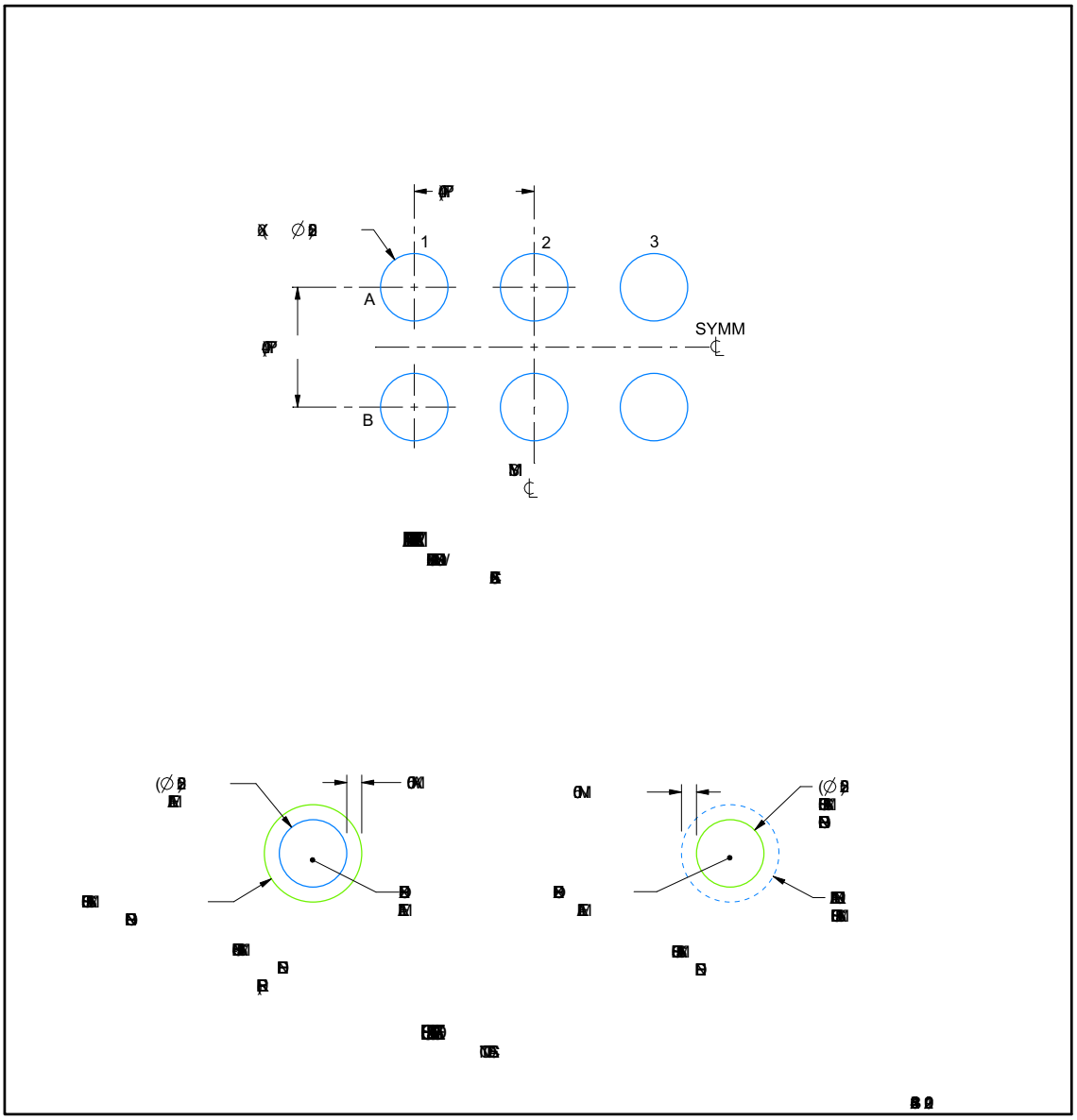
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YFD0006-C02

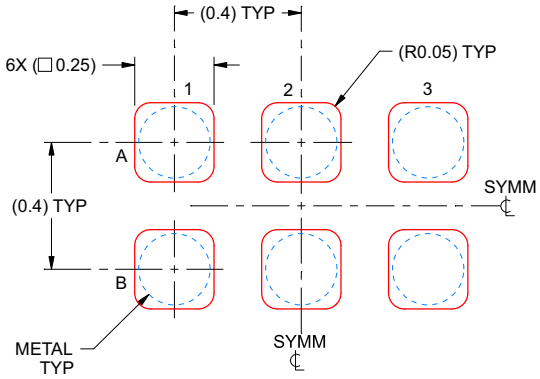
DSBGA - 0.4 mm max height



EXAMPLE STENCIL DESIGN

YFD0006-C02 — **DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4224626/B 02/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA186A1IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E7	Samples
INA186A1IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E7	Samples
INA186A1IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZLW	Samples
INA186A1IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZLW	Samples
INA186A1IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IJ	Samples
INA186A2IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E8	Samples
INA186A2IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E8	Samples
INA186A2IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZMW	Samples
INA186A2IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZMW	Samples
INA186A2IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IK	Samples
INA186A3IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E9	Samples
INA186A3IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1E9	Samples
INA186A3IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZNW	Samples
INA186A3IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZNW	Samples
INA186A3IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IL	Samples
INA186A4IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EA	Samples
INA186A4IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EA	Samples
INA186A4IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZOW	Samples
INA186A4IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZOW	Samples
INA186A4IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA186A5IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EB	Samples
INA186A5IDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1EB	Samples
INA186A5IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZPW	Samples
INA186A5IDDFT	ACTIVE	SOT-23-THIN	DDF	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZPW	Samples
INA186A5IYFDR	ACTIVE	DSBGA	YFD	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA186 :

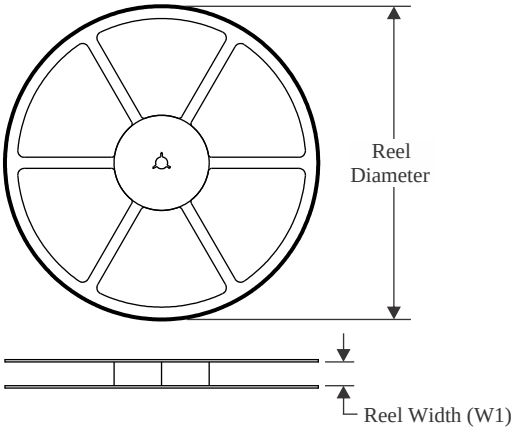
- Automotive : INA186-Q1

NOTE: Qualified Version Definitions:

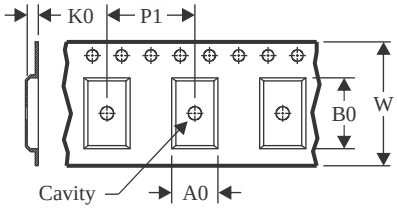
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

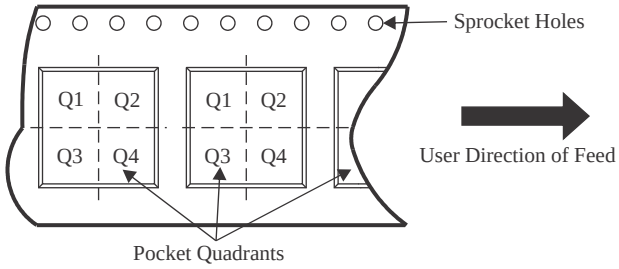


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

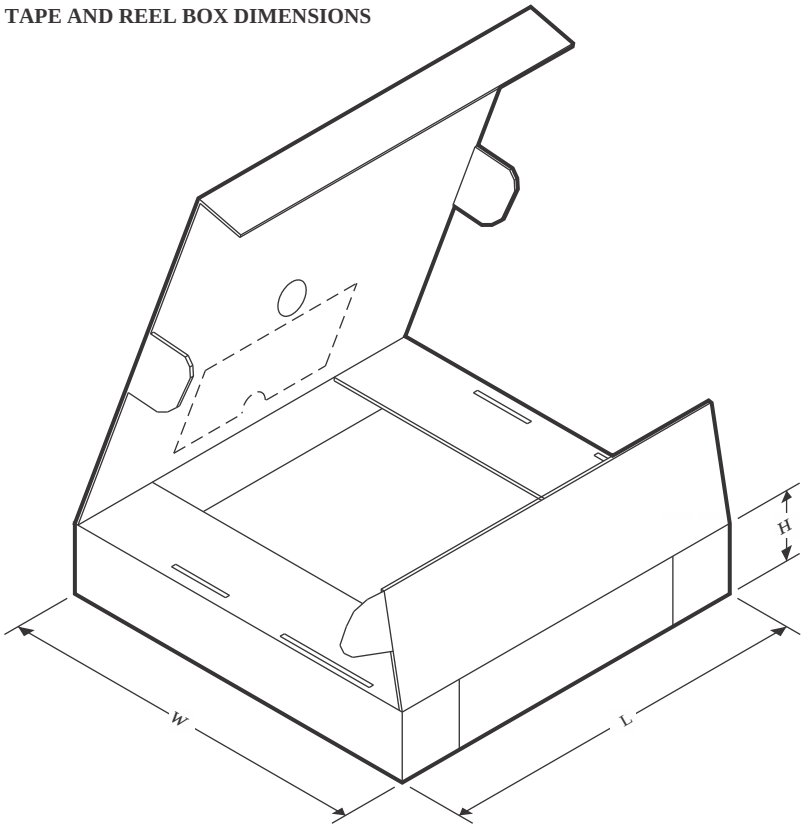


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA186A1IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A1IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A1IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A1IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A2IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A2IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A2IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A2IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A3IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A3IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A3IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A3IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A3IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA186A4IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A4IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A4IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A4IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A4IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2
INA186A5IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A5IDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA186A5IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A5IDDFT	SOT-23-THIN	DDF	8	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA186A5IYFDR	DSBGA	YFD	6	3000	178.0	8.4	0.84	1.27	0.46	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA186A1IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A1IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A1IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A1IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A2IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A2IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A2IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A2IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A3IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A3IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A3IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A3IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A3IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0
INA186A4IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A4IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A4IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A4IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A4IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0

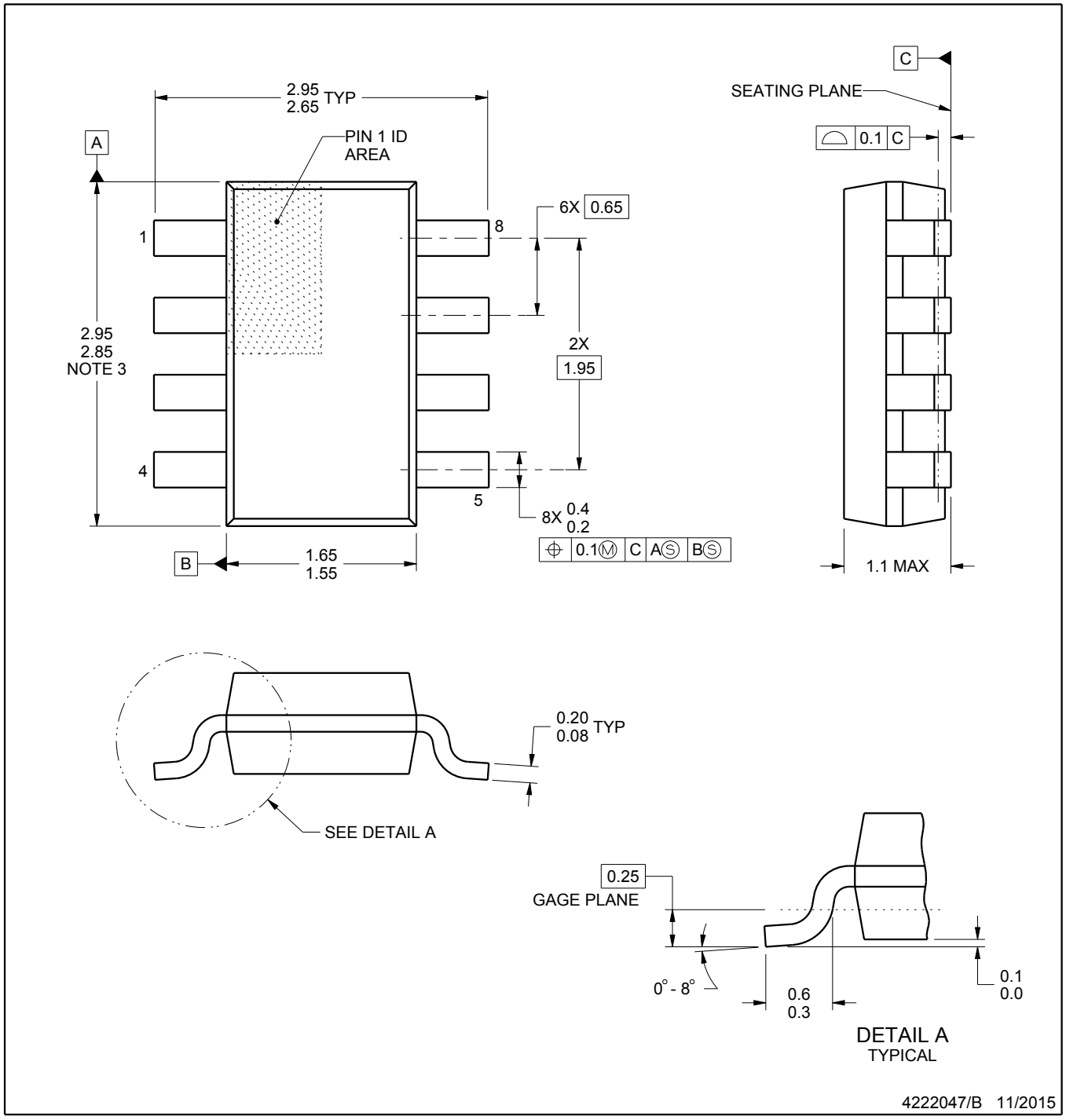
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA186A5IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA186A5IDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA186A5IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA186A5IDDFT	SOT-23-THIN	DDF	8	250	210.0	185.0	35.0
INA186A5IYFDR	DSBGA	YFD	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DDF0008A

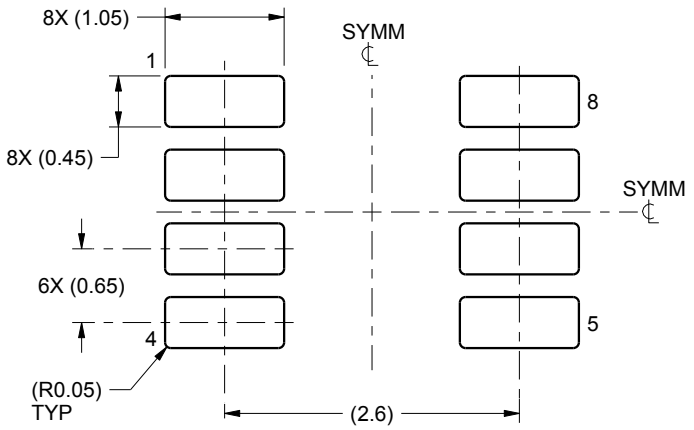
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

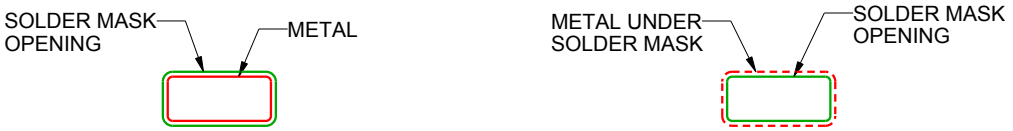


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

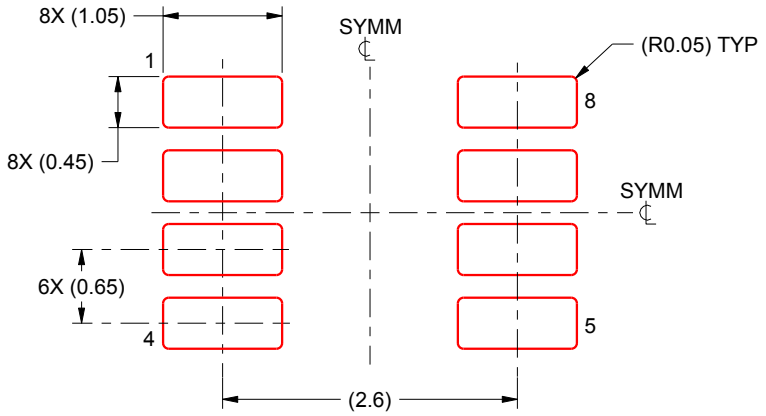
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

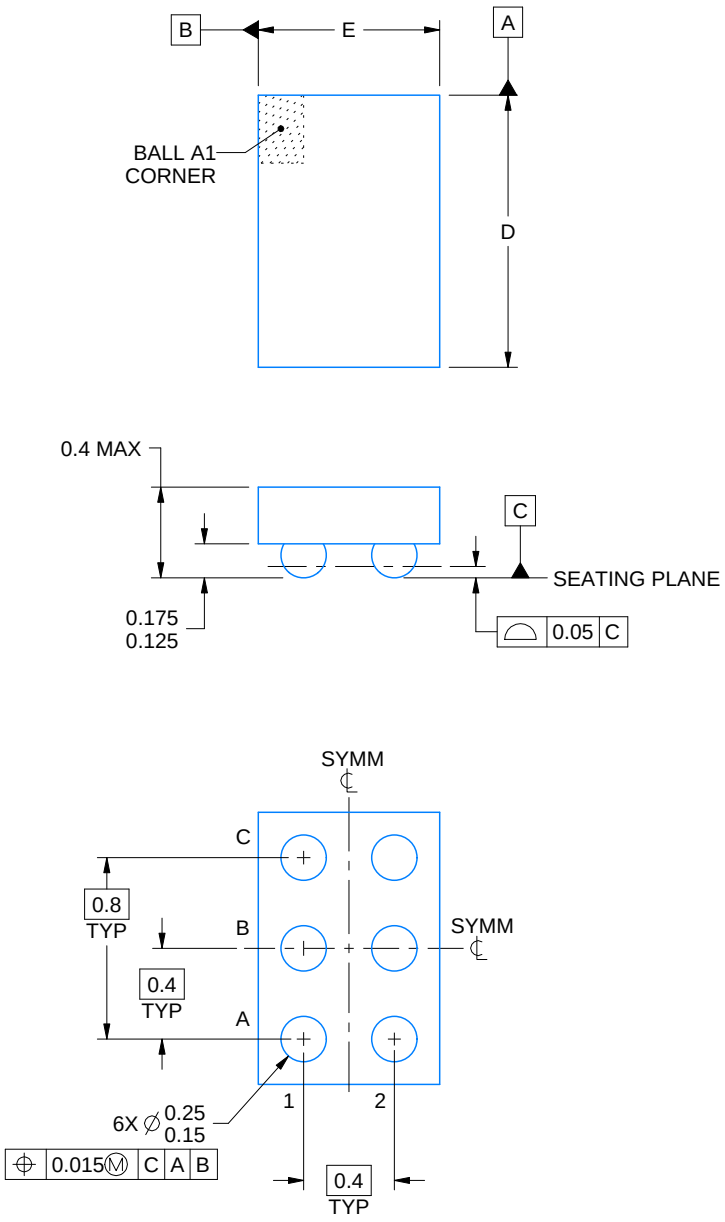


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



4219510/A 11/2019

NOTES:

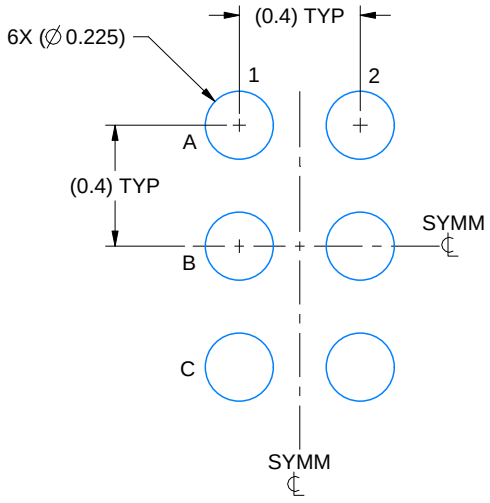
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

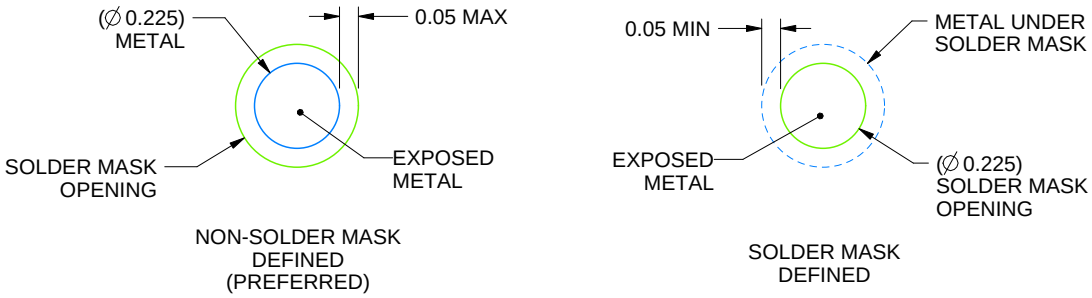
YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219510/A 11/2019

NOTES: (continued)

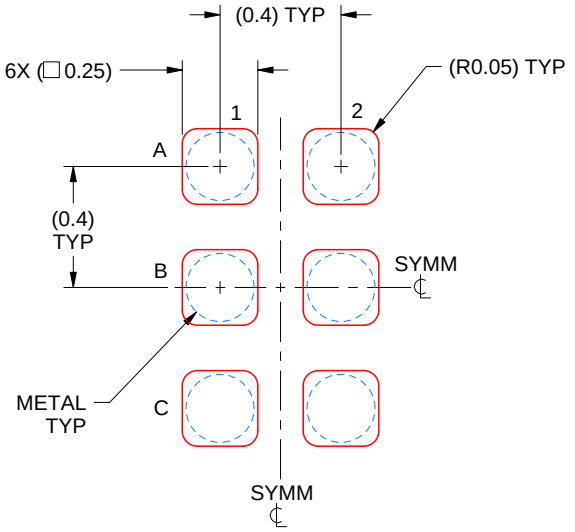
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFD0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



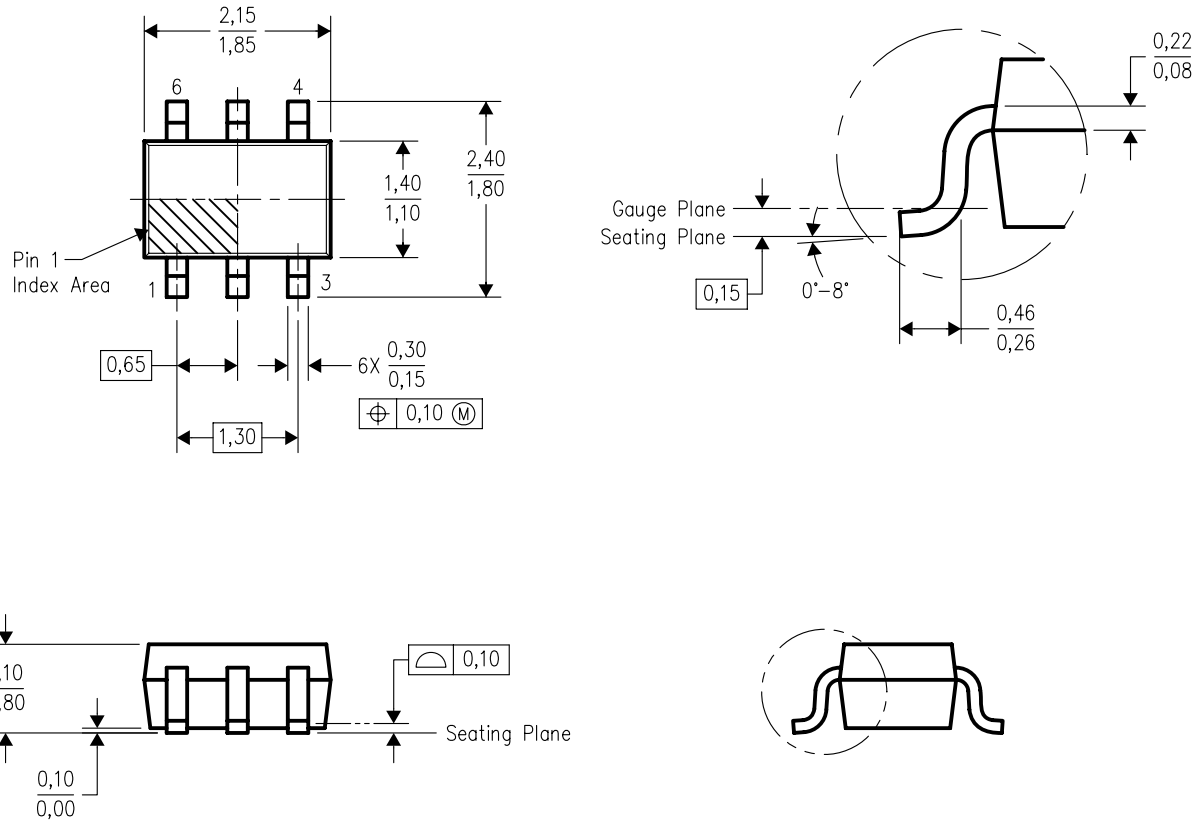
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219510/A 11/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

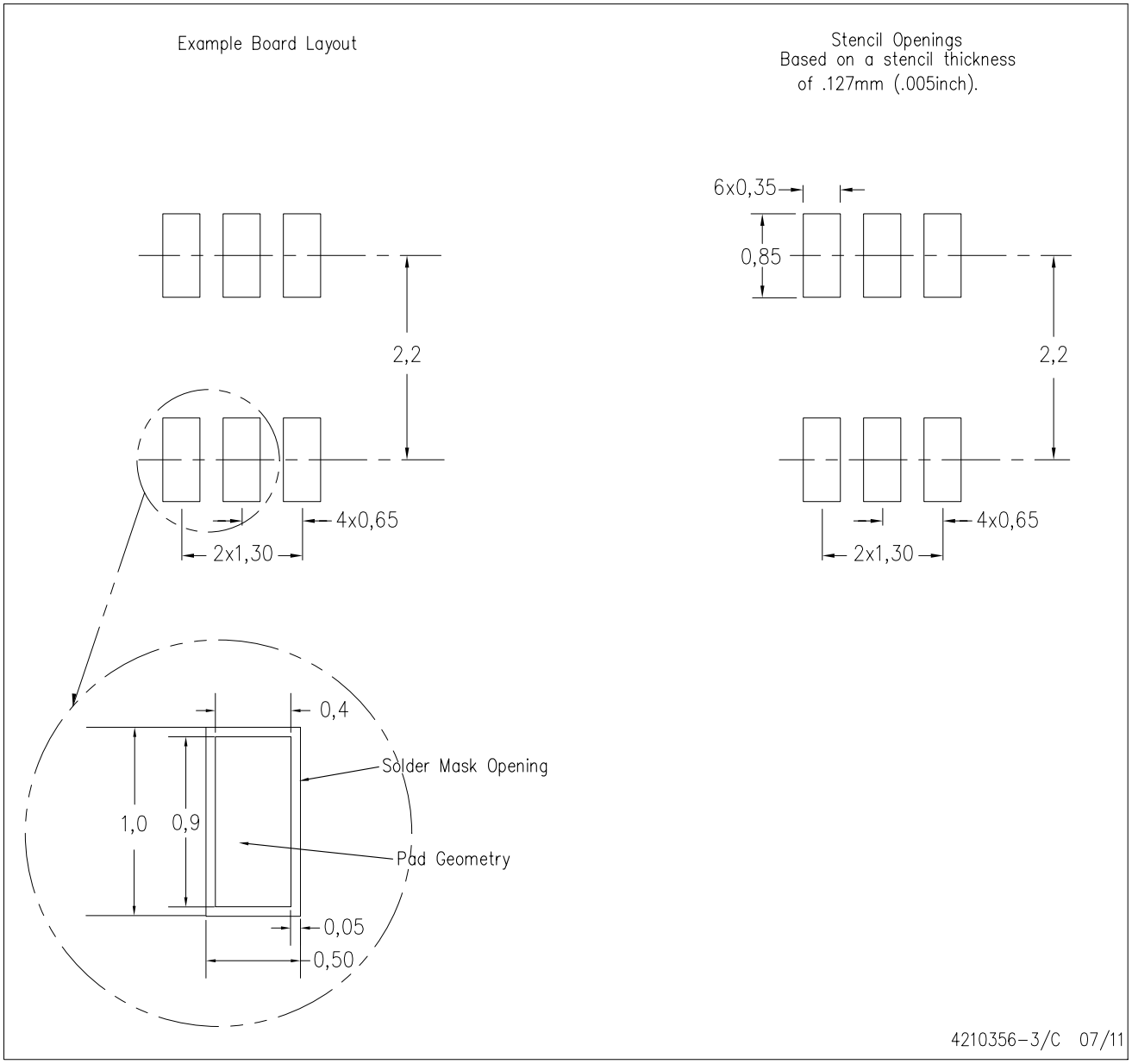
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS

INA210, INA211, INA212, INA213, INA214, INA215

SBOS437J – MAY 2008 – REVISED FEBRUARY 2017

INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors

1 Features

- Wide Common-Mode Range: –0.3 V to 26 V
- Offset Voltage: ±35 μV (Maximum, INA210) (Enables Shunt Drops of 10-mV Full-Scale)
- Accuracy:
  - Gain Error (Maximum Over Temperature):
    - ±0.5% (Version C)
    - ±1% (Versions A and B)
  - 0.5-μV/°C Offset Drift (Maximum)
  - 10-ppm/°C Gain Drift (Maximum)
- Choice of Gains:
  - INA210: 200 V/V
  - INA211: 500 V/V
  - INA212: 1000 V/V
  - INA213: 50 V/V
  - INA214: 100 V/V
  - INA215: 75 V/V
- Quiescent Current: 100 μA (Maximum)
- SC70 and Thin UQFN Packages: All Models

2 Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Power Management
- Battery Chargers

3 Description

The INA21x are voltage-output, current-shunt monitors (also called current-sense amplifiers) that are commonly used for overcurrent protection, precision-current measurement for system optimization, or in closed-loop feedback circuits. This series of devices can sense drops across shunts at common-mode voltages from –0.3 V to 26 V, independent of the supply voltage. Six fixed gains are available: 50 V/V, 75 V/V, 100 V/V, 200 V/V, 500 V/V, or 1000 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

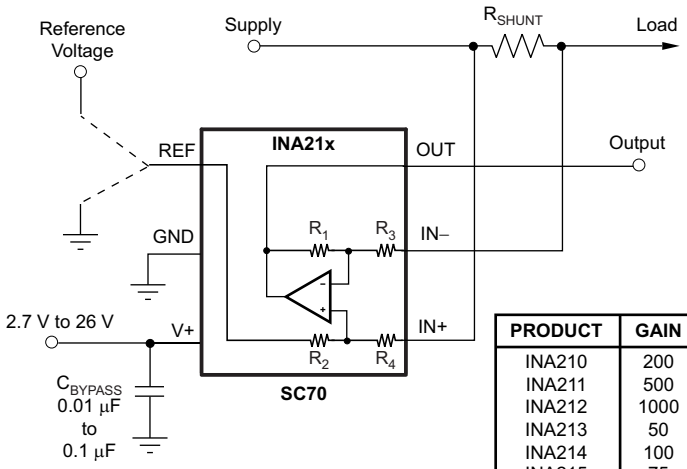
These devices operate from a single 2.7-V to 26-V power supply, drawing a maximum of 100 μA of supply current. All versions are specified over the extended operating temperature range (–40°C to +125°C), and offered in SC70 and UQFN packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA21x	SC70 (6)	2.00 mm × 1.25 mm
	UQFN (10)	1.80 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



PRODUCT	GAIN	R_3 and R_4	R_1 and R_2
INA210	200	5 kΩ	1 MΩ
INA211	500	2 kΩ	1 MΩ
INA212	1000	1 kΩ	1 MΩ
INA213	50	20 kΩ	1 MΩ
INA214	100	10 kΩ	1 MΩ
INA215	75	13.3 kΩ	1 MΩ

$V_{OUT} = (I_{LOAD} \times R_{SHUNT})$ Gain + V_{REF}

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (September 2016) to Revision J — **Page**

- Added 2017 copyright to front page graphic ... 1
- Deleted *Device Options* table ... 5
- Added Common-mode analog inputs (Versions B and C) to *Absolute Maximum Ratings* table ... 6
- Changed HBM ESD value (Version A) from 4000 to 2000 V in *ESD Ratings* table ... 6
- Changed formatting of *Thermal Information* table note ... 7
- Deleted static literature number from document reference in *Related Documentation* section ... 27

Changes from Revision H (June 2016) to Revision I — **Page**

- Deleted all notes regarding preview devices throughout data sheet; all devices now active ... 1

Changes from Revision G (July 2014) to Revision H — **Page**

- Changed Features section: deleted last bullet, changed packages bullet ... 1
- Deleted last *Applications* bullet ... 1
- Changed *Description* section ... 1
- Changed *Device Information* table ... 1
- Moved storage temperature to *Absolute Maximum Ratings* table ... 6
- Changed *ESD Ratings* table: changed title, changed format to current standards ... 6
- Deleted both *Machine Model* rows from *ESD Ratings* table ... 6
- Changed first sentence referencing Equation 1 in *Input Filtering* section: replaced *seen* with *measured* ... 16
- Changed second sentence referencing Equation 1 in *Input Filtering* section ... 17
- Corrected punctuation and added clarity to first and second paragraphs in *Shutting Down the INA21x Series* section ... 18
- Changed *impressed* to *present* in fourth paragraph of *Shutting Down the INA21x Series* section ... 18

Changes from Revision F (June 2014) to Revision G **Page**

- Changed Simplified Schematic: added equation below gain table ... 1
- Changed $V_{(ESD)}$ *HBM* specifications for version A in Handling Ratings table ... 6

Changes from Revision E (June 2013) to Revision F **Page**

- Changed format to meet latest data sheet standards; added Pin Functions, Recommended Operating Conditions, and Thermal Information tables, *Overview*, *Functional Block Diagram*, *Application Information*, *Power Supply Recommendations*, and *Layout* sections, and moved existing sections ... 1
- Added INA215 to document ... 1
- Added INA215 sub-bullet to fourth Features bullet ... 1
- Added INA215 to simplified schematic table ... 1
- Added Thermal Information table ... 6
- Added INA215 to Figure 7 ... 10
- Added INA215 to Figure 15 ... 11
- Added INA215 to Figure 25 ... 18

Changes from Revision D (November 2012) to Revision E **Page**

Changes from Revision C (August 2012) to Revision D **Page**

- Changed Frequency Response, *Bandwidth* parameter in Electrical Characteristics table ... 6

Changes from Revision B (June 2009) to Revision C **Page**

- Added silicon version B row to Input, *Common-Mode Input Range* parameter in Electrical Characteristics table ... 6
- Added silicon version B ESD ratings to Abs Max table ... 6
- Corrected typo in Figure 9 ... 10
- Updated Figure 12 ... 10
- Changed *Input Filtering* section ... 16
- Added *Improving Transient Robustness* section ... 21

Changes from Revision A (June 2008) to Revision B **Page**

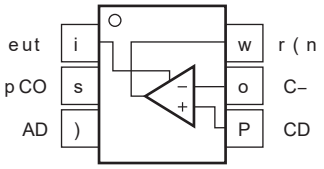
- Added RSW package to device photo ... 1
- Added UQFN package to *Features* list ... 1
- Updated front page graphic ... 1
- Added RSW package pin out drawing ... 5
- Added footnote 3 to *Electrical Characteristics* table ... 6
- Added UQFN package information to *Temperature Range* section of *Electrical Characteristics* table ... 6
- Changed Figure 2 to reflect operating temperature range ... 10
- Changed Figure 4 to reflect operating temperature range ... 10
- Changed Figure 6 to reflect operating temperature range ... 10
- Changed Figure 13 to reflect operating temperature range ... 11
- Changed Figure 14 to reflect operating temperature range ... 11
- Added RSW description to the *Basic Connections* section ... 15
- Changed 60 μV to 100 μV in last sentence of the *Selecting RS* section ... 15

Changes from Original (May 2008) to Revision A **Page**

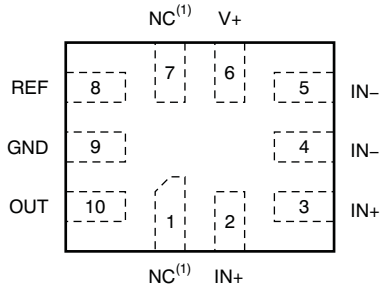
- Deleted first footnote of *Electrical Characteristics* table 6
- Changed Figure 7 10
- Changed Figure 15 11

5 Pin Configurations and Functions

DCK Package
6-Pin SC70
Top View



RSW Package
10-Pin Thin UQFN
Top View



(1) NC denotes no internal connection. These pins can be left floating or connected to any voltage between V– and V+.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCK	RSW		
GND	2	9	Analog	Ground
IN–	5	4, 5	Analog input	Connect to load side of shunt resistor
IN+	4	2, 3	Analog input	Connect to supply side of shunt resistor
NC	—	1, 7	—	Not internally connected. Leave floating or connect to ground.
OUT	6	10	Analog output	Output voltage
REF	1	8	Analog input	Reference voltage, 0 V to V+
V+	3	6	Analog	Power supply, 2.7 V to 26 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			26	V
Analog inputs, V_{IN+}, V_{IN-}(2)	Differential (V_{IN+}) – (V_{IN-})	–26	26	V
	Common-mode (Version A)(3)	GND – 0.3	26	V
	Common-mode (Version B)(3)	GND – 0.1	26	V
	Common-mode (Version C)(3)	GND – 0.1	26	V
REF input		GND – 0.3	(V_S) + 0.3	V
Output(3)		GND – 0.3	(V_S) + 0.3	V
Input current into any terminal(3)			5	mA
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any terminal may exceed the voltage shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
INA21x, (VERSION A)				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
INA21x, (VERSIONS B AND C)				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA21x		UNIT
		DCK (SC70)	RSW (UQFN)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	107.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	18.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.4	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, $V_{SENSE} = V_{IN+} - V_{IN-}$
INA210, INA213, INA214, and INA215: V_S = 5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted
INA211 and INA212: V_S = 12 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input range		Version A T_A = –40°C to +125°C	–0.3		26	V
			Versions B and C T_A = –40°C to +125°C	–0.1		26	
CMRR	Common-mode rejection ratio	INA210, INA211, INA212, INA214, INA215	V_{IN+} = 0 V to 26 V V_{SENSE} = 0 mV T_A = –40°C to +125°C	105	140		dB
		INA213	V_{IN+} = 0 V to 26 V V_{SENSE} = 0 mV T_A = –40°C to +125°C	100	120		
V_O	Offset voltage, RTI[1]	INA210, INA211, INA212	V_{SENSE} = 0 mV		±0.55	±35	µV
		INA213	V_{SENSE} = 0 mV		±5	±100	
		INA214, INA215	V_{SENSE} = 0 mV		±1	±60	
dV_{OS}/dT	RTI vs temperature		V_{SENSE} = 0 mV T_A = –40°C to +125°C		0.1	0.5	µV/°C
PSRR	RTI vs power supply ratio		V_S = 2.7 V to 18 V V_{IN+} = 18 V V_{SENSE} = 0 mV		±0.1	±10	µV/V
I_{IB}	Input bias current		V_{SENSE} = 0 mV	15	28	35	µA
I_{IO}	Input offset current		V_{SENSE} = 0 mV		±0.02		µA
OUTPUT							
G	Gain	INA210			200		V/V
		INA211			500		
		INA212			1000		
		INA213			50		
		INA214			100		
		INA215			75		
E_G	Gain error		V_{SENSE} = –5 mV to 5 mV T_A = –40°C to +125°C (Versions A and B)		±0.02%	±1%	
			V_{SENSE} = –5 mV to 5 mV T_A = –40°C to +125°C (Version C)		±0.02%	±0.5%	
	Gain error vs temperature		T_A = –40°C to +125°C		3	10	ppm/°C
	Nonlinearity error		V_{SENSE} = –5 mV to 5 mV		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF
VOLTAGE OUTPUT[2]							
	Swing to V+ power-supply rail		R_L = 10 kΩ to GND T_A = –40°C to +125°C		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND		R_L = 10 kΩ to GND T_A = –40°C to +125°C		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth		C_{LOAD} = 10 pF, INA210		14		kHz
			C_{LOAD} = 10 pF, INA211		7		
			C_{LOAD} = 10 pF, INA212		4		
			C_{LOAD} = 10 pF, INA213		80		
			C_{LOAD} = 10 pF, INA214		30		
			C_{LOAD} = 10 pF, INA215		40		
SR	Slew rate				0.4		V/µs
NOISE, RTI[1]							
	Voltage noise density				25		nV/√Hz

(1) RTI = referred-to-input.
(2) See Typical Characteristic curve, *Output Voltage Swing vs Output Current* (Figure 10).

Electrical Characteristics (continued)

at T_A = 25°C, $V_{SENSE} = V_{IN+} - V_{IN-}$
INA210, INA213, INA214, and INA215: V_S = 5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted
INA211 and INA212: V_S = 12 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Operating voltage range		T_A = –40°C to +125°C	2.7		26	V
I_Q	Quiescent current		V_{SENSE} = 0 mV		65	100	µA
	I_Q over temperature		T_A = –40°C to +125°C			115	µA
TEMPERATURE RANGE							
	Specified range			–40		125	°C
	Operating range			–55		150	°C
θ_{JA}	Thermal resistance	SC70			250		°C/W
		Thin UQFN			80		°C/W

6.6 Typical Characteristics

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

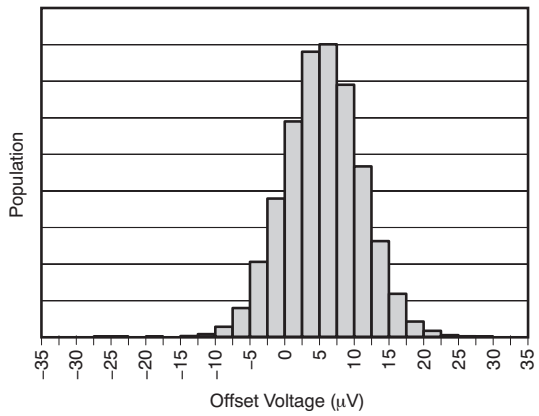


Figure 1. Input Offset Voltage Production Distribution

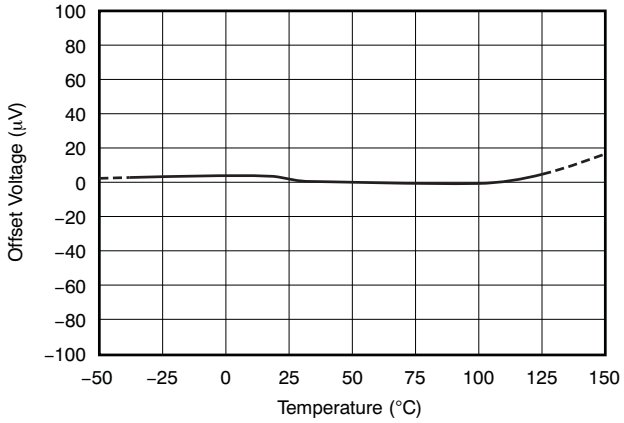


Figure 2. Offset Voltage vs Temperature

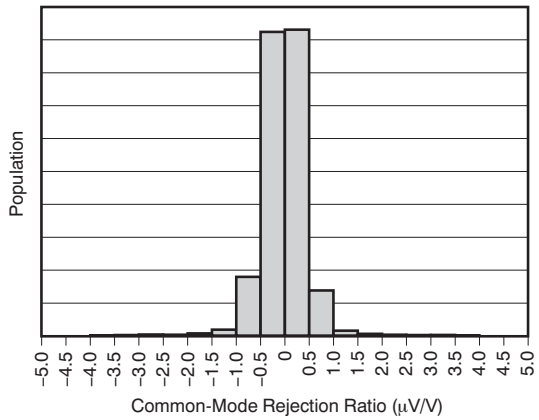


Figure 3. Common-Mode Rejection Production Distribution

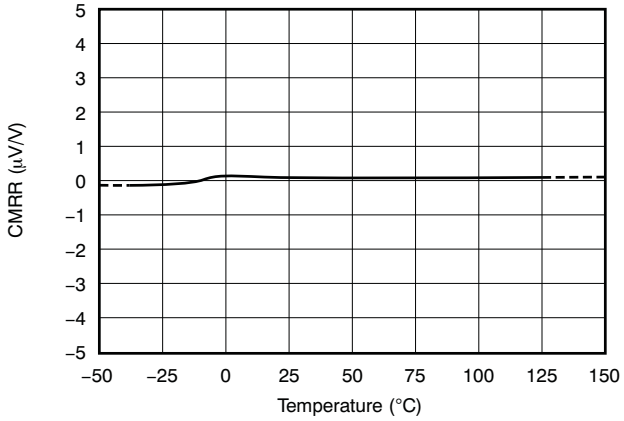


Figure 4. Common-Mode Rejection Ratio vs Temperature

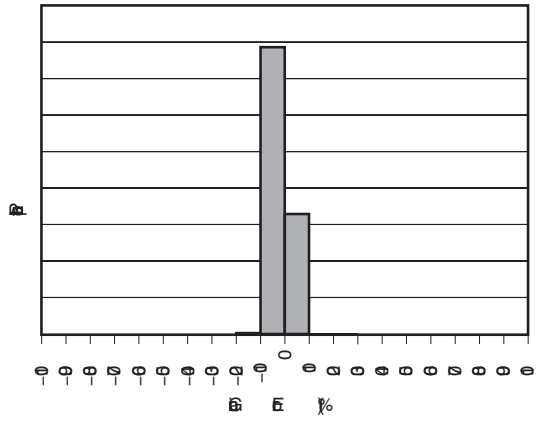


Figure 5. Gain Error Production Distribution

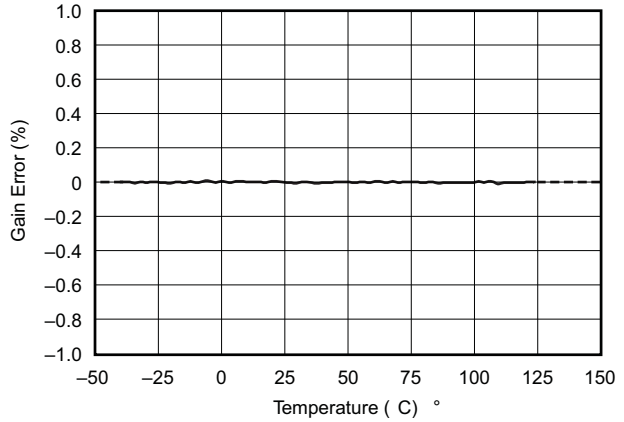


Figure 6. Gain Error vs Temperature

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

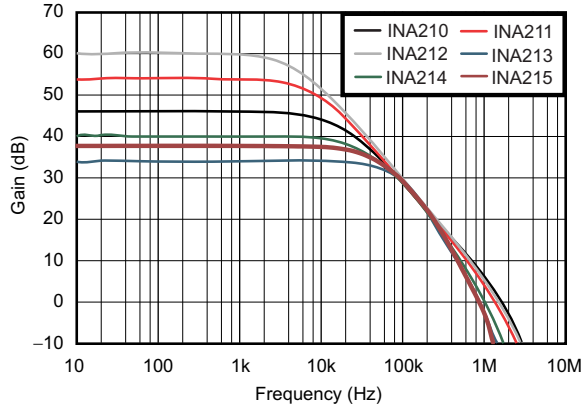
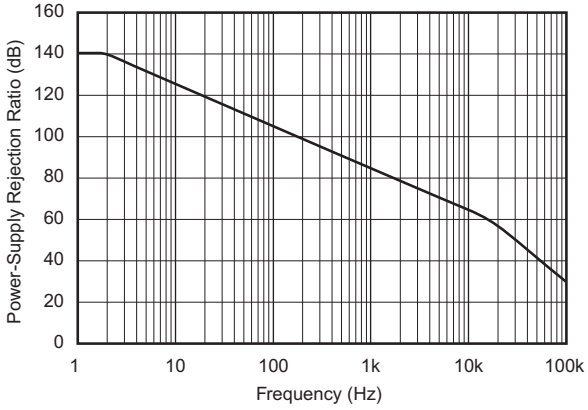
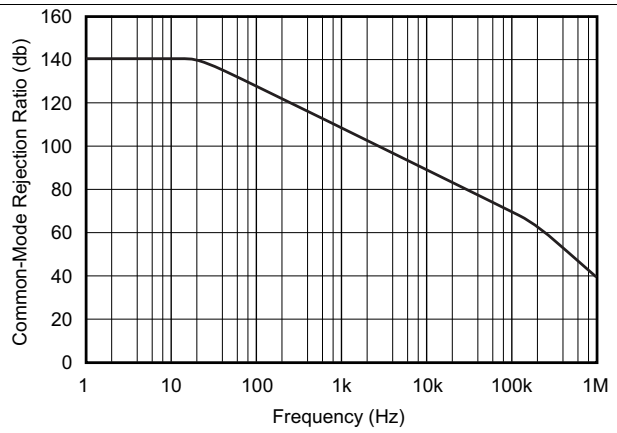


Figure 7. Gain vs Frequency



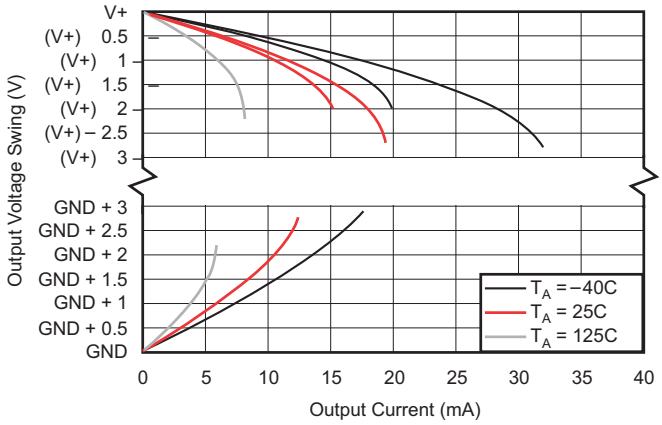
V_S = 5 V + 250-mV sine disturbance
V_{CM} = 0 V V_{REF} = 2.5 V V_{DIF} = shorted

Figure 8. Power-Supply Rejection Ratio vs Frequency



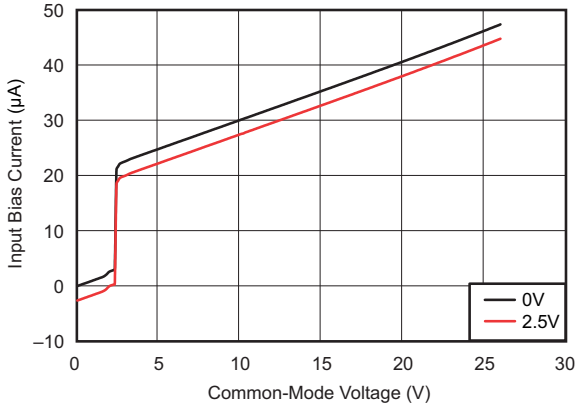
V_S = 5 V V_{CM} = 1 V sine V_{DIF} = shorted
V_{REF} = 2.5 V

Figure 9. Common-Mode Rejection Ratio vs Frequency



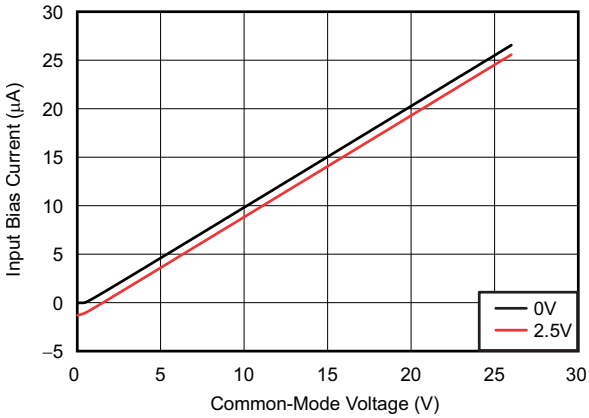
V_S = 2.7 V V_S = 2.7 V V_S = 5 V to 26 V
V_S = 2.7 V to 26 V

Figure 10. Output Voltage Swing vs Output Current



I_{B+}, $I_{B–}$, V_{REF} = 0 V
I_{B+}, $I_{B–}$, V_{REF} = 2.5 V

Figure 11. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 5 V



I_{B+}, $I_{B–}$, V_{REF} = 0 V I_{B+}, $I_{B–}$, V_{REF} = 2.5 V I_{B+}, V_{REF} = 2.5 V

Figure 12. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

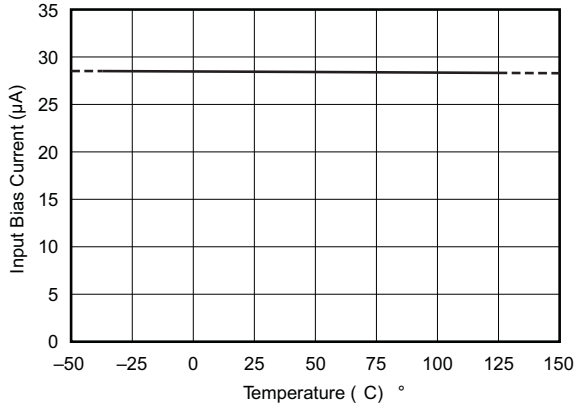


Figure 13. Input Bias Current vs Temperature

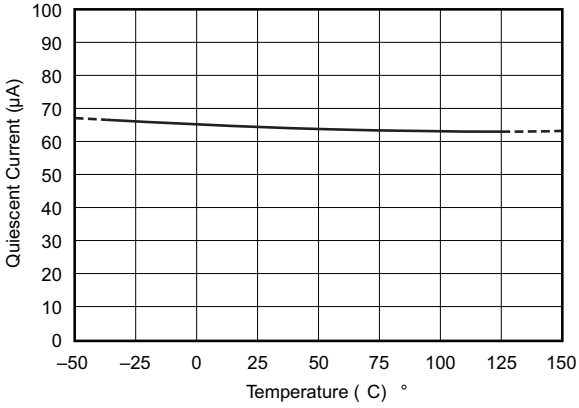
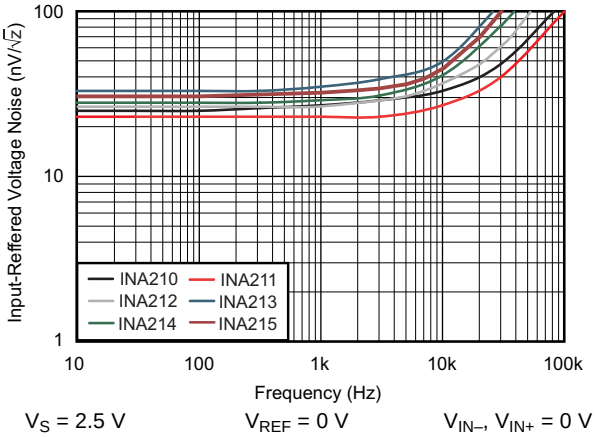
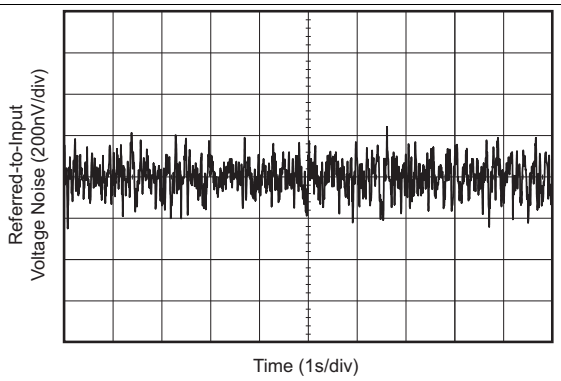


Figure 14. Quiescent Current vs Temperature



V_S = 2.5 V V_{REF} = 0 V $V_{IN–}$, V_{IN+} = 0 V

Figure 15. Input-Referred Voltage Noise vs Frequency



V_S = 2.5 V V_{CM} = 0 V V_{DIF} = 0 V
V_{REF} = 0 V

Figure 16. 0.1-Hz to 10-Hz Voltage Noise (Referred-To-Input)

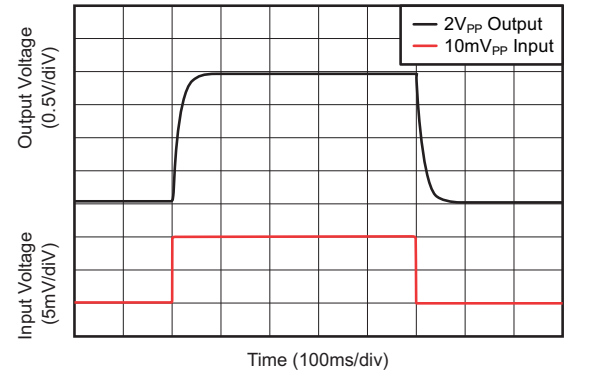


Figure 17. Step Response (10-mV_{PP} Input Step)

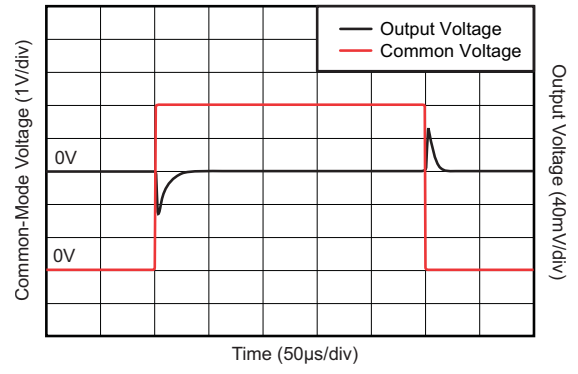


Figure 18. Common-Mode Voltage Transient Response

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

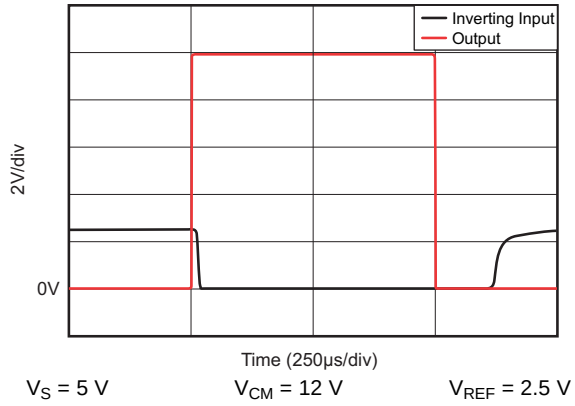


Figure 19. Inverting Differential Input Overload

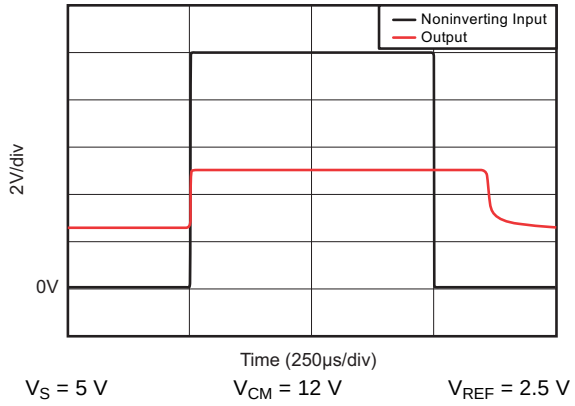


Figure 20. Noninverting Differential Input Overload

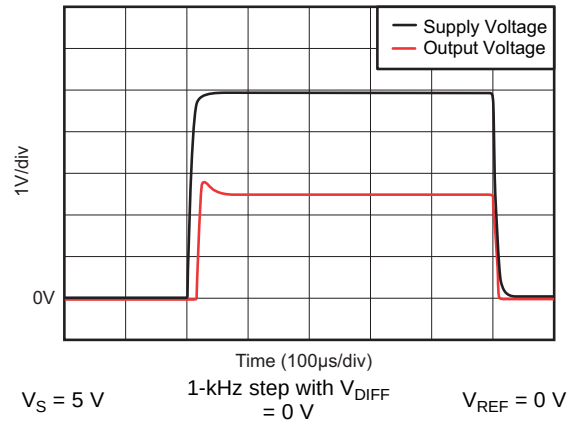


Figure 21. Start-Up Response

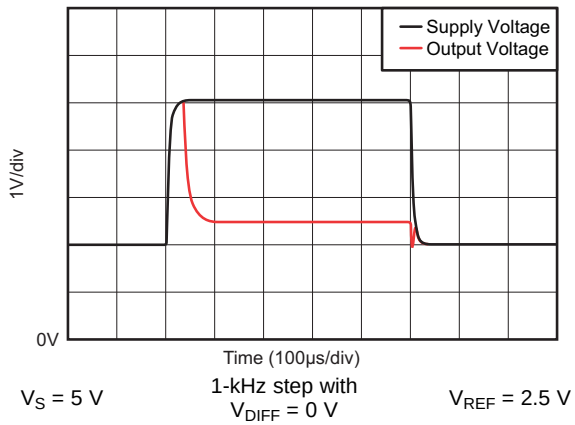


Figure 22. Brownout Recovery

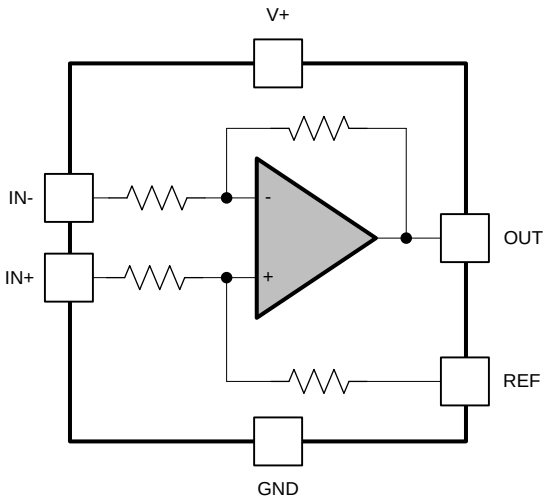
7 Detailed Description

7.1 Overview

The INA21x are 26-V, common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connections

Figure 23 shows the basic connections of the INA21x. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

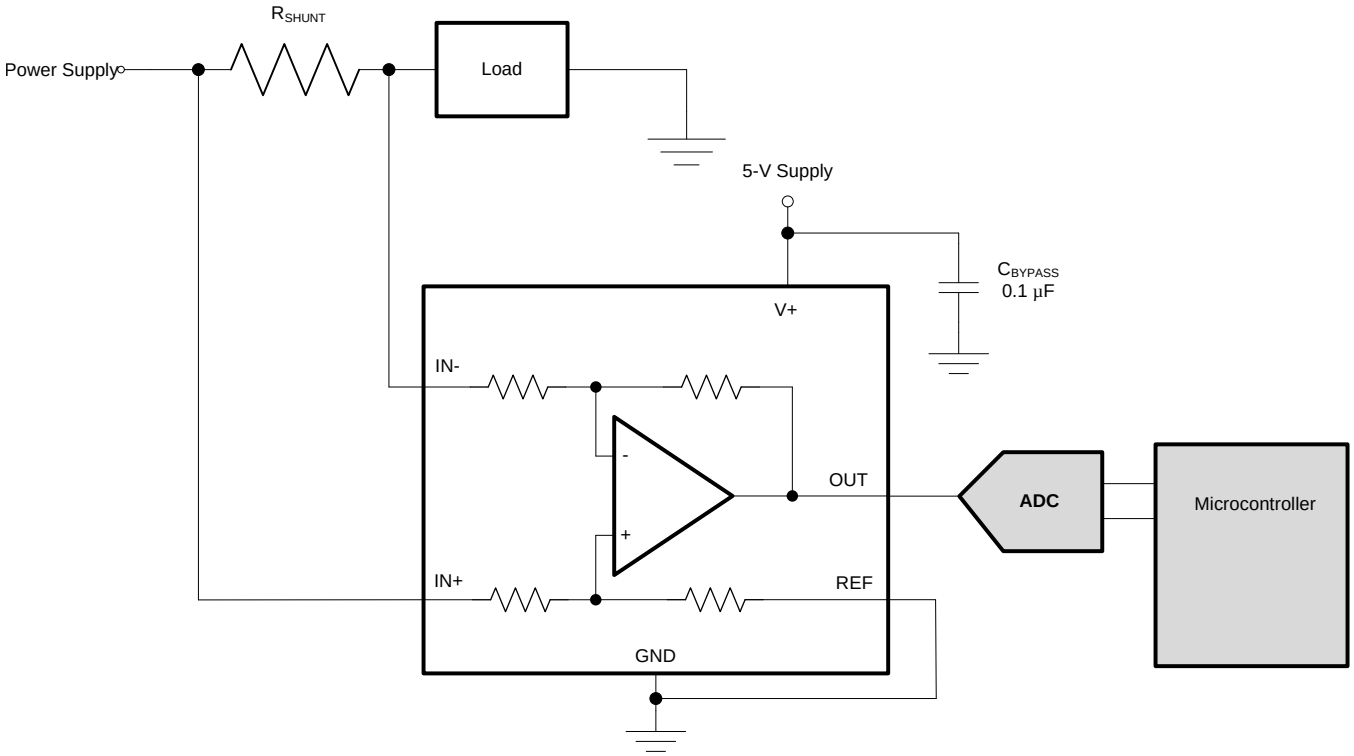


Figure 23. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package options, two pins are provided for each input. Tie these pins together (that is, tie IN+ to IN+ and tie IN– to IN–).

7.3.2 Selecting R_S

The zero-drift offset performance of the INA21x offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The INA21x series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA213, INA214, or INA215 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA213 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 60 mV, with only 100 µV of offset.

7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 24 shows a filter placed at the inputs pins.

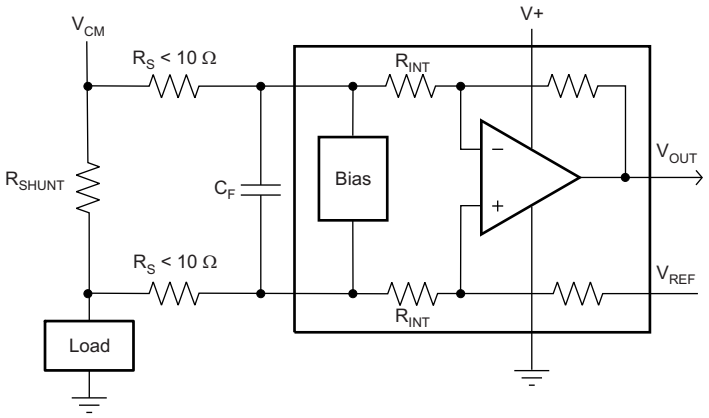


Figure 24. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in Figure 24 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 24). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (1)$$

where:

- R_{INT} is the internal input resistor (R3 and R4), and
- R_S is the external series resistance.

Device Functional Modes (continued)

With the adjustment factor from Equation 1, including the device internal input resistance, this factor varies with each gain version, as shown in Table 1. Each individual device gain error factor is shown in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (k)
INA210	200	5
INA211	500	2
INA212	1000	1
INA213	50	20
INA214	100	10
INA215	75	13.3

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA210	$\frac{1000}{R_S + 1000}$
INA211	$\frac{10{,}000}{(13 \times R_S) + 10{,}000}$
INA212	$\frac{}{" \times}$
INA213	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
INA214	$\frac{10{,}000}{(9 \times R_S) + 10{,}000}$
INA215	$\frac{8{,}000}{(7 \times R_S) + 8{,}000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

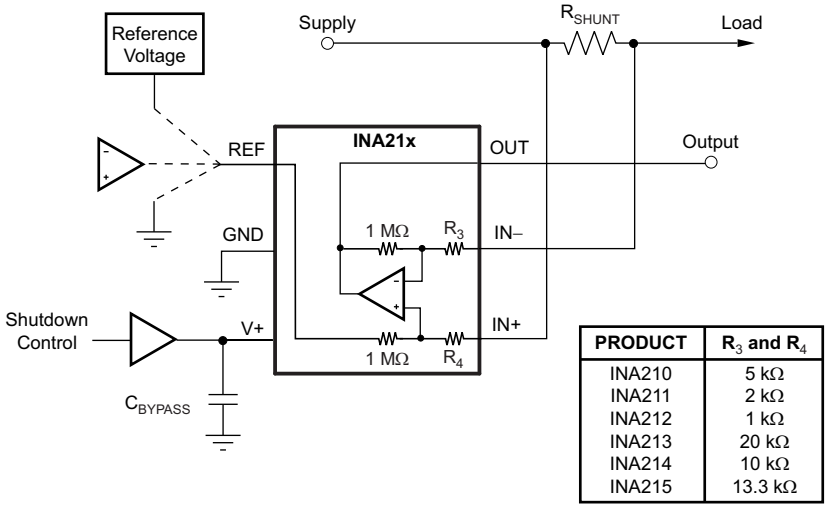
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA212 and the corresponding gain error equation from Table 2, a series resistance of 10 Ω results in a gain error factor of 0.982. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 1.77% solely because of the external 10-Ω series resistors. Using an INA213 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

7.4.2 Shutting Down the INA21x Series

Although the INA21x series does not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INA21x. This gate or switch turns on and turns off the INA21x power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA21x in shutdown mode, as shown in Figure 25.



PRODUCT	R_3 and R_4
INA210	5 kΩ
INA211	2 kΩ
INA212	1 kΩ
INA213	20 kΩ
INA214	10 kΩ
INA215	13.3 kΩ

NOTE: 1-MΩ paths from shunt inputs to reference and INA21x outputs.

Figure 25. Basic Circuit for Shutting Down The INA21x With a Grounded Reference

Note that there is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA21x to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the INA21x is shut down, the calculation is direct; instead of assuming 1 MΩ to ground, however, assume 1 MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA21x does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 1-MΩ resistor.

As a final note, when the device is powered up, there is an additional, nearly constant, and well-matched 25 μA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

7.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA21x series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin must be buffered by an op amp.

In systems where the INA21x output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 26 depicts a method of taking the output from the INA21x by using the REF pin as a reference.

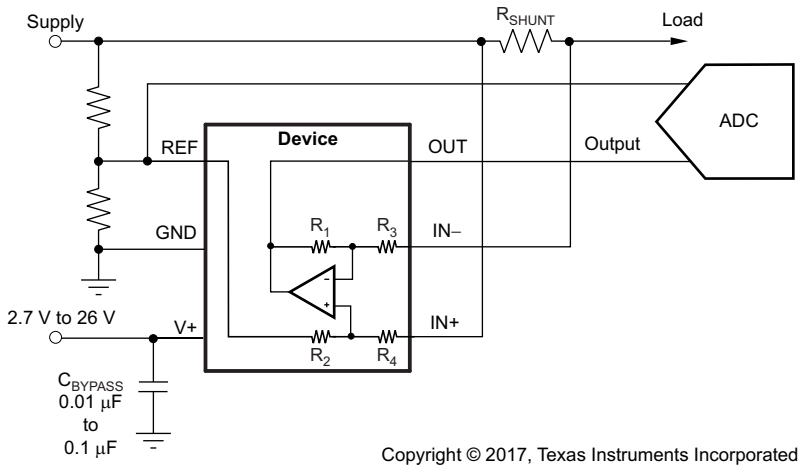


Figure 26. Sensing the INA21x to Cancel the Effects of Impedance on the REF Input

7.4.4 Using The INA21x With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA21x series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only zener diode or zener-type transient absorbers (sometimes referred to as *transzorbs*) ;any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the zener; see Figure 27. Keeping these resistors as small as possible is preferable, typically around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Input Filtering* section. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

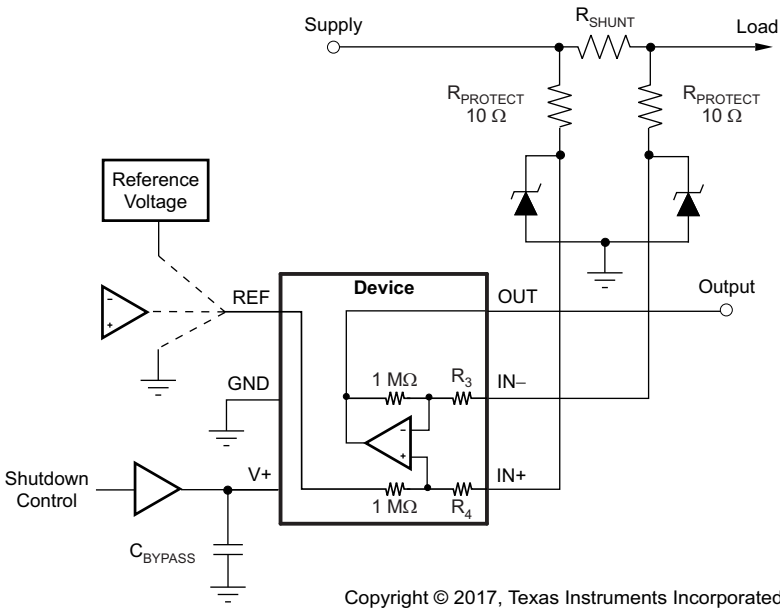


Figure 27. INA21x Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 28. In either of these examples, the total board area required by the INA21x with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

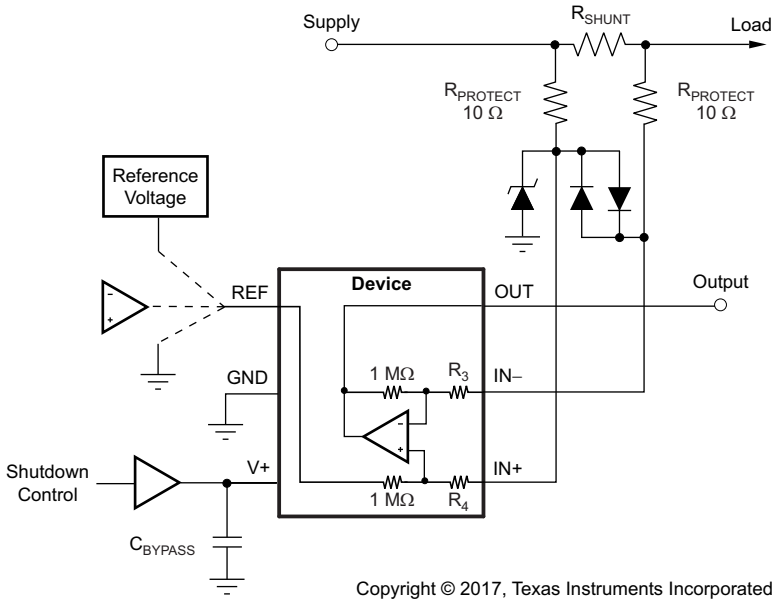


Figure 28. INA21x Transient Protection Using a Single Transzorb and Input Clamps

7.4.5 Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, keep these resistances under 10 Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 29.

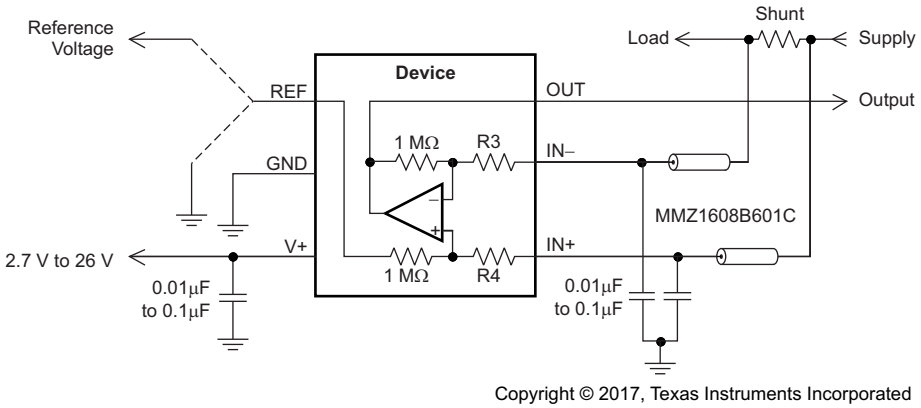


Figure 29. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B and C devices are now available with new ESD structures that are not susceptible to this latching condition. Version B and C devices are incapable of sustaining these damage-causing latched conditions so these devices do not have the same sensitivity to the transients that the version A devices have, thus making the version B and C devices a better fit for these applications.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA21x devices measure the voltage developed across a current-sensing resistor when current passes through the device. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

8.2 Typical Applications

8.2.1 Unidirectional Operation

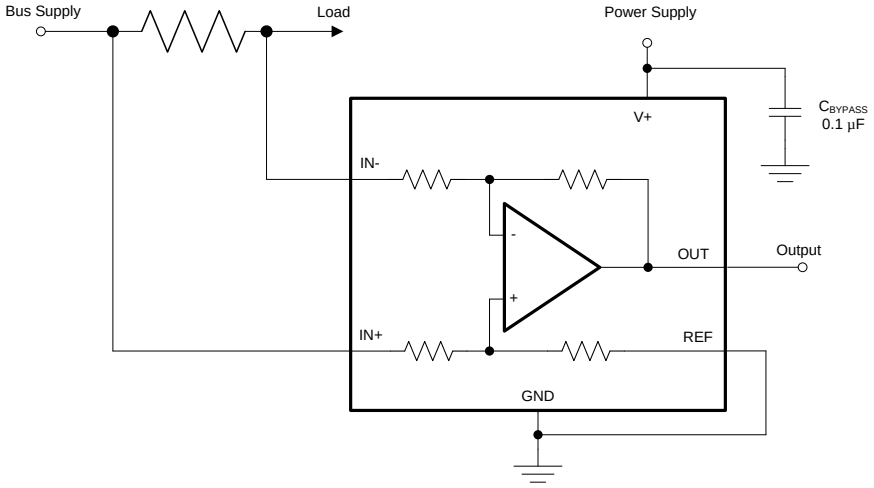


Figure 30. Unidirectional Application Schematic

8.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 30. When the input signal increases, the output voltage at the OUT pin increases.

8.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

Typical Applications (continued)

8.2.1.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 31. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

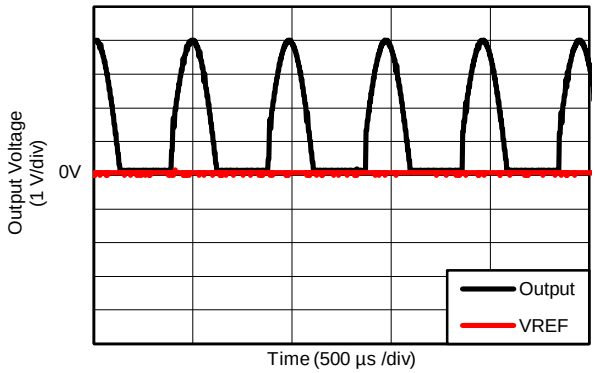


Figure 31. Unidirectional Application Output Response

Typical Applications (continued)

8.2.2 Bidirectional Operation

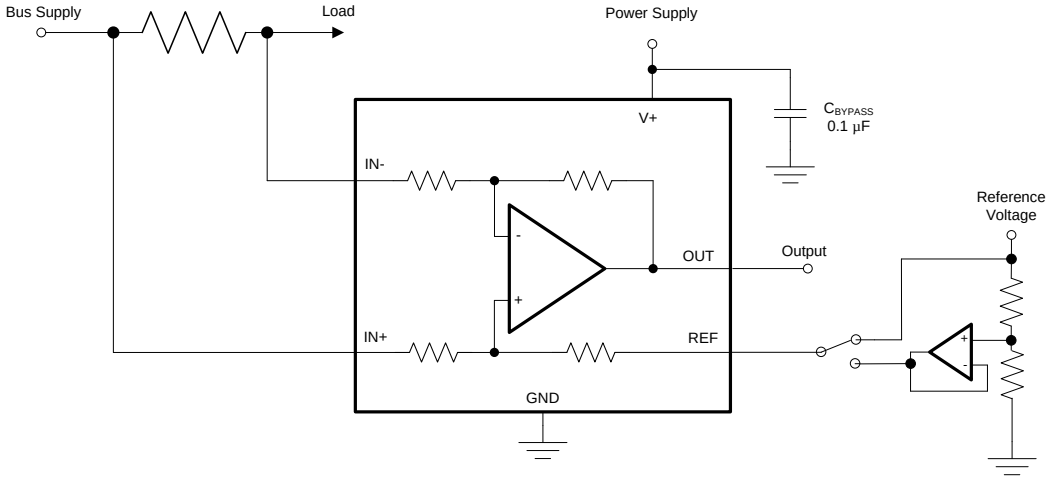


Figure 32. Bidirectional Application Schematic

8.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

8.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 32. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, V_{REF} is typically set at midscale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than midscale when the bidirectional current and corresponding output signal do not need to be symmetrical.

8.2.2.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 33. With the REF pin connected to a reference voltage (2.5 V in this case) the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

Typical Applications (continued)

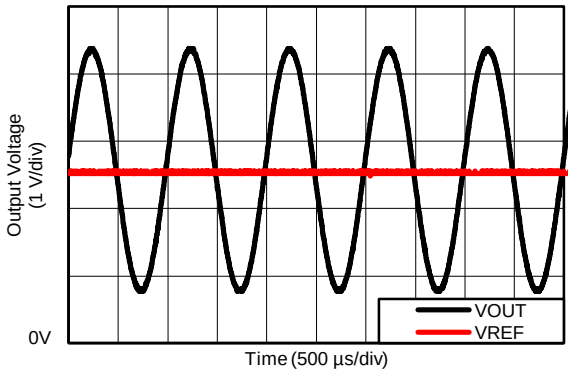


Figure 33. Bidirectional Application Output Response

9 Power Supply Recommendations

The input circuitry of the INA21x can accurately measure beyond the power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Note also that the INA21x can withstand the full input signal range up to 26 V at the input pins, regardless of whether the device has power applied or not.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

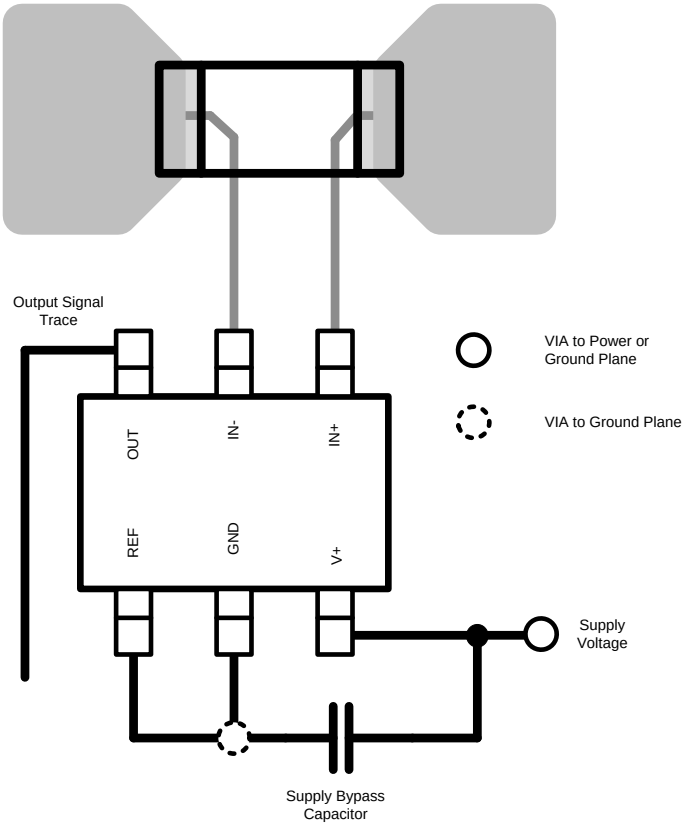


Figure 34. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *INA210-215EVM User's Guide*

11.2 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA210	Click here	Click here	Click here	Click here	Click here
INA211	Click here	Click here	Click here	Click here	Click here
INA212	Click here	Click here	Click here	Click here	Click here
INA213	Click here	Click here	Click here	Click here	Click here
INA214	Click here	Click here	Click here	Click here	Click here
INA215	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA210AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KNJ	Samples
INA210AIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(KNJ, NSJ)	Samples
INA210BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SED	Samples
INA210BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SED	Samples
INA210BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHQ	Samples
INA210BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHQ	Samples
INA210CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16B	Samples
INA210CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16B	Samples
INA210CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16C	Samples
INA210CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16C	Samples
INA211AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEE	Samples
INA211BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEE	Samples
INA211BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13Q	Samples
INA211BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13Q	Samples
INA211CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16D	Samples
INA211CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16D	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA211CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16U	Samples
INA211CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16U	Samples
INA212AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples
INA212AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples
INA212BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEC	Samples
INA212BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEC	Samples
INA212BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13U	Samples
INA212BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13U	Samples
INA212CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16E	Samples
INA212CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16E	Samples
INA212CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16V	Samples
INA212CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16V	Samples
INA213AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KPJ	Samples
INA213AIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KPJ	Samples
INA213BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEF	Samples
INA213BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEF	Samples
INA213BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHT	Samples
INA213BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHT	Samples
INA213CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16F	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA213CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16F	Samples
INA213CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16W	Samples
INA213CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16W	Samples
INA214AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples
INA214AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples
INA214AIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KRJ	Samples
INA214AIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KRJ	Samples
INA214BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEA	Samples
INA214BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SEA	Samples
INA214BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHU	Samples
INA214BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHU	Samples
INA214CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16G	Samples
INA214CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	16G	Samples
INA214CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16X	Samples
INA214CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16X	Samples
INA215AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SME	Samples
INA215AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	SME	Samples
INA215BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	13S	Samples
INA215BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	13S	Samples
INA215BIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13R	Samples
INA215BIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	13R	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA215CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17K	Samples
INA215CIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17K	Samples
INA215CIRSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16Z	Samples
INA215CIRSWT	ACTIVE	UQFN	RSW	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	16Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA210, INA211, INA212, INA213, INA214, INA215 :

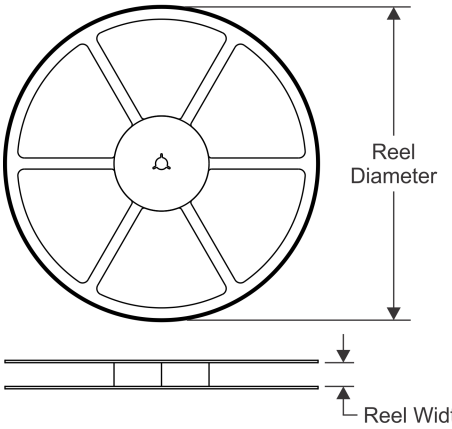
- Automotive : INA210-Q1, INA211-Q1, INA212-Q1, INA213-Q1, INA214-Q1, INA215-Q1

NOTE: Qualified Version Definitions:

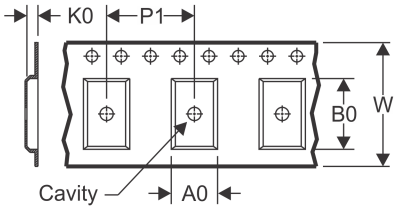
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

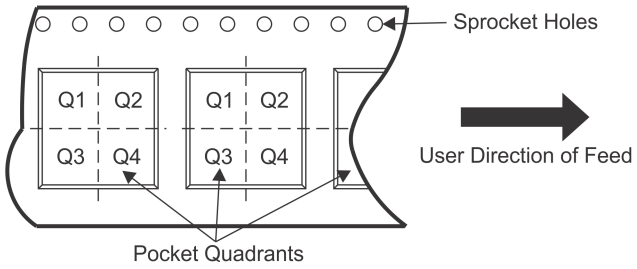


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

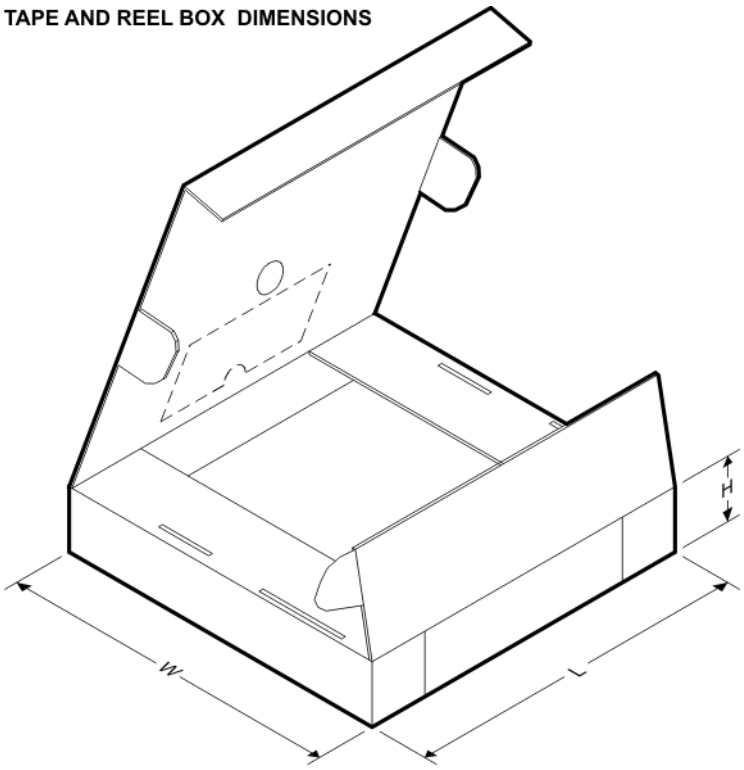
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA210AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA210AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA210BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA210BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA210CIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA211AIDCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA211AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA211AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA211BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA211BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA211CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA211CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA211CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA212AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212AIDCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA212AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212AIDCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
INA212BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA212BIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA212BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA212BIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA212CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA212CIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA212CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA212CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA213AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA213AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA213AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213AIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA213BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA213BIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA213BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA213CIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA214AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA214AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA214AIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214BIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA214BIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA214BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA214CIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA214CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA215AIDCKR	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA215AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA215BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA215BIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA215BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA215CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215CIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215CIRSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA215CIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA215CIRSWT	UQFN	RSW	10	250	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1
INA215CIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA210AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA210AIDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA210AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210AIDCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA210BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA210BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA210BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210BIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA210BIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA210CIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA210CIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA210CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA210CIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA210CIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA210CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA211AIDCKR	SC70	DCK	6	3000	223.0	270.0	35.0
INA211AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA211AIDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA211AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA211AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA211AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA211AIDCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA211AIDCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA211BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA211BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA211BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA211BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA211BIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA211BIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA211CIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA211CIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA211CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA211CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA211CIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA212AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA212AIDCKR	SC70	DCK	6	3000	223.0	270.0	35.0
INA212AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA212AIDCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA212BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA212BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA212BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA212BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA212BIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA212BIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA212BIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA212BIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA212CIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA212CIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA212CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA212CIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA212CIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA212CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA213AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA213AIDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA213AIDCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA213AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213AIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA213AIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA213BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA213BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA213BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213BIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA213BIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA213BIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA213CIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA213CIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA213CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA213CIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA213CIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA213CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA214AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214AIDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
INA214AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214AIDCKT	SC70	DCK	6	250	213.0	191.0	35.0
INA214AIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA214BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214BIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA214BIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA214BIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA214BIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA214CIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214CIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA214CIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA214CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA214CIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA215AIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA215AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA215AIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA215AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA215BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0

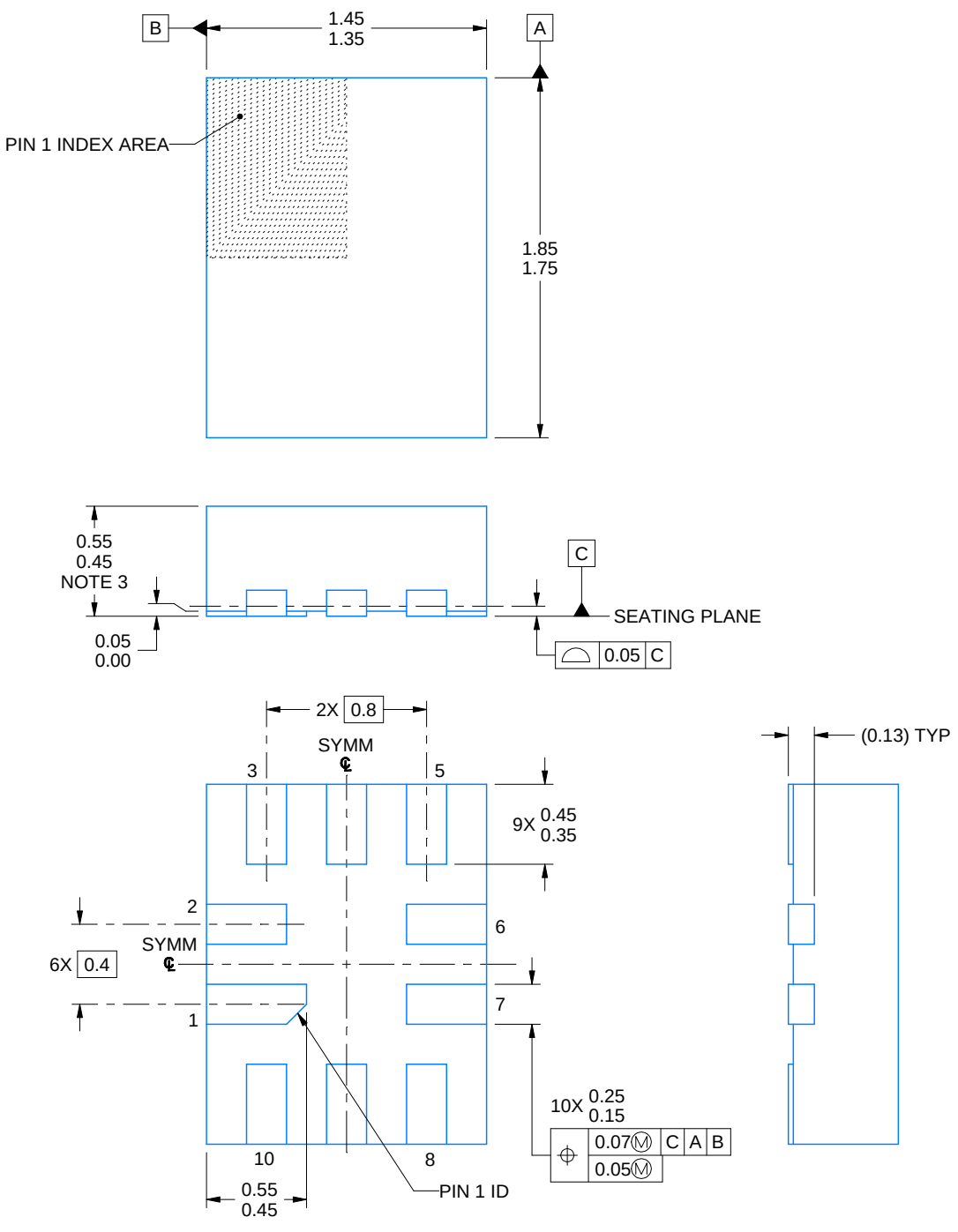
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA215BIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA215BIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA215BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA215BIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA215BIRSWR	UQFN	RSW	10	3000	200.0	183.0	25.0
INA215BIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA215BIRSWT	UQFN	RSW	10	250	200.0	183.0	25.0
INA215CIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA215CIDCKT	SC70	DCK	6	250	340.0	340.0	38.0
INA215CIRSWR	UQFN	RSW	10	3000	189.0	185.0	36.0
INA215CIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA215CIRSWT	UQFN	RSW	10	250	189.0	185.0	36.0
INA215CIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0

RSW0010A

PACKAGE OUTLINE

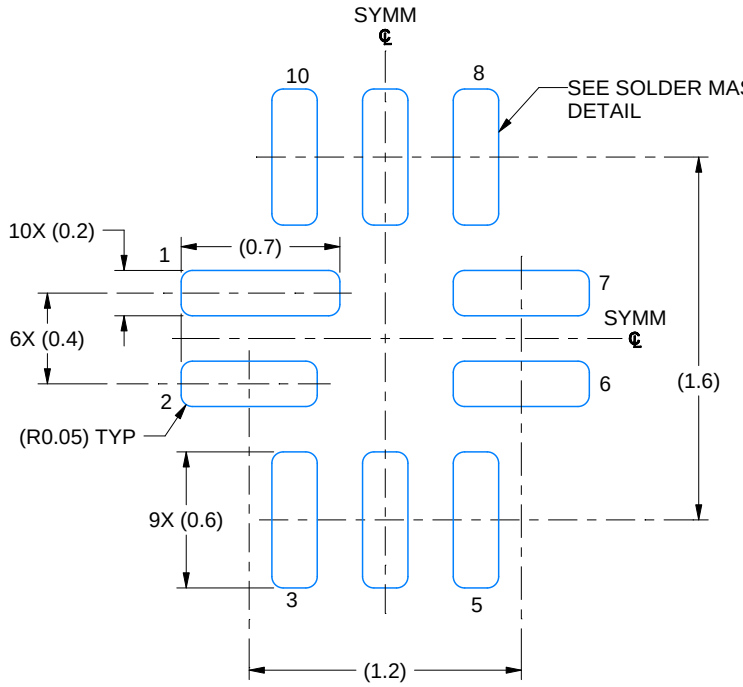
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

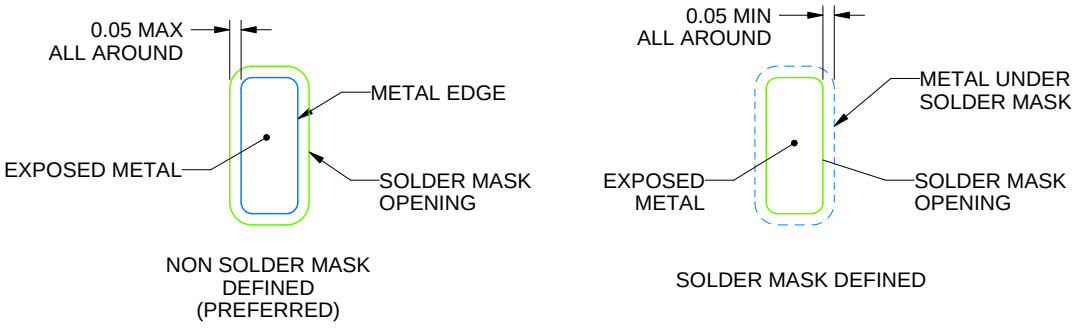


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

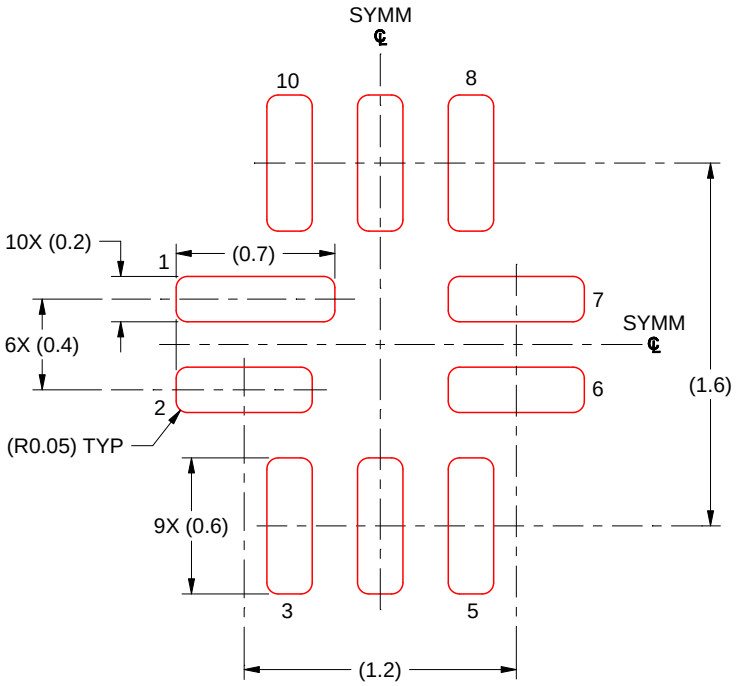


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



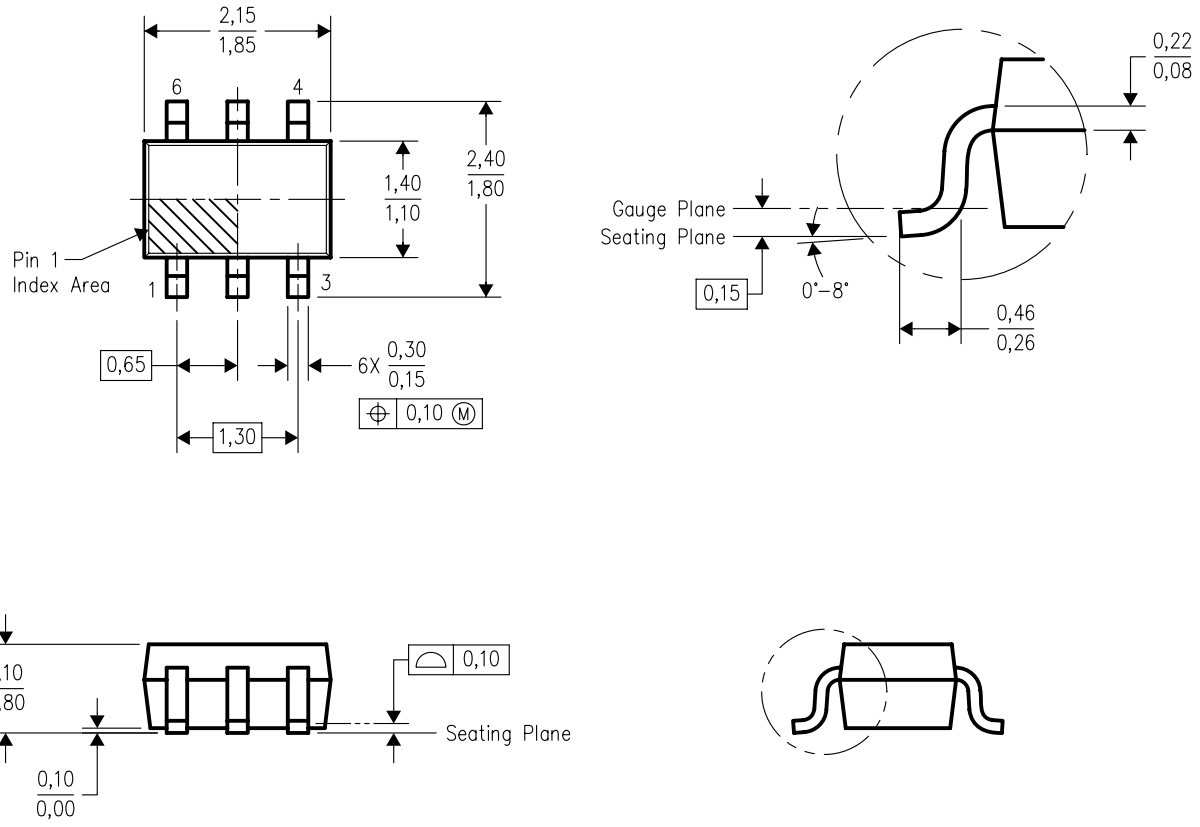
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

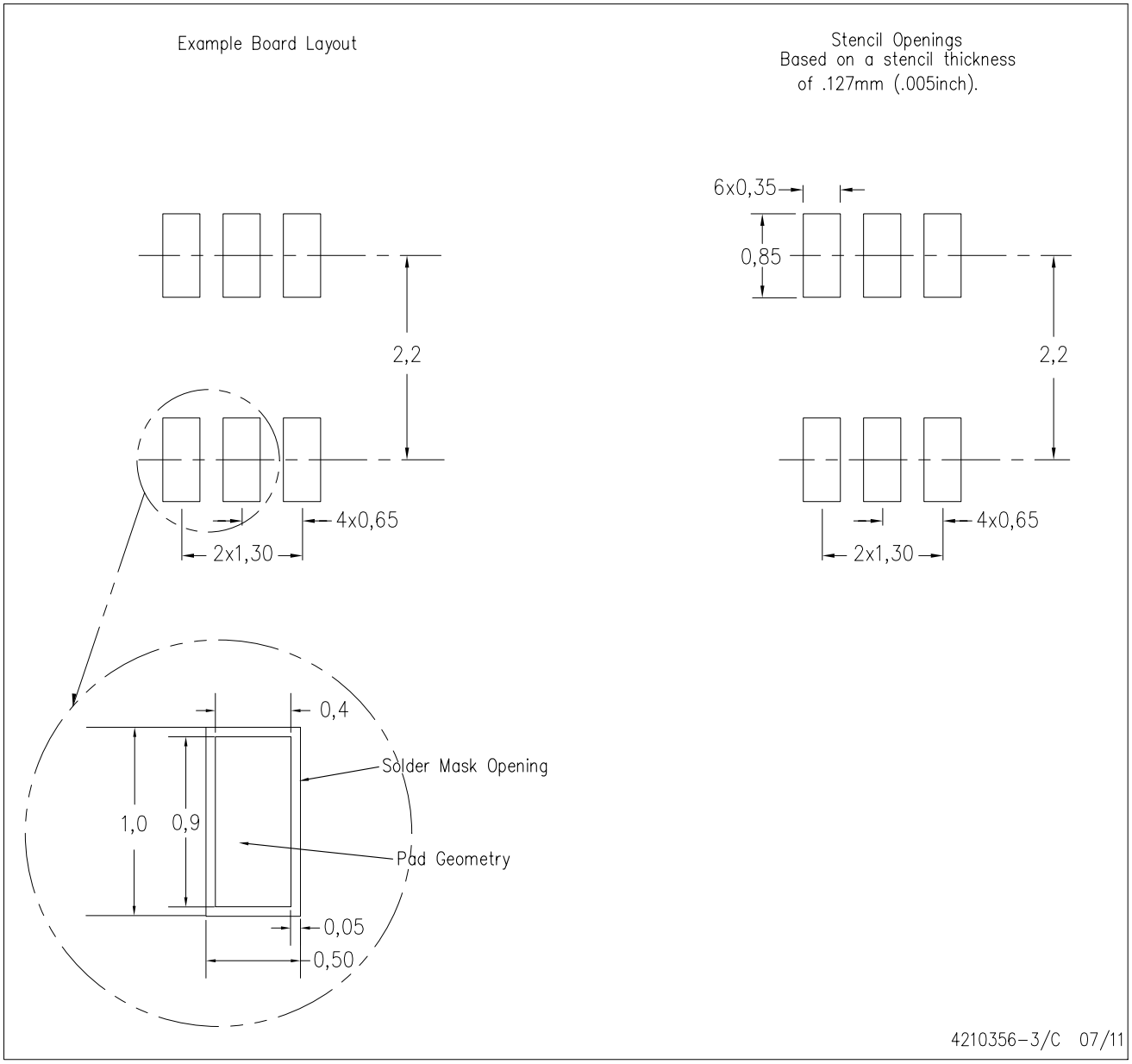
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

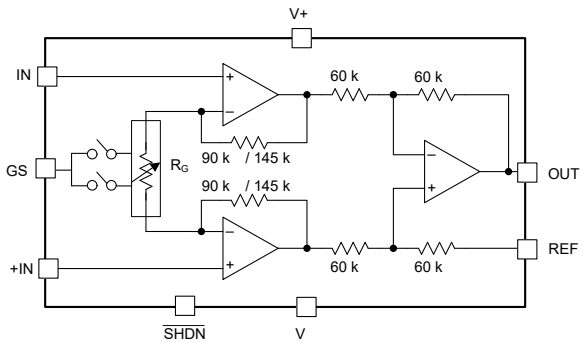
INA350 Cost and Size Optimized, Low Power, 1.8-V to 5.5-V Selectable Gain Instrumentation Amplifier

1 Features

- Ideal for size, cost, and power conscious designs
- Selectable gain options
  - G = 10 or G = 20 (INA350ABS)
  - G = 30 or G = 50 (INA350CDS)
- Space saving ultra-small package options
  - 10-pin X2QFN (RUG) – 3 mm^2
  - 8-pin WSON (DSG) – 4 mm^2
  - 8-pin SOT23-THN (DDF) – 4.64 mm^2
- Optimized performance for 10-bit to 14-bit systems
  - CMRR: 95 dB (typ) across all gains
  - Offset voltage: 0.2 mV (typ) across all gains
  - Gain error (typ):
    - 0.05% for G = 10; 0.06% for G = 20
    - 0.075% for G = 30; 0.082% for G = 50
- Bandwidth: 100 kHz for G = 10 (typ)
- Drives 500 pF with less than 20% overshoot (typ)
- Optimized quiescent current: 100 µA (typ)
- Shutdown option for power conscious applications
- Supply range: 1.8 V (±0.9 V) to 5.5 V (±2.75 V)
- Specified temperature range: –40°C to 125°C

2 Applications

- Bridge network sensing
- Differential to single-ended conversion
- Weigh scale
- Analog input module
- Flow transmitter
- Wearable fitness and activity monitor
- Blood glucose monitor
- Pressure and temperature sensing



Note: 90 kΩ for INA350ABS and 145 kΩ for INA350CDS

Simplified Internal Schematic

3 Description

INA350 is a selectable-gain instrumentation amplifier that offers four gain options across INA350ABS and INA350CDS variants available in small packages. INA350ABS has gain options of 10 or 20 and INA350CDS has gain options of 30 or 50. These gain options can be selected by toggling the gain select (GS) pin. INA350 is ideal for bridge-type sensing and for differential to single-ended conversion applications.

Built with precision matched integrated resistors, INA350 saves on BOM costs, pick-and-place machine handling costs, and board space by removing the need for precise or closely-matched external resistors. The device interface directly to low-speed, 10-bit to 14-bit, analog-to-digital converters (ADC) and is ideal for replacing discrete implementation of instrumentation amplifiers built with commodity amplifiers and discrete resistors.

Designed with the three-amplifier architecture, INA350 is optimized for delivering performance. It achieves 85 dB of minimum CMRR and 0.6% of maximum gain error, along with 1.2 mV of maximum offset across all gain options, while consuming just 125 µA of maximum quiescent current. It has an integrated shutdown option to turn off the amplifier when idle for additional power savings in battery powered applications.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA350ABS, INA350CDS	WSON (8)	2.00 mm × 2.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
	X2QFN (10)(2)	1.50 mm × 2.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) This package is preview only.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2021) to Revision B (April 2022)	Page
• Removed the preview note for INA350CDS from the *Device Information* table	1
• Removed the preview note for INA350CDS from the *Device Comparison Table*	3
• Updated the *Electrical Characteristics* table for INA350CDS production release	6
• Included G = 30 and G = 50 data into the *EMIRR Testing* curve	21
• Included G = 30 and G = 50 data into the *Input Common-Mode Voltage vs Output Voltage* curve	28
• Removed the note about external resistor, RG	30

Changes from Revision * (November 2021) to Revision A (December 2021)	Page
• Changed the device status from *Advance Information* to *Production Data*	1

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS		
		SOT-23-8 DDF	WSON DSG	X2QFN RUG(1)
INA350ABS	1	8	8	8
INA350CDS	1	8	8	8

(1) Package is preview only.

6 Pin Configuration and Functions

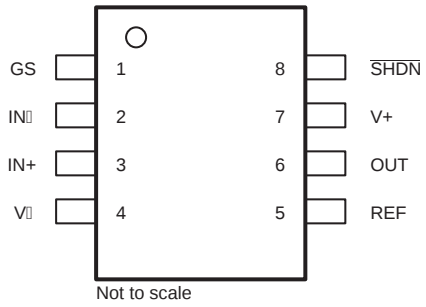
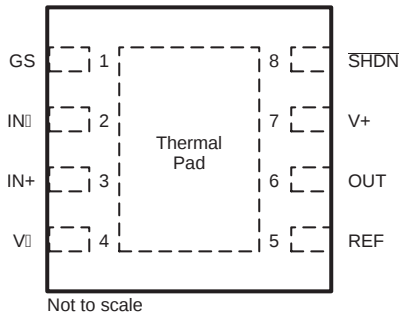


Figure 6-1. DDF Package
8-Pin SOT-23
(Top View)



Note: Connect Thermal Pad to (V−)

Figure 6-2. DSG Package
8-Pin WSON With Exposed Thermal Pad
(Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Negative (inverting) input
IN+	3	O	Positive (non-inverting) input
OUT	6	—	Output
REF	5	—	Reference input. This pin must be driven by a low impedance source.
GS	1	I	Gain select – logic low (G = 10 for INA350ABS and G = 30 for INA350CDS) Gain select – logic high (G = 20 for INA350ABS and G = 50 for INA350CDS) Gain select – no connect (G = 20 for INA350ABS and G = 50 for INA350CDS)
$\overline{\text{SHDN}}$	8	I	Shutdown – logic high (device enabled) Shutdown – logic low (device disabled) Shutdown – no connect (device enabled)
V–	4	—	Negative supply
V+	7	—	Positive supply

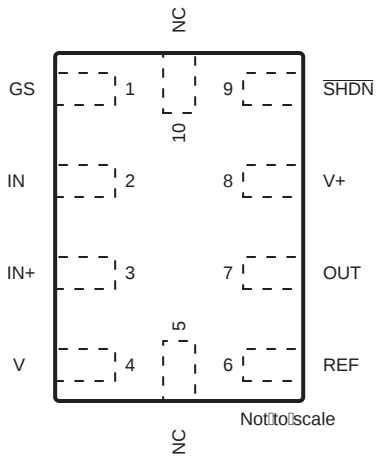


Figure 6-3. RUG Package
10-Pin X2QFN
(Top View)

Table 6-2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Negative (inverting) input
IN+	3	O	Positive (noninverting) input
OUT	7	—	Output
REF	6	—	Reference input. This pin must be driven by a low impedance source.
GS	1	I	Gain select – logic low (G = 10 for INA350ABS and G = 30 for INA350CDS) Gain select – logic high (G = 20 for INA350ABS and G = 50 for INA350CDS) Gain select – no connect (G = 20 for INA350ABS and G = 50 for INA350CDS)
$\overline{\text{SHDN}}$	9	I	Shutdown – logic high (device enabled) Shutdown – logic low (device disabled) Shutdown – no connect (device enabled)
V–	4	—	Negative supply
V+	8	—	Positive supply
NC	5, 10	—	No connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6	V
Signal input pins	Common mode voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(2)	–10	10	mA
Output short-circuit(4)		Continuous		
Operating Temperature, T_A		–55	150	°C
Junction Temperature, T_J			150	
Storage Temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less
(3) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.
(4) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S = (V+) – (V–)	Single-supply	1.8	5.5	V
	Dual-supply	±0.9	±2.75	
Input Voltage Range		(V–)	(V+)	V
Specified temperature	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA350ABS, INA350CDS			UNIT
		DDF (SOT-23-THN)	DSG (WSON)	RUG (X2QFN)	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.1	89.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	101.7	111.8	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.8	55.8	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.6	9.3	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.3	55.7	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	31.0	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{REF} = V_S/2, G = 10, 20, 30 & 50, R_L = 10 kΩ connected to V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Offset Voltage, RTI(1)	V_S = 5.5 V	T_A = 25°C		±0.2	±1.2	mV
V_{OSI}	Offset Voltage over T, RTI(1)	V_S = 5.5 V	T_A = –40°C to 125°C			±1.3	mV
V_{OSI}	Offset temp drift, RTI(2)	V_S = 5.5 V	T_A = –40°C to 125°C		±0.6		µV/°C
PSRR	Power-supply rejection ratio		T_A = 25°C		20	75	µV/V
Z_{IN-DM}	Differential Impedance				100 || 5		GΩ || pF
Z_{IN-CM}	Common Mode Impedance				100 || 9		GΩ || pF
V_{CM}	Input Stage Common Mode Range(3)			(V–)		(V+)	V
CMRR DC	Common-mode rejection ratio, RTI	V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 5.5 V, V_{REF} = V_S/2	85	95		dB
CMRR DC	Common-mode rejection ratio, RTI	V_{CM} = (V–) + 0.1 V to (V+) – 1 V, High CMRR Region	V_S = 3.3 V, V_{REF} = V_S/2		94		dB
CMRR DC	Common-mode rejection ratio, RTI	V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	V_S = 5.5 V, V_{REF} = V_S/2	62	75		dB
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			±0.65		pA
I_{OS}	Input offset current	V_{CM} = V_S / 2			±0.25		pA
NOISE VOLTAGE							
e_{NI}	Input referred voltage noise density(5)		f = 1 kHz		36		nV/√Hz
e_{NI}	Input referred voltage noise density(5)		f = 10 kHz		34		nV/√Hz
E_{NI}	Input referred voltage noise(5)	f_B = 0.1 Hz to 10 Hz			3.2		$µV_{PP}$
i_n	Input current noise	f = 1 kHz	f = 1 kHz		22		fA/√Hz
GAIN							
GE	Gain error(4)	G = 10, V_{REF} = V_S/2	V_O = (V–) + 0.1 V to (V+) – 0.1V		±0.05	±0.50	%
		G = 20, V_{REF} = V_S/2			±0.06	±0.60	
	Gain error(4)	G = 30, V_{REF} = V_S/2			±0.075	±0.60	
		G = 50, V_{REF} = V_S/2			±0.082	±0.60	
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
V_{OL}	Negative rail headroom	R_L = 10 kΩ to V_S/2			15	30	mV
C_L Drive	Load capacitance drive	V_O = 100 mV step, Overshoot < 20%			500		pF
Z_O	Closed-loop output impedance	f = 10 kHz			51		Ω
I_{SC}	Short-circuit current	V_S = 5.5 V			±20		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 10	V_{IN} = 10 mV_{pk-pk}		100		kHz
		G = 20			50		
	Bandwidth, –3 dB	G = 30			40		
		G = 50			25		
THD + N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, G = 10, R_L = 100 kΩ f = 1 kHz, 80-kHz measurement BW			0.04		%
THD + N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, G = 50, R_L = 100 kΩ f = 1 kHz, 80-kHz measurement BW	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, G = 50, R_L = 100 kΩ f = 1 kHz, 80-kHz measurement BW		0.15		%

7.5 Electrical Characteristics (continued)

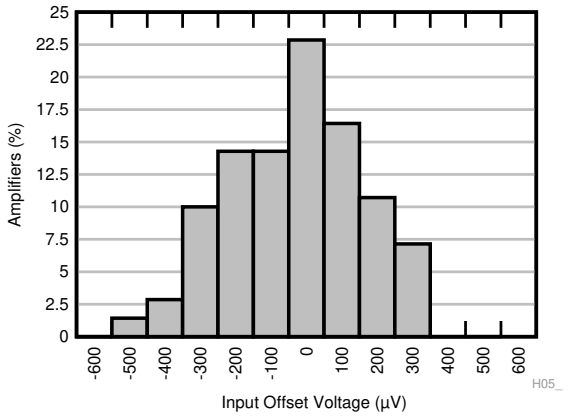
For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, V_{REF} = V_S/2, G = 10, 20, 30 & 50, R_L = 10 kΩ connected to V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V_{IN_EMIRR} = 100 mV			96		dB
SR	Slew rate	V_S = 5 V, V_O = 2 V step			0.24		V/µs
t_S	Settling time	G = 10, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			17		µs
		G = 10, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			38		
		G = 20, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			20		
		G = 20, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			27		
	Settling time	G = 30, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			30		
		G = 30, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			57		
		G = 50, To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			44		
		G = 50, To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, C_L = 10 pF			85		
	Overload recovery	V_{IN} = 1 V, G = 10			16		µs
	Overload recovery	V_{IN} = 1 V, G = 50	V_{IN} = 1 V, G = 50		6.5		µs
REFERENCE INPUT							
R_{IN}	Input impedance				60		kΩ
	Voltage range			(V–)		(V+)	V
	Gain to output				1		V/V
	Reference gain error				±0.004		%
POWER SUPPLY							
V_S	Power-supply voltage	Single-supply		1.7		5.5	V
V_S	Power-supply voltage	Dual-supply		±0.85		±2.75	V
I_Q	Quiescent current	V_{IN} = 0 V			100	125	µA
		T_A = –40°C to 125°C				135	
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–			0.70	1.25	µA
V_{IL}	Logic low threshold voltage (Gain Select)	G = 10 for INA350ABS, G = 30 for INA350CDS				(V–) + 0.2 V	V
V_{IH}	Logic high threshold voltage (Gain Select)	G = 20 for INA350ABS, G = 50 for INA350CDS		(V–) + 1 V			V
t_{ON}	Amplifier enable time (full shutdown) (6)	V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–			100		µs
t_{OFF}	Amplifier disable time (6)	V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–			4		µs
	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V			10		nA
	$\overline{SHDN}$ pin input bias current (per pin)	(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V			175		nA

(1) Total offset, referred-to-input (RTI): V_{OS} = (V_{OSI}) + (V_{OSO} / G).
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}{}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Input common mode voltage range of the just the input stage of the instrumentation amplifier. The entire INA350x input range depends on the combination input common-mode voltage, differential voltage, gain, reference voltage and power supply voltage. *Typical Characteristic* curves will be added with more information.
(4) Min and Max values are specified by characterization.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}{}^2 + (e_{NO} / G)^2]}$
(6) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

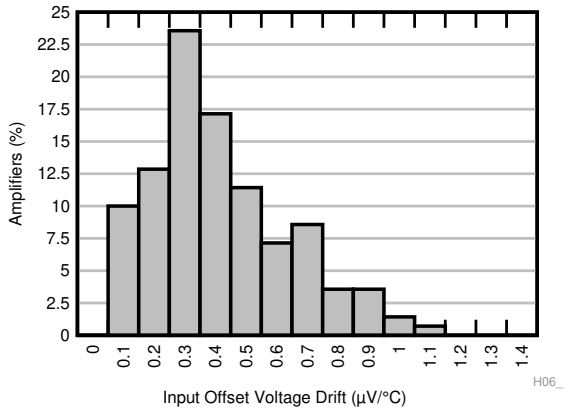
7.6 Typical Characteristics

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



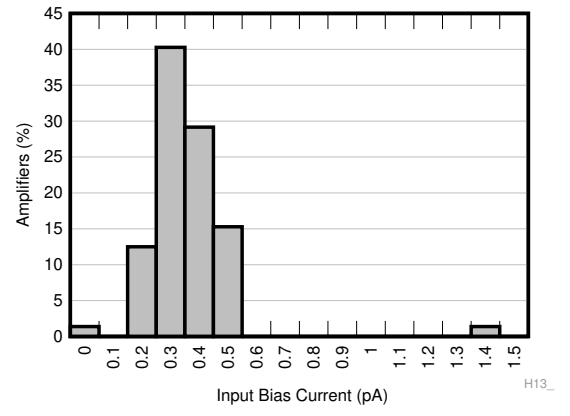
G = 10, 20, 30, 50 N = 140 µ = 18 µV σ = 0.185 mV

Figure 7-1. Typical Distribution of Input Referred Offset Voltage



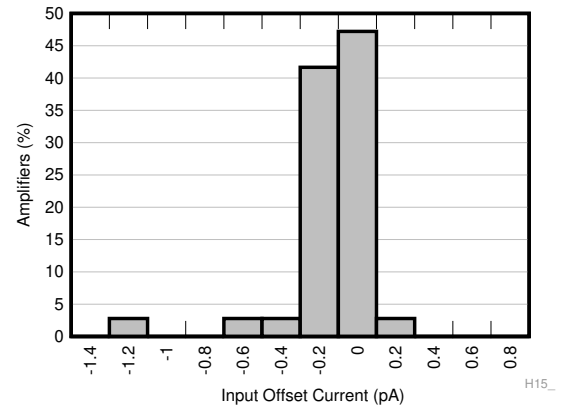
G = 10, 20, 30, 50 N = 140 µ = 0.37 µV/°C σ = 0.23 µV/°C

Figure 7-2. Typical Distribution of Input Referred Offset Drift



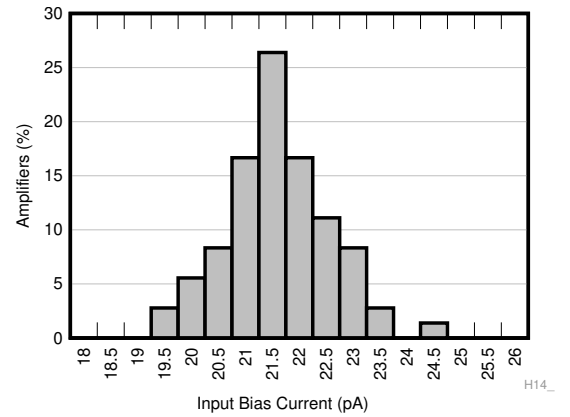
T_A = 25°C N = 72 µ = 0.40 pA σ = 0.15 pA

Figure 7-3. Typical Distribution of Input Bias Current



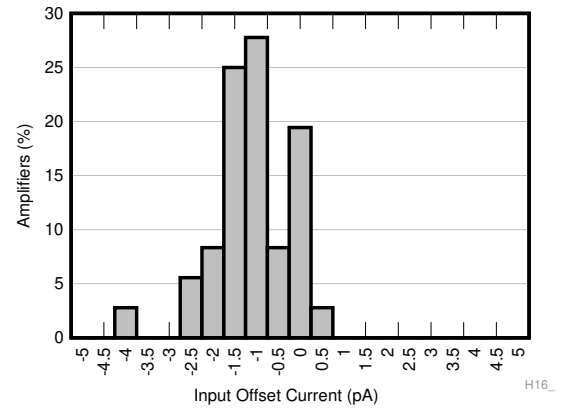
T_A = 25°C N = 36 µ = –0.03 pA σ = 0.23 pA

Figure 7-4. Typical Distribution of Input Offset Current



T_A = 85°C N = 72 µ = 22 pA σ = 0.95 pA

Figure 7-5. Typical Distribution of Input Bias Current

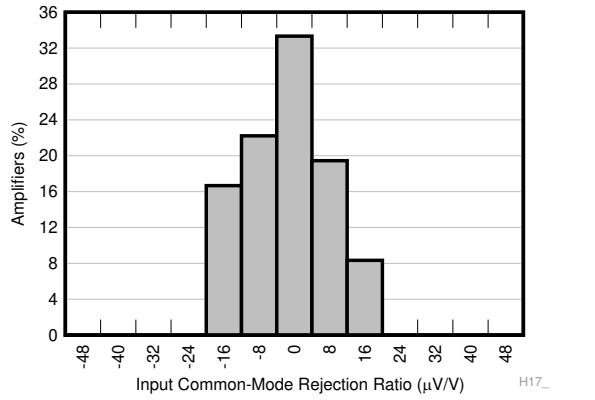


T_A = 85°C N = 36 µ = –1 pA σ = 1 pA

Figure 7-6. Typical Distribution of Input Offset Current

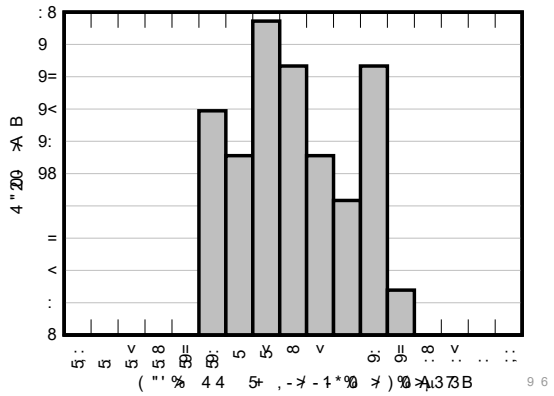
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



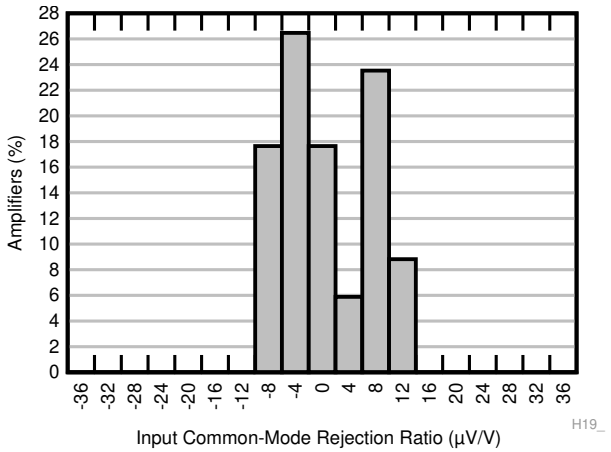
G = 10 N = 36 µ = 2.50 µV/V σ = 8.92 µV/V

Figure 7-7. Typical Distribution of CMRR



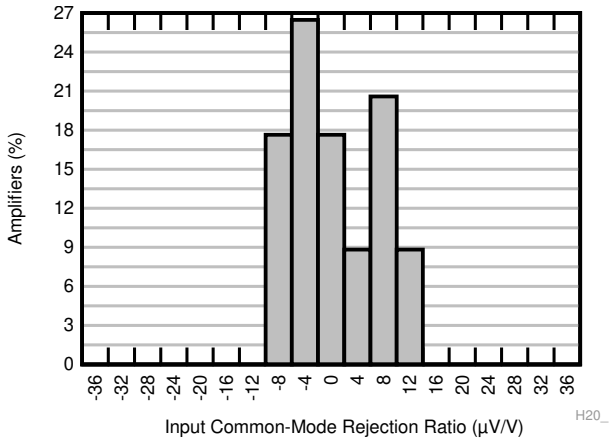
G = 20 N = 36 µ = 2.33 µV/V σ = 8.45 µV/V

Figure 7-8. Typical Distribution of CMRR



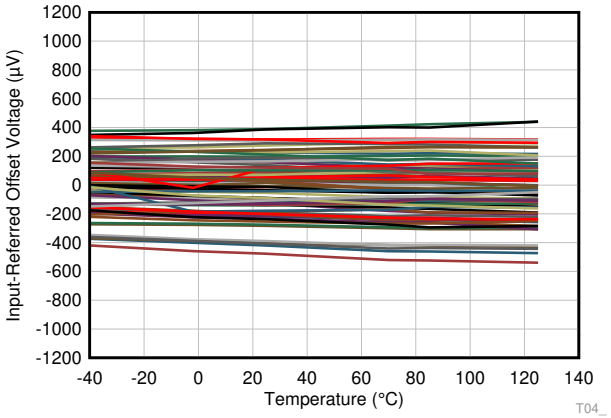
G = 30 N = 34 µ = –1.05 µV/V σ = 6.85 µV/V

Figure 7-9. Typical Distribution of CMRR



G = 50 N = 34 µ = –1.43 µV/V σ = 6.62 µV/V

Figure 7-10. Typical Distribution of CMRR



G = 10, 20, 30, 50

Figure 7-11. Input Referred Offset Voltage vs Temperature

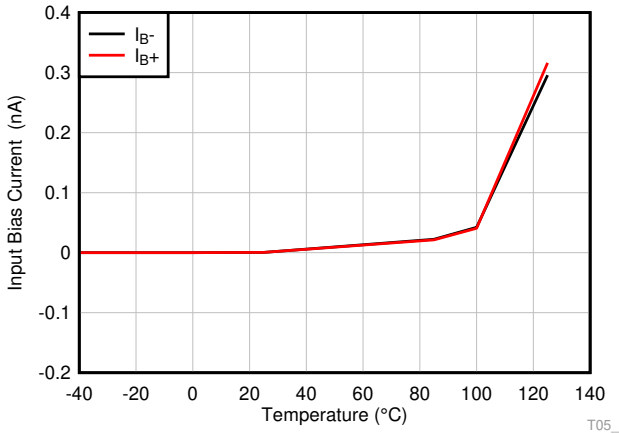


Figure 7-12. Input Bias Current vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

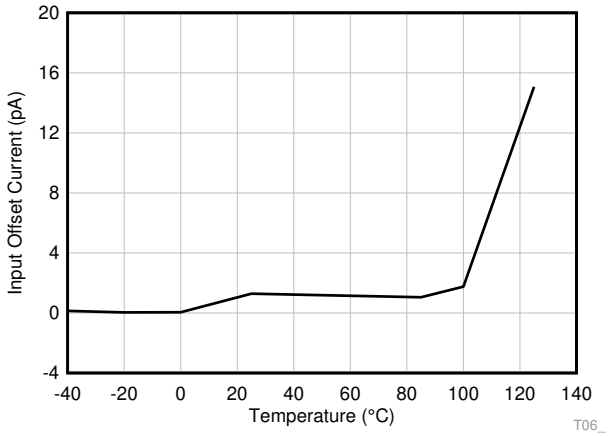


Figure 7-13. Input Offset Current vs Temperature

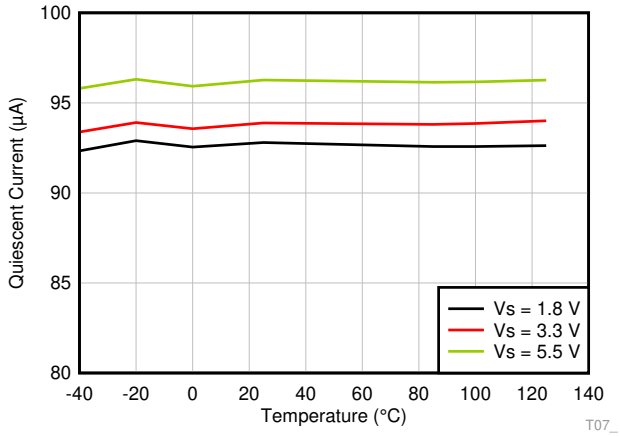


Figure 7-14. Quiescent Current vs Temperature

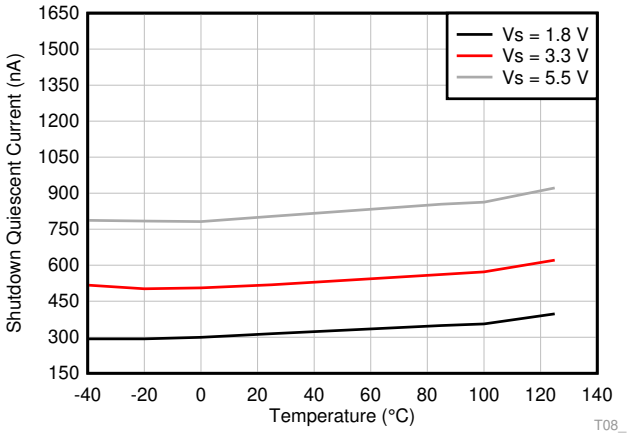


Figure 7-15. Shutdown Quiescent Current vs Temperature

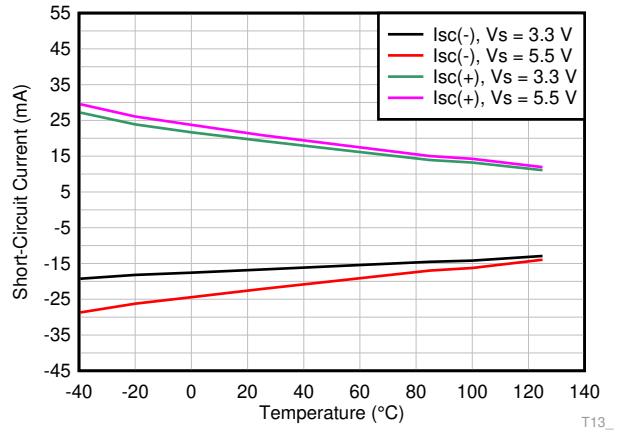


Figure 7-16. Short Circuit Current vs Temperature

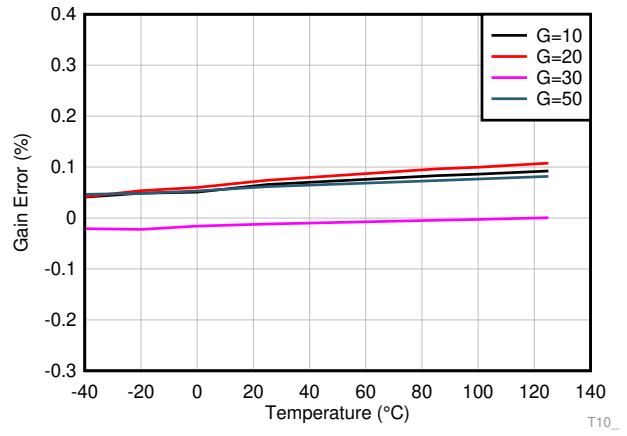


Figure 7-17. Gain Error vs Temperature

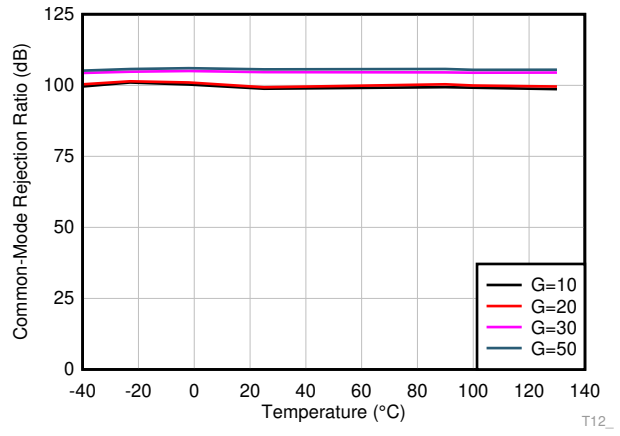
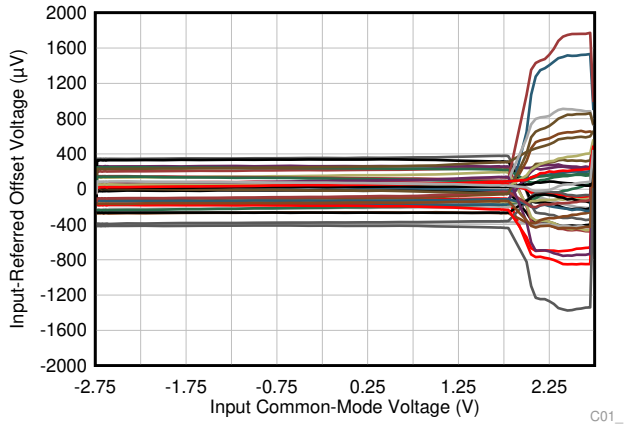


Figure 7-18. CMRR vs Temperature

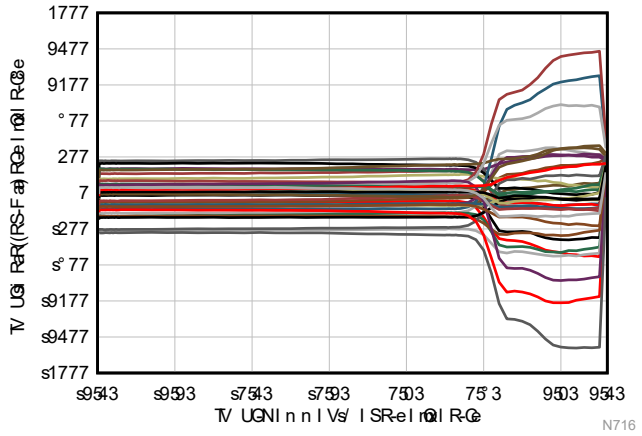
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



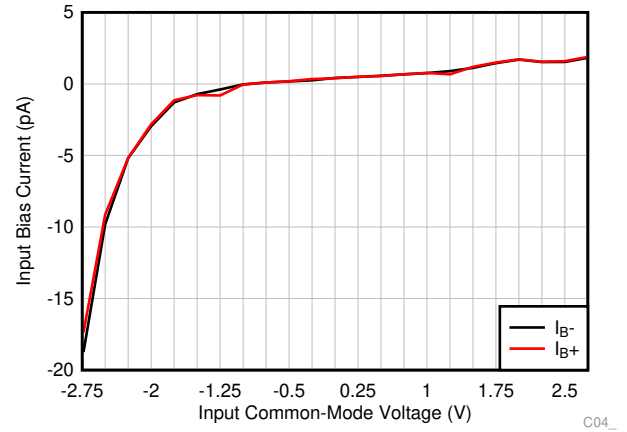
V+ = 2.75 V and V– = –2.75 V

Figure 7-19. Input Referred Offset Voltage vs Input Common-Mode Voltage



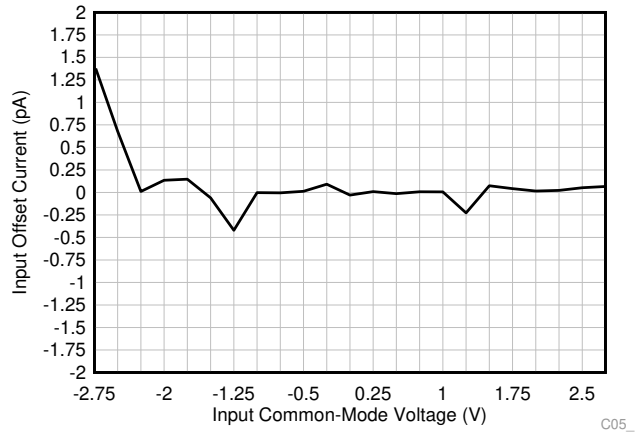
V+ = 1.65 V and V– = –1.65 V

Figure 7-20. Input Referred Offset Voltage vs Input Common-Mode Voltage



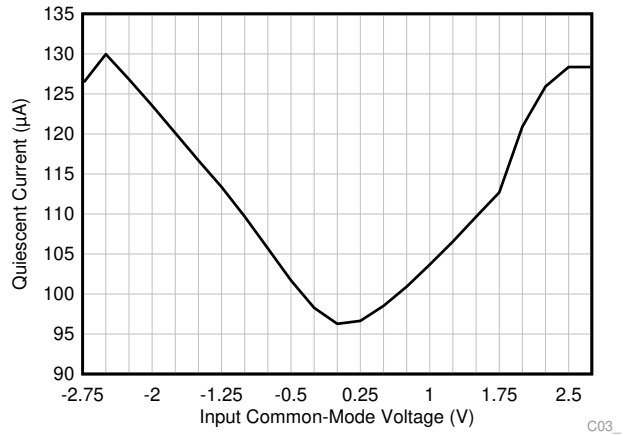
V+ = 2.75 V and V– = –2.75 V

Figure 7-21. Input Bias Current vs Input Common-Mode Voltage



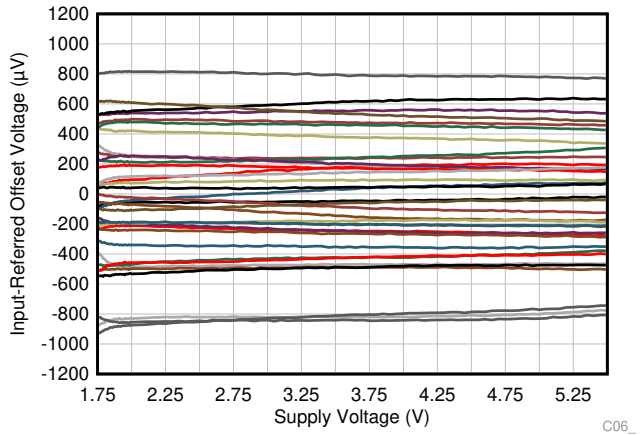
V+ = 2.75 V and V– = –2.75 V

Figure 7-22. Input Offset Current vs Input Common-Mode Voltage



V+ = 2.75 V and V– = –2.75 V

Figure 7-23. Quiescent Current vs Input Common-Mode Voltage



G = 10

Figure 7-24. Input Referred Offset Voltage vs Supply Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

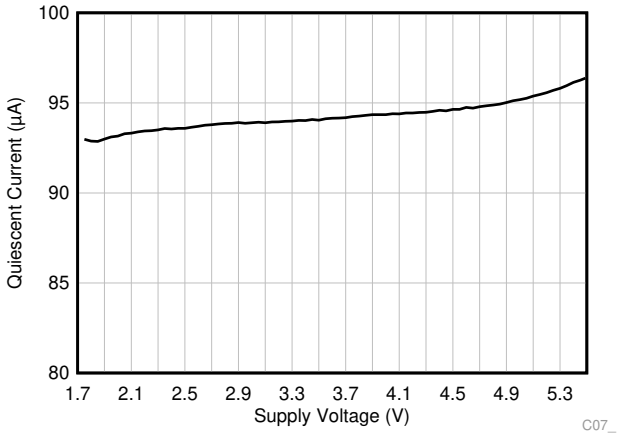


Figure 7-25. Quiescent Current vs Supply Voltage

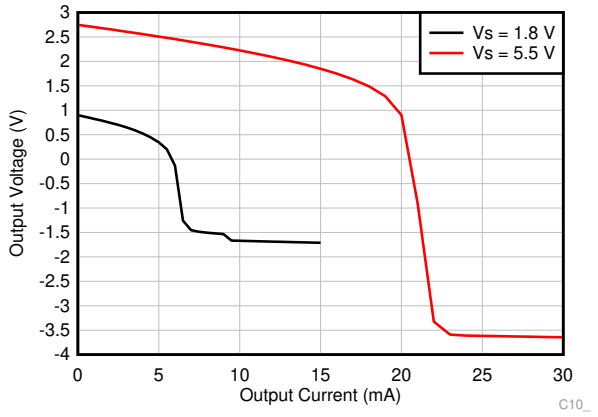


Figure 7-26. Output Voltage vs Output Current (Sourcing)

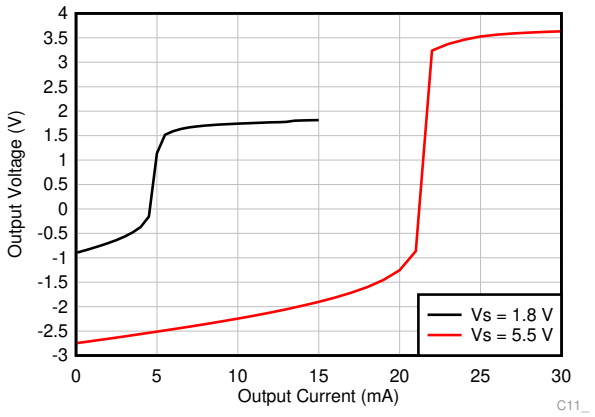


Figure 7-27. Output Voltage vs Output Current (Sinking)

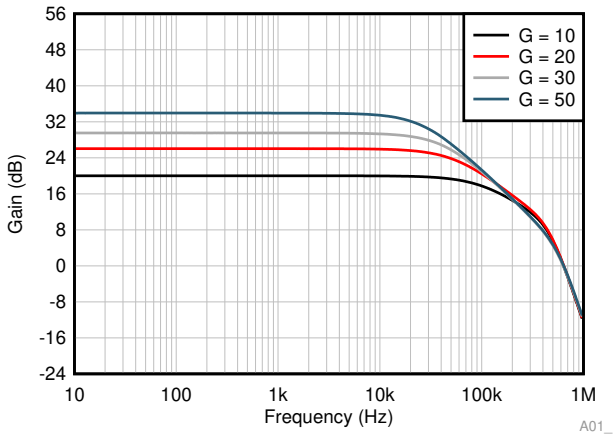


Figure 7-28. Closed-Loop Gain vs Frequency

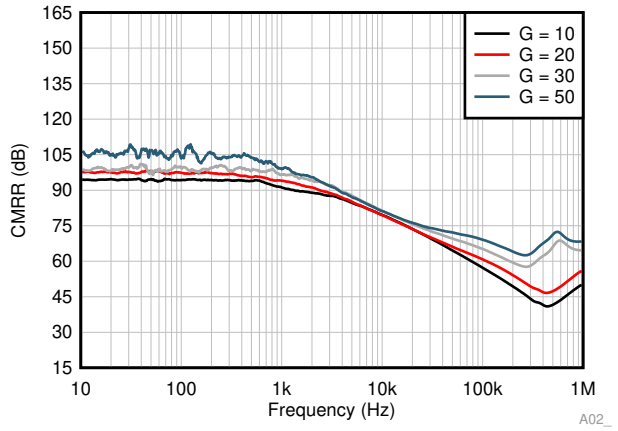


Figure 7-29. CMRR (Referred to Input) vs Frequency

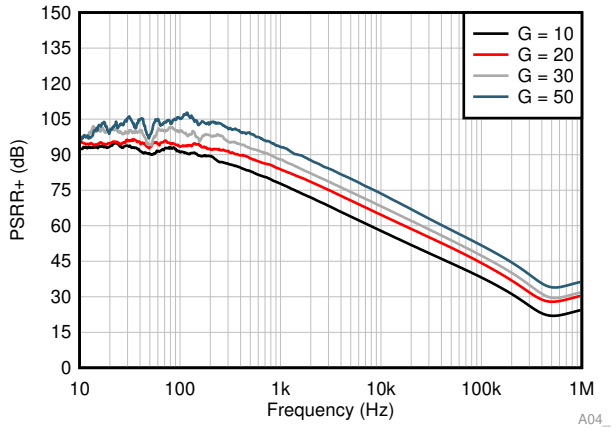


Figure 7-30. PSRR+ (Referred to Input) vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)

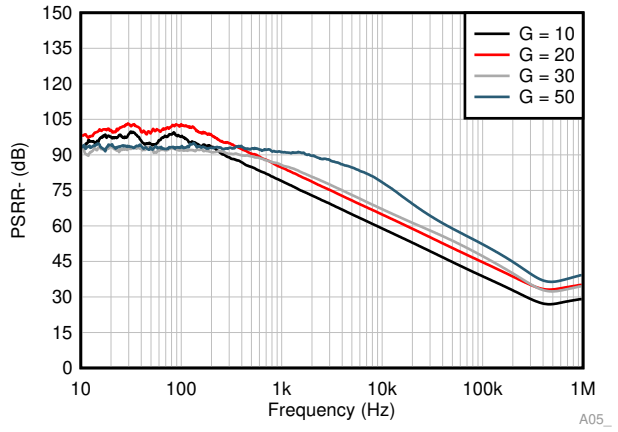


Figure 7-31. PSRR– (Referred to Input) Vs Frequency

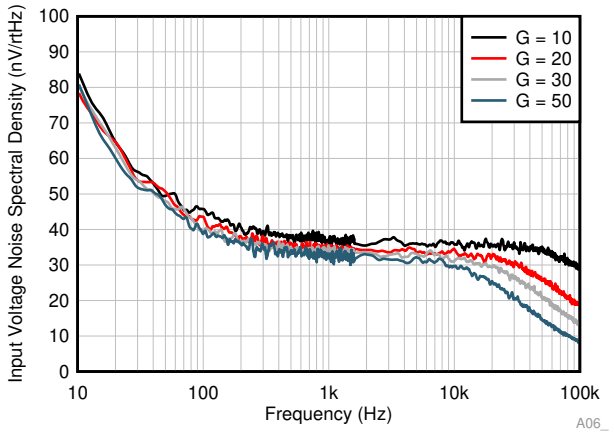


Figure 7-32. Input Referred Voltage Noise Spectral Density

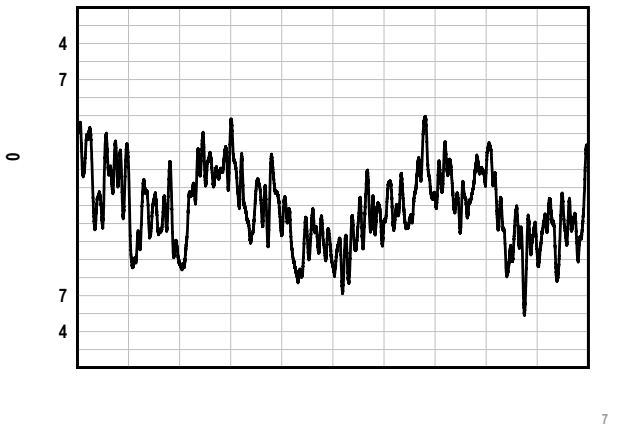


Figure 7-33. 0.1 Hz to 10 Hz Voltage Noise in Time Domain

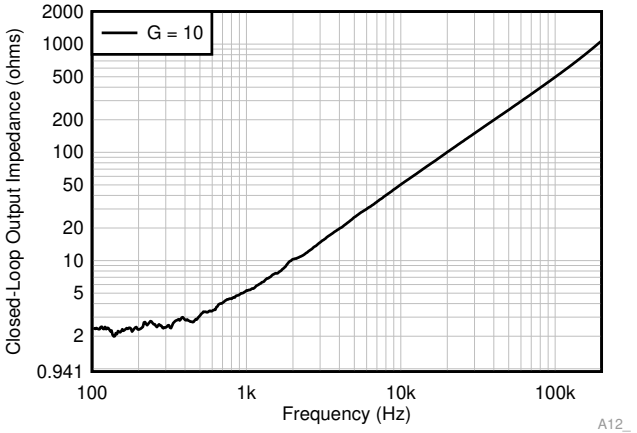


Figure 7-34. Closed-Loop Output Impedance vs Frequency

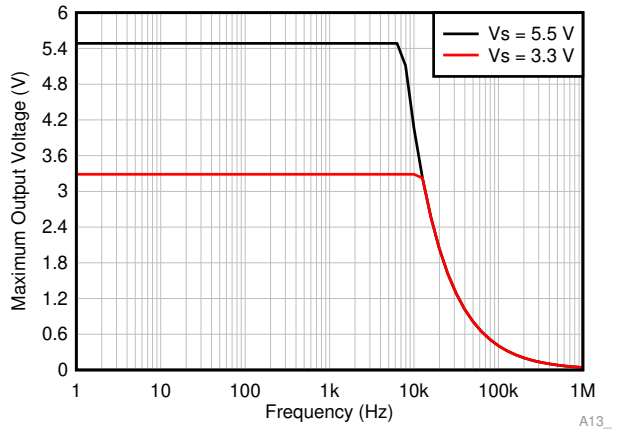
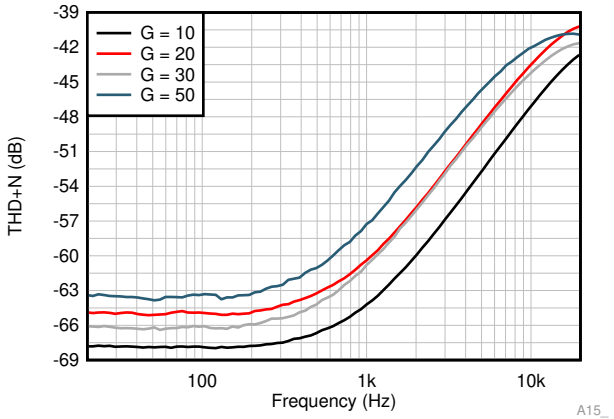


Figure 7-35. Maximum Output Voltage vs Frequency

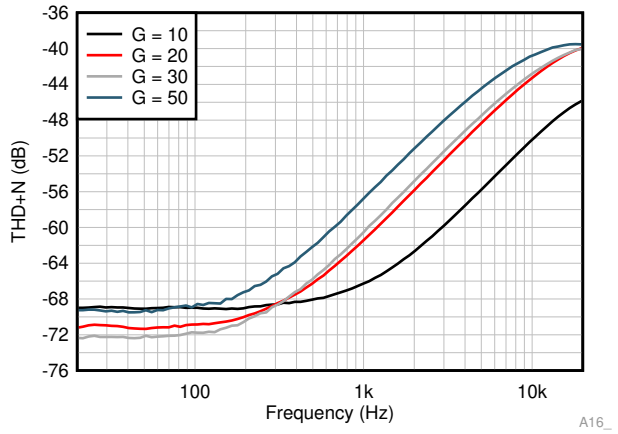


V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 10 kΩ V_{OUT} = 0.5 V_{RMS}

Figure 7-36. THD + N Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



V_S = 5.5 V BW = 80 kHz V_{CM} = 2.75 V
R_L = 100 kΩ V_{OUT} = 1 V_{RMS}

Figure 7-37. THD + N Frequency

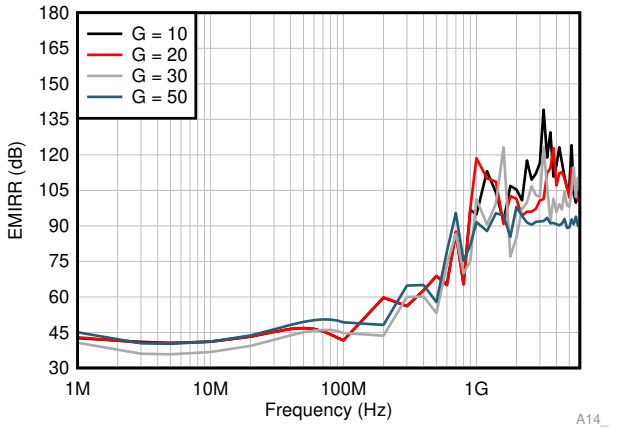
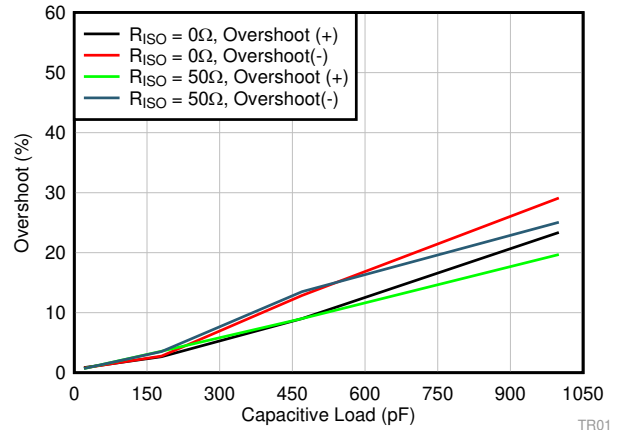
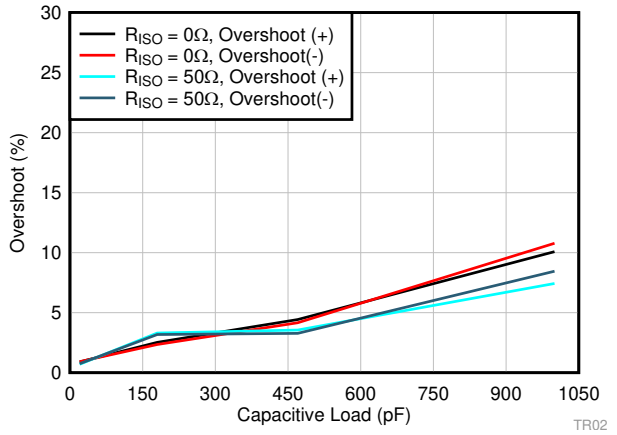


Figure 7-38. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



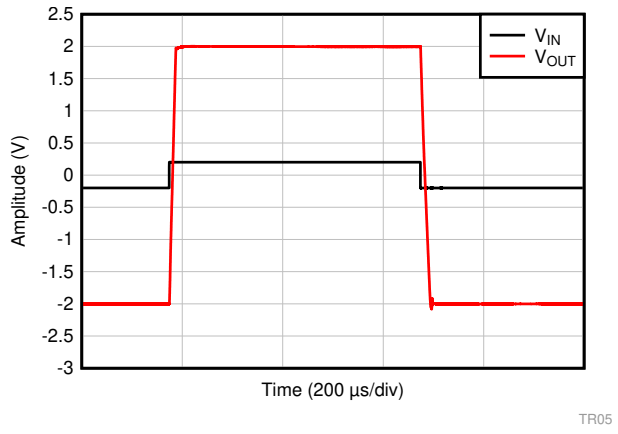
V_S = 5.5 V G = 10 V_{OUT} = 100 mV_{PP}

Figure 7-39. Small-Signal Overshoot vs Capacitive Load



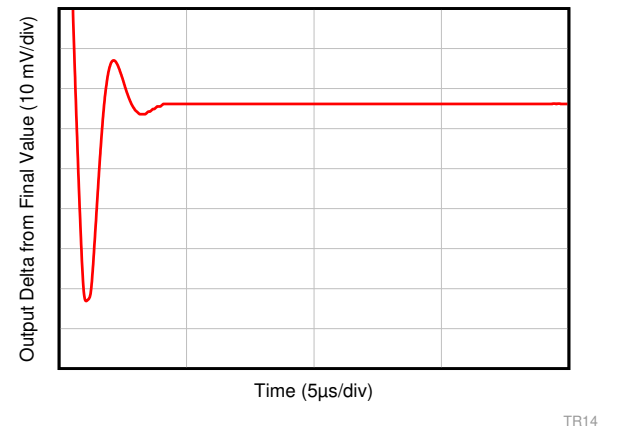
V_S = 5.5 V G = 20 V_{OUT} = 100 mV_{PP}

Figure 7-40. Small-Signal Overshoot vs Capacitive Load



V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 4 V_{PP}

Figure 7-41. Large Signal Step Response

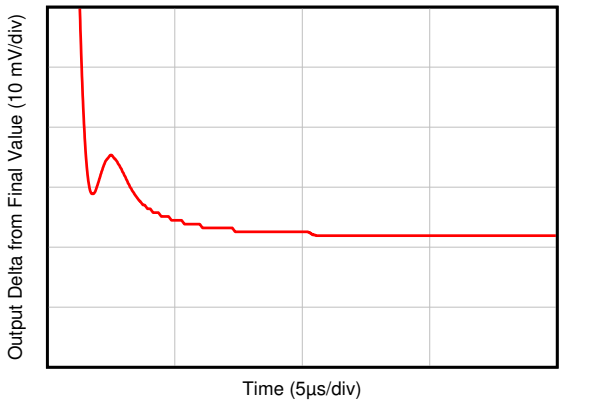


V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 4 V_{PP}

Figure 7-42. Large Signal Settling Time (Falling Edge)

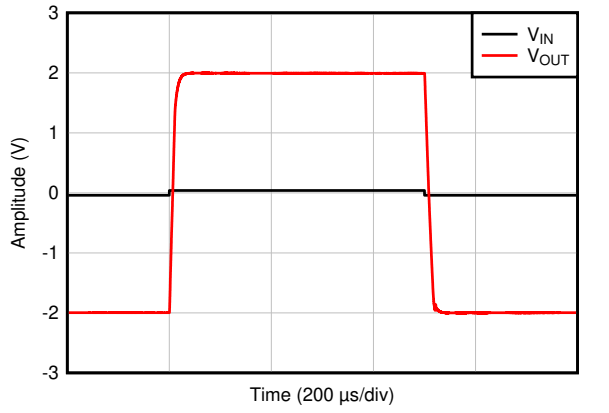
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



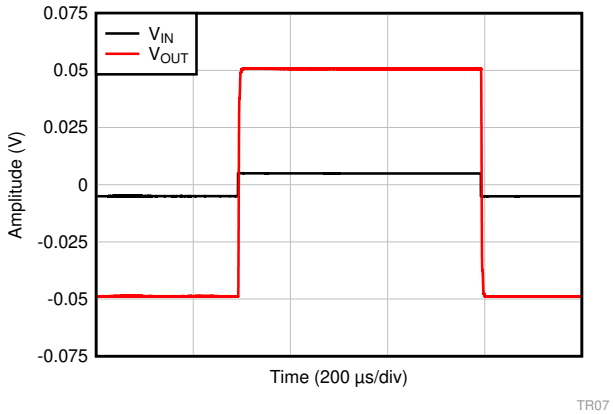
V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 4 V_{PP}

Figure 7-43. Large Signal Settling Time (Rising Edge)



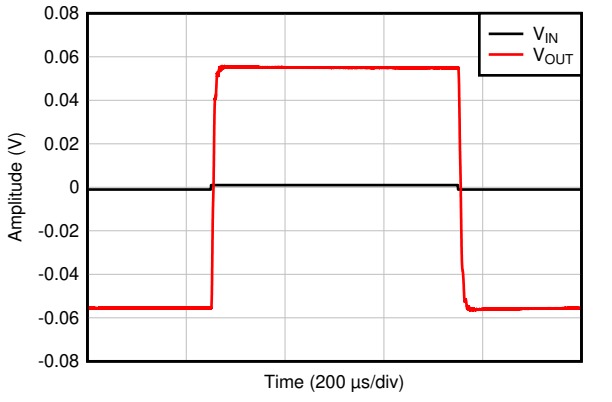
V+ = 2.75 V V– = –2.75 V G = 50 V_{OUT} = 4 V_{PP}

Figure 7-44. Large Signal Step Response



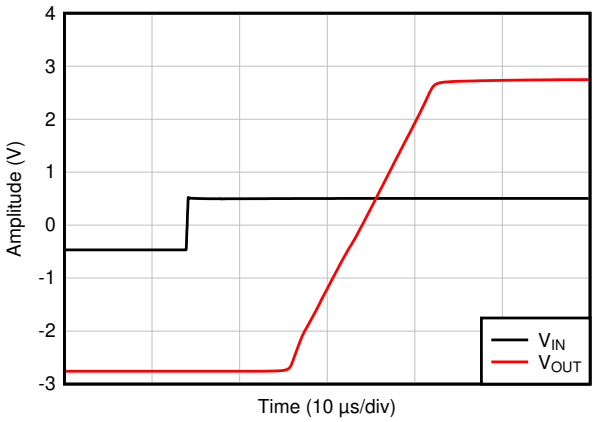
V+ = 2.75 V V– = –2.75 V G = 10 V_{OUT} = 0.1 V_{PP}

Figure 7-45. Small-Signal Step Response



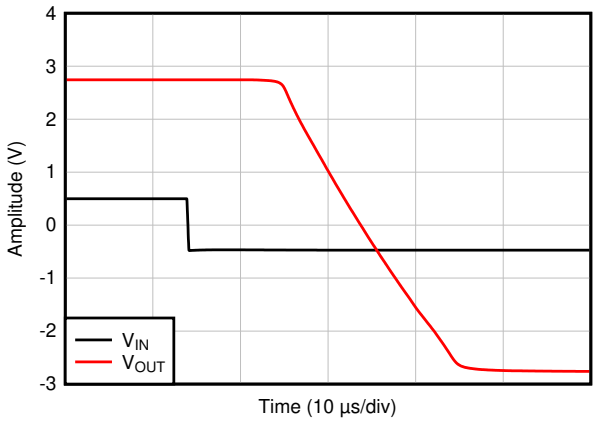
V+ = 2.75 V V– = –2.75 V G = 50 V_{OUT} = 0.1 V_{PP}

Figure 7-46. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 1 V_{PP}

Figure 7-47. Over-Load Recovery (Rising Edge)

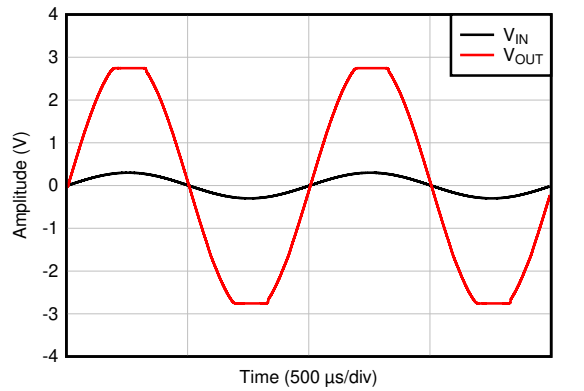


V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 1 V_{PP}

Figure 7-48. Over-Load Recovery (Falling Edge)

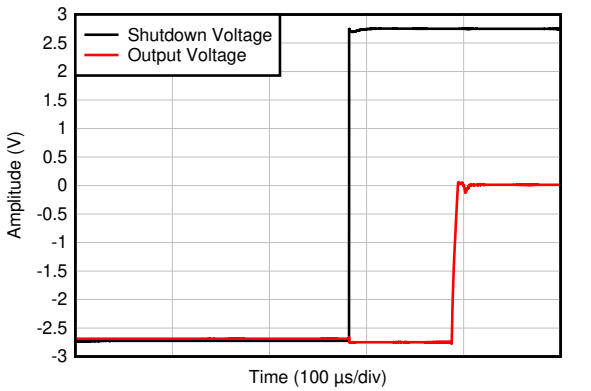
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



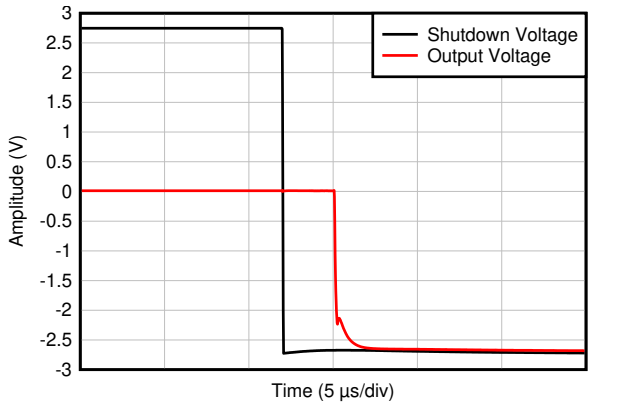
V+ = 2.75 V V– = –2.75 V G = 10 V_{IN} = 0.6 V_{PP}

Figure 7-49. No Phase Reversal



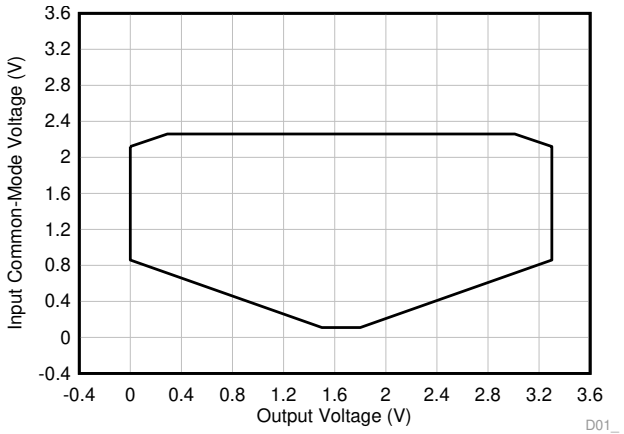
V+ = +2.75 V V– = –2.75 V G = 10

Figure 7-50. Enable Response



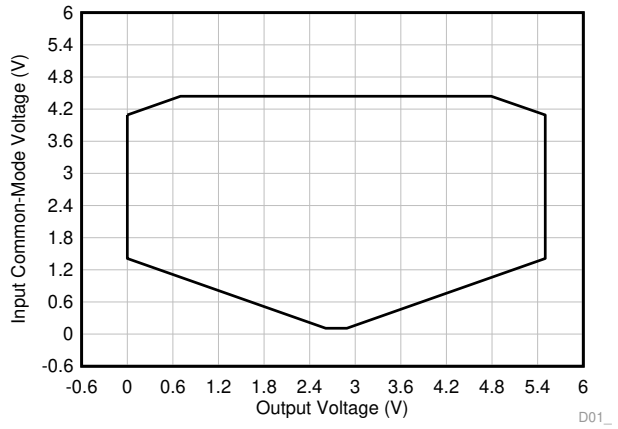
V+ = +2.75 V V– = –2.75 V G = 10

Figure 7-51. Disable Response



V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 7-52. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

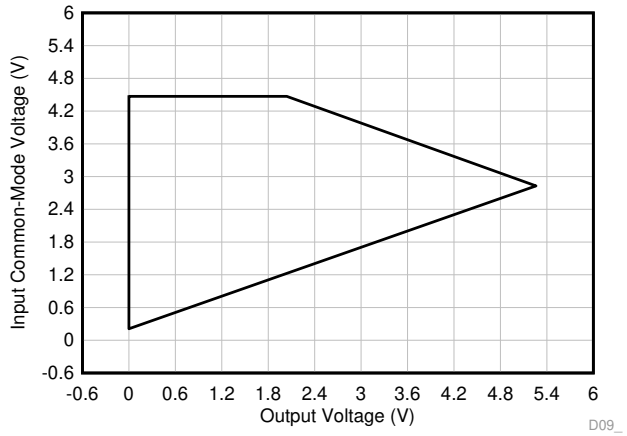
Figure 7-53. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 7-54. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

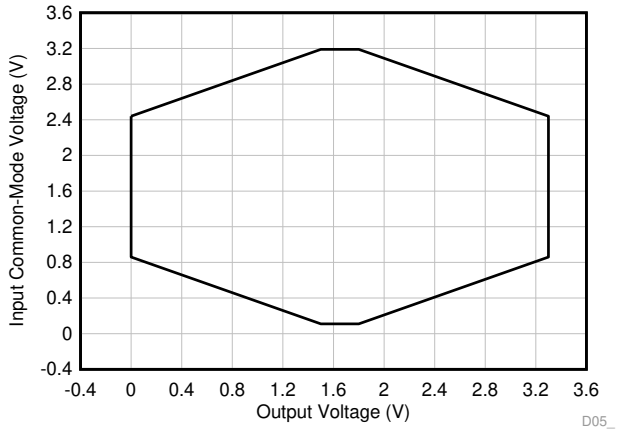
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5 V, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0 V, R_L = 10 kΩ, C_L = 10 pF, V_{REF} = V_S / 2, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 10 (unless otherwise noted)



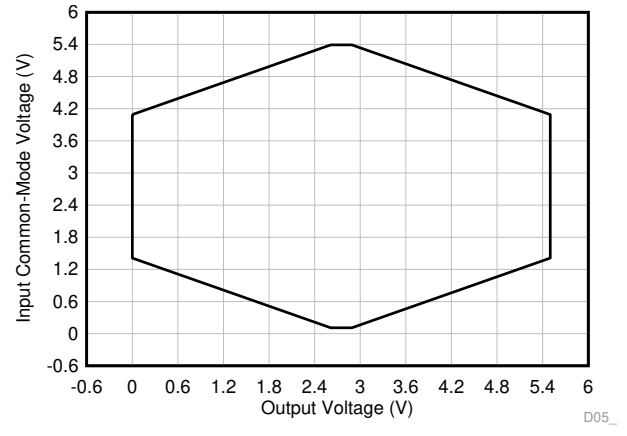
V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 7-55. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



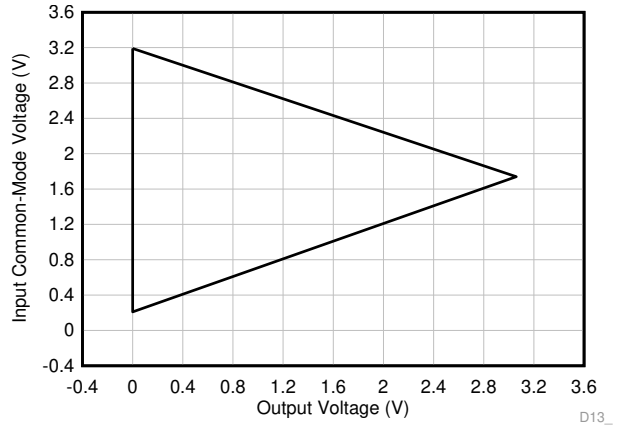
V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 7-56. Input Common-Mode Voltage vs Output Voltage



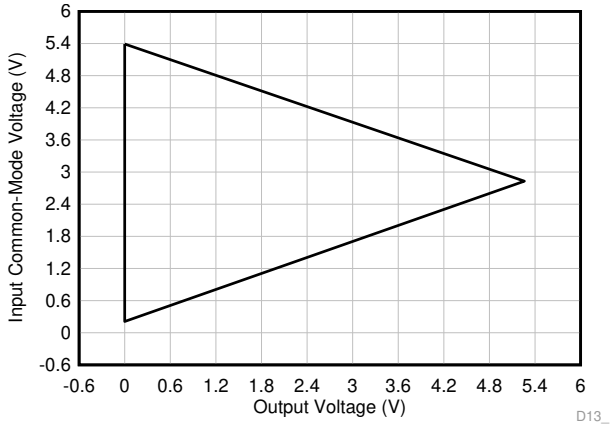
V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = V_S / 2

Figure 7-57. Input Common-Mode Voltage vs Output Voltage



V_S = 3.3 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 7-58. Input Common-Mode Voltage vs Output Voltage



V_S = 5.5 V G = 10, 20, 30, 50 V_{REF} = 0 V

Figure 7-59. Input Common-Mode Voltage vs Output Voltage

8 Detailed Description

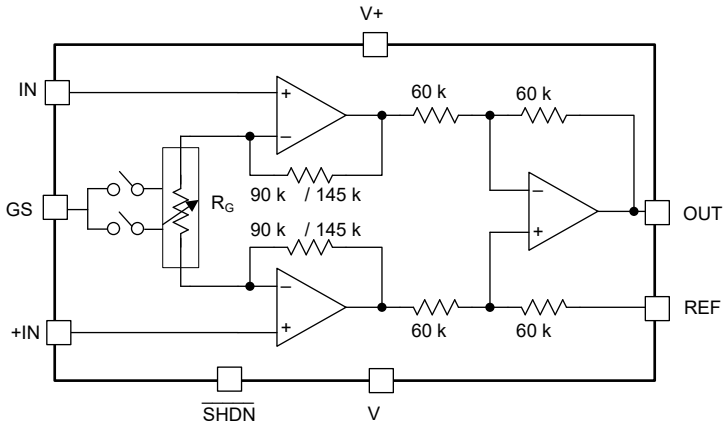
8.1 Overview

INA350 is a selectable gain instrumentation amplifier mainly targeted to provide an integrated small size, cost effective solution for applications employing general purpose INAs or discrete implementation of INAs using commodity amplifiers and resistors. It incorporates a three op amp INA architecture integrating three operational amplifiers and seven precision matched integrated resistors. It is mainly targeted for use in 10-bit to 14-bit systems, but calibrating offset and gain error at a system level can further improve system resolution and accuracy enabling use in precision applications.

One of the key features of INA350 is that it does not need any external resistors to set the gain. Often these external resistors warrant tighter tolerance and need to be routed carefully which adds to the system complexity and cost. INA350 is offered in four gain options across two variants. INA350ABS has two gain options of 10 and 20. INA350CDS has two other gain options of 30 and 50. Gains can be selected by connecting the GS pin to logic high or logic low. Note that the GS pin can be left floating as well, as it is designed with an internal pull up to default to the same configuration as GS tied logic high.

The INA350 is developed for industrial applications in factory automation and appliances sector where pressure sensing and temperature sensing are done using bridge-type sensor networks and load cells. It can also be used in tight spaces in medical applications such as patient monitoring, sleep diagnostics, electronic hospital beds, blood glucose monitoring, and so forth for voltage sensing and differential to single-ended conversion. INA350 can enable these applications to reduce their overall size through the use of tiny packages, including a 2-mm × 1.5-mm X2QFN package and a 2-mm × 2-mm WSON package.

8.2 Functional Block Diagram



Note: 90 kΩ for INA350ABS and 145 kΩ for INA350CDS

Simplified Internal Schematic

8.3 Feature Description

8.3.1 Gain-Setting

The gain equation of INA350ABS can be given by Equation 1:

$$G = 1 + \frac{180\ k\Omega}{R_G} \quad (1)$$

The value of the internal gain resistor R_G for INA350ABS can then be derived from the gain equation:

$$R_G = \frac{180\ k\Omega}{G - 1} \quad (2)$$

Similarly The gain equation of INA350CDS can be given by Equation 1:

$$G = 1 + \frac{290\ k\Omega}{R_G} \quad (3)$$

The value of the internal gain resistor R_G for INA350CDS can then be derived from the gain equation:

$$R_G = \frac{290\ k\Omega}{G - 1} \quad (4)$$

Gain selection table below outlines how to choose different gain options across INA350ABS and INA350CDS. The 60-kΩ, 90-kΩ, and 145-kΩ resistors mentioned are all typical values of the on-chip resistors.

Table 8-1. Gain Selection Table

DEVICE	GAIN SELECT (GS)	SELECTED GAIN
INA350ABS	High or No Connect	20
	Low	10
INA350CDS	High or No Connect	50
	Low	30

8.3.1.1 Gain Error and Drift

Gain error in INA350 is limited by the mismatch of the integrated precision resistors and it is specified based on characterization results. Gain error of maximum 0.5% can be expected for the gains of 10 and 0.6% for the gains of 20, 30 and 50. Gain drift in INA350 is limited by the slight mismatch of the temperature coefficient of the integrated resistors. Since these integrated resistors are precision matched with low temperature coefficient resistors to begin with, the overall gain drift would be much better in comparison to discrete implementation of the instrumentation amplifiers built using external resistors.

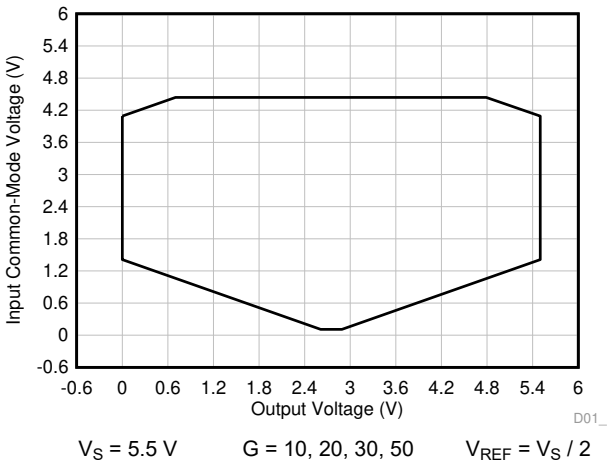
8.3.2 Input Common-Mode Voltage Range

INA350 has two gain stages, the first stage has a common-mode gain of 1 and a differential gain set by the GS pin. The second stage is configured in a difference-amplifier configuration with differential gain of 1 and ideally rejects all of the input common mode completely. The second stage also provides a gain of 1 from REF pin to set the output common-mode voltage.

The linear input voltage range of the INA350, even for a rail-to-rail first stage is dictated by the signal swing at output of the first stage as well as the input common-mode voltage range output swing of the second stage. It is imperative that the INA350 stays linear for a particular combination of gain, reference, and input common-mode voltage for a chosen input differential. Input common-mode voltage (V_{CM}) vs output voltage graphs (V_{OUT}) in this section show a particular reference voltage and gain configuration to outline the linear performance region of INA350. A good common-mode rejection can be expected when operating with in the limits of the V_{CM} vs V_{OUT} graph. Note, that the INA350 linear input voltage cannot be close to or extend beyond the supply rails as the output of the first stage will be driven into saturation.

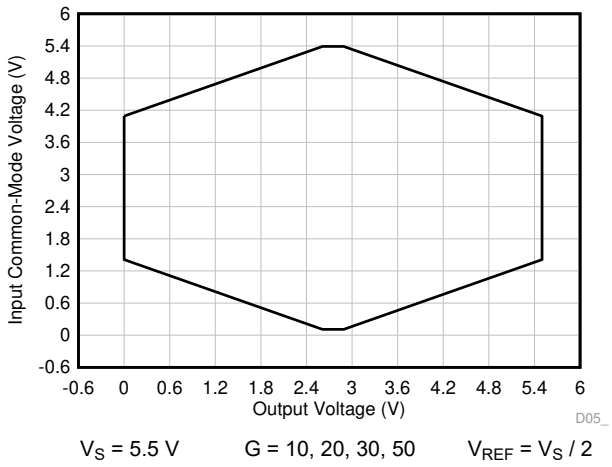
The common-mode range for the most common operating conditions is outlined below. Figure 8-1 shows the region of operation where a minimum of 85 dB can be achieved. Figure 8-2 has much wider region of operation

with a lower minimum CMRR of 62 dB, because the input signal crosses over the transition region of the input pairs to achieve rail-to-rail operation. The common-mode range for other operating conditions is best calculated with the INA V_{CM} vs V_{OUT} tool located under the *Amplifiers and Comparators* section of the Analog Engineer's Calculator on ti.com. INA350-HCM model can be specifically used for applications requiring high CMRR and corresponds to performance shown in Figure 8-1. INA350xxS model can be used for applications where the input common mode can be expected to vary rail-to-rail and it corresponds to performance shown in Figure 8-2 where CMRR drops to 62-dB minimum.



V_S = 5.5 V G = 10, 20, 30, 50 $V_{REF} = V_S / 2$

Figure 8-1. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V_S = 5.5 V G = 10, 20, 30, 50 $V_{REF} = V_S / 2$

Figure 8-2. Input Common-Mode Voltage vs Output Voltage

8.3.3 EMI Rejection

The INA350 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the INA350 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-3 shows the results of this testing on the INA350. Table 8-2 shows the EMIRR IN+ values for the INA350 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

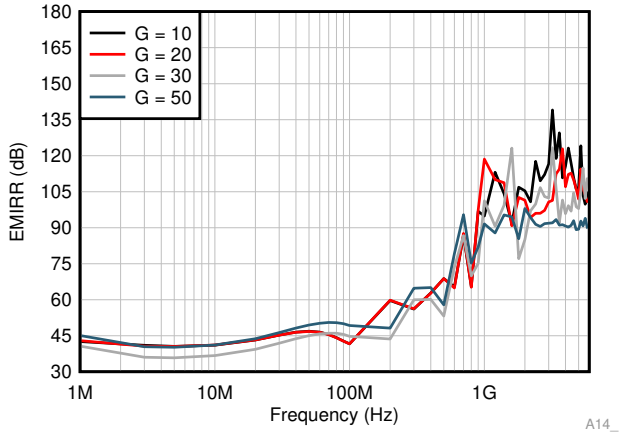


Figure 8-3. EMIRR Testing

Table 8-2. INA350 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	60 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	92 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	90 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	95 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	108 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105 dB

8.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

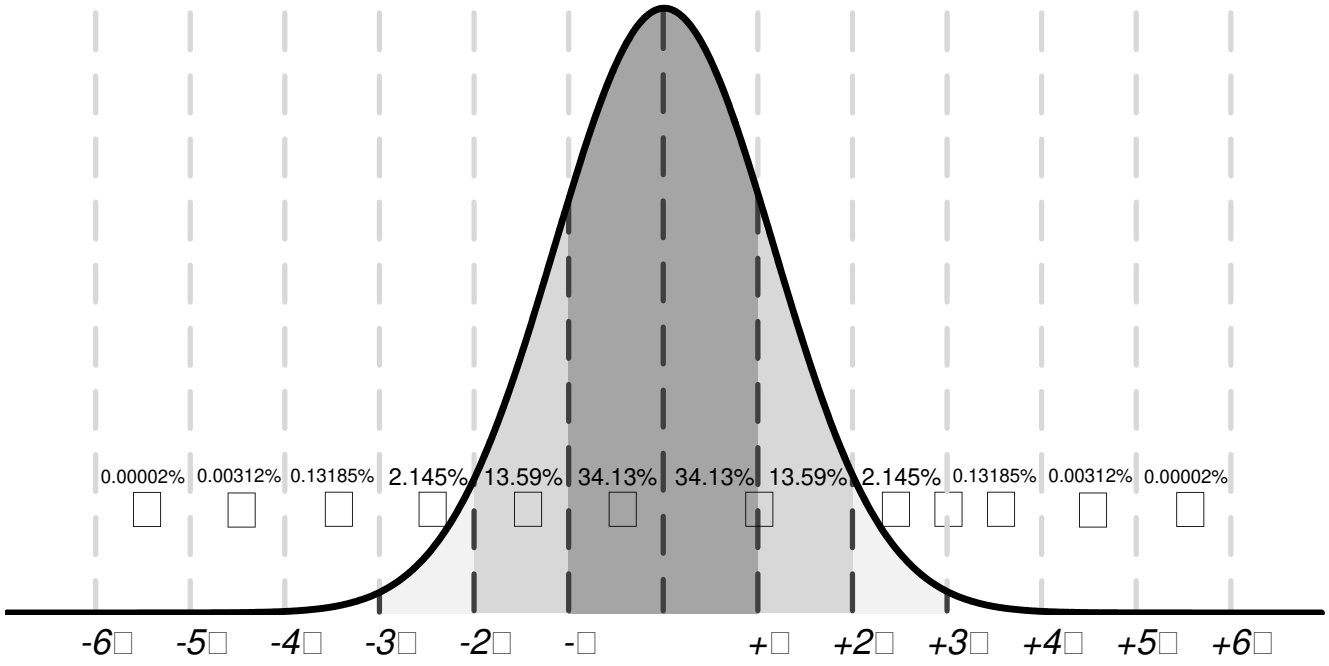


Figure 8-4. Ideal Gaussian Distribution

Figure 8-4 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, the INA350 typical input voltage offset is 200 µV, so 68.2% of all INA350 devices are expected to have an offset from –200 µV to +200 µV. At 4 σ (±800 µV), 99.9937% of the distribution has an offset voltage less than ±800 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the INA350 family has a maximum offset voltage of 1.2 mV at 25°C, and even though this corresponds to 6 σ (≈1 in 500 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1.2 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for your application, and design worst-case conditions using this value. As stated earlier, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guard band to design a system around. In this case, the INA350 family does not have a maximum or minimum for offset voltage drift, but based on Figure 7-2 and the typical value of 0.6 µV/°C in the *Electrical Characteristics* table, it can be calculated from that the 6-σ value for offset voltage drift is about 2 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset drift without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-5 shows the ESD circuits contained in the INA350 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

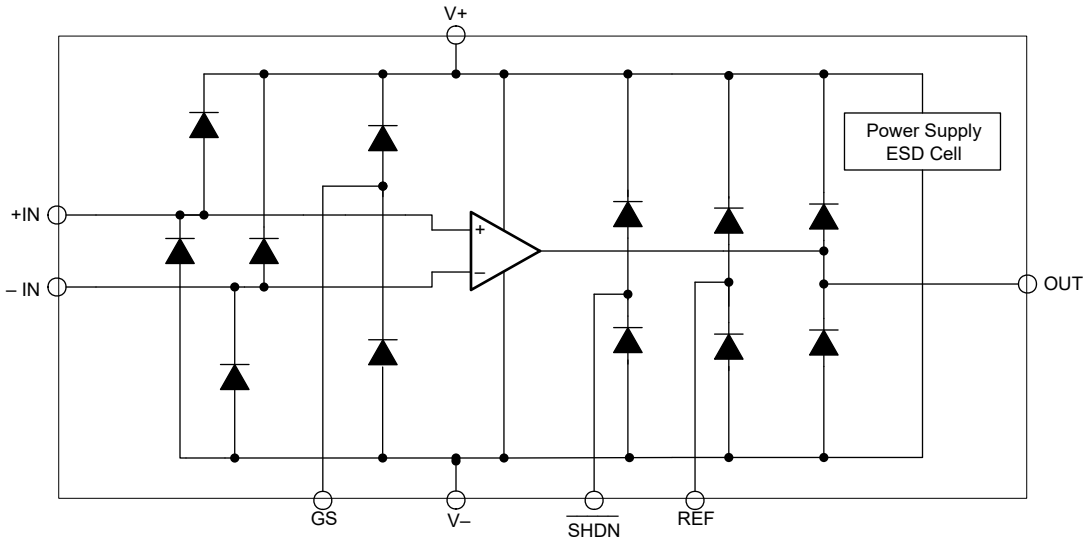


Figure 8-5. Equivalent Internal ESD Circuitry

8.4 Device Functional Modes

The INA350 has a shutdown or disable mode to enable power savings in battery powered applications. The shutdown mode has a maximum quiescent current of just 1.25 µA, which is 100 times lower from the quiescent current when the amplifier is powered-on or enabled.

INA350 enters disable mode when the $\overline{\text{SHDN}}$ pin is tied low. INA350 is enabled when the $\overline{\text{SHDN}}$ pin is tied high. A no connection or a floating $\overline{\text{SHDN}}$ pin enables or powers-on the INA as the pin has an internal pull up current to default to the same configuration as $\overline{\text{SHDN}}$ pin tied high.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA350 is developed with respect to the voltage on the reference pin (REF). Often in dual-supply operation, REF pin connects to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level is useful (for example, 2.75-V in a 5.5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA350 can drive a single-supply ADC.

The voltage source applied to the reference pin must have a low output impedance. Any resistance at the reference pin (R_{REF}) in is in series with the internal 60-kΩ resistor.

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier that results in a degraded common-mode rejection ratio (CMRR). For the best performance, keep the source impedance to the REF pin (R_{REF}) less than 5 Ω.

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, buffer the divider by an op amp, as shown in Figure 9-1, to avoid CMRR degradation.

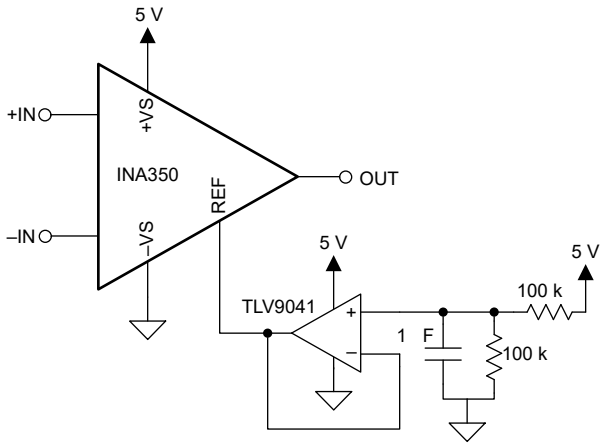


Figure 9-1. Use an Op Amp to Buffer Reference Voltages

9.1.2 Input Bias Current Return Path

The input impedance of the INA350 is extremely high, but a path must be provided for the input bias current of both inputs. This input bias current is typically a few pico amps but at high temperature this can be a few nano amps. High input impedance means that the input bias current changes little with varying input voltage.

For proper operation, input circuitry must provide a path for this input bias current. Figure 9-2 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA350, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in Figure 9-2). With a higher source impedance, use two equal resistors to provide a balanced input, with the possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.

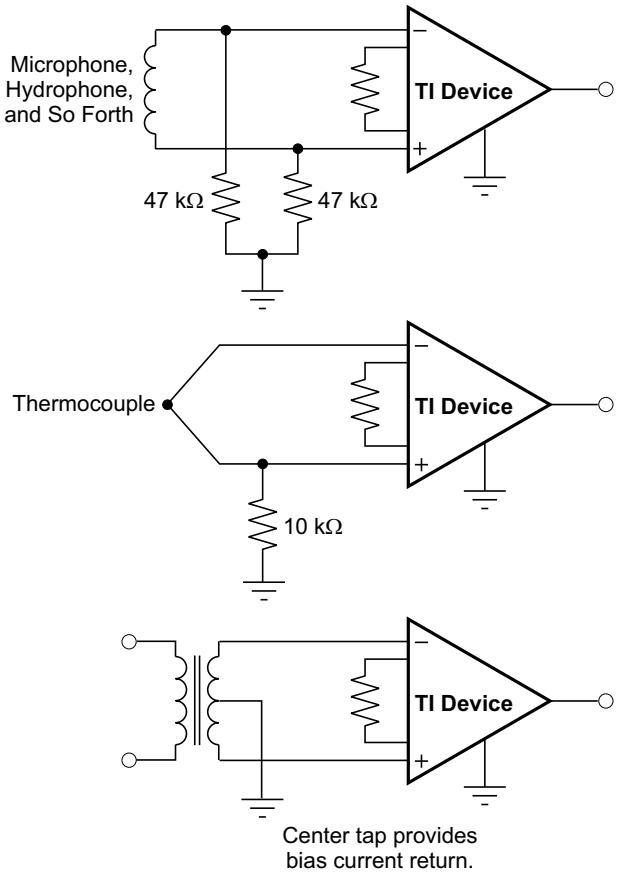


Figure 9-2. Providing an Input Common-Mode Current Path

9.2 Typical Applications

9.2.1 Resistive-Bridge Pressure Sensor

The INA350 is an integrated instrumentation amplifier that measures small differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 100 µA (typical) and has a smaller form factor.

The device is designed for portable applications where sensors measure physical parameters, such as changes in fluid, pressure, temperature, or humidity. An example of a pressure sensor used in the medical sector is in portable infusion pumps or dialysis machines.

The pressure sensor is made of a piezo-resistive element that can be derived as a classical 4-resistor Wheatstone bridge.

Occlusion (infusion of fluids, medication, or nutrients) happens only in one direction, and therefore can only cause the resistive element (R) to expand. This expansion causes a change in voltage on one leg of the Wheatstone bridge, which induces a differential voltage V_{DIFF}.

Figure 9-3 showcases an example circuit for an occlusion pressure sensor application, as required in infusion pumps. When blockage (occlusion) occurs against a set-point value, the tubing depresses, thus causing the piezo-resistive element to expand (Node AD: R + ΔR). The signal chain connected to the bridge downstream processes the pressure change and can trigger an alarm.

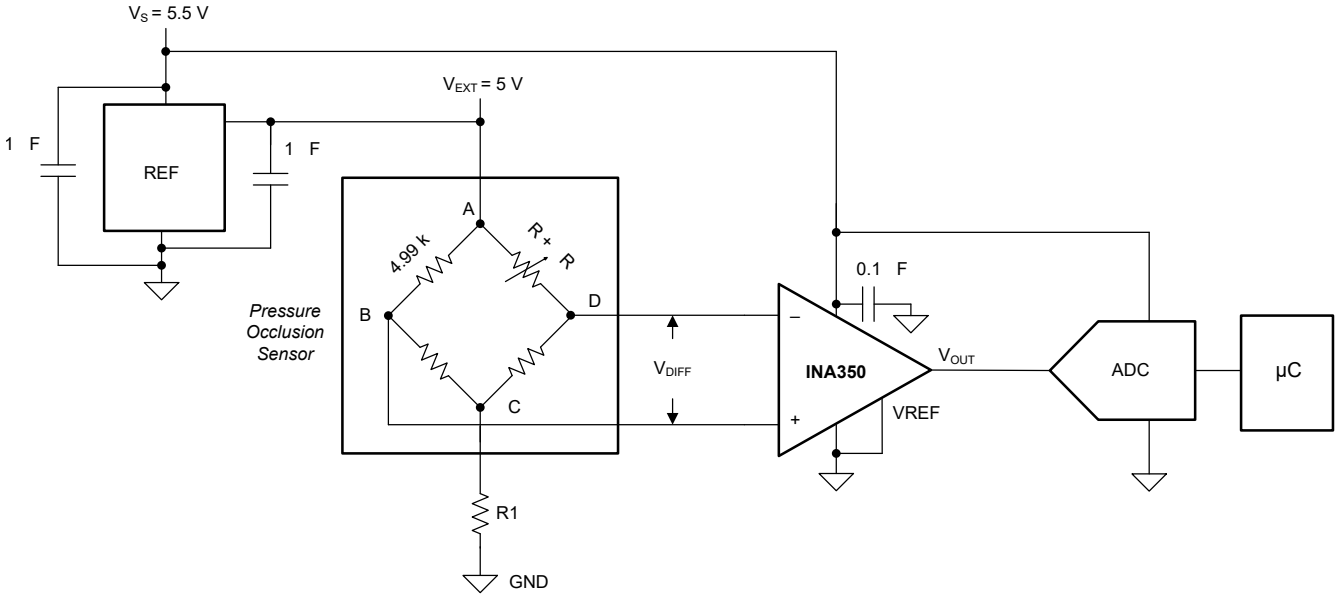


Figure 9-3. Resistive-Bridge Pressure Sensor

Low-tolerance bridge resistors must be used to minimize the offset and gain errors.

Given that there is only a positive differential voltage applied, this circuit is laid out in single-ended supply mode. The excitation voltage, V_{EXT}, to the bridge must be precise and stable; otherwise, measurement errors can be introduced.

9.2.1.1 Design Requirements

For this application, the design requirements are as shown in Table 9-1.

Table 9-1. Design Requirements

DESCRIPTION	VALUE
Single supply voltage	V_S = 5.5 V
Excitation voltage	V_{EXT} = 5.0 V
Occlusion pressure range	P = 1 psi to 12 psi, increments of P = 0.5 psi
Occlusion pressure sensitivity	S = 2 ±0.5 (25%) mV/V/psi
Occlusion pressure impedance (R)	R = 4.99 kΩ ±50 Ω (0.1%)
Total pressure sampling rate	Sr = 20 Hz
Full-scale range of ADC	$V_{ADC(fs)}$ = V_{OUT} = 3.0 V

9.2.1.2 Detailed Design Procedure

This section provides basic calculations to lay out the instrumentation amplifier with respect to the given design requirements.

One of the key considerations in resistive-bridge sensors is the common-mode voltage, V_{CM}. If the bridge is balanced (no pressure, thus no voltage change), $V_{CM(zero)}$ is half of the bridge excitation (V_{EXT}). In this example $V_{CM\ (zero)}$ is 2.5 V. For the maximum pressure of 12 psi, the bridge common-mode voltage, $V_{CM(MAX)}$, is calculated by:

$$V_{CM(MAX)} = \frac{V_{DIFF}}{2} + V_{CM(zero)} \tag{5}$$

where

- $$V_{DIFF} = S_{MAX} \times V_{EXT} \times P_{MAX} = 2.5\frac{mV}{V \times psi} \times 5\ V \times 12\ psi = 150\ mV \tag{6}$$

Thus, the maximum common-mode voltage applied results in:

$$V_{CM(MAX)} = \frac{150\ mV}{2} + 2.5\ V = 2.575\ V \tag{7}$$

Similarly, the minimum common-mode voltage can be calculated as,

$$V_{CM(MIN)} = \frac{-150\ mV}{2} + 2.5\ V = 2.425\ V \tag{8}$$

The next step is to calculate the gain required for the given maximum sensor output voltage span, V_{DIFF}, in respect to the required V_{OUT}, which is the full-scale range of the ADC.

The following equation calculates the gain value using the maximum input voltage and the required output voltage:

$$G = \frac{V_{OUT}}{V_{DIFF(MAX)}} = \frac{3.0\ V}{150\ mV} = 20\ V/V \tag{9}$$

Considering, INA350 is a selectable gain INA with gain options of 10, 20, 30, 50, the INA350ABS with GS tied high enables G = 20 ensuring the maximum output signal swing for the ADC.

Next, let us make sure that the INA350 can operate within this range checking the *Input Common-Mode Voltage vs Output Voltage* curves in the *Typical Characteristics* section. The relevant figure is also in this section for convenience. Looking at Figure 9-4, we can confirm that a output signal swing of 3 V is supported for the input signal swing between 2.425 V and 2.575 V, thus making sure of the linear operation.

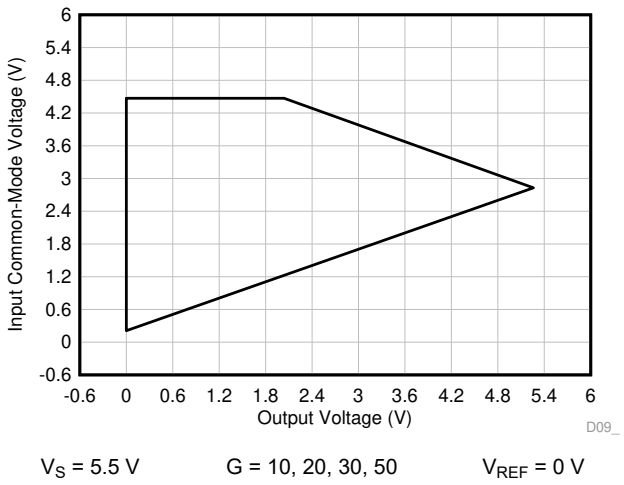


Figure 9-4. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

Additional series resistor in the Wheatstone bridge string (R1) may or may not be required. This is decided based on the intended output voltage swing for a particular combination of supply voltage, reference voltage and the selected gain for an input common mode voltage range. R1 helps adjust the input common-mode voltage range, and thus can help accommodate the intended output voltage swing. In this particular example, it are not required and can be shorted out.

9.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in Figure 9-3.

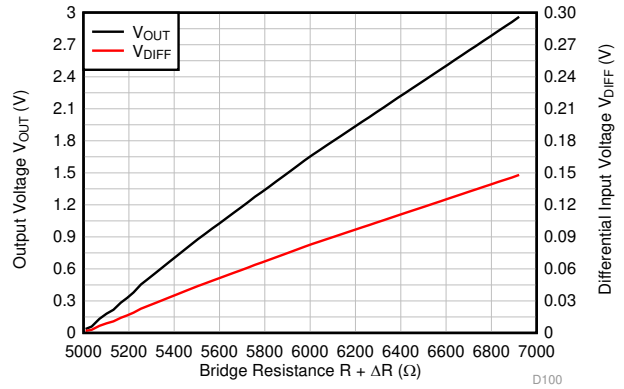


Figure 9-5. Input Differential Voltage, Output Voltage vs Bridge Resistance

10 Power Supply Recommendations

The nominal performance of the INA350 is specified with a supply voltage of ±2.75 V and midsupply reference voltage. The device also operates using power supplies from ±0.85 V (1.7 V) to ±2.75 V (5.5 V) and non-midsupply reference voltages with excellent performance. Parameters can vary significantly with operating voltage and reference voltage.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

11.2 Layout Example

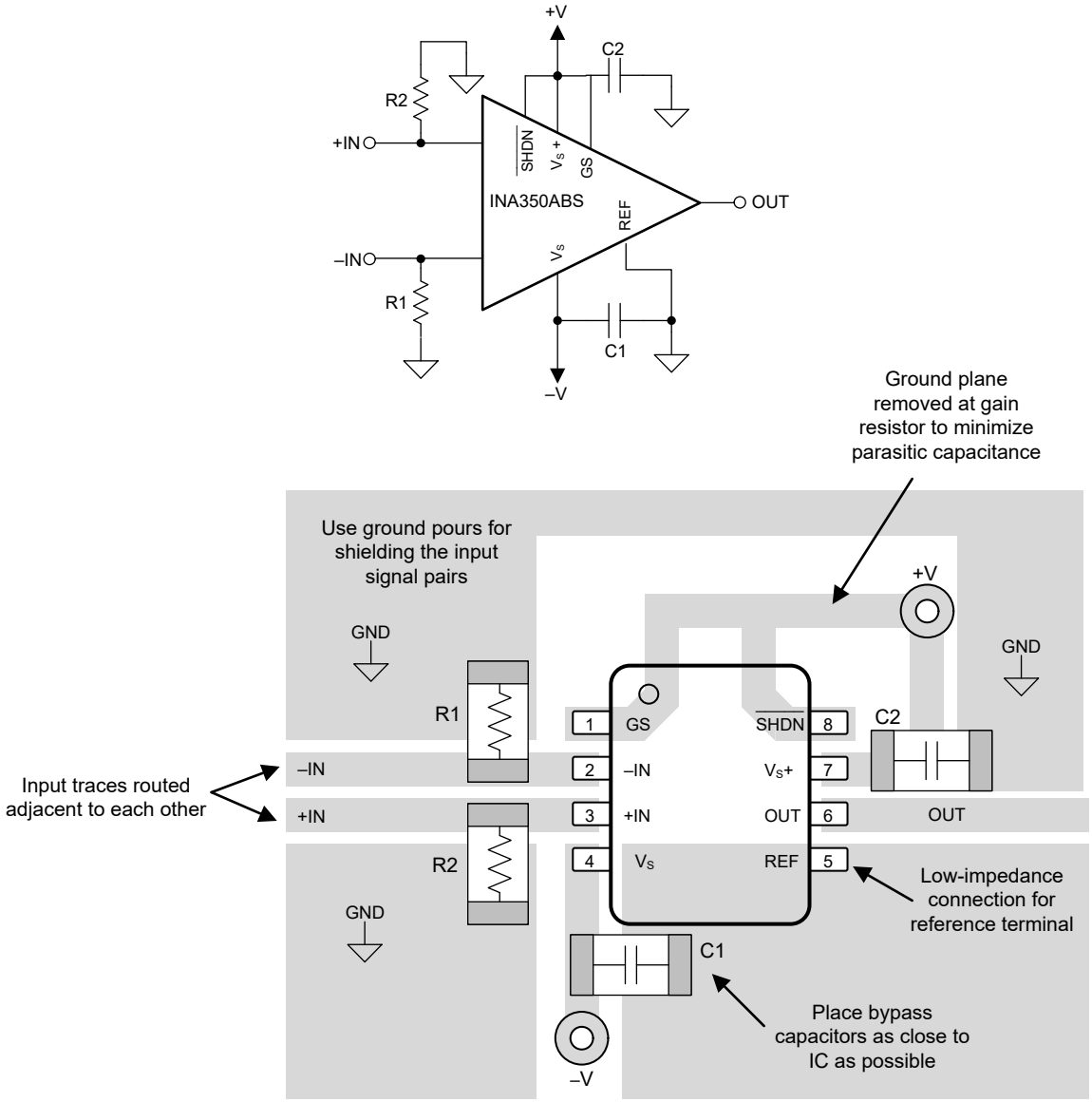


Figure 11-1. Example Schematic and Associated PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineers Calculator*

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA350ABSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN35A	Samples
INA350ABSIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I35A	Samples
INA350CDSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IN35C	Samples
INA350CDSIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I35C	Samples
PINA350ABSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PINA350ABSIDSGR	ACTIVE	WSON	DSG	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PINA350CDSIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PINA350CDSIDSGR	ACTIVE	WSON	DSG	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

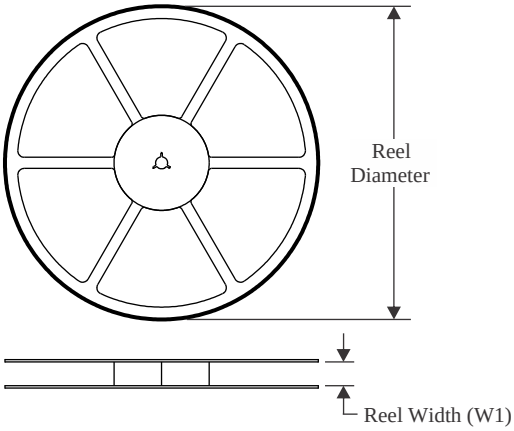
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

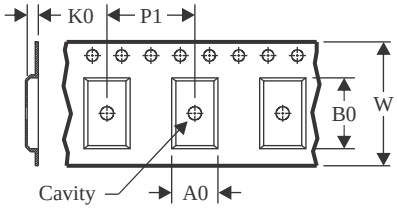
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

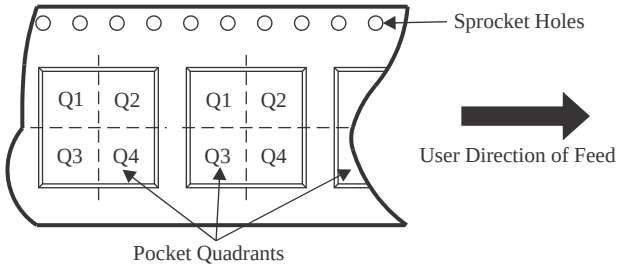


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

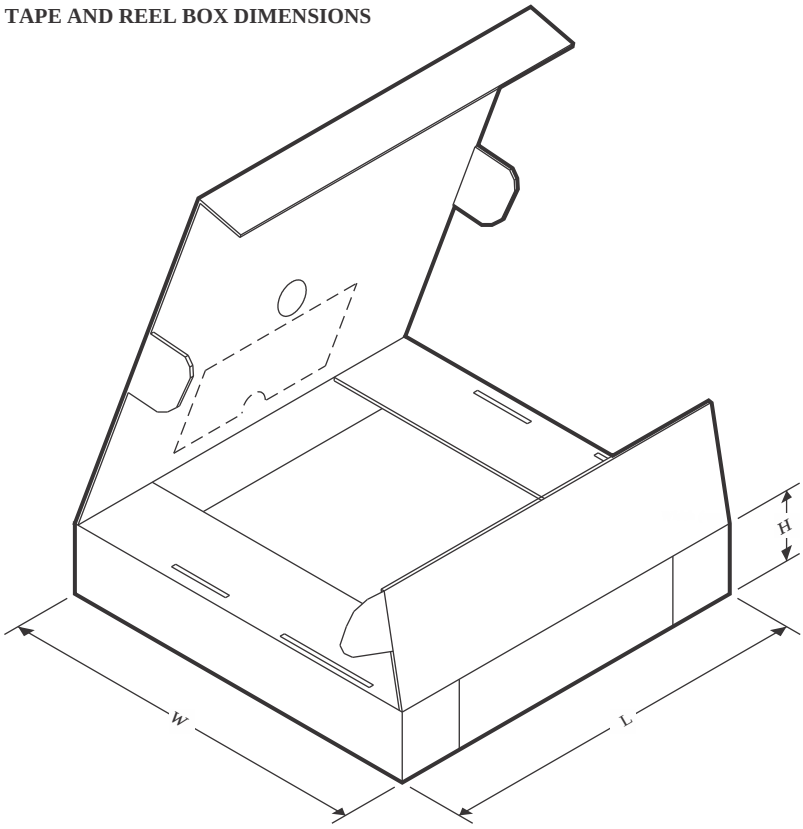
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA350ABSIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA350ABSIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA350CDSIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA350CDSIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

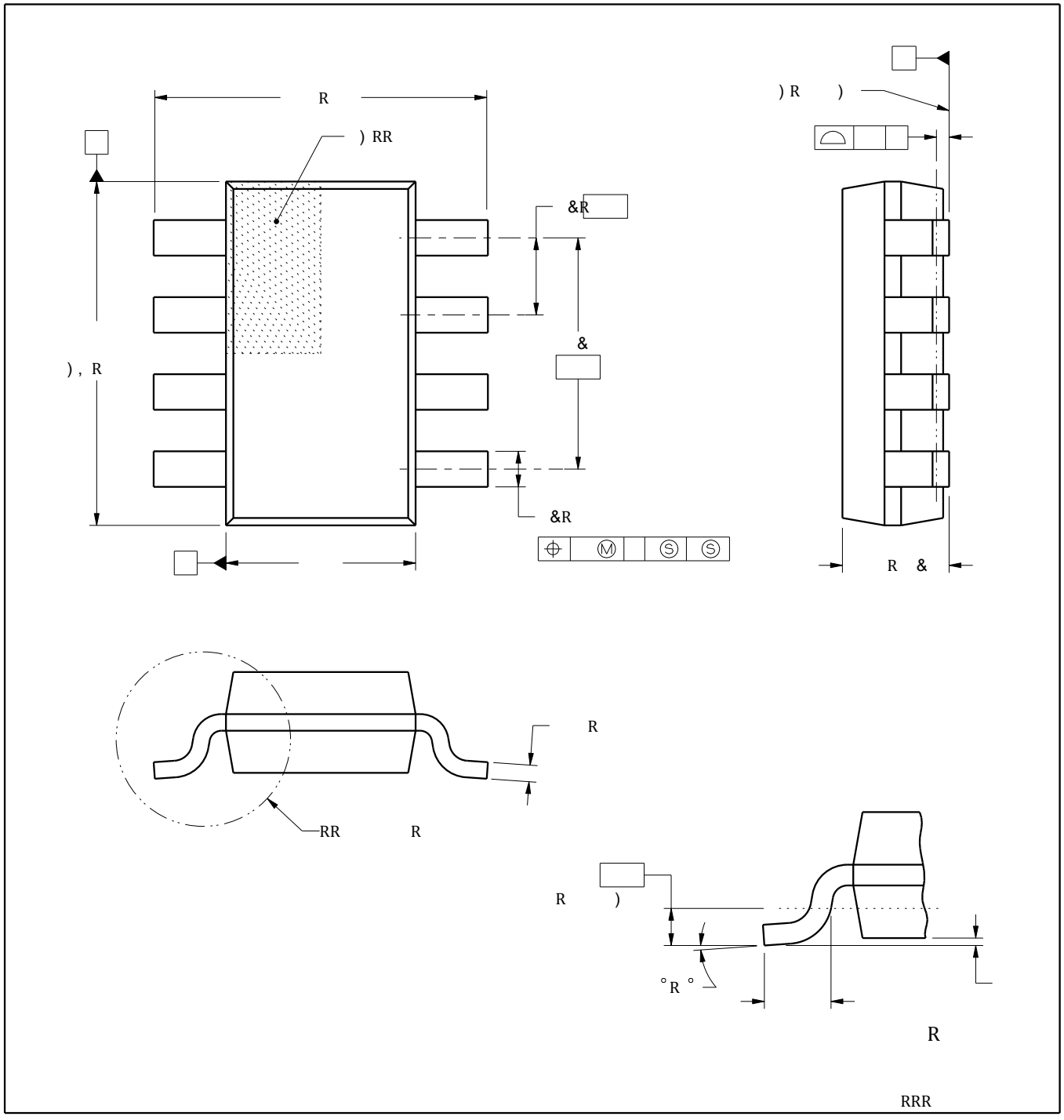
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA350ABSIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA350ABSIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
INA350CDSIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
INA350CDSIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0

R R)

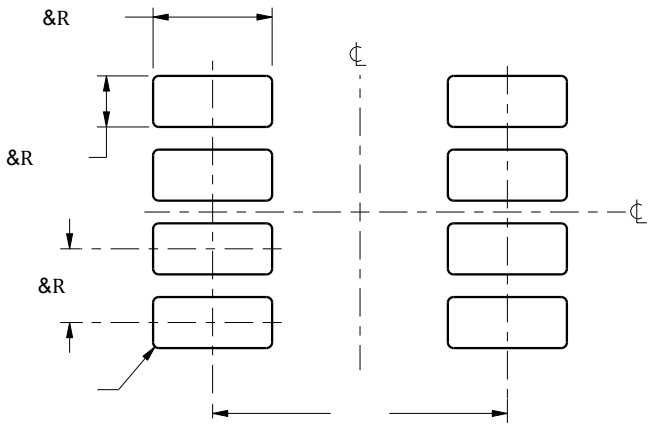


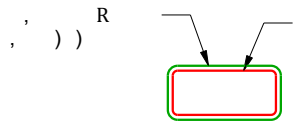
), R
R
R RR RRR R R RR RRRRR RR
RRRRR R R
R R R R R R R R
R R R R R R R OR OR R R R R OR OR R R R R
RRRRRR RR
R

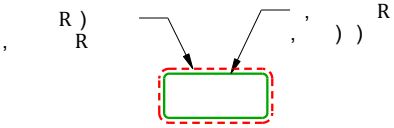
EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23 - 1.1 mm max height







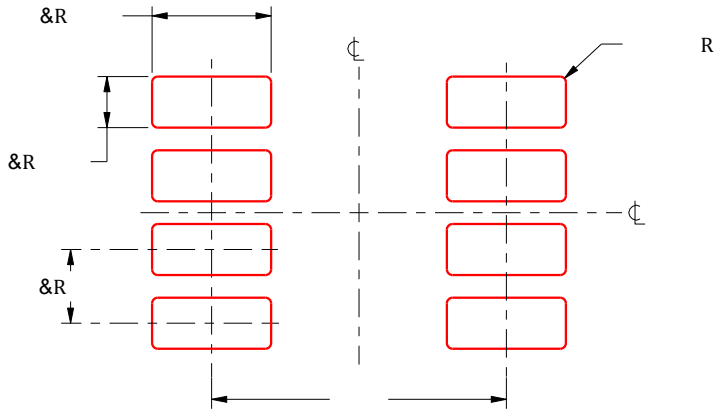
RRR

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

R R)



, R R &
R) R R R R)
&

RRR

) , R
R
RR R R R RRRRR RR R RR R RR
RRRRR RRR
RR R R RR R RR R
R

GENERIC PACKAGE VIEW

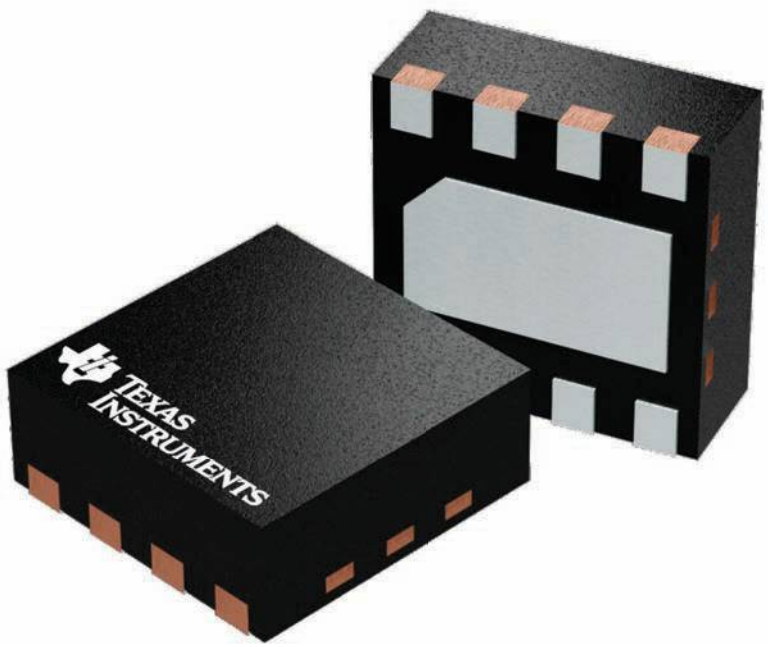
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



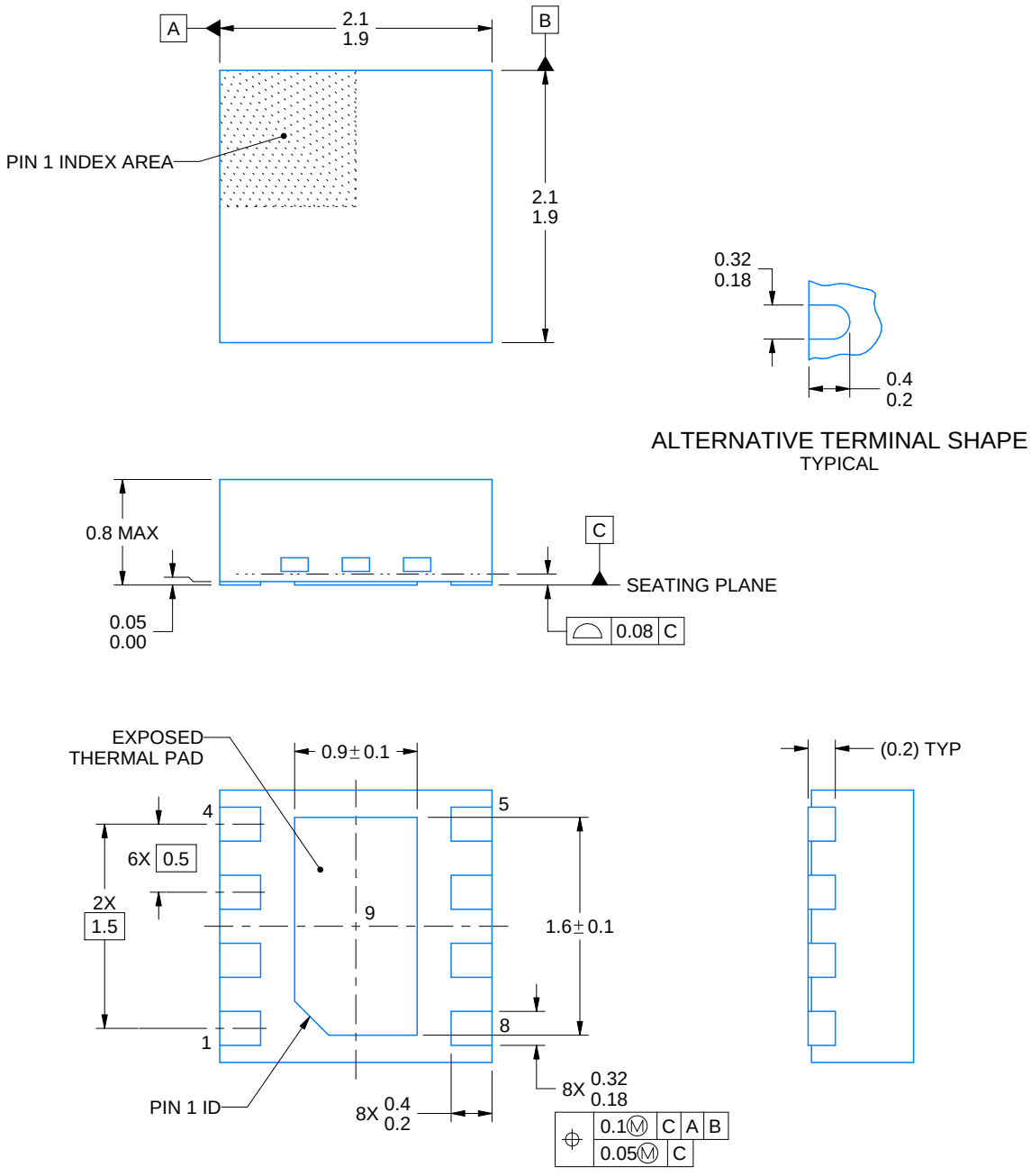
4224783/A

PACKAGE OUTLINE

DSG0008A

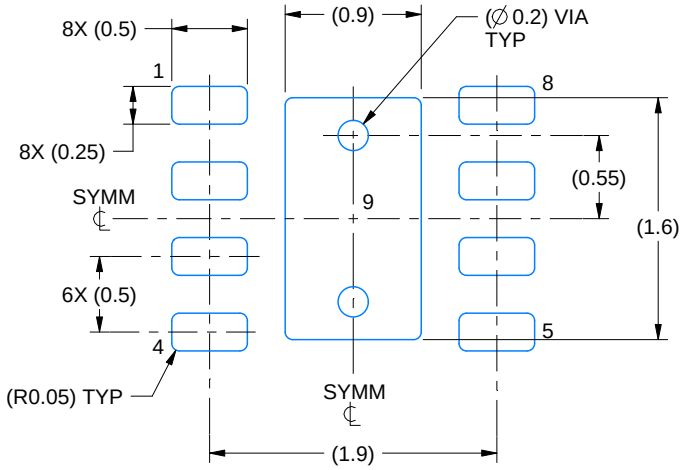
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

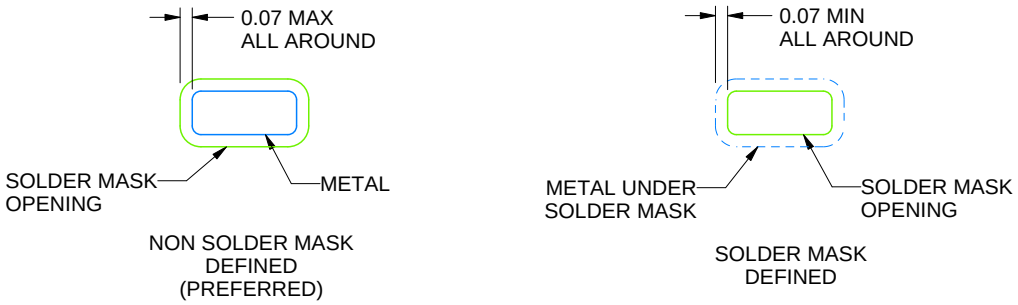


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

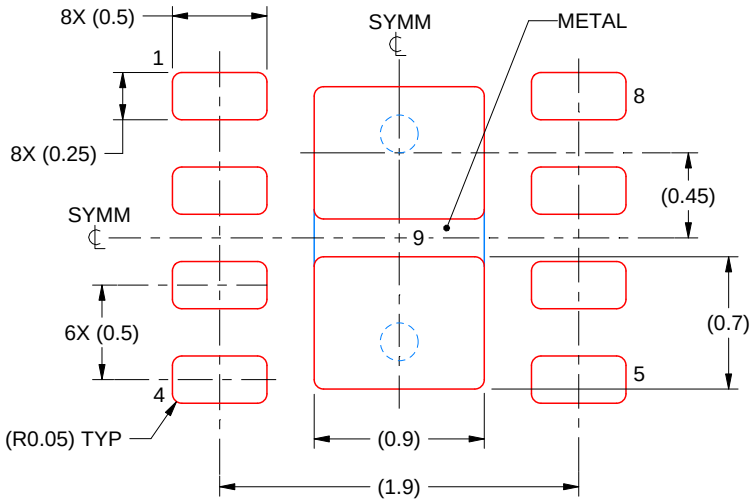


SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
ISOUSB111
SLLSFC6A – NOVEMBER 2021 – REVISED APRIL 2022

ISOUSB111 Full/Low Speed Isolated USB Repeater

1 Features

- Compliant to USB 2.0
- Supports low speed (1.5 Mbps) and full speed (12 Mbps) signaling
- Automatic speed and connection detection
- Supports L1 (sleep) and L2 (suspend) low-power states
- Supports automatic role reversal for USB On-The-Go (OTG) and Type C Dual Role Port (DRP) designs
- High CMTI: 100 kV/µs
- V_{BUS} voltage range: 4.25 V to 5.5 V
  - 3.3 V internal LDO
- Meets CISPR32 class B emissions limits
- Ambient temperature range: –40°C to +125°C
- 16-SOIC package
- Safety-related certifications:
  - 8000-V_{PK} V_{IOTM} and 2121-V_{PK} V_{IORM} (Reinforced and Basic Options) per DIN VDE V 0884-11
  - 5700-V_{RMS} isolation for 1 minute per UL 1577
  - IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV and CSA certifications
  - All certifications planned

2 Applications

- USB Hub, Host, Peripheral and Cable Isolation
- Medical
- Factory automation
- Motor drives
- Grid infrastructure
- Power delivery

Reinforced and Basic Isolation Options

FEATURE	ISOUSB111	ISOUSB111B
Protection Level	Reinforced	Basic
Surge Test Voltage	12800 V_{PK}	6000 V_{PK}
Isolation Rating	5700 V_{RMS}	3000 V_{RMS}
Working Voltage	1500 V_{RMS} / 2121 V_{PK}	1500 V_{RMS} / 2121 V_{PK}

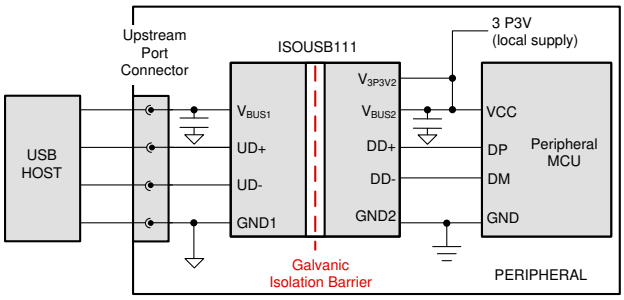
3 Description

ISOUSB111 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5 Mbps) and full speed (12 Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. The device also supports automatic role reversal - if after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. This feature enables the device to support USB On-The-Go (OTG) and Type-C Dual Role Port (DRP) implementations. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of up to 5700 V_{RMS} and a working voltage of 1500 V_{RMS}. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISOUSB111 device is available for both basic and reinforced isolation (see *Reinforced and Basic Isolation Options*). It supports a wide ambient temperature range of –40°C to +125°C. The device is available in the standard SOIC-16 (16-DW) packageand a smaller SSOP-16 (16-DWX) package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
ISOUSB111	SOIC (16) DW	10.30 mm × 7.50 mm
	SSOP (16) DWX	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (April 2022)	Page
• T_A Max value updated to 125°C	5

5 Pin Configuration and Functions

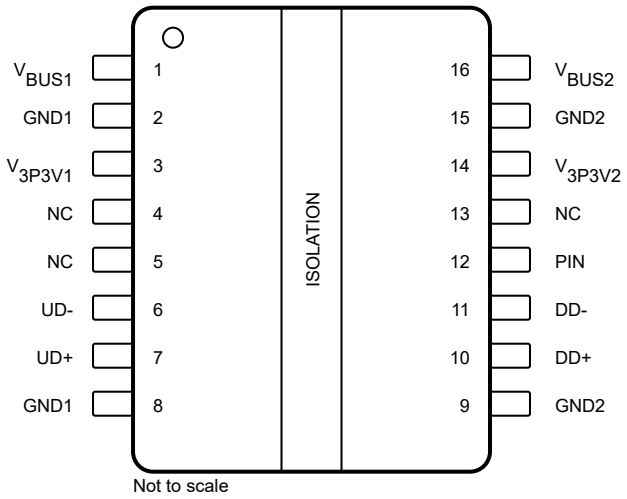


Figure 5-1. DW Package 16-Pin SOIC Top View

Pin Functions—16 DW

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS1}. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
4	NC	—	Preferably leave floating or connect to V_{3P3V1}. It is also OK to connect to GND1.
5	NC	—	Preferably leave floating or connect to V_{3P3V1}. It is also OK to connect to GND1.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	PIN	I	Upstream pull-up enable. If this pin is low, pull-up on DD+ and DD- is not recognized.
13	NC	—	Preferably leave floating or connect to V_{3P3V2}. It is also OK to connect to GND2.
14	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS2}. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

ADVANCE INFORMATION

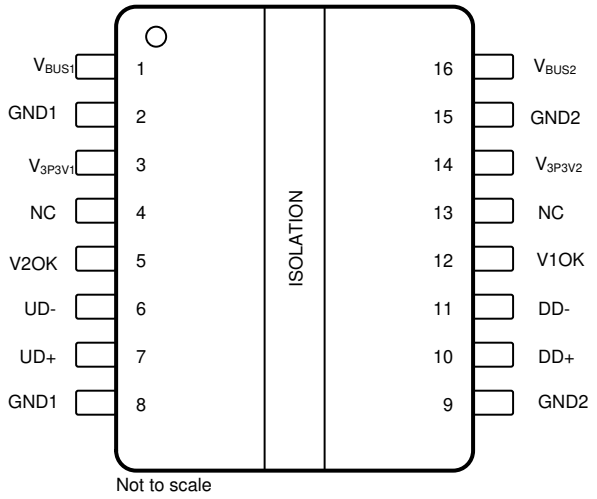


Figure 5-2. DWX Package 16-Pin SSOP Top View

Table 5-1. Pin Functions—16 DWX

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS1}. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
4	NC	—	Leave floating or connect to V_{3P3V1}.
5	V2OK	O	High level on this pin indicates that side 2 is powered up.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	V1OK	—	High level on this pin indicates that side 1 is powered up.
13	NC	—	Leave floating or connect to V_{3P3V2}.
14	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS2}. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{BUS1}, V_{BUS2}	V_{BUS} supply voltage	-0.3	6	V
V_{3P3V1}, V_{3P3V2}	3.3-V input supply voltage	–0.3	4.25	V
V_{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cummulative duration of 1000 hrs.	–0.3	6	V
V_{IO}	IO voltage range (PIN,)	–0.3	V_{3P3Vx}+0.3(3)	V
I_O	Output current on output pins (V*OK)	-10	10	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 4.25 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUSx}	V_{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V_{3P3Vx}	3.3-V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
T_A	Operating free-air temperature	-40		125	°C
T_J	Junction temperature	–55		150	°C

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC1(1)		ISOUSB111 DW (SOIC) 16 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	30	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOUSB111						
P_D	Maximum power dissipation (both sides)	V_{BUS1} = V_{BUS2} = 5.5 V, T_J = 150°C, C_L = 50 pF each on DD- and DD+, Input a 6-MHz 50% duty cycle differential 3.3-V square wave on UD- and UD+			165	mW
P_{D1}	Maximum power dissipation (side-1)				82.5	mW
P_{D2}	Maximum power dissipation (side-2)				82.5	mW

ADVANCE INFORMATION

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS		UNIT
			DW-16	DWX-16	
IEC 60664-1					
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	>8	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>8	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	
DIN VDE V 0884-11:2017-011(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	1500	1500	V_{RMS}
		DC voltage	2121	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage ISOUSB111	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	8000	8000	V_{PK}
	Maximum transient isolation voltage ISOUSB111B		4242	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOUSB111(3)	Test method per IEC 62368-1, 1.2/50 ms waveform, V_{TEST} = 1.6 × V_{IOSM} = 12800 V_{PK} (qualification)	8000	8000	V_{PK}
	Maximum surge isolation voltage ISOUSB111B(3)	Test method per IEC 62368-1, 1.2/50 ms waveform, V_{TEST} = 1.3 × V_{IOSM} = 6000 V_{PK} (qualification)	4615	4615	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, Vini = VIOTM, tini = 60 s; ISOUSB111: Vpd(m) = 1.6 × V_{IORM}, tm = 10 s ISOUSB111B: Vpd(m) = 1.2 × V_{IORM}, tm = 10 s	≤ 5	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), Vini = V_{IOTM}, tini = 1 s; ISOUSB111: Vpd(m) = 1.875 × V_{IORM}, tm = 1 s ISOUSB111B: Vpd(m) = 1.5 × V_{IORM}, tm = 1 s	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 pft), f = 1 MHz	1	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	> 10^{12}	W
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	> 10^9	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage, ISOUSB111	V_{TEST} = V_{ISO} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)	5700	5700	V_{RMS}
	Withstand isolation voltage, ISOUSB111B		3000	3000	V_{RMS}

(1) Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
(2) ISOUSB111 is suitable for safe electrical insulation and ISOUSB111B is suitable for basic electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

ADVANCE INFORMATION

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN VDE V 0884-11:2017-01	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Maximum transient isolation voltage, ISOUSB111: 8000 V_{PK} ISOUSB111B: 4242 V_{PK} Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, ISOUSB111: 8000 V_{PK} (Reinforced) ISOUSB111B: 4615 V_{PK} (Basic)	IEC 62368-1 2nd Ed., for pollution degree 2, material group I ISOUSB111: 800 V_{RMS} reinforced isolation ISOUSB111B: 1000 V_{RMS} basic isolation ---------- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1+A1 ISOUSB111: 2 MOPP (Means of Patient Protection) 250 V_{RMS} (354 V_{PK}) maximum working voltage	Single protection, ISOUSB111: 5700 V_{RMS} ISOUSB111B: 3000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	EN 61010-1:2010/A1:2019 ISOUSB111: 600 V_{RMS} reinforced isolation ISOUSB111B: 1000 V_{RMS} basic isolation ---------- EN 62368-1:2014 ISOUSB111: 800 V_{RMS} reinforced isolation ISOUSB111B: 1000 V_{RMS} basic isolation
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =70°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			324	mA
		$R_{\theta JA}$ = 70°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			495	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 70°C/W, T_J = 150°C, T_A = 25°C			1785	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		11.5	14.8	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		9.5	13	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		9.5	13	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	9.8	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L2 Suspend mode	Upstream Facing side		1.5	2.05	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
$UV+_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V
$UV-_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$UVHYS_{(VBUSx)}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$UV+_{(V3P3Vx)}$	Under voltage threshold when supply voltage is rising, V_{3P3V}				2.95	V
$UV-_{(V3P3Vx)}$	Under voltage threshold when supply voltage is falling, V_{3P3V}		1.95			V
$UVHYS_{(V3P3Vx)}$	Under voltage threshold hysteresis, V_{3P3V}			0.11		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x V_{3PV3x}			V
V_{IL}	Low-level input voltage				0.3 x V_{3PV3x}	V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				10	µA
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
Z_{INP_xDx}	Impedance to GND, no pull up/down	Vin=3.6 V, V_{3P3Vx}=3.0 V, T_J < 125 °C, USB 2.0 Spec Section 7.1.6	300			kΩ
C_{IO_xDx}	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	kΩ
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	kΩ

ADVANCE INFORMATION

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D- with pull up enabled on upstream port with external load disconnected.	3		3.6	V
UDx, DDx, INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Host downstream port pull down resistor enabled and Device pulled up to 3.0 V - 3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V_{DI}	Differential Input Sensitivity	|(xD+)-(xD-)|; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V_{LSFS_HYS}	Differential Input Hysteresis FS/LS	|(xD+)-(xD-)|; (measured at connector) V_{CM} = 0.8 V to 2.0 V	25	75	245	mV
V_{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1, (measured at connector with RL of 0.9 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
V_{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, Measured during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	°C
TSD-	Thermal shutdown turn-off temperature		150	160	170	°C
TSD_{HYS}	Thermal shutdown hysteresis			10		°C

(1) If V_{BUSx} pins are externally connected to the corresponding V_{3P3Vx} pins, then UVLO thresholds on V_{BUSx} are governed by $UV+_{(V3P3Vx)}$, $UV-_{(V3P3Vx)}$ and $UVHYS_{(V3P3Vx)}$

ADVANCE INFORMATION

6.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
$T_{SUPRAMP}$	Allowed power supply ramp-up times on V_{BUSx} and V_{3P3Vx} external power supplies		0.005		100	ms
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with 5 µs power up time.		5	10	ms
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching (T_{FR}/T_{FM})	USB 2.0 Spec 7.1.2, Excluding the first transition from the Idle state, Figure 7-9, C_L = 50 pF	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/ TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
$T_{FILTCONN}$	Debounce filter on FS or LS Connect Detection		45	70	80	µs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	µs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	µs
T_{2SUSP}	Time taken by the US side to detect suspend mode (L2) and draw less than 2.5 mA current when bus is continuously in idle state.		3		10	ms
$t_{DRESUMEL1}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	µs
$t_{DRESUMEL2}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	µs
$t_{DWAKEL1}$	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	µs
$t_{DWAKEL2}$	Maximum pulse width of remote wake that is guranteed to be detected when in suspend/L2 state.				900	µs
$t_{DRSMPROP}$	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	V_{CM} = 1200 VPK	75	100		kV/µs
REPEATER TIMING - LS, FS						

ADVANCE INFORMATION

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-20		20	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	210			ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	14			ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

ISOUSB111 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5 Mbps) and Full Speed (12 Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB111 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal - if after disconnect, if a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed.

ISOUSB111 is available in basic and reinforced isolation options with isolation withstand voltage of 3000 V_{RMS} and 5700 V_{RMS} respectively, and with surge test voltage of 6 kV_{PK} and 12.8 kV_{PK} respectively. The device can operate completely off a 4.25 V to 5.5 V supply (USB VBUS power) or from local 3.3-V supply, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

7.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB111 is shown in Figure 7-1. The device comprises the following:

1. Transmit and receive circuits and pull-up and pull-down resistors according to the USB standard.
2. Digital logic to handle bi-directional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} supplies from the V_{BUSx} supplies.
4. Galvanic isolation.

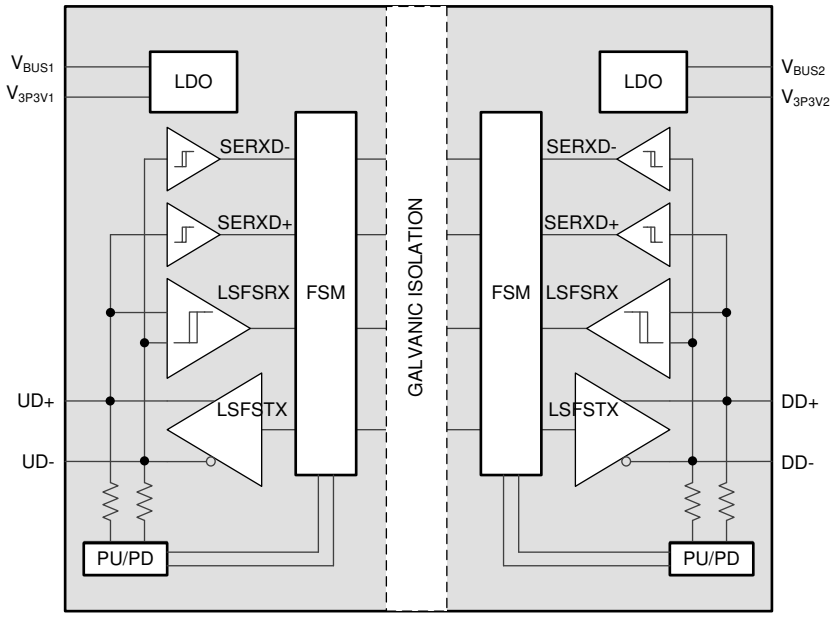


Figure 7-1. ISOUSB111 Simplified Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply Options

The ISOUSB111 can be powered by connecting a 4.25 V to 5.5 V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is suitable for the side facing the USB connector, where a 5-V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external power 3.3-V supply can be connected to both. This second option is suitable for the side facing the microcontroller, where a 5-V supply may not be available.

ADVANCE INFORMATION

7.3.2 Power Up

Until all power supplies on both sides of ISOUSB111 are above their respective UVLO thresholds, the device ignores any activity on the bus lines on both upstream and downstream side. Once the power supplies are above their UVLO thresholds, the device is ready to respond to activity on the bus lines.

7.3.3 Symmetric Operation, Dual-Role Port and Role-Reversal

ISOUSB111 supports symmetric operation. Normally, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, it is also possible to connect UD+ and UD- to a peripheral and DD+ and DD- to a host or hub. Whichever side sees a connect first (D+ or D- pulled up to 3.3V) becomes the downstream facing side. This feature enables implementation of dual-role port (for eg. type C dual-role port) and role-reversal (for eg. OTG Host Negotiation Protocol - HNP). In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignement is swapped.

7.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB111, internal 15 kΩ pull-down resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCONN}$, the ISOUSB111 device treats this as a connect. The ISOUSB111 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB111 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB111 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

7.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL}threshold) for a time period higher than T_{DDIS}. Upon disconnect detection in FS and LS modes, the ISOUSB111 device removes the pull-up resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB111 then waits for the next connect event to occur.

7.3.6 Reset

The ISOUSB111 device detects Reset assertion (prolonged SE0 state) on its upstream facing side, and transmits the same to the downstream facing side. In FS and LS states the reset is detected within 2.5 µs.

7.3.7 LS/FS Message Traffic

The ISOUSB111 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till either an End-of-Packet (EOP) or a long idle is seen. At this point, the ISOUSB111 device tri-states it's LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

7.3.8 L2 Power Management State (Suspend) and Resume

The ISOUSB111 device supports Suspend low power state, also called L2 state in the USB 2.0 Link Power Management engineering change notice (ECN). Suspend mode is detected if the bus stays in the LS/FS idle state for more than 3 ms. When Suspend is detected from LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L2 low-power mode is completed within 10 ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signalled by the host by driving two

low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the resume and wake signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state it was in before entering the L2 state.

7.3.9 L1 Power Management State (Sleep) and Resume

The ISOUSB111 device supports the additional L1 or Sleep low power state defined in the USB 2.0 Link Power Management ECN. When L1 entry is detected from the LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L1 low-power mode is completed within 50 µs.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a ‘K’ state by the host or the device respectively. The end of resume is signalled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state it was in before entering the L1 state.

7.4 Device Functional Modes

Table 7-1 lists the functional modes for the ISOUSB111 device.

Table 7-1. Function Table

SIDE 1 SUPPLY V_{BUS1}, V_{3P3V1} (1)	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V_{PIN}	SIDE 2 SUPPLY V_{BUS2}, V_{3P3V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	H	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and vice-versa.
Powered	15-kΩ PD	L	Powered	15-kΩ PD	Disconnected state is presented on both upstream and downstream
Powered	15-kΩ PD	X	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	X	Powered	15-kΩ PD	
Unpowered	Z	X	Unpowered	Undetermined	

(1) Powered = ($V_{BUSx} \geq UV+_{(VBUSx)}$) || ($V_{BUSx} = V_{3P3Vx} \geq UV+_{(V3P3Vx)}$) ; Unpowered = ($V_{BUSx} < UV-_{(VBUSx)}$) & ($V_{3P3Vx} < UV-_{(V3P3Vx)}$) ; X = Irrelevant; H = High level; L = Low level; Z = High impedance

ADVANCE INFORMATION

8 Power Supply Recommendations

0.1 µF capacitors are recommended to be placed very close to V_{3P3Vx} pins to GNDx. 1-µF capacitors are recommended to be placed placed very close to V_{BUSx} pins to GNDx.

These decoupling capacitor recommendations are irrespective of whether the 3.3 V supplies are provided externally or generated using internal LDOs.

Refer to the Section 10.1.1 section for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins on the top layer without the use of vias.

While isolating a host/hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's SN6505B. For such applications, detailed power supply design, and transformer selection recommendations are available in the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet. If CDP functionality is enabled while isolation host/hub, the isolated power supply must be capable of delivering 1.5 A on VBUS.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Isolated Host or Hub

Figure 9-1 shows an application for isolating a host or a hub using ISOUSB111. In this example, on the microntroller side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3-V local supply. Note that, for a host or hub, the USB standard requires a 120-µF capacitor to be placed on the VBUS so as to be able provide in-rush current when a downstream peripheral is attached. In addition, a 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

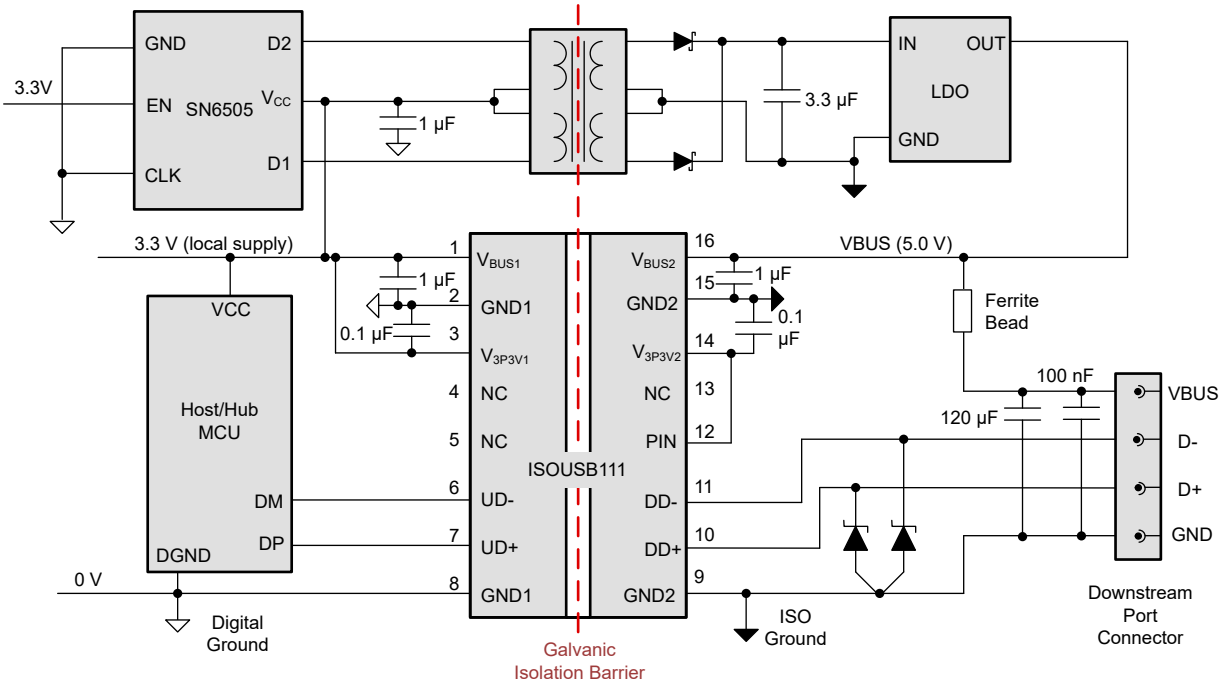


Figure 9-1. Isolated Host or Hub with ISOUSB111

9.1.2 Isolated Peripheral - Self-Powered

Figure 9-2 shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, on the microntroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

ADVANCE INFORMATION

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

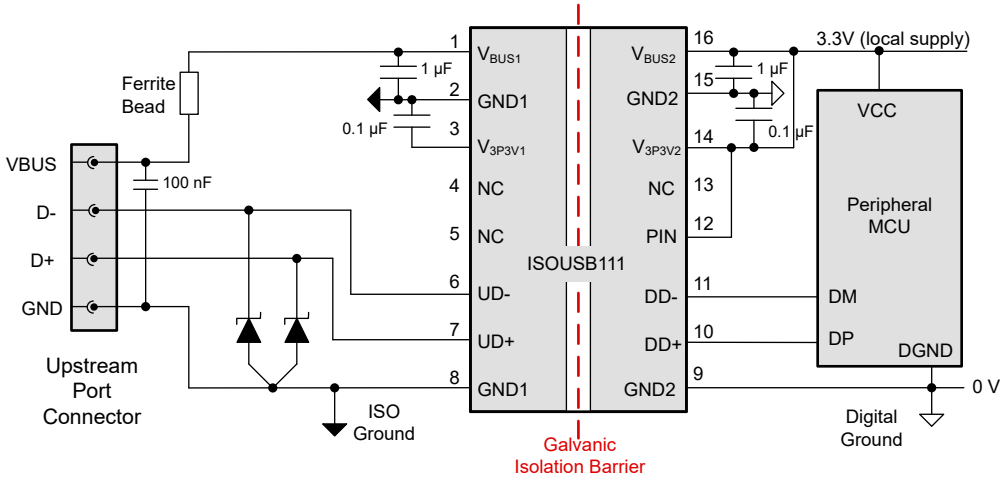


Figure 9-2. Isolated Self-Powered Peripheral with ISOUSB111

9.1.3 Isolated Peripheral - Bus-Powered

Figure 9-3 shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3-V local supply while deriving power from the USB VBUS. On the microntroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

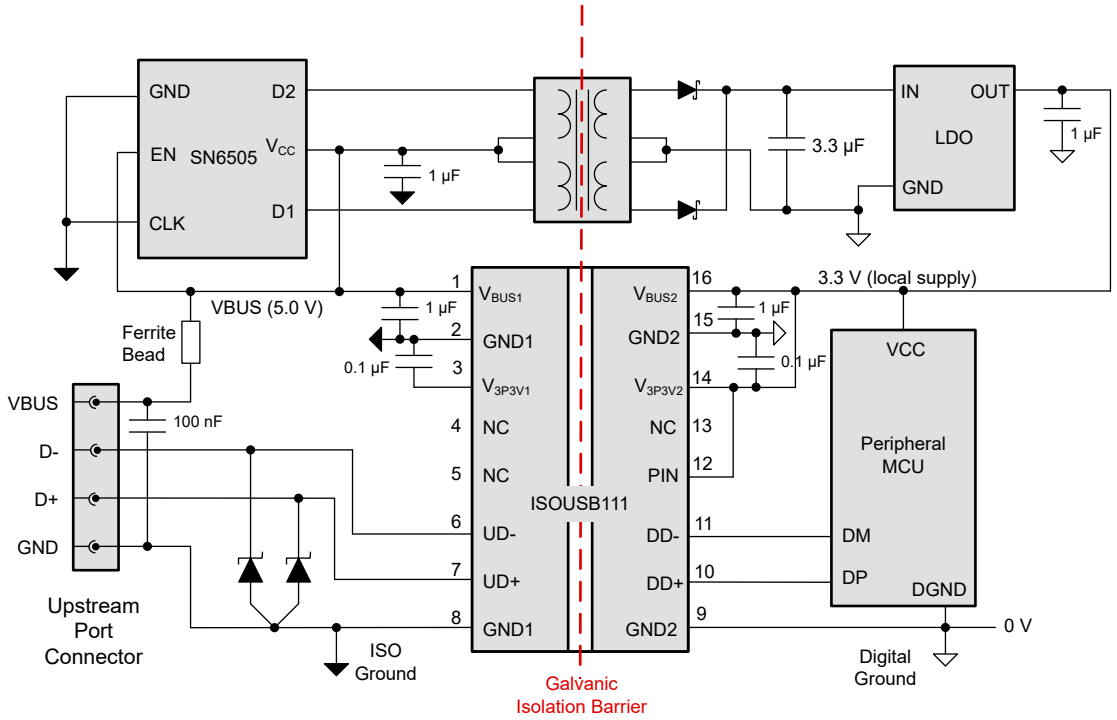


Figure 9-3. Isolated Bus-Powered Peripheral using ISOUSB111

9.1.4 Application Curve

9.1.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 9-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 and DWX-16 packages is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

ADVANCE INFORMATION

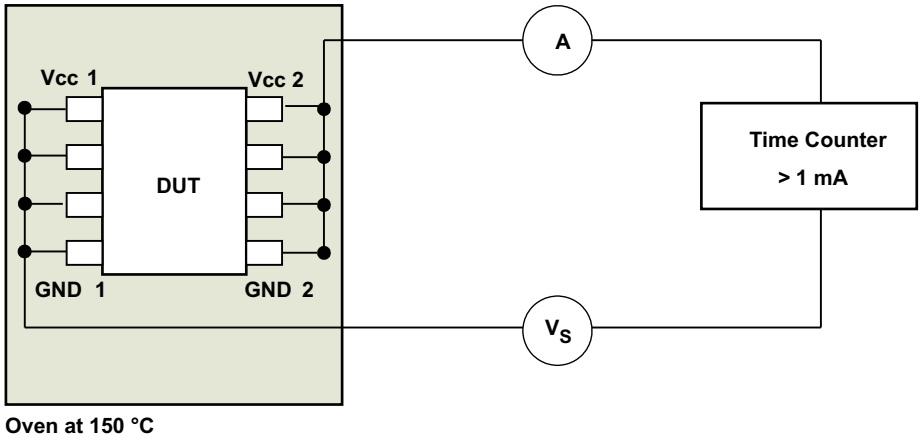


Figure 9-4. Test Setup for Insulation Lifetime Measurement

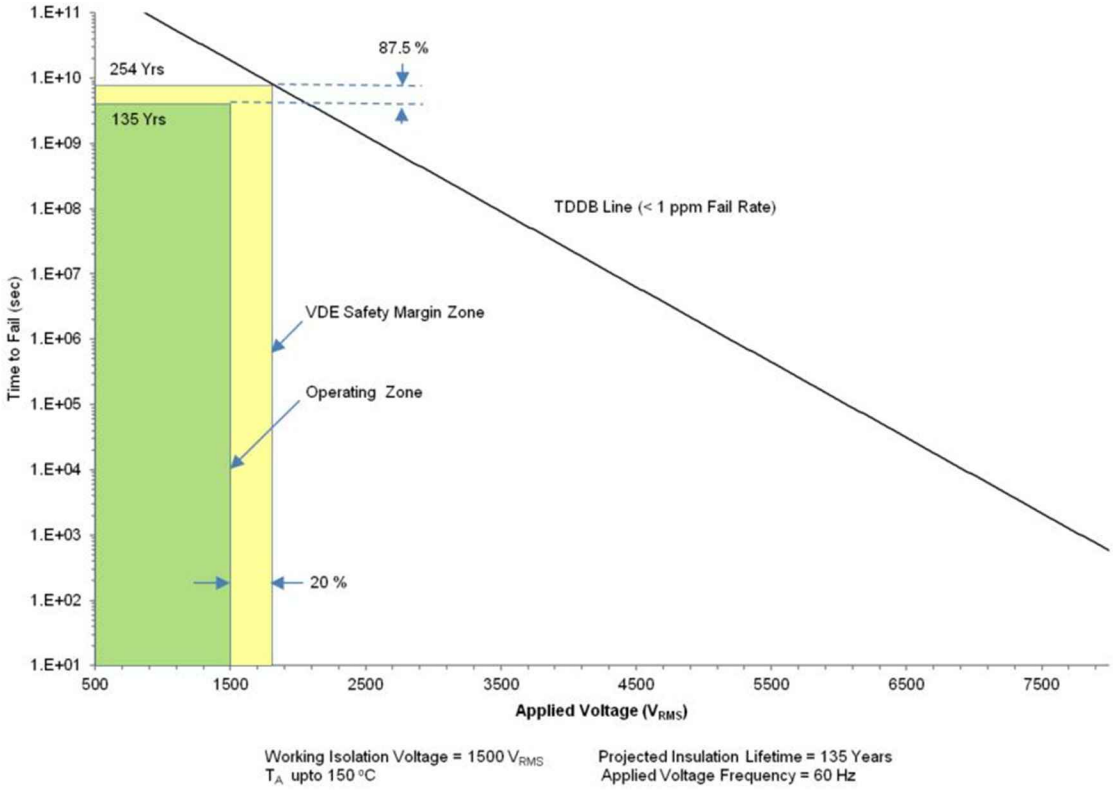


Figure 9-5. Insulation Lifetime Projection Data

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Two layers are sufficient to accomplish a low EMI PCB design.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90-Ω differential impedance and as close to 45-Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

10.1.1 Layout Example

The layout example in this section shows the recommended placement for de-coupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The ESD protection diodes should be placed close to the connector with a strong connection to the ground plane. The example shown is for an isolated host or hub, but similar considerations apply for isolated peripherals also. The 120-µF capacitor on VBUS only applies to host or hub and should not be used for peripherals. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed on the VBUS route, after the 100-nF (and 120-µF) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.

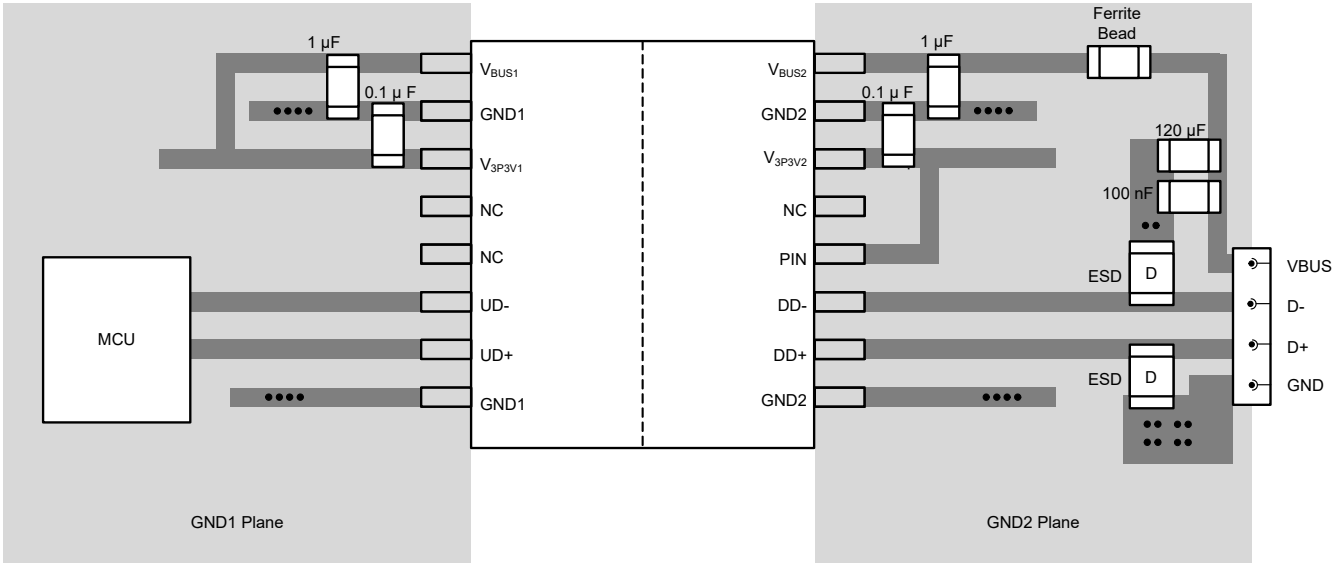


Figure 10-1. Layout Example for ISOUSB111

10.1.2 PCB Material

For digital circuit boards operating at less than 500 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

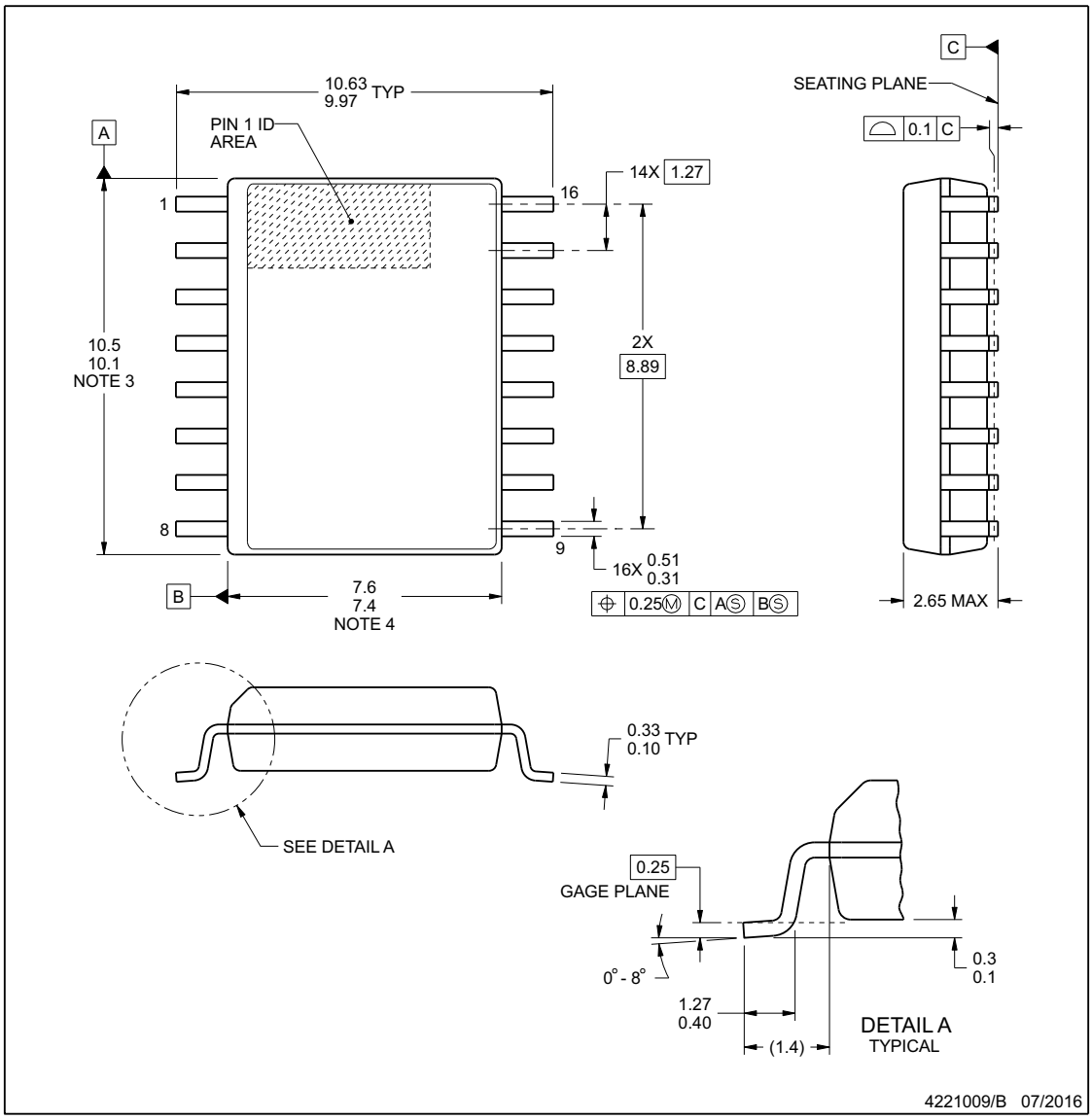
ADVANCE INFORMATION

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

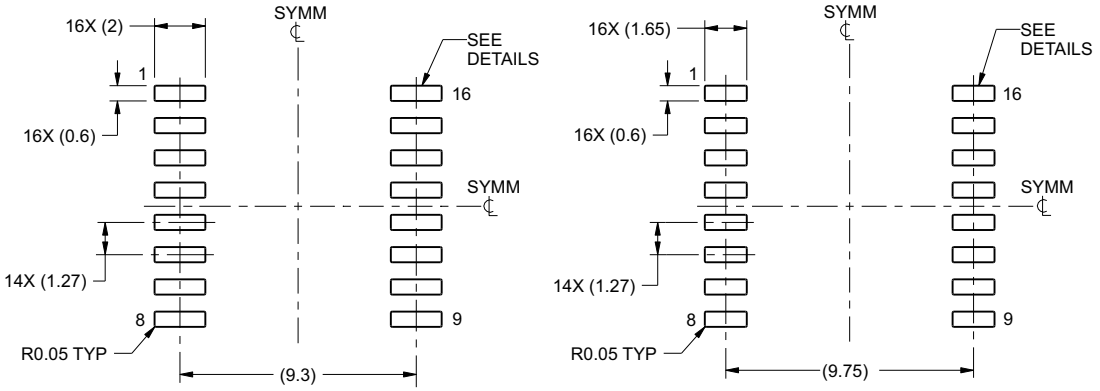
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

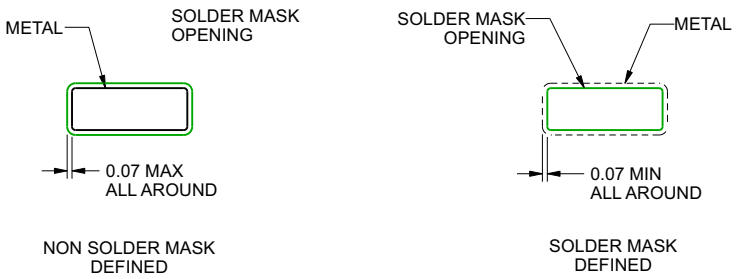
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

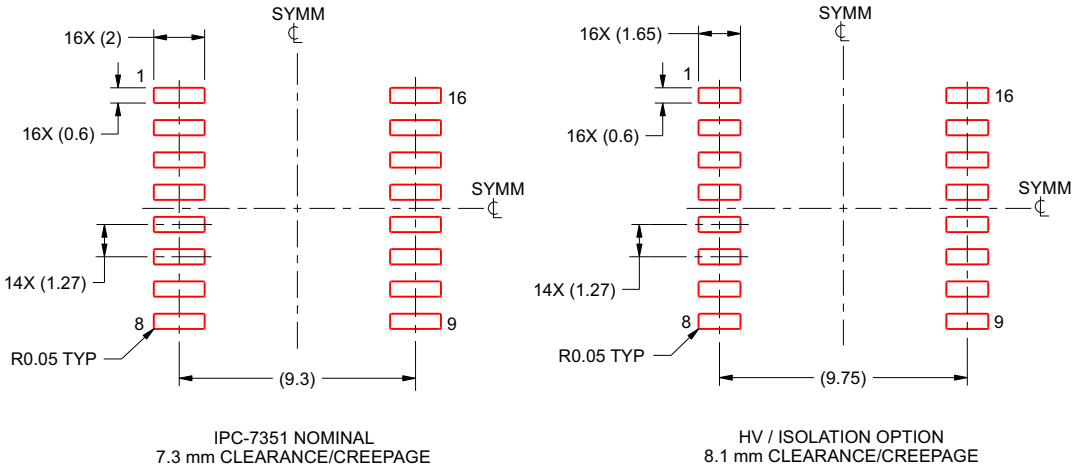
ADVANCE INFORMATION

PDVr t uP 57Pc (ku) P5ke c

) 0 668

5nK(394 1 1 1So 2C.A2a

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

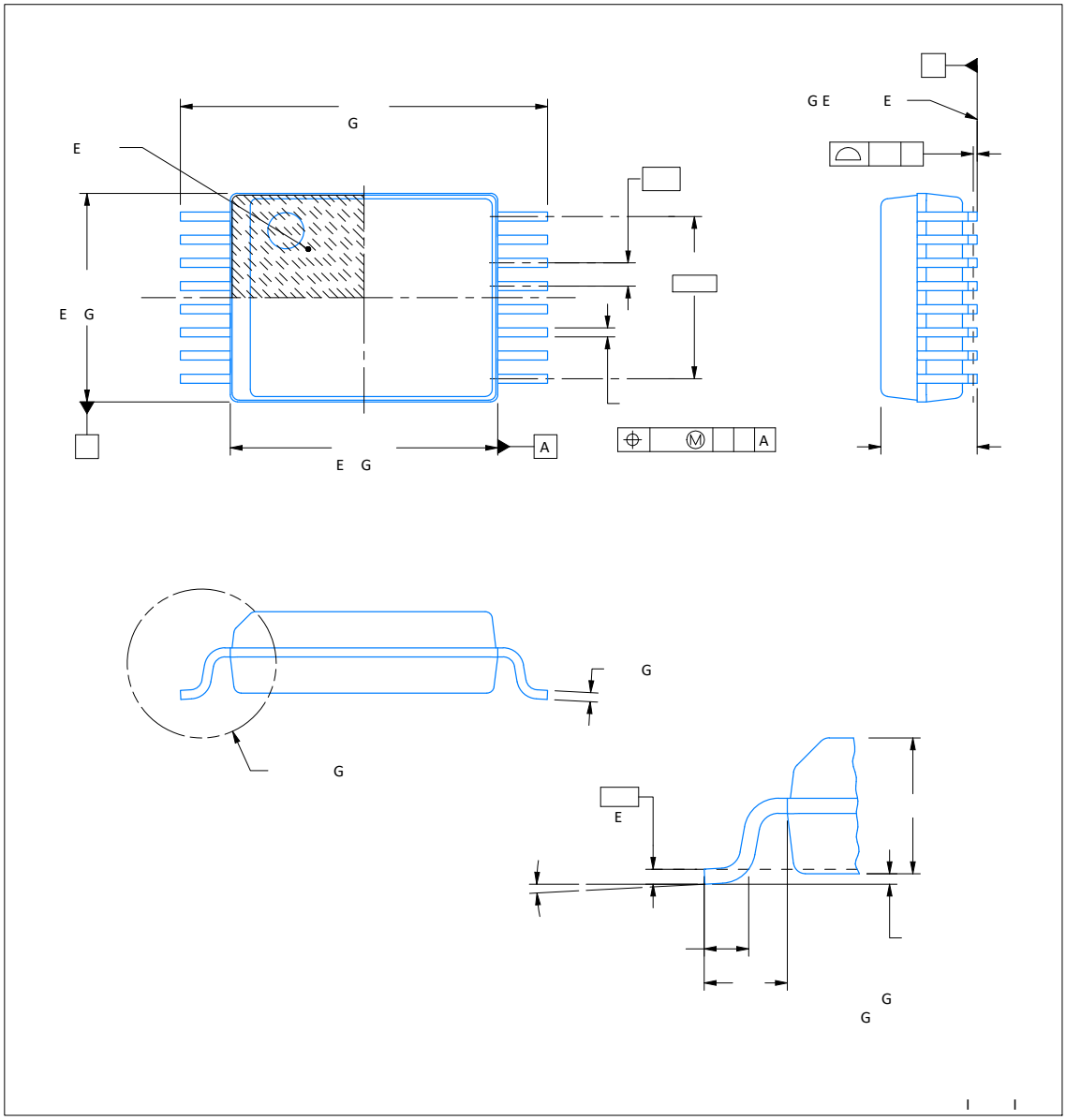
ADVANCE INFORMATION

PACKAGE OUTLINE

DWX0016A

SSOP - 2.6 mm max height

G E



E G

D D

G
G

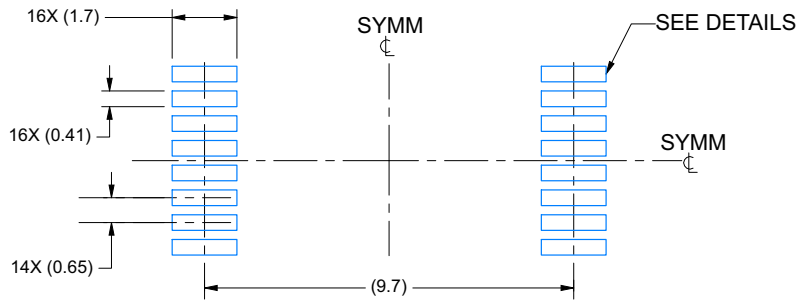
G

ADVANCE INFORMATION

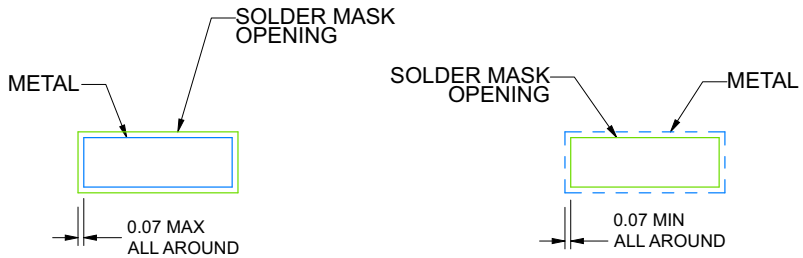
EXAMPLE BOARD LAYOUT

DWX0016A — **SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226511/A 01/2021

NOTES: (continued)

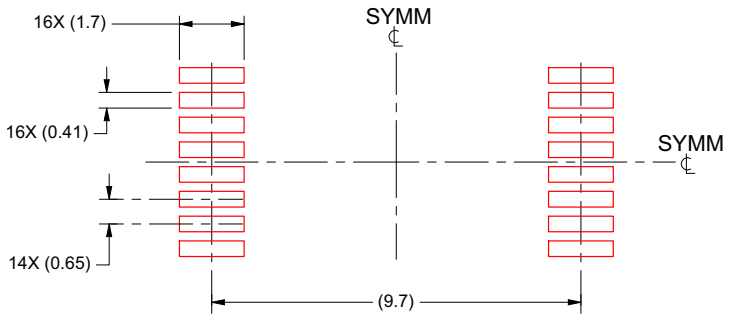
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

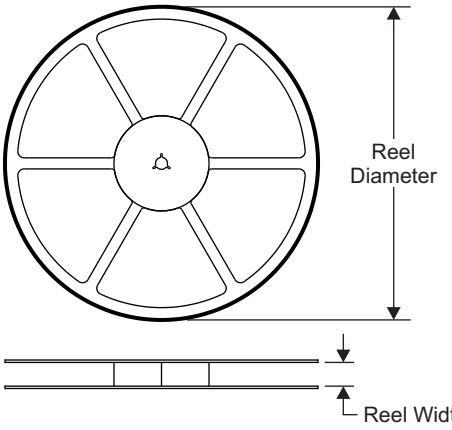
4226511/A 01/2021

NOTES: (continued)

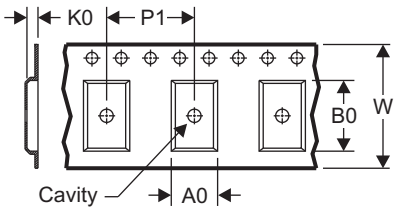
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

12.1 Tape and Reel Information

REEL DIMENSIONS

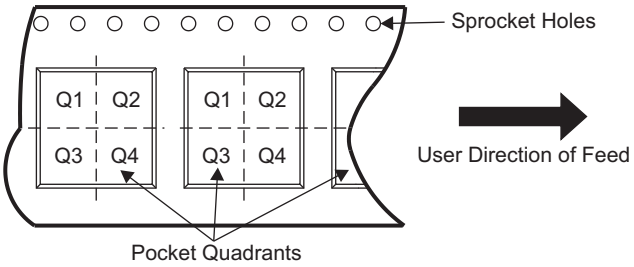


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

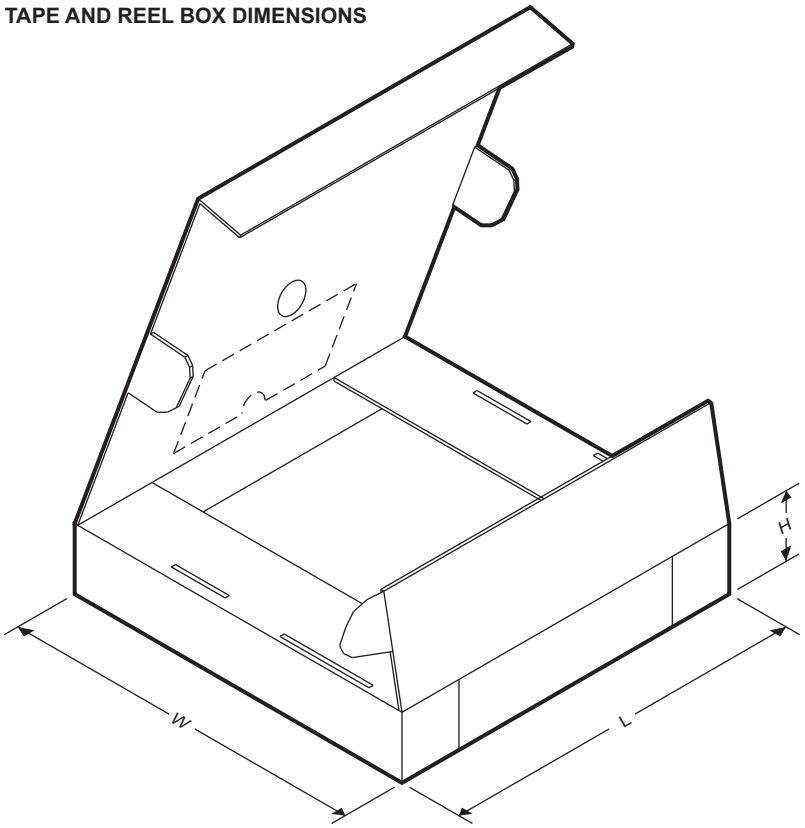
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOUSB111DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOUSB111DWXR	SSOP	DWX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOUSB111DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISOUSB111DWXR	SSOP	DWX	16	1000	350.0	350.0	43.0

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XISOUSB111DWR	ACTIVE	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
XISOUSB111DWXR	ACTIVE	SSOP	DWX	16	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

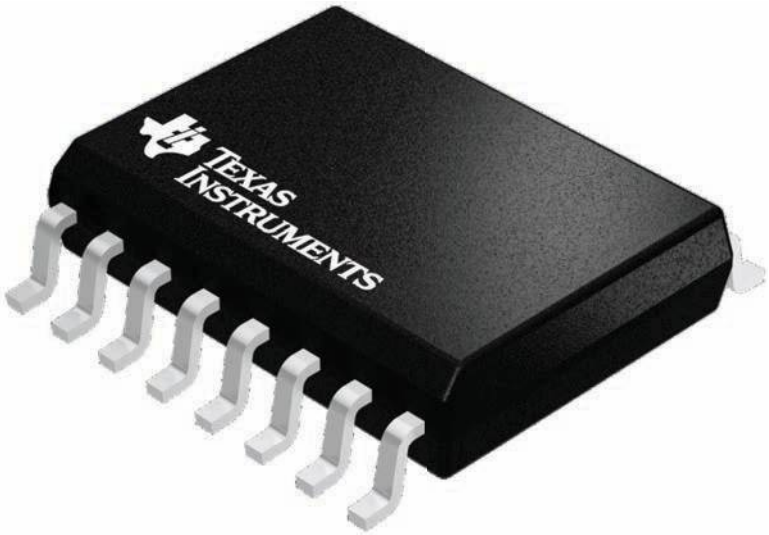
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
ISOUSB211
SLLSFC5A – NOVEMBER 2021 – REVISED MARCH 2022

ISOUSB211 High/Full/Low Speed Isolated USB Repeater

1 Features

- Compliant to USB 2.0
- Supports low speed (1.5 Mbps), full speed (12 Mbps) and high speed (480 Mbps) signaling
- Automatic speed and connection detection
- Programmable equalization to compensate board trace loss in high speed mode
- CDP advertising on downstream side
- Supply OK indication on opposite side
- Supports automatic role reversal
- High CMTI: 100 kV/µs
- V_{BUS} voltage range: 4.25 V to 5.5 V
  - 3.3 V and 1.8 V internal LDOs
- Meets CISPR32 class B emissions limits
- Ambient temperature range: –40°C to +125°C
- Small footprint 28-SSOP package
- Safety-related certifications:
  - 8000-V_{PK} V_{IOTM} and 2121-V_{PK} V_{IORM} (Reinforced and Basic Options) per DIN VDE V 0884-11
  - 5700-V_{RMS} isolation for 1 minute per UL 1577
  - IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
  - CQC, TUV and CSA certifications
  - All certifications planned

2 Applications

- USB Hub, Host, Peripheral and Cable Isolation
- Medical
- Factory automation
- Motor drives
- Grid infrastructure
- Power delivery

Reinforced and Basic Isolation Options

FEATURE	ISOUSB211	ISOUSB211B
Protection Level	Reinforced	Basic
Surge Test Voltage	12800 V_{PK}	6000 V_{PK}
Isolation Rating	5700 V_{RMS}	3000 V_{RMS}
Working Voltage	1500 V_{RMS} / 2121 V_{PK}	1500 V_{RMS} / 2121 V_{PK}

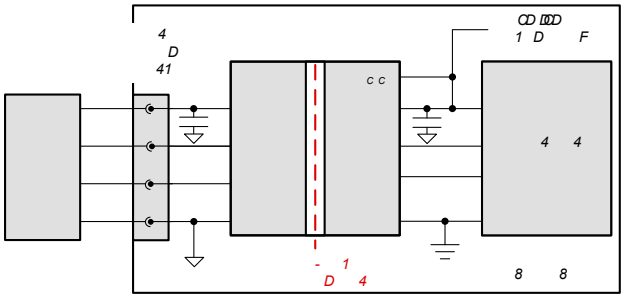
3 Description

ISOUSB211 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5 Mbps), full speed (12 Mbps) and high speed (480 Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pull-ups/ pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. The device also supports automatic role reversal - if after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. The ISOUSB211 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of up to 5700 V_{RMS} and a working voltage of 1500 V_{RMS}. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISOUSB211 device is available for both basic and reinforced isolation (see *Reinforced and Basic Isolation Options*). It supports a wide ambient temperature range of –40°C to +125°C. The device is available in the small foot-print SSOP-28 (28-DP) package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
ISOUSB211	SSOP (28) DP	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

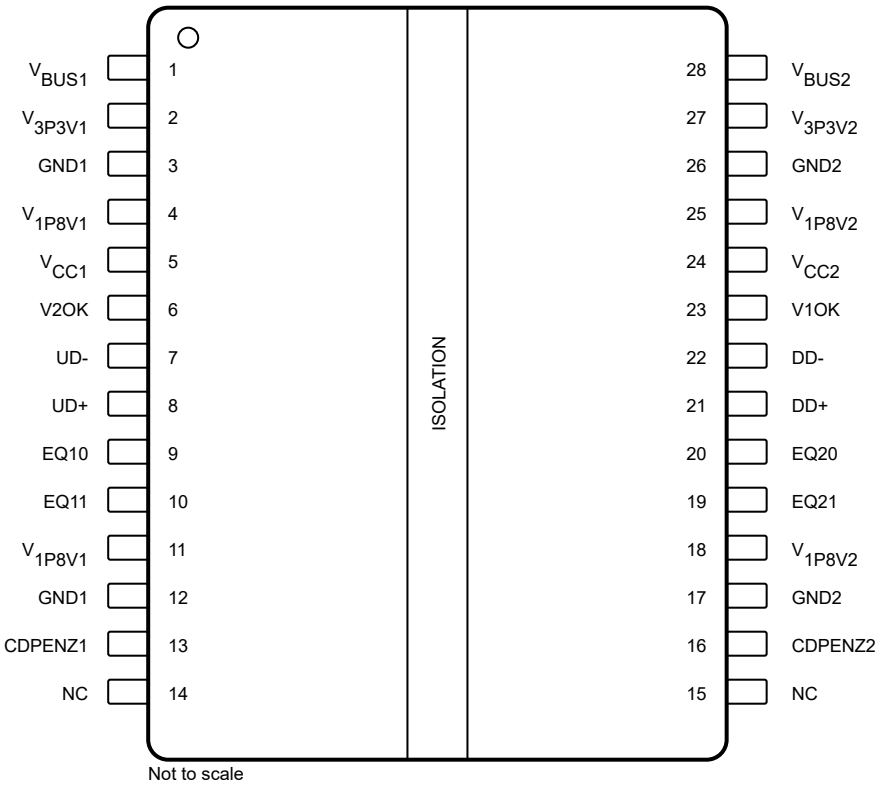
Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (March 2022)	Page
• T_A Max value updated to 125°C	5
• Updated Thermal Considerations section	28

5 Pin Configuration and Functions



Not to scale

Figure 5-1. DP Package 28-Pin SSOP Top View

Table 5-1. Pin Functions—28 Pins

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS1}. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
2	V_{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V_{BUS1} connect a bypass capacitor between V_{3P3V1} and GND1. In this case an internal LDO generates V_{3P3V1}. Else, connect V_{BUS1} and V_{3P3V1} to an external 3.3 V power supply.
3	GND1	—	Ground 1. Ground reference for Isolator Side 1.
4	V_{1P8V1}	—	Power Supply for Side 1. If a 2.35 V to 5.5 V supply is connected to V_{CC1} connect a bypass capacitor between V_{1P8V1} and GND1. In this case an internal LDO generates V_{1P8V1}. Else, connect V_{CC1} and V_{1P8V1} to an external 1.8 V power supply.
5	V_{CC1}	—	Input Power Supply for Side 1. If a 2.35 V to 5.5 V (example USB power bus, or a DC-DC supply derived from USB power bus) supply is available connect it to V_{CC1}. In this case an internal LDO generates V_{1P8V1}. Else, connect V_{CC1} and V_{1P8V1} to an external 1.8 V power supply.
6	V2OK	O	High level on this pin indicates that side 2 is powered up.
7	UD-	I/O	Upstream facing port D-.
8	UD+	I/O	Upstream facing port D+.
9	EQ10	I	Equalization setting for Side 1, LSB. Logic Input.
10	EQ11	I	Equalization setting for Side 1, MSB. Logic Input.
11	V_{1P8V1}	—	Connect pin 11 to pin 4, with local bypass capacitors near pin 11.
12	GND1	—	Ground 1. Ground reference for Isolator Side 1.
13	CDPENZ1	I	Active low singal. Enables CDP advertising on UD+/UD- pins.
14	NC	—	Leave floating or connect to V_{3P3V1}.

ADVANCE INFORMATION

Table 5-1. Pin Functions—28 Pins (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
15	NC	—	Leave floating or connect to V_{3P3V2}.
16	CDPENZ2	I	Active low singal. Enables CDP advertising on DD+/DD- pins.
17	GND2	—	Ground 2. Ground reference for Isolator Side 2.
18	V_{1P8V2}	—	Connect pin 18 to pin 25, with local bypass capacitors near pin 18.
19	EQ21	I	Equalization setting for Side 2, MSB. Logic Input.
20	EQ20	I	Equalization setting for Side 2, LSB. Logic Input.
21	DD+	I/O	Downstream facing port D+.
22	DD-	I/O	Downstream facing port D-.
23	V1OK	O	High level on this pin indicates that side 1 is powered up.
24	V_{CC2}	—	Input Power Supply for Side 2. If a 2.35 V to 5.5 V (example USB power bus, or a DC-DC supply derived from USB power bus) supply is available connect it to V_{CC2}. In this case an internal LDO generates V_{1P8V2}. Else, connect V_{CC2} and V_{1P8V2} to an external 1.8 V power supply.
25	V_{1P8V2}	—	Power Supply for Side 1. If a 2.35 V to 5.5 V supply is connected to V_{CC2} connect a bypass capacitor between V_{1P8V2} and GND2. In this case an internal LDO generates V_{1P8V2}. Else, connect V_{CC2} and V_{1P8V2} to an external 1.8 V power supply.
26	GND2	—	Ground 2. Ground reference for Isolator Side 2.
27	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
28	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS2}. In this case an internal LDO generates V_{3P3V2}. Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{BUS1}, V_{BUS2}	V_{BUS} supply voltage	-0.3	6	V
V_{CC1}, V_{CC2}	V_{CC} supply voltage	-0.3	6	V
V_{3P3V1}, V_{3P3V2}	3.3-V input supply voltage	–0.3	4.25	V
V_{1P8V1}, V_{1P8V2}	1.8-V input supply voltage	–0.3	2.1	V
V_{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cummulative duration of 1000 hrs.	–0.3	6	V
V_{IO}	IO voltage range (V*OK, EQ*, CDPENZ*)	–0.3	V_{3P3Vx}+0.3(3)	V
I_O	Output current on output pins (V*OK)	-10	10	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 4.25 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±1500	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUSx}	V_{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V_{3P3Vx}	3.3-V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
V_{CCx}	Input voltage to internal 1.8V LDO (inclusive of any ripple)	2.4	3	5.5	V
V_{1P8Vx}	1.8-V input supply voltage (inclusive of any ripple)	1.71	1.8	1.94	V
T_A	Operating free-air temperature	–40		125	°C
T_J	Junction temperature	–55		150	°C

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC(1)		ISOUSB211 DP (SSOP) 28 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	51	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	30	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOUSB211						
P_D	Maximum power dissipation (both sides)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, R_L = 50 Ω each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			1232	mW
P_{D1}	Maximum power dissipation (side-1)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, R_L = 50 Ω each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			616	mW
P_{D2}	Maximum power dissipation (side-2)	V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, R_L = 50 Ω each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			616	mW

ADVANCE INFORMATION

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
			DP-28	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8	mm
CPG	External Creepage(1)	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage ISOUSB211	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
	Maximum transient isolation voltage ISOUSB211B		4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOUSB211(3)	Test method per IEC 62368-1, 1.2/50 ms waveform, V_{TEST} = 1.6 × V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
	Maximum surge isolation voltage ISOUSB211B(3)	Test method per IEC 62368-1, 1.2/50 ms waveform, V_{TEST} = 1.3 × V_{IOSM} = 6000 V_{PK} (qualification)	4615	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, Vini = VIOTM, tini = 60 s; ISOUSB211: Vpd(m) = 1.6 × V_{IORM}, tm = 10 s ISOUSB211B: Vpd(m) = 1.2 × V_{IORM}, tm = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), Vini = V_{IOTM}, tini = 1 s; ISOUSB211: Vpd(m) = 1.875 × V_{IORM}, tm = 1 s ISOUSB211B: Vpd(m) = 1.5 × V_{IORM}, tm = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 pft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	W
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage, ISOUSB211	V_{TEST} = V_{ISO} , t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100% production)	5700	V_{RMS}
	Withstand isolation voltage, ISOUSB211B		3000	V_{RMS}

(1) Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
(2) ISOUSB211 is suitable for safe electrical insulation and ISOUSB211B is suitable for basic electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

ADVANCE INFORMATION

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN VDE V 0884-11:2017-01	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Maximum transient isolation voltage, ISOUSB211: 8000 V_{PK} ISOUSB211B: 4242 V_{PK} Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, ISOUSB211: 8000 V_{PK} (Reinforced) ISOUSB211B: 4615 V_{PK} (Basic)	IEC 62368-1 2nd Ed., for pollution degree 2, material group I ISOUSB211: 800 V_{RMS} reinforced isolation ISOUSB211B: 1000 V_{RMS} basic isolation ---------- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1+A1 ISOUSB211: 2 MOPP (Means of Patient Protection) 250 V_{RMS} (354 V_{PK}) maximum working voltage	Single protection, ISOUSB211: 5700 V_{RMS} ISOUSB211B: 3000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	EN 61010-1:2010/A1:2019 ISOUSB211: 600 V_{RMS} reinforced isolation ISOUSB211B: 1000 V_{RMS} basic isolation ---------- EN 62368-1:2014 ISOUSB211: 800 V_{RMS} reinforced isolation ISOUSB211B: 1000 V_{RMS} basic isolation
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DP-28 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =51°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			445	mA
		$R_{\theta JA}$ = 51°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			680	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 51°C/W, T_J = 150°C, T_A = 25°C			2450	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - High Speed (HS) mode	Receive side HS Active (240 MHz signal rate), EQxx = 00, R_L = 45 Ω to ground on D+ and D-		10.5	13.5	mA
		Transmit side HS Active (240 MHz signal rate), EQxx = 00, R_L= 45 Ω to ground on D+ and D-		10.5	13.5	mA
		HS Idle State, EQxx = 00, R_L = 45 Ω to ground on D+ and D-		10.5	13.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		11.5	14.8	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		9.5	13	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		9.5	13	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	9.8	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - L2 Suspend mode	Upstream Facing side		1.5	2.05	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or V_{3P3V} current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - High Speed (HS) mode	Receive side HS Active (240 MHz signal rate), EQxx = 00, R_L = 45 Ω to ground on D+ and D-		80	96	mA
		Transmit side HS Active (240 MHz signal rate), EQxx = 00, R_L = 45 Ω to ground on D+ and D-		80	96	mA
		HS Idle State, EQxx = 00, R_L = 45 Ω to ground on D+ and D-.		74	90	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		0.08	0.2	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, C_L = 50 pF		0.08	0.2	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		0.08	0.2	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, C_L = 450 pF		0.08	0.2	mA
		FS/LS Idle State		0.08	0.2	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L1 Sleep mode	Upstream Facing side		0.08	0.2	mA
		Downstream Facing side		0.08	0.2	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L2 Suspend mode	Upstream Facing side		0.25	0.45	mA
		Downstream Facing side		0.25	0.45	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Not attached	Upstream Facing side		0.08	0.2	mA
		Downstream Facing side		0.08	0.2	mA
$UV+_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V

ADVANCE INFORMATION

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UV-_{(VBUSx)}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$UVHYS_{(VBUSx)}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$UV+_{(V3P3Vx)}$	Under voltage threshold when supply voltage is rising, V_{3P3V}				2.95	V
$UV-_{(V3P3Vx)}$	Under voltage threshold when supply voltage is falling, V_{3P3V}		1.95			V
$UVHYS_{(V3P3Vx)}$	Under voltage threshold hysteresis, V_{3P3V}			0.11		V
$UV+_{(VCCx)}$ (2)	Under voltage threshold when supply voltage is rising, V_{CC}				2.35	V
$UV-_{(VCCx)}$ (2)	Under voltage threshold when supply voltage is falling, V_{CC}		2			V
$UVHYS_{(VCCx)}$ (2)	Under voltage threshold hysteresis, V_{CC}			0.05		V
$UV+_{(V1P8Vx)}$	Under voltage threshold when supply voltage is rising, V_{1P8V}				1.66	V
$UV-_{(V1P8Vx)}$	Under voltage threshold when supply voltage is falling, V_{1P8V}		1.25			V
$UVHYS_{(V1P8Vx)}$	Under voltage threshold hysteresis, V_{1P8V}			0.05		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x V_{3PV3x}			V
V_{IL}	Low-level input voltage				0.3 x V_{3PV3x}	V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	µA
I_{IL}	Low-level input current				10	µA
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_O = -3 mA for 3.0 V ≤ V_{3P3Vx} ≤ 3.6 V	V_{3P3Vx} - 0.2			V
V_{OL}	Low-level output voltage	I_O = 3 mA for 3.0 V ≤ V_{3P3Vx} ≤ 3.6 V			0.2	V
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
Z_{INP_xDx}	Impedance to GND, no pull up/down	Vin=3.6 V, V_{3P3Vx}=3.0 V, T_J < 125 °C, USB 2.0 Spec Section 7.1.6	300			kΩ
C_{IO_xDx}	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	kΩ
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	kΩ
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	kΩ
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D- with pull up enabled on upstream port with external load disconnected.	3		3.6	V
V_{HSTERM}	Termination voltage in high speed	USB 2.0 Spec Section 7.1.6.2, The output voltage in the high-speed idle state	–10		10	mV

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{HSTERM}	Driver Output Resistance (which also serves as high-speed termination)	(VOH= 0 to 600mV) USB 2.0 Spec Section 7.1.1.1 and Figure 7-5.	40.5	45	49.5	Ω
UDx, DDx, INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Host downstream port pull down resistor enabled and Device pulled up to 3.0 V - 3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V_{DI}	Differential Input Sensitivity	|(xD+)-(xD-)|; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V_{LSFS_HYS}	Differential Input Hysteresis FS/LS	|(xD+)-(xD-)|; (measured at connector) V_{CM} = 0.8 V to 2.0 V	25	75	245	mV
V_{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1, (measured at connector with RL of 0.9 kΩ to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
V_{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, Measured during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
UDx, DDx, INPUT LEVELS HS						
V_{HSSQ}	High-speed squelch/no-squelch detection threshold	USB 2.0 Spec Section 7.1.7.2 (specification refers to peak differential signal amplitude), measured at 240MHz with increasing amplitude, V_{CM}=-50mV to 500mV	100	116	150	mV
V_{HSDSC}	High-speed disconnect detection threshold $_{HSDC}$ typical values	USB 2.0 Spec Section 7.1.7.2 (specification refers to differential signal amplitude). V_{CM} = -50 mV to 500 mV	525	575	625	mV
V_{CHIRP_TH}	Chirp detection threshold	Chirp detection threshold (measured as peak differential signal amplitude). V_{CM} = -50 mV to 500 mV	100	215	365	mV
V_{HSRX}	High-speed differential input signaling levels data sensitivity	Peak-to-peak at 240 MHz			100	mV
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	USB 2.0 Spec Section 7.1.4.2, receiver should be able to receive with this common mode range	–50	200	500	mV
UDx, DDx, OUTPUT LEVELS HS						
V_{HSOH}	High-speed data signaling high	USB 2.0 Spec Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, EQxx = 00, Test load is an ideal 45 Ω to GND on D+ and D-	360	400	440	mV

ADVANCE INFORMATION

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HSOL}	High-speed data signaling low	USB 2.0 Spec Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, EQxx = 00, Test load is an ideal 45 Ω to GND on D+ and D-.	–10		10	mV
V_{HSOI}	High-speed data signaling idle, driver is off termination is on (measured single ended)	USB 2.0 Spec Section 7.1.7.2, PE disabled,Test load is an ideal 45 Ω to GND on D+ and D-.	–10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load is an ideal 45 Ω to GND on D+ and D-, with 1.5 kΩ pull-up to 3.3 V on D+.	700	900	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load is an ideal 45 Ω to GND on D+ and D-, with 1.5 kΩ pull-up to 3.3 V on D+.	–900	–700	–500	mV
U2_TX_{CM}	High-speed TX DC Common Mode	Test load is an ideal 45 Ω to GND on D+ and D-.	–50	200	500	mV
EQUALIZATION AND PRE-EMPHASIS						
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=low, 240MHz	-0.24	0.46	0.75	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=float, 240MHz	0.27	0.98	1.5	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=high, 240MHz	0.70	1.50	2.2	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=low, 240MHz	1.04	2.00	2.81	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=float, 240MHz	1.45	2.68	3.8	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=high, 240MHz	1.73	3.09	4.4	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=low, 240MHz	2.00	3.46	4.7	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=float, 240MHz	2.25	3.80	5.1	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=high, 240MHz	2.25	3.80	5.1	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=low, 240MHz	0.25	0.48	0.75	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=float, 240MHz	0.62	0.9	1.2	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=high, 240MHz	0.89	1.36	1.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=low, 240MHz	1.4	1.7	2.0	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=float, 240MHz	1.7	2.1	2.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=high, 240MHz	2.1	2.5	2.9	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=low, 240MHz	2.7	3.2	3.7	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=float, 240MHz	3.4	4.0	4.6	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=high, 240MHz	3.4	4.0	4.6	dB
CDP						
V_{DM_SRC}	VDM_SRC Voltage	Load Current in the range of 0 to 250 uA	0.5		0.7	V
I_{DP_SINK}	IDP_SINK (D+)	D+ Voltage = 0 V to 0.7 V	25		175	µA
V_{DAT_REF+}	VDAT_REF comparator rising threshold		300		400	mV
V_{DAT_REF-}	VDAT_REF comparator falling threshold		300		400	mV
$V_{DAT\_REF\_HYS}$	VDAT_REF comparator hysteresis		15	20	25	mV
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	°C
TSD-	Thermal shutdown turn-off temperature		150	160	170	°C

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_{HYS}	Thermal shutdown hysteresis			10		°C

(1) If V_{BUSx} pins are externally connected to the corresponding V_{3P3Vx} pins, then UVLO thresholds on V_{BUSx} are governed by $UV+_{(V3P3Vx)}$, $UV-_{(V3P3Vx)}$ and $UVHYS_{(V3P3Vx)}$

(2) If V_{CCx} pins are externally connected to the corresponding V_{1P8Vx} pins, then UVLO thresholds on V_{CCx} are governed by $UV+_{(V1P8Vx)}$, $UV-_{(V1P8Vx)}$ and $UVHYS_{(V1P8Vx)}$

ADVANCE INFORMATION

6.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
$T_{SUPRAMP}$	Allowed power supply ramp-up times on V_{BUSx} , V_{3P3Vx} ,V_{CCx} and V_{1P8Vx} external power supplies		0.005		100	ms
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with 5 µs power up time.		5	10	ms
UDx, DDx, HS Driver Switching Characteristics						
T_{HSR}	Rise Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, ideal 45 Ω to GND loads on D+ and D-, EQxx = 00	429	450	528	ps
T_{HSF}	Fall Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, ideal 45 Ω to GND loads on D+ and D-, EQxx = 00	426	443	526	ps
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, C_L = 50 pF	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching (T_{FR}/T_{FM})	USB 2.0 Spec 7.1.2, Excluding the first transition from the Idle state, Figure 7-9, C_L = 50 pF	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/ TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
$T_{FILTCONN}$	Debounce filter on FS or LS Connect Detection		45	70	80	µs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	µs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	µs
T_{2SUSP}	Time taken by the US side to detect suspend mode (L2) and draw less than 2.5 mA current when bus is continuously in idle state.		3		10	ms
$t_{DRESUMEL1}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	µs
$t_{DRESUMEL2}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	µs
$t_{DWAKEL1}$	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	µs
$t_{DWAKEL2}$	Maximum pulse width of remote wake that is guranteed to be detected when in suspend/L2 state.				900	µs

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DRSMPROP}$	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	V_{CM} = 1200 VPK	75	100		kV/µs
REPEATER TIMING - LS, FS						
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-20		20	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	210			ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	–6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	14			ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns
REPEATER TIMING - HS						
T_{HSSOPT}	High-speed Start of Packet Truncation	USB 2.0 spec, section 7.1.10.		6	8	UI
T_{HSEOPD}	High-speed End of Packet Dribble	USB 2.0 spec, section 7.1.13.		7	8	UI
T_{HSPD}	High-speed Propagation Delay	USB 2.0 spec, section 7.1.14.	2	3	4	ns
T_{HSTJ}	High-speed total additive jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				120	ps
T_{HSRJ}	High-speed additive random jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				35	ps
T_{HSDJ}	High-speed additive deterministic jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				82	ps

ADVANCE INFORMATION

Over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25°C, V_{BUSx} = 5 V, V_{3P3Vx} = 3.3 V, V_{1P8Vx} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HSDIS}	Time window of contiuous no transition during which the HS Disconnect Detector output must be sampled		36		82	ns
T_{FILT}	Time for which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	USB 2.0 spec, section 7.1.7.5.	2.5			µs
CDP TIMING						
T_{VDMSRC_EN}	Time taken to enable VDMSRC on D- after detecting VDPSRC connection on D+				0.1	ms
T_{VDMSRC_DIS}	Time taken to dsiable VDMSRC on D- after detecting VDPSRC disconnection on D+				0.1	ms
$T_{CON\_IDPSINK\_DIS}$	Time taken to dsiable IDP_SINK on D+ after detecting connect				0.1	ms

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

ISOUSB211 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5 Mbps), Full Speed (12 Mbps) and High Speed (480 Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB211 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal - if after disconnect, if a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. The ISOUSB211 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. High Speed (HS) Test Mode entry is also automatically detected, as required by the USB2.0 standard, to enable HS compliance tests.

ISOUSB211 is available in basic and reinforced isolation options with isolation withstand voltage of 3000 V_{RMS} and 5700 V_{RMS} respectively, and with surge test voltage of 6 kV_{PK} and 12.8 kV_{PK} respectively. The device can operate completely off a 4.25 V to 5.5 V supply (USB VBUS power) or from local 3.3-V and 1.8-supplies, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

7.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB211 is shown in Figure 7-1. The device comprises the following:

1. Transmit and receive circuits and pull-up and pull-down resistors according to the USB standard.
2. Digital logic to handle bi-directional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} and V_{1P8Vx}supplies from the V_{BUSx} and V_{CCx}supplies respectively.
4. Galvanic isolation.

ADVANCE INFORMATION

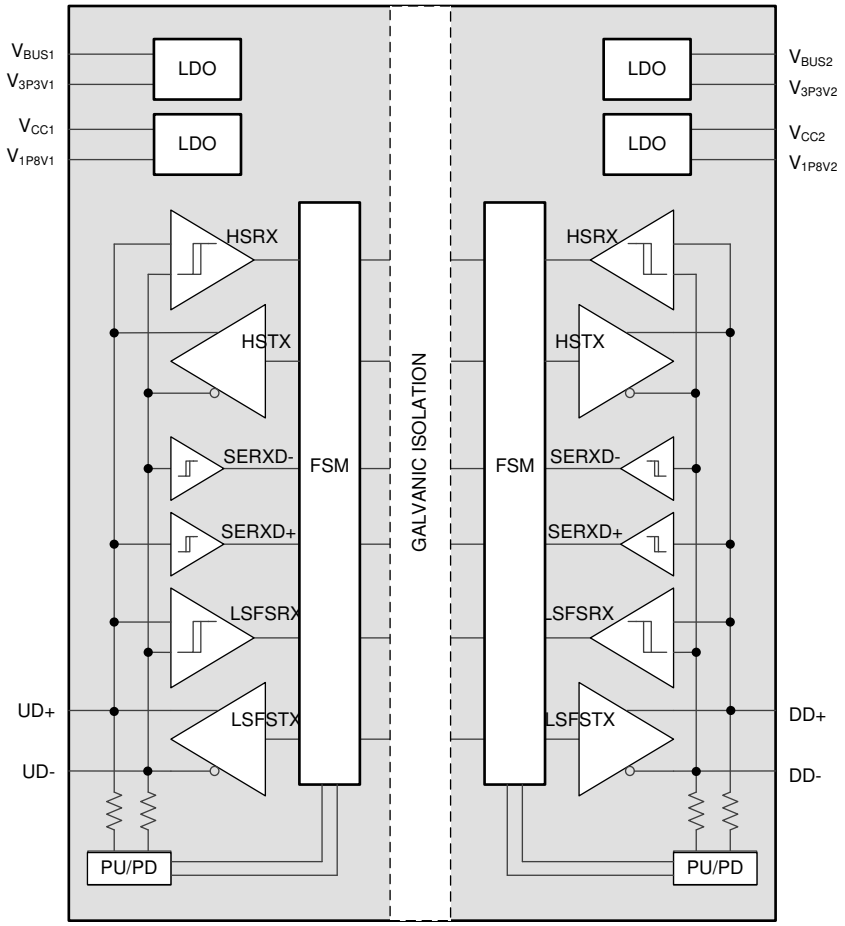


Figure 7-1. ISOUSB211 Simplified Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply Options

The ISOUSB211 can be powered by connecting a 4.25 V to 5.5 V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is suitable for the side facing the USB connector, where a 5-V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external power 3.3-V supply can be connected to both. This second option is suitable for the side facing the microcontroller, where a 5-V supply may not be available.

The ISOUSB211 also needs a 1.8-V supply for operation. A 2.4 V to 5.5 V supply can be connected on V_{CCx} pins, in which case internal LDOs generate the V_{1P8Vx} supplies. In the simplest implementation, V_{CCx} can be connected to the USB VBUS on the side facing the connector, and to the 3.3-V local supply on the side facing the microcontroller. In this implementation, there is power dissipation on the internal LDOs of ISOUSB, which limits the maximum ambient temperature supported by ISOUSB211.

To reduce power dissipation inside the ISOUSB211, an external 1.8-V supply can be connected to both V_{CCx} and V_{1P8Vx} pins shorted together, in which case the internal 1.8-V LDOs of ISOUSB211 are bypassed. In this implementation, some of the power dissipation is transferred to the external 1.8-V supply, and overall higher ambient temperature operation is achieved for the ISOUSB211. If the external 1.8-V supply is an LDO, the effect is to reduce power dissipation inside ISOUSB211, but overall no reduction in system current or power dissipation is achieved. Alternatively, if the external 1.8-V supply is a DC-DC (buck) converter, both system power and ISOUSB211 power dissipation can be reduced.

A third option is to include external resistors between VCCx pins and VBUS and 3.3-V local supplies. These resistors can be accomodated since V_{CCx} pins operate down to 2.4 V. The resistors drop voltage and dissipate

power and serve a similar purpose as external 1.8-V LDOs, that is, reduce power dissipation inside ISOUSB211 and allow higher ambient temperature operation.

Refer to the Thermal Considerations section for further details on how to optimize ISOUSB211 internal power dissipation according to the maximum ambient temperature required in the system, and for recommendations on external resistors, LDOs and buck converters.

7.3.2 Power Up

Until all power supplies on both sides of ISOUSB211 are above their respective UVLO thresholds, the device ignores any activity on the bus lines on both upstream and downstream side. Once the power supplies are above their UVLO thresholds, the device is ready to respond to activity on the bus lines. When the power supplies on side 1 are up, this is indicated on side 2 by V1OK = High. Similarly, V2OK = High indicates that Side 2 is fully powered up.

7.3.3 Symmetric Operation, Dual-Role Port and Role-Reversal

ISOUSB211 supports symmetric operation. Normally, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, it is also possible to connect UD+ and UD- to a peripheral and DD+ and DD- to a host or hub. Whichever side sees a connect first (D+ or D- pulled up to 3.3V) becomes the downstream facing side. This feature enables implementation of dual-role port (for eg. type C dual-role port) and role-reversal (for eg. OTG Host Negotiation Protocol - HNP). In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignement is swapped.

7.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB211, internal 15 kΩ pull-down resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCONN}$, the ISOUSB211 device treats this as a connect. The ISOUSB211 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB211 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB211 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

A high-speed (HS) capable device is attached to the ISOUSB211 device would proceed to perform high-speed handshake using chirp signaling as specified in the USB2.0 standard. This would be followed by chirp signals from the host. The ISOUSB211 device reflects these chirp signals across the barrier, including HS idle (SE0) states from downstream to upstream and vice versa. Upon successful completing of the HS handshake ISOUSB211 speed is set to High speed. Once set to high-speed, the speed of the repeater can only be changed after power down, HS disconnect event, or if the peripheral or host/hub do not perform HS handshake after a reset.

7.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL}threshold) for a time period higher than T_{DDIS}. Upon disconnect detection in FS and LS modes, the ISOUSB211 device removes the pull-up resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB211 then waits for the next connect event to occur.

When in High Speed (HS) mode, if the ISOUSB211 detects a continuous period of no transitions lasting T_{HSDIS}, the devices samples the DD+ and DD- lines using the HS Disconnect detector. If the input differential voltage crosses V_{HSDSC} during T_{HSDIS}, the repeater removes the HS termination from both the downstream and upstream terminals and transitions to a disconnect state. The ISOUSB211 then waits for the next connect event to occur.

ADVANCE INFORMATION

7.3.6 Reset

The ISOUSB211 device detects Reset assertion (prolonged SE0 state) on its upstream facing side, and transmits the same to the downstream facing side. In FS and LS states the reset is detected within 2.5 µs. In HS state, an extended HS idle state can be the beginning of reset, or an entry into L2 Power Management state. ISOUSB211 is able to make the distinction between the two, and accordingly either continue to drive HS idle (same as reset) on the downstream side or transition to the L2 suspend state.

7.3.7 LS/FS Message Traffic

The ISOUSB211 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till either an End-of-Packet (EOP) or a long idle is seen. At this point, the ISOUSB211 device tri-states it's LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

7.3.8 HS Message Traffic

The ISOUSB211 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the HS idle state first. Transition from HS idle state to valid HS data is detected by the HS Squelch Detector. After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till the bus returns to HS idle state, also indicated by the HS Squelch Detector. At this point, the ISOUSB211 device tri-states it's HS transmitters, and waits for the next transition from the HS idle state.

7.3.9 Equalization and Pre-emphasis

The ISOUSB211 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. These settings are controlled by EQ11 and EQ10 on side 1 and EQ21 and EQ20 on side 2. The EQxx pins can be connected to ground, connected to 3.3-V supply or left floating, together creating 9 different equalization levels. EQ11 and EQ10 can be chosen based on the length of D+/D- board trace and corresponding channel loss estimated on side 1, and similarly EQ21 and EQ20 for side 2. Typical 45-Ohm trace in FR4 has about 0.15 dB/inch for 480 Mbps signaling. Further adjustments to the EQ settings can be made by observing the transmit eye-diagram at the connector. If the trace lengths are very small, no equalization may be needed, and the EQxx pins can be connected to ground.

7.3.10 L2 Power Management State (Suspend) and Resume

The ISOUSB211 device supports L2 or Suspend low power state. Suspend mode is detected if the bus stays in the LS/FS/HS idle state for more than 3 ms. When Suspend is detected from LS and FS idle state, the ISOUSB211 continues in the LS or FS idle state, at the same time reducing internal power consumption. If Suspend is detected from HS idle state, the ISOSUB211 detects the DS port transition to FS idle state (FS J), and reflects this upstream, while disabling all high-speed circuits to reduce power consumption. The transition to the L2 low-power mode is completed within 10 ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211 followed by Resume signaling from the host/hub on the upstream facing side. Resume and Wake are signaled by a ‘K’ state. ISOUSB211 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/ Wake signaling the device returns to LS, FS or HS idle state depending on the state it was in before entering the L2 state.

7.3.11 L1 Power Management State (Sleep) and Resume

The ISOUSB211 device supports L1 or Sleep low power state. When L1 entry is detected from the LS and FS idle state, the ISOUSB211 continues in the LS or FS idle state, at the same time reducing internal power consumption. If L1 entry is detected from HS idle state, the ISOSUB211 disables all high-speed circuits to reduce power consumption. The transition to the L1 low-power mode is completed within 50 µs.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211 followed by Resume signaling from the host/hub on the upstream facing side. Resume and Wake are signaled by a 'K' state. ISOUSB211 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/ Wake signaling the device returns to LS, FS or HS idle state depending on the state it was in before entering the L1 state.

7.3.12 HS Test Mode Support

USB2.0 standards needs test mode support, where the host/hub or peripheral is expected to enter High Speed test-modes based on commands received. ISOUSB211 is able to automatically detect test mode entry to enable HS compliance tests.

7.3.13 CDP Advertising

The ISOUSB211 device supports CDP advertising on both downstream and upstream facing side according to Battery Charger standard BC 1.2. CDP advertizing is useful when isolating a host or hub, to indicate to the connected peripheral that the port is capable of supplying 1.5 A of current on VBUS. CDP advertising can be enabled by connecting the dowsnstream side CDPENZx pin to ground (active low).

7.4 Device Functional Modes

Function Table lists the functional modes for the ISOUSB211 device.

Table 7-1. Function Table

SIDE 1 SUPPLY V_{BUS1}, V_{3P3V1} V_{CC1}, V_{1P8V1} (1)	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V_{BUS2}, V_{3P3V2} V_{CC2}, V_{1P8V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and vice-versa.
Powered	15-kΩ PD	Powered	15-kΩ PD	Disconnected state is presented on both upstream and downstream
Powered	15-kΩ PD	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	Powered	15-kΩ PD	
Unpowered	Z	Unpowered	Undetermined	

(1) Powered =((V_{BUSx} ≥ $UV+_{(VBUSx)}$) || (V_{BUSx} = V_{3P3Vx} ≥ $UV+_{(V3P3Vx)}$)) & ((V_{CCx} ≥ $UV+_{(VCCx)}$) || (V_{CCx} = V_{1P8Vx} ≥ $UV+_{(V1P8Vx)}$)) ; Unpowered = ((V_{BUSx} < $UV-_{(VBUSx)}$) & (V_{3P3Vx} < $UV-_{(V3P3Vx)}$)) || ((V_{CCx} < $UV-_{(VCCx)}$) & (V_{1P8Vx} < $UV-_{(V1P8Vx)}$)); X = Irrelevant; H = High level; L = Low level; Z = High impedance

ADVANCE INFORMATION

8 Power Supply Recommendations

0.1 µF capacitors are recommended to be placed very close to V_{3P3Vx} pins to GNDx. 1-µF capacitors are recommended to be placed placed very close to V_{BUSx} pins to GNDx. 2-µF, 0.1-µF, and 10-nF capacitors are recommended to be placed between V_{1P8Vx} and GNDx, between pins 4 and 3, between pins 25 and 26, between pins 11 and 12, and between pins 25 and 26 respectively, as close to the device as possible. Place the lower value capacitors closer to the IC. If V_{CCx} pins are connected through resistors as shown in Example Configuration 3 1-µF capacitors are recommended to be placed between V_{CCx} (pins 5, 24) and GNDx (pins 3, 26), as close to the device as possible, with higher priority being accorded to the capacitors on V_{1P8Vx} pins.

These decoupling capacitor recommendations are irrespective of whether the 3.3 V and 1.8 V supplies are provided externally or generated using internal LDOs.

Refer to the Section 10.1.1 section for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins on the top layer without the use of vias. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC.

While isolating a host/hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's SN6505B. For such applications, detailed power supply design, and transformer selection recommendations are available in the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet. If CDP functionality is enabled while isolation host/hub, the isolated power supply must be capable of delivering 1.5 A on VBUS.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Isolated Host or Hub

Figure 9-1 shows an application for isolating a host or a hub using ISOUSB211. In this example, on the microntroller side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3-V supply. The V_{1P8V1} supply is generated using the internal 1.8-V LDO by providing 3.3-V supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3-V LDO. V_{CC2} and V_{1P8V2} are together connected to an external 1.8-V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the Power Supply Recommendations section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3-V local supply. Note that, for a host or hub, the USB standard requires a 120-µF capacitor to be placed on the VBUS so as to be able provide in-rush current when a downstream peripheral is attached. In addition, a 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

If the isolated power supply used is capable of providing >1.5 A current on the VBUS, the port can be configured as a CDP port according to Battery Charger specification BC 1.2. To do this, the CDPENZ2 pin of ISOUSB211

must be connected to ground as shown. Under this condition ISOUSB211 responds to BC 1.2 signaling from a connected peripheral indicating to the peripheral that the port is capable of supply 1.5-A current on VBUS.

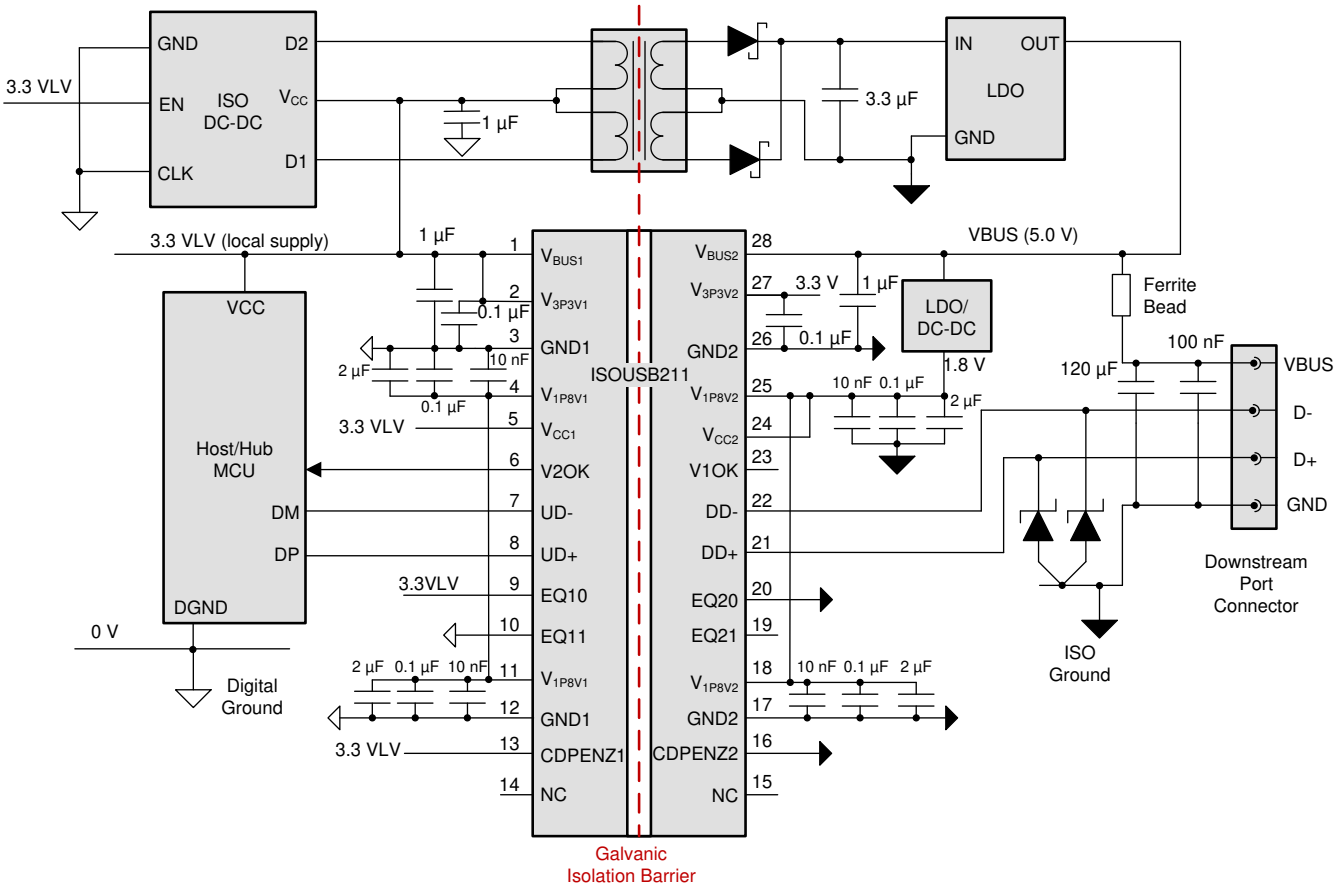


Figure 9-1. Isolated Host or Hub with ISOUSB211

9.1.2 Isolated Peripheral - Self-Powered

Figure 9-2 shows an application for isolating a self-powered peripheral using ISOUSB211. In this example, on the microntroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. The V_{1P8V2} supply is generated using the internal 1.8-V LDO by providing 3.3-V supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO. V_{CC1} and V_{1P8V1} are together connected to an external 1.8-V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

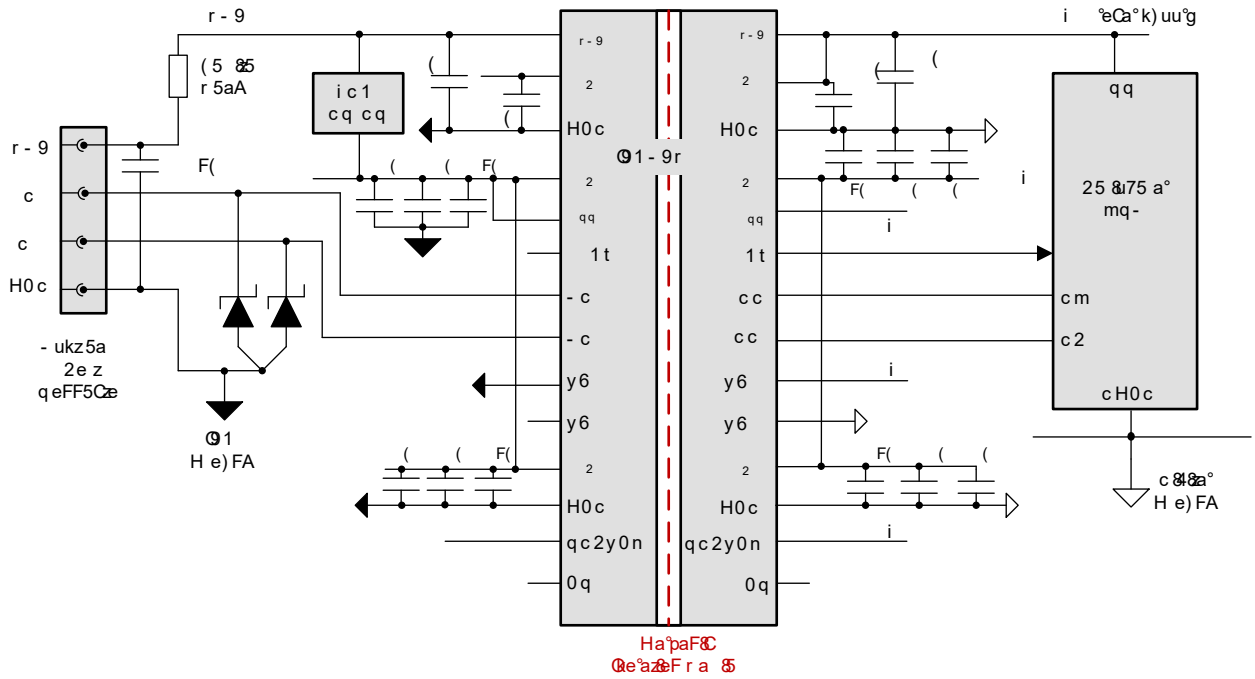


Figure 9-2. Isolated Self-Powered Peripheral with ISOUSB211

9.1.3 Isolated Peripheral - Bus-Powered

Figure 9-3 shows an application for isolating a self-powered peripheral using ISOUSB211. In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3-V local supply while deriving power from the USB VBUS. On the microntroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. The V_{1P8V2} supply is generated using the internal 1.8-V LDO by connecting the 3.3-V local supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO. V_{CC1} and V_{1P8V1} are connected together connected to an external 1.8-V supply derived from VBUS. Please refer to Thermal Considerations for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the Power Supply Recommendations section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10-µF. A 100-nF capacitor is recommended close to the VBUS pin to handle tranisent currents.

ADVANCE INFORMATION

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

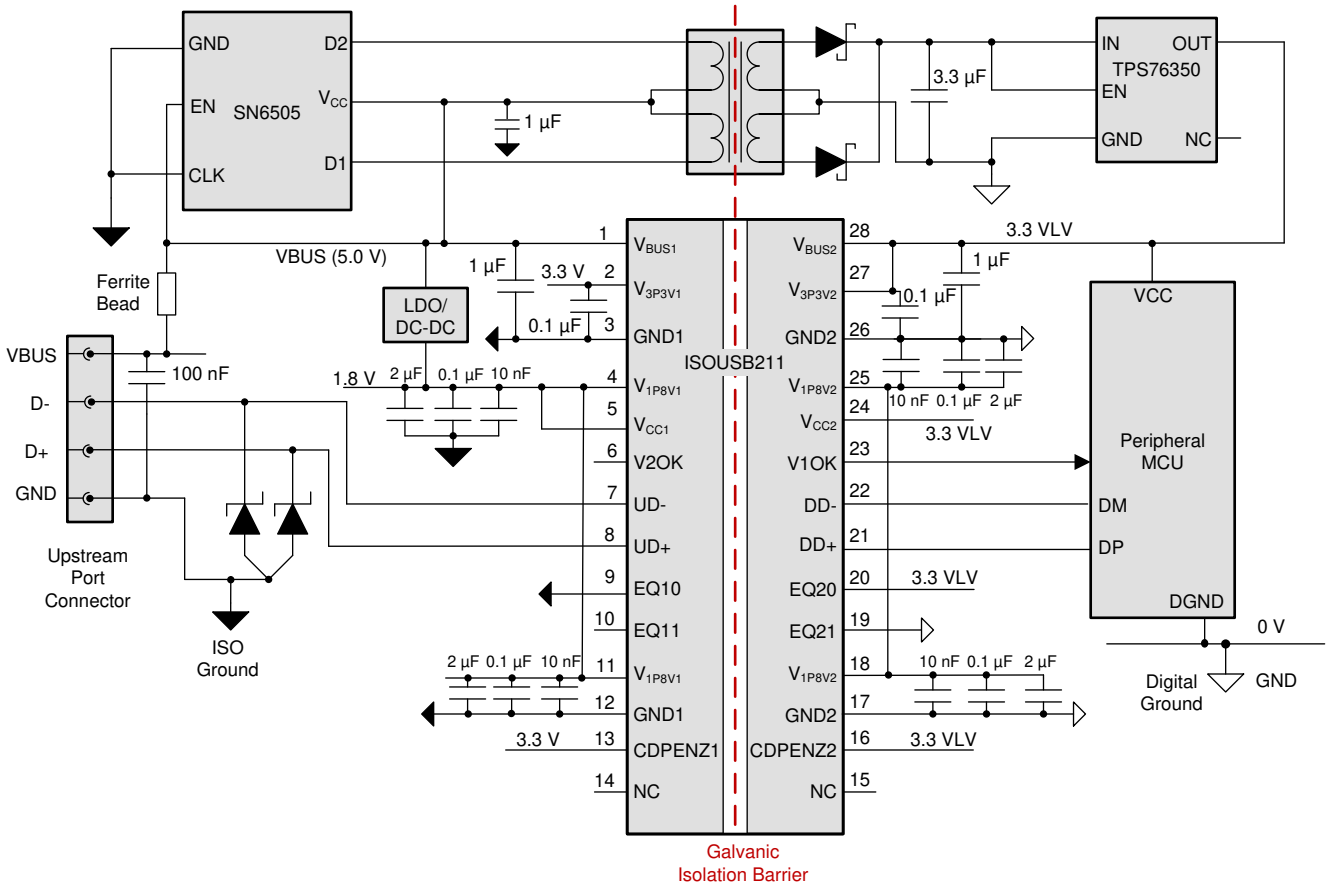


Figure 9-3. Isolated Bus-Powered Peripheral using ISOUSB211

9.1.4 Application Curve

9.1.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 9-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DP-28 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

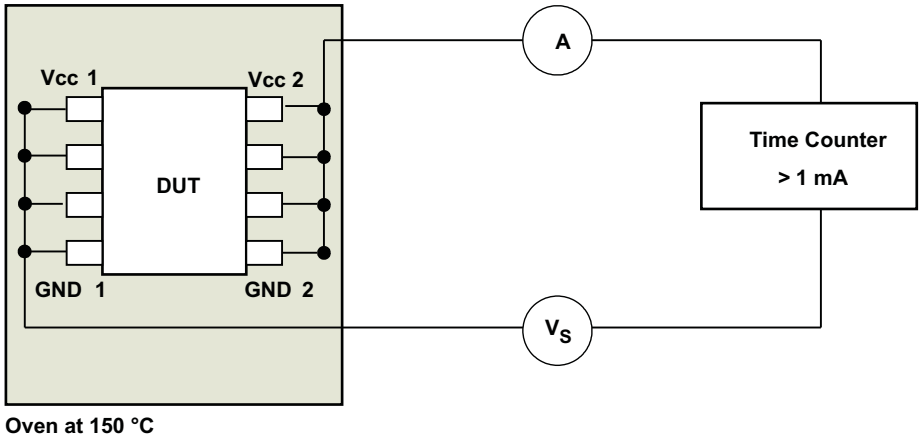


Figure 9-4. Test Setup for Insulation Lifetime Measurement

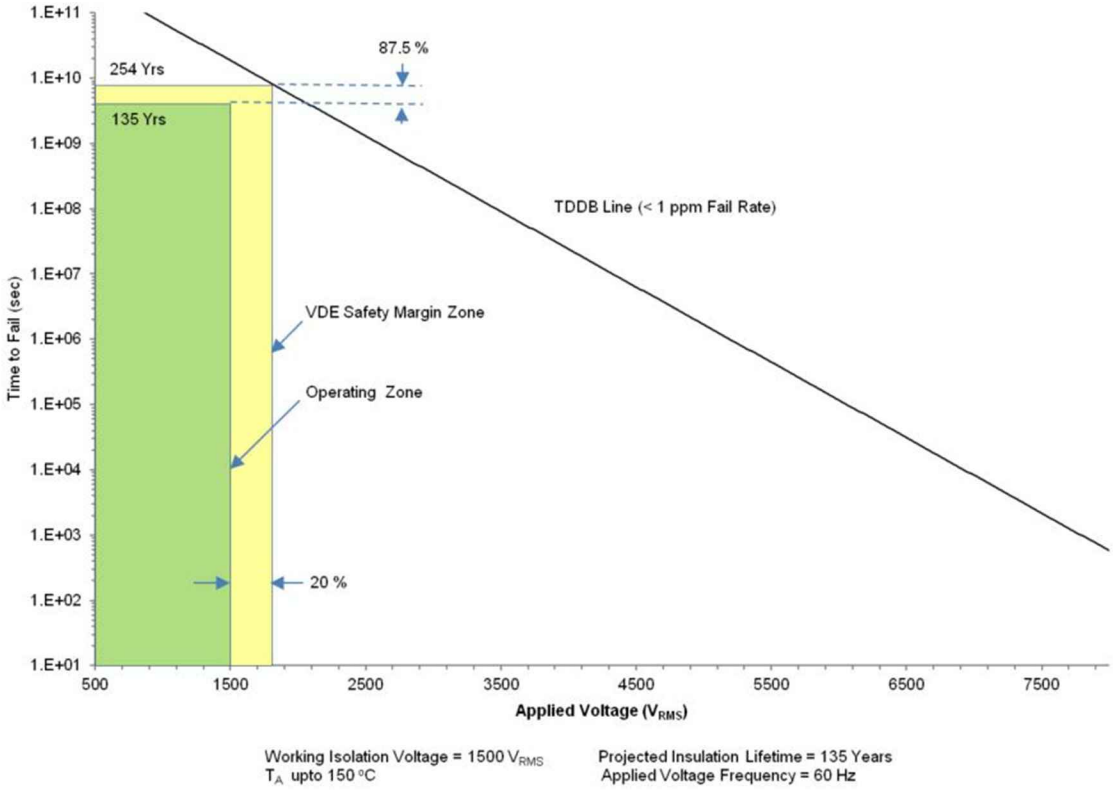


Figure 9-5. Insulation Lifetime Projection Data

9.2 Meeting USB2.0 HS Eye-Diagram Specifications

The USB2.0 standadards specifies TX and RX eye-diagram templates that must be met at the connector. The horizontal eye-opening achieved at the connector is a combination of the performance at the microcontroller, the additive jitter of the ISOUSB211, and the inter-symbol interference resulting from the insertion loss of D+/D- board traces. For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided.

The ISOUSB211 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagrams. EQ11 and EQ10 can be chosen based on the length of D+/D- board traces and corresponding channel loss estimated on side 1,

ADVANCE INFORMATION

and similarly EQ21 and EQ20 for side 2. The EQxx pins can be connected to ground, connected to 3.3-V supply or left floating, together creating 9 different equalization levels.

Typical 45-Ohm traces in FR4 have an insertion loss of about 0.15 dB/inch for 480 Mbps signaling. This number can be used to arrive at an estimate for the amount of Equalization/Pre-emphasis needed and the corresponding EQ settings. Further adjustments to the EQxx settings can be made by observing the transmit eye-diagram at the connector, and chossing the setting that gives the best eye-opening. Chosing the right setting for the transmit path will also result in an optimum performance for the receive path. If the trace lengths are very small, no equalization may be needed, and the EQxx pins can be connected to ground.

9.3 Thermal Considerations

ISOUSB211 offers different power supply input options, including internal LDOs, that can be used to optimize thermal performance in HS mode. If the 3.3-V and 1.8-V supplies are supplied using external regulators, the power dissipated inside the ISOUSB chip is lower. The internal power dissipated, when taken with the junction-to-air thermal resistance defined in the Thermal Information table can be used to determine the junction temperature for a given ambient temperature. The junction temperature must not exceed 150°C. This section describes different power supply configurations for ISOUSB211 and explains how the power dissipated inside ISOUSB211 and the internal temperature rise can be calculated in each case.

For optimal thermal performance, connect small ground planes to the GNDx pins, and connect these planes to the ground layer with multiple vias as shown in Layout Example.

9.3.1 V_{BUS} / V_{3P3V} Power

If VBUS is connected to external 5.0-V supply, with V3P3V generated through an internal LDO, the power dissipated is $V_{BUSx} \times I_{VBUSx}$.

If VBUSx and V3P3Vx are shorted together and connected to an external 3.3V supply, the power dissipated due to this supply is $V_{3P3Vx} \times I_{3P3Vx}$.

9.3.2 V_{CCx} / V_{1P8Vx} Power

If V_{CCx} is connected to external 2.4 to 5.0-V supply, with V_{1P8Vx} generated through the internal 1.8-V LDO, the power dissipated is $V_{CCx} \times I_{VCCx}$.

If V_{CCx} and V_{1P8Vx} are are shorted together and connected to an external 1.8-V supply, the power dissipated due to this supply is $V_{1P8Vx} \times I_{1P8Vx}$.

9.3.3 Example Configuration 1

In the application example shown in Figure 9-6, ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side. No other external regulators or power supplies are used.

In this scenario, the total power consumption inside ISOUSB211 from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2}$

Assuming 5.25 V as the maximum value of VBUS1, and 3.5 V as the maximum value of the 3.3-V local supply, the internal power dissipation is calculated as:

5.25 V×13.5 mA + 5.25 V×96 mA + 3.5 V×13.5 mA+3.5 V×96 mA = 960 mW.

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 49°C internal temperature rise. Ambient temperature up to 101°C can be supported for this configuration.

ADVANCE INFORMATION

This configuration offers the simplest implementation, but the ambient temperature supported is lower than other configurations.

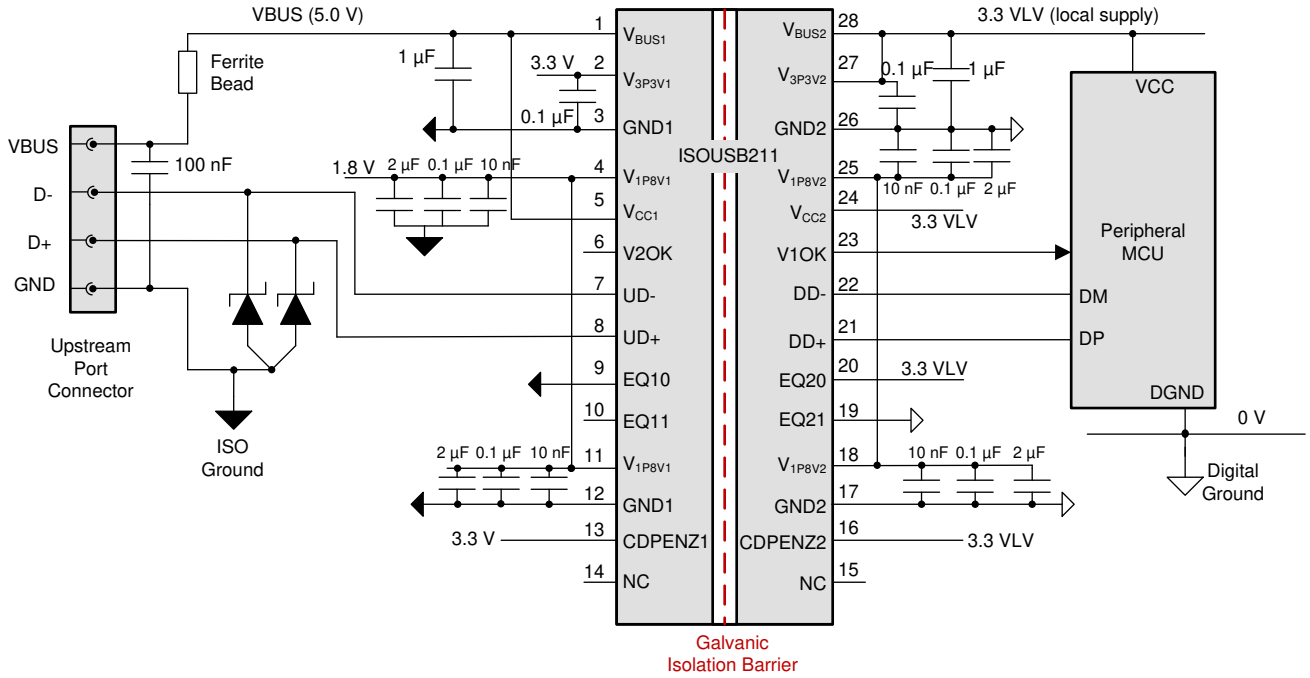


Figure 9-6. Using ISOUSB211 without External 1.8-V Regulators

9.3.4 Example Configuration 2

In the application example shown in Figure 9-7, ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side to generate V_{3P3Vx}. An external LDO or DC-DC buck converter is used to generate V_{1P8Vx} on both sides.

In this scenario, the total power consumption from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{1P8V1} \times I_{1P8V1} + V_{3P3V2} \times I_{3P3V2} + V_{1P8V2} \times I_{1P8V2}$

Assuming 5.25 V as the maximum value of VBUS, and 1.89 V as the maximum value of the external 1.8-V power supply, the internal power dissipation is calculated as

5.25 V×13.5 mA + 1.89 V×96 mA + 3.5 V×13.5 mA+1.89 V×96 mA = 481 mW.

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 25°C internal temperature rise. Ambient temperature up to 125°C can be supported for this configuration.

TLV741P and TLV62568 are examples of low-cost LDO and buck converter respectively that may be used in this application. Both options reduce the power dissipation in ISOUSB211. However, the buck converter additionally reduces power dissipation at the system level, and also the current drawn from VBUS and local 3.3-V supplies.

ADVANCE INFORMATION

This configuation offers the lowest power dissipation and the highest ambient temperature operation using external regulators.

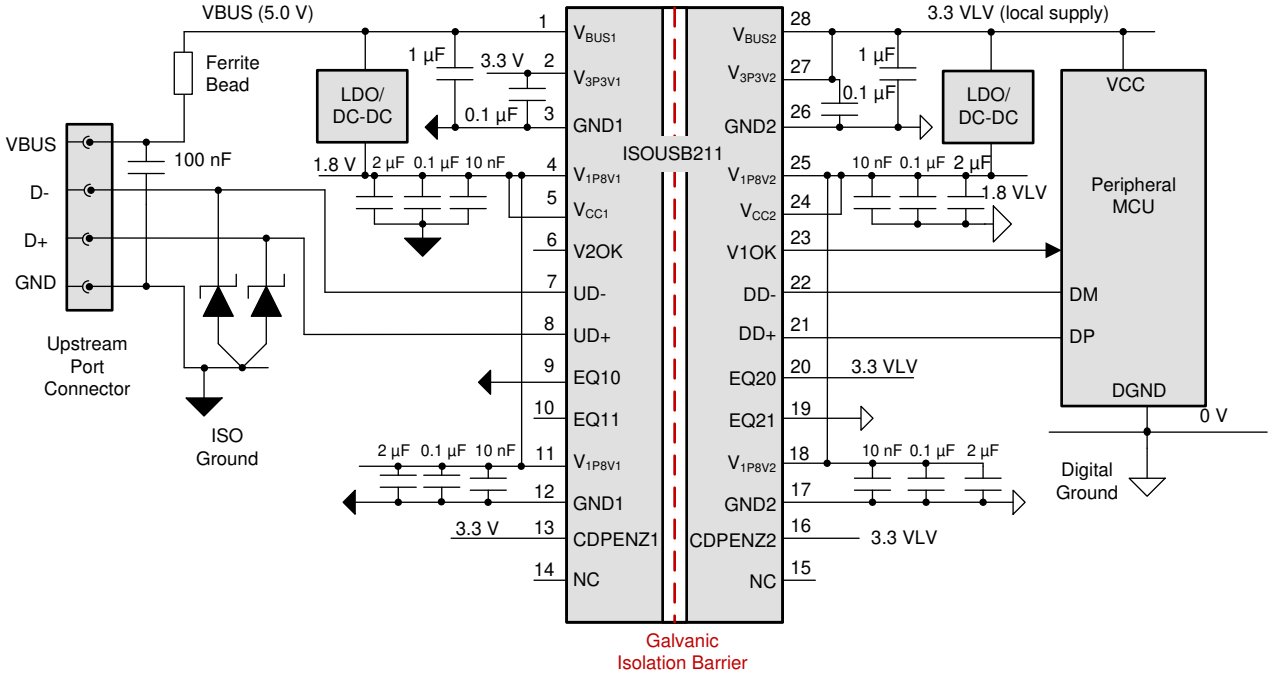


Figure 9-7. Using ISOUSB211 with 1.8-V supplied with External Regulators

9.3.5 Example Configuration 3

In the application example shown in Figure 9-8, ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side to generate V_{3P3Vx}. The internal LDOs are used to generate V_{1P8Vx} on both sides like in Example Configuration 1. However, the V_{CC1} and V_{CC2} are connected to VBUS and 3.3 VLV, not directly like in Example Configuration 1, but through resistors R1 (20 Ω, 250 mW) and R2 (5 Ω, 50 mW) respectively.

The external resistors drop voltage, and dissipate power, helping reduce the power dissipation within ISOUSB211, and the corresponding temperature rise. The resistor values are decided keeping in mind that the V_{CCx} voltage can be as low as 2.4 V. Additional 1-µF capacitors are needed on V_{CCx} pins.

In this scenario, the total power consumption inside the IC from both sides taken together is:

$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} - 20\ \Omega \times I_{VCC1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2} - 5\ \Omega \times I_{VCC2} \times I_{VCC2}$

Assuming 5.25 V as the maximum value of VBUS, and 3.5 V as the maximum value of the 3.3-V local supply, the internal power dissipation is calculated as

5.25 V×13.5 mA + 5.25 V×96 mA - 20 Ω×96 mA×96 mA + 3.5 V×13.5 mA+3.5 V×96 mA - 5 Ω×96 mA×96 mA = 728 mW.

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 38°C internal temperature rise. Ambient temperature up to 112°C can be supported for this configuration.

ADVANCE INFORMATION

This configuration offers a middle path between Example Configuration 1 and Example Configuration 2, achieving lower temperature rise, and higher ambient temperature operation, with the addition of only two resistors and two capacitors.

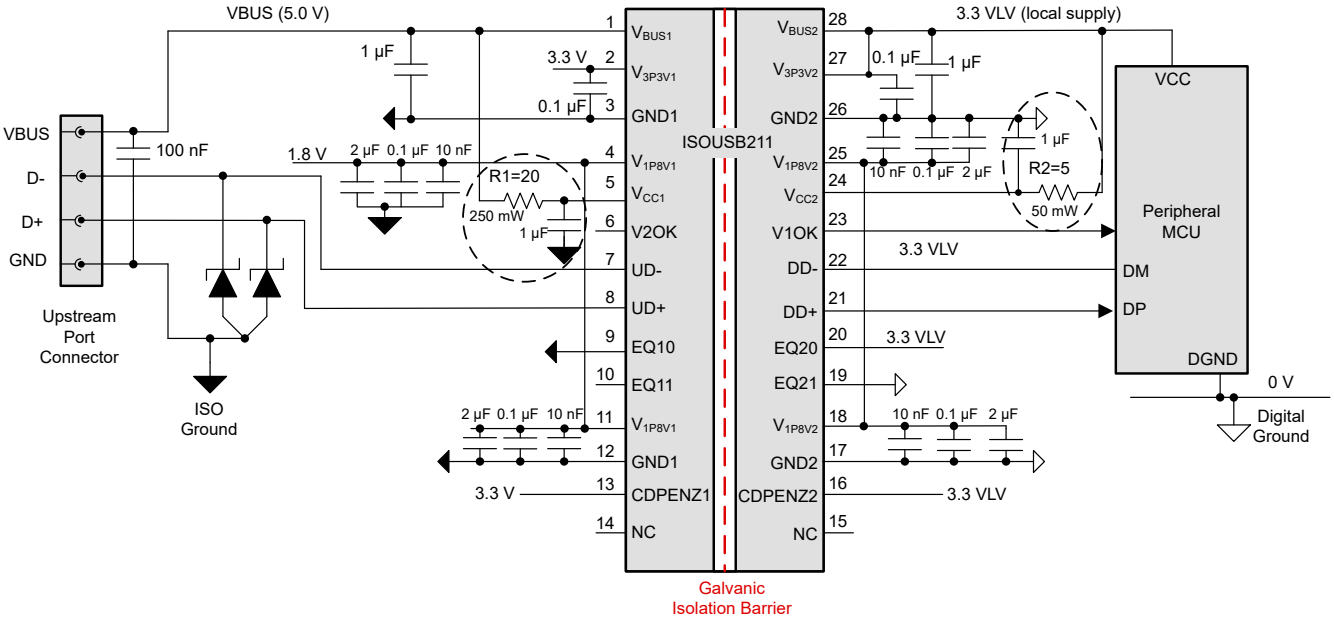


Figure 9-8. Using ISOUSB211 with Resistors in series with V_{CCx} pins

10 Layout

10.1 Layout Guidelines

Three layers are sufficient to accomplish a low EMI PCB design. Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, optional power layer, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90-Ω differential impedance and as close to 45-Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Connect a small plane (for example, 2 mm x 2 mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias. See Layout Example for details.

10.1.1 Layout Example

The layout example in this section shows the recommended placement for de-coupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC. The ESD protection diodes should be placed close to the connector with a strong connection to the ground plane. Pins 4 and 11 for V_{1P8V1} and pins 18 and 25 for V_{1P8V2} are connected together, but this connection is after the de-coupling capacitors. If more than 2 layers are available in the PCB, this connection should be made in an inner or bottom layer (ex. Layer 3 or 4) so as to not interrupt the ground plane under the D+/D- traces. The example shown is for an isolated host or hub, but similar considerations apply for isolated peripherals also. The 120-µF capacitor on VBUS only applies to host or hub and should not be used for peripherals. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed on the VBUS route, after the 100-nF (and 120-µF) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.

Connect a small plane (for example, 2 mm x 2 mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias.

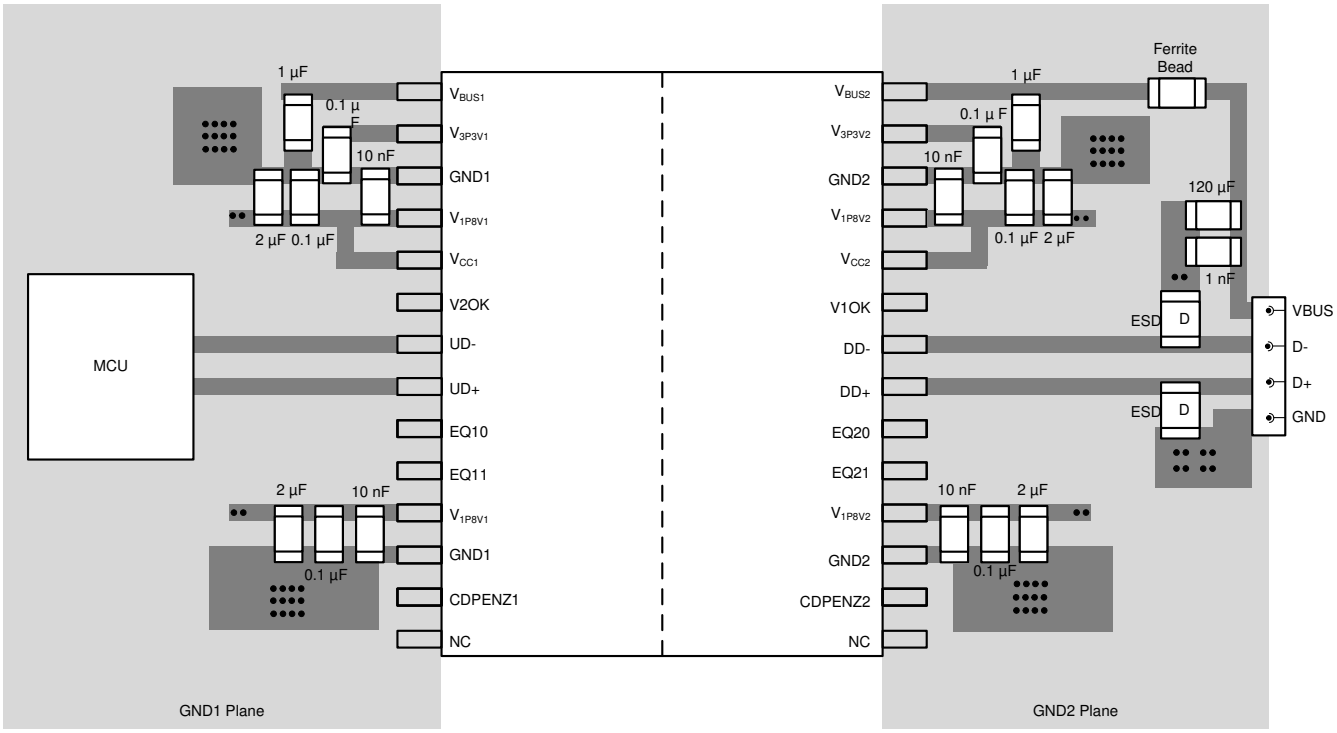


Figure 10-1. Layout Example for ISOUSB211

10.1.2 PCB Material

For digital circuit boards operating at less than 500 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

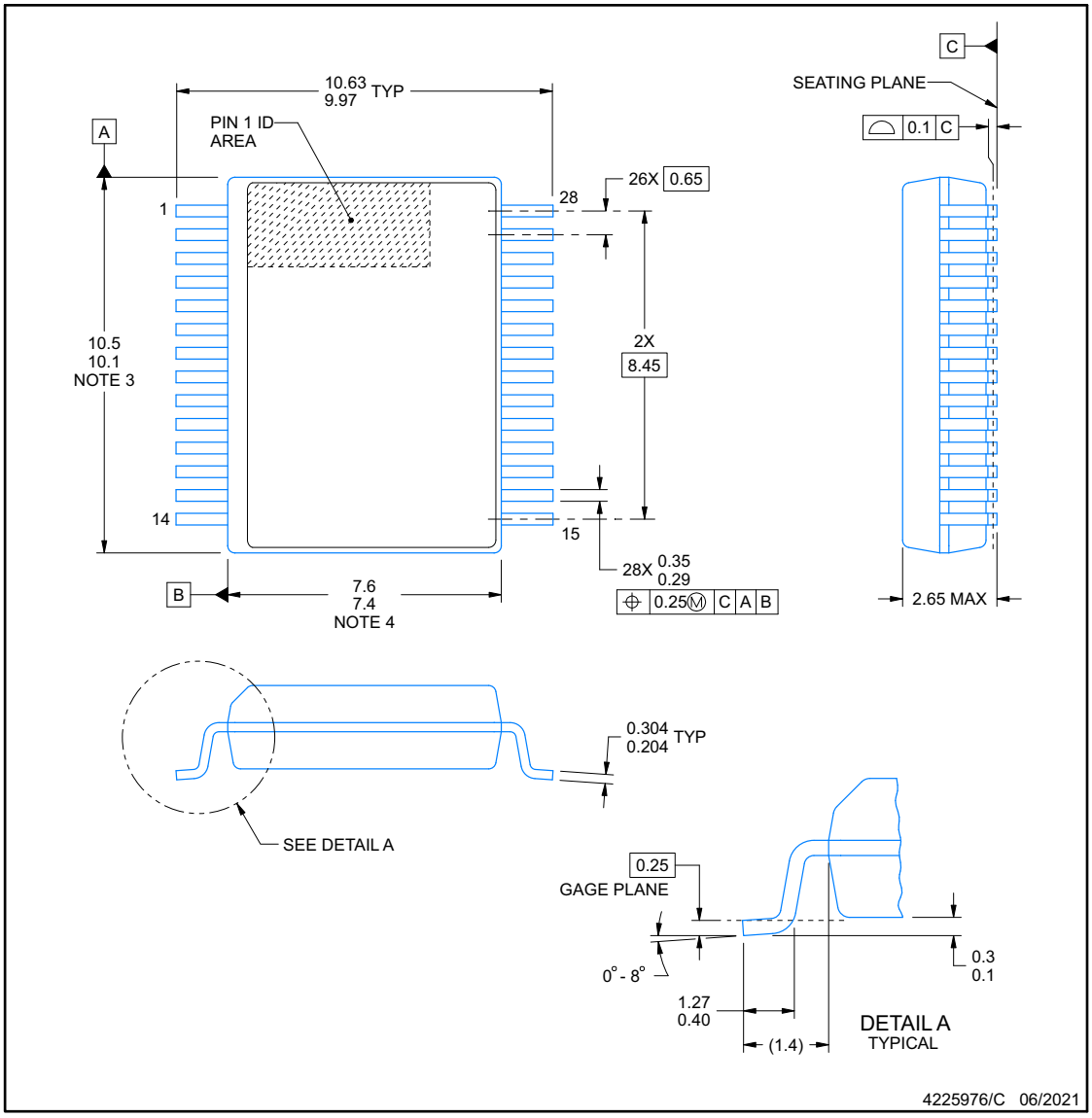
ADVANCE INFORMATION

PACKAGE OUTLINE

DP0028A

SSOP - 2.65 mm max height

SHRINK SMALL-OUTLINE PACKAGE



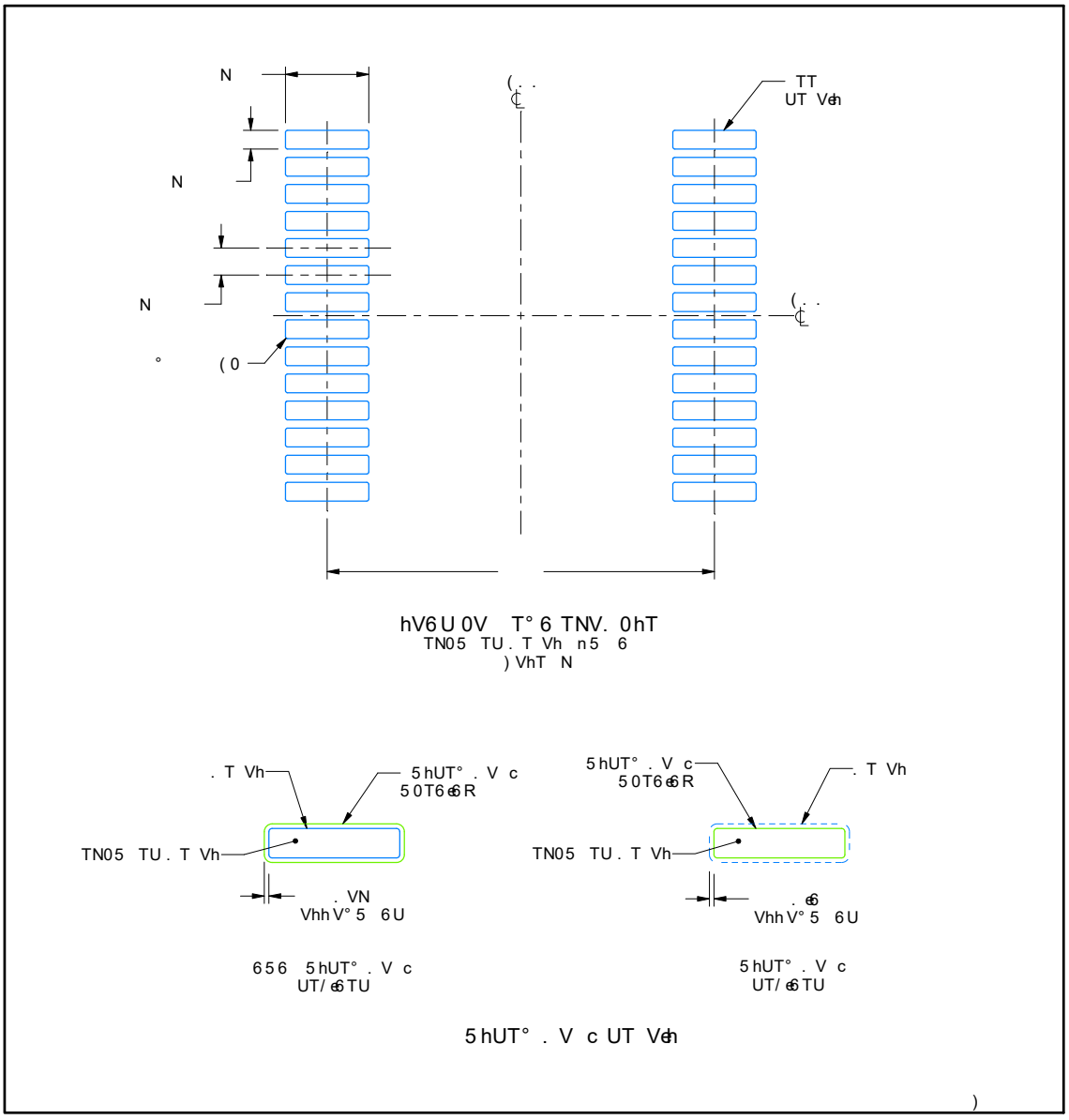
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DP0028A — SSOP - 2.65 mm max height



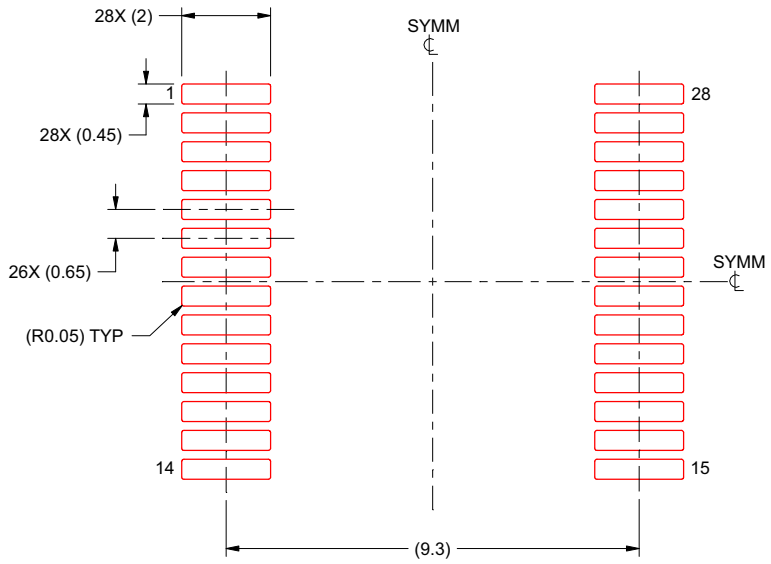
65 T 4 liCk82

0ko C4aiCl e0) am-as8 a i8xl ai8 28SC7l S
28x aS i 8xal 48So8it 88l al 2 ax kl 2 SC7l a Ca2S4al saxmoaS82 l o ax2 1aox4aiCl SC08

EXAMPLE STENCIL DESIGN

DP0028A — **SSOP - 2.65 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

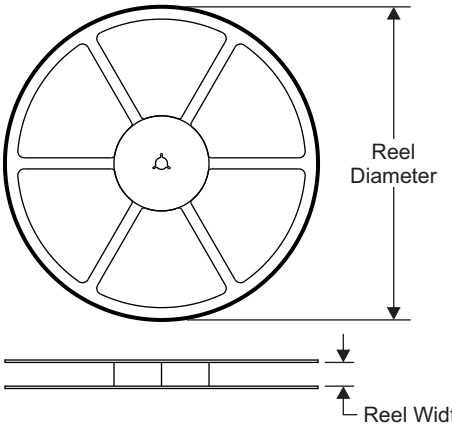
4225976/C 06/2021

NOTES: (continued)

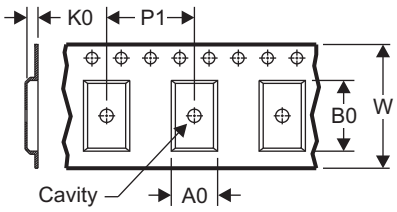
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

12.1 Tape and Reel Information

REEL DIMENSIONS

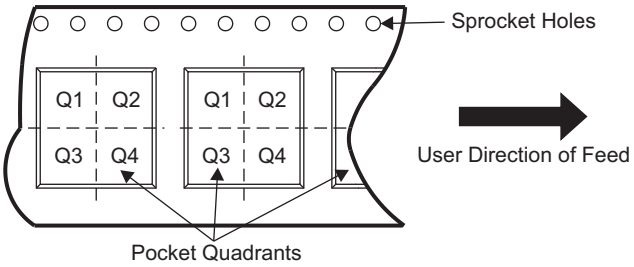


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

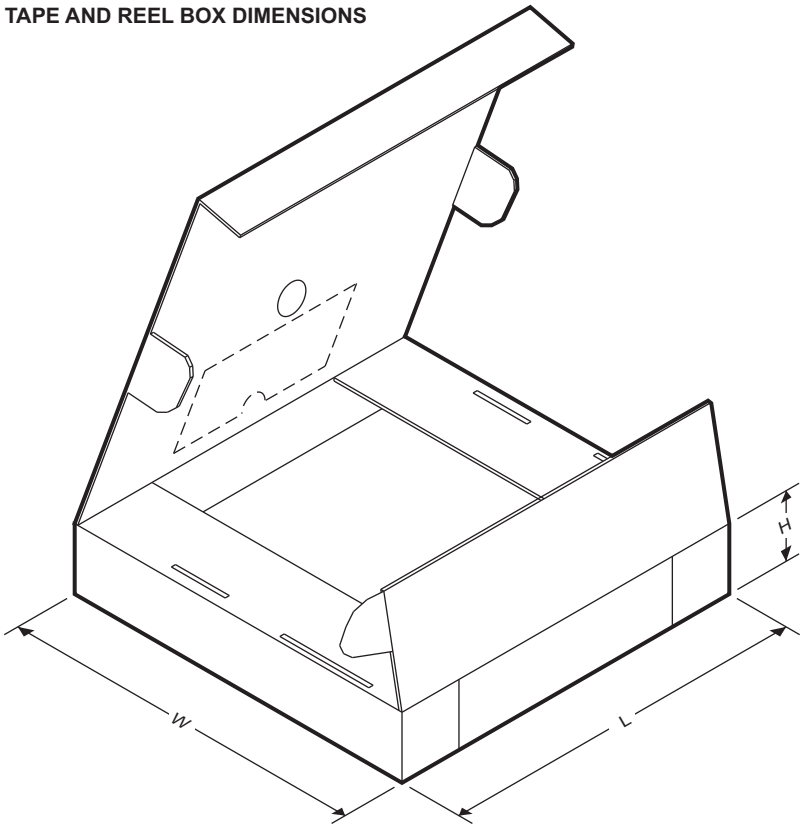
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XISOUSB211DPR	SSOP	DP	28	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XISOUSB211DPR	SSOP	DP	28	2000	350.0	350.0	43.0

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XISOUSB211DPR	ACTIVE	SSOP	DP	28	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
LM5143
SNVSC09 – MARCH 2022

LM5143 3.5-V to 65-V Dual Synchronous Buck DC/DC Controller With Ultra-Low I_Q

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Versatile synchronous buck DC/DC controller
  - Wide input voltage range of 3.5 V to 65 V
  - 1% accurate, fixed 3.3-V, 5-V, or adjustable outputs from 0.6 V to 55 V
  - 150°C maximum junction temperature
  - 4-µA typical shutdown mode current
  - 15-µA typical no-load standby current
- Two interleaved synchronous buck channels
  - Dual channel or single-output multiphase
  - 65-ns $t_{ON(min)}$ for high V_{IN}/V_{OUT} ratio
  - 60-ns $t_{OFF(min)}$ for low dropout
- Inherent protection features for robust design
  - Shunt or inductor DCR current sensing
  - Hiccup mode overcurrent protection
  - Independent ENABLE and PGOOD functions
  - Adjustable output voltage soft start
  - VCC, VDDA, and gate-drive UVLO protection
  - Thermal shutdown protection with hysteresis
- Optimized for CISPR 11 and CISPR 32 class B conducted and radiated EMI requirements
  - Slew-rate controlled adaptive gate drivers
  - Spread spectrum reduces peak emissions
- 100-kHz to 2.2-MHz switching frequency
  - SYNC in and SYNC out capability
  - Selectable diode emulation or FPWM modes
- 6-mm × 6-mm VQFN-40 package
- Create a custom design using the LM5143 with WEBENCH® Power Designer

2 Applications

- Communications systems: wireless infrastructure, remote radio unit (RRU)
- Industrial: factory automation and control, robotics
- Enterprise systems: high-performance computing

3 Description

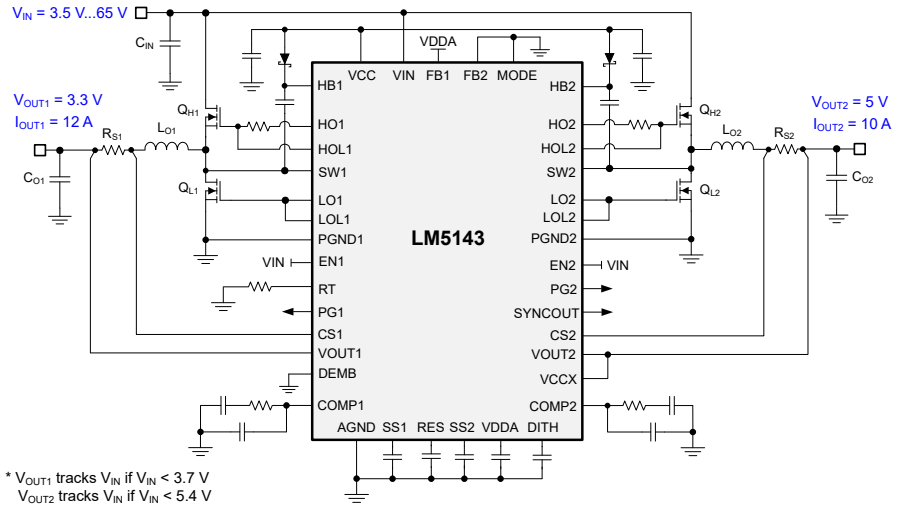
The LM5143 is a 65-V DC/DC synchronous buck controller for high-current single or dual outputs. Deriving from a family of wide-V_{IN} range controllers, the device uses an interleaved, stackable, peak current-mode control architecture for easy loop compensation, fast transient response, excellent load and line regulation, and accurate current sharing with paralleled phases for higher output current. A high-side switch minimum on time of 65 ns provides large step-down ratios, enabling the direct conversion from 12-V, 24-V, or 48-V inputs to low-voltage rails for reduced system complexity and cost. The LM5143 continues to operate during input voltage dips as low as 3.5 V, at nearly 100% duty cycle if needed.

The 15-µA no-load quiescent current with the output voltage in regulation extends operating run-time in battery-powered systems. Power the LM5143 from the output of the switching regulator or another available source for even lower input quiescent current and power loss.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM5143	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



High-Efficiency Dual Step-Down Regulator

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial release

5 Description (continued)

Several features are included to simplify compliance with CISPR 11 and CISPR 32 EMI requirements. Adaptively timed, high-current MOSFET gate drivers with adjustable slew rate control minimize body diode conduction during switching transitions, reducing switching losses and improving thermal and EMI performance at high input voltage and high switching frequency. To reduce input capacitor ripple current and EMI filter size, 180° interleaved operation is provided for two outputs. A 90° out-of-phase clock output works well for cascaded, multi-channel, or multiphase power stages. Resistor-adjustable switching frequency as high as 2.2 MHz can be synchronized to an external clock source up to 2.5 MHz to eliminate beat frequencies in noise-sensitive applications. Optional triangular spread spectrum modulation further improves the EMI signature.

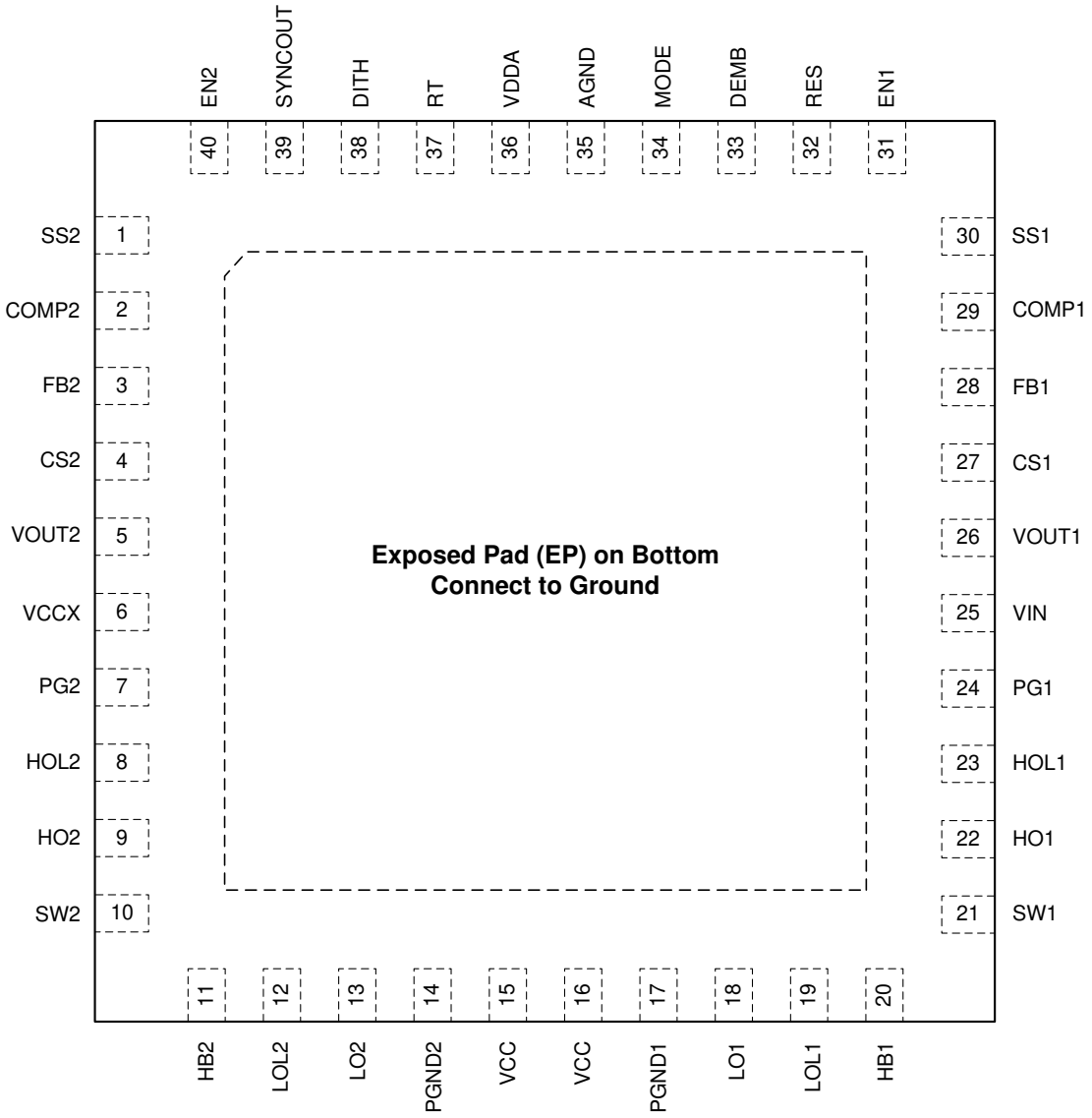
Additional features of the LM5143 include 150°C maximum junction temperature operation, user-selectable diode emulation for lower current consumption at light-load conditions, configurable soft-start functions, open-drain power-good flags for fault reporting and output monitoring, independent enable inputs, monotonic start-up into prebiased loads, an integrated VCC bias supply regulator with automatic changeover to an external bias connected at VCCX, programmable hiccup-mode overload protection, and thermal shutdown protection with automatic recovery. Current is sensed using the inductor DCR for highest efficiency or an optional shunt resistor for high accuracy.

The LM5143 controller comes in a 6-mm × 6-mm thermally enhanced, 40-pin VQFN package. The wide input voltage range, low quiescent current consumption, high-temperature operation, cycle-by-cycle current limit, low EMI signature, and small solution size provide an ideal point-of-load regulator solution for applications requiring enhanced reliability and durability.

6 Device Comparison Table

Device	Orderable Part Number	Package Drawing	Package Type	Wettable Flanks	Maximum V_{IN}
LM5143	LM5143RHAR	RHA	VQFNP	No	65 V
LM25143	LM25143RHAR	RHA	VQFNP	No	42 V

7 Pin Configuration and Functions



Connect the exposed pad on the bottom to AGND and PGND on the PCB.

Figure 7-1. 40-Pin VQFN RHA Package (Top View)

Table 7-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SS2	1	I	Channel 2 soft-start programming pin. An external ceramic capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling SS2 below 150 mV turns off the channel 2 gate driver outputs, but all the other functions remain active.
COMP2	2	O	Output of the channel 2 transconductance error amplifier. COMP2 is high impedance in single-output interleaved or single-output multiphase operation.
FB2	3	I	Feedback input of channel 2. Connect FB2 to VDDA for a 3.3-V output or connect FB2 to AGND for a fixed 5-V output. A resistive divider from VOUT2 to FB2 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB2 is 0.6 V.
CS2	4	I	Channel 2 current sense amplifier input. Connect CS2 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
VOUT2	5	I	Output voltage sense and the current sense amplifier input of channel 2. Connect VOUT2 to the output side of the channel 2 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
VCCX	6	P	Optional input for an external bias supply. If V_{VCCX} > 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Connect a ceramic capacitor between VCCX and PGND.
PG2	7	O	An open-collector output that goes low if VOUT2 is outside a specified regulation window
HOL2	8	O	Channel 2 high-side gate driver turn-off output
HO2	9	O	Channel 2 high-side gate driver turn-on output
SW2	10	P	Switching node of the channel 2 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
HB2	11	P	Channel 2 high-side driver supply for the bootstrap gate drive
LOL2	12	O	Channel 2 low-side gate driver turn-off output
LO2	13	O	Channel 2 low-side gate driver turn-on output
PGND2	14	G	Power-ground connection pin for the low-side NMOS gate driver
VCC	15, 16	P	VCC bias supply pin. Pins 15 and 16 must to be connected together on the PCB. Connect ceramic capacitors between VCC and PGND1 and between VCC and PGND2.
PGND1	17	G	Power-ground connection pin for the low-side NMOS gate driver
LO1	18	O	Channel 1 low-side gate driver turn-on output
LOL1	19	O	Channel 1 low-side gate driver turn-off output
HB1	20	P	Channel 1 high-side driver supply for the bootstrap gate drive
SW1	21	P	Switching node of the channel 1 buck regulator. Connect to the channel 1 bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
HO1	22	O	Channel 1 high-side gate driver turn-on output
HOL1	23	O	Channel 1 high-side gate driver turn-off output
PG1	24	O	An open-collector output that goes low if VOUT1 is outside a specified regulation window
VIN	25	P	Supply voltage input source for the VCC regulators
VOUT1	26	I	Output voltage sense and the current sense amplifier input of channel 1. Connect VOUT1 to the output side of the channel 1 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
CS1	27	I	Channel 1 current sense amplifier input. Connect CS1 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
FB1	28	I	Feedback input of channel 1. Connect the FB1 pin to VDDA for a 3.3-V output or connect FB1 to AGND for a 5-V output. A resistive divider from VOUT1 to FB1 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB1 is 0.6 V.
COMP1	29	O	Output of the channel 1 transconductance error amplifier (EA)
SS1	30	I	Channel 1 soft-start programming pin. An external capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling the SS1 voltage below 150 mV turns off the channel 1 gate driver outputs, but all the other functions remain active.

Table 7-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN1	31	I	An active high input (V_{EN1} > 2 V) enables output 1. If outputs 1 and 2 are disabled, the LM5143 is in shutdown mode unless a SYNC signal is present at DEMB. EN1 must never be floating.
RES	32	O	Restart timer pin. An external capacitor configures the hiccup-mode current limiting. A capacitor at the RES pin determines the time the controller remains off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel can operate in normal mode while the other is in hiccup-mode overload protection. Hiccup mode commences when either channel experiences 512 consecutive PWM cycles with cycle-by-cycle current limiting. Connect RES to VDDA during power up to disable hiccup-mode protection.
DEMB	33	I	Diode emulation pin. Connect DEMB to AGND to enable diode emulation mode. Connect DEMB to VDDA to operate the LM5143 in forced PWM (FPWM) mode with continuous conduction at light loads. DEMB can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
MODE	34	I	Connect MODE to AGND or VDDA for dual-output or interleaved single-output operation, respectively. This also configures the LM5143 with an EA transconductance of 1200 µS. Connecting a 10-kΩ resistor between MODE and AGND sets the LM5143 for dual-output operation with an ultra-low I_Q mode and an EA transconductance of 60 µS.
AGND	35	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits
VDDA	36	O	Internal analog bias regulator output. Connect a ceramic decoupling capacitor from VDDA to AGND.
RT	37	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100 kHz and 2.2 MHz.
DITH	38	I	A capacitor connected between the DITH pin and AGND is charged and discharged with a 20-µA current source. If dithering is enabled, the voltage on the DITH pin ramps up and down modulating the oscillator frequency between –5% and +5% of the internal oscillator. Connecting DITH to VDDA during power up disables the dither feature. DITH is ignored if an external synchronization clock is used.
SYNCOUT	39	O	SYNCOUT is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM5143 controller, all phases are 90° out of phase.
EN2	40	I	An active high input (V_{EN2} > 2 V) enables output 2. If outputs 1 and 2 are disabled, the LM5143 is in shutdown mode unless a SYNC signal is present on DEMB. EN2 must never be floating.

(1) P = Power, G = Ground, I = Input, O = Output

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	70	V
	SW1, SW2 to PGND	–0.3	70	
	SW1, SW2 to PGND (20-ns transient)	–5		
	HB1 to SW1, HB2 to SW2	–0.3	6.5	
	HB1 to SW1, HB2 to SW2 (20-ns transient)	–5		
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3	V_{HB} + 0.3	
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2 (20-ns transient)	–5		
	LO1, LOL1, LO2, LOL2 to PGND	–0.3	V_{VCC} + 0.3	
	LO1, LOL1, LO2, LOL2 to PGND (20-ns transient)	–1.5	V_{VCC} + 0.3	
	SS1, SS2, COMP1, COMP2, RES, RT, MODE, DITH to AGND	–0.3	V_{VDDA} + 0.3	
	EN1, EN2 to PGND	–0.3	70	
	VCC, VCCX, VDDA, PG1, PG2, DEMB, FB1, FB2 to AGND	–0.3	6.5	
	VOUT1, VOUT2, CS1, CS2 to AGND	–0.3	60	
	VOUT1 to CS1, VOUT2 to CS2	–0.3	0.3	
PGND to AGND		–0.3	0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent damage to the device. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operation Condition. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JESD22 JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN to PGND	–0.3		65	V
		SW1, SW2 to PGND	–0.3		65	
		HB1 to SW1, HB2 to SW2	–0.3	5	5.25	
		HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3		V_{HB} + 0.3	
		LO1, LOL1, LO2, LOL2 to PGND	–0.3	5	5.25	
		FB1, FB2, SS1, SS2, COMP1, COMP2, RES, DEMB, RT, MODE, DITH to AGND	–0.3		5.25	
		EN1, EN2 to PGND	–0.3		65	
		VCC, VCCX, VDDA to PGND	–0.3	5	5.25	
		VOUT1, VOUT2, CS1, CS2 to PGND	–0.3		55	
	PGND to AGND		–0.3		0.3	
T_J	Operating junction temperature		–40		150	°C

8.4 Thermal Information

THERMAL METRIC[1]		RHA (VQFNP)	UNIT
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{SHUTDOWN}$	Shutdown mode current	V_{EN1} = V_{EN2} = 0 V		3.5	7	µA
$I_{STANDBY1}$	Standby current, channel 1	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no load, not switching, DEMB = MODE = GND		24		µA
$I_{STANDBY2}$	Standby current, channel 2	V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no load, not switching, DEMB = MODE = GND		25		µA
$I_{STANDBY3}$	Standby current, channel 1, ultra-low I_Q mode	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to GND		16.5		µA
$I_{STANDBY4}$	Standby current, channel 2, ultra-low I_Q mode	V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to GND		21		µA
BIAS REGULATOR (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 100 mA, V_{VCCX} = 0 V	4.7	5	5.3	V
$V_{CC-UVLO}$	VCC UVLO rising threshold	V_{VCC} rising	3.2	3.3	3.4	V
$V_{VCC-HYST}$	VCC UVLO hysteresis			182		mV
$I_{VCC-LIM}$	VCC sourcing current limit			235		mA
ANALOG BIAS (VDDA)						
$V_{VDDA-REG}$	VDDA regulation voltage		4.75	5	5.25	V
$V_{VDDA-UVLO}$	VDDA UVLO rising threshold	V_{VCC} rising, V_{VCCX} = 0 V	3.1	3.2	3.3	V
$V_{VDDA-HYST}$	VDDA UVLO hysteresis	V_{VCCX} = 0 V		90		mV
R_{VDDA}	VDDA resistance	V_{VCCX} = 0 V		20		Ω
EXTERNAL BIAS (VCCX)						
$V_{VCCX-ON}$	$VCCX_{(ON)}$ rising threshold		4.1	4.3	4.4	V
R_{VCCX}	VCCX resistance	V_{VCCX} = 5 V		1.2		Ω
$V_{VCCX-HYST}$	VCCX hysteresis voltage			130		mV
CURRENT LIMIT (CS1, CS2)						
V_{CS1}	Current limit threshold 1	Measured from CS1 to VOUT1	66	73	82	mV
V_{CS2}	Current limit threshold 2	Measured from CS2 to VOUT2	66	73	82	mV
$t_{CS-DELAY}$	CS delay to output			40		ns
G_{CS}	CS amplifier gain		11.25	12	12.6	V/V
$I_{CS-BIAS}$	CS amplifier input bias current				15	nA
POWER GOOD (PG1, PG2)						
$PG1_{UV}$	PG1 UV trip level	Falling with respect to the regulation voltage	89.5%	92%	94%	
$PG2_{UV}$	PG2 UV trip level	Falling with respect to the regulation voltage	89.5%	92%	94%	
$PG2_{OV}$	PG2 OV trip level	Rising with respect to the regulation voltage	107.5%	110%	112.5%	
$PG2_{OV}$	PG2 OV trip level	Rising with respect to the regulation voltage	107.5%	110%	112.5%	
$PG1_{UV-HYST}$	PG1 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG1_{OV-HYST}$	PG1 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{UV-HYST}$	PG2 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{OV-HYST}$	PG2 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
V_{OL-PG1}	PG1 voltage	Open collector, I_{PG1} = 2 mA			0.4	V
V_{OL-PG2}	PG2 voltage	Open collector, I_{PG2} = 2 mA			0.4	V

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PG-RISE-DLY}$	OV filter time	V_{OUT} rising		25		µs
$t_{PG-FALL-DLY}$	UV filter time	V_{OUT} falling		22		µs
HIGH-SIDE GATE DRIVER (HO1, HO2, HOL1, HOL2)						
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100 mA		0.04		V
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100 mA, $V_{HO-HIGH}$ = V_{HB} – V_{HO}		0.09		V
$t_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		24		ns
$t_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		24		ns
I_{HO-SRC}	HO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{HO-SINK}$	HO peak sink current	V_{VCCX} = 5 V		4.25		A
V_{BT-UV}	BOOT UVLO	V_{VCC} falling		2.45		V
$V_{BT-UV-HYS}$	BOOT UVLO hysteresis			113		mV
I_{BOOT}	BOOT quiescent current			1.25		µA
LOW-SIDE GATE DRIVER (LO1, LO2, LOL1, LOL2)						
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100 mA		0.04		V
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100 mA		0.07		V
$t_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		4		ns
$t_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		3		ns
$I_{LO-SOURCE}$	LO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{LO-SINK}$	LO peak sink current	V_{VCCX} = 5 V		4.25		A
RESTART (RES)						
$I_{RES-SRC}$	RES current source			20		µA
V_{RES-TH}	RES threshold			1.2		V
HIC_{CYCLES}	HICCUP mode fault			512		cycles
R_{RES-PD}	RES pulldown resistance			5.7		Ω
OUTPUT VOLTAGE SETPOINT (VOUT1, VOUT2)						
$VOUT_{33}$	3.3-V output voltage setpoint	FB = VDDA, V_{IN} = 3.5 V to 65 V	3.267	3.3	3.335	V
$VOUT_{50}$	5-V output voltage setpoint	FB = AGND, V_{IN} = 5.5 V to 65 V	4.95	5	5.05	V
FEEDBACK (FB1, FB2)						
$V_{FB-3V3-SEL}$	VOUT select threshold 3.3-V output		4.6			V
R_{FB-5V}	Resistance FB to AGND for 5-V output	V_{MODE} = 0 V or R_{MODE} = 10 kΩ			500	Ω
$R_{FB-EXTRES}$	Thevenin equivelent resistance	V_{MODE} = 0 V or R_{MODE} = 10 kΩ, V_{FB} < 2 V	5			kΩ
$V_{FB2-LOW}$	Primary mode select logic level low	MODE = VDDA			0.8	V
$V_{FB2-HIGH}$	Primary mode select logic level high	MODE = VDDA	2			V
$V_{FB1-LOW}$	Diode emulation logic level low in secondary mode	MODE = FB2 = VDDA			0.8	V
$V_{FB1-HIGH}$	FPWM logic level high in secondary mode	MODE = FB2 = VDDA	2			V
V_{FB-REG}	Regulated feedback voltage	T_J = –40°C to 125°C	0.594	0.6	0.606	V
ERROR AMPLIFIER (COMP1, COMP2)						
g_{m1}	EA transconductance	FB to COMP, R_{MODE} < 5 kΩ to AGND	1020	1200		µs
g_{m2}	EA transconductance, ultra-low I_Q mode	MODE = GND, R_{MODE} = 10 kΩ		65		µs
I_{FB}	Error amplifier input bias current				30	nA
$V_{COMP-CLMP}$	COMP clamp voltage	V_{FB} = 0 V		3.3		V

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{COMP-SECOND}$	COMP leakage, secondary mode	V_{COMP} = 1 V, MODE = FB2 = VDDA			10	nA
$I_{COMP-INTLV}$	COMP2 leakage, interleaved mode	V_{COMP} = 1 V, MODE = VDDA, V_{FB2} = 0 V			10	nA
$I_{COMP-SRC1}$	EA source current	V_{COMP} = 1 V, V_{FB} = 0.4 V, V_{MODE} = 0 V		190		µA
$I_{COMP-SINK1}$	EA sink current	V_{COMP} = 1 V, V_{FB} = 0.8 V, V_{MODE} = 0 V		160		µA
$I_{COMP-SRC2}$	EA source current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.4 V, R_{MODE} = 10 kΩ to AGND		10		µA
$I_{COMP-SINK2}$	EA sink current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.8 V, R_{MODE} = 10 kΩ to AGND		12		µA
$V_{SS-OFFSET}$	EA SS offset with V_{FB} = 0 V	Raise V_{SS} until V_{COMP} > 300 mV		36		mV
ADAPTIVE DEADTIME CONTROL						
V_{GS-DET}	VGS detection threshold	VGS falling, no load		2.1		V
t_{DEAD1}	HO off to LO on dead time			22		ns
t_{DEAD2}	LO off to HO on dead time			20		ns
DIODE EMULATION (DEMB)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V
V_{DEMB_Rising}	DEMB input high threshold		2			V
V_{ZC-SW}	Zero-cross threshold	V_{DEMB} = 0 V		–7		mV
V_{ZC-SS}	Zero-cross threshold soft start	DEMB = VDDA, 50 SW cycles after first HO pulse		–6.1		mV
V_{ZC-DIS}	Zero-cross threshold disabled	DEMB = VDDA, 1000 SW cycles after first HO pulse		210		mV
ENABLE (EN1, EN2)						
V_{EN-LOW}	EN1/2 low threshold	V_{VCCX} = 0 V			0.8	V
$V_{EN-HIGH-TH}$	EN1/2 high threshold	V_{VCCX} = 0 V	2			V
$I_{EN-LEAK}$	EN1/2 leakage currernt	EN1, EN2 logic inputs only		0.05		µA
SWITCHING FREQUENCY (RT)						
V_{RT}	RT regulation voltage	10 kΩ < R_{RT} < 220 kΩ		0.8		V
MODE						
$R_{MODE-HIGH}$	Resistance to AGND for ultra-low I_Q		5			kΩ
$R_{MODE-LOW}$	Resistance to AGND for normal I_Q				0.5	kΩ
$V_{MODE-LOW}$	Non-interleaved mode input low threshold				0.8	V
$V_{MODE-HIGH}$	Interleaved mode input high threshold		2			V
SYNCHRONIZATION INPUT (SYNCIN)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V
$V_{DEMB-HIGH}$	DEMB input high threshold		2			V
$t_{SYNC-MIN}$	DEMB minimum pulse width	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	20		250	ns
F_{SYNCIN}	External SYNC frequency range	V_{IN} = 8 V to 18 V, % of the nominal frequency set by R_{RT}	–20%		20%	
$t_{SYNCIN-HO1}$	Delay from DEMB rising to HO1 rising edge			120		ns
$t_{SYNCIN-SECOND}$	Delay from DEMB falling edge to HO2 rising edge	Secondary mode, MODE = FB2 = VDDA		100		ns
$t_{DEMB-FILTER}$	Delay from DEMB low to diode emulation enable	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	15		50	µs

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{AWAKE-FILTER}$	Maximum SYNC period to maintain standby state	V_{EN1} = V_{EN2} = 0 V		27		µs
SYNCHRONIZATION OUTPUT (SYNCOUT)						
$V_{SYNCOUT-LO}$	SYNCOUT low-state voltage	$I_{SYNCOUT}$ = 16 mA			0.8	V
$F_{SYNCOUT}$	SYNCOUT frequency	MODE = FB2 = VDDA			0	Hz
$t_{SYNCOUT1}$	Delay from HO2 rising edge to SYNCOUT rising edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		2.5		µs
$t_{SYNCOUT2}$	Delay from HO2 rising edge to SYNCOUT falling edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		7.5		µs
DITHER (DITH)						
I_{DITH}	Dither source/sink current			21		µA
$V_{DITH-HIGH}$	Dither high-level threshold			1.25		V
$V_{DITH-LOW}$	Dither low-level threshold			1.15		V
SOFT START (SS1, SS2)						
I_{SS}	Soft-start current	V_{MODE} = 0 V	16	21	28	µA
R_{SS-PD}	Soft-start pulldown resistance	V_{MODE} = 0 V		3		Ω
V_{SS-FB}	SS to FB clamp voltage	V_{CS} – V_{VOUT} > 73 mV		130		mV
$I_{SS-SECOND}$	SS leakage, secondary mode	V_{SS} = 0.8 V, MODE = FB2 = VDDA		30		nA
$I_{SS-INTLV}$	SS2 leakage, interleaved mode	V_{SS} = 0.8 V, MODE = VDDA, V_{FB2} = 0 V		21		nA
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown			175		°C
$T_{SHD-HYS}$	Thermal shutdown hysteresis			15		°C

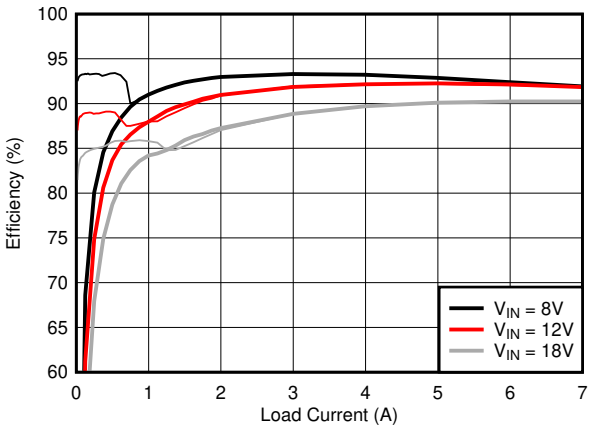
8.6 Switching Characteristics

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the gate driver outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW1}	Switching frequency 1	R_{RT} = 100 kΩ	195	220	245	kHz
F_{SW2}	Switching frequency 2	R_{RT} = 10 kΩ		2.2		MHz
F_{SW3}	Switching frequency 3	R_{RT} = 220 kΩ		100		kHz
SLOPE1	Internal slope compensation 1	R_{RT} = 10 kΩ		557		mV/µs
SLOPE2	Internal slope compensation 2	R_{RT} = 100 kΩ		64		mV/µs
$t_{ON(min)}$	Minimum on time			38	80	ns
$t_{OFF(min)}$	Minimum off time			80	105	ns
$PH_{HO1-HO2}$	Phase between HO1 and HO2	DEMB = MODE = AGND		180		°

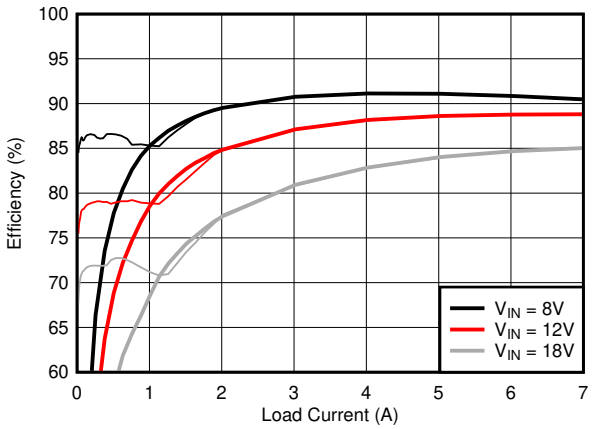
8.7 Typical Characteristics

V_{IN} = V_{EN1} = V_{EN2} = 12 V, T_J = 25°C, unless otherwise stated



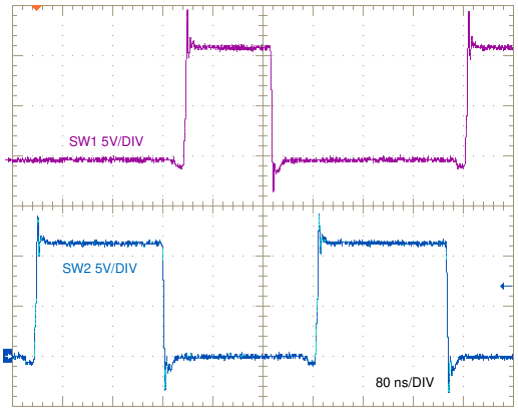
See Figure 10-4. V_{OUT} = 5 V F_{SW} = 2.1 MHz

Figure 8-1. Efficiency Versus Load



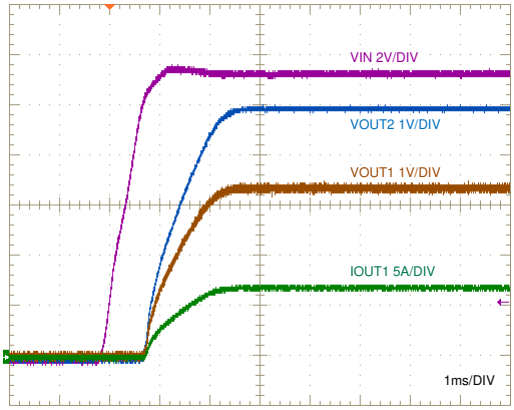
See Figure 10-4. V_{OUT} = 3.3 V F_{SW} = 2.1 MHz

Figure 8-2. Efficiency Versus Load



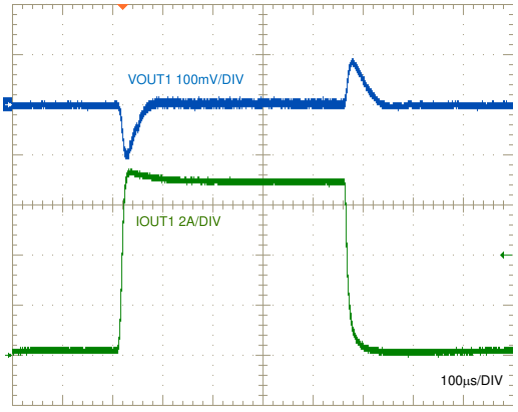
See Figure 10-4.

Figure 8-3. Switch Node Voltages



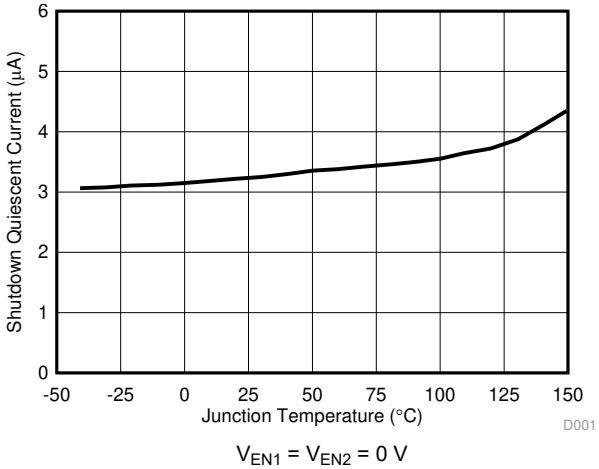
See Figure 10-4.

Figure 8-4. Start-Up Characteristic



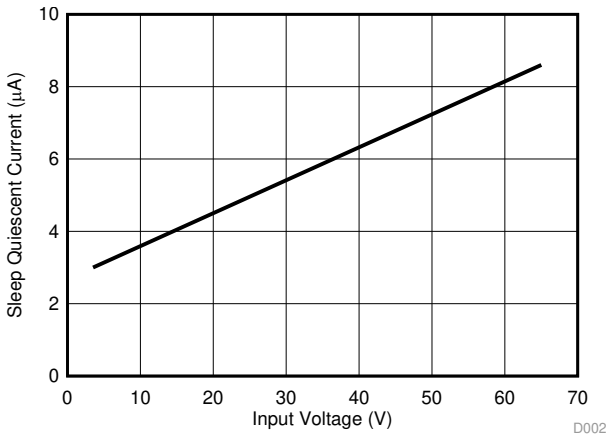
See Figure 10-4.

Figure 8-5. Load Transient Response



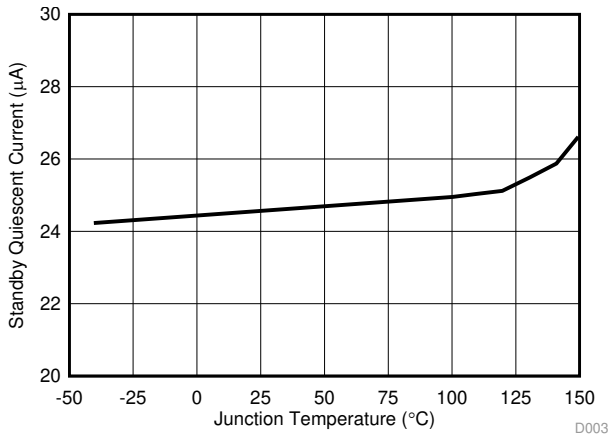
V_{EN1} = V_{EN2} = 0 V

Figure 8-6. Shutdown Current Versus Temperature



$V_{EN1} = V_{EN2} = 0$ V

Figure 8-7. Shutdown Current Versus Input Voltage



$V_{EN2} = 0$ V

Figure 8-8. Channel 1 Standby Current Versus Temperature

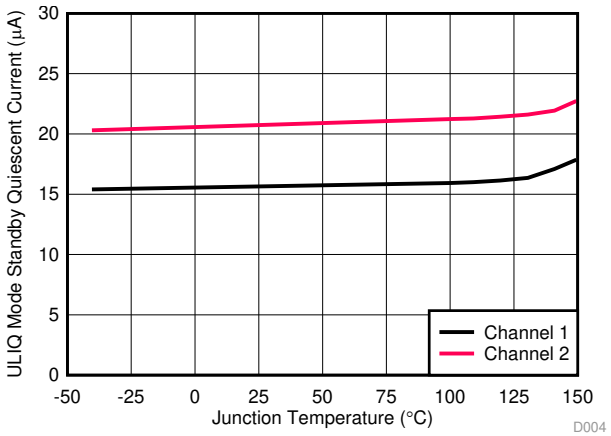


Figure 8-9. ULIQ Mode Standby Current Versus Temperature

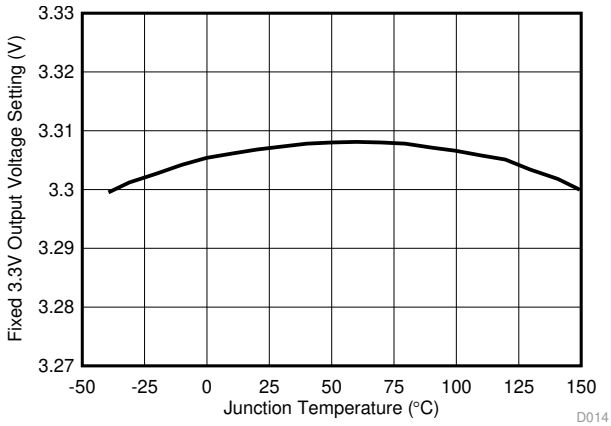


Figure 8-10. Fixed 3.3-V Output Voltage (VOUT1) Versus Temperature

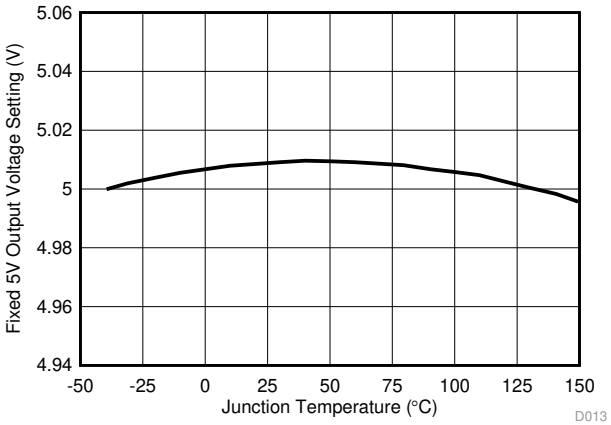


Figure 8-11. Fixed 5-V Output Voltage (VOUT1) Versus Temperature

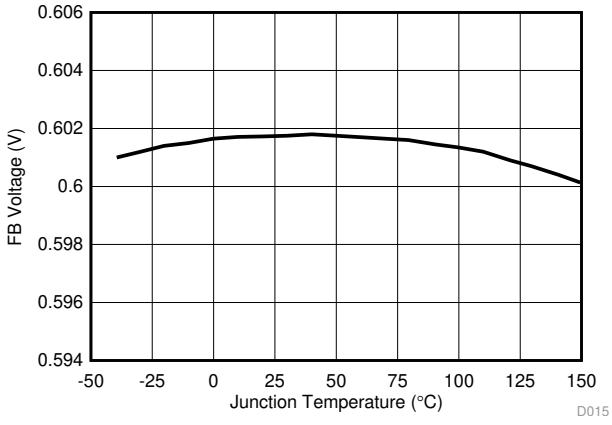


Figure 8-12. Feedback Voltage Versus Temperature

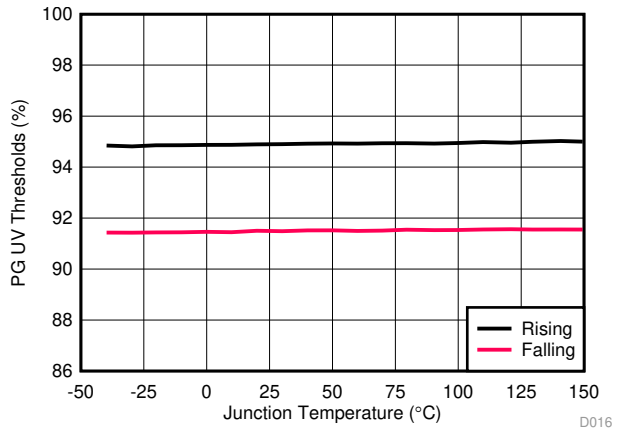


Figure 8-13. PG UV Thresholds Versus Temperature

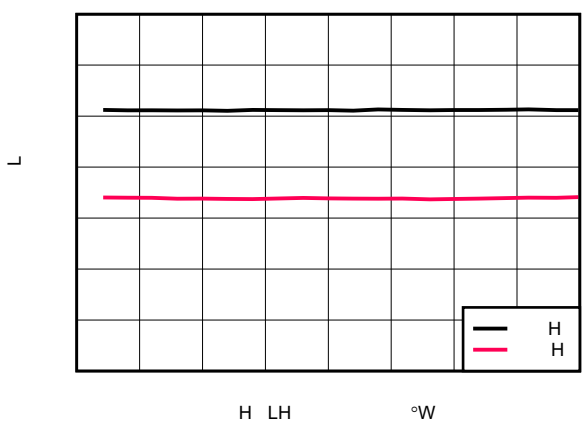


Figure 8-14. PG OV Thresholds Versus Temperature

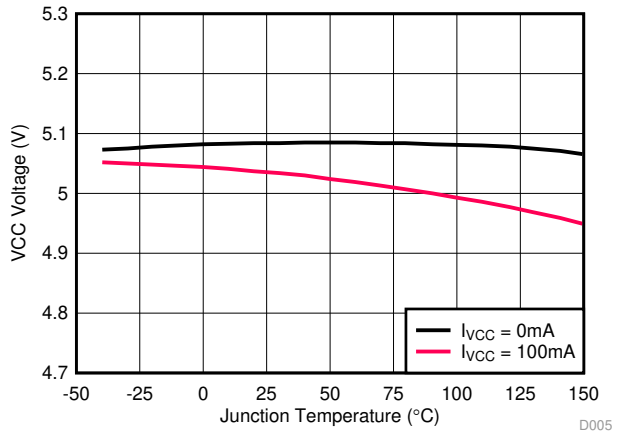


Figure 8-15. VCC Regulation Voltage Versus Temperature

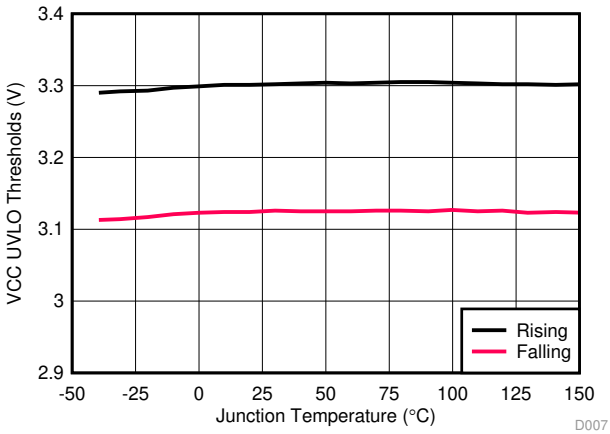


Figure 8-16. VCC UVLO Thresholds Versus Temperature

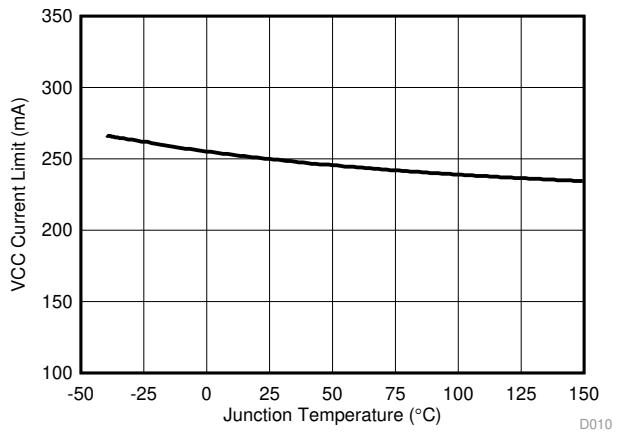


Figure 8-17. VCC Current Limit Versus Temperature

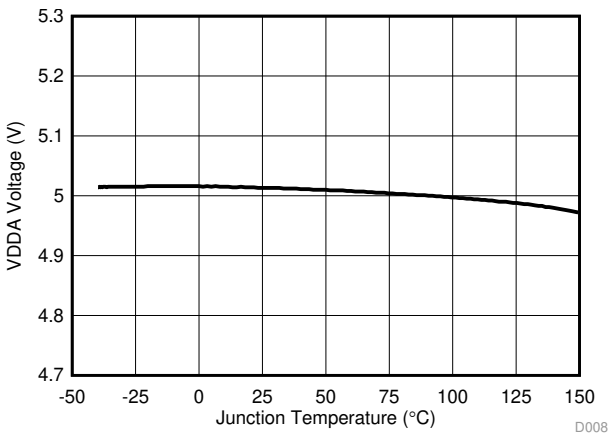


Figure 8-18. VDDA Regulation Voltage Versus Temperature

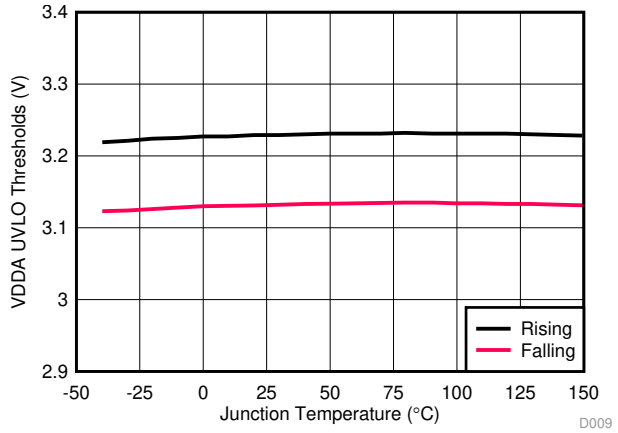


Figure 8-19. VDDA UVLO Thresholds Versus Temperature

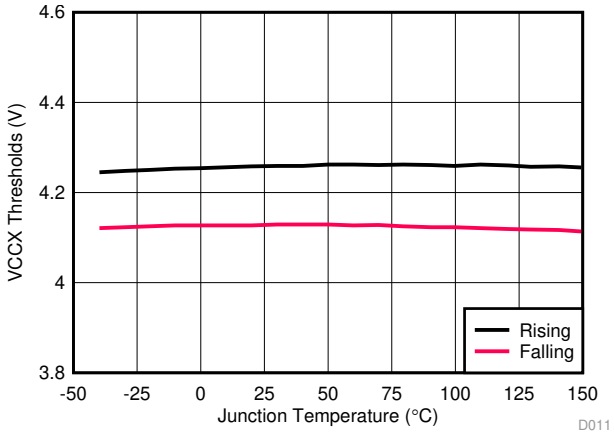


Figure 8-20. VCCX On/Off Thresholds Versus Temperature

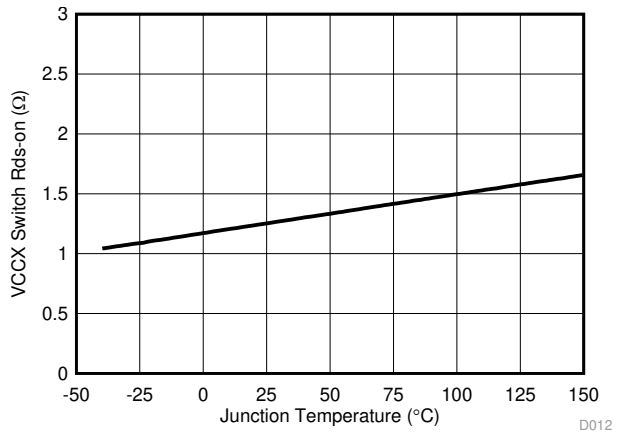


Figure 8-21. VCCX Switch Resistance Versus Temperature

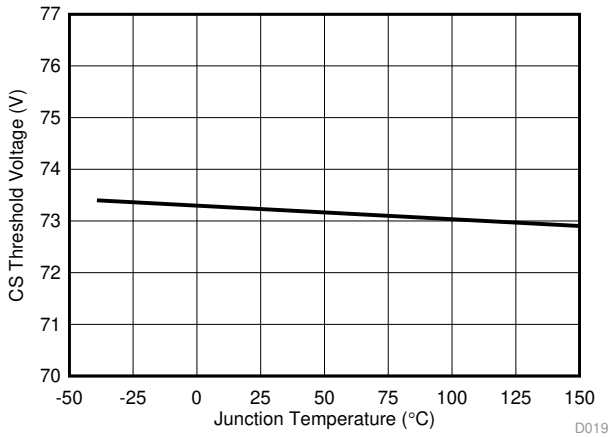


Figure 8-22. Current Sense (CS1) Threshold Versus Temperature

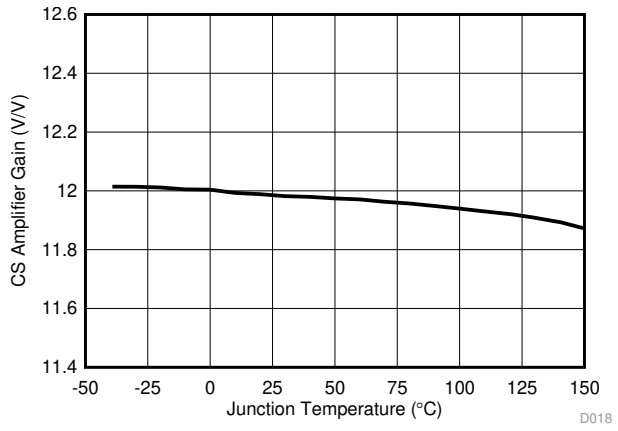


Figure 8-23. Current Sense (CS1) Amplifier Gain Versus Temperature

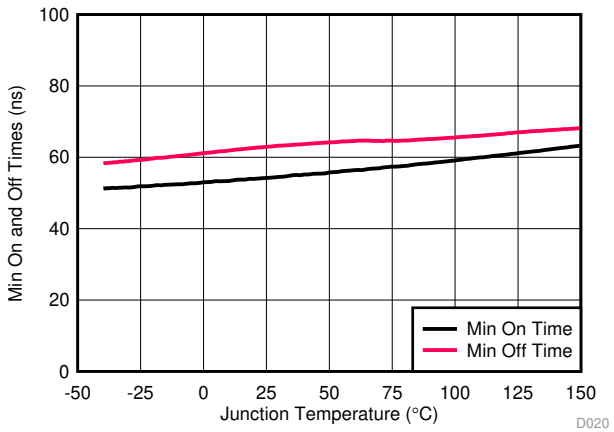


Figure 8-24. Minimum On Time and Off Time (HO1) Versus Temperature

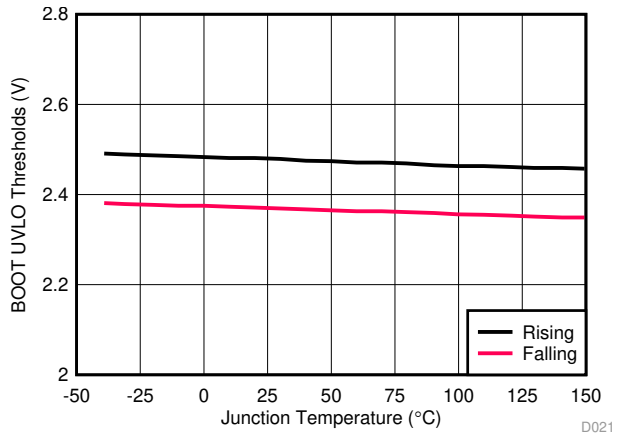


Figure 8-25. BOOT (HB1) UVLO Thresholds Versus Temperature

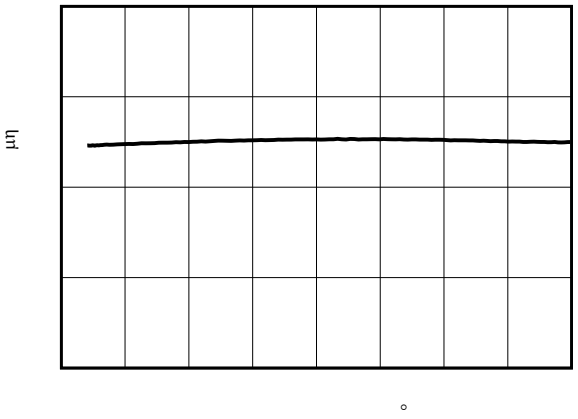


Figure 8-26. Soft-Start (SS1) Current Versus Temperature

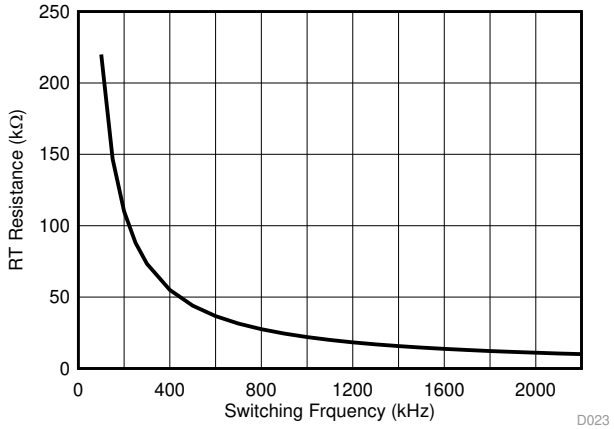


Figure 8-27. RT Resistance Versus Switching Frequency

9 Detailed Description

9.1 Overview

The LM5143 is a dual-phase or dual-channel switching controller that features all of the functions necessary to implement a high-efficiency synchronous buck power supply operating over a wide input voltage range from 3.5 V to 65 V. The LM5143 is configured to provide a fixed 3.3-V or 5-V output, or an adjustable output between 0.6 V to 55 V. This easy-to-use controller integrates high-side and low-side MOSFET drivers capable of sourcing 3.25-A and sinking 4.25-A peak current. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

Current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. It also supports a wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 100 kHz to 2.2 MHz, and the frequency can be synchronized as high as 2.5 MHz by applying an external clock to DEMB.

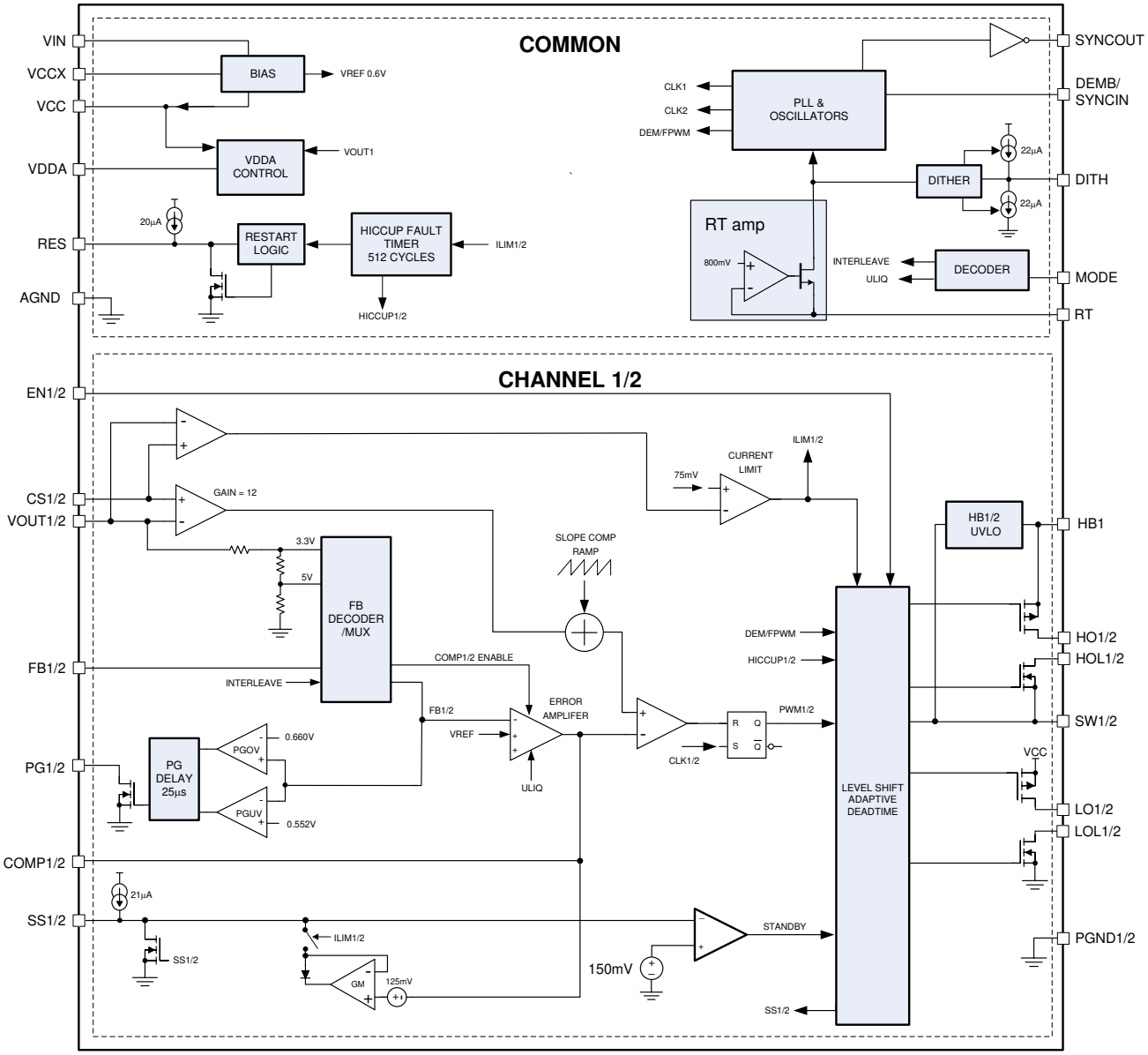
An external bias supply can be connected to VCCX to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include the following:

- Current limiting
- Thermal shutdown
- UVLO
- Remote shutdown capability

The LM5143 incorporates features to simplify the compliance with CISPR 11 and CISPR 32 EMI requirements. An optional spread spectrum frequency modulation (SSFM) technique reduces the peak EMI signature, while the adaptive gate drivers with slew rate control minimize high-frequency emissions. Finally, 180° out-of-phase interleaved operation of the two controller channels reduces input filtering and capacitor requirements.

The LM5143 is provided in a 40-pin VQFN package with an exposed pad to aid in thermal dissipation.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage Range (V_{IN})

The LM5143 operational input voltage range is from 3.5 V to 65 V. The device is intended for step-down conversions from 12-V, 24-V, and 48-V automotive supply rails. The application circuit in Figure 9-1 shows all the necessary components to implement an LM5143-based wide-V_{IN} dual-output step-down regulator using a single supply. The LM5143 uses an internal LDO subregulator to provide a 5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5 V plus the necessary subregulator dropout specification).

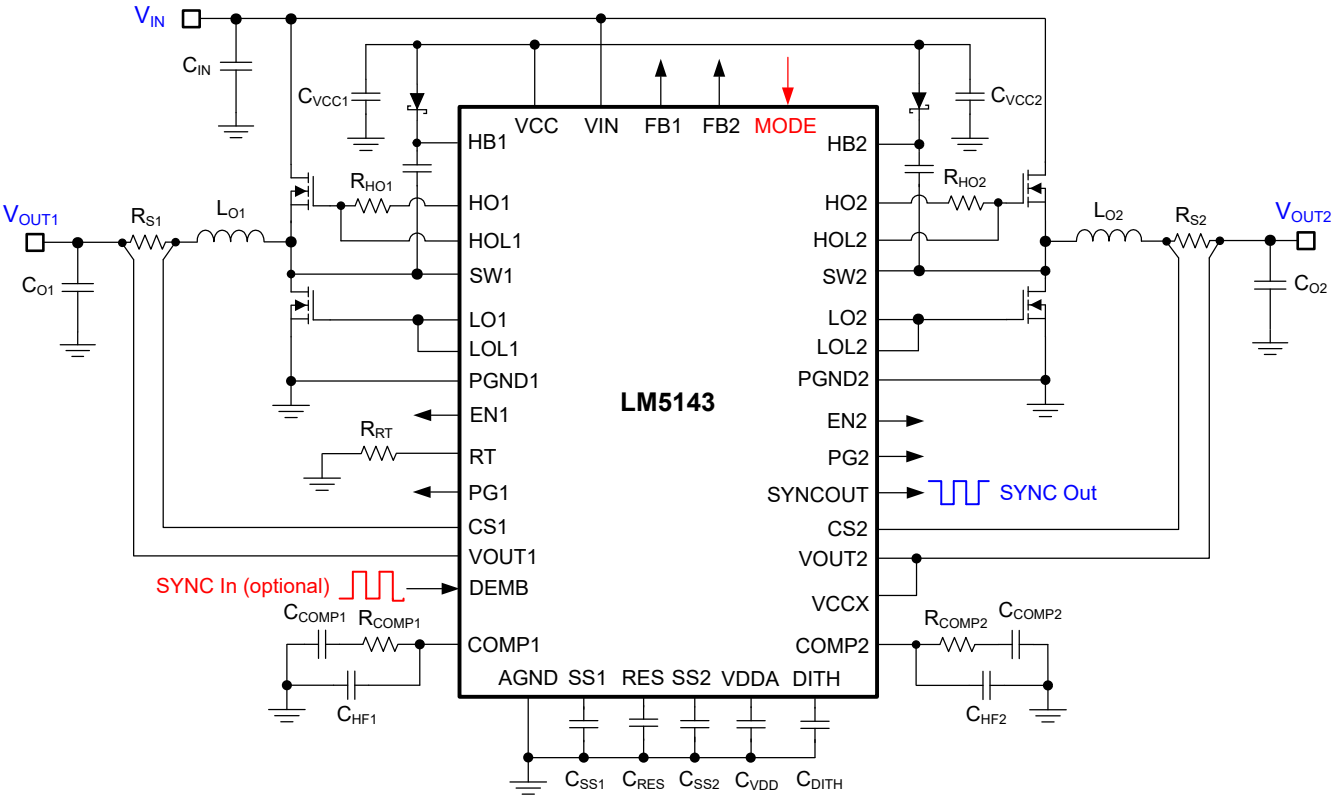


Figure 9-1. Dual-Output Regulator Schematic Diagram With an Input Voltage Range of 3.5 V to 65 V

In high input voltage applications, make sure the VIN and SW pins do not exceed their absolute maximum voltage rating of 70 V during line or load transient events. Voltage excursions that exceed the *Absolute Maximum Ratings* can damage the IC. Proceed carefully during PCB layout and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

9.3.2 High-Voltage Bias Supply Regulator (VCC, VCCX, VDDA)

The LM5143 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 65 V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

The VCC regulator output current limit is 170 mA (minimum). At power up, the regulator sources current into the capacitors connected at the VCC pin. When the VCC voltage exceeds 3.3 V, both output channels are enabled (if EN1 and EN2 are connected to a voltage greater than 2 V) and the soft-start sequence begins. Both channels remain active unless the VCC voltage falls below the VCC falling UVLO threshold of 3.1 V (typical) or EN1 or EN2 is switched to a low state. The LM5143 has two VCC pins that must be connected together on the PCB. TI recommends that two VCC capacitors are connected from VCC1 to PGND1 and from VCC2 to PGND2. The recommended range for each VCC capacitor is from 2.2 µF to 10 µF.

An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 470-nF ceramic capacitor to achieve a low-noise internal bias rail. Normally, VDDA is 5 V, but there are two operating conditions where it regulates at 3.3 V. The first is in skip cycle mode when V_{OUT1} is set to 3.3 V and V_{OUT2} is disabled. The second is in a cold-crank start-up where V_{IN} is 3.8 V and V_{OUT1} is 3.3 V.

Internal power dissipation of the VCC regulator can be minimized by connecting VCCX to a 5-V output at VOUT1 or VOUT2 or to an external 5-V supply. If the VCCX voltage is above 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Tie VCCX to AGND if it is unused. Never connect VCCX to a voltage greater than 6.5 V or less than –0.3 V. If an external supply is connected to VCCX to power the LM5143, V_{IN} must be greater than the external bias voltage during all conditions to avoid damage to the controller.

9.3.3 Enable (EN1, EN2)

The LM5143 contains two enable inputs. EN1 and EN2 facilitate independent start-up and shutdown control of V_{OUT1} and V_{OUT2}. The enable pins can be connected to a voltage as high as 70 V. If an enable input is greater than 2 V, its respective output is enabled. If an enable pin is pulled below 0.4 V, the output is shut down. If both outputs are disabled, the LM5143 is in a low-I_Q shutdown mode with a 4-µA typical current drawn from VIN. TI does not recommend leaving EN1 or EN2 floating.

9.3.4 Power-Good Monitor (PG1, PG2)

The LM5143 includes output voltage monitoring signals for V_{OUT1} and V_{OUT2} to simplify sequencing and supervision. The power-good function can be used to enable circuits that are supplied by the corresponding voltage rail or to turn on sequenced supplies. Each power-good output (PG1 and PG2) switches to a high impedance open-drain state when the corresponding output voltage is in regulation. Each output switches low when the corresponding output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25-µs deglitch filter prevents false tripping of the power-good signals during transients. TI recommends pullup resistors of 100 kΩ from PG1 and PG2 to the relevant logic rail. PG1 and PG2 are asserted low during soft start and when the corresponding buck regulator is disabled by EN1 or EN2.

If the LM5143 is in diode emulation mode (V_{DEMB} = 0 V) and enters sleep mode, the power-good comparators are turned off to reduce quiescent current consumption. When this occurs, PG1 and PG2 are open or pulled high (if a pullup resistor is connected) such that output undervoltage or overvoltage events are not detected.

9.3.5 Switching Frequency (RT)

The LM5143 oscillator is programmed by a resistor between RT and AGND to set an oscillator frequency between 100 kHz to 2.2 MHz. CLK1 is the clock for channel 1 and CLK2 is for channel 2. CLK1 and CLK2 are 180° out of phase. Use Equation 1 to calculate the RT resistance for a given switching frequency.

$$R_{RT}\left[k\Omega\right] = \frac{22}{F_{SW}\left[MHz\right]} \tag{1}$$

Under low V_{IN} conditions when either of the on times of the high-side MOSFETs exceeds the programmed oscillator period, the LM5143 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators (CLK1 and CLK2) operate independently and asynchronously until both channels can maintain output regulation at the programmed frequency.

The approximate input voltage level where this occurs is given by Equation 2.

$$V_{IN(min)} = V_{OUT} \cdot \frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \tag{2}$$

where

- t_{SW} is the switching period.

- $t_{OFF(min)}$ is the minimum off time of 60 ns.

9.3.6 Clock Synchronization (DEMB)

To synchronize the LM5143 to an external source, apply a logic-level clock signal (greater than 2 V) to DEMB. The LM5143 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.5 MHz. If there is an RT resistor and a synchronization signal, the LM5143 ignores the RT resistor and synchronizes to the external clock. Under low V_{IN} conditions when the minimum off time is reached, the synchronization signal is ignored, allowing the switching frequency to reduce to maintain output voltage regulation.

9.3.7 Synchronization Out (SYNCOUT)

The SYNCOUT voltage is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM5143 controller, all four phases are 90° out of phase.

9.3.8 Spread Spectrum Frequency Modulation (DITH)

The LM5143 provides a frequency dithering option that is enabled by connecting a capacitor from DITH to AGND. This generates a triangular voltage centered at 1.2 V at DITH. See Figure 9-2. The triangular waveform modulates the oscillator frequency by ±5% of the nominal frequency set by the RT resistance. Use Equation 3 to calculate the required DITH capacitance to set the modulating frequency, F_{MOD}. For the dithering circuit to effectively attenuate the peak EMI, the modulation rate must be less than 20 kHz for proper operation of the clock circuit.

$$C_{DITH} = \frac{21\,\mu A}{2 \cdot F_{MOD} \cdot 0.1V} \tag{3}$$

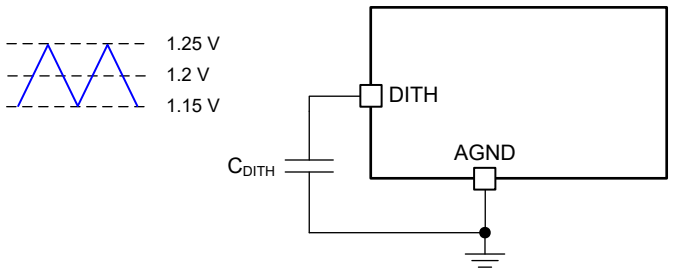


Figure 9-2. Switching Frequency Dithering

If DITH is connected to VDDA during power up, the dither feature is disabled and cannot be enabled unless VCC is recycled below the VCC UVLO threshold. If DITH is connected to AGND on power up, C_{DITH} is prevented from charging, disabling dither. Also, dither is disabled when the LM5143 is synchronized to an external clock.

9.3.9 Configurable Soft Start (SS1, SS2)

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM5143 features an adjustable soft start that determines the charging time of the output or outputs. Soft-start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced.

The LM5143 regulates the FB voltage to the SS voltage or the internal 600-mV reference, whichever is lower. At the beginning of the soft-start sequence when the SS voltage is 0 V, the internal 21-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the relevant FB and output voltages. Use Equation 4 to calculate the soft-start capacitance.

$$C_{SS}(nF) = 35 \cdot t_{SS}(ms) \quad (4)$$

where

- t_{SS} is the required soft-start time.

SS can be pulled low with an external circuit to stop switching, but this is not recommended. When the controller is in FPWM mode (set by connecting DEMB to VDDA), pulling SS low results in COMP being pulled down internally as well. LO remains on and the low-side MOSFET discharges the output capacitor, resulting in large negative inductor current. In contrast, the LO gate driver is disabled when the LM5143 internal logic pulls SS low due to a fault condition.

9.3.10 Output Voltage Setpoint (FB1, FB2)

The LM5143 outputs can be independently configured for one of the two fixed output voltages with no external feedback resistors, or adjusted to the desired voltage using an external resistor divider. V_{OUT1} or V_{OUT2} can be configured as a 3.3-V output by connecting the corresponding FB pin to VDDA, or a 5-V output by connecting FB to AGND. The FB1 and FB2 connections (either VDDA or GND) are detected during power up. The configuration settings are latched and cannot be changed until the LM5143 is powered down with the VCC voltage decreasing below its falling UVLO threshold, and then powered up again.

Alternatively, the output voltage can be set using external resistive dividers from the output to the relevant FB pin. The output voltage adjustment range is between 0.6 V and 55 V. The regulation threshold at FB is 0.6 V (V_{REF}). Use Equation 5 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2}, respectively. See Figure 9-3.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \cdot R_{FB2} \quad (5)$$

The recommended starting value for R_{FB2} is between 10 kΩ and 20 kΩ.

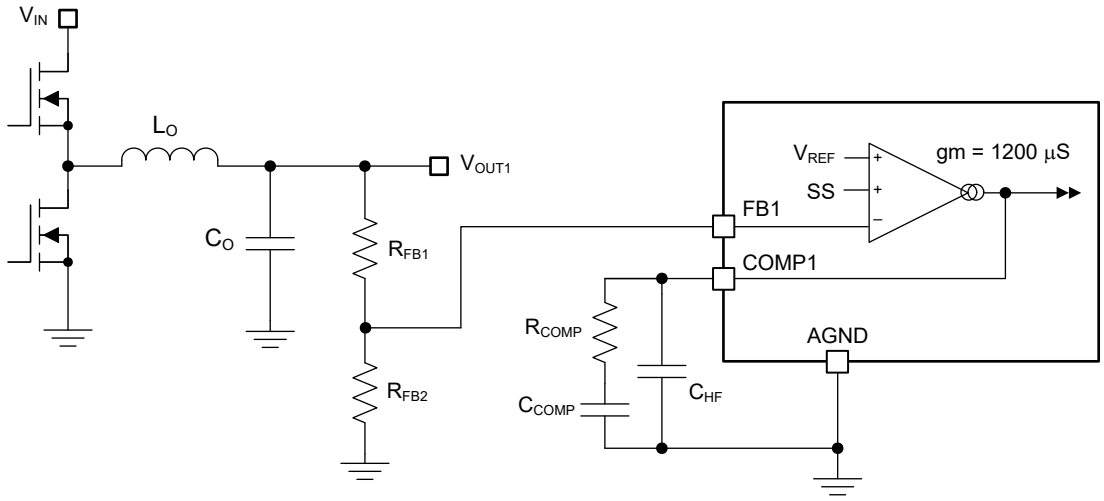


Figure 9-3. Control Loop Error Amplifier

The Thevenin equivalent impedance of the resistive divider connected to the FB pin must be greater than 5 kΩ for the LM5143 to detect the divider and set the channel to the adjustable output mode.

$$= \frac{\Omega \cdot \Omega}{\Omega + \Omega} > \Omega \quad (6)$$

If a low I_Q mode is required, take care when selecting the external resistors. The extra current drawn from the external divider is added to the LM5143 $I_{STANDBY}$ current (15 µA typical). The divider current reflected to V_{IN} is divided down by the ratio of V_{OUT}/V_{IN}. For example, if V_{OUT} is set to 5.55 V with R_{FB1} equal to 82.5 kΩ and R_{FB2} equal to 10 kΩ, use Equation 7 to calculate the input current from a 12-V input required to supply the current in the feedback resistors.

$$I_{VIN(DIVIDER)} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \cdot \frac{V_{OUT}}{\eta \cdot V_{IN}} = \frac{5.55\,V}{82.5k\Omega + 10k\Omega} \cdot \frac{5.55\,V}{80\% \cdot 12\,V} \approx 35\ \ A$$

$$I_{VIN} = I_{STANDBY} + I_{VIN(DIVIDER)} = 15\ \ A + 35\ \ A = 50\ \ A \tag{7}$$

If one output is enabled and the other disabled, the VCC output is in regulation. The HB voltage of the disabled channel charges to VCC through the bootstrap diode. As a result, the HO driver bias current (approximately 1.5 µA) can increase the output voltage of the disabled channel to approximately 2.2 V. If this is not desired, add a load resistor (100 kΩ) to the output that is disabled to maintain a low-voltage OFF state.

9.3.11 Minimum Controllable On Time

There are two limitations to the minimum output voltage adjustment range: the LM5143 voltage reference of 0.6 V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio of V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy Equation 8.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \cdot F_{SW} \tag{8}$$

where

- $t_{ON(min)}$ is 65 ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM5143 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5 V with an input voltage is 24 V and switching frequency of 2.1 MHz, the voltage conversion ratio test in Equation 9 is satisfied.

$$\frac{5\,V}{24\,V} > 65\,ns \cdot 2.1\,MHz$$

$$0.208 > 0.137 \tag{9}$$

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM5143 switching frequency to meet the requirement of Equation 8.

9.3.12 Error Amplifier and PWM Comparator (FB1, FB2, COMP1, COMP2)

Each channel of the LM5143 has an independent high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.6 V). The output of the transconductance amplifier is connected to the COMP pin, allowing the user to provide external control loop compensation. A type-II compensation network is generally recommended for peak current-mode control.

The amplifier has two gain settings, one is for normal operation with a g_m of 1200 µS and the other is for ultra-low I_Q with a g_m of 60 µS. For normal operation, connect MODE to AGND. For ultra-low operation I_Q, connect MODE to AGND through a 10-kΩ resistor.

9.3.13 Slope Compensation

The LM5143 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Use Equation 10 to calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope.

$$L_{O\text{-}IDEAL}(\quad T = \frac{V_{OUT}(V) \cdot R_S(m\Omega)}{24 \cdot F_{SW}(MHz)} \tag{10}$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, which increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

9.3.14 Inductor Current Sense (CS1, VOUT1, CS2, VOUT2)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

9.3.14.1 Shunt Current Sensing

Figure 9-4 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM5143 current sense amplifier.

If the peak differential current signal sensed from CS to VOUT exceeds the current limit threshold of 73 mV, the current limit comparator immediately terminates the applicable HO output for cycle-by-cycle current limiting. Use Equation 11 to calculate the shunt resistance.

$$R_S = \frac{V_{CS}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \tag{11}$$

where

- V_{CS} is current sense threshold of 73 mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

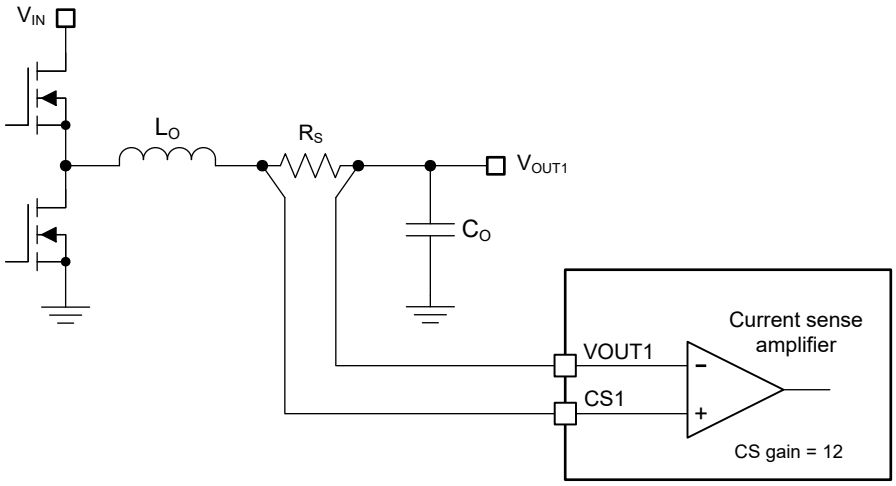


Figure 9-4. Shunt Current Sensing Implementation

The respective SS voltage is clamped 150 mV above FB during an overcurrent condition for each channel. Sixteen overcurrent events must occur before the SS clamp is enabled. This makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

9.3.14.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in Figure 9-5 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across the inductor DCR.

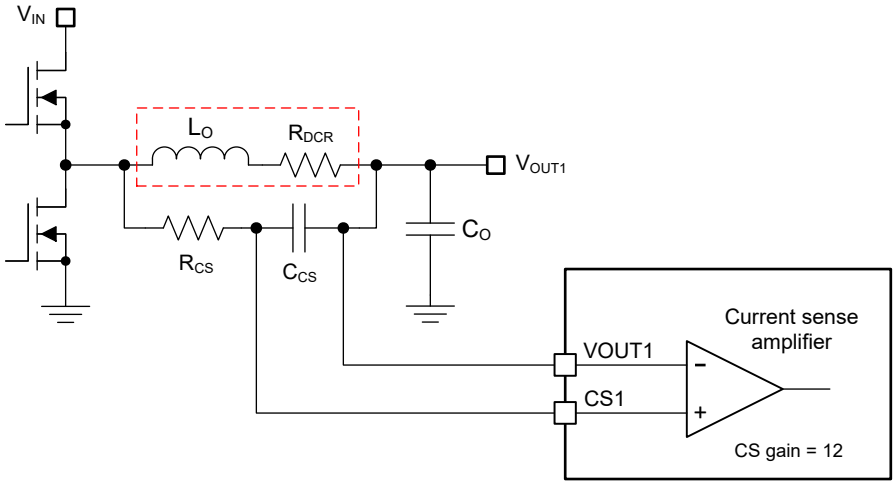


Figure 9-5. Inductor DCR Current Sensing Implementation

Use Equation 12 to calculate the voltage drop across the sense capacitor in the s-domain. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

$$V_{CS}(s) = \frac{1 + s \cdot \frac{L_O}{R_{DCR}}}{1 + s \cdot R_{CS} \cdot C_{CS}} \cdot R_{DCR} \cdot \left(I_{OUT(CL)} + \frac{\Delta I_L}{2} \right) \quad (12)$$

Choose the C_{CS} capacitance greater than or equal to 0.1 µF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe the guidelines found in Section 12.1 to make sure that noise and DC errors do not corrupt the differential current sense signals applied between the CS and VOUT pins.

9.3.15 Hiccup Mode Current Limiting (RES)

The LM5143 includes an optional hiccup mode protection function that is enabled when a capacitor is connected to the RES pin. In normal operation, the RES capacitor is discharged to ground. If 512 cycles of cycle-by-cycle current limiting occurs, SS is pulled low and the HO and LO outputs are disabled (see Figure 9-6). A 20-µA current source begins to charge the RES capacitor. When the RES voltage increases to 1.2 V, RES is pulled low and the SS capacitor begins to charge. The 512-cycle hiccup counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. Separate hiccup counters are provided for each channel, but the RES pin is shared by both channels. One channel can be in hiccup protection while the other operates normally. In the event that both channels are in an overcurrent condition triggering hiccup protection, the last hiccup counter to expire pulls RES low and starts the RES capacitor charging cycle. Both channels then restart together when V_{RES} = 1.2 V. If RES is connected to VDDA at power up, the hiccup function is disabled for both channels.

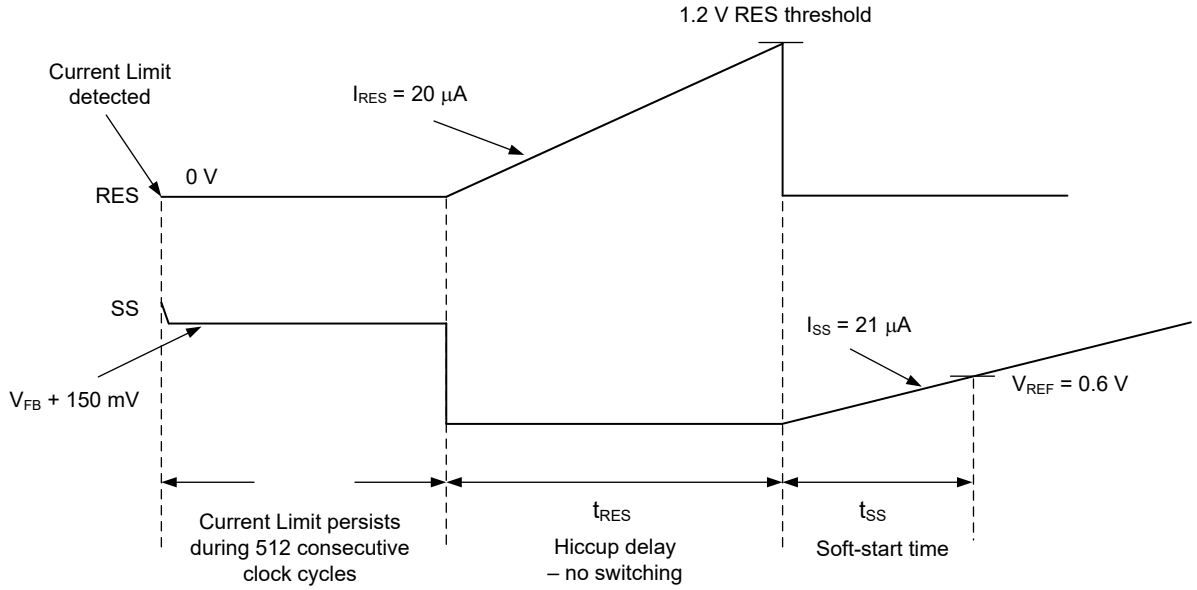


Figure 9-6. Hiccup Mode Timing Diagram

Use Equation 13 to calculate the RES capacitance.

$$C_{RES}(nF) = 17 \cdot t_{RES}(ms) \quad (13)$$

where

- t_{RES} is the specified hiccup delay as shown in Figure 9-6.

9.3.16 High-Side and Low-Side Gate Drivers (HO1/2, LO1/2, HOL1/2, LOL1/2)

The LM5143 contains N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET. The high-side gate driver works in conjunction with an external bootstrap diode,

D_{BST}, and bootstrap capacitor, C_{BST}. See Figure 9-7. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0 V and C_{BST} is charged from VCC through D_{BST}. TI recommends a 0.1-µF ceramic capacitor connected with short traces between the applicable HB and SW pins.

The LO and HO outputs are controlled with an adaptive dead-time methodology so that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.5 V (typical). LO is then enabled after a small delay (HO fall to LO rising delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 2.5 V. HO is then enabled after a small delay (LO falling to HO rising delay). This technique ensures adequate dead time for any size N-channel MOSFET component or parallel MOSFET configurations.

Caution is advised when adding series gate resistors, as this can decrease the effective dead time. Each of the high-side and low-side drivers has an independent driver source and sink output pins. This allows the user to adjust drive strength to optimize the switching losses for maximum efficiency and control the slew rate for reduced EMI signature. The selected N-channel high-side MOSFET determines the appropriate bootstrap capacitance values, C_{BST}, in Figure 9-7 according to Equation 14.

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{14}$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage.
- ΔV_{BST} is the voltage variation of the high-side MOSFET driver after turn-on.

To determine C_{BST}, choose ΔV_{BST} so that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1 µF. Use high-side and low-side MOSFETs with logic level gate threshold voltages.

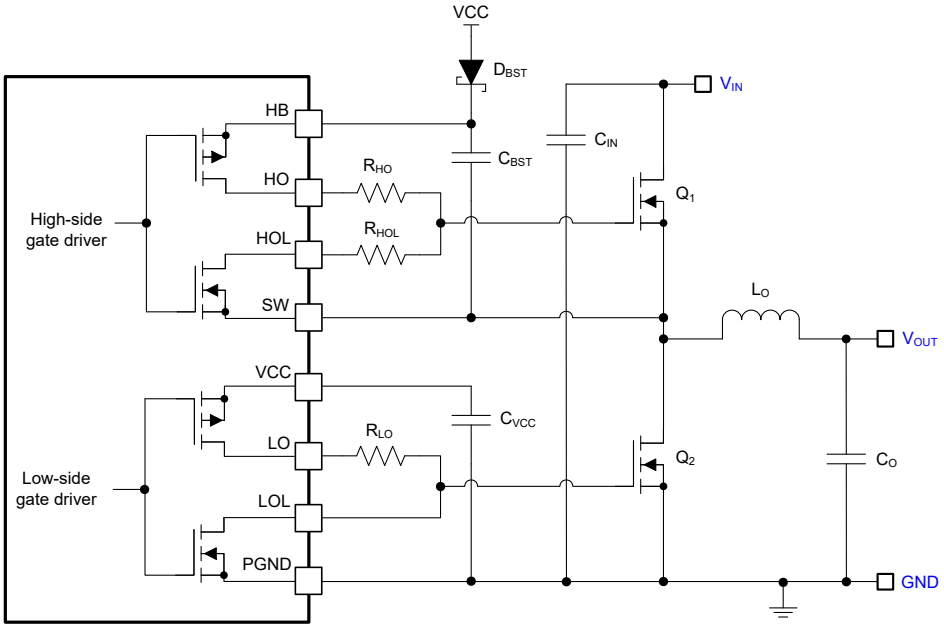


Figure 9-7. Integrated MOSFET Gate Drivers

9.3.17 Output Configurations (MODE, FB2)

9.3.17.1 Independent Dual-Output Operation

The LM5143 has two outputs that can operate independently. Both V_{OUT1} and V_{OUT2} can be set at 3.3 V or 5 V without installing external feedback resistors. Alternatively, set the output voltages between 0.6 V and 55 V using external feedback resistors based on Equation 5. See Table 9-1 and Figure 9-8. Connect MODE directly to AGND for independent outputs.

Table 9-1. Output Voltage Settings

Mode	FB1	FB2	VOUT1	VOUT2	Error Amplifier, g_m
AGND	AGND	AGND	5 V	5 V	1200 µS
AGND	VDDA	VDDA	3.3 V	3.3 V	1200 µS
AGND	VDDA	AGND	3.3 V	5 V	1200 µS
AGND	AGND	VDDA	5 V	3.3 V	1200 µS
AGND	$R_{divider}$	$R_{divider}$	0.6 V to 55 V	0.6 V to 55 V	1200 µS
10 kΩ to AGND	AGND	AGND	5 V	5 V	60 µS
10 kΩ to AGND	VDDA	VDDA	3.3 V	3.3 V	60 µS
10 kΩ to AGND	VDDA	AGND	3.3 V	5 V	60 µS
10 kΩ to AGND	AGND	VDDA	5 V	3.3 V	60 µS
10 kΩ to AGND	$R_{divider}$	$R_{divider}$	0.6 V to 55 V	0.6 V to 55 V	60 µS

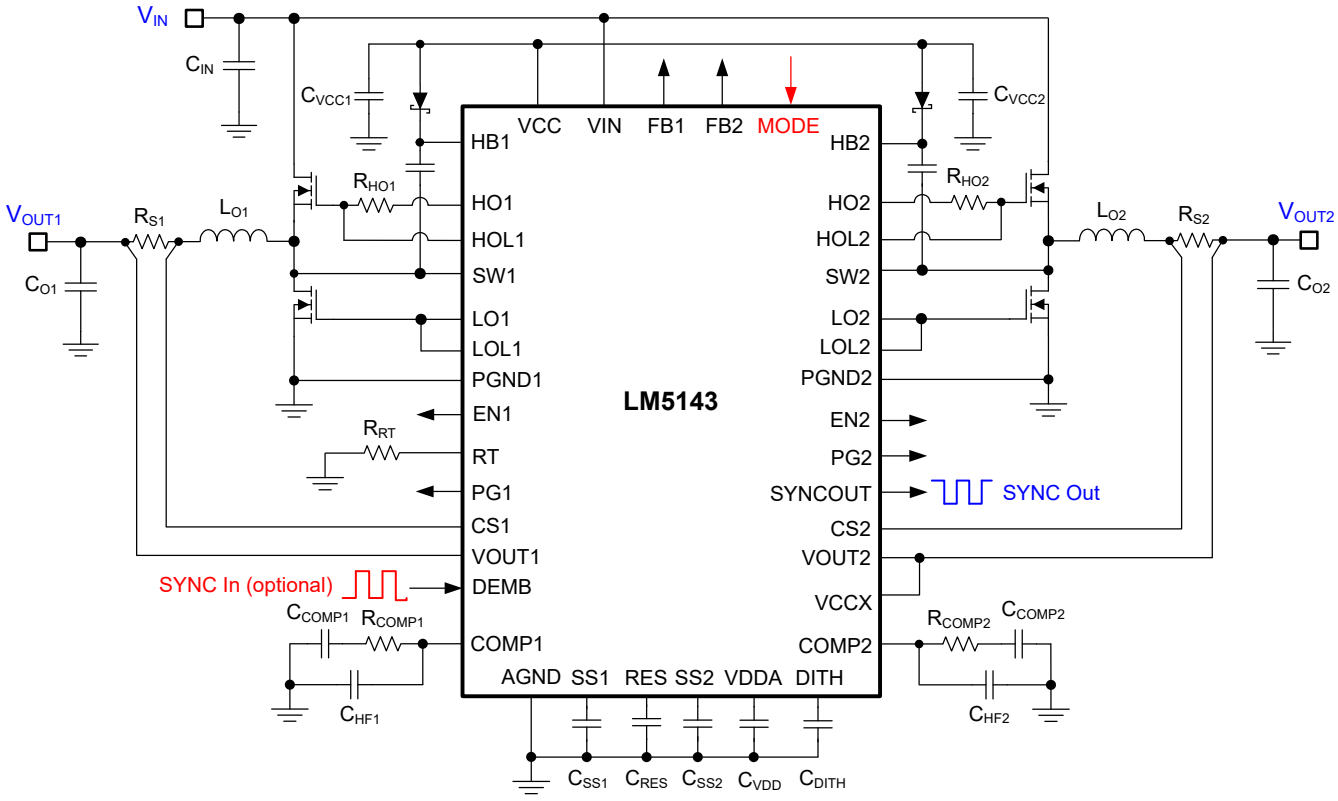


Figure 9-8. Regulator Schematic Configured for Independent Dual Outputs

9.3.17.2 Single-Output Interleaved Operation

Connect the MODE to VDDA and FB2 to AGND to configure the LM5143 for interleaved operation. This disables the channel 2 error amplifier and places it in a high impedance state. The controller is then in a primary and secondary configuration. Connect COMP1 to COMP2 and SS1 to SS2. Connect FB1 to VDDA for a 3.3-V output

and to AGND for a 5-V output. Connect FB1 to an external feedback divider for an output voltage between 0.6 V to 55 V. See Table 9-2 and Figure 9-9.

The LM5143 in single-output interleaved operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

Table 9-2. Single-Output Interleaved Operation

Mode	FB1	FB2	Output Setpoint
VDDA	AGND	AGND	5 V
VDDA	VDDA	AGND	3.3 V
VDDA	$R_{divider}$	AGND	0.6 V to 55 V

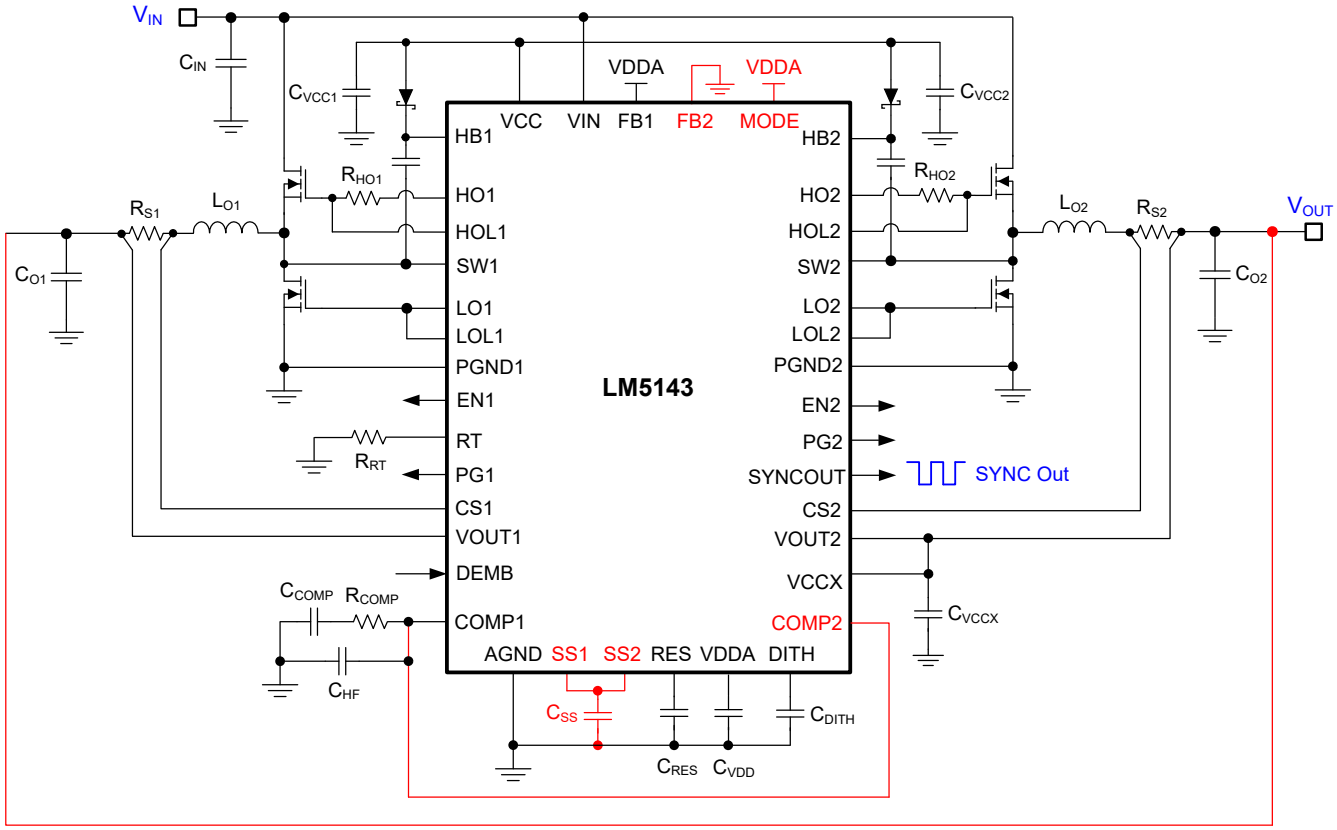


Figure 9-9. Two-Phase Regulator Schematic Configured for Single-Output Interleaved Operation

9.3.17.3 Single-Output Multiphase Operation

To configure the LM5143 for multiphase operation (three or four phases), two LM5143 controllers are required. See Figure 9-10. Configure the first controller (CNTRL1) as a primary and the second controller (CNTRL2) as a secondary. To configure the second controller as a secondary, connect the MODE and FB2 pins to VDDA. This disables both feedback error amplifiers of the secondary controller, placing them in a high-impedance state. Connect COMP1 and COMP2 of the primary and secondary together. Connect SS1 and SS2 of the primary and secondary together. Connect SYNCOUT of the primary controller to DEMB (SYNCIN) of the secondary. The SYNCOUT of the primary controller is 90° out-of-phase and facilitates interleaved operation. RT is not used for the oscillator when the LM5143 is in secondary mode but instead used for slope compensation. Therefore, select the RT resistance to be the same as that of the primary. The oscillator is derived from the primary controller. FPWM or DEM mode for the secondary is set by connecting its FB1 to VDDA or AGND, respectively. FPWM or DEM mode of the primary controller is set by its DEMB pin. See Table 9-3.

The LM5143 in single-output multiphase operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

See the *Benefits of a Multiphase Buck Converter White Paper* and *Multiphase Buck Design From Start to Finish Application Report* for more information.

Table 9-3. Single-Output Multiphase Operation

Mode	FB1 (Secondary)	FB2 (Secondary)	DEM or FPWM (Secondary)
VDDA	AGND	VDDA	DEM
VDDA	VDDA	VDDA	FPWM

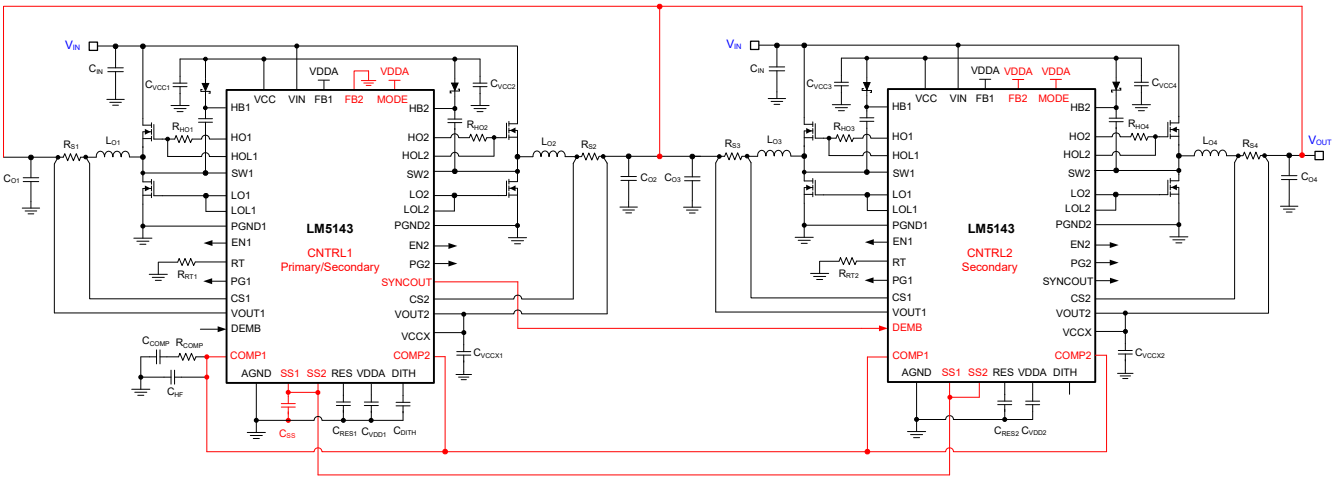


Figure 9-10. Multiphase Regulator Schematic Configured for Single-Output Interleaved Operation

Note

A design with five or more phases (using three or more LM5143 controllers) is feasible when appropriately phase-shifted clock signals are available. For example, a 6-phase design requires three LM5143 controllers with 0°, 60°, and 120° external SYNC signals to achieve the ideal phase separation of 360° divided by the total number of phases.

9.4 Device Functional Modes

9.4.1 Standby Modes

The LM5143 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage does not demand driver output pulses on a cycle-by-cycle basis. When the LM5143 controller detects 16 missed switching cycles, it enters standby mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM5143 to go into standby mode, the controller must be programmed for diode emulation (V_{DEMB} < 0.4 V).

There are two standby modes: ultra-low I_Q and normal mode. To enter ultra-low I_Q mode, connect MODE to AGND through a 10-kΩ resistor. In ultra-low I_Q mode, the transconductance amplifier gain is reduced from 1200 µS to 60 µS. The typical ultra-low I_Q is 15 µA with channel 1 set to 3.3 V and the channel 2 disabled. If ultra-low I_Q is not required, connect MODE to AGND. In normal mode, the I_Q is 25 µA with channel 1 set to 3.3 V and the second channel disabled.

9.4.2 Diode Emulation Mode

A fully synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during light-load, overvoltage, and prebias start-up conditions. The LM5143 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the applicable SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at light-load conditions; the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the DEMB pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect DEMB to AGND. If FPWM or continuous conduction mode (CCM) operation is desired, tie DEMB to VDDA. See Table 9-4. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in FPWM. A gradual change from DCM to CCM operation provides monotonic start-up performance.

Table 9-4. DEMB Settings

DEMB	FPWM/DEM
VDDA	FPWM
AGND	DEM
External clock	FPWM

9.4.3 Thermal Shutdown

The LM5143 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. Pulls SS1/2 and PG1/2 low
3. Turns off the VCC regulator
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical)

This is a non-latching protection, and as such, the device cycles into and out of thermal shutdown if the fault persists.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM5143 is a synchronous buck controller used to convert a higher input voltage to two lower output voltages. The following sections discuss the design procedure for a dual-output implementation using a specific circuit design example. To expedite and streamline the process of designing of a LM5143-based regulator, a comprehensive *LM5143 Quickstart Calculator* is available for download to assist the designer with component selection for a given application.

10.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The subsequent subsections discuss the following:

- Output inductor
- Input and output capacitors
- Power MOSFETs
- EMI input filter

10.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 15 based on a peak inductor current given by Equation 16.

$$L_O = \frac{V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{15}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{16}$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

10.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics – equivalent series resistance (ESR) and equivalent series inductance (ESL) – take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by Equation 17.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \tag{17}$$

Figure 10-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as quickly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

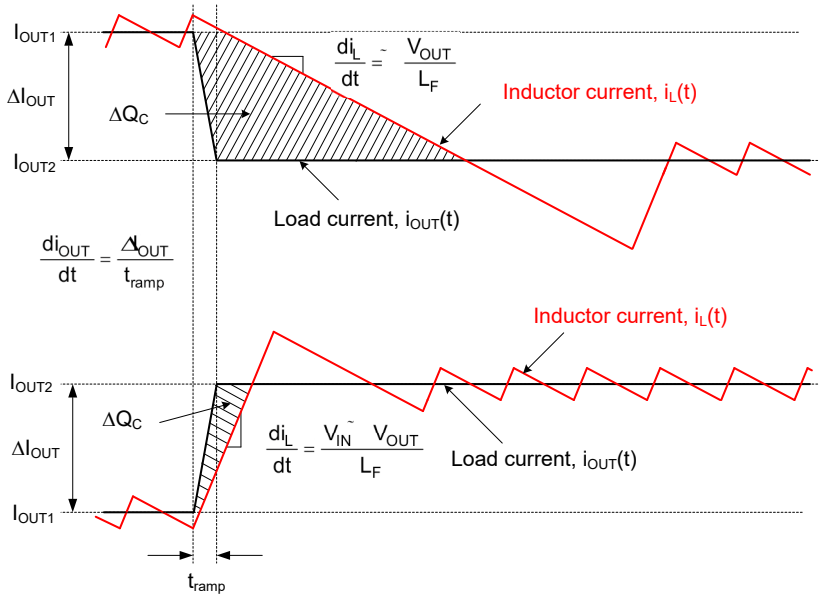


Figure 10-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12-V input to low output voltage (for example, 3.3 V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \tag{18}$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on the package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 17 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice for a 5-V output. Use Equation 18 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid-frequency and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

10.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use Equation 19 to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{19}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors is greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sink I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, use Equation 20 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{20}$$

Use Equation 21 to calculate the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{21}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and four 10-µF 50-V X7R ceramic

decoupling capacitors are usually sufficient for 12-V battery automotive applications. Select the input bulk capacitor based on its ripple current rating and operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The previous equations represent valid calculations when one output is disabled and the other output is fully loaded.

10.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a LM5143 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5 V
- Drain-source voltage rating, BV_{DSS}, is typically 40 V, 60 V, or 80 V, depending on the maximum input voltage.
- Gate charge parameters at V_{GS} = 5 V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 3 V, the 5-V gate drive amplitude of the LM5143 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in Table 10-1, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the *LM5143 Quickstart Calculator*. The calculator is available for download from the LM5143 product folder to assist with power loss calculations.

Table 10-1. MOSFET Power Losses

Power Loss Mode	High-Side MOSFET	Low-Side MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1} \cdot 1.3$	$P_{cond2} = D' \cdot \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2} \cdot 1.3$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	Negligible
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance, and the relevant driver resistance of the LM5143.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this is offset by the stored energy E_{oss2} on C_{oss2}. For more detail, refer to "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs," ECCE 2016.

(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on time (or D interval) and typically incurs most of the switching losses, so it is imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the following:

- Losses due to conduction
- Switching (voltage-current overlap)
- Output charge
- Typically two-thirds of the net loss attributed to body diode reverse recovery

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition dead times. The LM5143, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM5143 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

10.1.1.5 EMI Filter

As expressed by Equation 22, switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{22}$$

An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

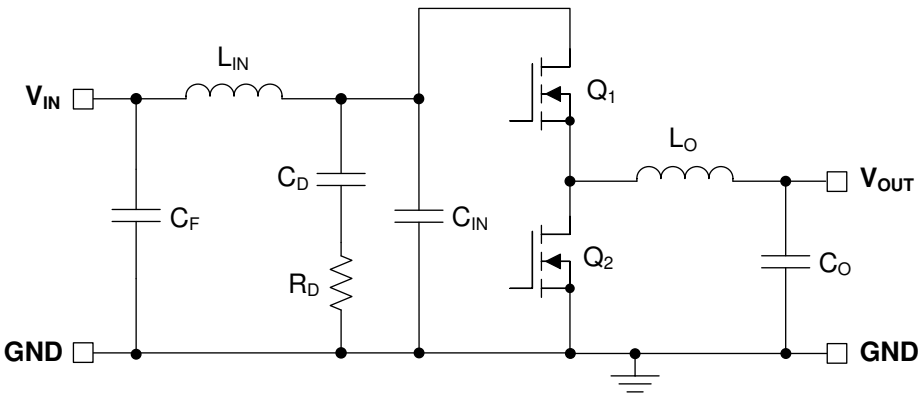


Figure 10-2. Buck Regulator With π-Stage EMI Filter

Referencing the filter schematic in Figure 10-2, the EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.

- The input filter inductance, L_{IN}, is usually selected between 1 µH and 10 µH, but it can be lower to reduce losses in a high-current design.
- Calculate input filter capacitance, C_F.
- Calculate damping capacitance, C_D, and damping resistance, R_D.

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 23.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \cdot F_{SW} \cdot C_{IN}} \cdot \sin\left(\pi \cdot D_{MAX}\right) \cdot \frac{1}{1\ V}\right) - V_{MAX} \tag{23}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification (for example, CISPR 25 Class 5).
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 24.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}}\right)^2 \tag{24}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Use Equation 25 to calculate the resonant frequency of the filter.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \tag{25}$$

The purpose of R_D is to reduce the peak output impedance of the filter at its resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of the filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 26.

$$C_D \geq 4 \cdot C_{IN} \tag{26}$$

Use Equation 27 to select the damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{27}$$

10.1.2 Error Amplifier and Compensation

Figure 10-3 shows a Type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown in Equation 28.

$$G_{EA(open\,loop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{28}$$

The EA high-frequency pole is neglected in Equation 28. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in Equation 29.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \cdot \frac{g_m \cdot R_{O\text{-}EA} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{29}$$

where

- V_{REF} is the feedback voltage reference of 0.6 V.
- g_m is the EA gain transconductance of 1200 µS.
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 64 MΩ.

$$\omega_{Z1} = \frac{1}{R_{COMP} \cdot C_{COMP}} \tag{30}$$

$$\omega_{p1} = \frac{1}{R_{O\text{-}EA} \cdot \left(C_{COMP} + C_{HF} + C_{BW}\right)} \cong \frac{1}{R_{O\text{-}EA} \cdot C_{COMP}} \tag{31}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \cdot \left(C_{COMP} \parallel \left(C_{HF} + C_{BW}\right)\right)} \cong \frac{1}{R_{COMP} \cdot C_{HF}} \tag{32}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, $R_{COMP} << R_{O\text{-}EA}$ and $C_{COMP} >> C_{BW}$ and C_{HF}, so the approximations are valid.

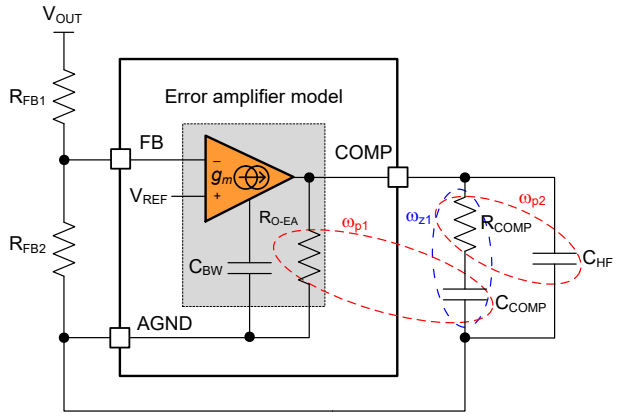


Figure 10-3. Error Amplifier and Compensation Network

10.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation, and test results of an LM5143-powered implementation, see the *TI Designs* reference design library.

10.2.1 Design 1 – 5-V and 3.3-V Dual-Output Buck Regulator for Computing Applications

Figure 10-4 shows the schematic diagram of a dual-output synchronous buck regulator with output voltages setpoints of 3.3 V and 5 V and a rated load current of 7 A for each output. In this example, the target half-load and full-load efficiencies are 91% and 90%, respectively, based on a nominal input voltage of 12 V that ranges from 3.5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve efficiency.

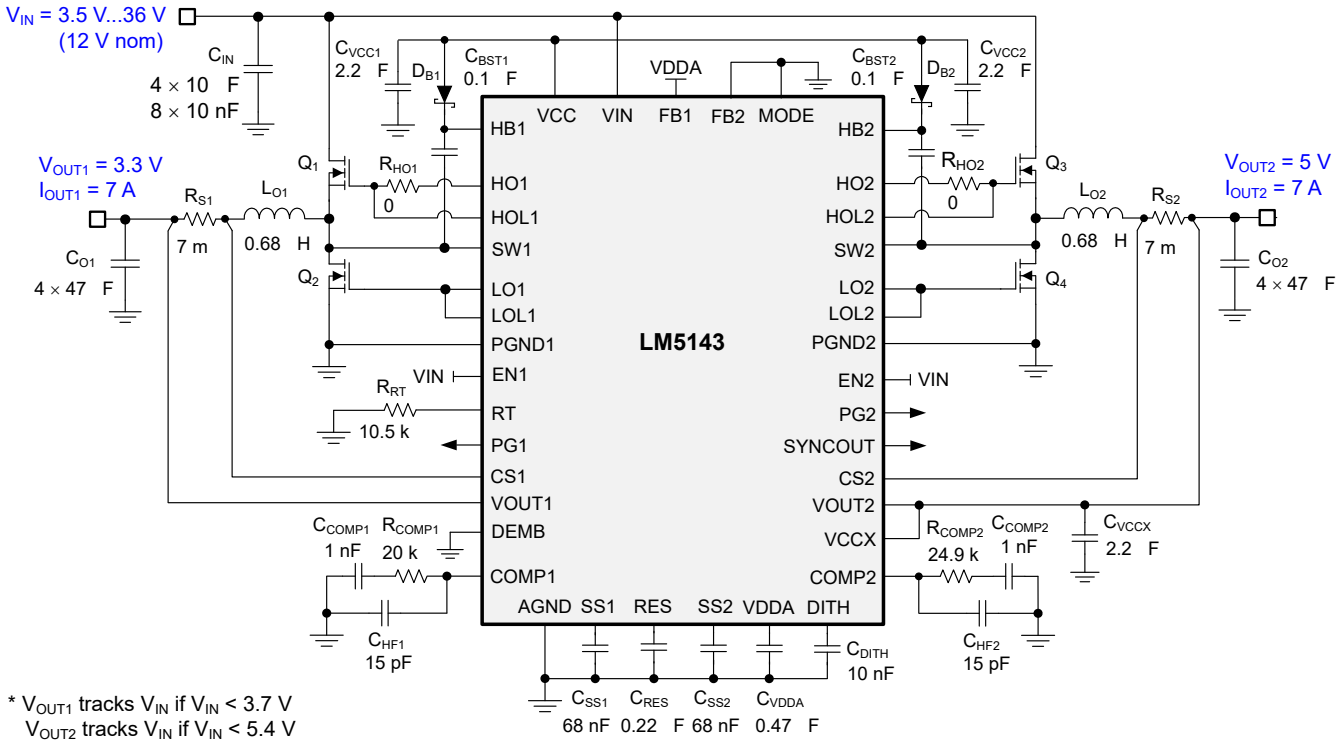


Figure 10-4. Application Circuit 1 With LM5143 Dual-Output Buck Regulator at 2.1 MHz

Note

This and subsequent design examples are provided herein to showcase the LM5143 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See Section 10 for more details.

10.2.1.1 Design Requirements

Table 10-2 shows the intended input, output, and performance parameters for this design example.

Table 10-2. Design Parameters

Design Parameter	Value
Input voltage range (steady state)	8 V to 18 V
Min transient input voltage (cold crank)	3.5 V
Max transient input voltage (load dump)	36 V
Output voltages	3.3 V, 5 V
Output currents	7 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Standby current, output 1 enabled, no load	< 50 µA
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start times are set at 2 ms by 68-nF soft-start capacitors.

The selected buck regulator powertrain components are cited in Table 10-3, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 10.1.1.4. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

Table 10-3. List of Materials for Application Circuit 1

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm	Würth Elektronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm	Würth Elektronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.7 × 6.5 × 3.1 mm	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W	Susumu	KRL2012E-M-R007
U_1	1	LM5143 65-V dual-channel/phase synchronous buck controller	Texas Instruments	LM5143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5143 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the *LM5143 Quickstart Calculator* available for download from the LM5143 product folder.

10.2.1.2.3 Inductor Calculation

1. Use Equation 33 to calculate the required buck inductance for each channel based on a 30% inductor ripple current at nominal input voltages.

$$L_{O1} = \frac{V_{OUT1}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT1}}{\Delta I_L \cdot F_{SW}} \right) = \frac{3.3\,V}{12\,V} \cdot \left(\frac{12\,V - 3.3\,V}{2.1A \cdot 2.1MHz} \right) = 0.54 \;\; H$$

$$L_{O2} = \frac{V_{OUT2}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT2}}{\Delta I_L \cdot F_{SW}} \right) = \frac{5\,V}{12\,V} \cdot \left(\frac{12\,V - 5\,V}{2.1A \cdot 2.1MHz} \right) = 0.66 \;\; H \quad (33)$$

2. Select a standard inductor value of 0.68 µH for both channels. Use Equation 34 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM5143 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO1(PK)} = I_{OUT1} + \frac{\Delta I_{LO1}}{2} = I_{OUT1} + \frac{V_{OUT1}}{2 \cdot L_{O1} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN(max)}} \right) = 7\,A + \frac{3.3\,V}{2 \cdot 0.68 \;\; H \cdot 2.1MHz} \cdot \left(1 - \frac{3.3\,V}{18\,V} \right) = 7.94\,A$$

$$I_{LO2(PK)} = I_{OUT2} + \frac{\Delta I_{LO2}}{2} = I_{OUT2} + \frac{V_{OUT2}}{2 \cdot L_{O2} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN(max)}} \right) = 7\,A + \frac{5\,V}{2 \cdot 0.68 \;\; H \cdot 2.1MHz} \cdot \left(1 - \frac{5\,V}{18\,V} \right) = 8.27\,A \quad (34)$$

3. Based on Equation 10, use Equation 35 to cross-check the inductance to set a slope compensation equal to the ideal one times the inductor current downslope.

$$L_{O1(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{3.3\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.46 \;\; H$$

$$L_{O2(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{5\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.69 \;\; H \quad (35)$$

10.2.1.2.4 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 20% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistances using Equation 36.

$$R_{S1} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO1(PK)}} = \frac{73\,mV}{1.2 \cdot 7.94\,A} = 7.66\,m\Omega$$

$$R_{S2} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO2(PK)}} = \frac{73\,mV}{1.2 \cdot 8.27\,A} = 7.36\,m\Omega \quad (36)$$

where

- $V_{CS(th)}$ is the 73-mV current limit threshold.

2. Select a standard resistance value of 7 mΩ for both shunts. A 0508 footprint component with wide aspect ratio termination design provides 1-W power rating, low parasitic series inductance, and compact PCB layout. Carefully observe the layout guidelines to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at [CS1, VOUT1] and [CS2, VOUT2].
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM5143.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay of $t_{CS-DELAY}$ of 40 ns, use Equation 37 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO1(PK-SC)} = I_{LO2(PK-SC)} = \frac{V_{CS(th)}}{R_{S1}} + \frac{V_{IN(max)} \cdot t_{CS-DELAY}}{L_{O1}} = \frac{73\,mV}{7\,m\Omega} + \frac{18\,V \cdot 40\,ns}{0.68\ \ H} = 11.49\,A \quad (37)$$

6. Based on this result, select an inductor for each channel with saturation current greater than 12 A across the full operating temperature range.

10.2.1.2.5 Output Capacitors

1. Use Equation 38 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 1.5% (50 mV for a 3.3-V output).

$$C_{OUT1} \geq \frac{L_{O1} \cdot \Delta I_{OUT1}{}^2}{\left(V_{OUT1} + \Delta V_{OVERSHOOT1}\right)^2 - V_{OUT1}{}^2} = \frac{0.68\ \ H \cdot (7\,A)^2}{(3.3\,V + 50\,mV)^2 - (3.3\,V)^2} = 100.2\ \ F$$

$$C_{OUT2} \geq \frac{L_{O2} \cdot \Delta I_{OUT2}{}^2}{\left(V_{OUT2} + \Delta V_{OVERSHOOT2}\right)^2 - V_{OUT2}{}^2} = \frac{0.68\ \ H \cdot (7\,A)^2}{(5\,V + 75\,mV)^2 - (5\,V)^2} = 44.1\ \ F \quad (38)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47-µF, 6.3-V, X7R, 1210 ceramic output capacitors for each channel. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use Equation 39 to estimate the peak-peak output voltage ripple of channel 1 at nominal input voltage.

$$\Delta V_{OUT1} = \sqrt{\left(\frac{\Delta I_{LO1}}{8 \cdot F_{SW} \cdot C_{OUT1}}\right)^2 + \left(R_{ESR} \cdot \Delta I_{LO1}\right)^2} = \sqrt{\left(\frac{1.89\,A}{8 \cdot 2.1\,MHz \cdot 130\ \ F}\right)^2 + \left(1\,m\Omega \cdot 1.89\,A\right)^2} \approx 2\,mV \quad (39)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 130 µF is the total effective (derated) ceramic output capacitance at 3.3 V.

4. Use Equation 40 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO1(RMS)} = \frac{\Delta I_{LO1}}{\sqrt{12}} = \frac{1.89\,A}{\sqrt{12}} = 0.55\,A$$

$$I_{CO2(RMS)} = \frac{\Delta I_{LO2}}{\sqrt{12}} = \frac{2.53\,A}{\sqrt{12}} = 0.73\,A \quad (40)$$

10.2.1.2.6 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Worst case input ripple for a two-channel buck regulator typically corresponds to when one channel operates at full load and the other channel is disabled or operates at no load. Use Equation 41 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(RMS)} = I_{OUT1} \cdot \sqrt{D \cdot (1-D)} = 7\,A \cdot \sqrt{0.5 \cdot (1-0.5)} = 3.5\,A \quad (41)$$

3. Use Equation 42 to find the required input capacitance.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT1}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT1})} = \frac{0.5 \cdot (1-0.5) \cdot 7\,A}{2.1MHz \cdot (120\,mV - 2m\Omega \cdot 7\,A)} = 7.8\ \ F \quad (42)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select two 10-µF, 50-V, X7R, 1210 ceramic input capacitors for each channel. Place these capacitors adjacent to the relevant power MOSFETs.
5. Use four 10-nF, 50-V, X7R, 0603 ceramic capacitors near each high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100 MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower EMI signature. Refer to Figure 12-2 in Section 12.1 for more detail.

10.2.1.2.7 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified open-loop gain crossover frequency, f_C, of 60 kHz, use Equation 43 to calculate R_{COMP1}, assuming an effective output capacitance of 130 µF. Select R_{COMP1} of 20 kΩ.

$$R_{COMP1} = 2 \cdot \pi \cdot f_C \cdot \frac{V_{OUT}}{V_{REF}} \cdot \frac{R_S \cdot G_{CS}}{g_m} \cdot C_{OUT} = 2 \cdot \pi \cdot 60kHz \cdot \frac{3.3\,V}{0.6\,V} \cdot \frac{7m\Omega \cdot 12}{1200\ \ S} \cdot 130\ \ F = 18.9k\Omega \quad (43)$$

2. Calculate C_{COMP1} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Select a C_{COMP1} capacitor of 1 nF.

$$C_{COMP1} = \frac{10}{2 \cdot \pi \cdot f_C \cdot R_{COMP1}} = \frac{10}{2 \cdot \pi \cdot 60kHz \cdot 20\ k\Omega} = 1.3nF \quad (44)$$

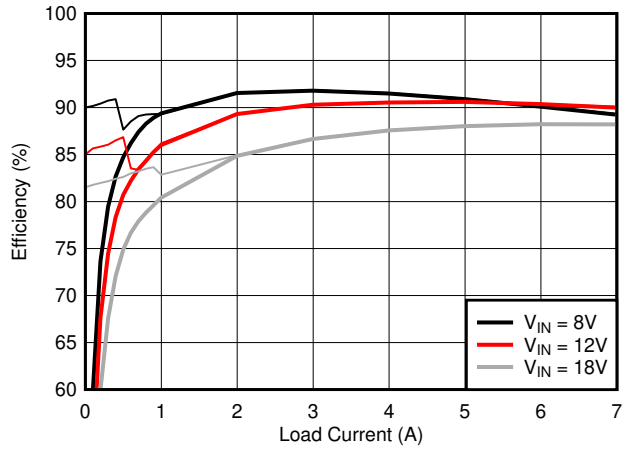
3. Calculate C_{HF1} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP. Select a C_{HF1} capacitor of 15 pF.

$$C_{HF1} = \frac{1}{2 \cdot \pi \cdot f_{ESR} \cdot R_{COMP1}} = \frac{1}{2 \cdot \pi \cdot 500\,kHz \cdot 20\,k\Omega} = 15.9\,pF \quad (45)$$

Note

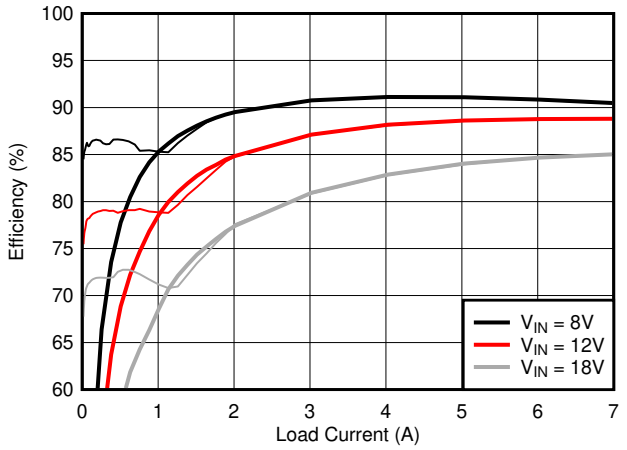
Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

10.2.1.3 Application Curves



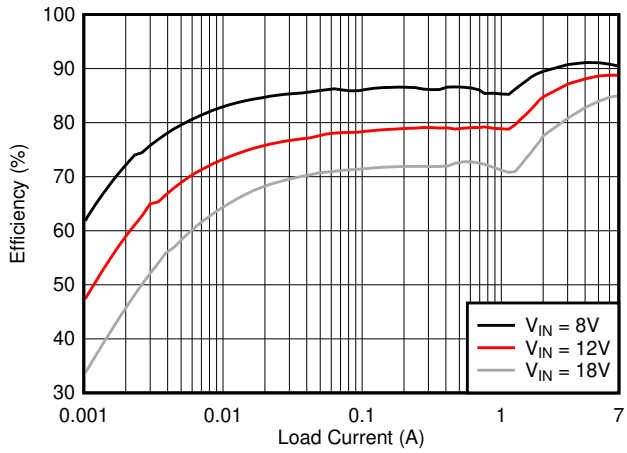
Channels loaded equally

Figure 10-5. Efficiency Versus I_{OUT}



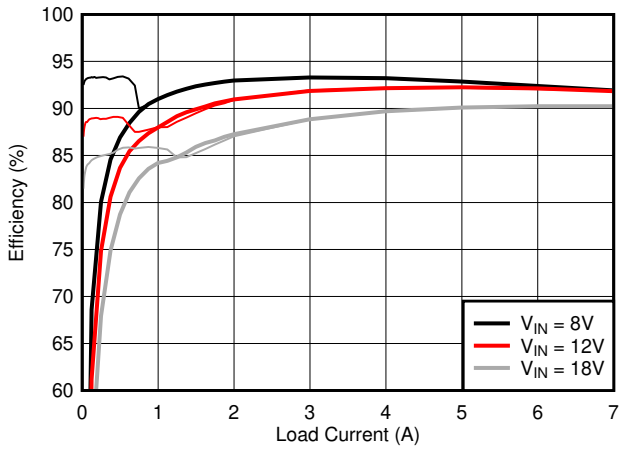
3.3-V output, channel 2 disabled

Figure 10-6. Efficiency Versus I_{OUT}



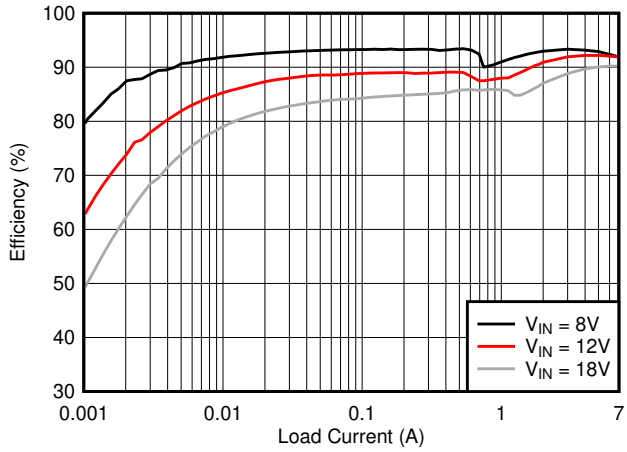
3.3-V output, channel 2 disabled

Figure 10-7. Efficiency Versus I_{OUT}, Log Scale



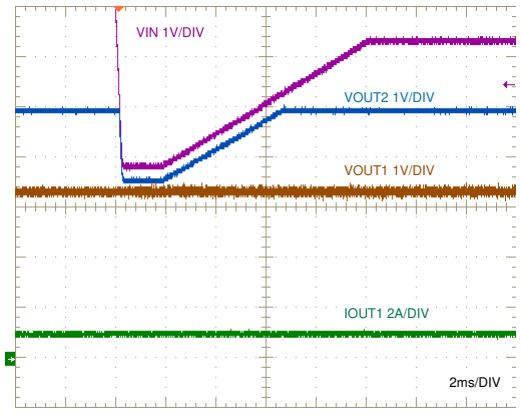
5-V output, channel 1 disabled

Figure 10-8. Efficiency Versus I_{OUT}



5-V output, channel 1 disabled

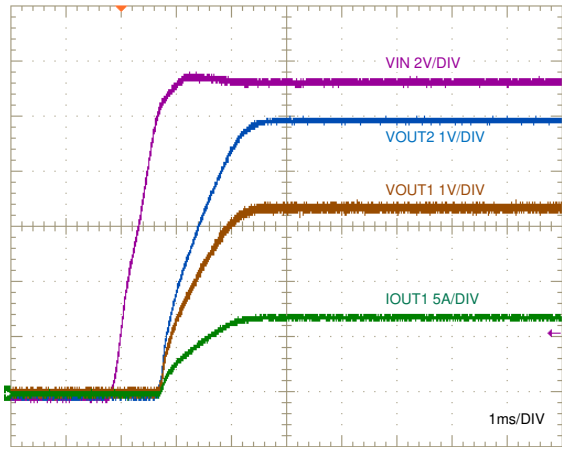
Figure 10-9. Efficiency Versus I_{OUT}, Log Scale



1-A loads

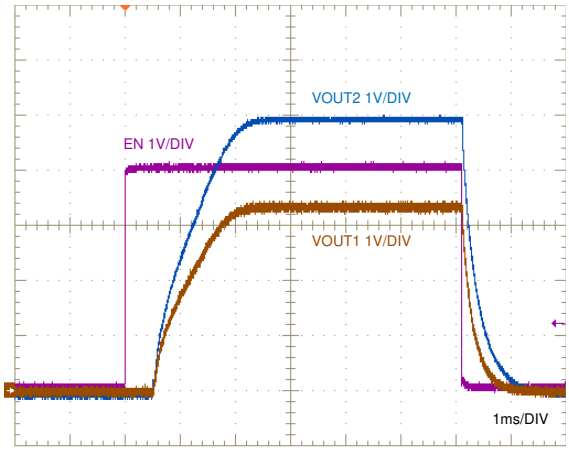
Figure 10-10. Cold-Crank Response to V_{IN} = 3.8 V

10.2.1.3 Application Curves (continued)



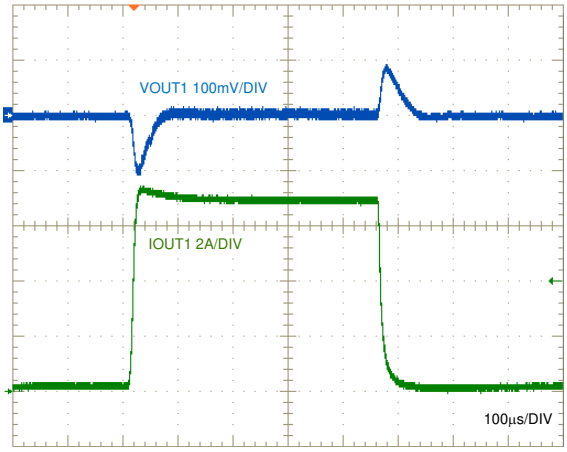
V_{IN} step to 12 V 7-A resistive loads

Figure 10-11. Start-Up Characteristic



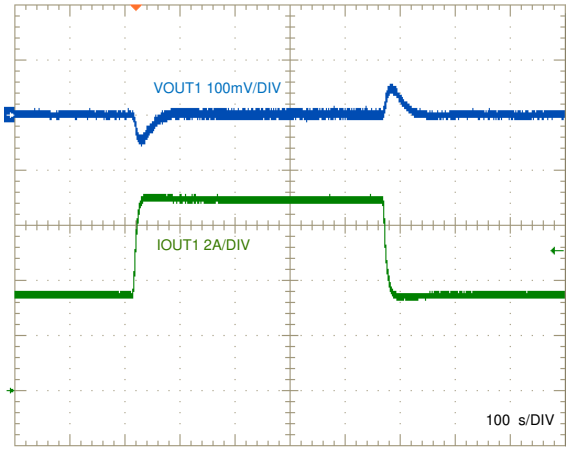
V_{IN} = 12 V 7-A resistive loads

Figure 10-12. ENABLE ON and OFF Characteristic



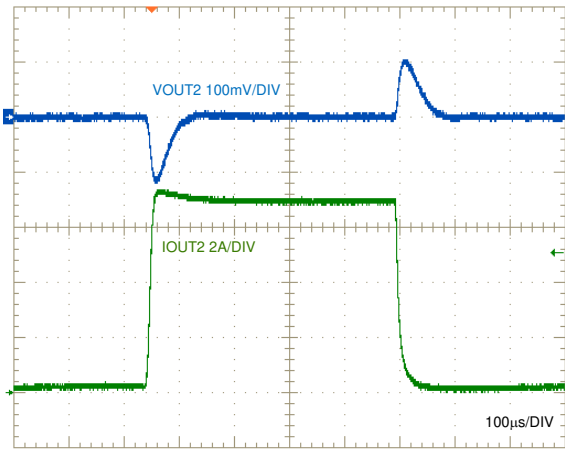
V_{IN} = 12 V FPWM

Figure 10-13. Load Transient, 3.3-V Output, 0 A to 7 A



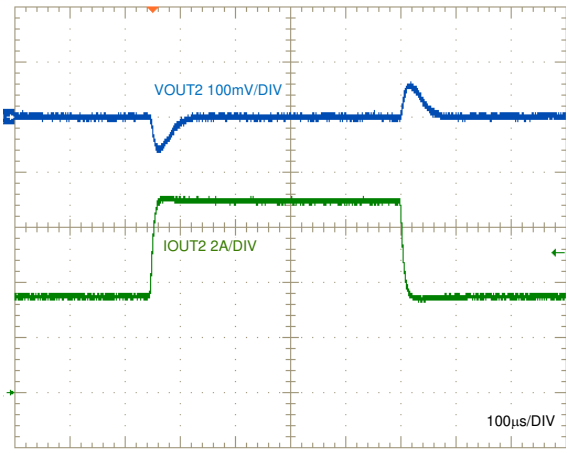
V_{IN} = 12 V FPWM

Figure 10-14. Load Transient, 3.3-V Output, 3.5 A to 7 A



V_{IN} = 12 V FPWM

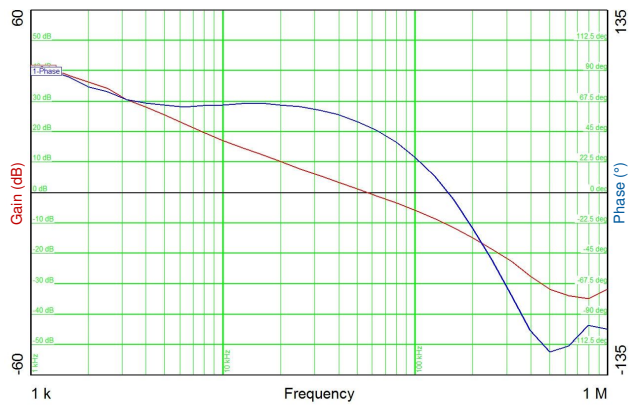
Figure 10-15. Load Transient, 5-V Output, 0 A to 7 A



V_{IN} = 12 V FPWM

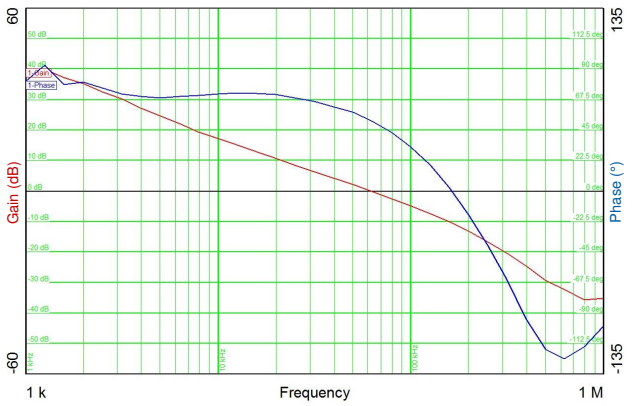
Figure 10-16. Load Transient, 5-V Output, 3.5 A to 7 A

10.2.1.3 Application Curves (continued)



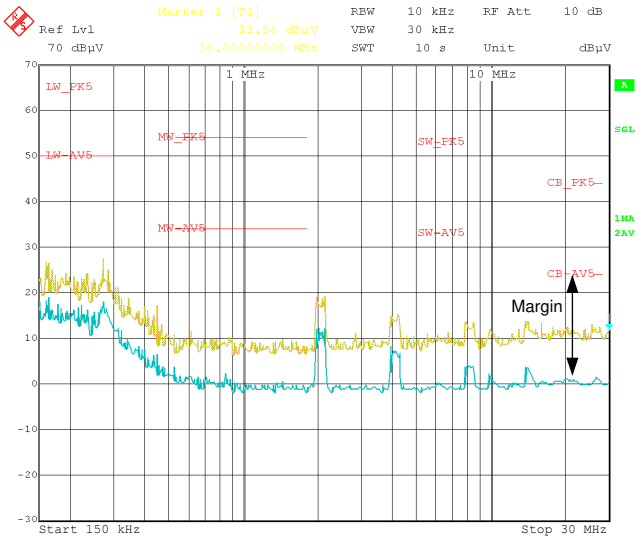
V_{IN} = 12 V 7-A resistive load

Figure 10-17. Bode Plot, 3.3-V Output



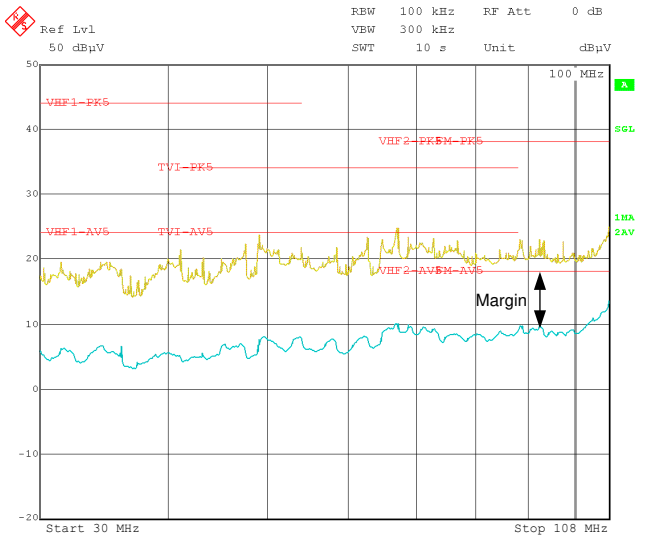
V_{IN} = 12 V 7-A resistive load

Figure 10-18. Bode Plot, 5-V Output



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

Figure 10-19. CISPR 25 Class 5 Conducted EMI, 150 kHz to 30 MHz



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

Figure 10-20. CISPR 25 Class 5 Conducted EMI, 30 MHz to 108 MHz

10.2.2 Design 2 – Two-Phase, 15-A, 2.1-MHz Single-Output Buck Regulator for Server Applications

Figure 10-21 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5 V and rated load current of 15 A. In this example, the target half-load and full-load efficiencies are 93% and 91%, respectively, based on a nominal input voltage of 12 V that ranges from 5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve light-load efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB1 to VDDA.

Note

See the *LM5143-Q1 4-phase Buck Regulator Design for Automotive ADAS Applications* application report for a four-phase, 30-A version of this design.

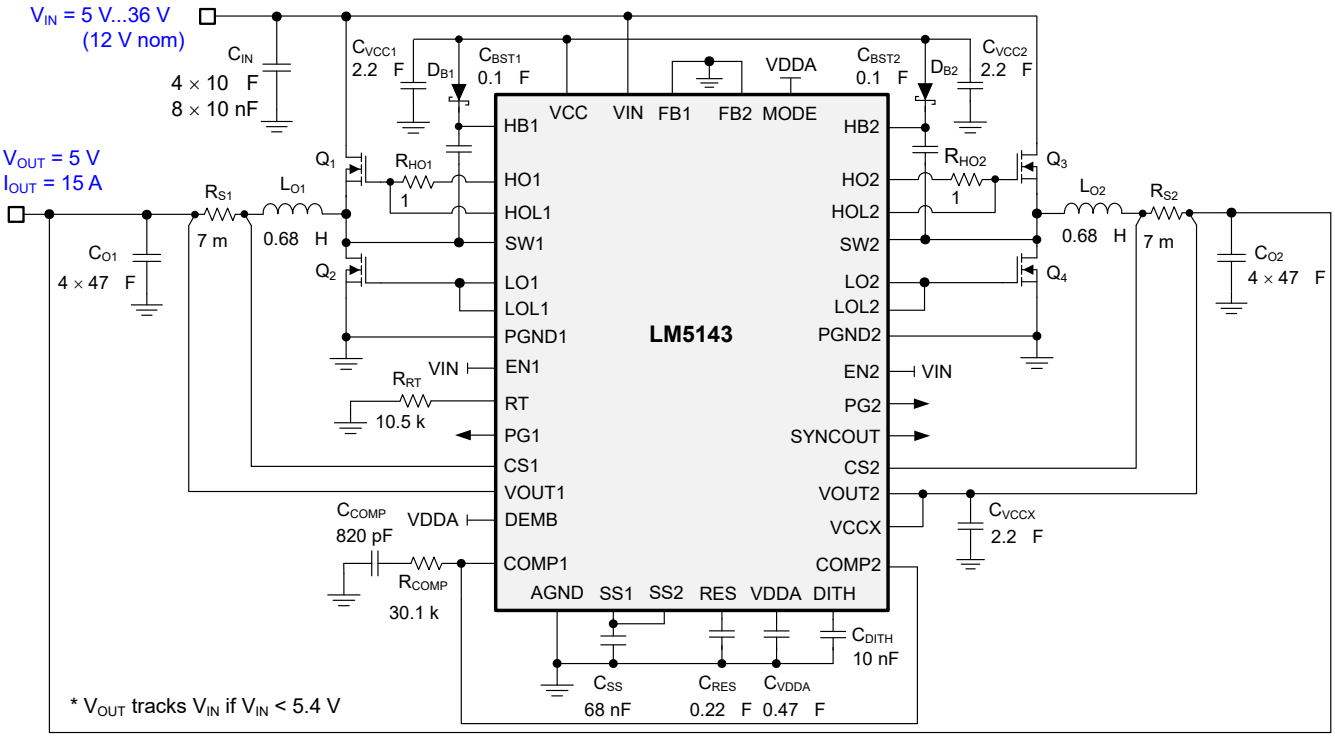


Figure 10-21. Application Circuit 2 With LM5143 Two-Phase Buck Regulator at 2.1 MHz

10.2.2.1 Design Requirements

Table 10-4 shows the intended input, output, and performance parameters for this automotive application design example.

Table 10-4. Design Parameters

Design Parameter	Value
Input voltage range (steady state)	5 V to 18 V
Minimum transient input voltage (cold crank)	5 V
Maximum transient input voltage (load dump)	36 V
Output voltage	5 V
Output current	15 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start time is set at 2 ms by a 68-nF soft-start capacitor.

The selected buck regulator powertrain components are cited in Table 10-5, and many of the components are available from multiple vendors. Similar to design 1, this design uses a low-DCR, composite inductor and ceramic output capacitor implementation.

Table 10-5. List of Materials for Application Circuit 2

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm	Würth Elekronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm	Würth Elekronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.7 × 6.5 × 3.1 mm	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W	Susumu	KRL2012E-M-R007
U_1	1	LM5143 65-V dual-channel/phase synchronous buck controller	Texas Instruments	LM5143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.2.2 Detailed Design Procedure

See Section 10.2.1.2.

10.2.2.3 Application Curves

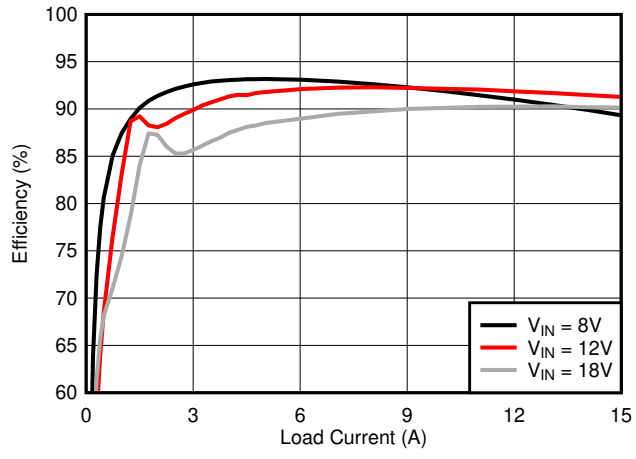
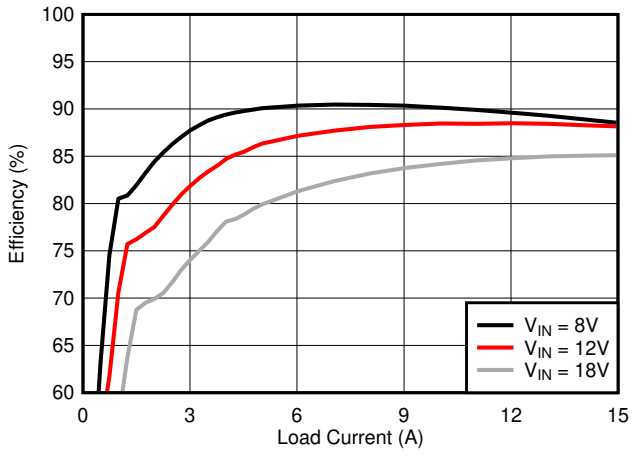


Figure 10-22. Efficiency Versus I_{OUT}, 5-V Output



Configure the regulator as a 3.3-V output by tying FB1 to VDDA.

Figure 10-23. Efficiency Versus I_{OUT}, 3.3-V Output

10.2.3 Design 3 – Two-Phase, 50-A, 300-kHz Single-Output Buck Regulator for ASIC Power Applications

Figure 10-24 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5 V. The expected DC load current is 35 A with transients up to 50 A. In this example, the target efficiency at 35 A is 94.5% using a power stage optimized for a nominal input voltage of 48 V. The switching frequency is set at 300 kHz by resistor R_{RT}, and inductor DCR current sensing is used to mitigate shunt-related losses at high current. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve light-load efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB1 to VDDA.

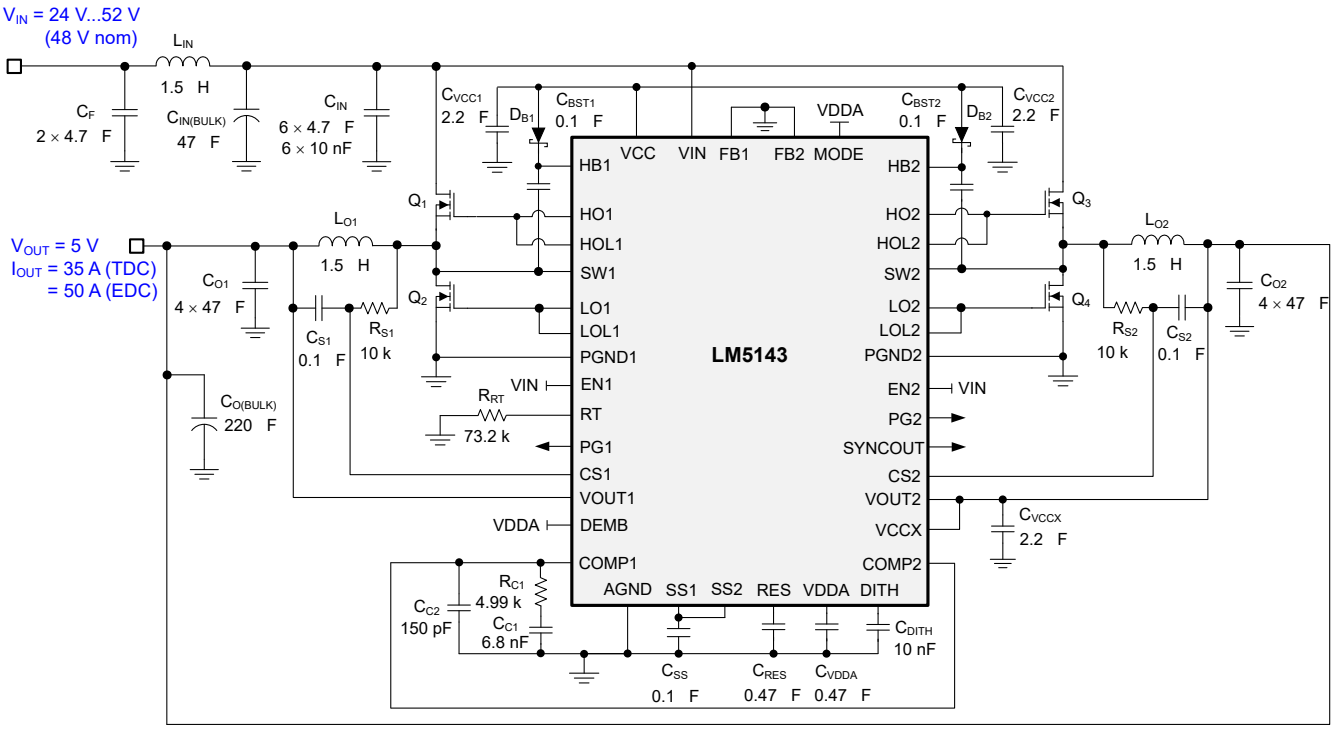


Figure 10-24. Application Circuit 3 With LM5143 Two-Phase Buck Regulator at 300 kHz

10.2.3.1 Design Requirements

Table 10-6 shows the intended input, output, and performance parameters for this design example.

Table 10-6. Design Parameters

Design Parameter	Value
Nominal input voltage	48 V
Input voltage range (steady state)	24 V to 52 V
Output voltage	5 V
Thermal design current (TDC)	35 A
Electrical design current (EDC)	50 A
Switching frequency	300 kHz
Output voltage regulation	±1%
Shutdown current	4 µA

The switching frequency is set at 300 kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 45 kHz with a phase margin greater than 50°. The output voltage soft-start time is set at 3 ms by a 100-nF soft-start capacitor. FPWM operation provides constant switching frequency over the full load current range for predictable EMI performance and optimal load transient response.

The selected buck regulator powertrain components are cited in Table 10-7, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 10.1.1.4. This design uses a low-DCR composite inductor and ceramic output capacitor implementation.

Table 10-7. List of Materials for Application Circuit 3

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	8	4.7 µF, 100 V, X7R, 1210, ceramic	AVX	12101C475K4Z2A
			TDK	CNA6P1X7R2A475K
		4.7 µF, 100 V, X7S, 1210, ceramic	Murata	GCM32DC72A475KE02L
			TDK	CGA6M3X7S2A475K
		10 µF, 75 V, X7R, 1210, ceramic	TDK	CGA6P1X7R1N106K
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
	6	100 µF, 6.3 V, X7S, 1210, ceramic	Murata	GRT32EC70J107ME13L
$C_{O(BULK)}$	1	220 µF, 10 V, 25 mΩ, 7343, polymer tantalum	Kemet	T598D227M010ATE025
			AVX	TCQD227M010R0025E
L_{O1}, L_{O2}	2	1.5 µH, 1.28 mΩ, 46.7 A, 13.3 × 12.8 × 8 mm	Cyntec	VCUD128T-1R5MS8
		1.5 µH, 2.3 mΩ, 35 A, 13.5 × 12.6 × 6.5 mm	Cyntec	VCMV136E-1R5MN2
		1.5 µH, 2.8 mΩ, 32.8 A, 13 × 12.5 × 6.5 mm	TDK	SPM12565VT-1R5M-D
		1.5 µH, 2.3 mΩ, 55.3 A, 13.5 × 12.5 × 6.2 mm	Würth Elektronik	744373965015
Q_1, Q_3	2	60 V, 11 mΩ, 4.5 nC, DFN5	Onsemi	NVMFS5C673NL
Q_2, Q_4	2	60 V, 2.6 mΩ, 24 nC, DFN5	Onsemi	NVMFS5C628NL
U_1	1	LM5143 65-V dual-channel/phase synchronous buck controller	Texas Instruments	LM5143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.3.2 Detailed Design Procedure

See Section 10.2.1.2.

10.2.3.3 Application Curves

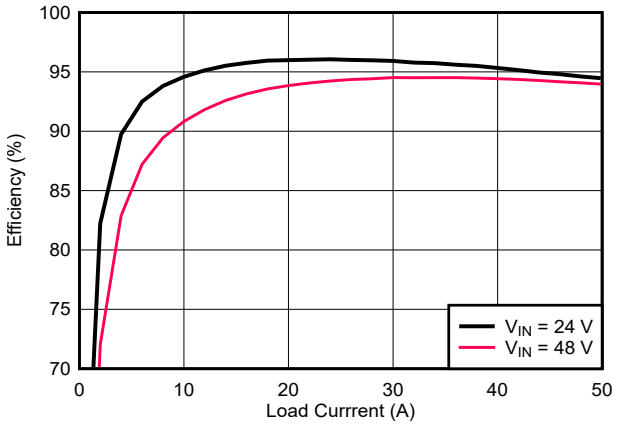


Figure 10-25. Efficiency Versus I_{OUT}

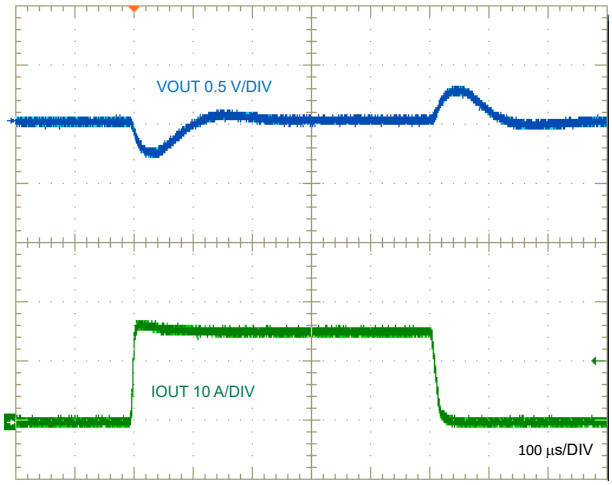


Figure 10-26. Load Transient, 0 A to 15 A

11 Power Supply Recommendations

The LM5143 buck controller is designed to operate over a wide input voltage range of 3.5 V to 65 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Use Equation 46 to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \tag{46}$$

where

- η is the efficiency.

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse effect on regulator operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the affects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters Application Report* provides helpful suggestions when designing an input filter for any switching regulator.

12 Layout

12.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM5143. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of Figure 12-1. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3, respectively, in Figure 12-1.

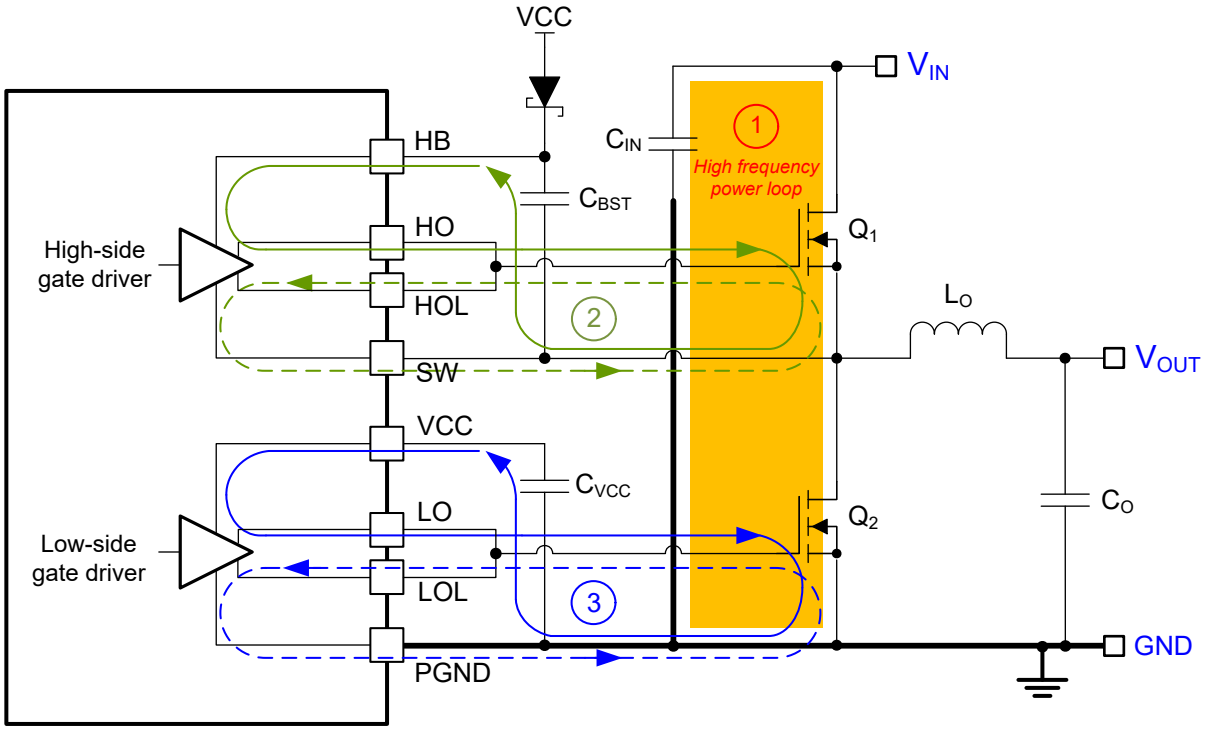


Figure 12-1. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

12.1.1 Power Stage Layout

- Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
- The DC/DC regulator has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and optimize switching performance.
  - Loop 1: The most important loop area to minimize is the path from the input capacitor or capacitors through the high-side and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 in Figure 12-1.
  - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

- The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
- Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
- The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in Figure 12-1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50 MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

12.1.2 Gate-Drive Layout

The LM5143 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turn-on, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop 2 of Figure 12-1.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop 3 of Figure 12-1.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO1/2, HOL1/2, LO1/2, and LOL1/2 to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 4.25 A. Use 0.65-mm (25 mils) or wider traces. Use via or vias, if necessary, of at least 0.5-mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LM5143 to the high-side MOSFET, taking advantage of flux cancellation.
- Minimize the current loop path from the VCC and HB pins through their respective capacitors as these provide the high instantaneous current, up to 4.25 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the HB and SW pins of the LM5143 to minimize the area of loop 2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM5143 to minimize the area of loop 3 associated with the low-side driver.

12.1.3 PWM Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP1/2, FB1/2, CS1/2, SS1/2, RES, and RT away from high-voltage switching nodes such as SW1/2, HO1/2, LO1/2, or HB1/2 to avoid mutual coupling.

Use internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Locate the upper and lower feedback resistors (if required) close to the respective FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the required output voltage sense point or points at the load or loads.
- Route the CS1/2 and VOUT1/2 traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used).
- Minimize the loop area from the VCC1/2 and VIN pins through their respective decoupling capacitors to the relevant PGND pins. Locate these capacitors as close as possible to the LM5143.

12.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM5143 controller is available in a small 6-mm × 6-mm 40-pin VQFN (RHA) PowerPAD package to cover a range of application requirements. The *Thermal Information* summarizes the thermal metrics of this package.

The 40-pin VQFNP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LM5143 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LM5143 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multilayer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the respective SW planes, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

12.1.5 Ground Plane Design

As mentioned previously, using one or more of the inner PCB layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND1 and PGND2 pins to the system ground plane using an array of vias under the exposed pad. Also connect the PGND1 and PGND2 pins directly to the return terminals of the input and output capacitors. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND1/2, VIN and SW1/2 can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

12.2 Layout Example

Based on the *LM5143-Q1EVM-2100* design, Figure 12-2 shows a single-sided layout of a dual-output synchronous buck regulator. Each power stage is surrounded by a GND pad geometry to connect an EMI shield if needed. The design uses layer 2 of the PCB as a power-loop return path directly underneath the top layer to create a low-area switching power loop of approximately 2 mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing. Refer to the *LM5143-Q1EVM-2100 Evaluation Module User's Guide* for more detail.

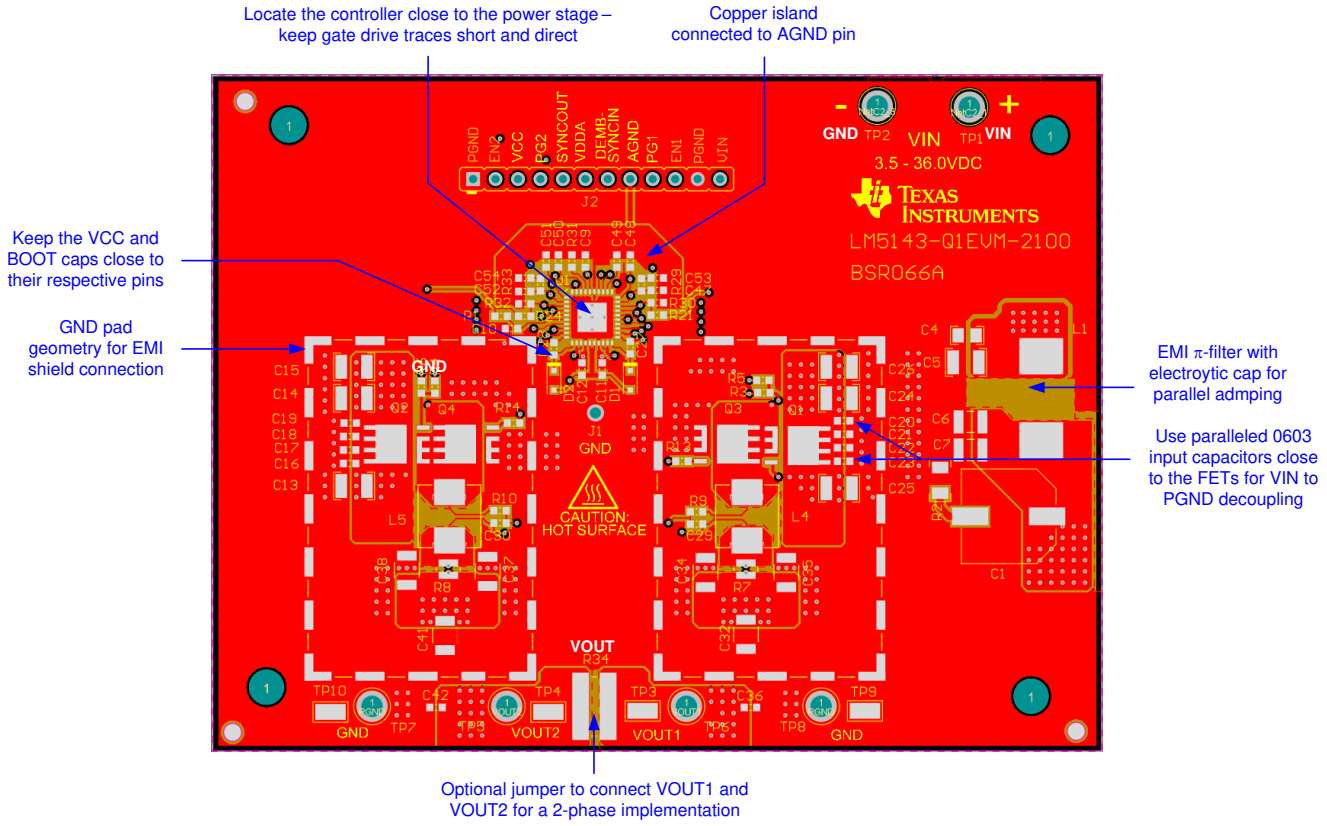


Figure 12-2. PCB Top Layer

As shown in Figure 12-3, the high-frequency power loop current of one channel flows through MOSFETs Q2 and Q4, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C16 through C19. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic inductance. Figure 12-4 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in Figure 12-3, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q2.

Four 10-nF input capacitors with small 0402 or 0603 case size are placed in parallel very close to the drain of each high-side MOSFET. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the layer-2 GND plane with multiple 12-mil (0.3-mm) diameter vias, further minimizing parasitic loop inductance.

Additional steps used in this layout example include:

- Keep the SW connection from the power MOSFETs to the inductor (for each channel) at minimum copper area to reduce radiated EMI.
- Locate the controller close to the gate terminals of the MOSFETs such that the gate drive traces are routed short and direct.

- Create an analog ground plane near the controller for sensitive analog components. The analog ground plane for AGND and power ground planes for PGND1 and PGND2 must be connected at a single point directly under the IC – at the die attach pad (DAP).

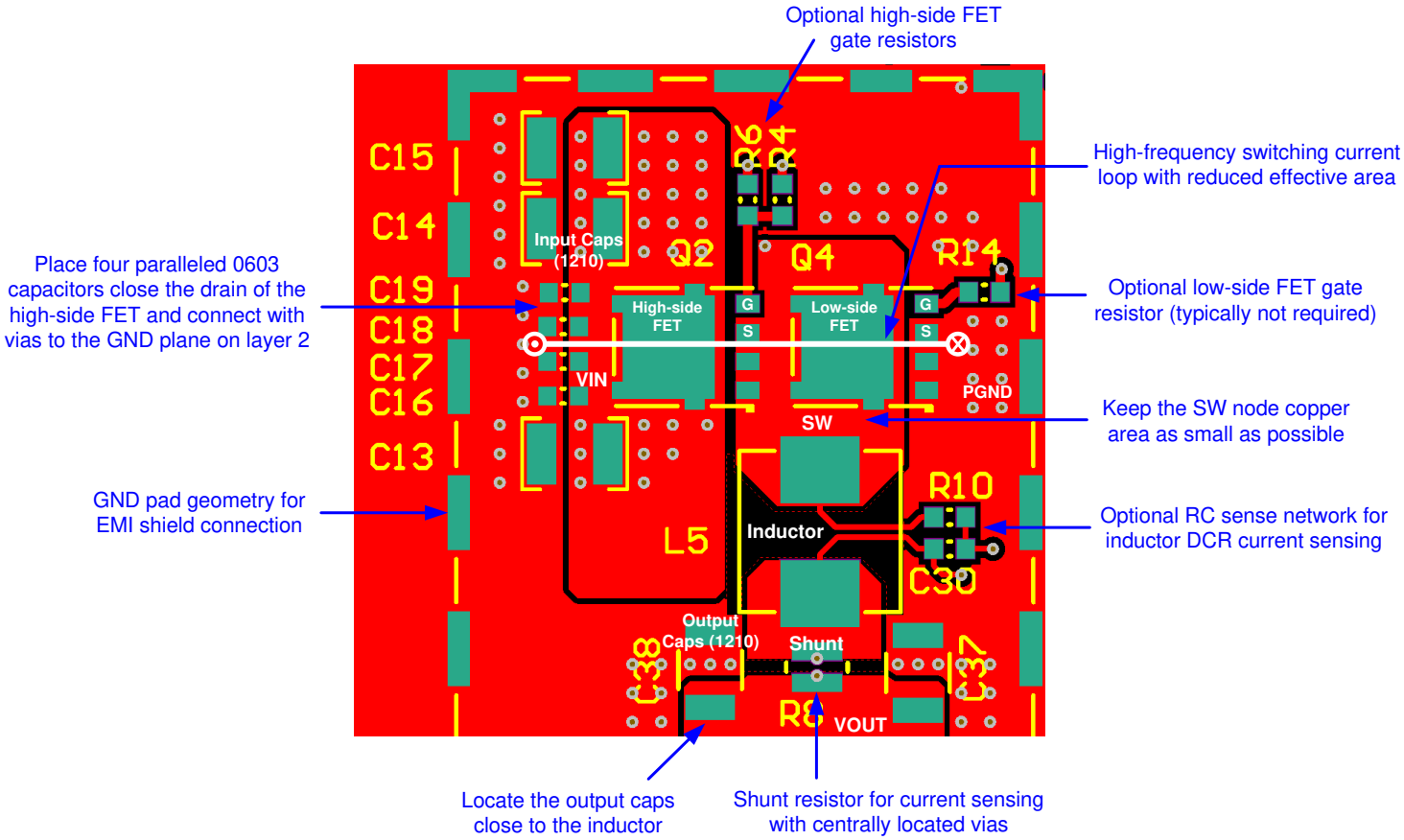
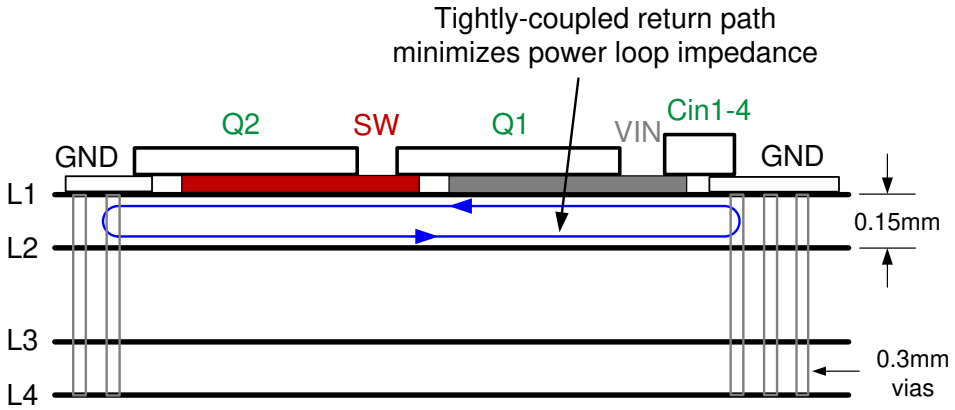


Figure 12-3. Power Stage Component Layout



Note

See the *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application report for more detail.

Figure 12-4. PCB Stack-up Diagram With Low L1-L2 Intra-layer Spacing

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.1.2 Development Support

With an input operating voltage as low as 3.5 V and up to 100 V as specified in Table 13-1, the LM(2)514x family of synchronous buck controllers from TI provides scalability and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF).

Table 13-1. Synchronous Buck DC/DC Controller Family

DC/DC Controller	Single or Dual	V_{IN} Range	Control Method	Gate Drive Voltage	Sync Output	EMI Mitigation
LM25141	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM25143	Dual	3.5 V to 42 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM25145	Single	6 V to 42 V	Voltage mode	7.5 V	180° phase shift	N/A
LM25148	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS
LM25149	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS, AEF
LM5141	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM5145	Single	6 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5146	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5148	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS
LM5149	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS, AEF

For development support, see the following:

- *LM5143 Quickstart Calculator*
- *LM5143 Simulation Models*
- *TI Reference Design Library*
- *WEBENCH® Design Center*
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series
- TI Designs:
  - *Automotive wide V_{IN} front-end reference design for digital cockpit processing units*
- Technical Articles:
  - *High-density PCB layout of DC/DC converters*
  - *Synchronous buck controller solutions support wide V_{IN} performance and flexibility*
  - *How to use slew rate for EMI control*
  - *How to reduce EMI and shrink power-supply size with an integrated active EMI filter*

13.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5143 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- User's Guides:
  - *LM5143-Q1 Synchronous Buck Controller EVM*
  - *LM5140-Q1 Synchronous Buck Controller High Density EVM*
  - *LM5141-Q1 Synchronous Buck Controller EVM*
  - *LM5146-Q1 EVM User's Guide*
  - *LM5145 EVM User's Guide*
- Application Reports:
  - *LM5143-Q1 Synchronous Buck Controller High-Density 4-Phase Design*
  - *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Technical Briefs:
  - *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
  - *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators*
- White Papers:
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*
- E-Book:
  - *An Engineer's Guide To EMI In DC/DC Regulators*

13.2.1.1 PCB Layout Resources

- Application Reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - *AN-1149 Layout Guidelines for Switching Power Supplies*
  - *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - *Constructing Your Power Supply – Layout Considerations*

13.2.1.2 Thermal Design Resources

- Application Reports:
  - *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - *Semiconductor and IC Package Thermal Metrics*
  - *Thermal Design Made Simple with LM43603 and LM43602*
  - *PowerPAD™ Thermally Enhanced Package*
  - *PowerPAD Made Easy*
  - *Using New Thermal Metrics*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
PowerPAD™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
is a registered trademark of TI.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5143RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	LM5143RH AR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5143 :

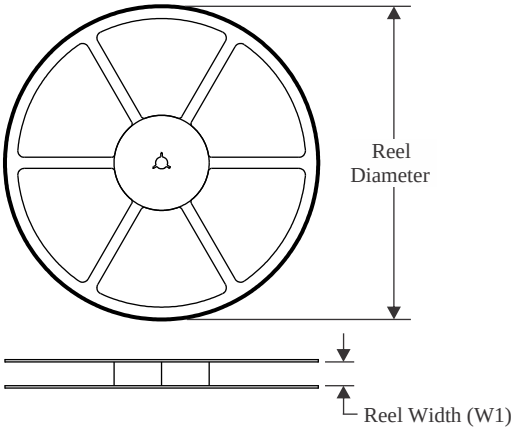
- Automotive : LM5143-Q1

NOTE: Qualified Version Definitions:

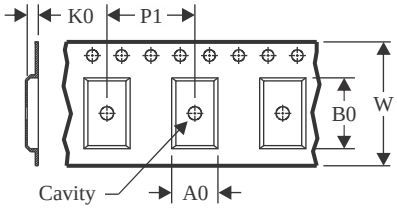
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

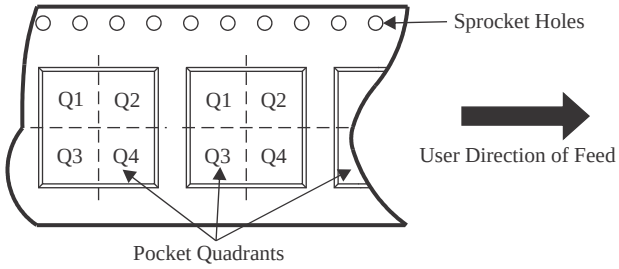


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

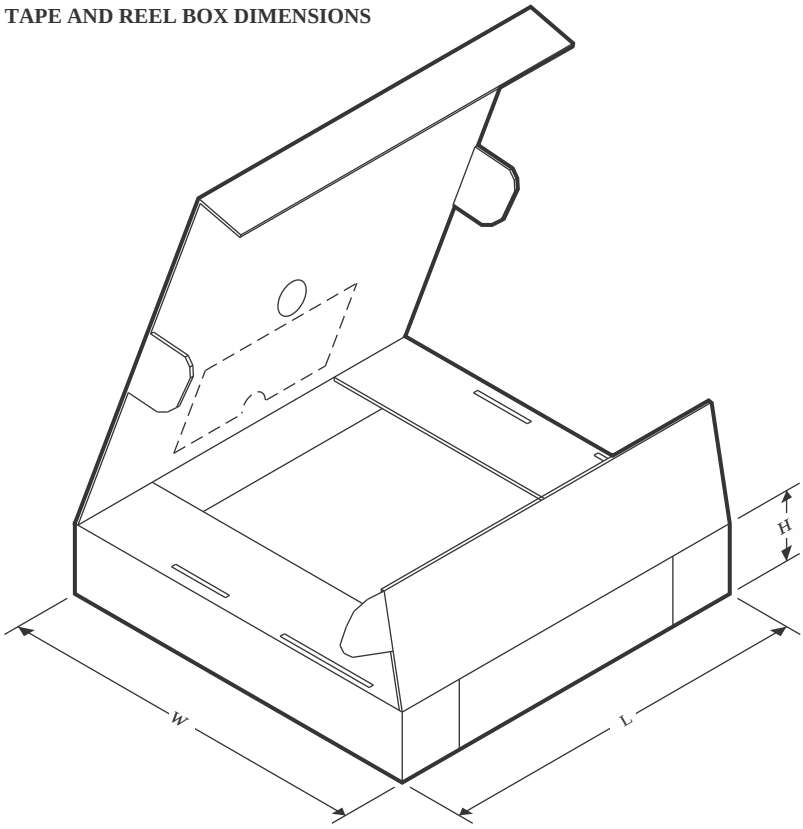
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5143RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5143RHAR	VQFN	RHA	40	2500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

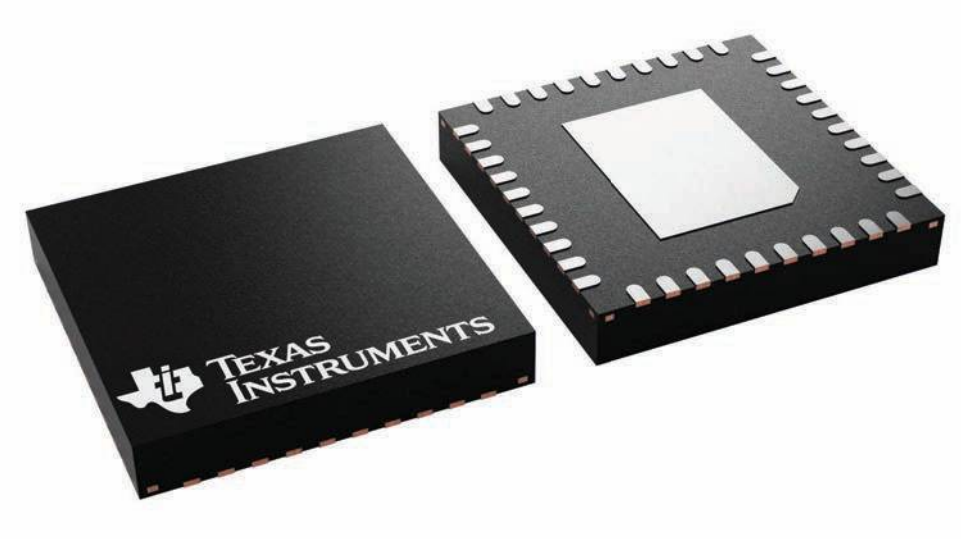
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



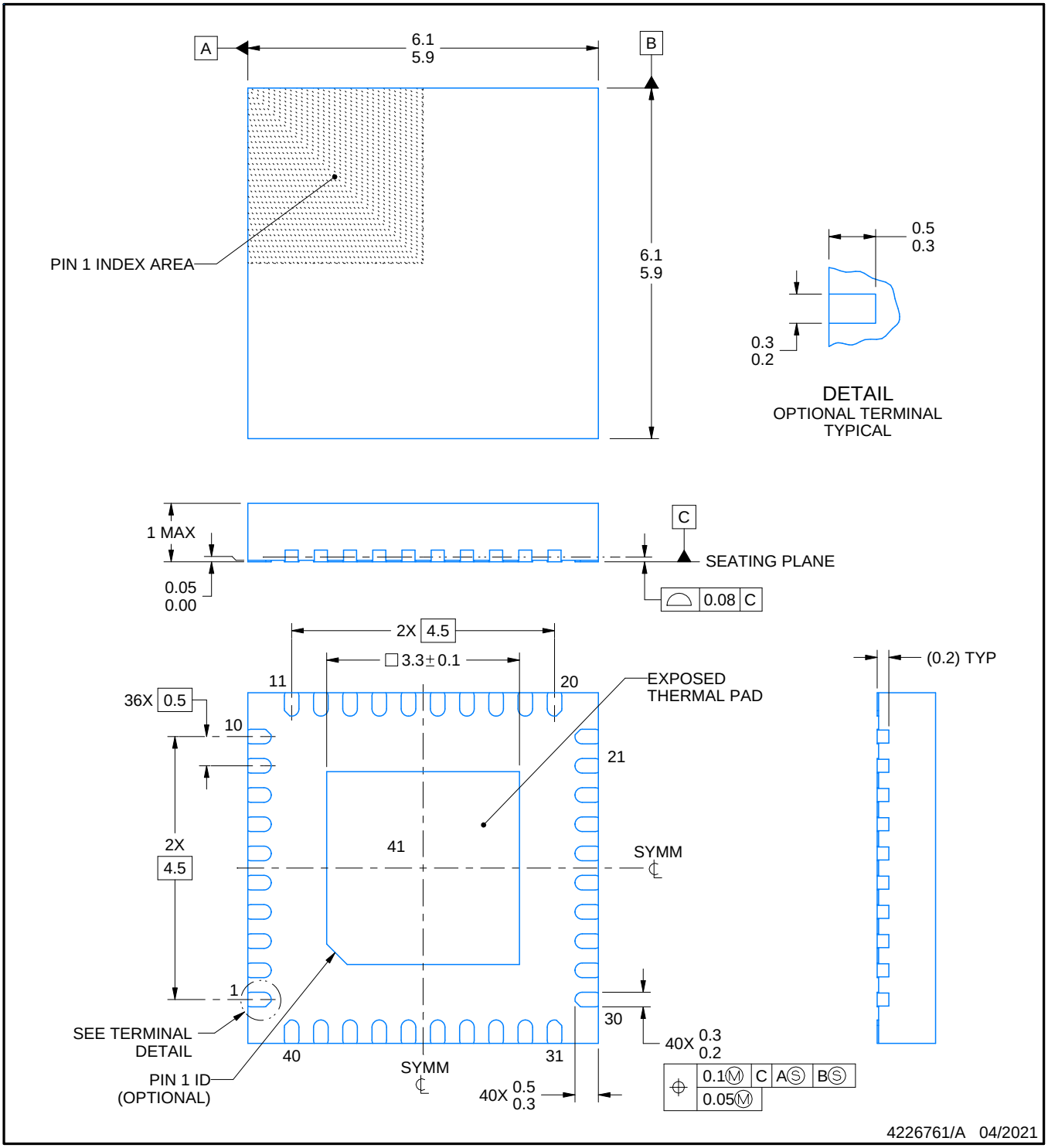
4225870/A

PACKAGE OUTLINE

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

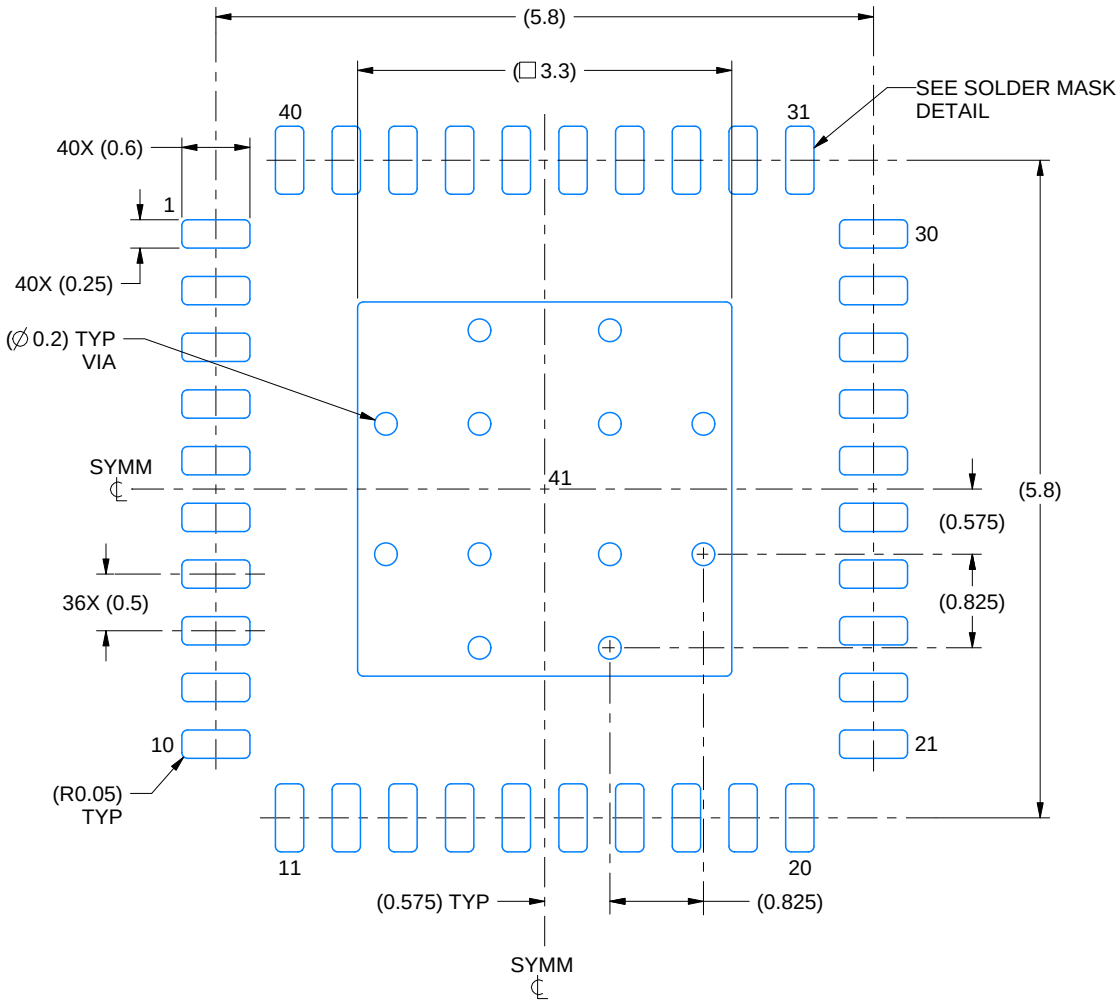
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0040P

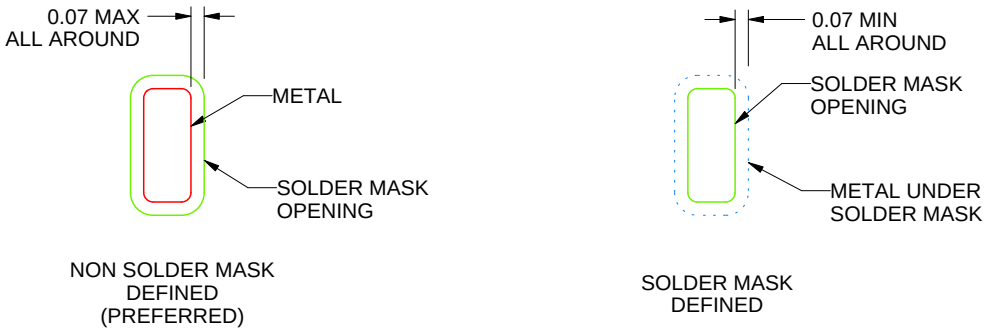
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

SCALE:15X

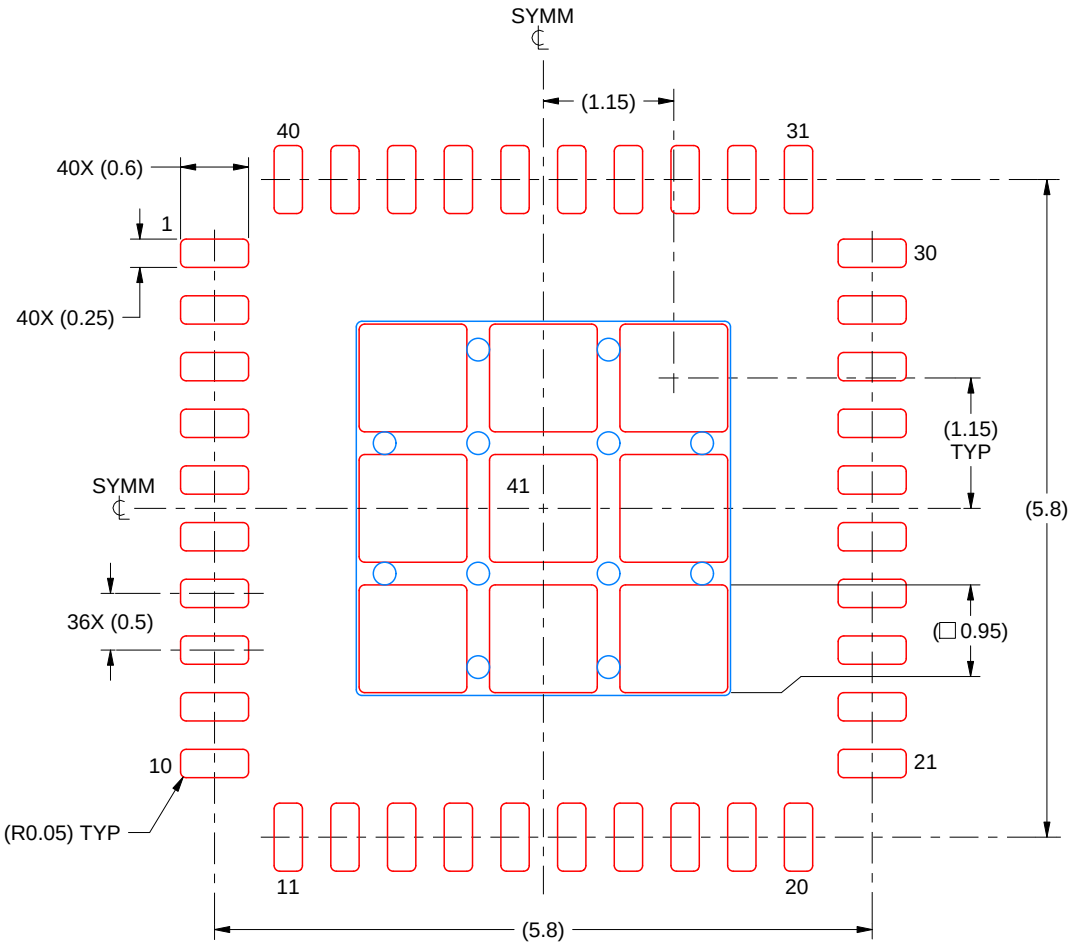


SOLDER MASK DETAILS

4226761/A 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
78.25% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4226761/A 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
LM25143
SNVSC10 – MARCH 2022

LM25143 3.5-V to 42-V Dual Synchronous Buck DC/DC Controller With Ultra-Low I_Q

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Versatile synchronous buck DC/DC controller
  - Wide input voltage range of 3.5 V to 42 V
  - 1% accurate, fixed 3.3-V, 5-V, or adjustable outputs from 0.6 V to 36 V
  - 150°C maximum junction temperature
  - 4-µA typical shutdown mode current
  - 15-µA typical no-load standby current
- Two interleaved synchronous buck channels
  - Dual channel or single-output multiphase
  - 65-ns $t_{ON(min)}$ for high V_{IN}/V_{OUT} ratio
  - 60-ns $t_{OFF(min)}$ for low dropout
- Inherent protection features for robust design
  - Shunt or inductor DCR current sensing
  - Hiccup mode overcurrent protection
  - Independent ENABLE and PGOOD functions
  - Adjustable output voltage soft start
  - VCC, VDDA, and gate-drive UVLO protection
  - Thermal shutdown protection with hysteresis
- Optimized for CISPR 11 and CISPR 32 class B conducted and radiated EMI requirements
  - Slew-rate controlled adaptive gate drivers
  - Spread spectrum reduces peak emissions
- 100-kHz to 2.2-MHz switching frequency
  - SYNC in and SYNC out capability
  - Selectable diode emulation or FPWM modes
- 6-mm × 6-mm VQFN-40 package
- Create a custom design using the LM25143 with WEBENCH® Power Designer

2 Applications

- Personal electronics: computer peripherals
- Industrial: 24-V bus systems, factory automation and control, robotics, power delivery
- Enterprise systems: high-performance computing

3 Description

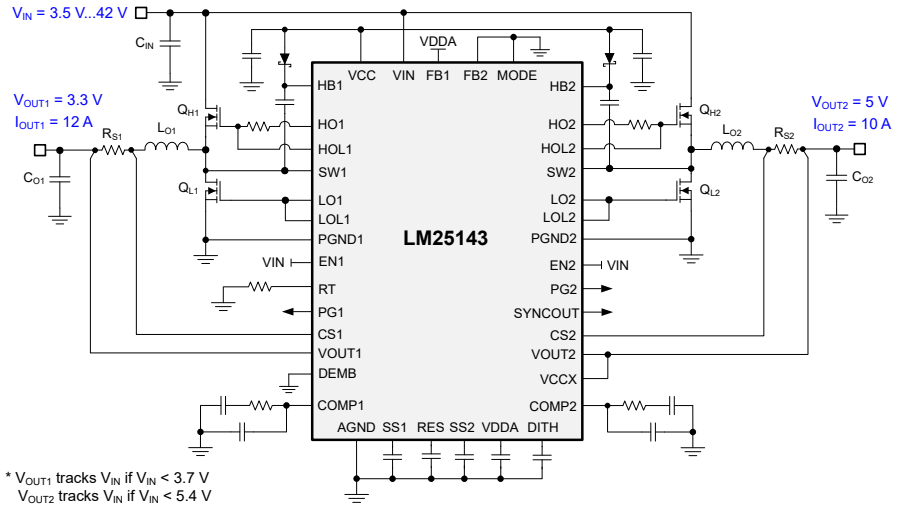
The LM25143 is a 42-V DC/DC synchronous buck controller for high-current single or dual outputs. Deriving from a family of wide-V_{IN} range controllers, the device uses an interleaved, stackable, peak current-mode control architecture for easy loop compensation, fast transient response, excellent load and line regulation, and accurate current sharing with paralleled phases for higher output current. A high-side switch minimum on time of 65 ns provides large step-down ratios, enabling the direct conversion from 12-V or 24-V inputs to low-voltage rails for reduced system complexity and cost. The LM25143 continues to operate during input voltage dips as low as 3.5 V, at nearly 100% duty cycle if needed.

The 15-µA no-load quiescent current with the output voltage in regulation extends operating run-time in battery-powered systems. Power the LM25143 from the output of the switching regulator or another available source for even lower input quiescent current and power loss.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM25143	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



High-Efficiency Dual Step-Down Regulator

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial release

5 Description (continued)

Several features are included to simplify compliance with CISPR 11 and CISPR 32 EMI requirements. Adaptively timed, high-current MOSFET gate drivers with adjustable slew rate control minimize body diode conduction during switching transitions, reducing switching losses and improving thermal and EMI performance at high input voltage and high switching frequency. To reduce input capacitor ripple current and EMI filter size, 180° interleaved operation is provided for two outputs. A 90° out-of-phase clock output works well for cascaded, multi-channel, or multiphase power stages. Resistor-adjustable switching frequency as high as 2.2 MHz can be synchronized to an external clock source up to 2.5 MHz to eliminate beat frequencies in noise-sensitive applications. Optional triangular spread spectrum modulation further improves the EMI signature.

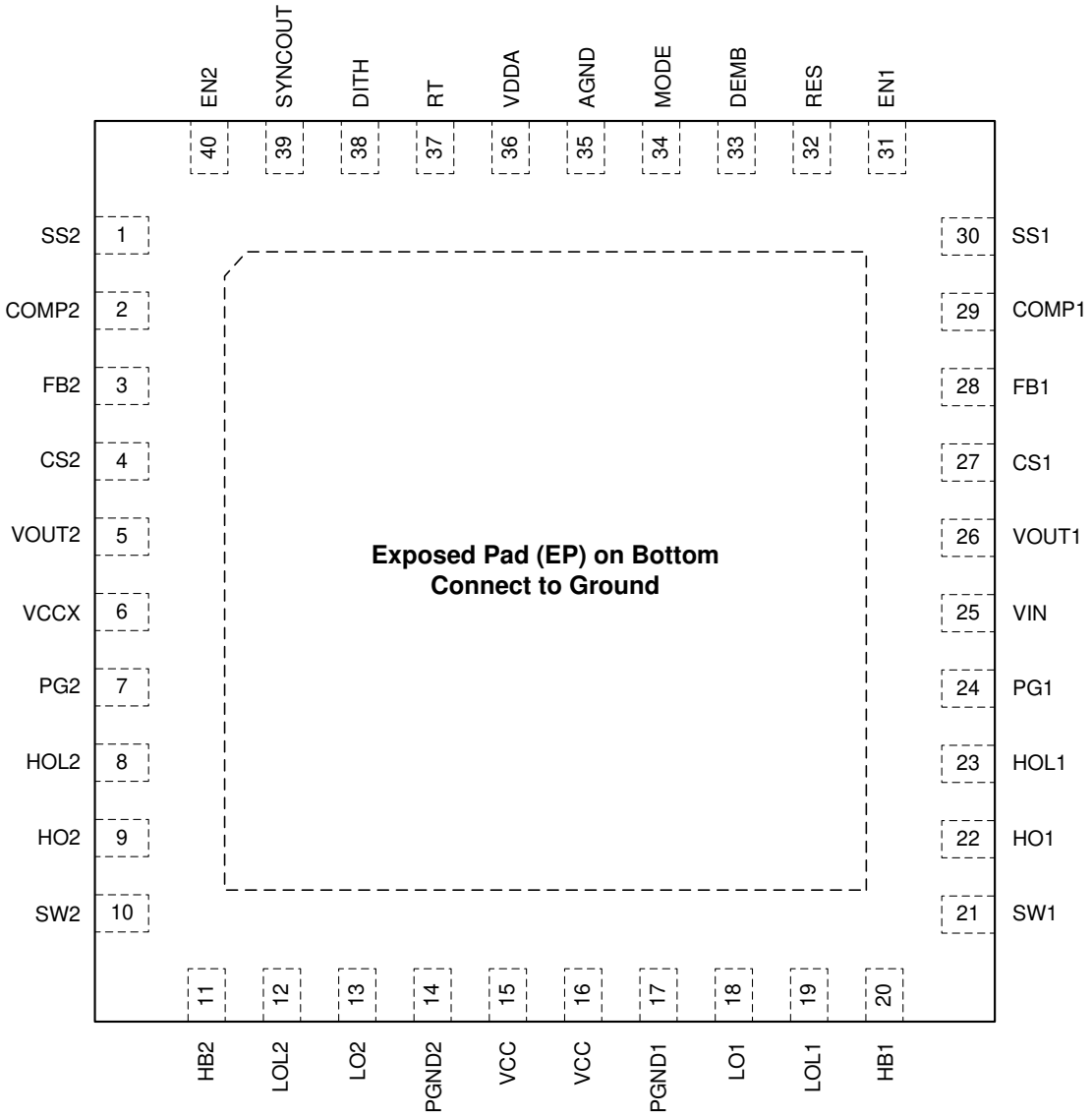
Additional features of the LM25143 include 150°C maximum junction temperature operation, user-selectable diode emulation for lower current consumption at light-load conditions, configurable soft-start functions, open-drain power-good flags for fault reporting and output monitoring, independent enable inputs, monotonic start-up into prebiased loads, an integrated VCC bias supply regulator with automatic changeover to an external bias connected at VCCX, programmable hiccup-mode overload protection, and thermal shutdown protection with automatic recovery. Current is sensed using the inductor DCR for highest efficiency or an optional shunt resistor for high accuracy.

The LM25143 controller comes in a 6-mm × 6-mm thermally enhanced, 40-pin VQFN package. The wide input voltage range, low quiescent current consumption, high-temperature operation, cycle-by-cycle current limit, low EMI signature, and small solution size provide an ideal point-of-load regulator solution for applications requiring enhanced reliability and durability.

6 Device Comparison Table

Device	Orderable Part Number	Package Drawing	Package Type	Wettable Flanks	Maximum V_{IN}
LM25143	LM25143RHAR	RHA	VQFN	No	42 V
LM5143	LM5143RHAR	RHA	VQFN	No	65 V

7 Pin Configuration and Functions



Connect the exposed pad on the bottom to AGND and PGND on the PCB.

Figure 7-1. 40-Pin VQFN RHA Package (Top View)

Table 7-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SS2	1	I	Channel 2 soft-start programming pin. An external ceramic capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling SS2 below 150 mV turns off the channel 2 gate driver outputs, but all the other functions remain active.
COMP2	2	O	Output of the channel 2 transconductance error amplifier. COMP2 is high impedance in single-output interleaved or single-output multiphase operation.
FB2	3	I	Feedback input of channel 2. Connect FB2 to VDDA for a 3.3-V output or connect FB2 to AGND for a fixed 5-V output. A resistive divider from VOUT2 to FB2 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB2 is 0.6 V.
CS2	4	I	Channel 2 current sense amplifier input. Connect CS2 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
VOUT2	5	I	Output voltage sense and the current sense amplifier input of channel 2. Connect VOUT2 to the output side of the channel 2 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
VCCX	6	P	Optional input for an external bias supply. If V_{VCCX} > 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Connect a ceramic capacitor between VCCX and PGND.
PG2	7	O	An open-collector output that goes low if VOUT2 is outside a specified regulation window
HOL2	8	O	Channel 2 high-side gate driver turn-off output
HO2	9	O	Channel 2 high-side gate driver turn-on output
SW2	10	P	Switching node of the channel 2 buck regulator. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
HB2	11	P	Channel 2 high-side driver supply for the bootstrap gate drive
LOL2	12	O	Channel 2 low-side gate driver turn-off output
LO2	13	O	Channel 2 low-side gate driver turn-on output
PGND2	14	G	Power-ground connection pin for the low-side NMOS gate driver
VCC	15, 16	P	VCC bias supply pin. Pins 15 and 16 must to be connected together on the PCB. Connect ceramic capacitors between VCC and PGND1 and between VCC and PGND2.
PGND1	17	G	Power-ground connection pin for the low-side NMOS gate driver
LO1	18	O	Channel 1 low-side gate driver turn-on output
LOL1	19	O	Channel 1 low-side gate driver turn-off output
HB1	20	P	Channel 1 high-side driver supply for the bootstrap gate drive
SW1	21	P	Switching node of the channel 1 buck regulator. Connect to the channel 1 bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
HO1	22	O	Channel 1 high-side gate driver turn-on output
HOL1	23	O	Channel 1 high-side gate driver turn-off output
PG1	24	O	An open-collector output that goes low if VOUT1 is outside a specified regulation window
VIN	25	P	Supply voltage input source for the VCC regulators
VOUT1	26	I	Output voltage sense and the current sense amplifier input of channel 1. Connect VOUT1 to the output side of the channel 1 current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used).
CS1	27	I	Channel 1 current sense amplifier input. Connect CS1 to the inductor side of the external current sense resistor (or to the relevant sense capacitor terminal if inductor DCR current sensing is used) using a low-current Kelvin connection.
FB1	28	I	Feedback input of channel 1. Connect the FB1 pin to VDDA for a 3.3-V output or connect FB1 to AGND for a 5-V output. A resistive divider from VOUT1 to FB1 sets the output voltage level between 0.6 V and 55 V. The regulation threshold at FB1 is 0.6 V.
COMP1	29	O	Output of the channel 1 transconductance error amplifier (EA)
SS1	30	I	Channel 1 soft-start programming pin. An external capacitor and an internal 20-µA current source set the ramp rate of the internal error amplifier reference during soft start. Pulling the SS1 voltage below 150 mV turns off the channel 1 gate driver outputs, but all the other functions remain active.

Table 7-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN1	31	I	An active high input (V_{EN1} > 2 V) enables output 1. If outputs 1 and 2 are disabled, the LM25143 is in shutdown mode unless a SYNC signal is present at DEMB. EN1 must never be floating.
RES	32	O	Restart timer pin. An external capacitor configures the hiccup-mode current limiting. A capacitor at the RES pin determines the time the controller remains off before automatically restarting in hiccup mode. The two regulator channels operate independently. One channel can operate in normal mode while the other is in hiccup-mode overload protection. Hiccup mode commences when either channel experiences 512 consecutive PWM cycles with cycle-by-cycle current limiting. Connect RES to VDDA during power up to disable hiccup-mode protection.
DEMB	33	I	Diode emulation pin. Connect DEMB to AGND to enable diode emulation mode. Connect DEMB to VDDA to operate the LM25143 in forced PWM (FPWM) mode with continuous conduction at light loads. DEMB can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
MODE	34	I	Connect MODE to AGND or VDDA for dual-output or interleaved single-output operation, respectively. This also configures the LM25143 with an EA transconductance of 1200 µS. Connecting a 10-kΩ resistor between MODE and AGND sets the LM25143 for dual-output operation with an ultra-low I_Q mode and an EA transconductance of 60 µS.
AGND	35	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits
VDDA	36	O	Internal analog bias regulator output. Connect a ceramic decoupling capacitor from VDDA to AGND.
RT	37	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100 kHz and 2.2 MHz.
DITH	38	I	A capacitor connected between the DITH pin and AGND is charged and discharged with a 20-µA current source. If dithering is enabled, the voltage on the DITH pin ramps up and down modulating the oscillator frequency between –5% and +5% of the internal oscillator. Connecting DITH to VDDA during power up disables the dither feature. DITH is ignored if an external synchronization clock is used.
SYNCOUT	39	O	SYNCOUT is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM25143 controller, all phases are 90° out of phase.
EN2	40	I	An active high input (V_{EN2} > 2 V) enables output 2. If outputs 1 and 2 are disabled, the LM25143 is in shutdown mode unless a SYNC signal is present on DEMB. EN2 must never be floating.

(1) P = Power, G = Ground, I = Input, O = Output

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	47	V
	SW1, SW2 to PGND	–0.3	47	
	SW1, SW2 to PGND (20-ns transient)	–5		
	HB1 to SW1, HB2 to SW1	–0.3	6.5	
	HB1 to SW1, HB2 to SW1 (20-ns transient)	–5		
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3	V_{HB} + 0.3	
	HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2 (20-ns transient)	–5		
	LO1, LOL1, LO2, LOL2 to PGND	–0.3	V_{VCC} + 0.3	
	LO1, LOL1, LO2, LOL2 to PGND (20-ns transient)	–1.5	V_{VCC} + 0.3	
	SS1, SS2, COMP1, COMP2, RES, RT, DITH, MODE to AGND	–0.3	V_{VDDA} + 0.3	
	EN1, EN2 to PGND	–0.3	47	
	VCC, VCCX, VDDA, PG1, PG2, DEMB, FB1, FB2 to AGND	–0.3	6.5	
	VOUT1, VOUT2, CS1, CS2	–0.3	47	
	VOUT1 to CS1, VOUT2 to CS2	–0.3	0.3	
PGND to AGND		–0.3	0.3	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent damage to the device. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operation Condition. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JESD22 JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN to PGND	–0.3		42	V
		SW1, SW2 to PGND	–0.3		42	
		HB1 to SW1, HB2 to SW1	–0.3	5	5.25	
		HO1 to SW1, HOL1 to SW1, HO2 to SW2, HOL2 to SW2	–0.3		V_{HB} + 0.3	
		LO1, LOL1, LO2, LOL2 to PGND	–0.3	5	5.25	
		FB1, FB2, SS1, SS2, COMP1, COMP2, RES, DEMB, RT, MODE, DITH to AGND	–0.3		5.25	
		EN1, EN2 to PGND	–0.3		42	
		VCC, VDDA to PGND	–0.3	5	5.25	
		VOUT1, VOUT2, CS1, CS2 to PGND	–0.3		37	
	PGND to AGND		–0.3		0.3	
T_J	Operating junction temperature		–40		150	°C

8.4 Thermal Information

THERMAL METRIC[1]		RHA (VQFNP)	UNIT
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{SHUTDOWN}$	Shutdown mode current	V_{EN1} = V_{EN2} = 0 V		3.5	7	µA
$I_{STANDBY1}$	Standby current, channel 1	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no load, not switching, DEMB = MODE = GND		24		µA
$I_{STANDBY2}$	Standby current, channel 2	V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no load, not switching, DEMB = MODE = GND		25		µA
$I_{STANDBY3}$	Standby current, channel 1, ultra-low I_Q mode	V_{EN1} = 5 V, V_{EN2} = 0 V, V_{VOUT1} = 3.3 V, in regulation, no load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to GND		16.5		µA
$I_{STANDBY4}$	Standby current, channel 2, ultra-low I_Q mode	V_{EN1} = 0 V, V_{EN2} = 5 V, V_{VOUT2} = 5 V, in regulation, no load, not switching, DEMB = GND, R_{MODE} = 10 kΩ to GND		21		µA
BIAS REGULATOR (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 100 mA, V_{VCCX} = 0 V	4.7	5	5.3	V
$V_{CC-UVLO}$	VCC UVLO rising threshold	V_{VCC} rising	3.2	3.3	3.4	V
$V_{VCC-HYST}$	VCC UVLO hysteresis			182		mV
$I_{VCC-LIM}$	VCC sourcing current limit			235		mA
ANALOG BIAS (VDDA)						
$V_{VDDA-REG}$	VDDA regulation voltage		4.75	5	5.25	V
$V_{VDDA-UVLO}$	VDDA UVLO rising threshold	V_{VCC} rising, V_{VCCX} = 0 V	3.1	3.2	3.3	V
$V_{VDDA-HYST}$	VDDA UVLO hysteresis	V_{VCCX} = 0 V		90		mV
R_{VDDA}	VDDA resistance	V_{VCCX} = 0 V		20		Ω
EXTERNAL BIAS (VCCX)						
$V_{VCCX-ON}$	$VCCX_{(ON)}$ rising threshold		4.1	4.3	4.4	V
R_{VCCX}	VCCX resistance	V_{VCCX} = 5 V		1.2		Ω
$V_{VCCX-HYST}$	VCCX hysteresis voltage			130		mV
CURRENT LIMIT (CS1, CS2)						
V_{CS1}	Current limit threshold 1	Measured from CS1 to VOUT1	66	73	82	mV
V_{CS2}	Current limit threshold 2	Measured from CS2 to VOUT2	66	73	82	mV
$t_{CS-DELAY}$	CS delay to output			40		ns
G_{CS}	CS amplifier gain		11.25	12	12.6	V/V
$I_{CS-BIAS}$	CS amplifier input bias current				15	nA
POWER GOOD (PG1, PG2)						
$PG1_{UV}$	PG1 UV trip level	Falling with respect to the regulation voltage	89.5%	92%	94%	
$PG2_{UV}$	PG2 UV trip level	Falling with respect to the regulation voltage	89.5%	92%	94%	
$PG2_{OV}$	PG2 OV trip level	Rising with respect to the regulation voltage	107.5%	110%	112.5%	
$PG2_{OV}$	PG2 OV trip level	Rising with respect to the regulation voltage	107.5%	110%	112.5%	
$PG1_{UV-HYST}$	PG1 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG1_{OV-HYST}$	PG1 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{UV-HYST}$	PG2 UV hysteresis	Rising with respect to the regulation voltage		3.4%		
$PG2_{OV-HYST}$	PG2 OV hysteresis	Rising with respect to the regulation voltage		3.4%		
V_{OL-PG1}	PG1 voltage	Open collector, I_{PG1} = 2 mA			0.4	V
V_{OL-PG2}	PG2 voltage	Open collector, I_{PG2} = 2 mA			0.4	V

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PG-RISE-DLY}$	OV filter time	V_{OUT} rising		25		µs
$t_{PG-FALL-DLY}$	UV filter time	V_{OUT} falling		22		µs
HIGH-SIDE GATE DRIVER (HO1, HO2, HOL1, HOL2)						
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100 mA		0.04		V
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100 mA, $V_{HO-HIGH}$ = V_{HB} – V_{HO}		0.09		V
$t_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		24		ns
$t_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		24		ns
I_{HO-SRC}	HO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{HO-SINK}$	HO peak sink current	V_{VCCX} = 5 V		4.25		A
V_{BT-UV}	BOOT UVLO	V_{VCC} falling		2.45		V
$V_{BT-UV-HYS}$	BOOT UVLO hysteresis			113		mV
I_{BOOT}	BOOT quiescent current			1.25		µA
LOW-SIDE GATE DRIVER (LO1, LO2, LOL1, LOL2)						
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100 mA		0.04		V
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100 mA		0.07		V
$t_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7 nF		4		ns
$t_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7 nF		3		ns
$I_{LO-SOURCE}$	LO peak source current	V_{HO} = V_{SW} = 0 V, V_{HB} = 5 V, V_{VCCX} = 5 V		3.25		A
$I_{LO-SINK}$	LO peak sink current	V_{VCCX} = 5 V		4.25		A
RESTART (RES)						
$I_{RES-SRC}$	RES current source			20		µA
V_{RES-TH}	RES threshold			1.2		V
HIC_{CYCLES}	HICCUP mode fault			512		cycles
R_{RES-PD}	RES pulldown resistance			5.7		Ω
OUTPUT VOLTAGE SETPOINT (VOUT1, VOUT2)						
$VOUT_{33}$	3.3-V output voltage setpoint	FB = VDDA, V_{IN} = 3.5 V to 65 V	3.267	3.3	3.335	V
$VOUT_{50}$	5-V output voltage setpoint	FB = AGND, V_{IN} = 5.5 V to 65 V	4.95	5	5.05	V
FEEDBACK (FB1, FB2)						
$V_{FB-3V3-SEL}$	VOUT select threshold 3.3-V output		4.6			V
R_{FB-5V}	Resistance FB to AGND for 5-V output	V_{MODE} = 0 V or R_{MODE} = 10 kΩ			500	Ω
$R_{FB-EXTRES}$	Thevenin equivelent resistance	V_{MODE} = 0 V or R_{MODE} = 10 kΩ, V_{FB} < 2 V	5			kΩ
$V_{FB2-LOW}$	Primary mode select logic level low	MODE = VDDA			0.8	V
$V_{FB2-HIGH}$	Primary mode select logic level high	MODE = VDDA	2			V
$V_{FB1-LOW}$	Diode emulation logic level low in secondary mode	MODE = FB2 = VDDA			0.8	V
$V_{FB1-HIGH}$	FPWM logic level high in secondary mode	MODE = FB2 = VDDA	2			V
V_{FB-REG}	Regulated feedback voltage	T_J = –40°C to 125°C	0.594	0.6	0.606	V
ERROR AMPLIFIER (COMP1, COMP2)						
g_{m1}	EA transconductance	FB to COMP, R_{MODE} < 5 kΩ to AGND	1020	1200		µs
g_{m2}	EA transconductance, ultra-low I_Q mode	MODE = GND, R_{MODE} = 10 kΩ		65		µs
I_{FB}	Error amplifier input bias current				30	nA
$V_{COMP-CLMP}$	COMP clamp voltage	V_{FB} = 0 V		3.3		V

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{COMP-SECOND}$	COMP leakage, secondary mode	V_{COMP} = 1 V, MODE = FB2 = VDDA			10	nA
$I_{COMP-INTLV}$	COMP2 leakage, interleaved mode	V_{COMP} = 1 V, MODE = VDDA, V_{FB2} = 0 V			10	nA
$I_{COMP-SRC1}$	EA source current	V_{COMP} = 1 V, V_{FB} = 0.4 V, V_{MODE} = 0 V		190		µA
$I_{COMP-SINK1}$	EA sink current	V_{COMP} = 1 V, V_{FB} = 0.8 V, V_{MODE} = 0 V		160		µA
$I_{COMP-SRC2}$	EA source current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.4 V, R_{MODE} = 10 kΩ to AGND		10		µA
$I_{COMP-SINK2}$	EA sink current, ultra-low I_Q mode	V_{COMP} = 1 V, V_{FB} = 0.8 V, R_{MODE} = 10 kΩ to AGND		12		µA
$V_{SS-OFFSET}$	EA SS offset with V_{FB} = 0 V	Raise V_{SS} until V_{COMP} > 300 mV		36		mV
ADAPTIVE DEADTIME CONTROL						
V_{GS-DET}	VGS detection threshold	VGS falling, no load		2.1		V
t_{DEAD1}	HO off to LO on dead time			22		ns
t_{DEAD2}	LO off to HO on dead time			20		ns
DIODE EMULATION (DEMB)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V
V_{DEMB_Rising}	DEMB input high threshold		2			V
V_{ZC-SW}	Zero-cross threshold	V_{DEMB} = 0 V		–7		mV
V_{ZC-SS}	Zero-cross threshold soft start	DEMB = VDDA, 50 SW cycles after first HO pulse		–6.1		mV
V_{ZC-DIS}	Zero-cross threshold disabled	DEMB = VDDA, 1000 SW cycles after first HO pulse		210		mV
ENABLE (EN1, EN2)						
V_{EN-LOW}	EN1/2 low threshold	V_{VCCX} = 0 V			0.8	V
$V_{EN-HIGH-TH}$	EN1/2 high threshold	V_{VCCX} = 0 V	2			V
$I_{EN-LEAK}$	EN1/2 leakage currernt	EN1, EN2 logic inputs only		0.05		µA
SWITCHING FREQUENCY (RT)						
V_{RT}	RT regulation voltage	10 kΩ < R_{RT} < 220 kΩ		0.8		V
MODE						
$R_{MODE-HIGH}$	Resistance to AGND for ultra-low I_Q		5			kΩ
$R_{MODE-LOW}$	Resistance to AGND for normal I_Q				0.5	kΩ
$V_{MODE-LOW}$	Non-interleaved mode input low threshold				0.8	V
$V_{MODE-HIGH}$	Interleaved mode input high threshold		2			V
SYNCHRONIZATION INPUT (SYNCIN)						
$V_{DEMB-LOW}$	DEMB input low threshold				0.8	V
$V_{DEMB-HIGH}$	DEMB input high threshold		2			V
$t_{SYNC-MIN}$	DEMB minimum pulse width	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	20		250	ns
F_{SYNCIN}	External SYNC frequency range	V_{IN} = 8 V to 18 V, % of the nominal frequency set by R_{RT}	–20%		20%	
$t_{SYNCIN-HO1}$	Delay from DEMB rising to HO1 rising edge			120		ns
$t_{SYNCIN-SECOND}$	Delay from DEMB falling edge to HO2 rising edge	Secondary mode, MODE = FB2 = VDDA		100		ns
$t_{DEMB-FILTER}$	Delay from DEMB low to diode emulation enable	V_{MODE} = 0 V or R_{MODE} = 10 kΩ	15		50	µs

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted), typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the drive outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{AWAKE-FILTER}$	Maximum SYNC period to maintain standby state	V_{EN1} = V_{EN2} = 0 V		27		µs
SYNCHRONIZATION OUTPUT (SYNCOUT)						
$V_{SYNCOUT-LO}$	SYNCOUT low-state voltage	$I_{SYNCOUT}$ = 16 mA			0.8	V
$F_{SYNCOUT}$	SYNCOUT frequency	MODE = FB2 = VDDA			0	Hz
$t_{SYNCOUT1}$	Delay from HO2 rising edge to SYNCOUT rising edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		2.5		µs
$t_{SYNCOUT2}$	Delay from HO2 rising edge to SYNCOUT falling edge	V_{DEMB} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT} = 220 kΩ		7.5		µs
DITHER (DITH)						
I_{DITH}	Dither source/sink current			21		µA
$V_{DITH-HIGH}$	Dither high-level threshold			1.25		V
$V_{DITH-LOW}$	Dither low-level threshold			1.15		V
SOFT START (SS1, SS2)						
I_{SS}	Soft-start current	V_{MODE} = 0 V	16	21	28	µA
R_{SS-PD}	Soft-start pulldown resistance	V_{MODE} = 0 V		3		Ω
V_{SS-FB}	SS to FB clamp voltage	V_{CS} – V_{VOUT} > 73 mV		130		mV
$I_{SS-SECOND}$	SS leakage, secondary mode	V_{SS} = 0.8 V, MODE = FB2 = VDDA		30		nA
$I_{SS-INTLV}$	SS2 leakage, interleaved mode	V_{SS} = 0.8 V, MODE = VDDA, V_{FB2} = 0 V		21		nA
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown			175		°C
$T_{SHD-HYS}$	Thermal shutdown hysteresis			15		°C

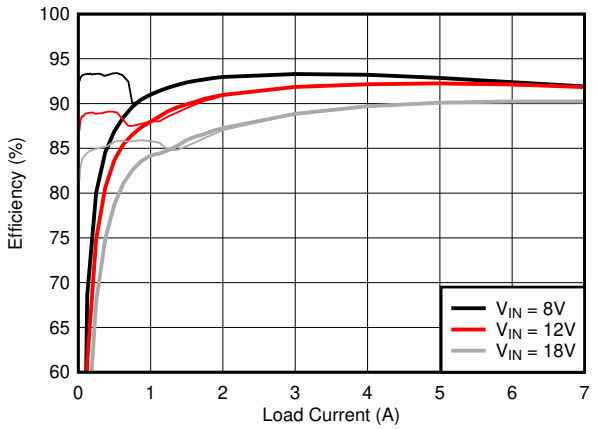
8.6 Switching Characteristics

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). Typical values correspond to T_J = 25°C, V_{VIN} = 12 V, V_{VCCX} = 5 V, V_{VOUT1} = 3.3 V, V_{VOUT2} = 5 V, V_{EN1} = V_{EN2} = 5 V, R_{RT} = 10 kΩ, F_{SW} = 2.2 MHz, no load on the gate driver outputs (HO1, HOL1, LO1, LOL1, HO2, HOL2, LO2, and LOL2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW1}	Switching frequency 1	R_{RT} = 100 kΩ	195	220	245	kHz
F_{SW2}	Switching frequency 2	R_{RT} = 10 kΩ		2.2		MHz
F_{SW3}	Switching frequency 3	R_{RT} = 220 kΩ		100		kHz
SLOPE1	Internal slope compensation 1	R_{RT} = 10 kΩ		557		mV/µs
SLOPE2	Internal slope compensation 2	R_{RT} = 100 kΩ		64		mV/µs
$t_{OFF(min)}$	Minimum off time			80	105	ns
$PH_{HO1-HO2}$	Phase between HO1 and HO2	DEMB = MODE = AGND		180		°

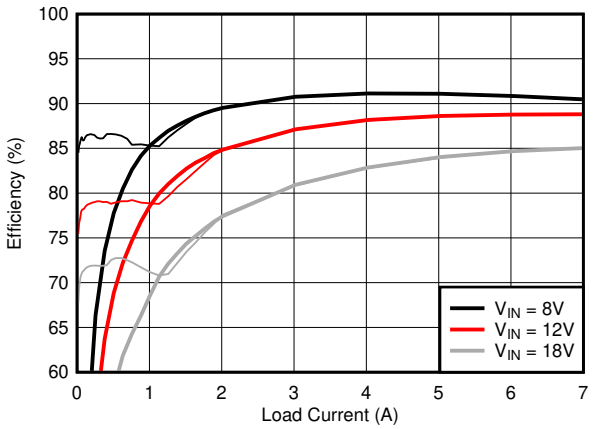
8.7 Typical Characteristics

V_{IN} = V_{EN1} = V_{EN2} = 12 V, T_J = 25°C, unless otherwise stated



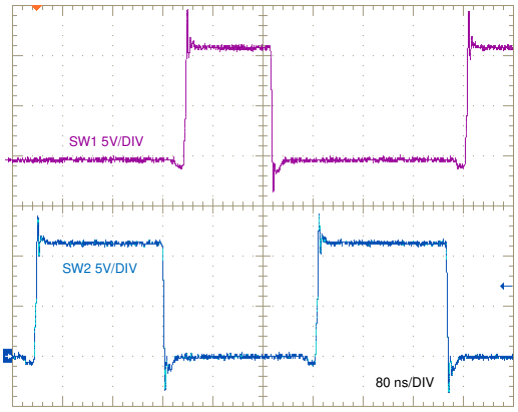
See Figure 10-4. V_{OUT} = 5 V F_{SW} = 2.1 MHz

Figure 8-1. Efficiency Versus Load



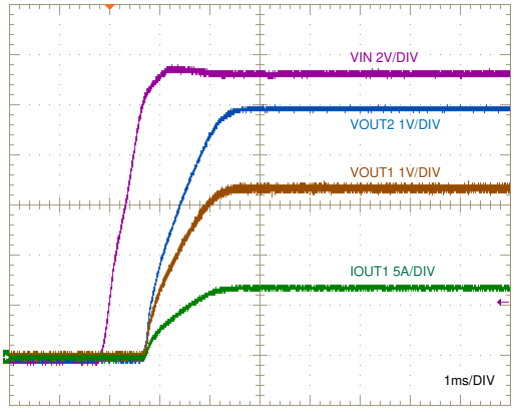
See Figure 10-4. V_{OUT} = 3.3 V F_{SW} = 2.1 MHz

Figure 8-2. Efficiency Versus Load



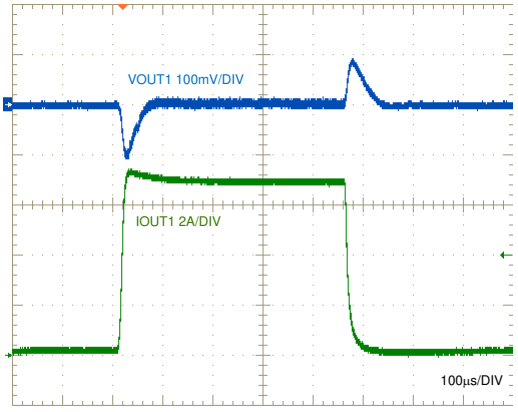
See Figure 10-4.

Figure 8-3. Switch Node Voltages



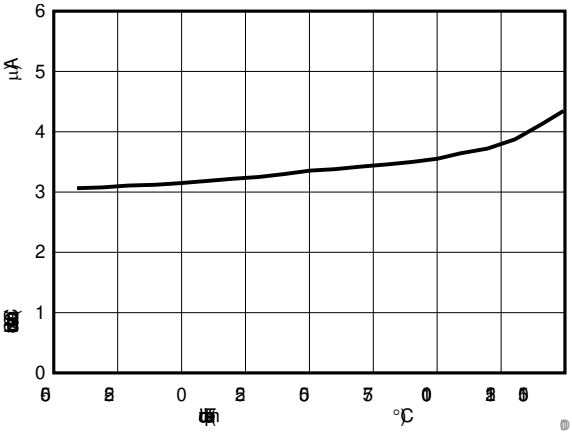
See Figure 10-4.

Figure 8-4. Start-Up Characteristic



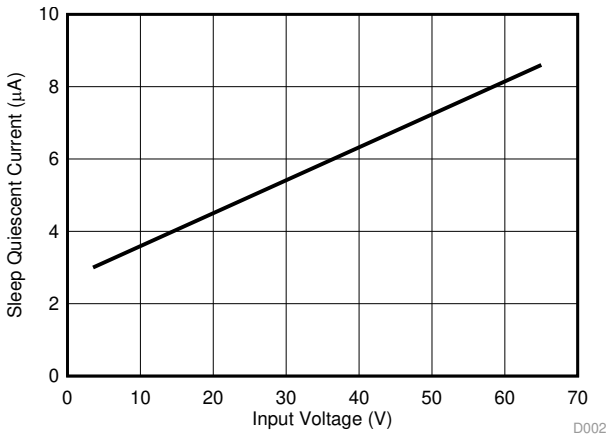
See Figure 10-4.

Figure 8-5. Load Transient Response



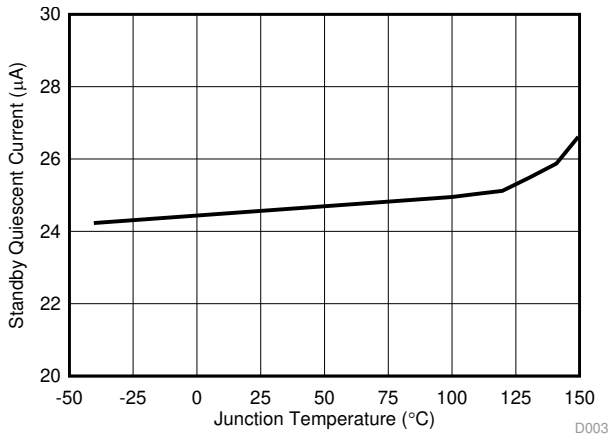
V_{EN1} = V_{EN2} = 0 V

Figure 8-6. Shutdown Current Versus Temperature



$V_{EN1} = V_{EN2} = 0$ V

Figure 8-7. Shutdown Current Versus Input Voltage



$V_{EN2} = 0$ V

Figure 8-8. Channel 1 Standby Current Versus Temperature

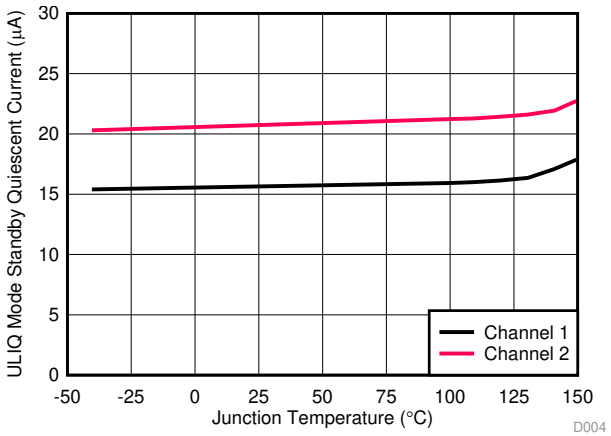


Figure 8-9. ULIQ Mode Standby Current Versus Temperature

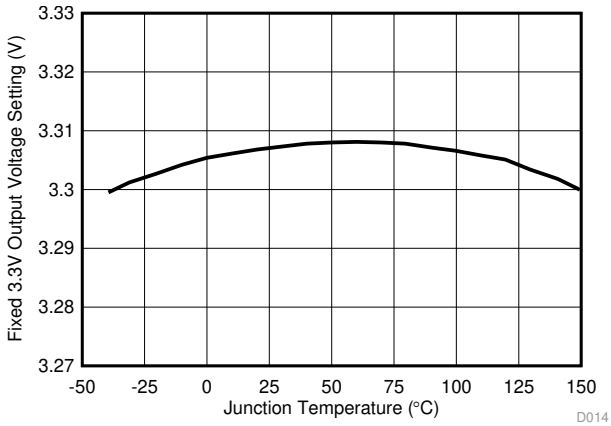


Figure 8-10. Fixed 3.3-V Output Voltage (VOUT1) Versus Temperature

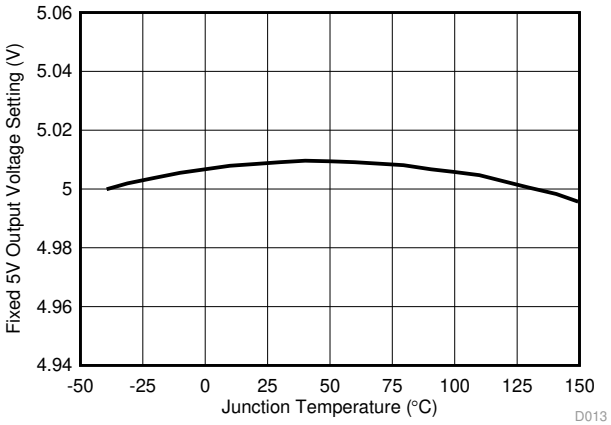


Figure 8-11. Fixed 5-V Output Voltage (VOUT1) Versus Temperature

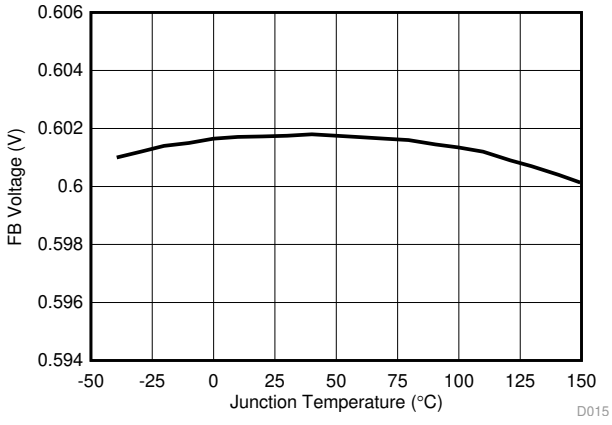


Figure 8-12. Feedback Voltage Versus Temperature

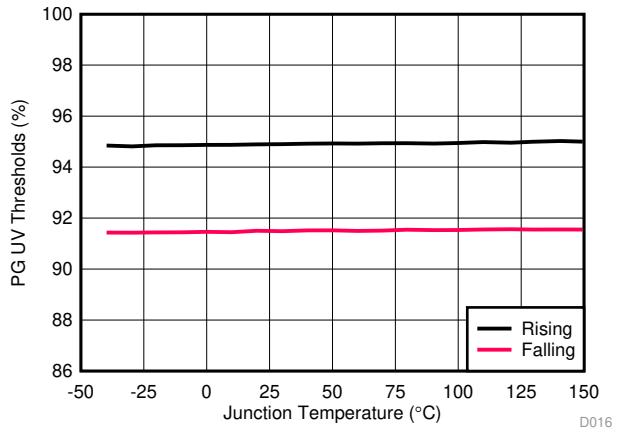


Figure 8-13. PG UV Thresholds Versus Temperature

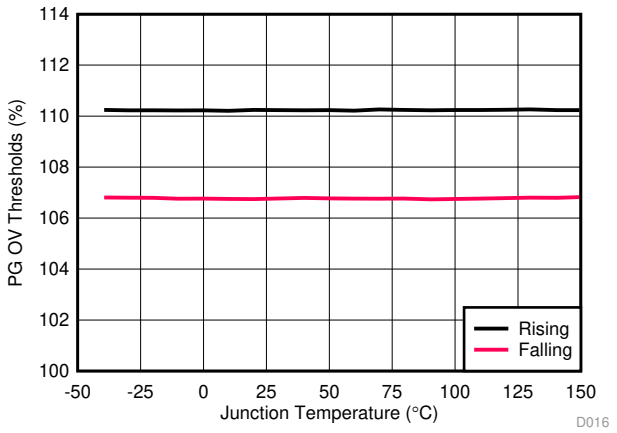


Figure 8-14. PG OV Thresholds Versus Temperature

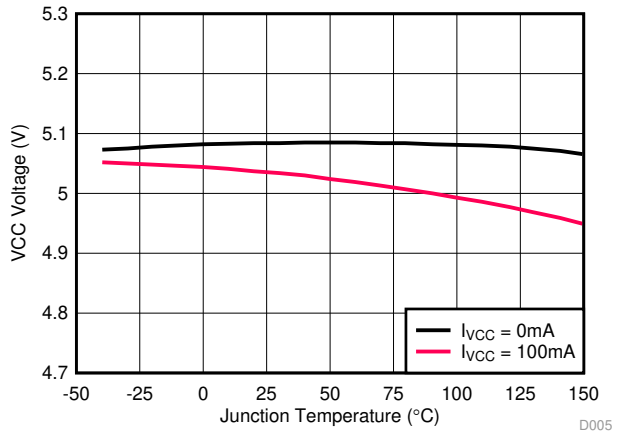


Figure 8-15. VCC Regulation Voltage Versus Temperature

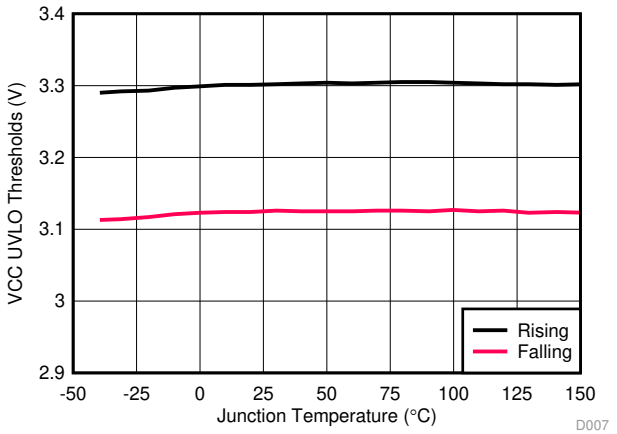


Figure 8-16. VCC UVLO Thresholds Versus Temperature

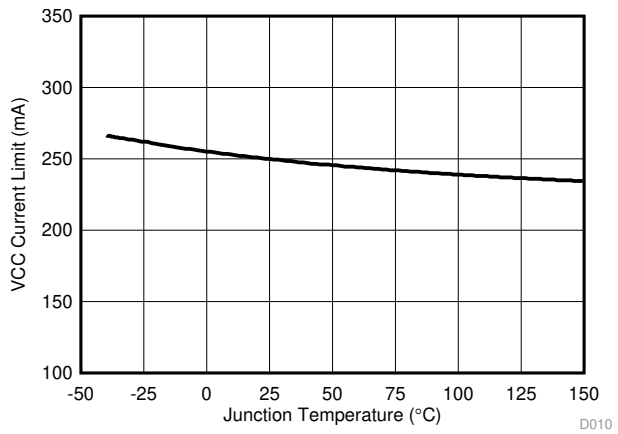


Figure 8-17. VCC Current Limit Versus Temperature

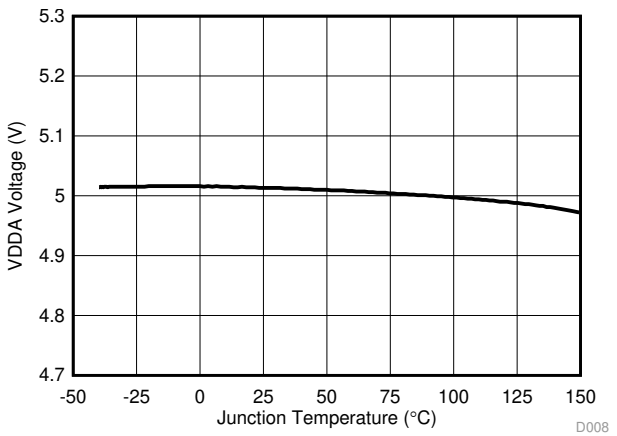


Figure 8-18. VDDA Regulation Voltage Versus Temperature

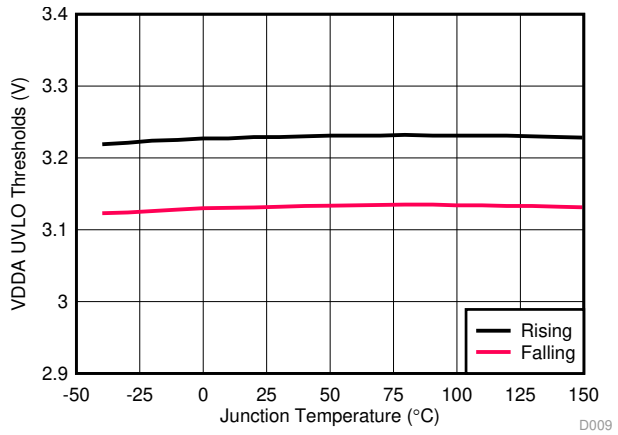


Figure 8-19. VDDA UVLO Thresholds Versus Temperature

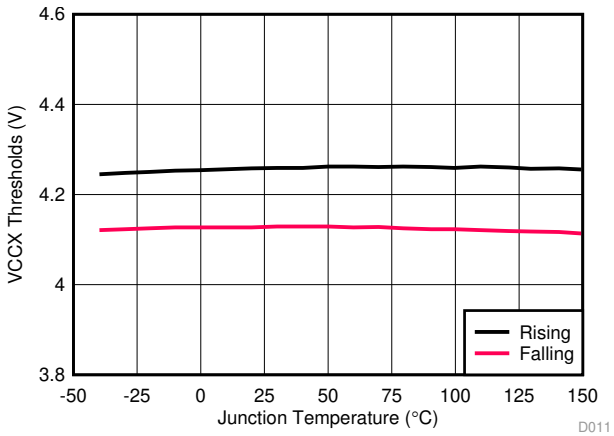


Figure 8-20. VCCX On/Off Thresholds Versus Temperature

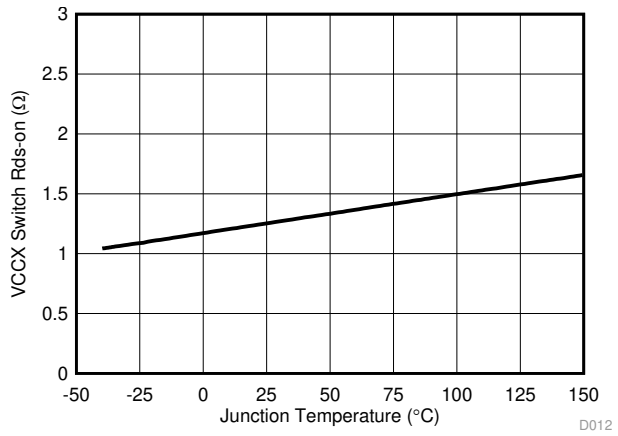


Figure 8-21. VCCX Switch Resistance Versus Temperature

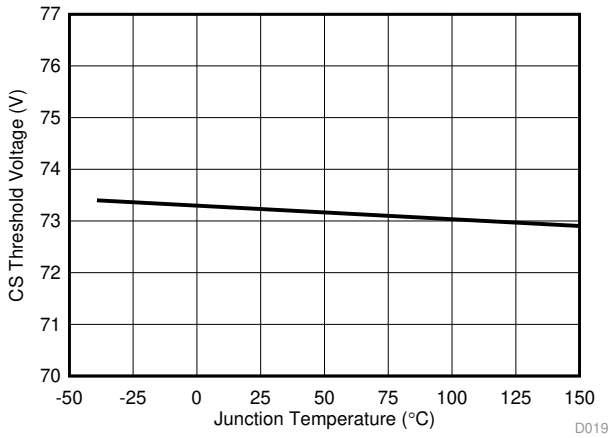


Figure 8-22. Current Sense (CS1) Threshold Versus Temperature

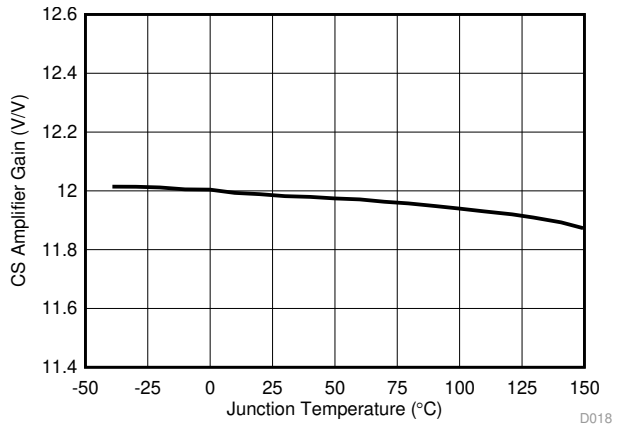


Figure 8-23. Current Sense (CS1) Amplifier Gain Versus Temperature

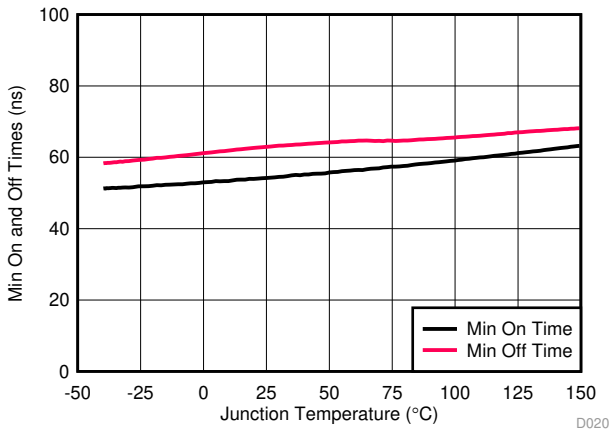


Figure 8-24. Minimum On Time and Off Time (HO1) Versus Temperature

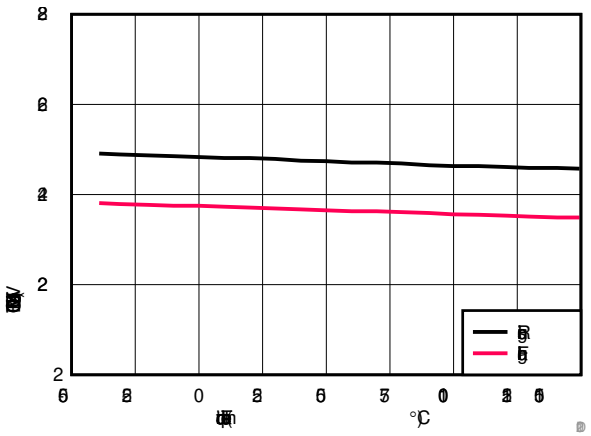


Figure 8-25. BOOT (HB1) UVLO Thresholds Versus Temperature

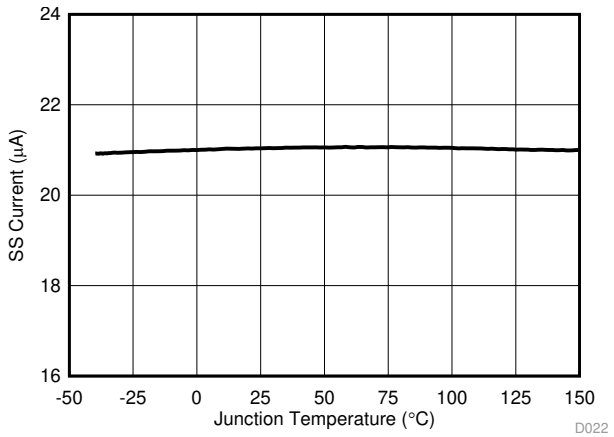


Figure 8-26. Soft-Start (SS1) Current Versus Temperature

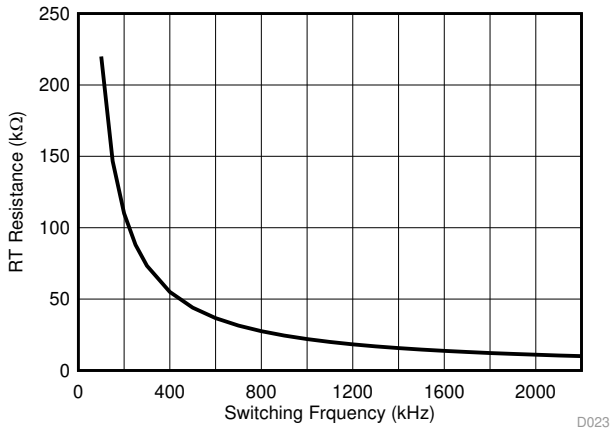


Figure 8-27. RT Resistance Versus Switching Frequency

9 Detailed Description

9.1 Overview

The LM25143 is a dual-phase or dual-channel switching controller that features all of the functions necessary to implement a high-efficiency synchronous buck power supply operating over a wide input voltage range from 3.5 V to 42 V. The LM25143 is configured to provide a fixed 3.3-V or 5-V output, or an adjustable output between 0.6 V to 36 V. This easy-to-use controller integrates high-side and low-side MOSFET drivers capable of sourcing 3.25-A and sinking 4.25-A peak current. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

Current-mode control using a shunt resistor or inductor DCR current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. It also supports a wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10-to-1) is required. The oscillator frequency is user-programmable between 100 kHz to 2.2 MHz, and the frequency can be synchronized as high as 2.5 MHz by applying an external clock to DEMB.

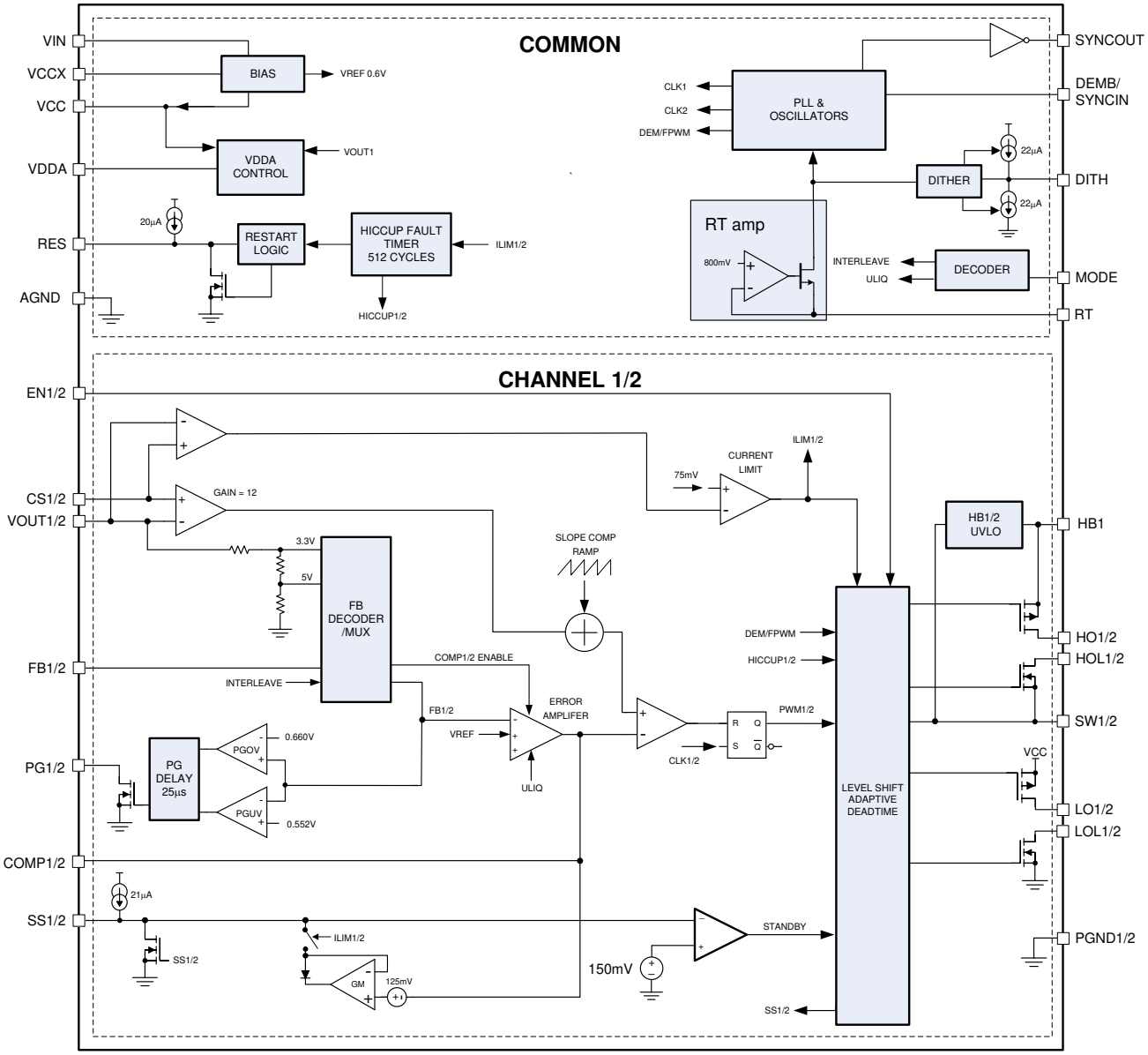
An external bias supply can be connected to VCCX to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include the following:

- Current limiting
- Thermal shutdown
- UVLO
- Remote shutdown capability

The LM25143 incorporates features to simplify the compliance with CISPR 11 and CISPR 32 EMI requirements. An optional spread spectrum frequency modulation (SSFM) technique reduces the peak EMI signature, while the adaptive gate drivers with slew rate control minimize high-frequency emissions. Finally, 180° out-of-phase interleaved operation of the two controller channels reduces input filtering and capacitor requirements.

The LM25143 is provided in a 40-pin VQFN package with an exposed pad to aid in thermal dissipation.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage Range (V_{IN})

The LM25143 operational input voltage range is from 3.5 V to 42 V. The device is intended for step-down conversions from 12-V and 24-V supply rails. The application circuit in Figure 9-1 shows all the necessary components to implement an LM25143-based wide-V_{IN} dual-output step-down regulator using a single supply. The LM25143 uses an internal LDO subregulator to provide a 5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 5 V plus the necessary subregulator dropout specification).

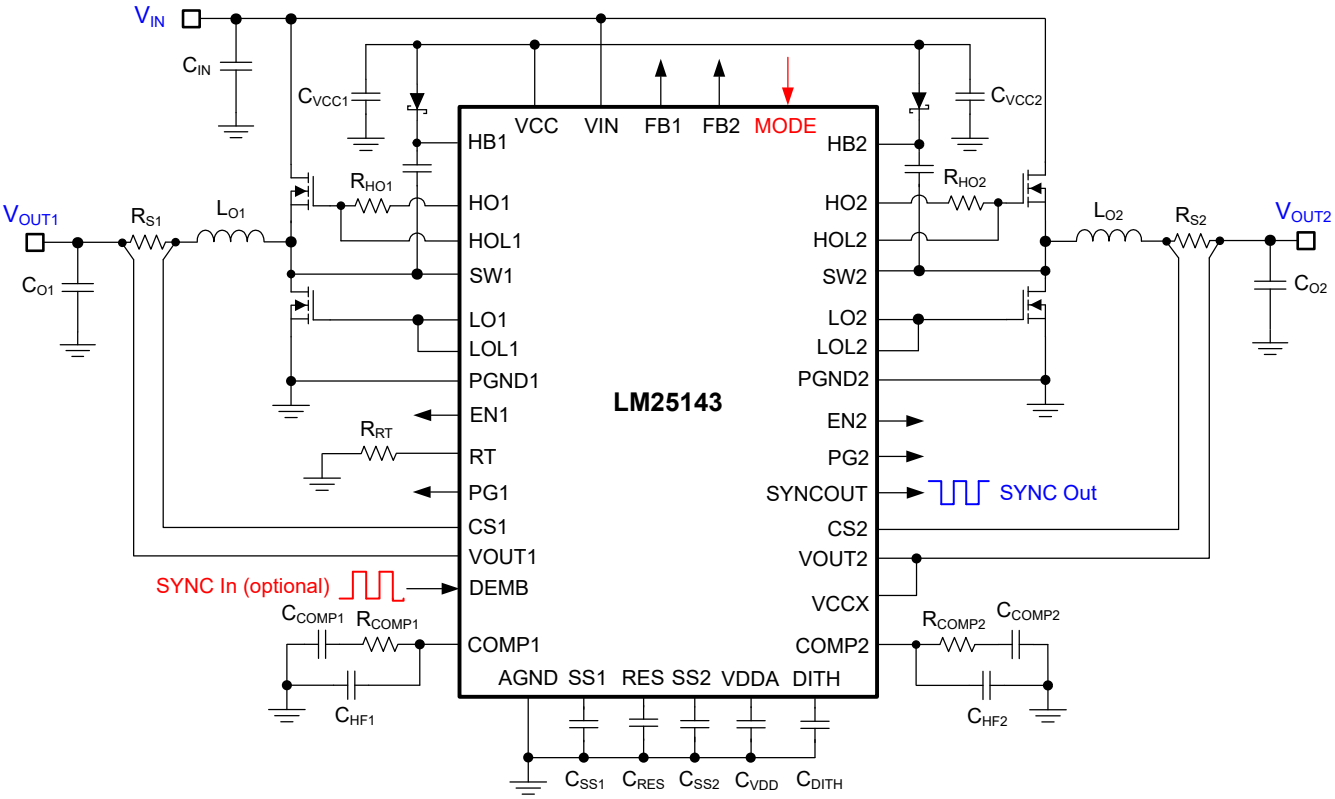


Figure 9-1. Dual-Output Regulator Schematic Diagram With an Input Voltage Range of 3.5 V to 42 V

In high input voltage applications, make sure the VIN and SW pins do not exceed their absolute maximum voltage rating of 47 V during line or load transient events. Voltage excursions that exceed the *Absolute Maximum Ratings* can damage the IC. Proceed carefully during PCB layout and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

9.3.2 High-Voltage Bias Supply Regulator (VCC, VCCX, VDDA)

The LM25143 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 42 V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

The VCC regulator output current limit is 170 mA (minimum). At power up, the regulator sources current into the capacitors connected at the VCC pin. When the VCC voltage exceeds 3.3 V, both output channels are enabled (if EN1 and EN2 are connected to a voltage greater than 2 V) and the soft-start sequence begins. Both channels remain active unless the VCC voltage falls below the VCC falling UVLO threshold of 3.1 V (typical) or EN1 or EN2 is switched to a low state. The LM25143 has two VCC pins that must be connected together on the PCB. TI recommends that two VCC capacitors are connected from VCC1 to PGND1 and from VCC2 to PGND2. The recommended range for each VCC capacitor is from 2.2 µF to 10 µF.

An internal 5-V linear regulator generates the VDDA bias supply. Bypass VDDA with a 470-nF ceramic capacitor to achieve a low-noise internal bias rail. Normally, VDDA is 5 V, but there are two operating conditions where it regulates at 3.3 V. The first is in skip cycle mode when V_{OUT1} is set to 3.3 V and V_{OUT2} is disabled. The second is in a cold-crank start-up where V_{IN} is 3.8 V and V_{OUT1} is 3.3 V.

Internal power dissipation of the VCC regulator can be minimized by connecting VCCX to a 5-V output at VOUT1 or VOUT2 or to an external 5-V supply. If the VCCX voltage is above 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Tie VCCX to AGND if it is unused. Never connect VCCX to a voltage greater than 6.5 V or less than –0.3 V. If an external supply is connected to VCCX to power the LM25143, V_{IN} must be greater than the external bias voltage during all conditions to avoid damage to the controller.

9.3.3 Enable (EN1, EN2)

The LM25143 contains two enable inputs. EN1 and EN2 facilitate independent start-up and shutdown control of V_{OUT1} and V_{OUT2}. The enable pins can be connected to a voltage as high as 70 V. If an enable input is greater than 2 V, its respective output is enabled. If an enable pin is pulled below 0.4 V, the output is shut down. If both outputs are disabled, the LM25143 is in a low-I_Q shutdown mode with a 4-µA typical current drawn from VIN. TI does not recommend leaving EN1 or EN2 floating.

9.3.4 Power-Good Monitor (PG1, PG2)

The LM25143 includes output voltage monitoring signals for V_{OUT1} and V_{OUT2} to simplify sequencing and supervision. The power-good function can be used to enable circuits that are supplied by the corresponding voltage rail or to turn on sequenced supplies. Each power-good output (PG1 and PG2) switches to a high impedance open-drain state when the corresponding output voltage is in regulation. Each output switches low when the corresponding output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25-µs deglitch filter prevents false tripping of the power-good signals during transients. TI recommends pullup resistors of 100 kΩ from PG1 and PG2 to the relevant logic rail. PG1 and PG2 are asserted low during soft start and when the corresponding buck regulator is disabled by EN1 or EN2.

If the LM25143 is in diode emulation mode (V_{DEMB} = 0 V) and enters sleep mode, the power-good comparators are turned off to reduce quiescent current consumption. When this occurs, PG1 and PG2 are open or pulled high (if a pullup resistor is connected) such that output undervoltage or overvoltage events are not detected.

9.3.5 Switching Frequency (RT)

The LM25143 oscillator is programmed by a resistor between RT and AGND to set an oscillator frequency between 100 kHz to 2.2 MHz. CLK1 is the clock for channel 1 and CLK2 is for channel 2. CLK1 and CLK2 are 180° out of phase. Use Equation 1 to calculate the RT resistance for a given switching frequency.

$$R_{RT}\left[k\Omega\right] = \frac{22}{F_{SW}\left[MHz\right]} \tag{1}$$

Under low V_{IN} conditions when either of the on times of the high-side MOSFETs exceeds the programmed oscillator period, the LM25143 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators (CLK1 and CLK2) operate independently and asynchronously until both channels can maintain output regulation at the programmed frequency.

The approximate input voltage level where this occurs is given by Equation 2.

$$V_{IN(min)} = V_{OUT} \cdot \frac{t_{SW}}{t_{SW} - t_{OFF(min)}} \tag{2}$$

where

- t_{SW} is the switching period.

- $t_{OFF(min)}$ is the minimum off time of 60 ns.

9.3.6 Clock Synchronization (DEMB)

To synchronize the LM25143 to an external source, apply a logic-level clock signal (greater than 2 V) to DEMB. The LM25143 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.5 MHz. If there is an RT resistor and a synchronization signal, the LM25143 ignores the RT resistor and synchronizes to the external clock. Under low V_{IN} conditions when the minimum off time is reached, the synchronization signal is ignored, allowing the switching frequency to reduce to maintain output voltage regulation.

9.3.7 Synchronization Out (SYNCOUT)

The SYNCOUT voltage is a logic level signal with a rising edge approximately 90° lagging HO2 (or 90° leading HO1). When the SYNCOUT signal is used to synchronize a second LM25143 controller, all four phases are 90° out of phase.

9.3.8 Spread Spectrum Frequency Modulation (DITH)

The LM25143 provides a frequency dithering option that is enabled by connecting a capacitor from DITH to AGND. This generates a triangular voltage centered at 1.2 V at DITH. See Figure 9-2. The triangular waveform modulates the oscillator frequency by ±5% of the nominal frequency set by the RT resistance. Use Equation 3 to calculate the required DITH capacitance to set the modulating frequency, F_{MOD}. For the dithering circuit to effectively attenuate the peak EMI, the modulation rate must be less than 20 kHz for proper operation of the clock circuit.

$$C_{DITH} = \frac{21\,\mu A}{2 \cdot F_{MOD} \cdot 0.1V} \tag{3}$$

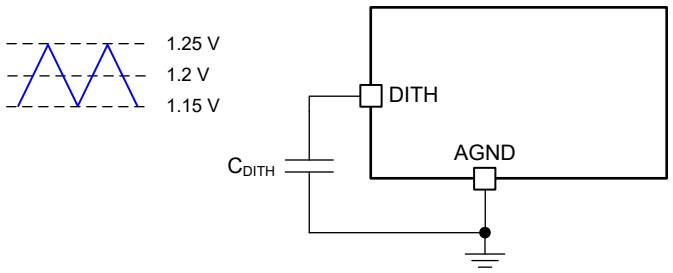


Figure 9-2. Switching Frequency Dithering

If DITH is connected to VDDA during power up, the dither feature is disabled and cannot be enabled unless VCC is recycled below the VCC UVLO threshold. If DITH is connected to AGND on power up, C_{DITH} is prevented from charging, disabling dither. Also, dither is disabled when the LM25143 is synchronized to an external clock.

9.3.9 Configurable Soft Start (SS1, SS2)

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM25143 features an adjustable soft start that determines the charging time of the output or outputs. Soft-start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced.

The LM25143 regulates the FB voltage to the SS voltage or the internal 600-mV reference, whichever is lower. At the beginning of the soft-start sequence when the SS voltage is 0 V, the internal 21-µA soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the relevant FB and output voltages. Use Equation 4 to calculate the soft-start capacitance.

$$C_{SS}(nF) = 35 \cdot t_{SS}(ms) \quad (4)$$

where

- t_{SS} is the required soft-start time.

SS can be pulled low with an external circuit to stop switching, but this is not recommended. When the controller is in FPWM mode (set by connecting DEMB to VDDA), pulling SS low results in COMP being pulled down internally as well. LO remains on and the low-side MOSFET discharges the output capacitor, resulting in large negative inductor current. In contrast, the LO gate driver is disabled when the LM25143 internal logic pulls SS low due to a fault condition.

9.3.10 Output Voltage Setpoint (FB1, FB2)

The LM25143 outputs can be independently configured for one of the two fixed output voltages with no external feedback resistors, or adjusted to the desired voltage using an external resistor divider. V_{OUT1} or V_{OUT2} can be configured as a 3.3-V output by connecting the corresponding FB pin to VDDA, or a 5-V output by connecting FB to AGND. The FB1 and FB2 connections (either VDDA or GND) are detected during power up. The configuration settings are latched and cannot be changed until the LM25143 is powered down with the VCC voltage decreasing below its falling UVLO threshold, and then powered up again.

Alternatively, the output voltage can be set using external resistive dividers from the output to the relevant FB pin. The output voltage adjustment range is between 0.6 V and 36 V. The regulation threshold at FB is 0.6 V (V_{REF}). Use Equation 5 to calculate the upper and lower feedback resistors, designated R_{FB1} and R_{FB2}, respectively. See Figure 9-3.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \cdot R_{FB2} \quad (5)$$

The recommended starting value for R_{FB2} is between 10 kΩ and 20 kΩ.

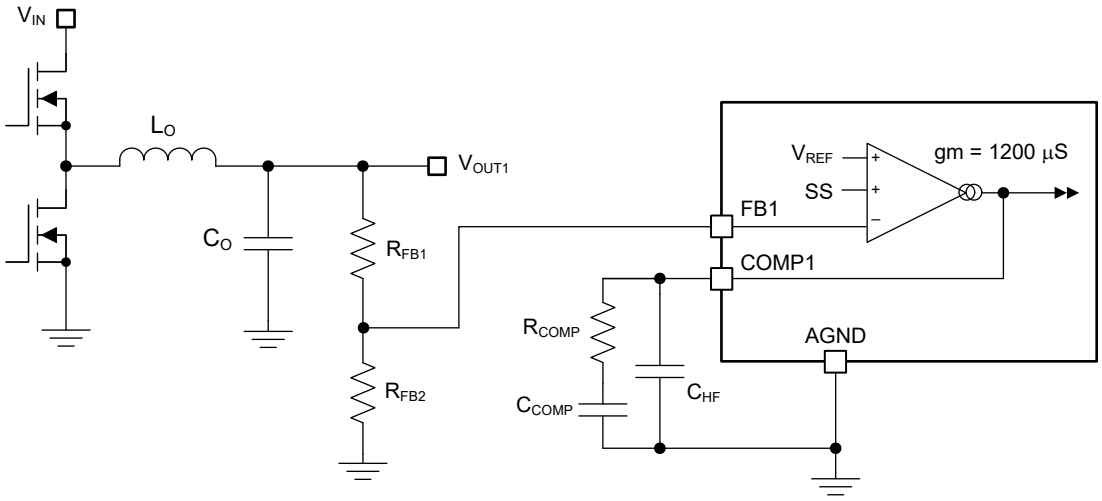


Figure 9-3. Control Loop Error Amplifier

The Thevenin equivalent impedance of the resistive divider connected to the FB pin must be greater than 5 kΩ for the LM25143 to detect the divider and set the channel to the adjustable output mode.

$$R_{TH} = \frac{R_{FB1} \cdot R_{FB2}}{R_{FB1} + R_{FB2}} > 5k\Omega \quad (6)$$

If a low I_Q mode is required, take care when selecting the external resistors. The extra current drawn from the external divider is added to the LM25143 $I_{STANDBY}$ current (15 µA typical). The divider current reflected to V_{IN} is divided down by the ratio of V_{OUT}/V_{IN}. For example, if V_{OUT} is set to 5.55 V with R_{FB1} equal to 82.5 kΩ and R_{FB2} equal to 10 kΩ, use Equation 7 to calculate the input current from a 12-V input required to supply the current in the feedback resistors.

$$I_{VIN(DIVIDER)} = \frac{V_{OUT}}{R_{FB1} + R_{FB2}} \cdot \frac{V_{OUT}}{\eta \cdot V_{IN}} = \frac{5.55\,V}{82.5k\Omega + 10k\Omega} \cdot \frac{5.55\,V}{80\% \cdot 12\,V} \approx 35\ \ A$$

$$I_{VIN} = I_{STANDBY} + I_{VIN(DIVIDER)} = 15\ \ A + 35\ \ A = 50\ \ A \tag{7}$$

If one output is enabled and the other disabled, the VCC output is in regulation. The HB voltage of the disabled channel charges to VCC through the bootstrap diode. As a result, the HO driver bias current (approximately 1.5 µA) can increase the output voltage of the disabled channel to approximately 2.2 V. If this is not desired, add a load resistor (100 kΩ) to the output that is disabled to maintain a low-voltage OFF state.

9.3.11 Minimum Controllable On Time

There are two limitations to the minimum output voltage adjustment range: the LM25143 voltage reference of 0.6 V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio of V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy Equation 8.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \cdot F_{SW} \tag{8}$$

where

- $t_{ON(min)}$ is 65 ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM25143 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5 V with an input voltage is 24 V and switching frequency of 2.1 MHz, the voltage conversion ratio test in Equation 9 is satisfied.

$$\frac{5\,V}{24\,V} > 65ns \cdot 2.1\,MHz$$

$$0.208 > 0.137 \tag{9}$$

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM25143 switching frequency to meet the requirement of Equation 8.

9.3.12 Error Amplifier and PWM Comparator (FB1, FB2, COMP1, COMP2)

Each channel of the LM25143 has an independent high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.6 V). The output of the transconductance amplifier is connected to the COMP pin, allowing the user to provide external control loop compensation. A type-II compensation network is generally recommended for peak current-mode control.

The amplifier has two gain settings, one is for normal operation with a g_m of 1200 µS and the other is for ultra-low I_Q with a g_m of 60 µS. For normal operation, connect MODE to AGND. For ultra-low operation I_Q, connect MODE to AGND through a 10-kΩ resistor.

9.3.13 Slope Compensation

The LM25143 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Use Equation 10 to calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope.

$$L_{O\text{-}IDEAL}(\ H) = \frac{V_{OUT}(V) \cdot R_S(m\Omega)}{24 \cdot F_{SW}(MHz)} \tag{10}$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, which increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

9.3.14 Inductor Current Sense (CS1, VOUT1, CS2, VOUT2)

There are two methods to sense the inductor current of the buck power stage. The first uses a current sense resistor (also known as a shunt) in series with the inductor, and the second avails of the DC resistance of the inductor (DCR current sensing).

9.3.14.1 Shunt Current Sensing

Figure 9-4 illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM25143 current sense amplifier.

If the peak differential current signal sensed from CS to VOUT exceeds the current limit threshold of 73 mV, the current limit comparator immediately terminates the applicable HO output for cycle-by-cycle current limiting. Use Equation 11 to calculate the shunt resistance.

$$R_S = \frac{V_{CS}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \tag{11}$$

where

- V_{CS} is current sense threshold of 73 mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

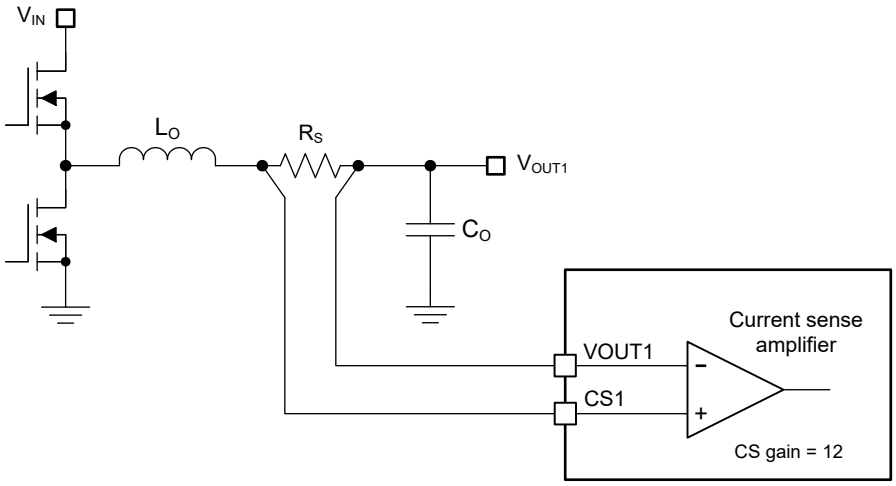


Figure 9-4. Shunt Current Sensing Implementation

The respective SS voltage is clamped 150 mV above FB during an overcurrent condition for each channel. Sixteen overcurrent events must occur before the SS clamp is enabled. This makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

9.3.14.2 Inductor DCR Current Sensing

For high-power applications that do not require accurate current-limit protection, inductor DCR current sensing is preferable. This technique provides lossless and continuous monitoring of the inductor current using an RC sense network in parallel with the inductor. Select an inductor with a low DCR tolerance to achieve a typical current limit accuracy within the range of 10% to 15% at room temperature. Components R_{CS} and C_{CS} in Figure 9-5 create a low-pass filter across the inductor to enable differential sensing of the voltage drop across the inductor DCR.

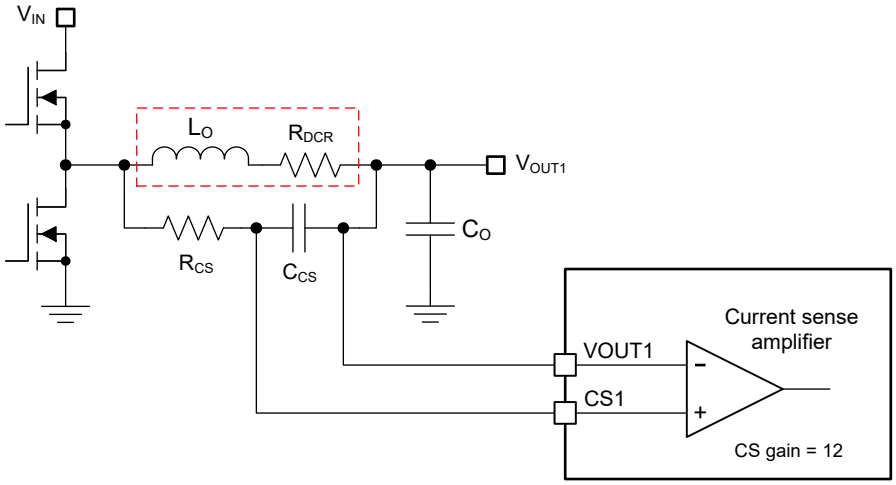


Figure 9-5. Inductor DCR Current Sensing Implementation

Use Equation 12 to calculate the voltage drop across the sense capacitor in the s-domain. When the $R_{CS}C_{CS}$ time constant is equal to L_O/R_{DCR}, the voltage developed across the sense capacitor, C_{CS}, is a replica of the inductor DCR voltage and accurate current sensing is achieved. If the $R_{CS}C_{CS}$ time constant is not equal to the L_O/R_{DCR} time constant, there is a sensing error as follows:

- $R_{CS}C_{CS} > L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is attenuated.
- $R_{CS}C_{CS} < L_O/R_{DCR}$ → the DC level is correct, but the AC amplitude is amplified.

$$V_{CS}(s) = \frac{1 + s \cdot \frac{L_O}{R_{DCR}}}{1 + s \cdot R_{CS} \cdot C_{CS}} \cdot R_{DCR} \cdot \left(I_{OUT(CL)} + \frac{\Delta I_L}{2} \right) \quad (12)$$

Choose the C_{CS} capacitance greater than or equal to 0.1 µF to maintain a low-impedance sensing network, thus reducing the susceptibility of noise pickup from the switch node. Carefully observe the guidelines found in Section 12.1 to make sure that noise and DC errors do not corrupt the differential current sense signals applied between the CS and VOUT pins.

9.3.15 Hiccup Mode Current Limiting (RES)

The LM25143 includes an optional hiccup mode protection function that is enabled when a capacitor is connected to the RES pin. In normal operation, the RES capacitor is discharged to ground. If 512 cycles of cycle-by-cycle current limiting occurs, SS is pulled low and the HO and LO outputs are disabled (see Figure 9-6). A 20-µA current source begins to charge the RES capacitor. When the RES voltage increases to 1.2 V, RES is pulled low and the SS capacitor begins to charge. The 512-cycle hiccup counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. Separate hiccup counters are provided for each channel, but the RES pin is shared by both channels. One channel can be in hiccup protection while the other operates normally. In the event that both channels are in an overcurrent condition triggering hiccup protection, the last hiccup counter to expire pulls RES low and starts the RES capacitor charging cycle. Both channels then restart together when V_{RES} = 1.2 V. If RES is connected to VDDA at power up, the hiccup function is disabled for both channels.

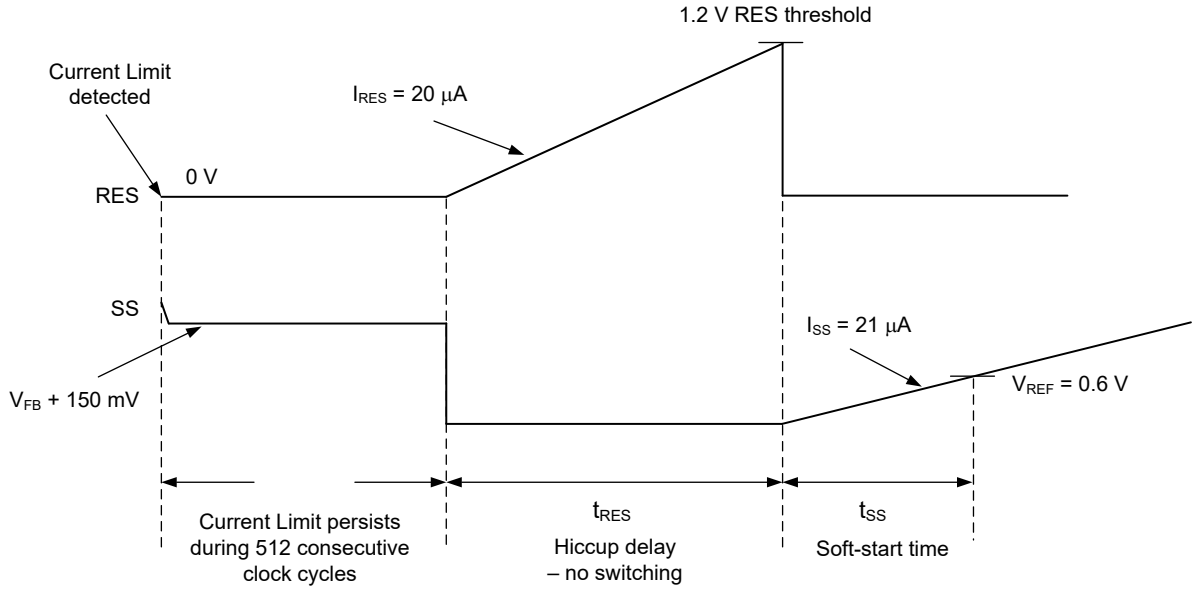


Figure 9-6. Hiccup Mode Timing Diagram

Use Equation 13 to calculate the RES capacitance.

$$C_{RES}(nF) = 17 \cdot t_{RES}(ms) \quad (13)$$

where

- t_{RES} is the specified hiccup delay as shown in Figure 9-6.

9.3.16 High-Side and Low-Side Gate Drivers (HO1/2, LO1/2, HOL1/2, LOL1/2)

The LM25143 contains N-channel MOSFET gate drivers and an associated high-side level shifter to drive the external N-channel MOSFET. The high-side gate driver works in conjunction with an external bootstrap diode,

D_{BST}, and bootstrap capacitor, C_{BST}. See Figure 9-7. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0 V and C_{BST} is charged from VCC through D_{BST}. TI recommends a 0.1-µF ceramic capacitor connected with short traces between the applicable HB and SW pins.

The LO and HO outputs are controlled with an adaptive dead-time methodology so that both outputs (HO and LO) are never enabled at the same time, preventing cross conduction. When the controller commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for the HO-SW voltage to drop below 2.5 V (typical). LO is then enabled after a small delay (HO fall to LO rising delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 2.5 V. HO is then enabled after a small delay (LO falling to HO rising delay). This technique ensures adequate dead time for any size N-channel MOSFET component or parallel MOSFET configurations.

Caution is advised when adding series gate resistors, as this can decrease the effective dead time. Each of the high-side and low-side drivers has an independent driver source and sink output pins. This allows the user to adjust drive strength to optimize the switching losses for maximum efficiency and control the slew rate for reduced EMI signature. The selected N-channel high-side MOSFET determines the appropriate bootstrap capacitance values, C_{BST}, in Figure 9-7 according to Equation 14.

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{14}$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage.
- ΔV_{BST} is the voltage variation of the high-side MOSFET driver after turn-on.

To determine C_{BST}, choose ΔV_{BST} so that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{BST} is 100 mV to 300 mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1 µF. Use high-side and low-side MOSFETs with logic level gate threshold voltages.

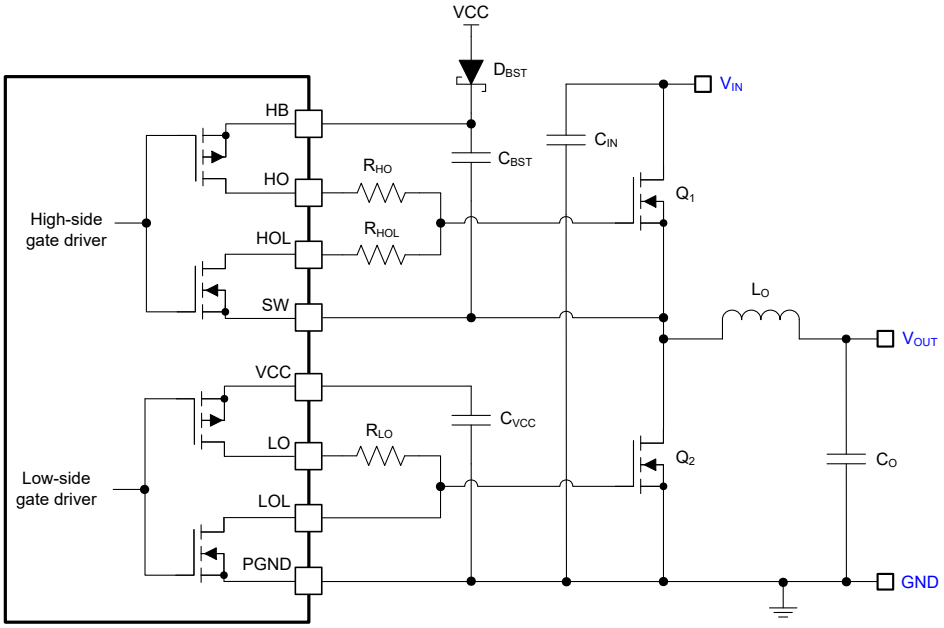


Figure 9-7. Integrated MOSFET Gate Drivers

9.3.17 Output Configurations (MODE, FB2)

9.3.17.1 Independent Dual-Output Operation

The LM25143 has two outputs that can operate independently. Both V_{OUT1} and V_{OUT2} can be set at 3.3 V or 5 V without installing external feedback resistors. Alternatively, set the output voltages between 0.6 V and 36 V using external feedback resistors based on Equation 5. See Table 9-1 and Figure 9-8. Connect MODE directly to AGND for independent outputs.

Table 9-1. Output Voltage Settings

Mode	FB1	FB2	VOUT1	VOUT2	Error Amplifier, g_m
AGND	AGND	AGND	5 V	5 V	1200 µS
AGND	VDDA	VDDA	3.3 V	3.3 V	1200 µS
AGND	VDDA	AGND	3.3 V	5 V	1200 µS
AGND	AGND	VDDA	5 V	3.3 V	1200 µS
AGND	$R_{divider}$	$R_{divider}$	0.6 V to 36 V	0.6 V to 36 V	1200 µS
10 kΩ to AGND	AGND	AGND	5 V	5 V	60 µS
10 kΩ to AGND	VDDA	VDDA	3.3 V	3.3 V	60 µS
10 kΩ to AGND	VDDA	AGND	3.3 V	5 V	60 µS
10 kΩ to AGND	AGND	VDDA	5 V	3.3 V	60 µS
10 kΩ to AGND	$R_{divider}$	$R_{divider}$	0.6 V to 36 V	0.6 V to 36 V	60 µS

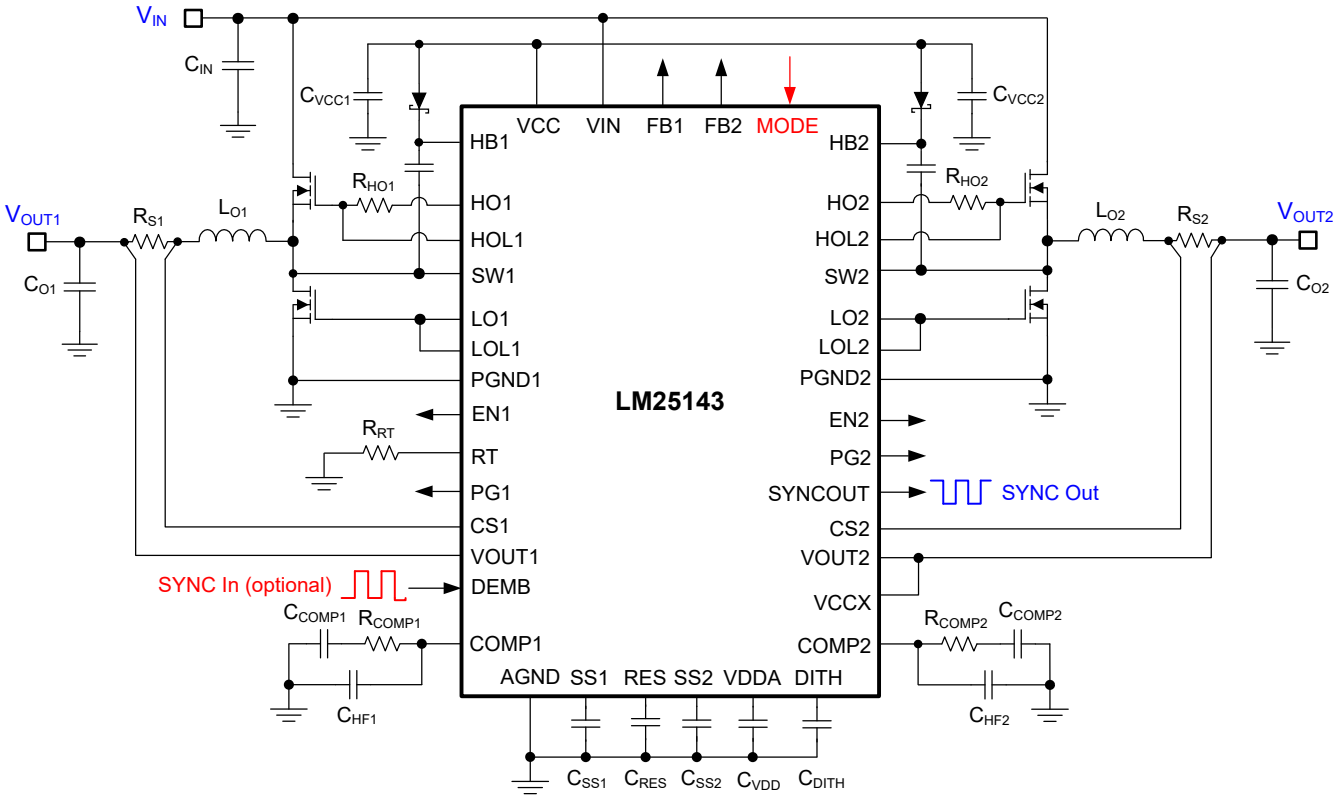


Figure 9-8. Regulator Schematic Configured for Independent Dual Outputs

9.3.17.2 Single-Output Interleaved Operation

Connect the MODE to VDDA and FB2 to AGND to configure the LM25143 for interleaved operation. This disables the channel 2 error amplifier and places it in a high impedance state. The controller is then in a primary and secondary configuration. Connect COMP1 to COMP2 and SS1 to SS2. Connect FB1 to VDDA for a

3.3-V output and to AGND for a 5-V output. Connect FB1 to an external feedback divider for an output voltage between 0.6 V to 36 V. See Table 9-2 and Figure 9-9.

The LM25143 in single-output interleaved operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

Table 9-2. Single-Output Interleaved Operation

Mode	FB1	FB2	Output Setpoint
VDDA	AGND	AGND	5 V
VDDA	VDDA	AGND	3.3 V
VDDA	$R_{divider}$	AGND	0.6 V to 36 V

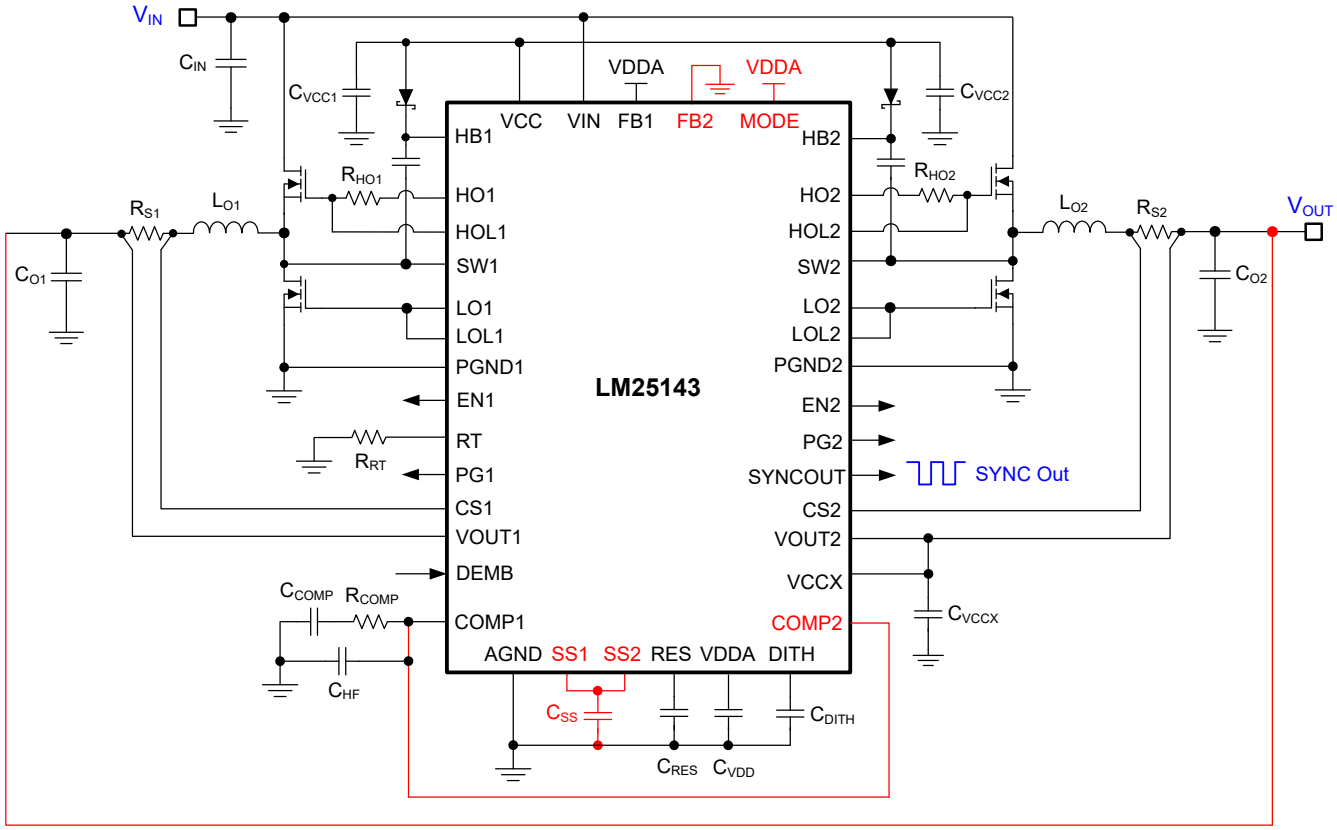


Figure 9-9. Two-Phase Regulator Schematic Configured for Single-Output Interleaved Operation

9.3.17.3 Single-Output Multiphase Operation

To configure the LM25143 for multiphase operation (three or four phases), two LM25143 controllers are required. See Figure 9-10. Configure the first controller (CNTRL1) as a primary and the second controller (CNTRL2) as a secondary. To configure the second controller as a secondary, connect the MODE and FB2 pins to VDDA. This disables both feedback error amplifiers of the secondary controller, placing them in a high-impedance state. Connect COMP1 and COMP2 of the primary and secondary together. Connect SS1 and SS2 of the primary and secondary together. Connect SYNCOUT of the primary controller to DEMB (SYNCIN) of the secondary. The SYNCOUT of the primary controller is 90° out-of-phase and facilitates interleaved operation. RT is not used for the oscillator when the LM25143 is in secondary mode but instead used for slope compensation. Therefore, select the RT resistance to be the same as that of the primary. The oscillator is derived from the primary controller. FPWM or DEM mode for the secondary is set by connecting its FB1 to VDDA or AGND, respectively. FPWM or DEM mode of the primary controller is set by its DEMB pin. See Table 9-3.

The LM25143 in single-output multiphase operation does not support phase shedding when the output voltage is set between 0.6 V to 1.5 V.

See the *Benefits of a Multiphase Buck Converter White Paper* and *Multiphase Buck Design From Start to Finish Application Report* for more information.

Table 9-3. Single-Output Multiphase Operation

Mode	FB1 (Secondary)	FB2 (Secondary)	DEM or FPWM (Secondary)
VDDA	AGND	VDDA	DEM
VDDA	VDDA	VDDA	FPWM

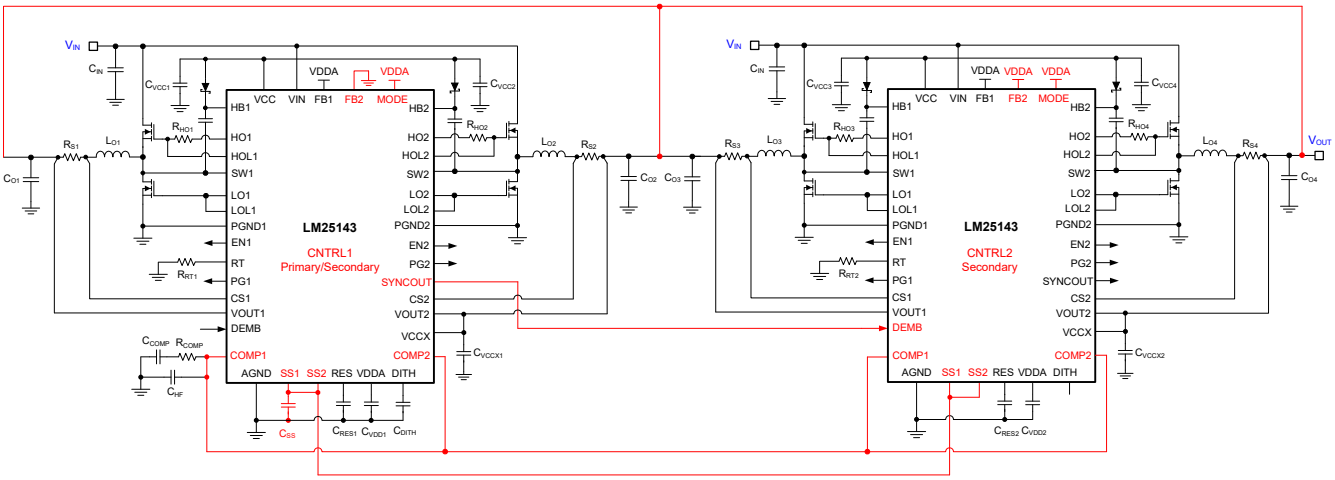


Figure 9-10. Multiphase Regulator Schematic Configured for Single-Output Interleaved Operation

Note

A design with five or more phases (using three or more LM25143 controllers) is feasible when appropriately phase-shifted clock signals are available. For example, a 6-phase design requires three LM25143 controllers with 0°, 60°, and 120° external SYNC signals to achieve the ideal phase separation of 360° divided by the total number of phases.

9.4 Device Functional Modes

9.4.1 Standby Modes

The LM25143 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage does not demand driver output pulses on a cycle-by-cycle basis. When the LM25143 controller detects 16 missed switching cycles, it enters standby mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM25143 to go into standby mode, the controller must be programmed for diode emulation (V_{DEMB} < 0.4 V).

There are two standby modes: ultra-low I_Q and normal mode. To enter ultra-low I_Q mode, connect MODE to AGND through a 10-kΩ resistor. In ultra-low I_Q mode, the transconductance amplifier gain is reduced from 1200 µS to 60 µS. The typical ultra-low I_Q is 15 µA with channel 1 set to 3.3 V and the channel 2 disabled. If ultra-low I_Q is not required, connect MODE to AGND. In normal mode, the I_Q is 25 µA with channel 1 set to 3.3 V and the second channel disabled.

9.4.2 Diode Emulation Mode

A fully synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during light-load, overvoltage, and prebias start-up conditions. The LM25143 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the applicable SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at light-load conditions; the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the DEMB pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect DEMB to AGND. If FPWM or continuous conduction mode (CCM) operation is desired, tie DEMB to VDDA. See Table 9-4. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in FPWM. A gradual change from DCM to CCM operation provides monotonic start-up performance.

Table 9-4. DEMB Settings

DEMB	FPWM/DEM
VDDA	FPWM
AGND	DEM
External clock	FPWM

9.4.3 Thermal Shutdown

The LM25143 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. Pulls SS1/2 and PG1/2 low
3. Turns off the VCC regulator
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical)

This is a non-latching protection, and as such, the device cycles into and out of thermal shutdown if the fault persists.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM25143 is a synchronous buck controller used to convert a higher input voltage to two lower output voltages. The following sections discuss the design procedure for a dual-output implementation using a specific circuit design example. To expedite and streamline the process of designing of a LM25143-based regulator, a comprehensive *LM25143 Quickstart Calculator* is available for download to assist the designer with component selection for a given application.

10.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The subsequent subsections discuss the following:

- Output inductor
- Input and output capacitors
- Power MOSFETs
- EMI input filter

10.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 15 based on a peak inductor current given by Equation 16.

$$L_O = \frac{V_{OUT}}{\Delta I_L \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{15}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{16}$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

10.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics – equivalent series resistance (ESR) and equivalent series inductance (ESL) – take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by Equation 17.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \tag{17}$$

Figure 10-1 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as quickly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

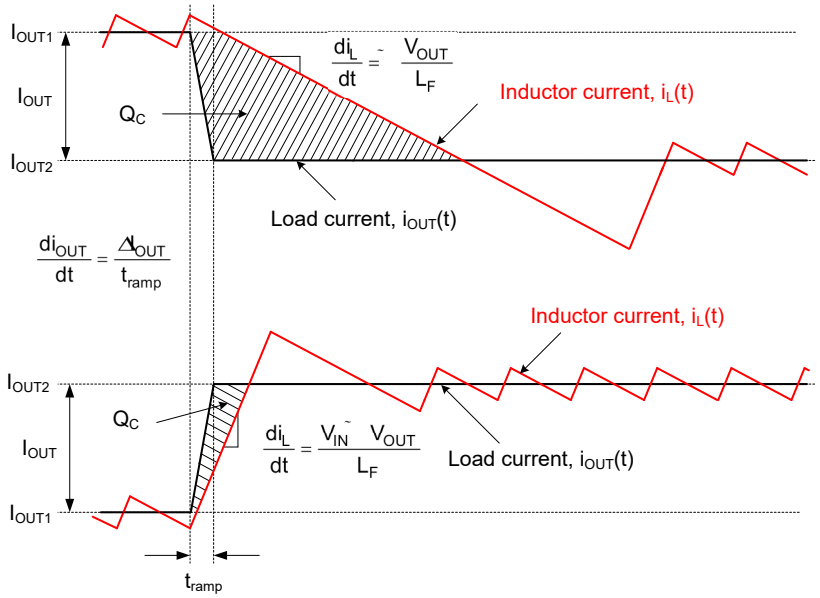


Figure 10-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12-V input to low output voltage (for example, 3.3 V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \tag{18}$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on the package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 17 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Two to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice for a 5-V output. Use Equation 18 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid-frequency and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

10.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use Equation 19 to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1 - D) + \frac{\Delta I_L^2}{12} \right)} \tag{19}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors is greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sink I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, use Equation 20 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta \quad = \frac{\cdot \times \cdot \left(\quad - \times \right)}{\cdot =} + \quad \cdot \tag{20}$$

Use Equation 21 to calculate the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$= \quad \geq \frac{\times \cdot \left(\quad - \times \right) \cdot}{\cdot \left(\Delta \quad - \quad \cdot \quad \right)} \tag{21}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and four 10-µF 50-V X7R ceramic

decoupling capacitors are usually sufficient for 12-V battery automotive applications. Select the input bulk capacitor based on its ripple current rating and operating temperature range.

Of course, a two-channel buck regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The previous equations represent valid calculations when one output is disabled and the other output is fully loaded.

10.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in a LM25143 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 5 V
- Drain-source voltage rating, BV_{DSS}, is typically 30 V, 40 V, or 60 V, depending on the maximum input voltage.
- Gate charge parameters at V_{GS} = 5 V
- Output charge, Q_{OSS}, at the relevant input voltage
- Body diode reverse recovery charge, Q_{RR}
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. With a Miller plateau voltage typically in the range of 2 V to 3 V, the 5-V gate drive amplitude of the LM25143 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses for one channel are summarized by the equations presented in Table 10-1, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the *LM25143 Quickstart Calculator*. The calculator is available for download from the LM25143 product folder to assist with power loss calculations.

Table 10-1. MOSFET Power Losses

Power Loss Mode	High-Side MOSFET	Low-Side MOSFET
MOSFET conduction(2) (3)	$P_{cond1} = D \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET switching	$P_{sw1} = \frac{V_{IN} \cdot F_{SW}}{2} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET gate drive(1)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET output charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	Negligible
Body diode conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body diode reverse recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance, and the relevant driver resistance of the LM25143.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this is offset by the stored energy E_{oss2} on C_{oss2}. For more detail, refer to "Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs," ECCE 2016.

(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on time (or D interval) and typically incurs most of the switching losses, so it is imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the following:

- Losses due to conduction
- Switching (voltage-current overlap)
- Output charge
- Typically two-thirds of the net loss attributed to body diode reverse recovery

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition dead times. The LM25143, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM25143 is well suited to drive TI's portfolio of NexFET™ power MOSFETs.

10.1.1.5 EMI Filter

As expressed by Equation 22, switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{22}$$

An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

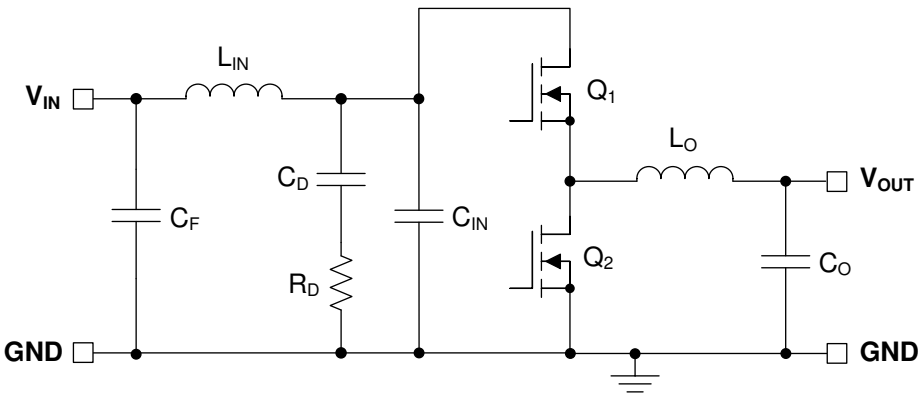


Figure 10-2. Buck Regulator With π-Stage EMI Filter

Referencing the filter schematic in Figure 10-2, the EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.

- The input filter inductance, L_{IN}, is usually selected between 1 µH and 10 µH, but it can be lower to reduce losses in a high-current design.
- Calculate input filter capacitance, C_F.
- Calculate damping capacitance, C_D, and damping resistance, R_D.

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 23.

$$Attn = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \cdot F_{SW} \cdot C_{IN}} \cdot \sin\left(\pi \cdot D_{MAX}\right) \cdot \frac{1}{1\ V}\right) - V_{MAX} \tag{23}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification (for example, CISPR 25 Class 5).
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 24.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}}\right)^2 \tag{24}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Use Equation 25 to calculate the resonant frequency of the filter.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \tag{25}$$

The purpose of R_D is to reduce the peak output impedance of the filter at its resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of the filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 26.

$$C_D \geq 4 \cdot C_{IN} \tag{26}$$

Use Equation 27 to select the damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{27}$$

10.1.2 Error Amplifier and Compensation

Figure 10-3 shows a Type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O\text{-}EA}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown in Equation 28.

$$G_{EA(open\,loop)}(s) = -\frac{g_m \cdot R_{O\text{-}EA}}{1 + s \cdot R_{O\text{-}EA} \cdot C_{BW}} \tag{28}$$

The EA high-frequency pole is neglected in Equation 28. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in Equation 29.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \cdot \frac{g_m \cdot R_{O\text{-}EA} \cdot \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{29}$$

where

- V_{REF} is the feedback voltage reference of 0.6 V.
- g_m is the EA gain transconductance of 1200 µS.
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 64 MΩ.

$$\omega_{Z1} = \frac{1}{R_{COMP} \cdot C_{COMP}} \tag{30}$$

$$\omega_{p1} = \frac{1}{R_{O\text{-}EA} \cdot \left(C_{COMP} + C_{HF} + C_{BW}\right)} \cong \frac{1}{R_{O\text{-}EA} \cdot C_{COMP}} \tag{31}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \cdot \left(C_{COMP} \parallel \left(C_{HF} + C_{BW}\right)\right)} \cong \frac{1}{R_{COMP} \cdot C_{HF}} \tag{32}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, $R_{COMP} << R_{O\text{-}EA}$ and $C_{COMP} >> C_{BW}$ and C_{HF}, so the approximations are valid.

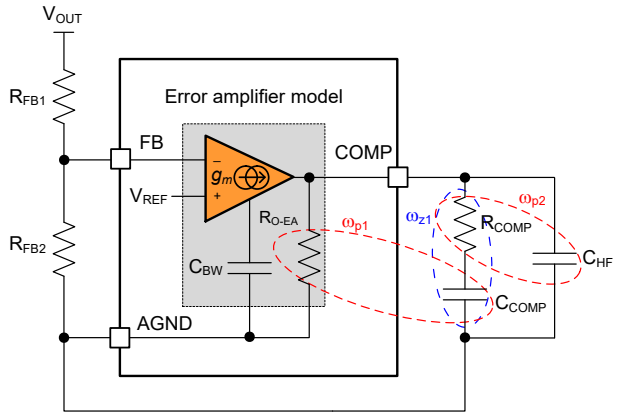


Figure 10-3. Error Amplifier and Compensation Network

10.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation, and test results of an LM25143-powered implementation, see the *TI Designs* reference design library.

10.2.1 Design 1 – 5-V and 3.3-V Dual-Output Buck Regulator for Computing Applications

Figure 10-4 shows the schematic diagram of a dual-output synchronous buck regulator with output voltages setpoints of 3.3 V and 5 V and a rated load current of 7 A for each output. In this example, the target half-load and full-load efficiencies are 91% and 90%, respectively, based on a nominal input voltage of 12 V that ranges from 3.5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve efficiency.

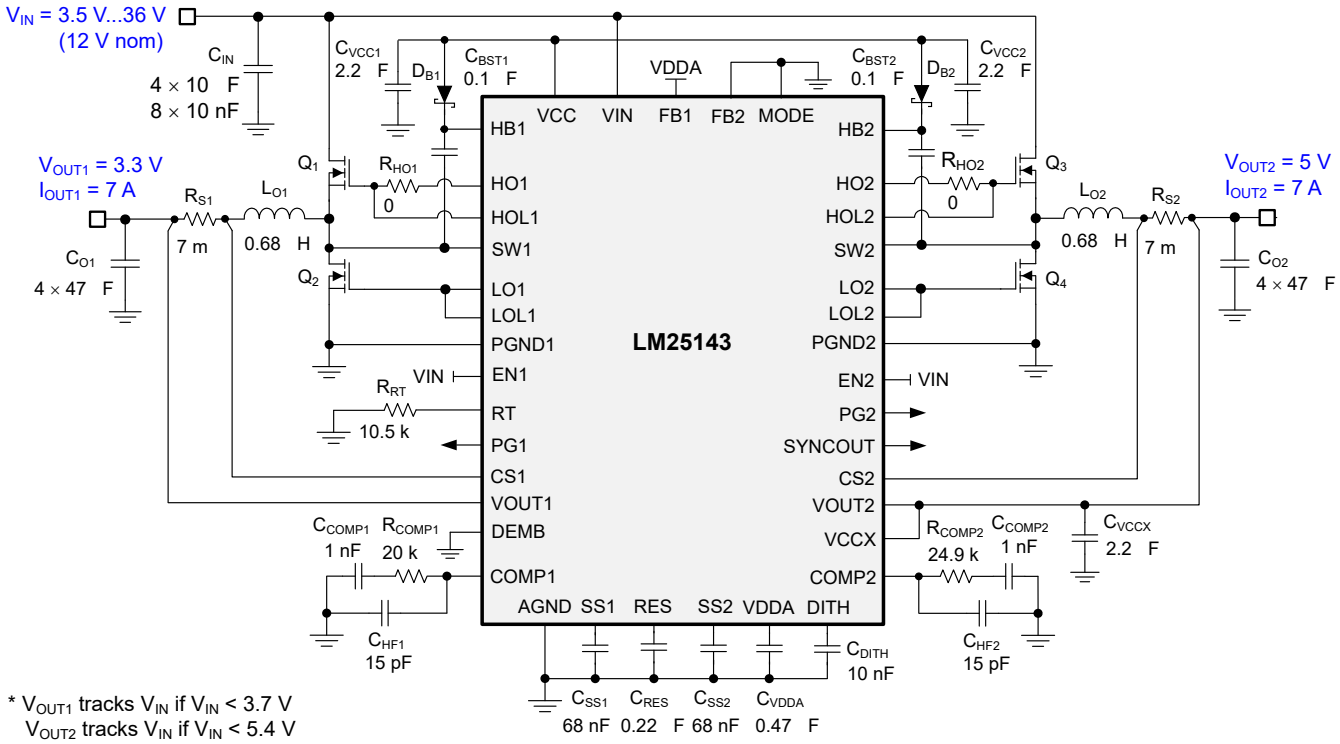


Figure 10-4. Application Circuit 1 With LM25143 Dual-Output Buck Regulator at 2.1 MHz

Note

This and subsequent design examples are provided herein to showcase the LM25143 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See Section 10 for more details.

10.2.1.1 Design Requirements

Table 10-2 shows the intended input, output, and performance parameters for this design example.

Table 10-2. Design Parameters

Design Parameter	Value
Input voltage range (steady state)	8 V to 18 V
Min transient input voltage (cold crank)	3.5 V
Max transient input voltage (load dump)	36 V
Output voltages	3.3 V, 5 V
Output currents	7 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Standby current, output 1 enabled, no load	< 50 µA
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start times are set at 2 ms by 68-nF soft-start capacitors.

The selected buck regulator powertrain components are cited in Table 10-3, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 10.1.1.4. This design uses a low-DCR, metal-powder composite inductor, and ceramic output capacitor implementation.

Table 10-3. List of Materials for Application Circuit 1

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm	Würth Elektronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm	Würth Elektronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.7 × 6.5 × 3.1 mm	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W	Susumu	KRL2012E-M-R007
U_1	1	LM25143 42-V dual-channel/phase synchronous buck controller	Texas Instruments	LM25143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25143 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the regulator specifications using the *LM25143 Quickstart Calculator* available for download from the LM25143 product folder.

10.2.1.2.3 Inductor Calculation

1. Use Equation 33 to calculate the required buck inductance for each channel based on a 30% inductor ripple current at nominal input voltages.

$$L_{O1} = \frac{V_{OUT1}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT1}}{\Delta I_L \cdot F_{SW}} \right) = \frac{3.3\,V}{12\,V} \cdot \left(\frac{12\,V - 3.3\,V}{2.1A \cdot 2.1MHz} \right) = 0.54 \;\; H$$

$$L_{O2} = \frac{V_{OUT2}}{V_{IN(nom)}} \cdot \left(\frac{V_{IN(nom)} - V_{OUT2}}{\Delta I_L \cdot F_{SW}} \right) = \frac{5\,V}{12\,V} \cdot \left(\frac{12\,V - 5\,V}{2.1A \cdot 2.1MHz} \right) = 0.66 \;\; H \quad (33)$$

2. Select a standard inductor value of 0.68 µH for both channels. Use Equation 34 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the LM25143 has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO1(PK)} = I_{OUT1} + \frac{\Delta I_{LO1}}{2} = I_{OUT1} + \frac{V_{OUT1}}{2 \cdot L_{O1} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN(max)}} \right) = 7\,A + \frac{3.3\,V}{2 \cdot 0.68 \quad \cdot} \cdot \left(1 - \frac{3.3\,V}{} \right) = 7.94\,A$$

$$I_{LO2(PK)} = I_{OUT2} + \frac{\Delta I_{LO2}}{2} = I_{OUT2} + \frac{V_{OUT2}}{2 \cdot L_{O2} \cdot F_{SW}} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN(max)}} \right) = 7\,A + \frac{5\,V}{2 \cdot 0.68 \quad \cdot} \cdot \left(1 - \frac{5\,V}{18\,V} \right) = 8.27\,A \quad (34)$$

3. Based on Equation 10, use Equation 35 to cross-check the inductance to set a slope compensation equal to the ideal one times the inductor current downslope.

$$L_{O1(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{3.3\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.46 \;\; H$$

$$L_{O2(sc)} = \frac{V_{OUT}\,(V) \cdot R_S\,(m\Omega)}{24 \cdot F_{SW}\,(MHz)} = \frac{5\,V \cdot 7\,m\Omega}{24 \cdot 2.1\,MHz} = 0.69 \;\; H \quad (35)$$

10.2.1.2.4 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 20% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistances using Equation 36.

$$R_{S1} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO1(PK)}} = \frac{73\,mV}{1.2 \cdot 7.94\,A} = 7.66\,m\Omega$$

$$R_{S2} = \frac{V_{CS(th)}}{1.2 \cdot I_{LO2(PK)}} = \frac{73\,mV}{1.2 \cdot 8.27\,A} = 7.36\,m\Omega \quad (36)$$

where

- $V_{CS(th)}$ is the 73-mV current limit threshold.

2. Select a standard resistance value of 7 mΩ for both shunts. A 0508 footprint component with wide aspect ratio termination design provides 1-W power rating, low parasitic series inductance, and compact PCB layout. Carefully observe the layout guidelines to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at [CS1, VOUT1] and [CS2, VOUT2].
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the LM25143.
5. The CS-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay of $t_{CS-DELAY}$ of 40 ns, use Equation 37 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LO1(PK-SC)} = I_{LO2(PK-SC)} = \frac{V_{CS(th)}}{R_{S1}} + \frac{V_{IN(max)} \cdot t_{CS-DELAY}}{L_{O1}} = \frac{73\,mV}{7\,m\Omega} + \frac{18\,V \cdot 40\,ns}{0.68\ \ H} = 11.49\,A \quad (37)$$

6. Based on this result, select an inductor for each channel with saturation current greater than 12 A across the full operating temperature range.

10.2.1.2.5 Output Capacitors

1. Use Equation 38 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load) assuming a load transient deviation specification of 1.5% (50 mV for a 3.3-V output).

$$C_{OUT1} \quad \frac{L_{O1}\ \ \Delta I_{OUT1}^{\ 2}}{\left(V_{OUT1} + \Delta V_{OVERSHOOT1}\right)^2 - V_{OUT1}^{\ 2}} \quad V \quad \frac{0.68\ \ H\ \left(7\,A\right)^2}{\left(3.3\,V + 50\,mV\right)^2 - \left(3.3\,V\right)^2} \quad V \quad 100.2\ \ F$$

$$C_{OUT2} \quad \frac{L_{O2}\ \ \Delta I_{OUT2}^{\ 2}}{\left(V_{OUT2} + \Delta V_{OVERSHOOT2}\right)^2 - V_{OUT2}^{\ 2}} \quad V \quad \frac{0.68\ \ H\ \left(7\,A\right)^2}{\left(5\,V + 75\,mV\right)^2 - \left(5\,V\right)^2} \quad V \quad 44.1\ \ F \quad (38)$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select four 47-µF, 6.3-V, X7R, 1210 ceramic output capacitors for each channel. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use Equation 39 to estimate the peak-peak output voltage ripple of channel 1 at nominal input voltage.

$$\Delta V_{OUT1} = \sqrt{\left(\frac{\Delta I_{LO1}}{8 \cdot F_{SW} \cdot C_{OUT1}}\right)^2 + \left(R_{ESR} \cdot \Delta I_{LO1}\right)^2} = \sqrt{\left(\frac{1.89\,A}{8 \cdot 2.1\,MHz \cdot 130\ \ F}\right)^2 + \left(1\,m\Omega \cdot 1.89\,A\right)^2} \approx 2\,mV \quad (39)$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 130 µF is the total effective (derated) ceramic output capacitance at 3.3 V.

4. Use Equation 40 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO1(RMS)} = \frac{\Delta I_{LO1}}{\sqrt{12}} = \frac{1.89\,A}{\sqrt{12}} = 0.55\,A$$

$$I_{CO2(RMS)} = \frac{\Delta I_{LO2}}{\sqrt{12}} = \frac{2.53\,A}{\sqrt{12}} = 0.73\,A \quad (40)$$

10.2.1.2.6 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. As mentioned earlier, dual-channel interleaved operation significantly reduces the input ripple amplitude. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Worst case input ripple for a two-channel buck regulator typically corresponds to when one channel operates at full load and the other channel is disabled or operates at no load. Use Equation 41 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(RMS)} = I_{OUT1} \cdot \sqrt{D \cdot (1-D)} = 7\,A \cdot \sqrt{0.5 \cdot (1-0.5)} = 3.5\,A \quad (41)$$

3. Use Equation 42 to find the required input capacitance.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT1}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT1})} = \frac{0.5 \cdot (1-0.5) \cdot 7\,A}{2.1MHz \cdot (120\,mV - 2m\Omega \cdot 7\,A)} = 7.8\ \ F \quad (42)$$

where

- ΔV_{IN} is the input peak-to-peak ripple voltage specification.
- R_{ESR} is the input capacitor ESR.

4. Recognizing the voltage coefficient of ceramic capacitors, select two 10-µF, 50-V, X7R, 1210 ceramic input capacitors for each channel. Place these capacitors adjacent to the relevant power MOSFETs.
5. Use four 10-nF, 50-V, X7R, 0603 ceramic capacitors near each high-side MOSFET to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100 MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower EMI signature. Refer to Figure 12-2 in Section 12.1 for more detail.

10.2.1.2.7 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified open-loop gain crossover frequency, f_C, of 60 kHz, use Equation 43 to calculate R_{COMP1}, assuming an effective output capacitance of 130 µF. Select R_{COMP1} of 20 kΩ.

$$R_{COMP1} = 2 \cdot \pi \cdot f_C \cdot \frac{V_{OUT}}{V_{REF}} \cdot \frac{R_S \cdot G_{CS}}{g_m} \cdot C_{OUT} = 2 \cdot \pi \cdot 60kHz \cdot \frac{3.3\,V}{0.6\,V} \cdot \frac{7m\Omega \cdot 12}{1200\ \ S} \cdot 130\ \ F = 18.9k\Omega \quad (43)$$

2. Calculate C_{COMP1} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Select a C_{COMP1} capacitor of 1 nF.

$$C_{COMP1} = \frac{10}{2 \cdot \pi \cdot f_C \cdot R_{COMP1}} = \frac{10}{2 \cdot \pi \cdot 60kHz \cdot 20\,k\Omega} = 1.3nF \quad (44)$$

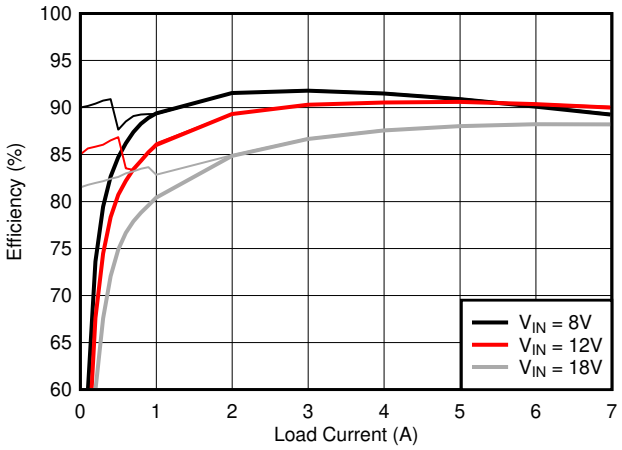
3. Calculate C_{HF1} to create a pole at the ESR zero and to attenuate high-frequency noise at COMP. Select a C_{HF1} capacitor of 15 pF.

$$C_{HF1} = \frac{1}{2 \cdot \pi \cdot f_{ESR} \cdot R_{COMP1}} = \frac{1}{2 \cdot \pi \cdot 500\,kHz \cdot 20\,k\Omega} = 15.9\,pF \quad (45)$$

Note

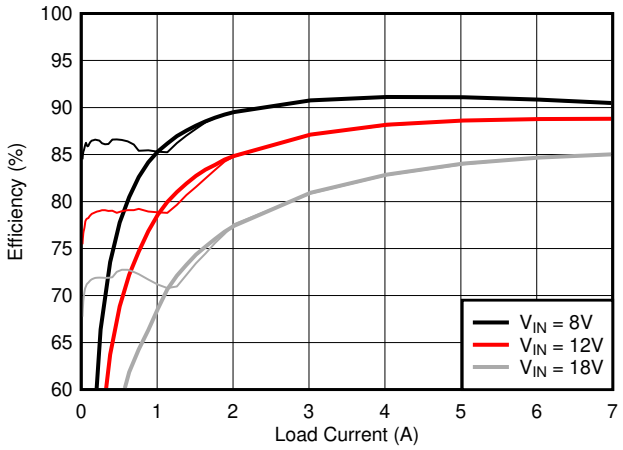
Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

10.2.1.3 Application Curves



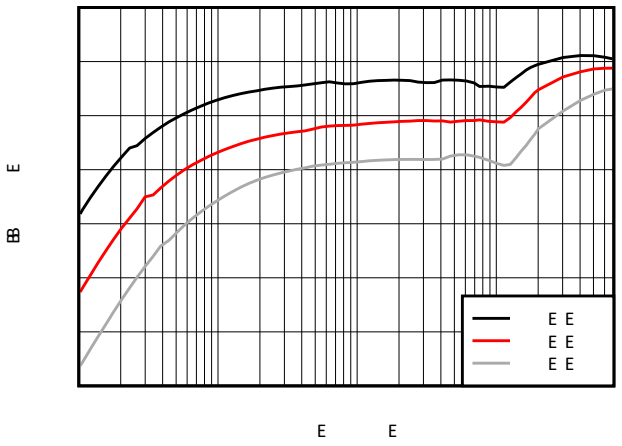
Channels loaded equally

Figure 10-5. Efficiency Versus I_{OUT}



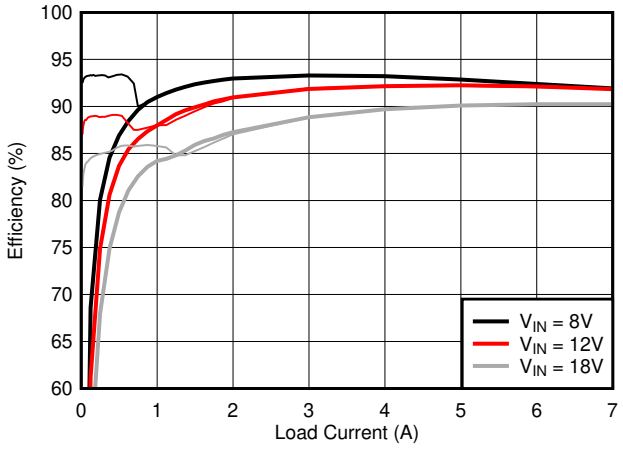
3.3-V output, channel 2 disabled

Figure 10-6. Efficiency Versus I_{OUT}



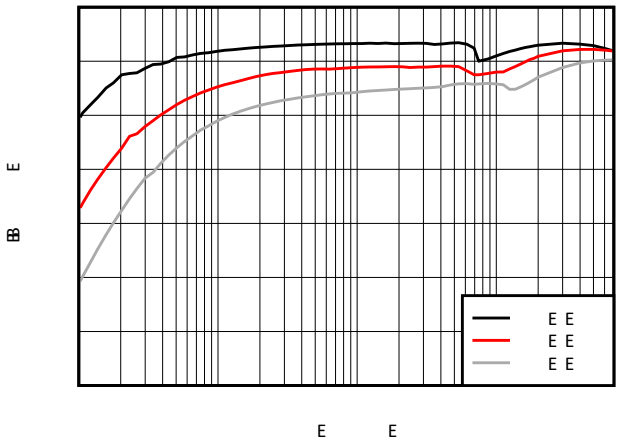
3.3-V output, channel 2 disabled

Figure 10-7. Efficiency Versus I_{OUT}, Log Scale



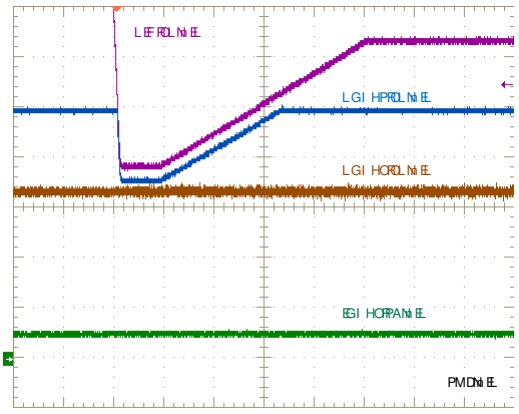
5-V output, channel 1 disabled

Figure 10-8. Efficiency Versus I_{OUT}



5-V output, channel 1 disabled

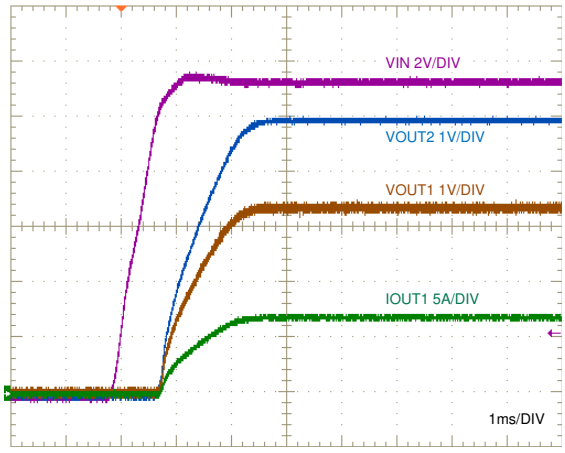
Figure 10-9. Efficiency Versus I_{OUT}, Log Scale



1-A loads

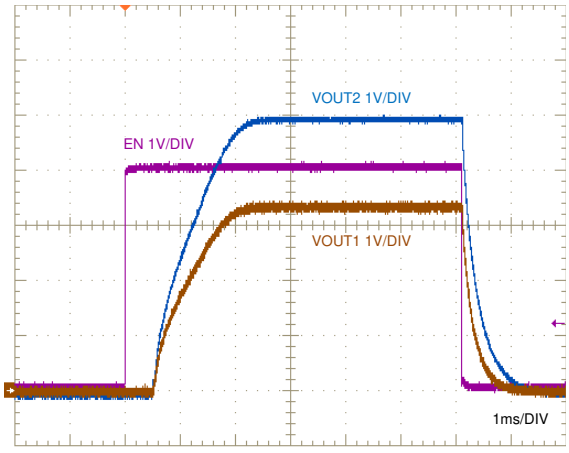
Figure 10-10. Cold-Crank Response to V_{IN} = 3.8 V

10.2.1.3 Application Curves (continued)



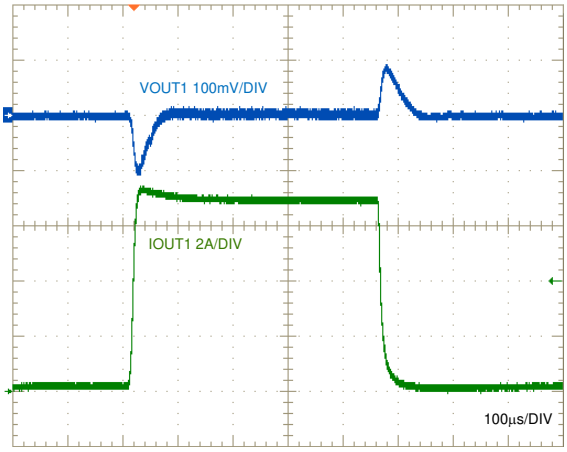
V_{IN} step to 12 V 7-A resistive loads

Figure 10-11. Start-Up Characteristic



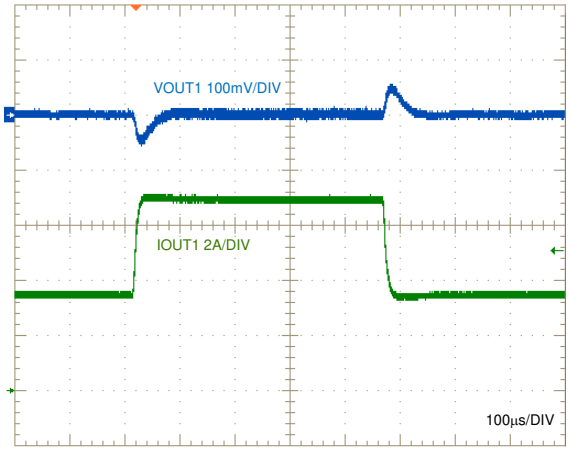
V_{IN} = 12 V 7-A resistive loads

Figure 10-12. ENABLE ON and OFF Characteristic



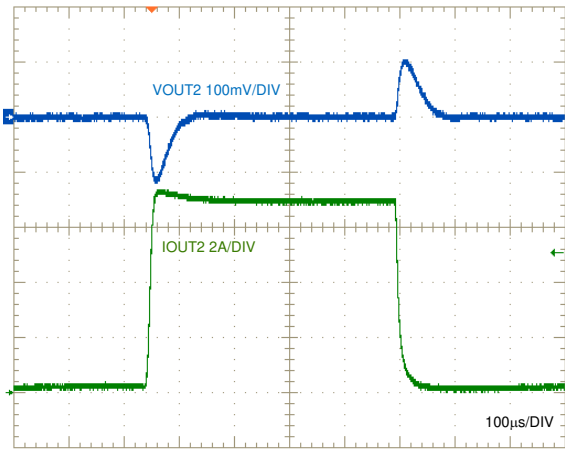
V_{IN} = 12 V FPWM

Figure 10-13. Load Transient, 3.3-V Output, 0 A to 7 A



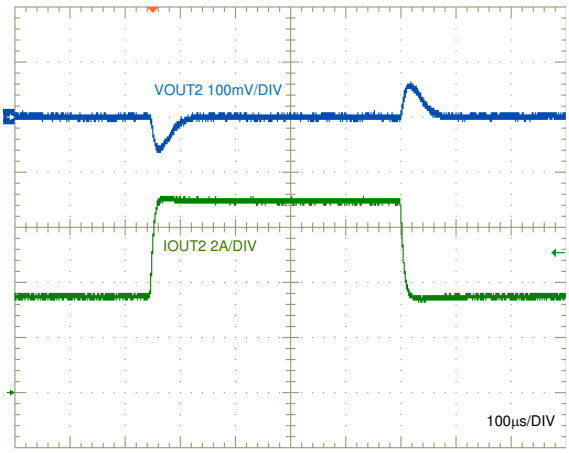
V_{IN} = 12 V FPWM

Figure 10-14. Load Transient, 3.3-V Output, 3.5 A to 7 A



V_{IN} = 12 V FPWM

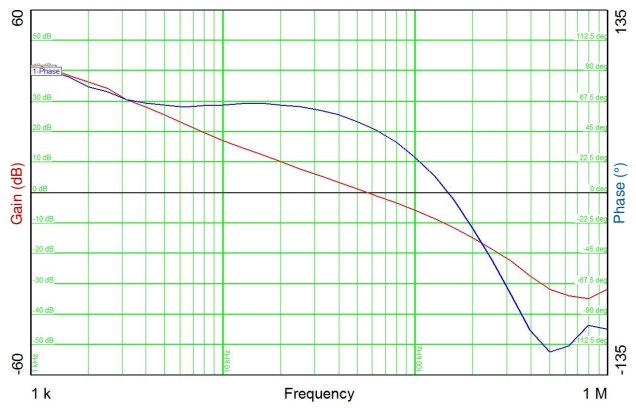
Figure 10-15. Load Transient, 5-V Output, 0 A to 7 A



V_{IN} = 12 V FPWM

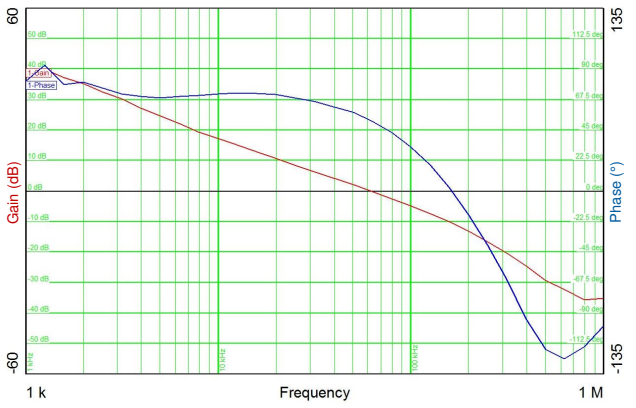
Figure 10-16. Load Transient, 5-V Output, 3.5 A to 7 A

10.2.1.3 Application Curves (continued)



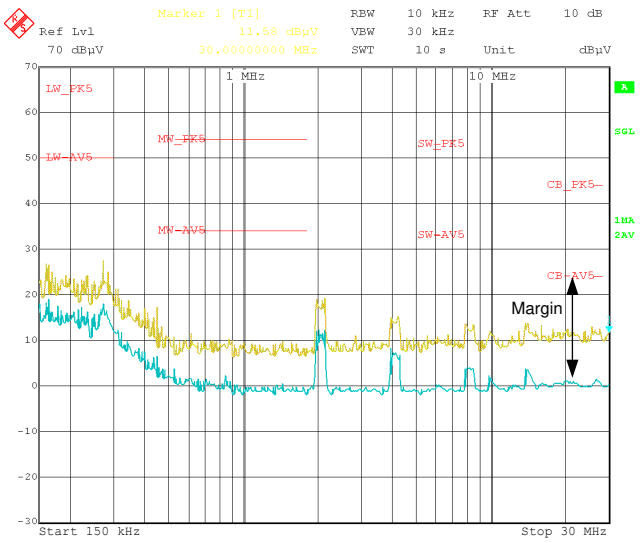
V_{IN} = 12 V 7-A resistive load

Figure 10-17. Bode Plot, 3.3-V Output



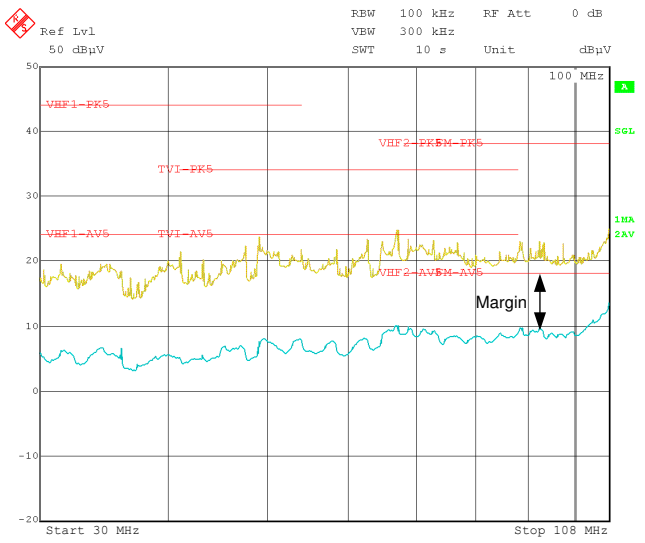
V_{IN} = 12 V 7-A resistive load

Figure 10-18. Bode Plot, 5-V Output



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

Figure 10-19. CISPR 25 Class 5 Conducted EMI, 150 kHz to 30 MHz



V_{IN} = 13.5 V V_{OUT} = 5 V 7-A resistive load

Figure 10-20. CISPR 25 Class 5 Conducted EMI, 30 MHz to 108 MHz

10.2.2 Design 2 – Two-Phase, 15-A, 2.1-MHz Single-Output Buck Regulator for Server Applications

Figure 10-21 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5 V and rated load current of 15 A. In this example, the target half-load and full-load efficiencies are 93% and 91%, respectively, based on a nominal input voltage of 12 V that ranges from 5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve light-load efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB1 to VDDA.

Note

See the *LM5143-Q1 4-phase Buck Regulator Design for Automotive ADAS Applications* application report for a four-phase, 30-A version of this design.

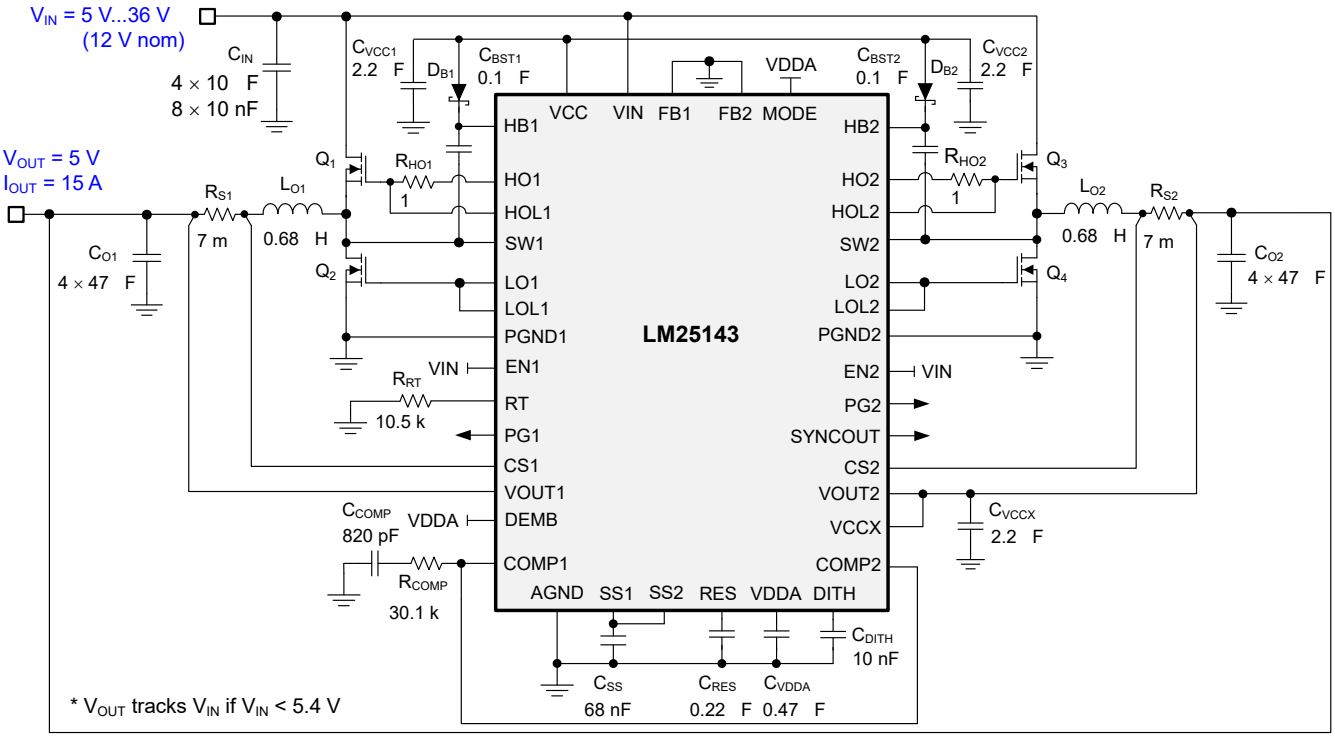


Figure 10-21. Application Circuit 2 With LM25143 Two-Phase Buck Regulator at 2.1 MHz

10.2.2.1 Design Requirements

Table 10-4 shows the intended input, output, and performance parameters for this automotive application design example.

Table 10-4. Design Parameters

Design Parameter	Value
Input voltage range (steady state)	5 V to 18 V
Minimum transient input voltage	5 V
Maximum transient input voltage	36 V
Output voltage	5 V
Output current	15 A
Switching frequency	2.1 MHz
Output voltage regulation	±1%
Shutdown current	4 µA

The switching frequency is set at 2.1 MHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 60 kHz with a phase margin greater than 50°. The output voltage soft-start time is set at 2 ms by a 68-nF soft-start capacitor.

The selected buck regulator powertrain components are cited in Table 10-5, and many of the components are available from multiple vendors. Similar to design 1, this design uses a low-DCR, composite inductor and ceramic output capacitor implementation.

Table 10-5. List of Materials for Application Circuit 2

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMJ325KB7106KMHT
		10 µF, 50 V, X7S, 1210, ceramic	Murata	GCM32EC71H106KA03
			TDK	CGA6P3X7S1H106M
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
			Taiyo Yuden	JMK325B7476KMHTR
		47 µF, 6.3 V, X7S, 1210, ceramic	TDK	CGA6P1X7S0J476M
L_{O1}, L_{O2}	2	0.68 µH, 4.8 mΩ, 25 A, 7.3 × 6.6 × 2.8 mm	Würth Elekronik	744373460068
		0.68 µH, 4.5 mΩ, 22 A, 6.95 × 6.6 × 2.8 mm	Cyntec	VCMV063T-R68MN2T
		0.68 µH, 3.1 mΩ, 20 A, 7 × 6.9 × 3.8 mm	Würth Elekronik	744311068
		0.68 µH, 7.4 mΩ, 12.2 A, 5.4 × 5.0 × 3 mm	TDK	SPM5030VT-R68-D
		0.68 µH, 2.9 mΩ, 15.3 A, 6.7 × 6.5 × 3.1 mm	Coilcraft	XGL6030-681
Q_1, Q_2, Q_3, Q_4	4	40 V, 5.7 mΩ, 9 nC, SON 5 × 6	Infineon	IPC50N04S5L-5R5
R_{S1}, R_{S2}	2	Shunt, 7 mΩ, 0508, 1 W	Susumu	KRL2012E-M-R007
U_1	1	LM25143 42-V dual-channel/phase synchronous buck controller	Texas Instruments	LM25143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.2.2 Detailed Design Procedure

See Section 10.2.1.2.

10.2.2.3 Application Curves

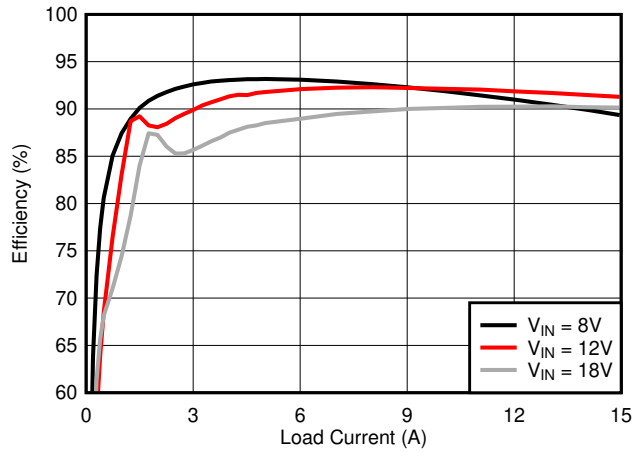
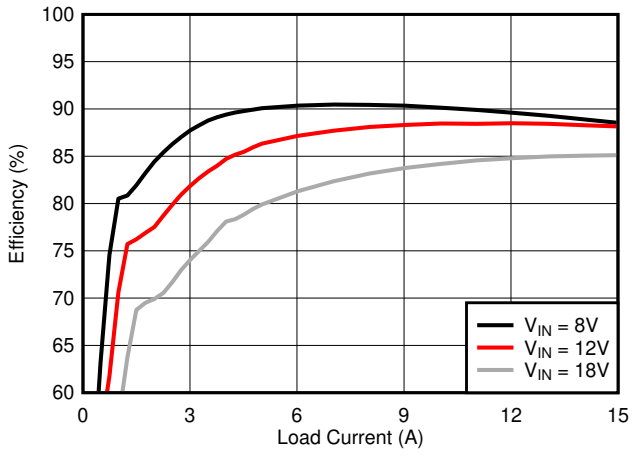


Figure 10-22. Efficiency Versus I_{OUT}, 5-V Output



Configure the regulator as a 3.3-V output by tying FB1 to VDDA.

Figure 10-23. Efficiency Versus I_{OUT}, 3.3-V Output

10.2.3 Design 3 – Two-Phase, 50-A, 300-kHz Single-Output Buck Regulator for ASIC Power Applications

Figure 10-24 shows the schematic diagram of a single-output, two-phase synchronous buck regulator with an output voltage of 5 V. The expected DC load current is 35 A with transients up to 50 A. In this example, the target efficiency at 35 A is 96% using a power stage optimized for a nominal input voltage of 24 V. The switching frequency is set at 300 kHz by resistor R_{RT}, and inductor DCR current sensing is used to mitigate shunt-related losses at high current. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve light-load efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB1 to VDDA.

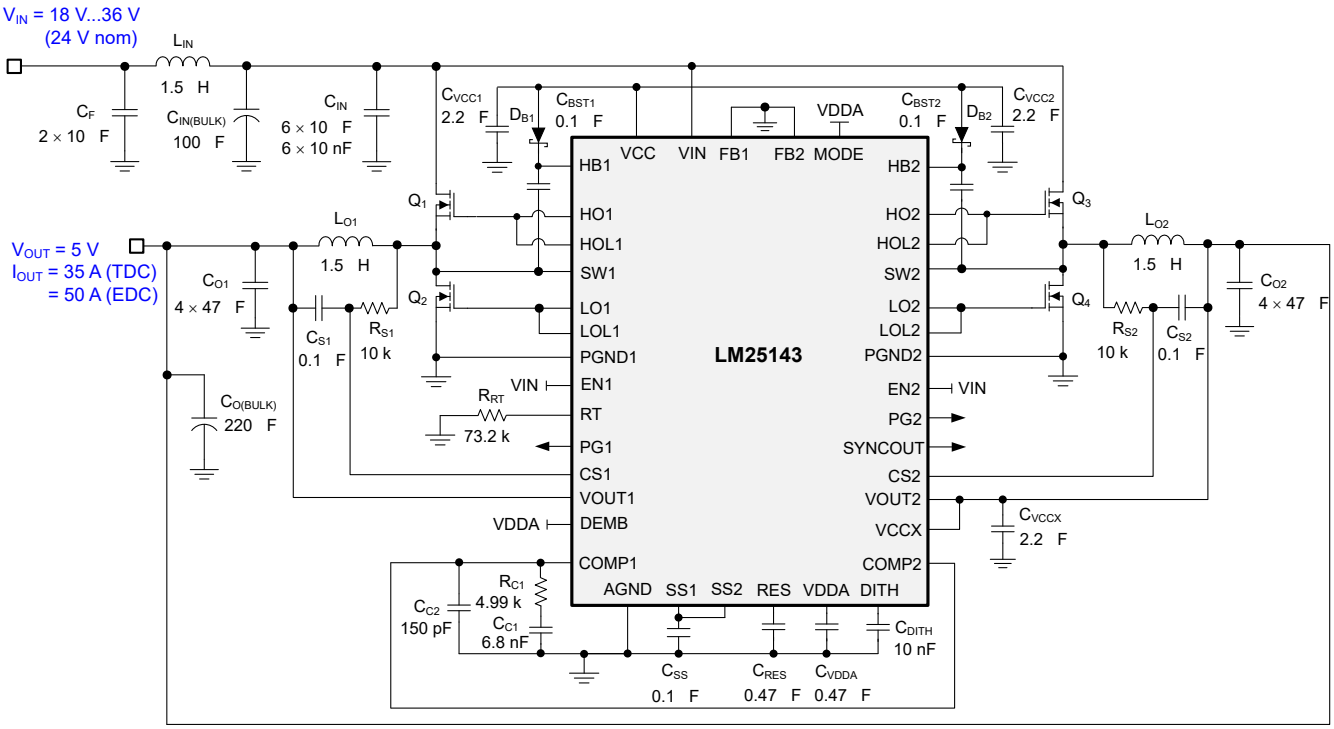


Figure 10-24. Application Circuit 3 With LM25143 Two-Phase Buck Regulator at 300 kHz

10.2.3.1 Design Requirements

Table 10-6 shows the intended input, output, and performance parameters for this design example.

Table 10-6. Design Parameters

Design Parameter	Value
Nominal input voltage	24 V
Input voltage range (steady state)	18 V to 36 V
Output voltage	5 V
Thermal design current (TDC)	35 A
Electrical design current (EDC)	50 A
Switching frequency	300 kHz
Output voltage regulation	±1%
Shutdown current	4 µA

The switching frequency is set at 300 kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 45 kHz with a phase margin greater than 50°. The output voltage soft-start time is set at 3 ms by a 100-nF soft-start capacitor. FPWM operation provides constant switching frequency over the full load current range for predictable EMI performance and optimal load transient response.

The selected buck regulator powertrain components are cited in Table 10-7, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in Section 10.1.1.4. This design uses a low-DCR composite inductor and ceramic output capacitor implementation.

Table 10-7. List of Materials for Application Circuit 3

Ref Des	Qty	Specification	Manufacturer(1)	Part Number
C_{IN}	6	10 µF, 50 V, X7R, 1210, ceramic	TDK	CNA6P1X7R1H106K
			AVX	12105C106K4T2A
		10 µF, 50 V, X7R, 1206, ceramic	TDK	CGA5L1X7R1H106K
C_O	8	47 µF, 6.3 V, X7R, 1210, ceramic	Murata	GCM32ER70J476KE19L
	6	100 µF, 6.3 V, X7S, 1210, ceramic	Murata	GRT32EC70J107ME13L
$C_{O(BULK)}$	1	220 µF, 10 V, 25 mΩ, 7343, polymer tantalum	Kemet	T598D227M010ATE025
			AVX	TCQD227M010R0025E
L_{O1}, L_{O2}	2	1.5 µH, 1.28 mΩ, 46.7 A, 13.3 × 12.8 × 8 mm	Cyntec	VCUD128T-1R5MS8
		1.5 µH, 2.3 mΩ, 35 A, 13.5 × 12.6 × 6.5 mm	Cyntec	VCMV136E-1R5MN2
		1.5 µH, 2.8 mΩ, 32.8 A, 13 × 12.5 × 6.5 mm	TDK	SPM12565VT-1R5M-D
		1.5 µH, 2.3 mΩ, 55.3 A, 13.5 × 12.5 × 6.2 mm	Würth Elektronik	744373965015
Q_1, Q_3	2	60 V, 11 mΩ, 4.5 nC, DFN5	Onsemi	NVMFS5C673NL
Q_2, Q_4	2	60 V, 2.6 mΩ, 24 nC, DFN5	Onsemi	NVMFS5C628NL
U_1	1	LM25143 42-V dual-channel/phase synchronous buck controller	Texas Instruments	LM25143RHAR

(1) See the *Third Party Products Disclaimer*.

10.2.3.2 Detailed Design Procedure

See Section 10.2.1.2.

10.2.3.3 Application Curves

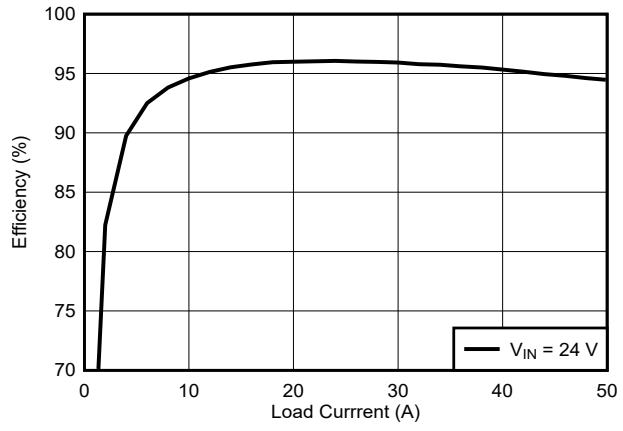


Figure 10-25. Efficiency Versus I_{OUT}

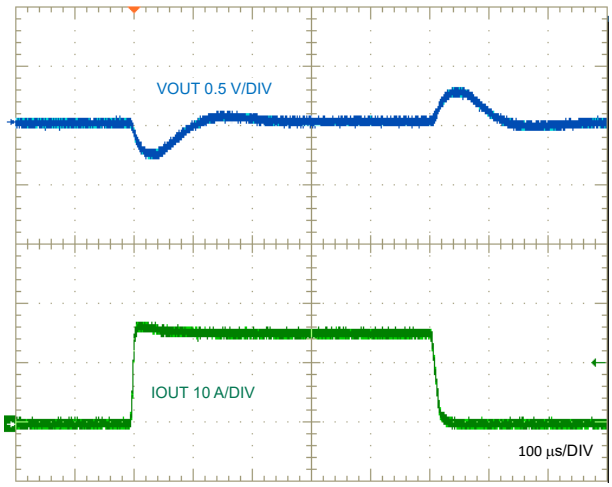


Figure 10-26. Load Transient, 0 A to 15 A

11 Power Supply Recommendations

The LM25143 buck controller is designed to operate over a wide input voltage range of 3.5 V to 42 V. The characteristics of the input supply must be compatible with the *Absolute Maxmimum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Use Equation 46 to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \cdot \eta} \tag{46}$$

where

- η is the efficiency.

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse effect on regulator operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the affects mentioned above. The *Simple Success with Conducted EMI for DC-DC Converters Application Report* provides helpful suggestions when designing an input filter for any switching regulator.

12 Layout

12.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain issues must be considered before designing a PCB layout using the LM25143. The high-frequency power loop of a buck regulator power stage is denoted by loop 1 in the shaded area of Figure 12-1. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3, respectively, in Figure 12-1.

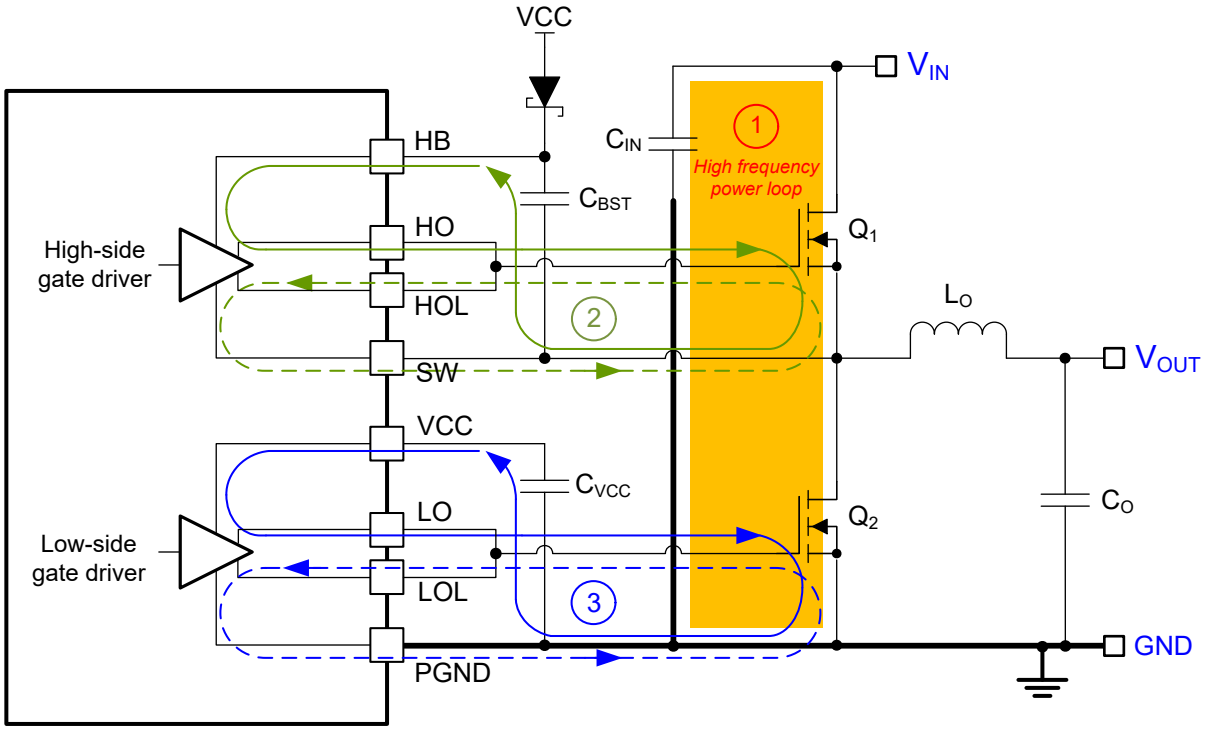


Figure 12-1. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

12.1.1 Power Stage Layout

- Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
- The DC/DC regulator has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and optimize switching performance.
  - Loop 1: The most important loop area to minimize is the path from the input capacitor or capacitors through the high-side and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop 1 in Figure 12-1.
  - Another loop, not as critical as loop 1, is the path from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.

- The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
- Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
- The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 in Figure 12-1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (greater than 50 MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

12.1.2 Gate-Drive Layout

The LM25143 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 2: high-side MOSFET, Q_1. During the high-side MOSFET turn-on, high current flows from the bootstrap (boot) capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop 2 of Figure 12-1.
- Loop 3: low-side MOSFET, Q_2. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop 3 of Figure 12-1.

TI strongly recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO1/2, HOL1/2, LO1/2, and LOL1/2 to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as 4.25 A. Use 0.65-mm (25 mils) or wider traces. Use via or vias, if necessary, of at least 0.5-mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LM25143 to the high-side MOSFET, taking advantage of flux cancellation.
- Minimize the current loop path from the VCC and HB pins through their respective capacitors as these provide the high instantaneous current, up to 4.25 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the HB and SW pins of the LM25143 to minimize the area of loop 2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM25143 to minimize the area of loop 3 associated with the low-side driver.

12.1.3 PWM Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP1/2, FB1/2, CS1/2, SS1/2, RES, and RT away from high-voltage switching nodes such as SW1/2, HO1/2, LO1/2, or HB1/2 to avoid mutual coupling.

Use internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Locate the upper and lower feedback resistors (if required) close to the respective FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the required output voltage sense point or points at the load or loads.
- Route the CS1/2 and VOUT1/2 traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor (if shunt current sensing is used) or to the sense capacitor (if inductor DCR current sensing is used).
- Minimize the loop area from the VCC1/2 and VIN pins through their respective decoupling capacitors to the relevant PGND pins. Locate these capacitors as close as possible to the LM25143.

12.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM25143 controller is available in a small 6-mm × 6-mm 40-pin VQFN (RHA) PowerPAD package to cover a range of application requirements. The summarizes the thermal metrics of this package.

The 40-pin VQFNP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LM25143 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LM25143 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multilayer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the respective SW planes, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

12.1.5 Ground Plane Design

As mentioned previously, using one or more of the inner PCB layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND1 and PGND2 pins to the system ground plane using an array of vias under the exposed pad. Also connect the PGND1 and PGND2 pins directly to the return terminals of the input and output capacitors. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND1/2, VIN and SW1/2 can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

12.2 Layout Example

Based on the *LM5143-Q1EVM-2100* design, Figure 12-2 shows a single-sided layout of a dual-output synchronous buck regulator. Each power stage is surrounded by a GND pad geometry to connect an EMI shield if needed. The design uses layer 2 of the PCB as a power-loop return path directly underneath the top layer to create a low-area switching power loop of approximately 2 mm². This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing. Refer to the *LM5143-Q1EVM-2100 Evaluation Module User's Guide* for more detail.

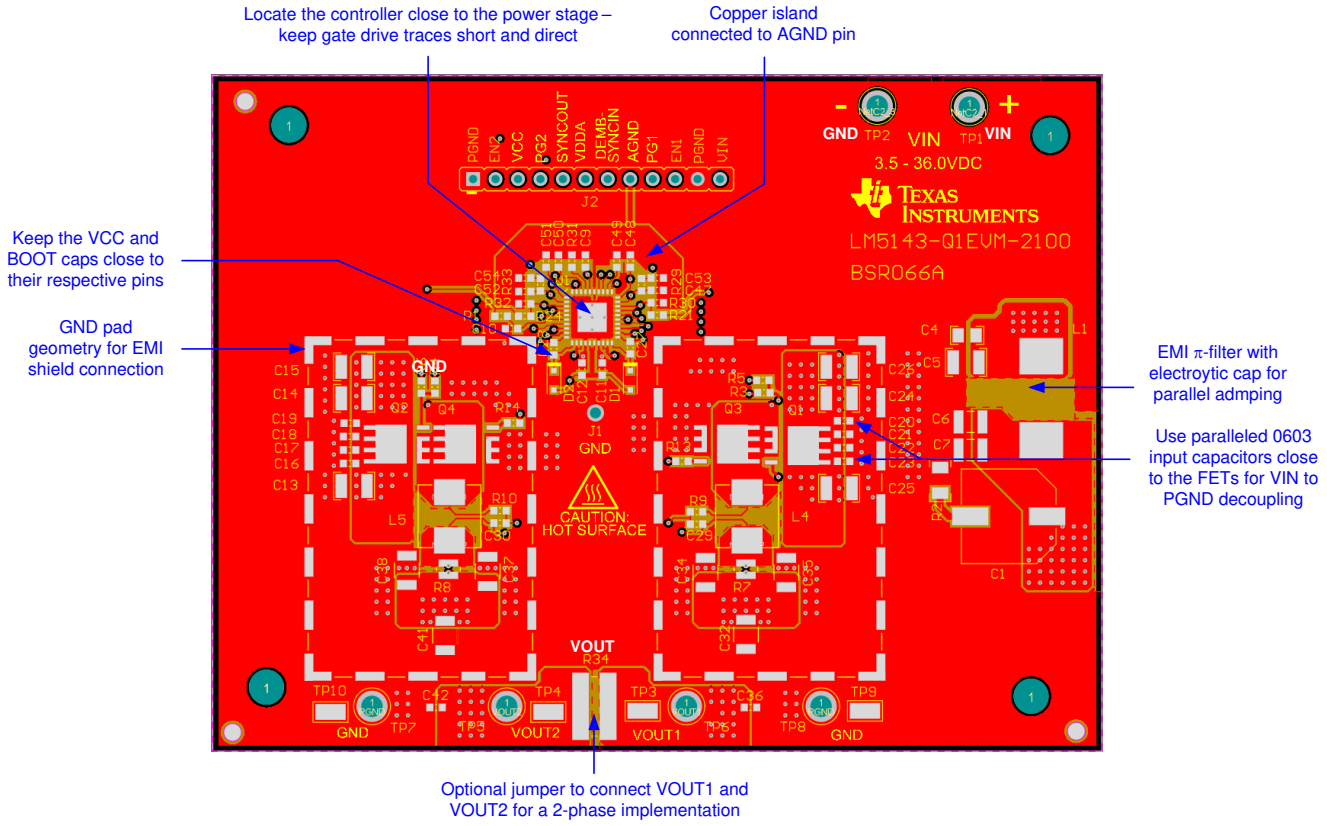


Figure 12-2. PCB Top Layer

As shown in Figure 12-3, the high-frequency power loop current of one channel flows through MOSFETs Q2 and Q4, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C16 through C19. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic inductance. Figure 12-4 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in Figure 12-3, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q2.

Four 10-nF input capacitors with small 0402 or 0603 case size are placed in parallel very close to the drain of each high-side MOSFET. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the layer-2 GND plane with multiple 12-mil (0.3-mm) diameter vias, further minimizing parasitic loop inductance.

Additional steps used in this layout example include:

- Keep the SW connection from the power MOSFETs to the inductor (for each channel) at minimum copper area to reduce radiated EMI.
- Locate the controller close to the gate terminals of the MOSFETs such that the gate drive traces are routed short and direct.

- Create an analog ground plane near the controller for sensitive analog components. The analog ground plane for AGND and power ground planes for PGND1 and PGND2 must be connected at a single point directly under the IC – at the die attach pad (DAP).

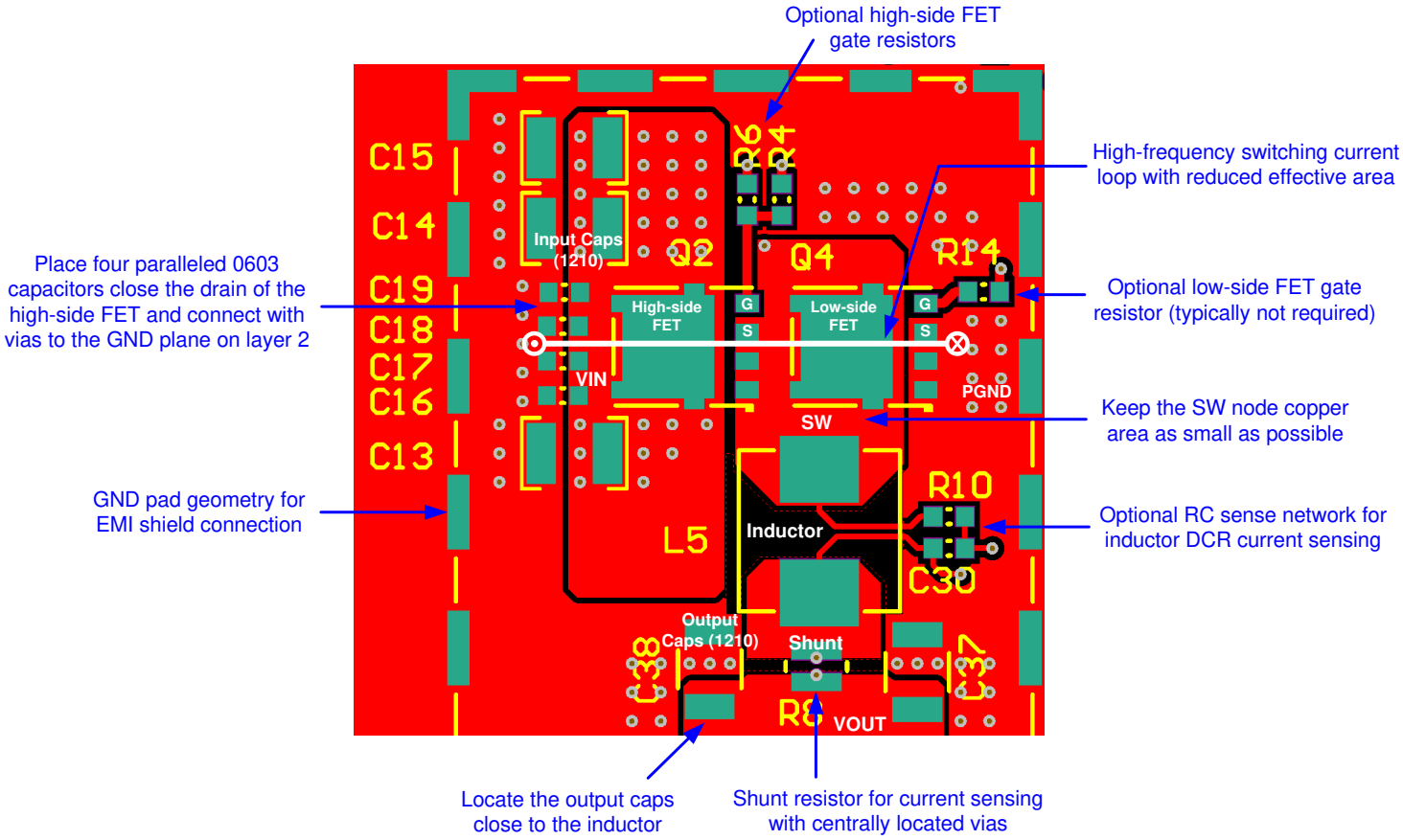
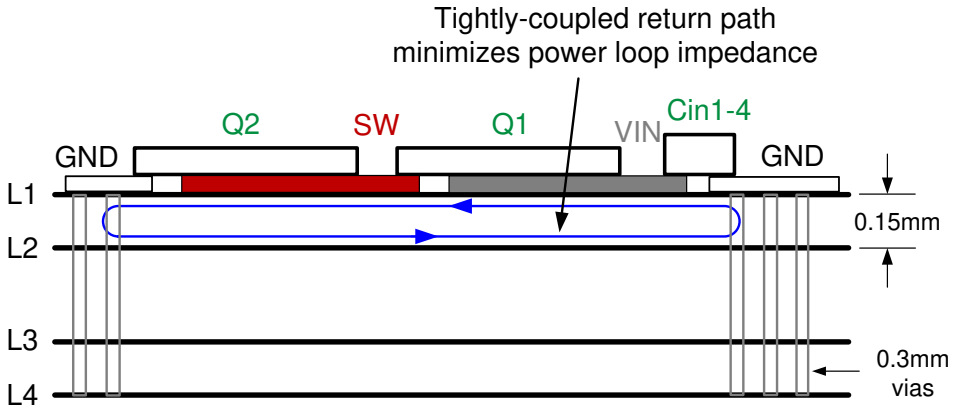


Figure 12-3. Power Stage Component Layout



Note

See the *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* application report for more detail.

Figure 12-4. PCB Stack-up Diagram With Low L1-L2 Intra-layer Spacing

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.1.2 Development Support

With an input operating voltage as low as 3.5 V and up to 100 V as specified in Table 13-1, the LM(2)514x family of synchronous buck controllers from TI provides scalability and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF).

Table 13-1. Synchronous Buck DC/DC Controller Family

DC/DC Controller	Single or Dual	V_{IN} Range	Control Method	Gate Drive Voltage	Sync Output	EMI Mitigation
LM25141	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM25143	Dual	3.5 V to 42 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM25145	Single	6 V to 42 V	Voltage mode	7.5 V	180° phase shift	N/A
LM25148	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS
LM25149	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS, AEF
LM5141	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM5145	Single	6 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5146	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5148	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS
LM5149	Single	3.5 V to 80 V	Peak current mode	5 V	180° phase shift	DRSS, AEF

For development support, see the following:

- *LM25143 Quickstart Calculator*
- *LM25143 Simulation Models*
- *TI Reference Design Library*
- *WEBENCH® Design Center*
- To design a low-EMI power supply, review TI's comprehensive EMI Training Series
- TI Designs:
  - *Automotive wide V_{IN} front-end reference design for digital cockpit processing units*
- Technical Articles:
  - *High-density PCB layout of DC/DC converters*
  - *Synchronous buck controller solutions support wide V_{IN} performance and flexibility*
  - *How to use slew rate for EMI control*
  - *How to reduce EMI and shrink power-supply size with an integrated active EMI filter*

13.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25143 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- User's Guides:
  - *LM5143-Q1 Synchronous Buck Controller EVM*
  - *LM5140-Q1 Synchronous Buck Controller High Density EVM*
  - *LM5141-Q1 Synchronous Buck Controller EVM*
  - *LM5146-Q1 EVM User's Guide*
  - *LM5145 EVM User's Guide*
- Application Reports:
  - *LM5143-Q1 Synchronous Buck Controller High-Density 4-Phase Design*
  - *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  - *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Technical Briefs:
  - *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
  - *EMI Filter Components And Their Nonidealities For Automotive DC/DC Regulators*
- White Papers:
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*
- E-Book:
  - *An Engineer's Guide To EMI In DC/DC Regulators*

13.2.1.1 PCB Layout Resources

- Application Reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - *AN-1149 Layout Guidelines for Switching Power Supplies*
  - *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - *Constructing Your Power Supply – Layout Considerations*

13.2.1.2 Thermal Design Resources

- Application Reports:
  - *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - *Semiconductor and IC Package Thermal Metrics*
  - *Thermal Design Made Simple with LM43603 and LM43602*
  - *PowerPAD™ Thermally Enhanced Package*
  - *PowerPAD Made Easy*
  - *Using New Thermal Metrics*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
PowerPAD™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
is a registered trademark of TI.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

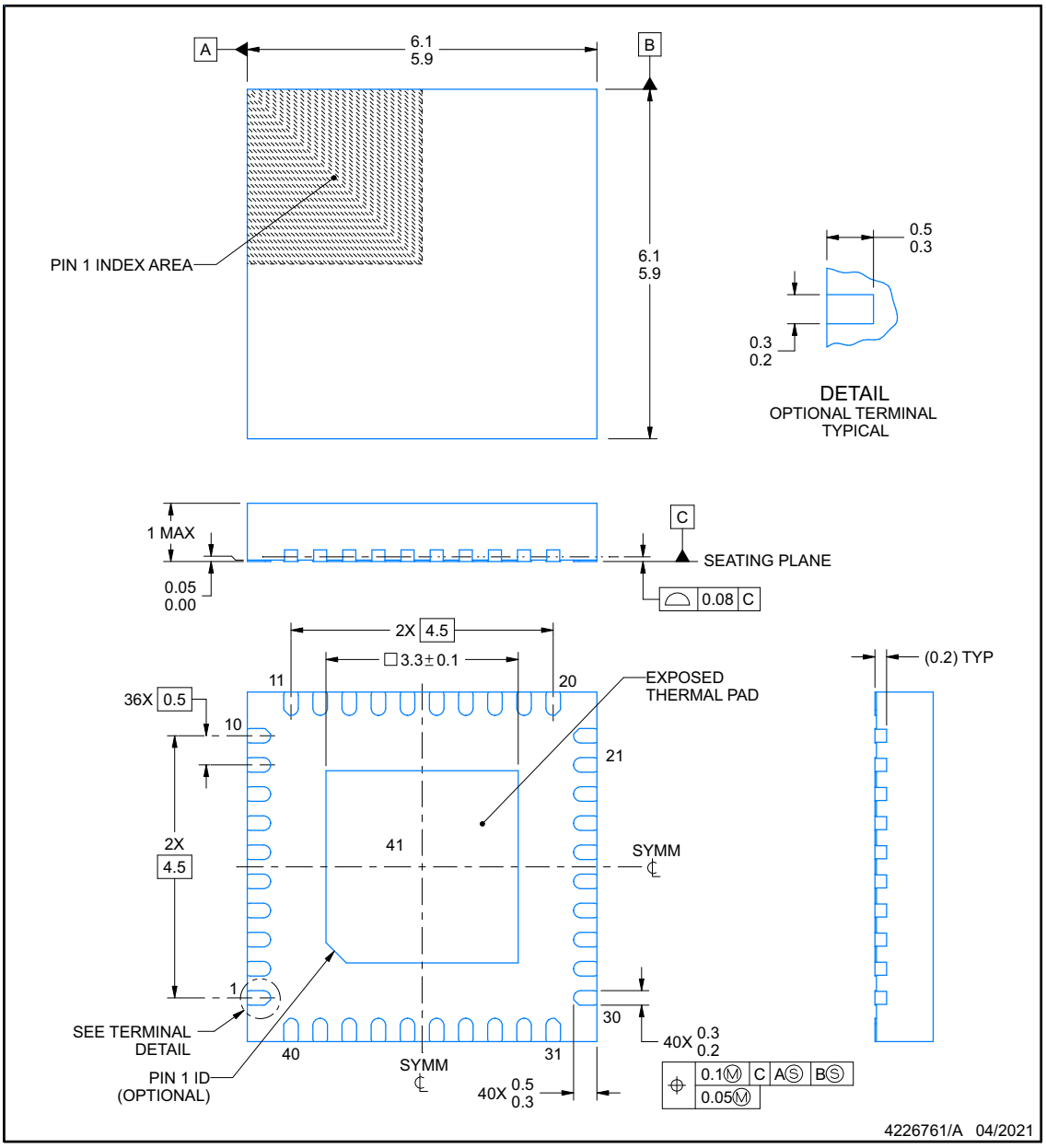
The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

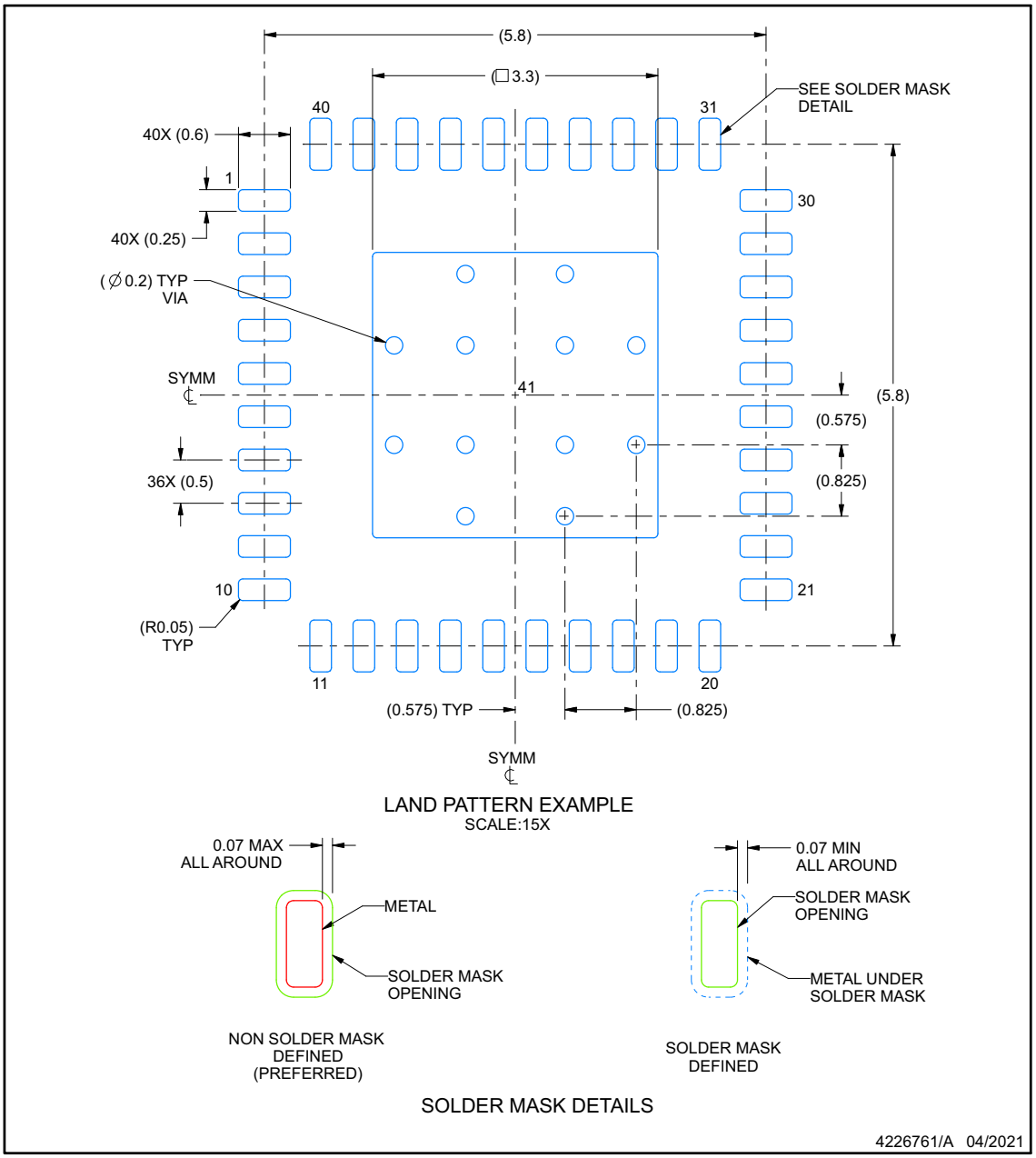
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



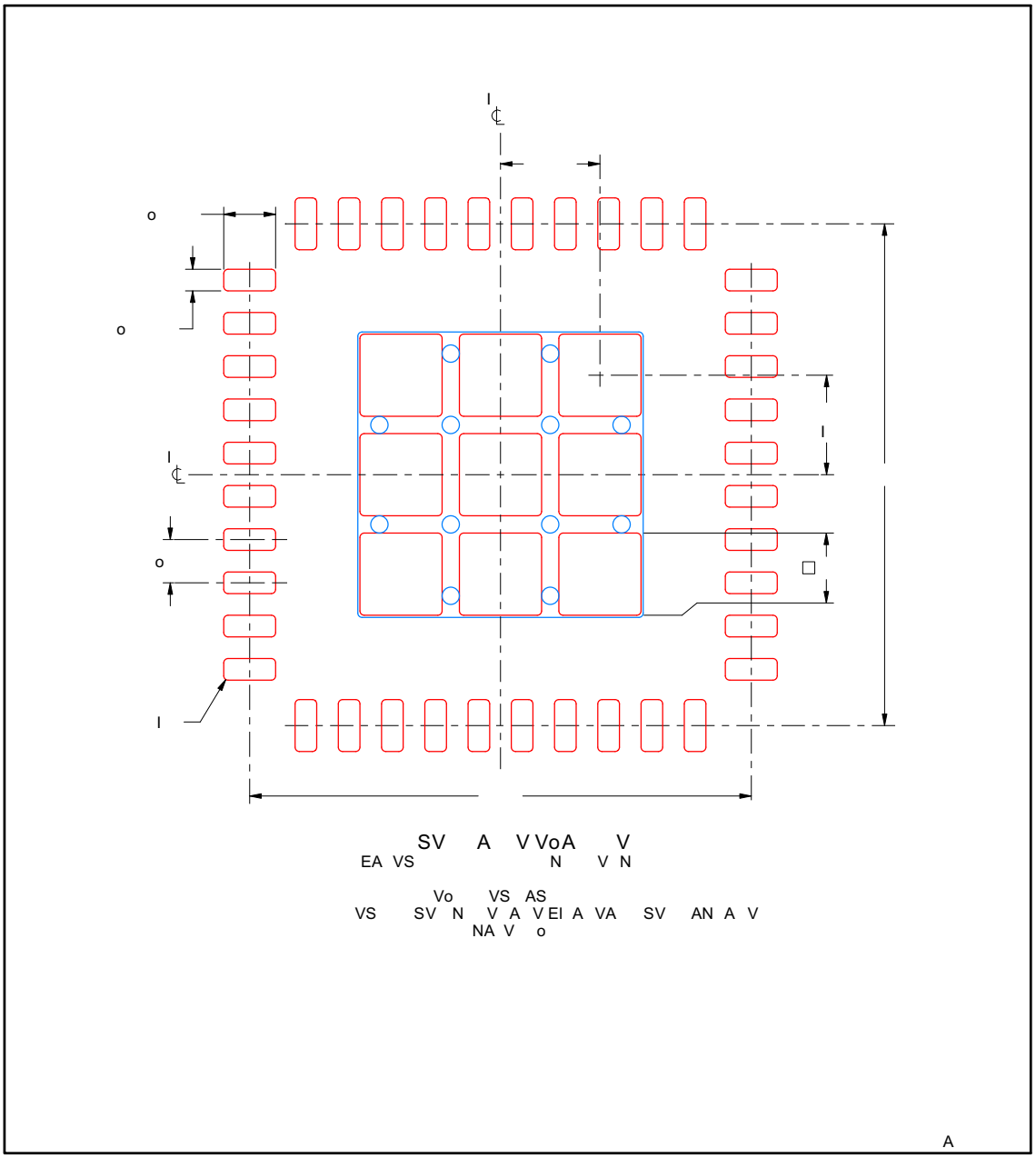
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.

EXAMPLE STENCIL DESIGN

RHA0040P — **VQFN - 1 mm max height**

A N AS 2 A AN VAS



SV A V VoA V
EA VS N V N

Vo VS AS
VS SV N V A V EI A VA SV AN A V
NA V o

A

V rB B

1 B R 1 1 1 R r B 1r B r1B 1 r 1 1R 1 N 1B
B1 r B rB

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25143RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	LM25143R HAR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

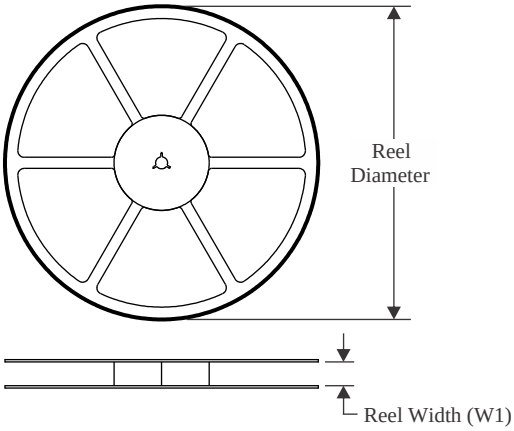
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

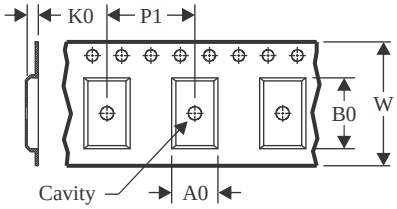
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

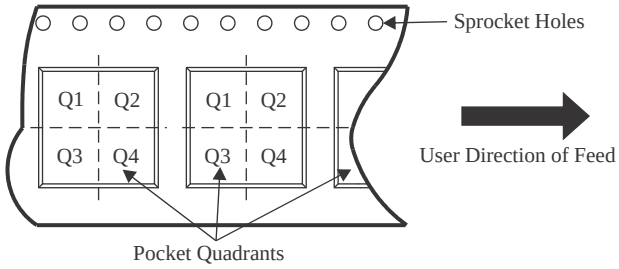


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

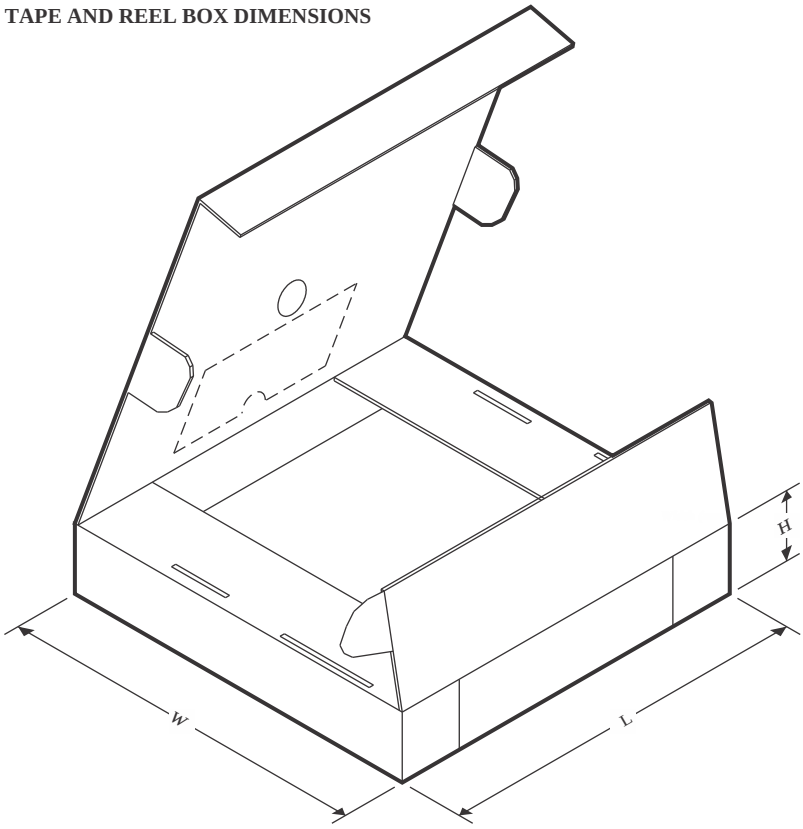
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25143RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25143RHAR	VQFN	RHA	40	2500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

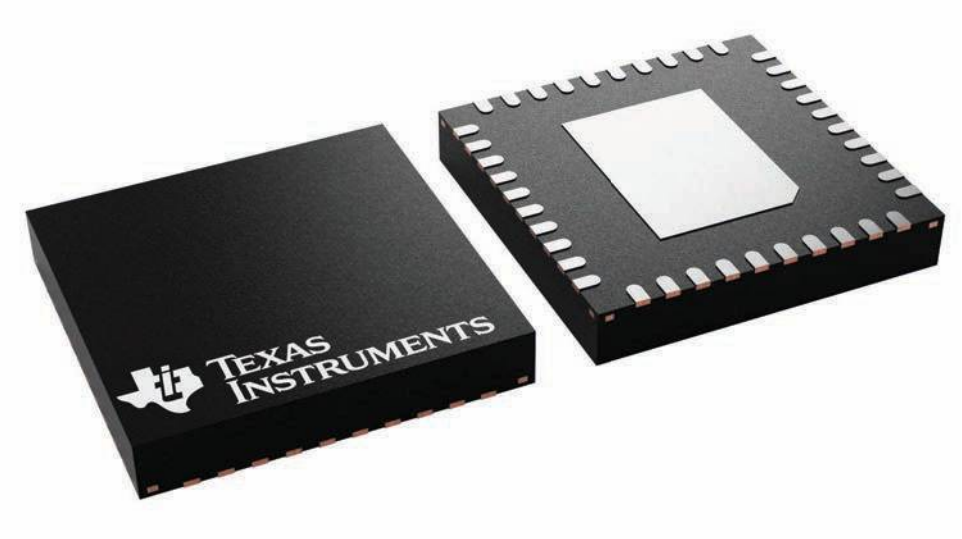
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



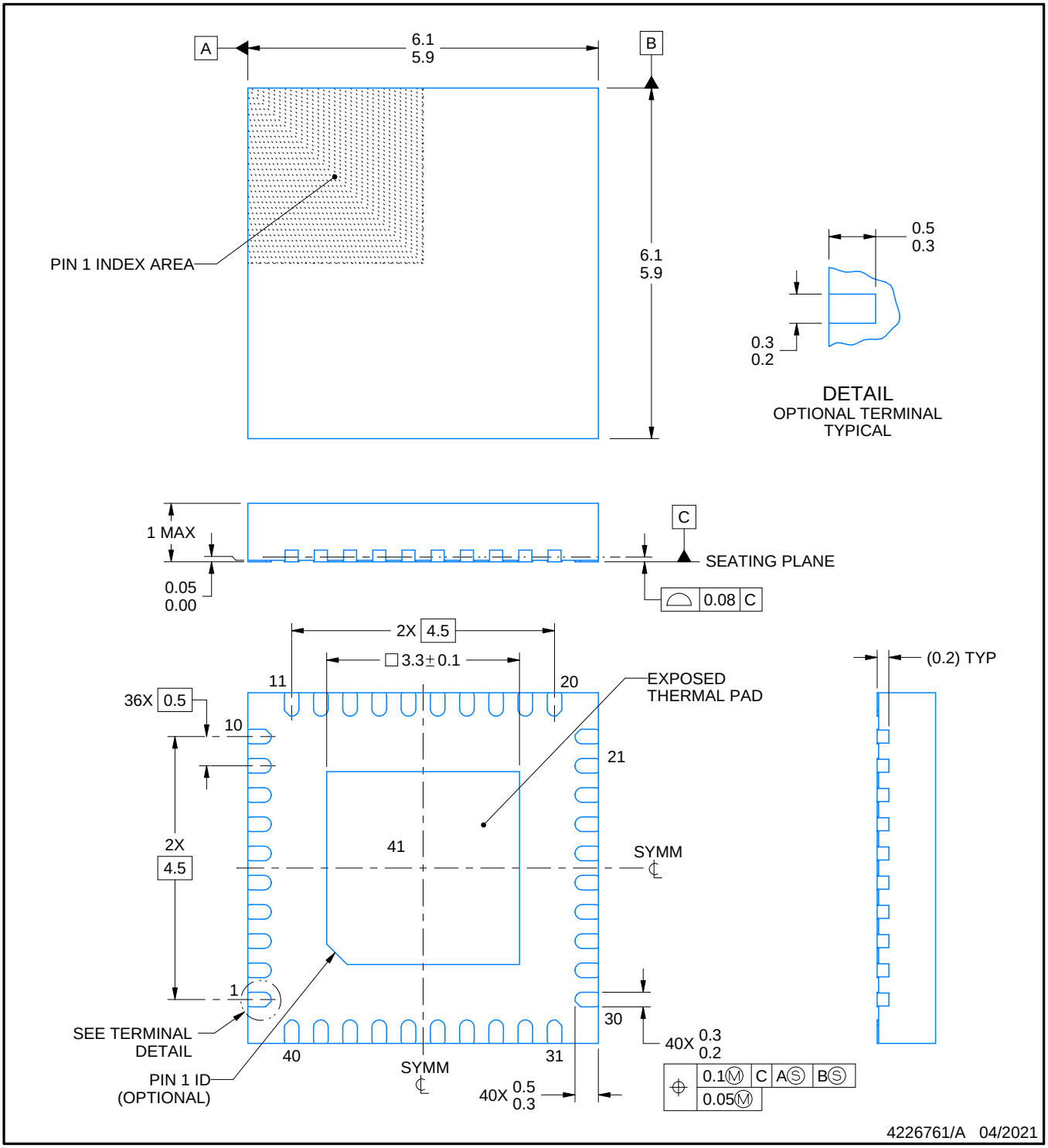
4225870/A

PACKAGE OUTLINE

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

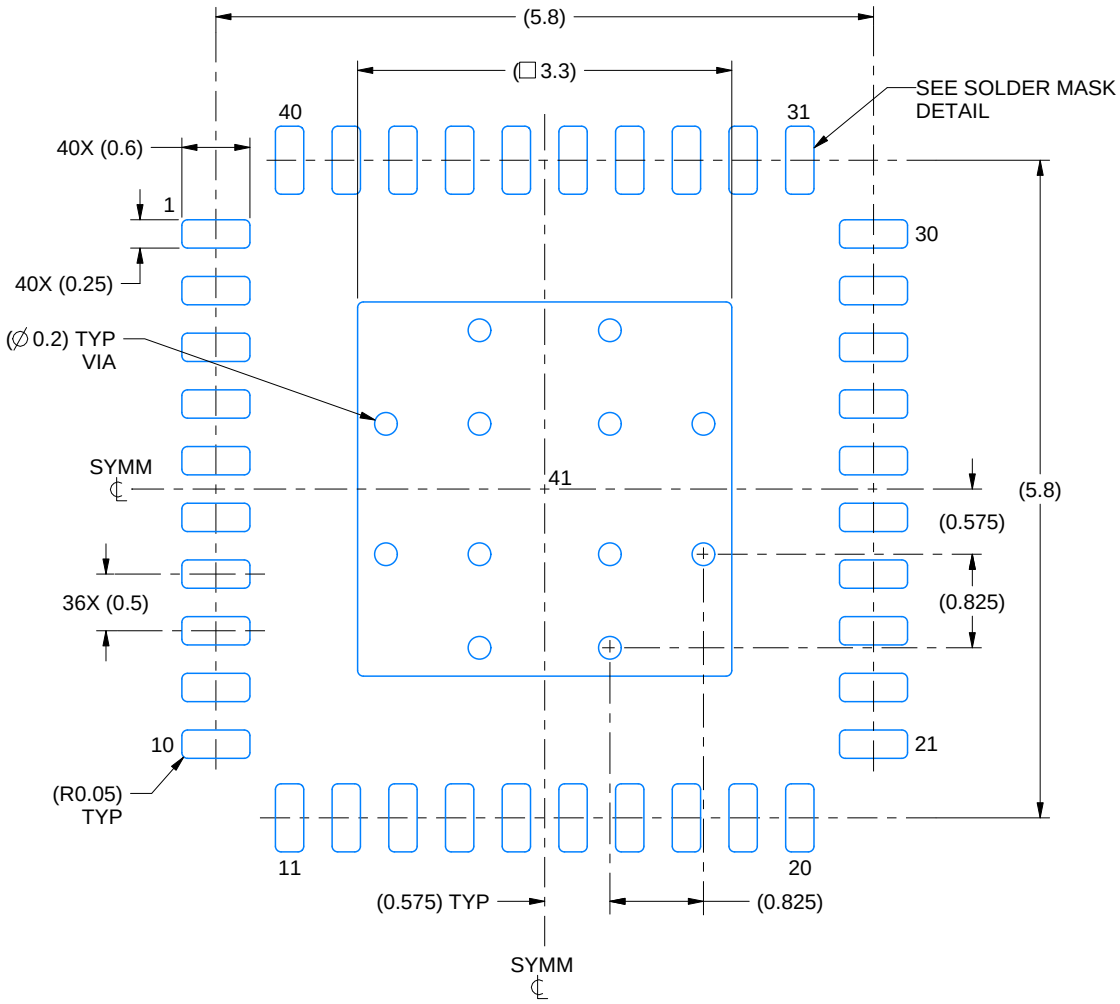
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0040P

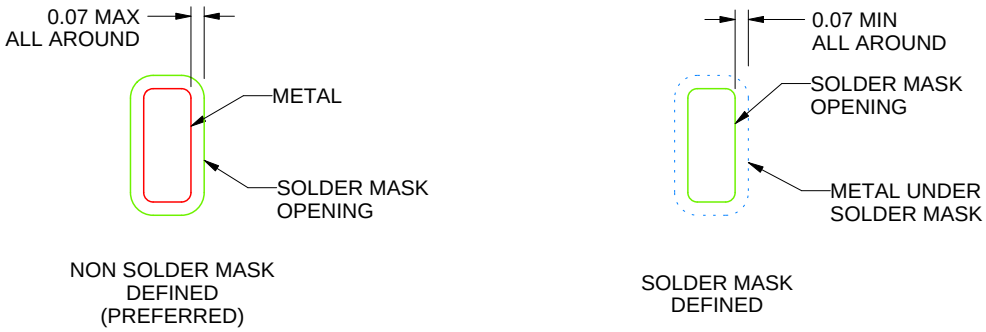
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

SCALE:15X

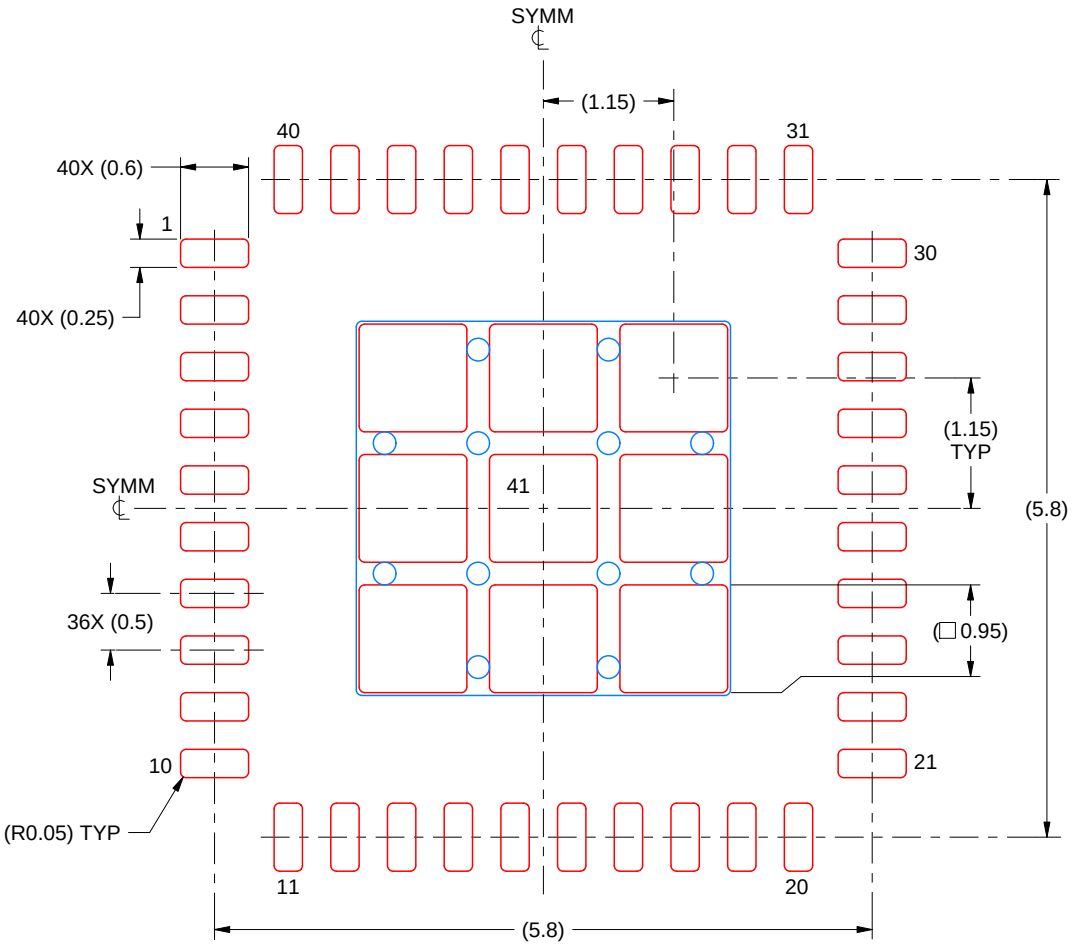


SOLDER MASK DETAILS

4226761/A 04/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
78.25% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4226761/A 04/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
LM74502, LM74502H
SNOSDE5A – DECEMBER 2021 – REVISED MAY 2022

LM74502, LM74502H Low IQ High Side Switch Controller with Reverse Polarity and Overvoltage Protection

1 Features

- 3.2-V to 65-V input range (3.9-V start-up)
- –65-V input reverse voltage rating
- Integrated charge pump to drive
  - External back-to-back N-Channel MOSFETs
  - External high side switch MOSFET
  - External reverse polarity protection MOSFET
- Gate drive variants
  - LM74502: 60-µA peak gate drive source capacity
  - LM74502H: 11-mA peak gate drive source capacity
- 2.3-A peak gate sink current capacity
- Enable pin feature
- 45-µA typical operating quiescent current (EN/UVLO = High)
- 1-µA shutdown current (EN/UVLO = Low)
- Adjustable overvoltage and undervoltage protection
- –40°C to +125°C ambient operating temperature range
- Available in 8-pin SOT-23 package 2.90 mm × 1.60 mm

2 Applications

- Factory automation and control – PLC digital output modules
- Industrial motor drives
- Industrial transport
- Power supply reverse polarity protection

3 Description

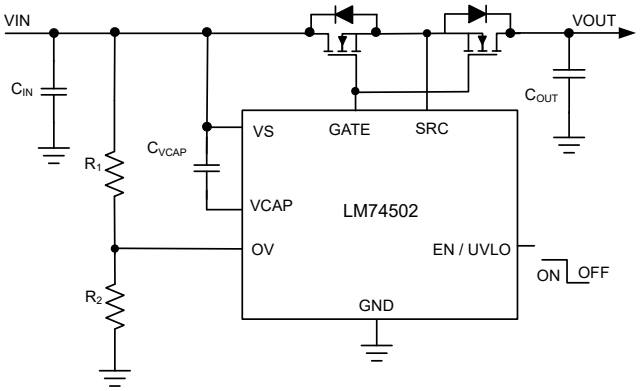
The LM74502, LM74502H is a controller which operates in conjunction with an external back-to-back connected N-channel MOSFETs to realize a low loss reverse polarity protection and load disconnect solution. The device can also be configured to drive high side MOSFET as a load switch with overvoltage protection . The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V, 24-V and 48-V input systems. The device can withstand and protect the loads from negative supply voltages down to –65 V. The LM74502, LM74502H does not have reverse current blocking and is suitable for input reverse polarity protection only.

The LM74502 controller provides a charge pump gate drive for an external N-channel MOSFET. with the enable pin low, the controller is off and draws approximately 1 µA of current, thus offering low system current when put into sleep mode. LM74502 and LM74502H offers programmable overvoltage and undervoltage protection which cuts off the load from the input source in case of these fault events. The devices are available in a 2.9 mm × 1.6 mm 8-pin DDF package and are specified over a –40°C to +125°C temperature range.

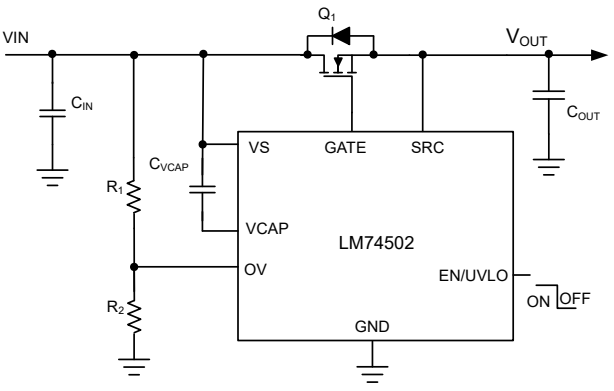
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74502	SOT-23 (8)	2.90 mm × 1.60 mm
LM74502H		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LM74502 Typical Application Schematic



LM74502 as a Load Switch Controller with Overvoltage Protection

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (May 2022)	Page
• Removed the product preview note from LM74502H throughout the document	1
• Updated document title	1
• Added LM74502H to the *Pin Configuration and Functions* section	3

5 Pin Configuration and Functions

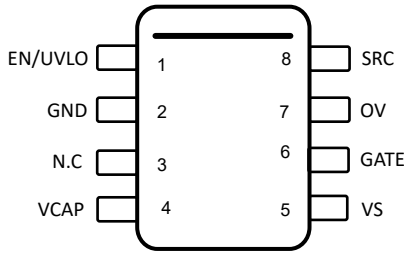


Figure 5-1. DDF Package 8-Pin SOT-23 LM74502, LM74502H Top View

Table 5-1. LM74502, LM74502H Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	EN/UVLO Input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling the pin low below $V_{(ENF)}$ makes the device enter into low Iq shutdown mode. For UVLO, connect an external resistor ladder from input supply to EN/UVLO to ground.
2	GND	G	Ground pin
3	N.C	—	No connection
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	VS	I	Input power supply pin to the controller. Connect a 100-nF capacitor across VS and GND pins.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	OV	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply to OV pin to ground. When the voltage at OV pin exceeds the overvoltage cutoff threshold then the GATE is pulled low. GATE turns ON when the OV pin voltage goes below the OVP falling threshold. Connect OV pin to ground when OV feature is not used.
8	SRC	I	Source pin. Connect to common source point of external back-to-back connected N-channel MOSFETs or the source pin of the high side switch MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS to GND	–65	65	V
	EN/UVLO, OV to GND, $V_{(VS)}$ > 0 V	–0.3	65	V
	EN/UVLO, OV, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(65 + $V_{(VS)}$)	
	SRC to GND, $V_{(VS)}$ ≤ 0 V		($V_{(VS)}$ + 0.3)	V
	SRC to GND, $V_{(VS)}$ > 0 V	–(70 – $V_{(VS)}$)	$V_{(VS)}$	V
Output Pins	GATE to SRC	0	15	V
	VCAP to VS	–0.3	15	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS to GND	–60		60	V
	EN/UVLO, OV, SRC to GND	–60		60	
External capacitance	VS	22			nF
	VCAP to VS	0.1			µF
External MOSFET max V_{GS} rating	GATE to SRC	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *electrical characteristics*
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM74502 LM74502H DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		4		60	V
$V_{(VS\_POR)}$	VS POR Rising threshold				3.9	V
	VS POR Falling threshold		2.2	2.8	3.1	V
$V_{(VS\ POR(Hys))}$	VS POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN/UVLO)}$ = 0 V		0.9	1.5	µA
$I_{(Q)}$	Operating Quiescent Current	I_{GND}		45	65	µA
$I_{(REV)}$	VS pin leakage current during input reverse polarity	0 V ≤ $V_{(VS)}$ ≤ – 65 V		100	150	µA
ENABLE INPUT						
$V_{(EN\_UVLOF)}$	Enable/UVLO falling threshold		1.027	1.14	1.235	V
$V_{(EN\_UVLOR)}$	Enable/UVLO rising threshold		1.16	1.24	1.32	
$V_{(ENF)}$	Enable threshold voltage for low I_Q shutdown		0.32	0.64	0.94	V
$V_{(EN\_Hys)}$	Enable Hysteresis		38	90	132	mV
$I_{(EN/UVLO)}$	Enable sink current	$V_{(EN/UVLO)}$ = 12 V		3	5	µA
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(GATE)} – V_{(SRC)}$ = 5 V	40	60	77	µA
$I_{(GATE)}$	Peak source current	$V_{(GATE)} – V_{(SRC)}$ = 5 V, LM74502H	3	11		mA
	Peak sink current	EN= High to Low $V_{(GATE)} – V_{(SRC)}$ = 5 V		2370		mA
RDS_{ON}	discharge switch RDS_{ON}	EN = High to Low $V_{(GATE)} – V_{(SRC)}$ = 100 mV	0.4		2	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} – V_{(VS)}$ = 7 V	162	300	600	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} – V_{(VS)}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(VS)}$	Charge pump voltage at $V_{(VS)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA	8			V
$V_{(VCAP)} – V_{(VS)}$	Charge pump turn on voltage		10.3	11.6	13	V
$V_{(VCAP)} – V_{(VS)}$	Charge pump turn off voltage		11	12.4	13.9	V
$V_{(VCAP)} – V_{(VS)}$	Charge Pump Enable comparator Hysteresis		0.45	0.8	1.25	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(S)}$ UV release at rising edge		5.7	6.5	7.5	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(S)}$ UV threshold at falling edge		5.05	5.4	6.2	V
OVERVOLTAGE PROTECTION						
$V_{(OVR)}$	Overvoltage threshold input, rising		1.165	1.25	1.333	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.063	1.143	1.222	V
$V_{(OV\_Hys)}$	OV Hysteresis			100		mV
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 5 V	12	50	110	nA

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN/UVLO)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	EN high to Gate Turn On delay	$V_{(VCAP)}$ > $V_{(VCAP\ UVLOR)}$, $V_{(EN/UVLO)}$ > $V_{(EN\_UVLOR)}$ to $V_{(GATE-SRC)}$ > 5 V, $C_{(GATE-SRC)}$ = 4.7 nF LM74502H		75	110	µs
$t_{UVLO\_OFF(deg)\_GATE}$	GATE Turnoff delay during EN/UVLO	$V_{(EN/UVLO)}$ ↓ to $V_{(GATE-SRC)}$ < 1 V, $C_{(GATE-SRC)}$ = 4.7 nF		2		µs
$t_{OVP\_OFF(deg)\_GATE}$	GATE Turnoff delay during OV	$V_{(OV)}$ ↑ to $V_{(GATE-SRC)}$ < 1 V, $C_{(GATE-SRC)}$ = 4.7 nF		0.6	1	µs
$t_{OVP\_ON(deg)\_GATE}$	GATE Turnon delay during OV	$V_{(OV)}$ ↓ to $V_{(GATE-SRC)}$ > 5 V, $C_{(GATE-SRC)}$ = 4.7 nF LM74502H		5	10	µs

6.7 Typical Characteristics

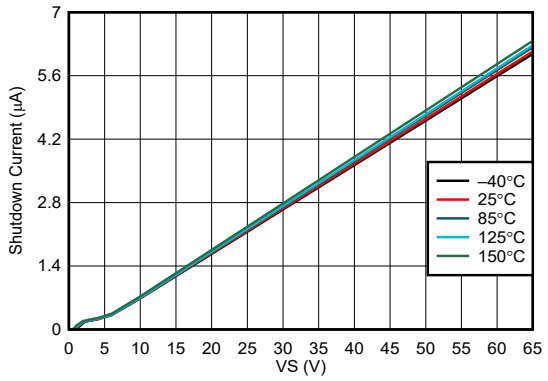


Figure 6-1. Shutdown Supply Current vs Supply Voltage

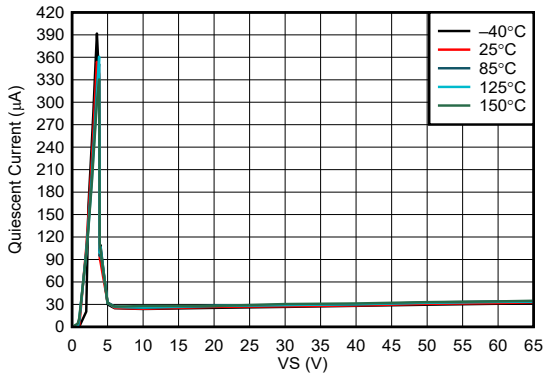


Figure 6-2. Operating Quiescent Current vs Supply Voltage

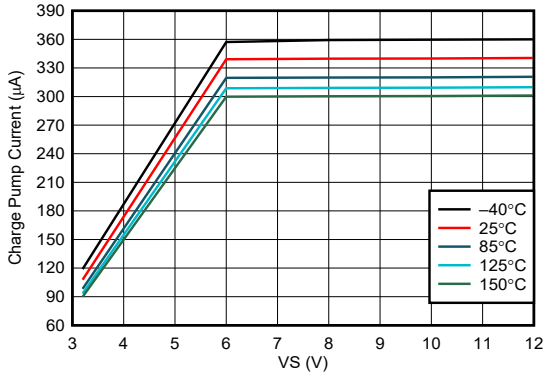


Figure 6-3. Charge Pump Current vs Supply Voltage at V_{CAP} = 6 V

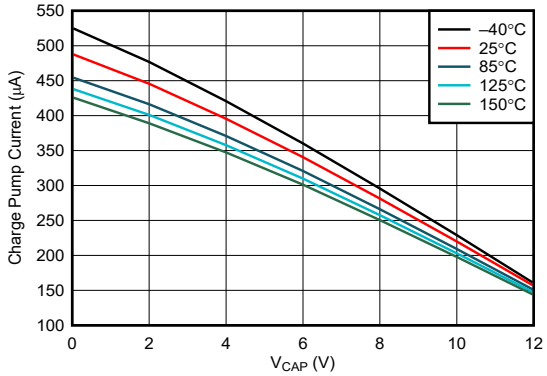


Figure 6-4. Charge Pump V-I Characteristics at VS > = 12 V

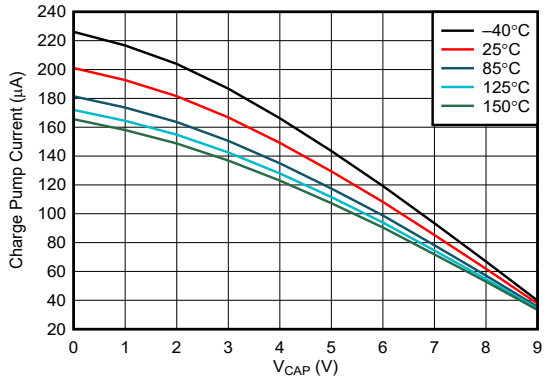


Figure 6-5. Charge Pump V-I Characteristics at VS = 3.2 V

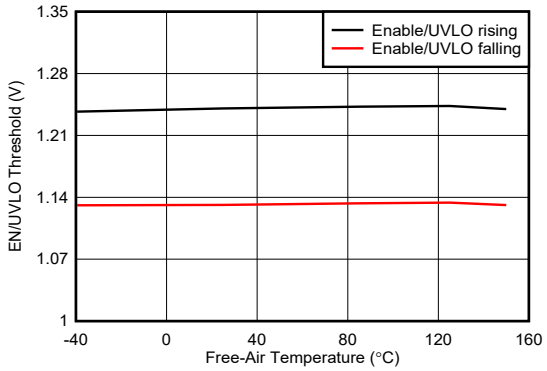


Figure 6-6. EN/UVLO Rising and Falling threshold vs Temperature

6.7 Typical Characteristics (continued)

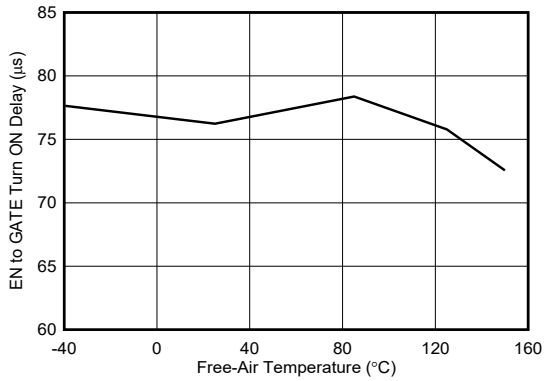


Figure 6-7. Enable to Gate Delay vs Temperature (LM74502H-Q1)

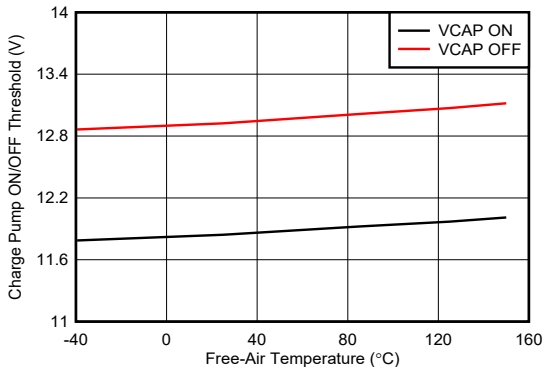


Figure 6-8. Charge Pump ON and OFF Threshold vs Temperature

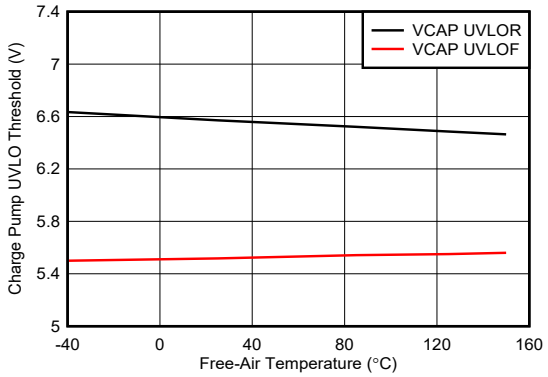


Figure 6-9. Charge Pump UVLO Threshold vs Temperature

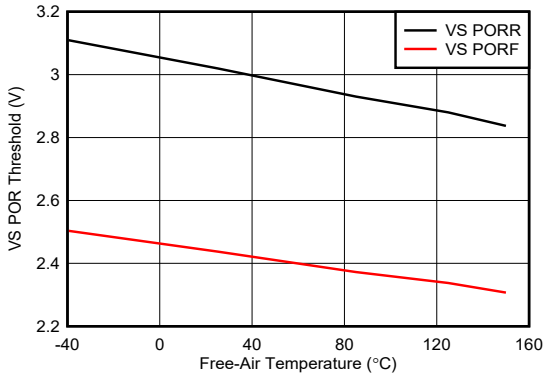


Figure 6-10. VS POR Threshold vs Temperature

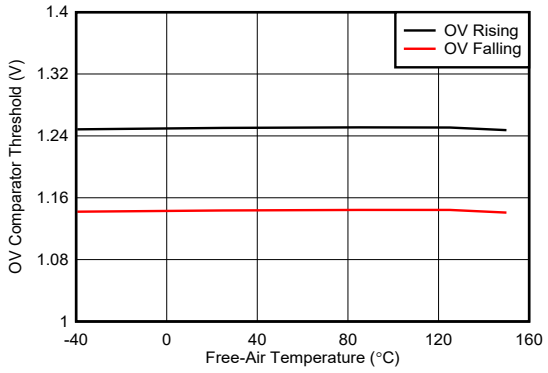


Figure 6-11. OV Comparator Threshold vs Temperature

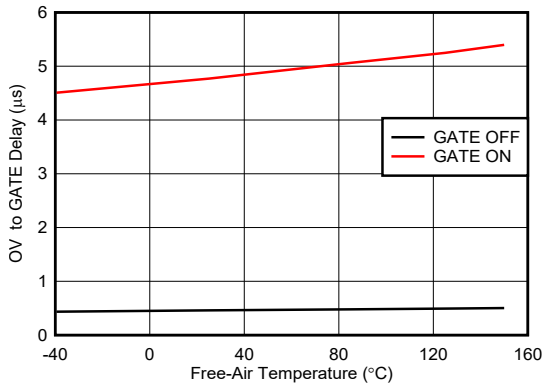


Figure 6-12. OV to GATE Delay vs Temperature (LM74502H-Q1)

7 Parameter Measurement Information

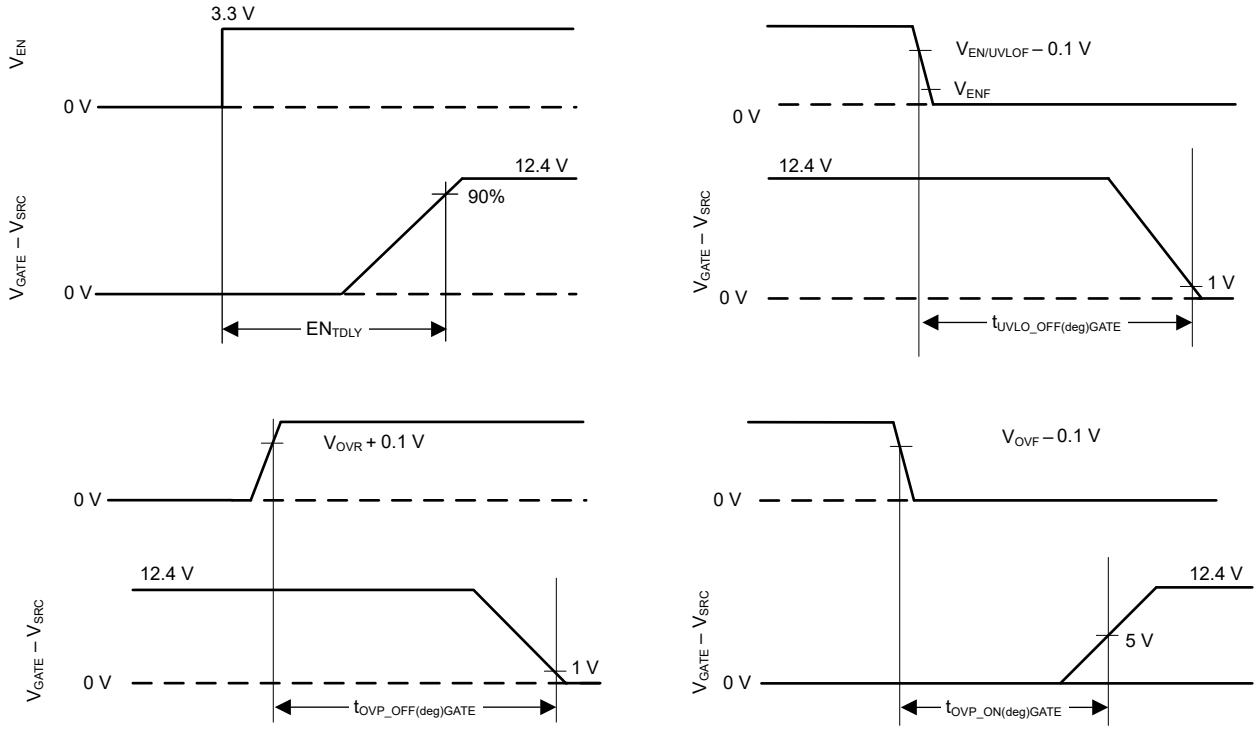


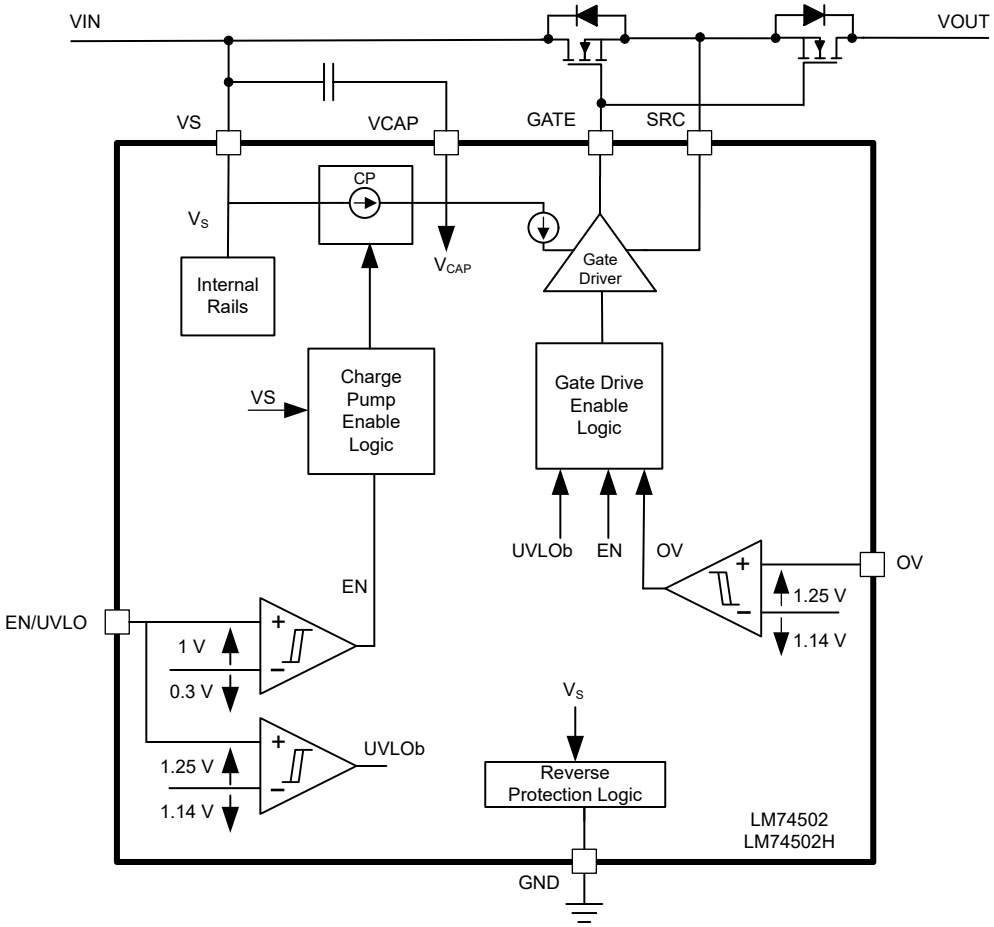
Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74502 and LM74502H controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit with load disconnect feature. This easy to use reverse polarity protection controller is paired with an external back-to-back connected N-channel MOSFETs to replace other reverse polarity schemes such as a P-channel MOSFETs. The wide input supply range of 4 V to 65 V allows protection and control of 12-V and 24-V input supply systems. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated charge pump drives external back-to-back connected N-channel MOSFETs with gate drive voltage of approximately 13 V. LM74502 with its 60-µA peak gate drive strength is suitable for applications that needs inherent inrush current control. LM74502H with its fast gate drive strength of 11-mA peak is suitable for applications which need fast turn-on and turn-off of external MOSFET switch. LM74502 features an adjustable overvoltage protection using the OV pin. with the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low shutdown current of 1 µA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The VS pin is used to power the LM74502's internal circuitry, typically drawing 45 µA when enabled and 1 µA when disabled. If the VS pin voltage is greater than the POR Rising threshold, then LM74502 operates in either shutdown mode or conduction mode in accordance with the EN/UVLO pin voltage. The voltage from VS to GND is designed to vary from 65 V to –65 V, allowing the LM74502 to withstand negative voltage transients.

8.3.2 Charge Pump (VCAP)

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and VS pin to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN/UVLO pin voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled the charge pump sources a charging current of 300 µA typically. If EN/UVLO pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to VS voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 75\ \mu s + C_{(VCAP)} \times \frac{V_{(VCAP\_UVLOR)}}{300\ \mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across VS and VCAP pins
- $V_{(VCAP\_UVLOR)}$ = 6.5 V (typical)

To remove any chatter on the gate drive approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to VS voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the VCAP to VS voltage is below to 11.6 V typically at which point the charge pump is enabled. The voltage between VCAP and VS continue to charge and discharge between 11.6 V and 12.4 V as shown in Figure 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74502 is reduced. When the charge pump is disabled it sinks 5-µA typical.

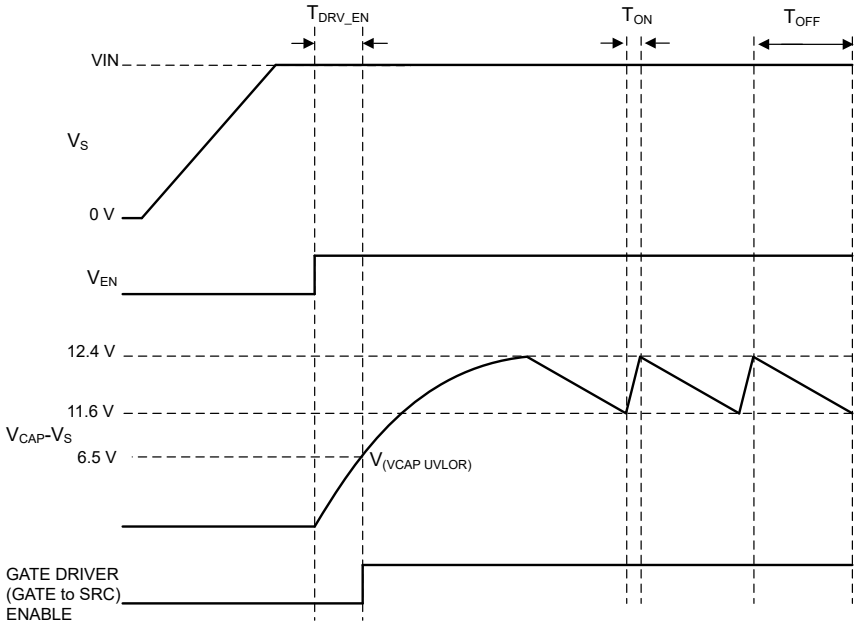


Figure 8-1. Charge Pump Operation

8.3.3 Gate Driver (GATE, SRC)

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE to SRC voltage.

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The VCAP to VS voltage must be greater than the undervoltage lockout voltage.
- The VS voltage must be greater than VS POR rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the SRC pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the conduction mode enhancing the external MOSFET completely.

The controller offers two gate drive variants. LM74502 with typical peak gate drive strength of 60 µA is suitable to achieve smooth start-up with inherent inrush current control due to its lower gate drive strength.

LM74502H with its 11 -mA typical peak gate drive strength is suitable for applications which need faster turn on such as load switch applications.

LM74502, LM74502H SRC pin is capable of handling negative voltage which also makes it suitable for load disconnect switch applications with loads which are inductive in nature.

8.3.3.1 Inrush Current Control

An external circuit as shown in Figure 8-2 can be added on the GATE pin of the LM74502 to have additional inrush current control for the applications which have large capacitive loads.

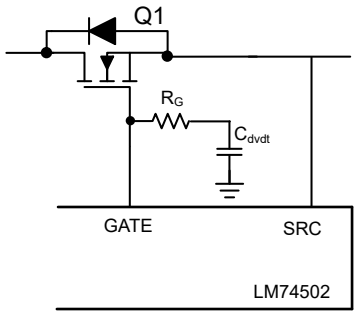


Figure 8-2. Inrush Current Limiting Using LM74502

The C_{dVdT} capacitor is required for slowing down the GATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate C_{dVdT} capacitance value.

$$C_{dvdt} = \frac{I_{GATE} \times C_{OUT}}{I_{INRUSH}} \quad (2)$$

where I_{GATE} is 60 µA (typical), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_G, in series with the C_{dVdT} capacitor acts as an isolation resistor between C_{dvdt} and gate of the MOSFET.

The inrush current control scheme shown in Figure 8-2 is not applicable to LM74502H as its gate drive is optimized for fast turn-on load switch applications.

8.3.4 Enable (EN/UVLO)

The LM74502 has an enable pin, EN/UVLO. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in the *Gate Driver (GATE, SRC)* and *Charge Pump (VCAP)* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74502 in shutdown mode. The EN/UVLO pin can withstand a voltage as large as 65 V and as low as –65 V. This feature allows for the EN/UVLO pin to be connected directly to the VS pin if enable functionality is not needed. In conditions where EN/UVLO is left floating, the internal sink current of 3 uA pulls EN/UVLO pin low and disables the device.

An external resistor divider connected from input to EN/UVLO to ground can be used to implement the input Undervoltage Lockout (UVLO) functionality in the system. When EN/UVLO pin voltage is lower than UVLO comparator falling threshold ($V_{EN/UVLOR}$) but higher than enable falling threshold (V_{ENF}), the device disables gate drive voltage, however, charge pump is kept on. This action ensures quick recovery of gate drive when UVLO condition is removed. If UVLO functionality is not required, connect EN/UVLO pin to VS.

8.3.5 Overvoltage Protection (OV)

LM74502 provides programmable overvoltage protection feature with OV pin. A resistor divider can be connected from input source to OV pin to ground in order to set overvoltage threshold. An internal comparator compares the input voltage against fixed reference (1.25 V) and disables the gate drive as soon as OV pin voltage goes above the OV comparator reference. When the resistor divider is referred from input supply side, device is configured for overvoltage cutoff functionality. When the resistor divider is referred from output side (V_{OUT}), the device is configured for overvoltage clamp functionality.

When OV pin voltage goes above OV comparator V_{OVR} threshold (1.25-V typical), the device disables gate drive, however, charge pump remains active. When OV pin voltage falls below V_{OVF} threshold (1.14-V typical), the gate is quickly turned on as charge pump is kept on and the device does not go through the device start-up process. When OV pin is not used, it can be connected to ground.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74502 enters shutdown mode when the EN/UVLO pin voltage is below the specified input low threshold $V_{(ENF)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74502 enters low I_Q operation with the VS pin only sinking 1 µA of current.

8.4.2 Conduction Mode

For the LM74502 to operate in conduction mode the gate driver must be enabled as described in the *Gate Driver (GATE, SRC)* section. If these conditions are achieved the GATE pin is

- Internally driven through 60-µA current source in case of LM74502
- Internally connected to the VCAP for fast turn-on of external FET in case of LM74502H

LM74502, LM74502H gate drive is disabled when OV pin voltage is above V_{OVR} threshold or EN/UVLO pin voltage is lower than $V_{EN/UVLOF}$ threshold.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM74502 is used with back-to-back connected N-Channel MOSFETs in a typical reverse polarity protection with load disconnect application. The schematic for the 12-V input supply reverse polarity protection is shown in Figure 9-1, where the LM74502 is used to drive the back-to-back connected MOSFETs Q1 and Q2 in series with a 12-V supply.

9.2 Typical Application

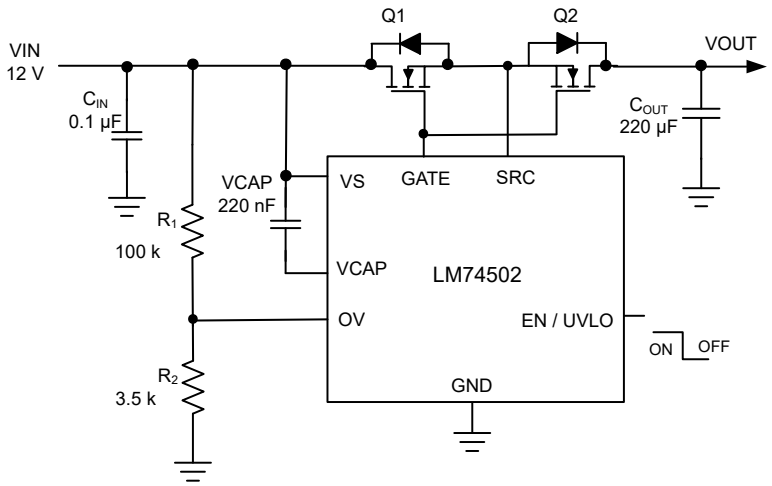


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters listed in Table 9-1 is presented.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V nominal
Overvoltage protection	37 V
Output current	5-A full load
Output capacitance	220-µF typical output capacitance

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range (including overvoltage protection)
- Maximum load current

9.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum gate-to-source voltage $V_{GS(MAX)}$ and the drain-to-source On resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This requirement would include any anticipated fault conditions. The maximum V_{GS} LM74502 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected. If a MOSFET with V_{GS} rating < 15 V is selected, a zener diode can be used between GATE to SRC pin to clamp V_{GS} to safe level.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred. Selecting a MOSFET with RDS(ON) that gives VDS drop 20 mV to 50 mV provides good trade off in terms of power dissipation and cost.

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.2.3 Overvoltage Protection

Resistors R1 and R2 connected in series is used to program the overvoltage threshold. Connecting R1 to VIN provides overvoltage cutoff and switching the connection to VOUT provides overvoltage clamp response. The resistor values required for setting the overvoltage threshold V_{OV} to 37 V are calculated by solving Equation 3

$$V_{OVR} = \frac{R_2 \times V_{OV}}{R_1 + R_2} \tag{3}$$

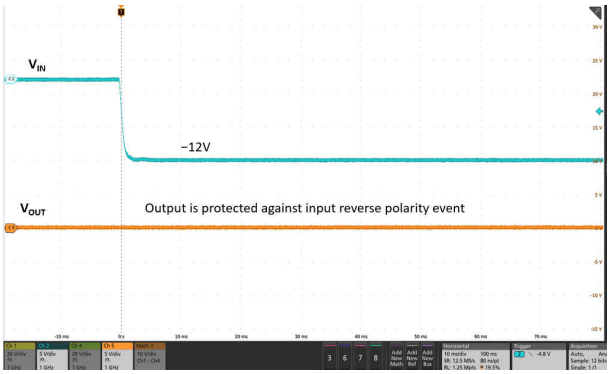
For minimizing the input current drawn from the supply through resistors R1 and R2, it is recommended to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OV pin. Select (R1 + R2) such that current through resistors is around 100 times higher than the leakage through OV pin. Based on the device electrical characteristics, V_{OVR} is 1.25 V , Select (R1) = 100 kΩ and R2 = 3.5 kΩ as a standard resistor value to set overvoltage cutoff of 37 V.

9.2.2.4 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

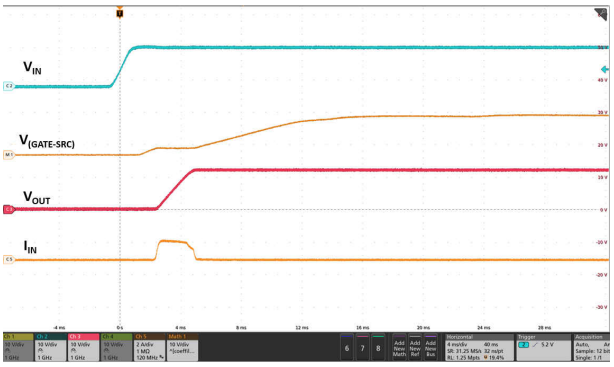
- C_{VCAP}: minimum recommended value of VCAP (µF) ≥ 10 × Effective $C_{ISS(MOSFET)}$ (µF), 0.22 µF is selected
- C_{IN}: typical input capacitor of 0.1 µF
- C_{OUT}: typical output capacitor 220 µF

9.2.3 Application Curves



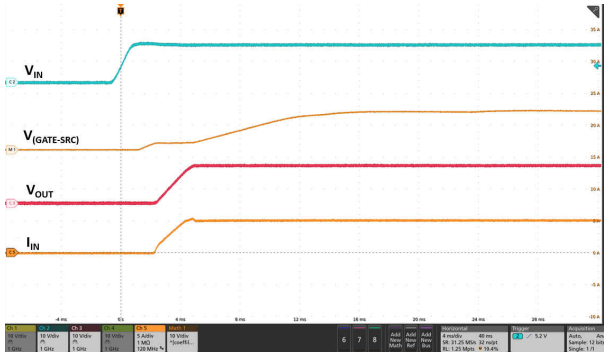
Time (10 ms/DIV)

Figure 9-2. Start-up with Reverse Voltage –12 V)



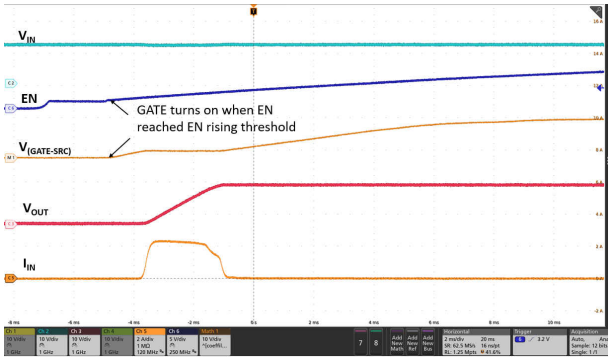
Time (4 ms/DIV)

Figure 9-3. Start-up with No Load



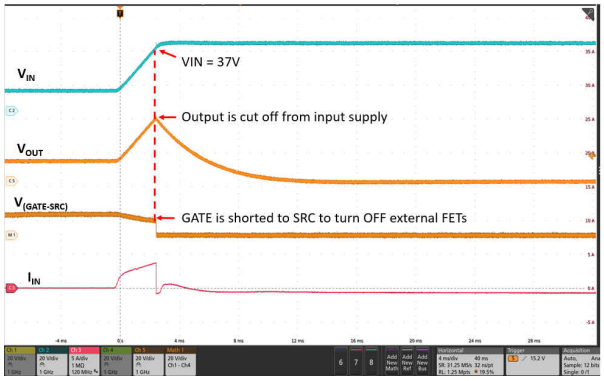
Time (4 ms/DIV)

Figure 9-4. Start-up with 5-A Load



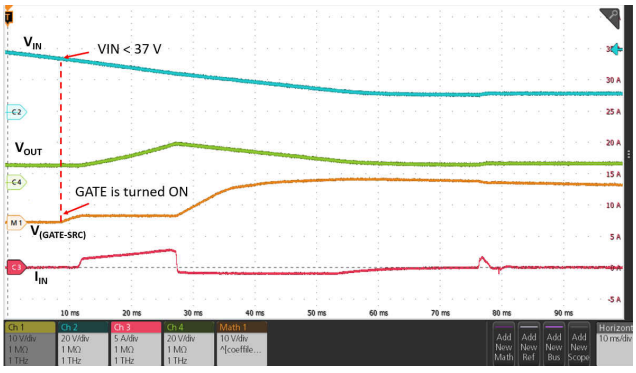
Time (2 ms/DIV)

Figure 9-5. Start-up with EN Control



Time (4 ms/DIV)

Figure 9-6. Overvoltage Cutoff Response (37 V)



Time (10 ms/DIV)

Figure 9-7. Overvoltage Recovery

9.3 Input Surge Stopper Using LM74502, LM74502H

Many industrial applications need to comply with input overvoltage transients and surge events specified by standards such as IEC61000-4-x. LM74502, LM74502H can be configured as input surge stopper to provide overvoltage along with input reverse supply protection.

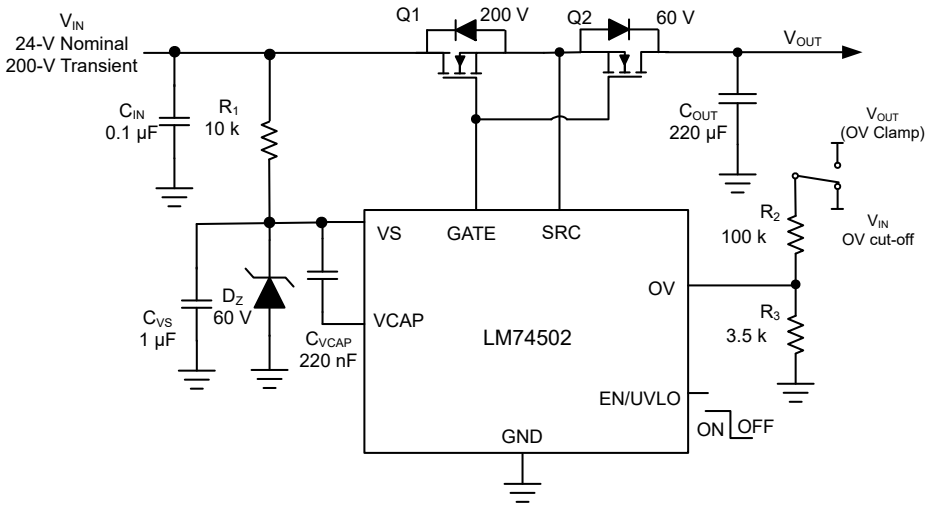


Figure 9-8. Typical Surge Stopper Application for 24-V Powered Systems

As shown in Figure 9-8 MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and LM74502 from input transient. Note that only the VS pin is exposed to input transient through a resistor, R1. A 60-V rated zener diode is used to clamp and protect the VS pin within recommended operating condition. Rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level.

9.3.1 VS Capacitance, Resistor R_1 and Zener Clamp (D_Z)

Minimum of 1 µF C_{VS} capacitance is required. During input overvoltage transient, resistor R1 and zener diode D_Z are used to protect VS pin from exceeding the maximum ratings by clamping V_{VS} to 60 V. Choosing R1 = 10 kΩ, the peak power dissipated in zener diode D_Z can be calculated using Equation 4.

$$P_{DZ} = V_{DZ} \times \frac{(V_{IN(MAX)} - V_{DZ})}{R_1} \tag{4}$$

Where V_{DZ} is the breakdown voltage of zener diode. Select the zener diode which can handle peak power requirement.

Peak power dissipated in resistor R1 can be calculated using Equation 5.

$$P_{R1} = \frac{(V_{IN(MAX)} - V_{DZ})^2}{R_1} \tag{5}$$

Select a resistor package which can handle peak power and maximum DC voltage.

9.3.2 Overvoltage Protection

For the overvoltage setting, refer to the resistor selection procedure described in *Overvoltage Protection*. Select (R2) = 100 kΩ and R3 = 3.5 kΩ as a standard resistor value to set overvoltage cutoff of 37 V.

9.3.3 MOSFET Selection

The VDS rating of the MOSFET Q1 must be minimum $V_{IN(max)}$ for designs with output overvoltage cutoff where output can reach 0 V with higher loads. For designs with output overvoltage clamp, MOSFET VDS rating must

be ($V_{IN(max)}$ – V_{OUT_CLAMP}). The VGS rating is based on GATE-SRC maximum voltage of 15 V. TI recommends a 20-V VGS rated MOSFET. Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET must be considered with sufficient design margin for reliable operation. An additional zener diode from GATE to SRC can be needed to protect the external FET in case output is expected to drop to the level where it can exceed external FET $V_{GS(max)}$ rating.

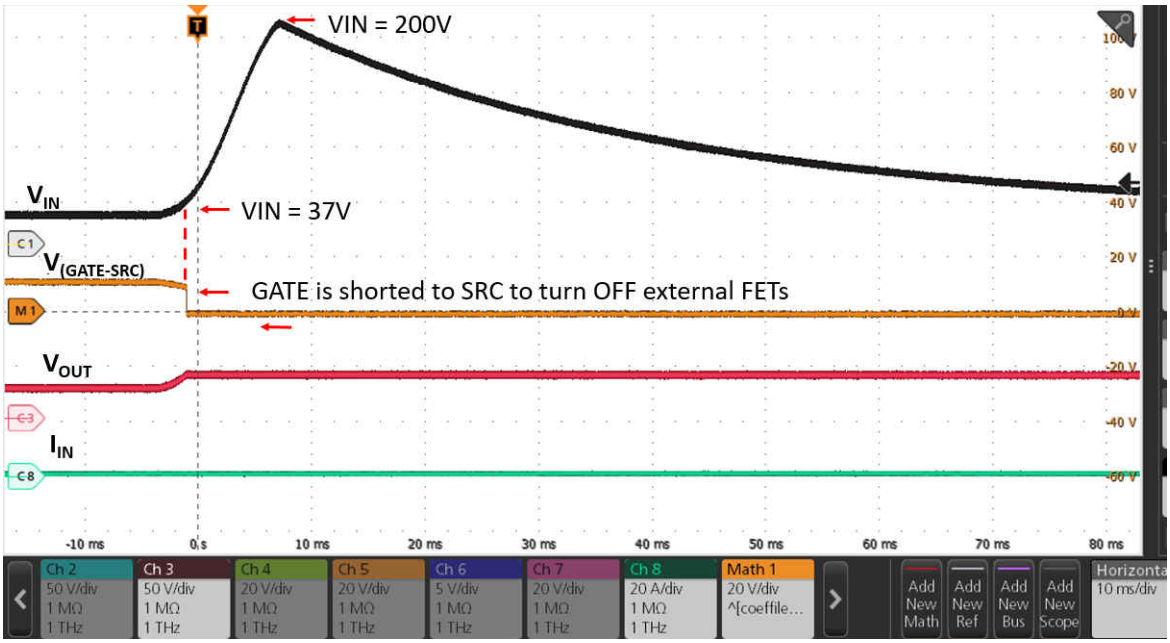


Figure 9-9. 200-V Surge Stopper with Overvoltage Cutoff Using LM74502

9.4 Fast Turn-On and Turn-Off High Side Switch Driver Using LM74502H

In applications such as industrial motor drives and safety power line communication digital output modules, N-Channel MOSFET based high side switch is very commonly used to disconnect the loads from supply line in case of faults such as overvoltage event . LM74502, LM74502H can be used to drive external MOSFET to realize simple high side switch with overvoltage protection. Figure 9-10 shows a typical application circuit where LM74502H is used to drive external MOSFET Q1 as a main power path connect and disconnect switch. A resistor divider from input to OV pin to ground can be used the set the overvoltage threshold.

If VOUT node (SRC pin) of the device is expected to drop in case of events such as overcurrent or short-circuit on load side then additional zener diode is required across gate and source pin of external MOSFET to protect it from exceeding it's maximum V_{GS} rating.

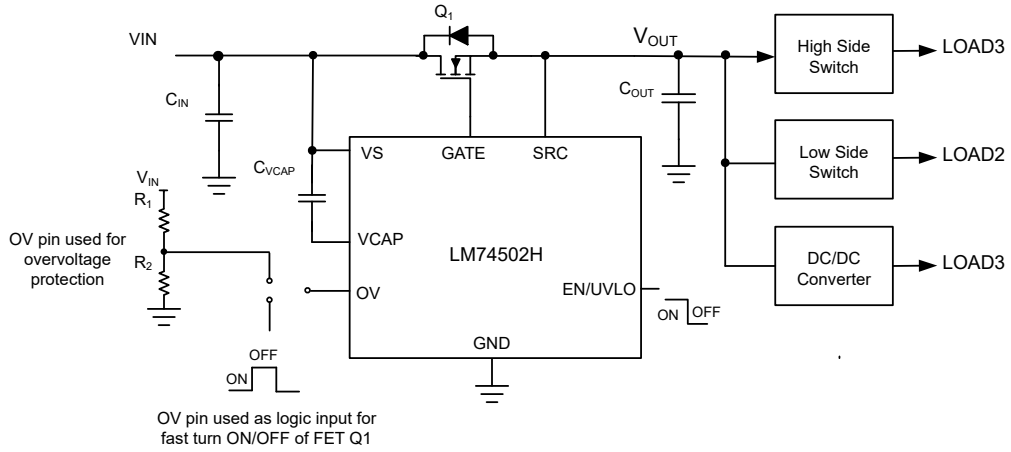


Figure 9-10. Fast Turn-ON and OFF High Side Switch Using LM74502H

Many industrial safety applications require fast switching off of MOSFET to verify proper functioning of the high side disconnect switch for diagnostic purpose. LM74502H OV pin can be used as control input to realize fast turn-on and turn-off load switch functionality. with OV pin pulled above V_{OVR} threshold of (1.25-V typical), LM74502H turns off the external MOSFET (with Ciss = 4.7 nF) within 1 µs typically. When OV pin is pulled low, LM74502H with its peak gate drive strength of 11 mA turns on external MOSFET with turn on speed of 7-µs typical. Figure 9-11 shows LM74502H GATE to SRC response when OV pin is used as logic input for turning external MOSFET on and off.

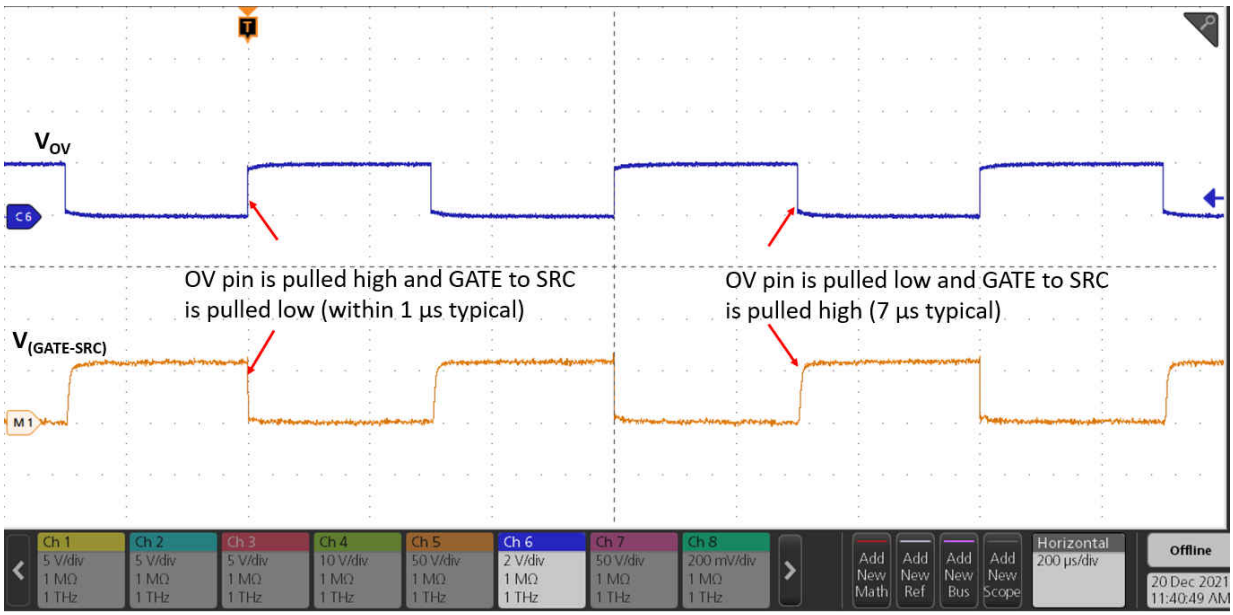


Figure 9-11. Fast Turn-On and Turn-Off High Side Switch Driver Using LM74502H

10 Power Supply Recommendations

The LM74502, LM74502H reverse polarity protection controller is designed for the supply voltage range of 3.2 V ≤ V_S ≤ 65 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 0.1 µF. Based on system requirements, a higher input bypass capacitor may be needed with LM74502H to avoid supply glitch in case of high inrush current start-up event. To prevent LM74502 and surrounding components from damage under the conditions of a direct output short circuit, use a power supply having overload and short-circuit protection.

11 Layout

11.1 Layout Guidelines

- Place the input capacitor C_{IN} of 0.1-µF minimum close to VS pin to ground. This typically helps with better EMI performance.
- Connect GATE and SRC pin of LM74502, LM74502H close to the MOSFET's GATE and SOURCE pin.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- The charge pump capacitor across VCAP and VS pin must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The GATE pin of the LM74502, LM74502H must be connected to the MOSFET gate with short trace. Avoid excessively thin and long running trace to the Gate Drive.

11.2 Layout Example

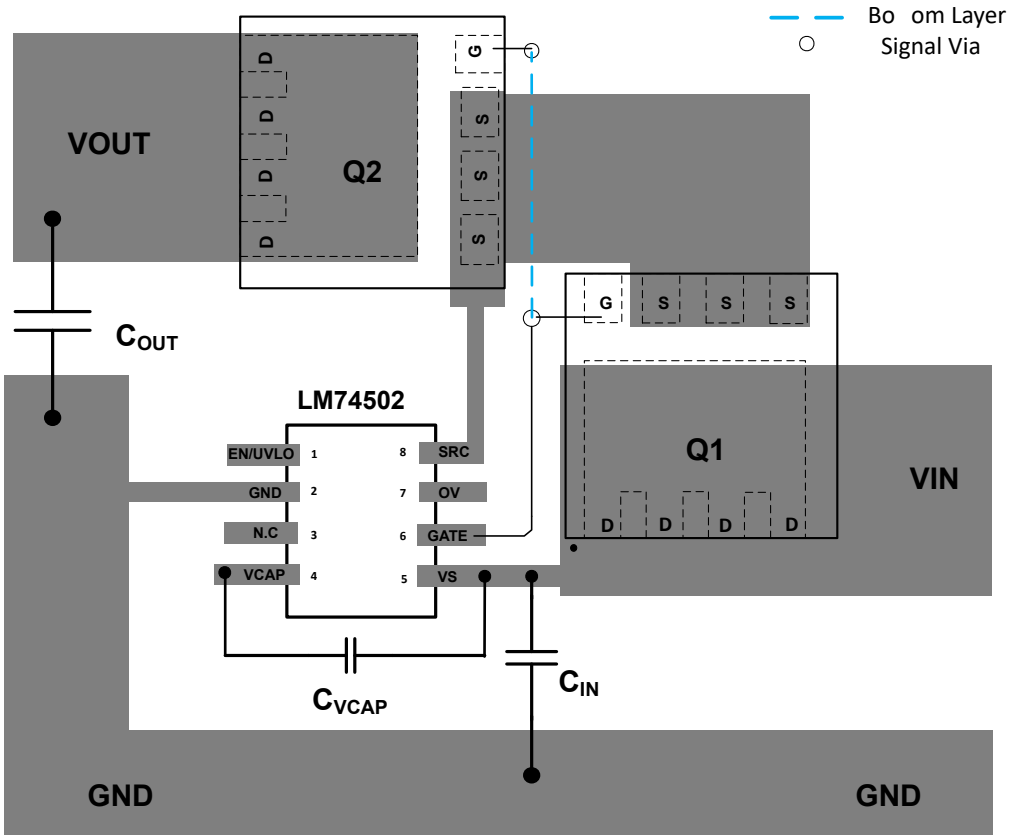


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74502DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM502	Samples
LM74502HDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L502H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM74502, LM74502H :

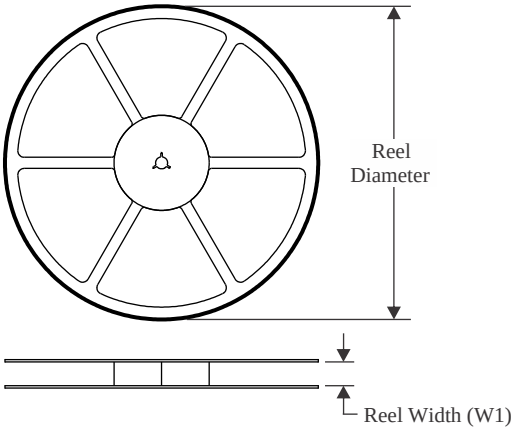
- Automotive : LM74502-Q1, LM74502H-Q1

NOTE: Qualified Version Definitions:

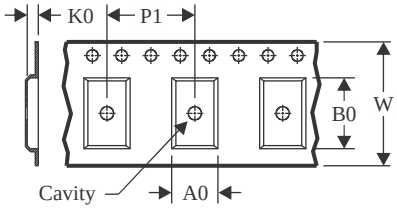
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

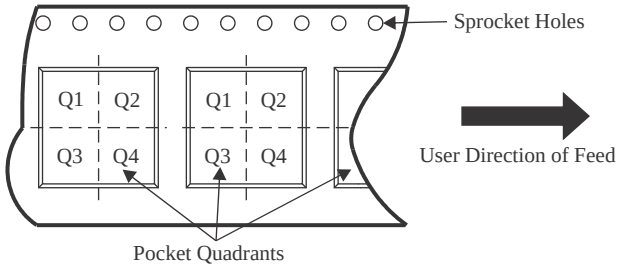


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

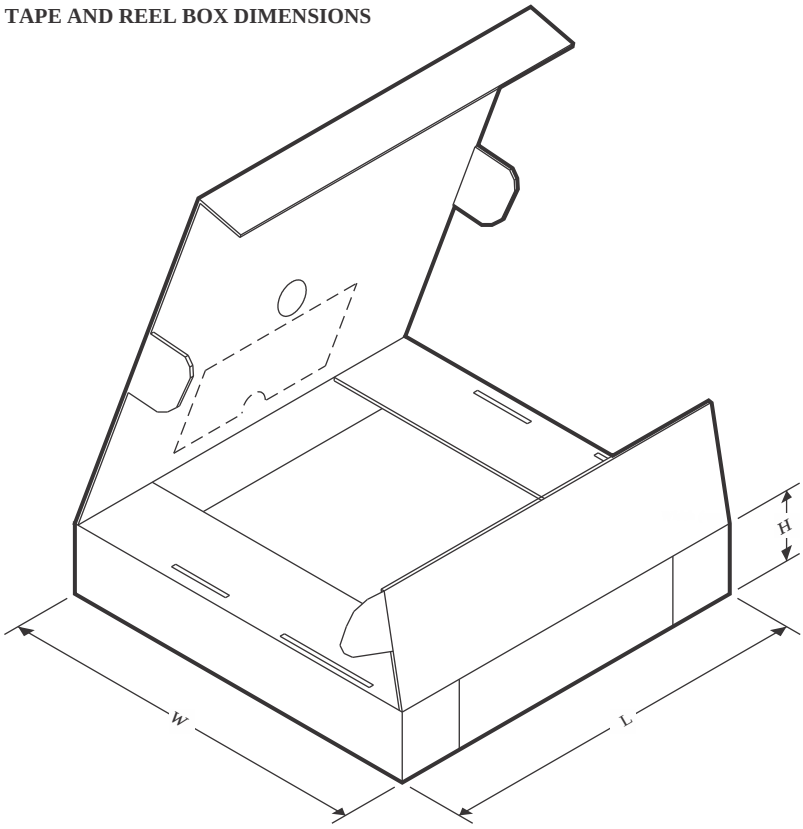
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74502DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM74502HDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

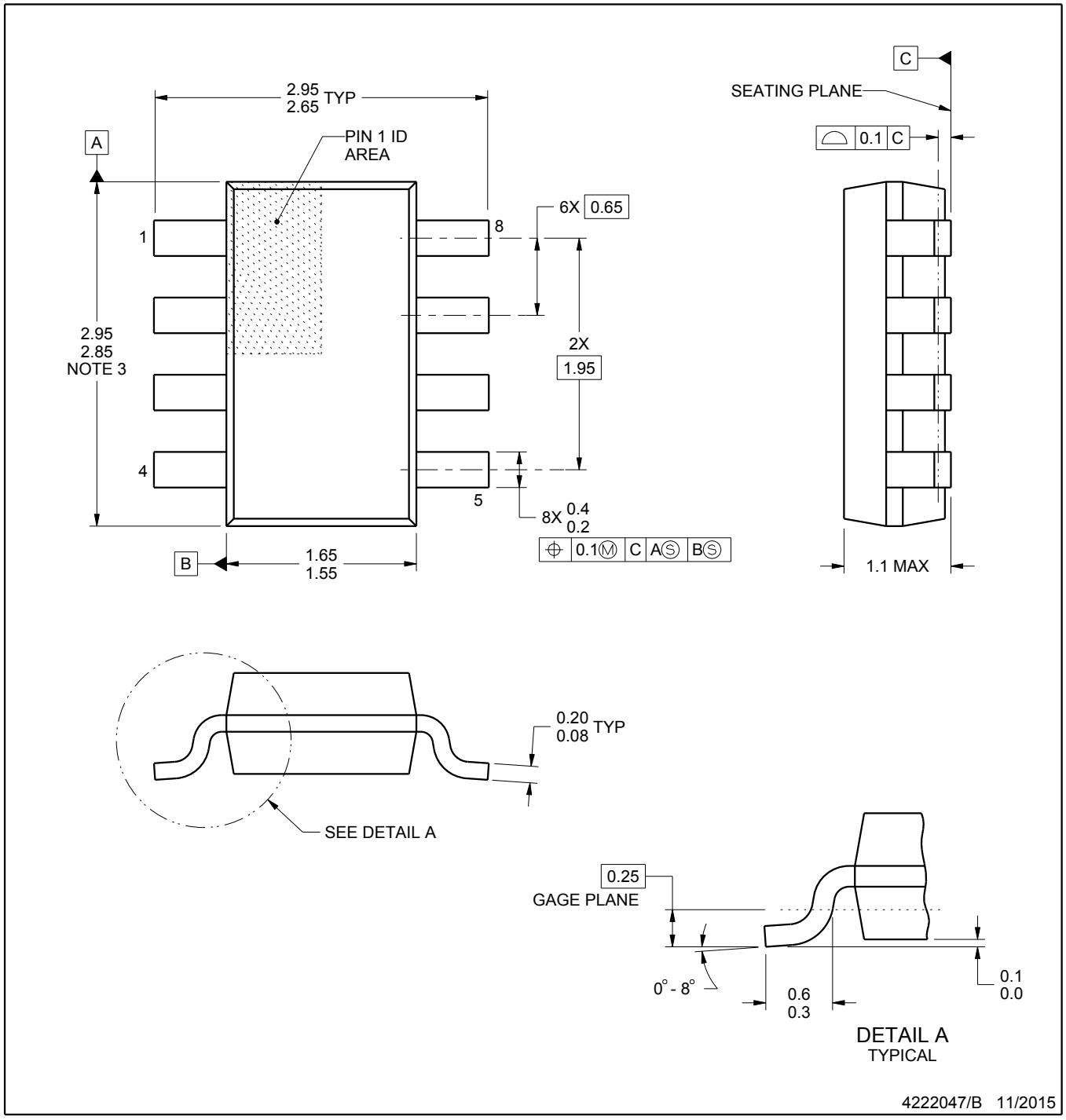
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74502DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM74502HDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

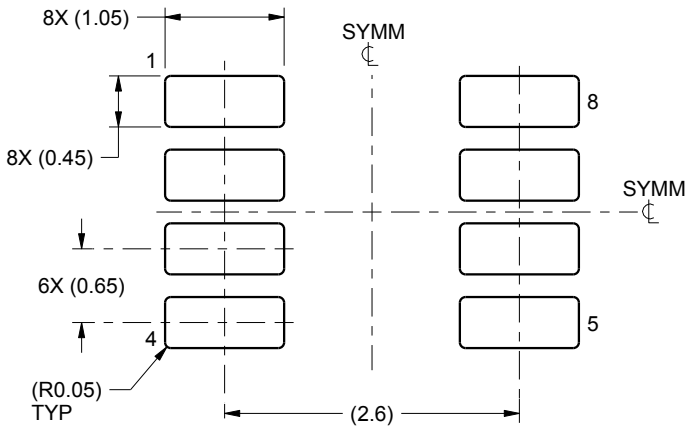
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

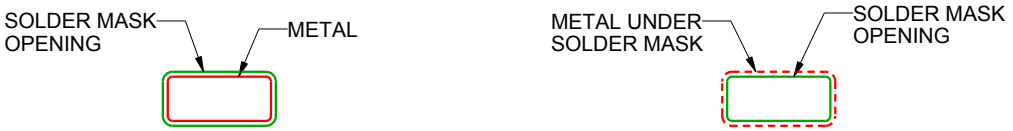


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

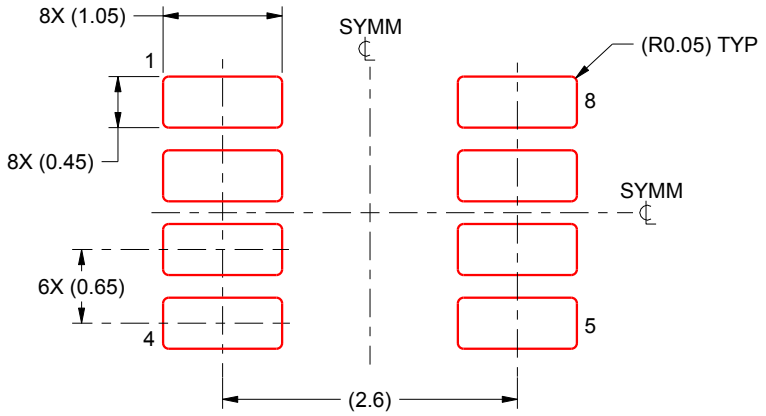
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

LP87702 Dual Buck Converter and 5-V Boost With Diagnostic Functions

1 Features

- FMEDA and Functional Safety Manual Available to Support System-Level Functional Safety Requirements up to SIL-2 (IEC 61508)
- Two High-Efficiency Step-Down DC/DC converters:
  - Maximum Output Current 3.5 A
  - 2-MHz, 3-MHz, or 4-MHz Switching Frequency
  - Auto PWM/PFM and Forced-PWM Operations
  - Output Voltage = 0.7 V to 3.36 V
- 5-V 600 mA Boost Converter
- Two Inputs for External Voltage Monitoring
- Two Programmable Power-Good Signals
- Dedicated Reference Voltage for Diagnostics
- Window Watchdog with Reset Output
- External Clock Input to Synchronize Switching
- Spread-Spectrum Modulation
- Programmable Start-up and Shutdown Delays and Sequencing with Enable Signal
- Configurable General Purpose Outputs (GPOs)
- I^2C-Compatible Interface
- Interrupt Function with Programmable Masking
- Output Short-Circuit and Overload Protection
- Overtemperature Warning and Protection
- Overvoltage Protection (OVP) and Undervoltage Lockout (UVLO)

2 Applications

- Building Automation:
  - Automated Doors and Gates
  - Motion Detector (PIR/Motion Sensor)
  - Video Surveillance:
    - Occupancy Detection (People Tracking, People Counting)
- Factory Automation:
  - Industrial Robot – Safety Area Scanner
  - Autonomous Guided Vehicle (AGV)
  - Level Transmitter – Sensing
- Industrial Transport:
  - Traffic Enforcement
  - Intersection Monitoring
  - Road-Railway Sensors
  - Intelligent Lighting Sensors
- Appliances:
  - AC Control
  - Appliances User Interface and Connectivity Modules

3 Description

The LP87702 contains two step-down DC/DC converters, and a 5-V boost converter to support safety critical applications. The device integrates two voltage monitoring inputs for external power supplies and a window watchdog.

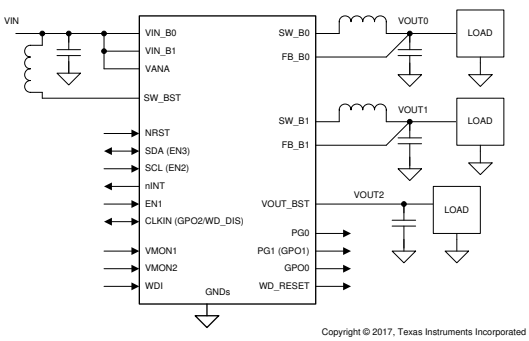
The automatic PWM/PFM (AUTO mode) operation gives high efficiency over a wide output current range for buck converters.

This device contains one-time-programmable (OTP) memory. Each orderable part number has specific OTP settings for a given application. Details of the default OTP configuration for each orderable part number is found in the technical reference manual.

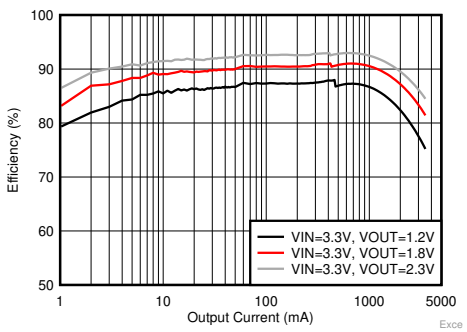
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP87702	VQFN (32)	5.00 mm × 5.00 mm

(1) See the orderable addendum at the end of the data sheet for all available packages.



Simplified Schematic



Buck Efficiency vs Output Current

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2021	*	Initial Release

5 Pin Configuration and Functions

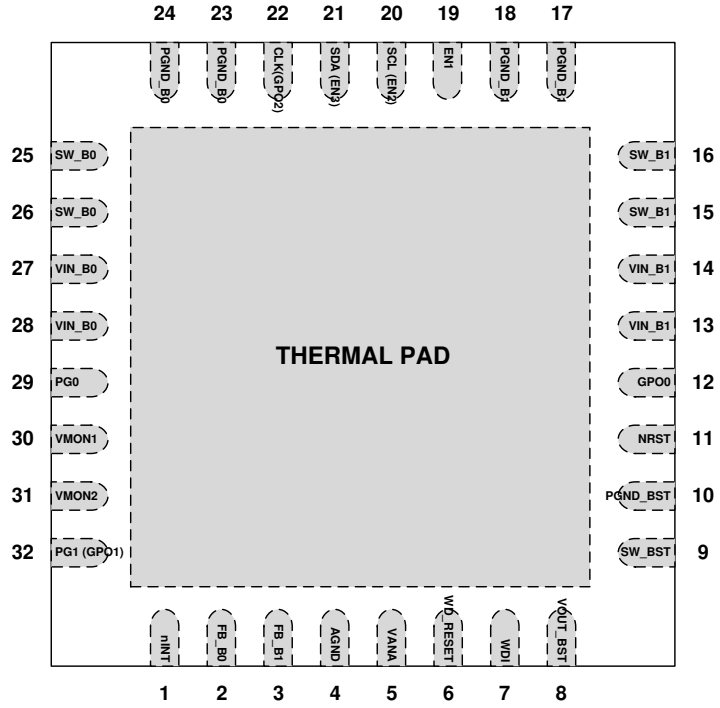


Figure 5-1. RHB Package 32-Pin VQFN With Thermal Pad Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
AGND	4	G	Ground
CLKIN	22	D/I/O	External clock input. Alternative function is general purpose digital output 2 (GPO2).
EN1	19	D/I	Programmable Enable 1 signal.
FB_B0	2	A	Output voltage feedback for Buck0.
FB_B1	3	A	Output voltage feedback for Buck1.
GPO0	12	D/O	General purpose digital output 0.
nINT	1	D/O	Open-drain interrupt output. Active LOW.
NRST	11	D/I	Reset signal for the device.
PG0	29	D/O	Programmable power-good indication signal.
PG1	32	D/O	Programmable power-good indication signal. Alternative function is general purpose digital output 1 (GPO1).
PGND_B0	23, 24	P/G	Power ground for Buck0.
PGND_B1	17, 18	P/G	Power Ground for Buck1.
PGND_BST	10	P/G	Power ground for boost.
SCL	20	D/I	Serial interface clock input for I2C access. Connect a pullup resistor. Alternative function is programmable to the enable 2 signal.
SDA	21	D/I/O	Serial interface data input and output for I2C access. Connect a pullup resistor. Alternative function is programmable to the enable 3 signal.
SW_B0	25, 26	P/O	Buck0 switch node.
SW_B1	15, 16	P/O	Buck1 switch node.
SW_BST	9	P/I	Boost input.
VANA	5	P	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.
VMON1	30	A/I	Voltage monitoring input 1.

Table 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VMON2	31	A/I	Voltage monitoring input 2.
VIN_B0	27, 28	P/I	Input for Buck0. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed.
VIN_B1	13, 14	P/I	Input for Buck1. The separate power pins VIN_Bx are not connected together internally – VIN_Bx pins must be connected together in the application and be locally bypassed.
VOUT_BST	8	P/O	Boost output.
WD_RESET	6	D/O	Reset output from window watchdog
WDI	7	D/I	Digital input signal for window watchdog
Thermal pad	N/A	G	
A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin			

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	–0.3	6	V
SW_B0, SW_B1	Voltage on buck switch nodes	–0.3	(VIN_Bx + 0.3 V) with 6-V maximum	V
FB_B0, FB_B1	Voltage on buck voltage sense nodes	–0.3	(VANA + 0.3 V) with 6-V maximum	V
VOUT_BST	Voltage on boost output	–0.3	6	V
SCL (EN2), SDA (EN3), VMON1, VMON2	Voltage on voltage monitoring pins	–0.3	(VANA + 0.3 V) with 6-V maximum	V
NRST, EN1, nINT	Voltage on logic pins (input or output pins)	–0.3	6	V
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	–0.3	(VANA + 0.3 V) with 6-V maximum	V
T_{J-MAX}	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C
Maximum lead temperature (soldering, 10 sec.)			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±500	
		Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
INPUT VOLTAGE				
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	2.8	5.5	V
VMON1, VMON2	Voltage on voltage monitoring pins	0	5.5	V
NRST, EN1, EN2, EN3, nINT	Voltage on logic pins (input or output pins)	0	5.5	
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V maximum	V
TEMPERATURE				

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Junction temperature, T_J	−40	140	°C
Ambient temperature, T_A	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	17.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL COMPONENTS						
C_{IN_BUCK}	Input filtering capacitance for buck converters	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		µF
C_{OUT_BUCK}	Output filtering capacitance for buck converters	Effective total capacitance. Maximum includes POL capacitance	15	22	100	µF
$C_{OUT\_BUCK\_POL}$	Point-of-load (POL) capacitance for buck converters	Optional POL capacitance		22		µF
C_{OUT_BST}	Output filtering capacitance for boost converter	Effective capacitance	10	22	40	µF
ESR_C	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L_{BUCK}	Inductor for buck converters	Inductance of the inductor		0.47		µH
			–30%		30%	
L_{BST}	Inductor for boost converters	Inductance of the inductor, 2-MHz switching		1		µH
		Inductance of the inductor, 4-MHz switching		1		
		Inductance of the inductor	–30%		30%	
DCR_L	Inductor DCR			25		mΩ
BUCK CONVERTERS						
$V_{(VIN\_Bx)}$, $V_{(VANA)}$	Input voltage range		2.8	3.3	5.5	V
V_{OUT_Bx}	Output voltage	Programmable voltage range	0.7	1	3.36	V
		Step size, 0.7 V ≤ V_{OUT} < 0.73 V		10		mV
		Step size, 0.73 V ≤ V_{OUT} < 1.4 V		5		
		Step size, 1.4 V ≤ V_{OUT} ≤ 3.36 V		20		
I_{OUT_Bx}	Output current	Output current			3.5 (3)	A

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Minimum voltage difference between $V_{(VIN\_Bx)}$ and V_{OUT_Bx} for electrical characteristics	$V_{(VIN\_Bx)} – V_{OUT}$, I_{OUT_Bx} ≤ 2 A	0.8			V
		$V_{(VIN\_Bx)} – V_{OUT}$, I_{OUT_Bx} > 2 A	1			
	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode, V_{OUT} < 1.0 V	–20		20	mV
		Force PWM mode, V_{OUT} ≥ 1.0 V	–2%		2%	
		PFM mode, V_{OUT} < 1.0 V, the average output voltage level is increased by max. 20 mV	–20		40	mV
		PFM mode, V_{OUT} ≥ 1.0 V, the average output voltage level is increased by max. 20 mV	–2%		2% + 20mV	
	Ripple voltage	PWM mode, V_{OUT} = 1.2 V, f_{SW} = 4 MHz, C_{OUT} = 22 + 22 µF (GCM31CR71A226KE02)		5		mV_{p-p}
		PFM mode, L = 0.47 µH, C_{OUT} = 22 + 22 µF (GCM31CR71A226KE02)		25		
DC_{LNR}	DC line regulation	I_{OUT} = $I_{OUT(max)}$		±0.05		%/V
DC_{LDR}	DC load regulation in PWM mode	V_{OUT_Bx} = 1.0 V, I_{OUT} from 0 to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response	I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs, PWM mode, V_{VIN_Bx} = 3.3V, V_{OUT_Bx} = 1.2 V, C_{OUT} = 22 + 22 µF, L = 0.47 µH, f_{SW} = 4 MHz		±65		mV
T_{LNSR}	Transient line response	$V_{(VIN\_Bx)}$ stepping 3 V ↔ 3.5 V, T_R = T_F = 10 µs, I_{OUT} = $I_{OUT(max)}$		±20		mV
$I_{LIM\ FWD}$	Forward current limit for both bucks (peak for every switching cycle)	Programmable range	1.5		4.5	A
		Step size		0.5		
		Accuracy, $V_{(VIN\_Bx)}$ ≥ 3 V, I_{LIM} = 4 A	–5%	7.5%	20%	
		Accuracy, 2.8 V ≤ $V_{(VIN\_Bx)}$ < 3 V, I_{LIM} = 4 A	–20%	7.5%	20%	
$I_{LIM\ NEG}$	Negative current limit		1.6	2	3	A
$R_{DS(ON)}$ BUCK HS FET	On-resistance, high-side FET	Each phase, between VIN_Bx and SW_Bx pins (I = 1.0 A)		60	110	mΩ
$R_{DS(ON)}$ BUCK LS FET	On-resistance, low-side FET	Each phase, between SW_Bx and PGND_Bx pins (I = 1.0 A)		55	80	mΩ
f_{SW}	Switching frequency, PWM mode OTP programmable	2-MHz setting or V_{OUT_Bx} < 0.8 V	1.8	2	2.2	MHz
		3-MHz setting and V_{OUT_Bx} ≥ 0.8 V	2.7	3	3.3	
		4-MHz setting and V_{OUT_Bx} ≥ 1.1 V	3.6	4	4.4	
	Start-up time (soft start)	From ENx to V_{OUT_Bx} = 0.35 V (slew-rate control begins)		120		µs
	Overshoot during start-up				50	mV
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 010, V_{VOUT_Bx} ≥ 0.7 V	–15%	10	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 011, V_{VOUT_Bx} ≥ 0.7 V	–15%	7.5	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 100, V_{VOUT_Bx} ≥ 0.7 V	–15%	3.8	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 101, V_{VOUT_Bx} ≥ 0.7 V	–15%	1.9	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 110, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.94	15%	mV/µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 111, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.47	15%	mV/µs

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PFM-PWM}$	PFM-to-PWM switch - current threshold(5)			520		mA
$I_{PWM-PFM}$	PWM-to-PFM switch - current threshold(5)			240		mA
	Output pull-down resistance	Converter disabled	75	125	175	Ω
BOOST CONVERTER						
V_{IN_BST}	Input voltage range for boost power inputs		2.8	3.3	4	V
	Input voltage range when bypass switch mode selected		4.5		5.5	V
V_{OUT_BST}	Output voltage, boost mode	BOOST_VSET = 00		4.9		V
		BOOST_VSET = 01		5.0		
		BOOST_VSET = 10		5.1		
		BOOST_VSET = 11		5.2		
I_{OUT_BST}	Output current	Both boost and bypass mode			0.6	A
I_{LIM_BST}	Output current limit	BOOST_ILIM = 00, V_{IN_BST} < 3.6 V	0.8	1	1.3	A
		BOOST_ILIM = 01, V_{IN_BST} < 3.6 V	1.1	1.4	1.9	
		BOOST_ILIM = 10, V_{IN_BST} < 3.6 V	1.5	1.9	2.3	
		BOOST_ILIM = 11, V_{IN_BST} < 3.6 V	2.2	2.8	3.4	
$V_{OUT\_BST\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature. Boost mode	Default output voltage	–3%		3%	
V_{DROP}	Voltage drop, bypass mode,	Iout = 250 mA			83	mV
	Ripple voltage, boost mode	22 µF effective output capacitance		20		mV_{p-p}
DC_{LDR}	DC load regulation, boost mode	I_{OUT} = 1 mA to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response, boost mode	I_{OUT} = 1 mA to 250 mA, T_R = T_F = 1 µs, 22 µF effective output capacitance, VIN > 3 V	–220		220	mV
I_{SHORT}	Short circuit current limitation	During start-up, both boost and bypass mode. Short circuit current limit applies until V_{OUT_BST} = V_{IN_BST}		625		mA
$R_{DS(ON)}$ BST HS FET	On-resistance, high-side FET	Pin-to-pin, between SW_BST and VOUT_BST pins (I = 250 mA)		145	220	mΩ
$R_{DS(ON)}$ BST LS FET	On-resistance, low-side FET	Pin-to-pin, between SW_BST and PGND_BST pins (I = 250 mA)		90	175	mΩ
f_{SW}	Switching frequency, boost mode	2-MHz setting	1.8	2	2.2	MHz
		4-MHz setting	3.6	4	4.4	MHz
	Start-up time, boost mode	From enable to boost VOUT within 3% of target value. C_{OUT_BST} = 22 µF		450		µs
	Output pull-down resistance	Converter disabled		135		Ω
EXTERNAL CLOCK AND PLL						

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External input clock(6)	Nominal frequency	1		24	MHz
	Nominal frequency step size		1		
	Required accuracy from nominal frequency	–30%		10%	
External clock detection	Delay for detecting loss of external clock, nominal internal clock, clock accuracy ±10%			1.8	µs
	Delay for detecting valid external clock, nominal internal clock, clock accuracy ±10%			20	
Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		µs
PLL output clock jitter	Cycle to cycle		300		ps, p-p
MONITORING FUNCTIONS					
VANA Voltage Monitoring	Voltage threshold, VANA_THRESHOLD = 0		3.3		V
	Voltage threshold, VANA_THRESHOLD = 1		5.0		
	Voltage window, VANA_WINDOW = 00	±3%	±4%	±5%	
	Voltage window, VANA_WINDOW = 01	±4%	±5%	±6%	
	Voltage window, VANA_WINDOW = 10 or 11	±9%	±10%	±11%	
VMON1 and VMON2 Voltage Monitoring Thresholds	VMONx_THRESHOLD = 000		0.65		V
	VMONx_THRESHOLD = 001		0.8		
	VMONx_THRESHOLD = 010		1.0		
	VMONx_THRESHOLD = 011		1.1		
	VMONx_THRESHOLD = 100		1.2		
	VMONx_THRESHOLD = 101		1.3		
	VMONx_THRESHOLD = 110		1.8		
	VMONx_THRESHOLD = 111		1.8		
VMON1 and VMON2 Voltage Monitoring Windows	VMONx_WINDOW = 00, VMONx_THRESHOLD from 000 to 111	±1%	±2%	±3%	
	VMONx_WINDOW = 01, VMONx_THRESHOLD from 000 to 111	±2%	±3%	±4%	
	VMONx_WINDOW = 10, VMONx_THRESHOLD from 000 to 111	±3%	±4%	±5%	
	VMONx_WINDOW = 11, VMONx_THRESHOLD from 000 to 111	±5%	±6%	±7%	
Buck0 and Buck1 Voltage Monitoring Windows	BUCKx_WINDOW = 00	±20	±30	±40	mV
	BUCKx_WINDOW = 01	±37	±50	±63	
	BUCKx_WINDOW = 10	±57	±70	±83	
	BUCKx_WINDOW = 11	±77	±90	±103	
Boost Voltage Monitoring	BOOST_WINDOW = 00	±0.6%	±2%	±3.4%	
	BOOST_WINDOW = 01	±2.6%	±4%	±5.4%	
	BOOST_WINDOW = 10	±4.6%	±6%	±7.4%	
	BOOST_WINDOW = 11	±6.6%	±8%	±9.4%	
Deglitch time	VANA, VMONx and BOOST monitoring	12		17	µs
	BUCKx monitoring	6		9	
PROTECTION FUNCTIONS					
Thermal warning	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	°C
	Temperature rising, TDIE_WARN_LEVEL = 1	130	140	150	
	Hysteresis		20		

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown	Temperature rising	140	150	160	°C
		Hysteresis		20		
$VANA_{OVP}$	VANA Overvoltage	Voltage rising, VANA_OVP_SEL = 0	5.6	5.8	6.1	V
		Voltage falling, VANA_OVP_SEL = 0	5.45	5.73	5.96	
		Voltage rising, VANA_OVP_SEL = 1	4.1	4.3	4.6	
		Voltage falling, VANA_OVP_SEL = 1	3.95	4.23	4.46	
		Hysteresis	40		200	mV
$VANA_{UVLO}$	VANA Undervoltage Lockout	Voltage rising	2.51	2.63	2.75	V
		Voltage falling	2.5	2.6	2.7	
	BUCKx short circuit detection	Threshold	0.32	0.35	0.45	V
	Bypass short circuit current limit			270	420	mA
LOAD CURRENT MEASUREMENT FOR BUCK CONVERTERS						
	Current measurement range	Current corresponding to maximum output code (note: maximum current for LP87702 buck is 3.5A)			10.22	A
	Resolution	LSB		20		mA
	Measurement accuracy	I_{OUT} > 1A		<10%		
	Measurement time	Auto mode (automatically changing to PWM mode for the measurement)		50		µs
		PWM mode			25	
CURRENT CONSUMPTION						
	Shutdown current consumption	NRST = 0		1		µA
	Standby current consumption, converters disabled	NRST = 1		9		µA
	Active current consumption, one buck converter enabled in Auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		55		µA
	Active current consumption, two buck converters enabled in Auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		90		µA
	Active current consumption during PWM operation, one buck converter enabled	I_{OUT_Bx} = 0 mA		15		mA
	Active current consumption during PWM operation, two buck converters enabled	I_{OUT_Bx} = 0 mA		27		mA
	Active current consumption, Boost converter in PWM operation	I_{OUT_BST} = 0 mA, f_{SW} = 4 MHz		18		mA
	PLL and clock detector current consumption	Additional current consumption when enabled, 2 MHz external clock		2		mA

Limits apply over the junction temperature range –40°C ≤ T_J ≤ 140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_A = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted. (1) (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT SIGNALS SCL, SDA, NRST, EN1, EN2, EN3, CLKIN, WDI						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
V_{HYS}	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	ENx, CLKIN, WDI pull-down resistance	ENx_PD = 1, CLKIN_PD = 1, WDI_PD = 1		500		kΩ
	NRST pull-down resistance	Always enabled		500		kΩ
DIGITAL OUTPUT SIGNALS nINT, SDA						
V_{OL}	Output low level	SDA: I_{SOURCE} = 20 mA			0.5	V
		nINT: I_{SOURCE} = 2 mA			0.4	
R_P	External pull-up resistor for nINT	To VIO Supply		10		kΩ
DIGITAL OUTPUT SIGNALS PGOOD, PG1, GPO0, GPO1, GPO2, WD_RESET						
V_{OL}	Output low level	I_{SOURCE} = 2 mA			0.4	V
V_{OH}	Output high level, configured to push-pull	I_{SINK} = 2 mA	V_{VANA} - 0.4		V_{VANA}	
V_{PU}	Supply voltage for external pull-up resistor, configured to open-drain				V_{VANA}	
R_{PU}	External pull-up resistor, configured to open-drain			10		kΩ
ALL DIGITAL INPUTS						
I_{LEAK}	Input current	All logic inputs except NRST, over pin voltage range, when PD not enabled	–1		1	µA
		NRST, over pin voltage range. Other logic inputs when PD enabled.	–1		20	µA

(1) All voltage values are with respect to network ground.

(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis.

(3) The maximum output current can be limited by the forward current limit $I_{LIM\ FWD}$. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.

(4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current. Applies when internal oscillator is used.

(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level.

(6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

6.6 I²C Serial Bus Timing Parameters

See [1].			MIN	MAX	UNIT
f_{SCL}	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode +		1	MHz
		High-speed mode, C_b = 100 pF		3.4	
		High-speed mode, C_b = 400 pF		1.7	
t_{LOW}	SCL low time	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode +	0.5		
		High-speed mode, C_b = 100 pF	160		ns
		High-speed mode, C_b = 400 pF	320		
t_{HIGH}	SCL high time	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode, C_b = 100 pF	60		ns
		High-speed mode, C_b = 400 pF	120		
$t_{SU;DAT}$	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode +	50		
		High-speed mode	10		
$t_{HD;DAT}$	Data hold time	Standard mode	0.01	3.45	µs
		Fast mode	0.01	0.9	
		Fast mode +	0.01		
		High-speed mode, C_b = 100 pF	10	70	ns
		High-speed mode, C_b = 400 pF	10	150	
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7		µs
		Fast Mode	1.3		
		Fast mode +	0.5		
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode	4		µs
		Fast Mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	

See (1).			MIN	MAX	UNIT
t_{fDA}	Fall time of SDA signal	Standard mode		250	ns
		Fast mode	20+0.1 C_b	250	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{fCL}	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
C_b	Capacitive load for each bus line (SCL and SDA)			400	pF
t_{SP}	Pulse width of spike suppressed (Spikes shorter than indicated width are suppressed)	Fast mode, Fast mode +		50	ns
		High-speed mode		10	

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.

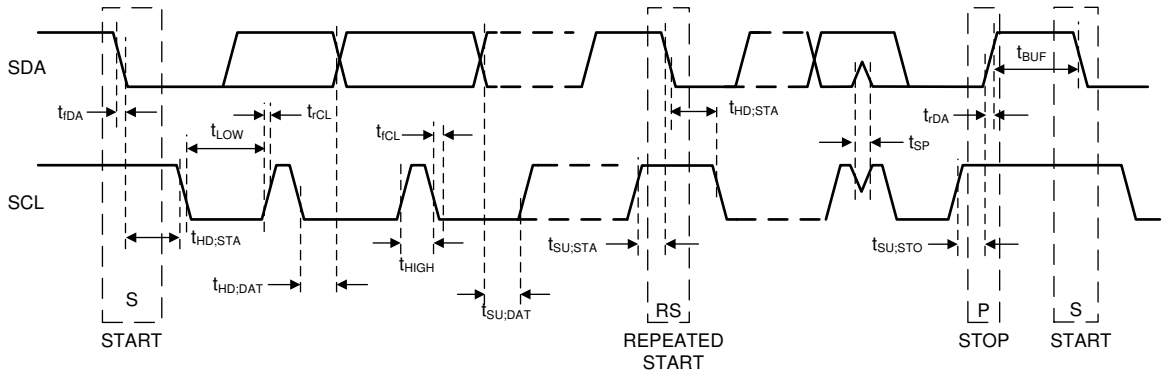


Figure 6-1. I²C Timing

6.7 Typical Characteristics

Unless otherwise specified: V_{IN} = 3.3 V, T_A = 25°C, f_{SW} -setting 4 MHz, L0 = L1 = 0.47 µH (TOKO DFE252012PD-R47M), L2 = 1 µH (TFM252012ALMA1R0), C_{OUT_BUCK} = 22 µF, and C_{POL_BUCK} = 22 µF, C_{OUT_BOOST} = 22 µF. Measurements are done using connections in the Figure 8-1.

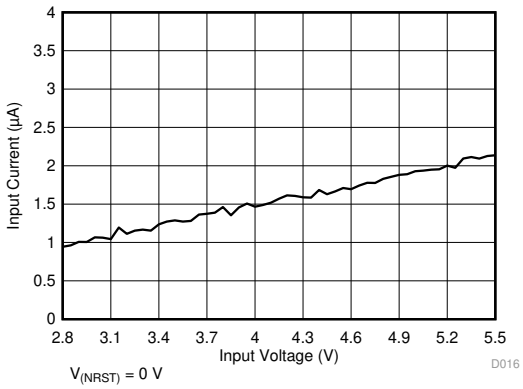


Figure 6-2. Shutdown Current Consumption vs Input Voltage

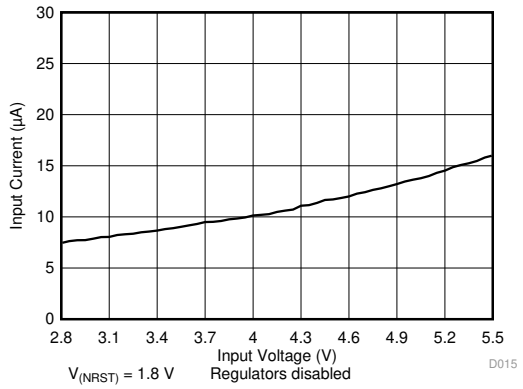


Figure 6-3. Standby Current Consumption vs Input Voltage

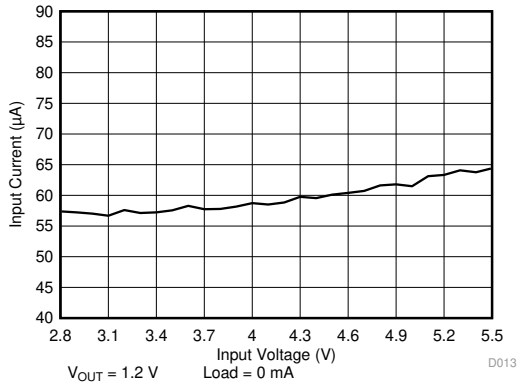


Figure 6-4. Active State Current Consumption vs Input Voltage, One Buck Converter Enabled in PFM Mode

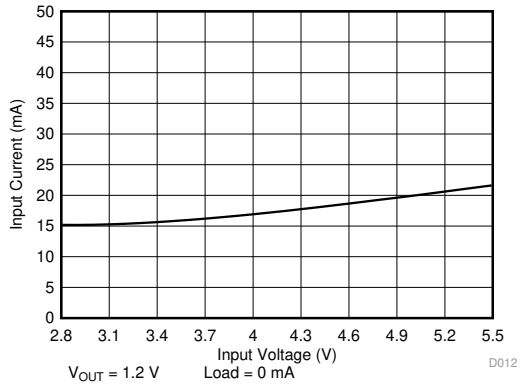


Figure 6-5. Active State Current Consumption vs Input Voltage, One Buck Converter Enabled in PWM Mode

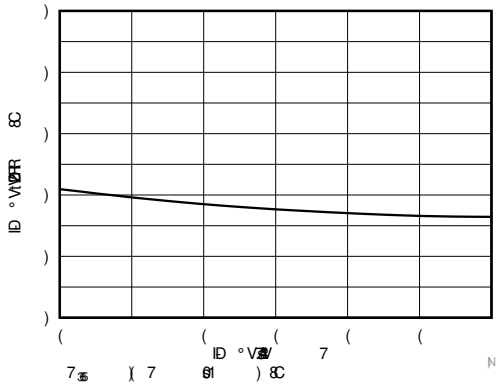


Figure 6-6. Active State Current Consumption vs Input Voltage, Boost Converter Enabled in PWM Mode

7 Detailed Description

7.1 Overview

The LP87702 is a high-efficiency, high-performance power supply IC with two step-down DC/DC converters (Buck0 and Buck1) and boost converter for automotive and industrial applications. The input voltage range is from 2.8 V to 5.5 V. The typical application input voltage levels are 3.3 V and 5 V. $VANA_{OVP}$ is set to 4.3 V (typical) with 3.3 V input and boost enabled. The boost can be used as a load switch and $VANA_{OVP}$ is set to 5.8 V (typical) when input voltage is 5 V. $VANA_{OVP}$ is selected in OTP by VANA_OVP_SEL and is a fixed factory setting. Table 7-1 lists the output characteristics of the various converters.

Table 7-1. Supply Specification

SUPPLY	OUTPUT		
	V_{OUT} RANGE (V)	RESOLUTION (mV)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
Boost	4.9 to 5.2	100	600
Buck0	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500
Buck1	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500

The LP87702 converters support switching clock synchronization to an external clock connected to CLKIN input. The external clock can be from 1 MHz to 24 MHz with 1-MHz steps. Alternatively, optional spread spectrum mode can be enabled to reduce EMI.

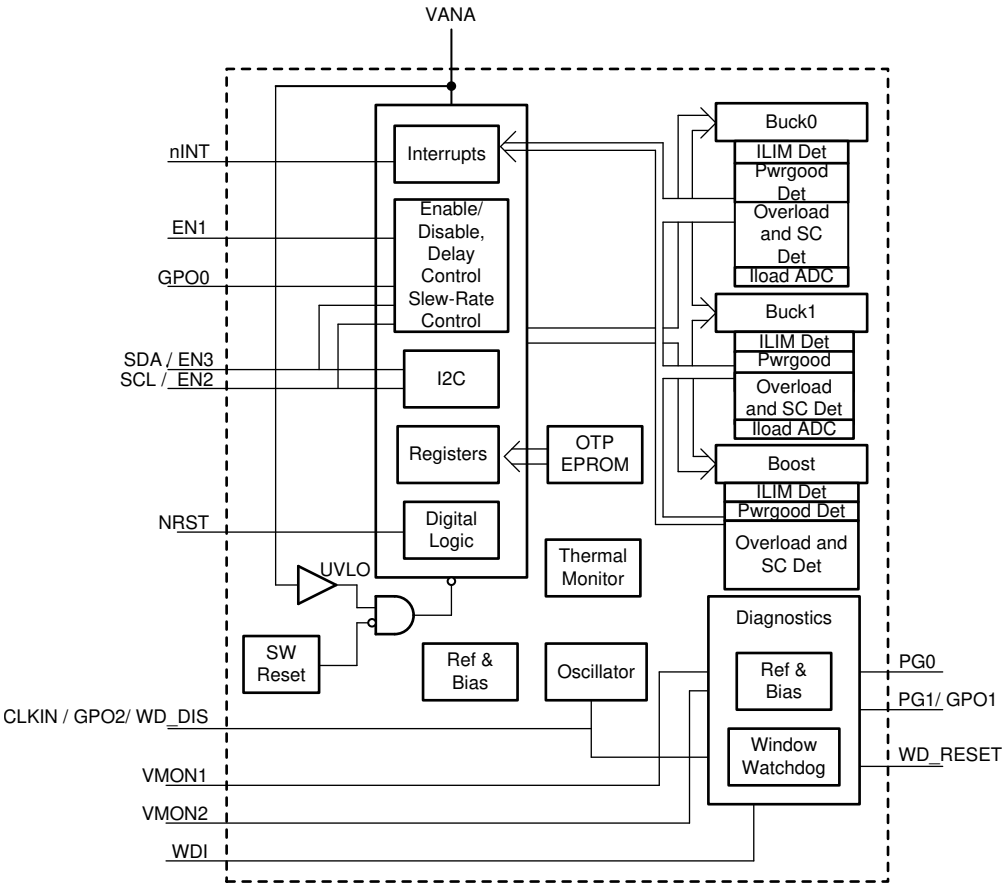
LP87702 features include diagnostics, monitoring, and protections for the devices internal and system level operation, which are the following:

- Soft start
- Input undervoltage lockout
- Programmable undervoltage or window (overvoltage and undervoltage) monitoring for the input (from VANA pin)
- Programmable undervoltage or window (overvoltage and undervoltage) monitoring for the buck and boost converter outputs
- Two inputs (VMONx) with programmable undervoltage or window (overvoltage and undervoltage) thresholds, for monitoring external rails in the system
- One dedicated power-good output (PG0) to which selected monitoring signals can be combined
- Second programmable power-good output (PG1), multiplexed with general purpose output (GPO1)
- Power good flags with maskable interrupt
- Programmable window watchdog
- Buck and boost converter overload detection
- Thermal warning with two selectable thresholds
- Thermal shutdown

LP87702 control interface:

- Up to three enable inputs (EN1, EN2, and EN3) with programmable power-up or power-down sequence control
- Optional I2C (multiplexed with EN2 and EN3 inputs)
- Interrupt signal (nINT) to host
- Reset input (NRST)
- One dedicated general purpose output (GPO0)
- Watchdog disable WD_DIS, multiplexed with CLKIN/GPO2

7.2 Functional Block Diagram



7.3 Feature Descriptions

7.3.1 Step-Down DC/DC Converters

7.3.1.1 Overview

The LP87702 includes two high-efficiency step-down DC/DC converters. The buck converters deliver 0.7-V to 3.36-V regulated voltage rails from 2.8-V to 5.5-V input-supply voltage. The converters are designed for flexibility; most of the functions are programmable, thus optimizing the converter operation for each application:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PWM or PFM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection PG0 or PG1
- Average output current sensing (for PFM entry and load current measurement)

Some of the key parameters that can be programmed through the registers (with default values set by OTP bits):

- Output voltage
- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays with ENx pin control

There are two modes of operation for the buck converters, depending on the output current required: pulse width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 520 mA or higher. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load currents. When buck is disabled, buck output is isolated from the input voltage rail. Output has an optional pulldown resistor.

Figure 7-1 shows a block diagram of a single buck converter.

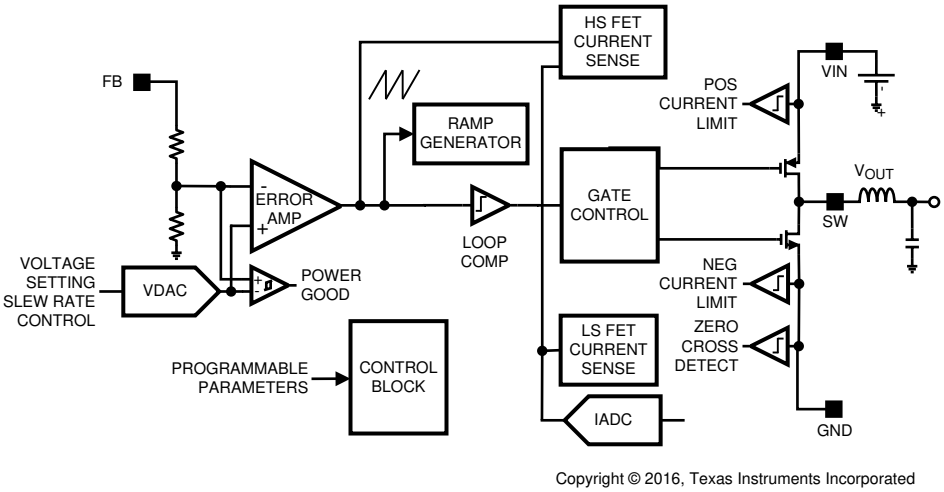


Figure 7-1. Detailed Block Diagram Showing One Buck Converter

7.3.1.2 Transition Between PWM and PFM Modes

The LP87702 buck converter operates in PWM mode at load current of about 520 mA or higher. The device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation) at lighter load current levels. A high efficiency is achieved over a wide output-load current range by combining the PFM and the PWM modes.

7.3.1.3 Buck Converter Load Current Measurement

Buck load current can be monitored through the I^2C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT bit in the SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The converter is forced to PWM mode during the measurement. The measurement sequence is 50 µs long at maximum. LP87702 can be configured to give out an I_MEAS_INT interrupt in the INT_TOP_1 register after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_MEAS_MASK bit in TOP_MASK_1 register. The measurement result can be read from I_LOAD_1 and I_LOAD_2 registers. The buck converter load current measurement result is 9-bit wide, with 8 LSB bits stored in I_LOAD_1 register and 1 MSB bit stored in I_LOAD_2 register. The single bit resolution is 20 mA, with a maximum load current value of 10.22 A.

7.3.2 Boost Converter

The LP87702 device integrates a boost converter with programmable output voltage from 4.9 V to 5.2 V in 0.1 V steps, and input voltage range from 2.8 V to 4 V. The boost converter has flexibility to support wide range of application conditions:

- Forced PWM operation
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection to PG0 and PG1 or both

The following parameters can be programmed through the registers, with default values set by the OTP bits (unless otherwise noted):

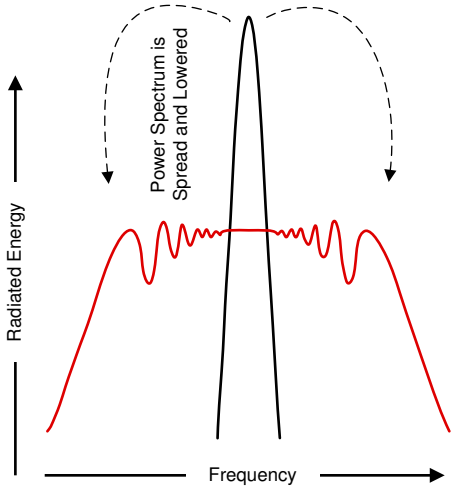
- Output voltage level (BOOST_VSET)
- Switch current limit (BOOST_ILIM)
- Enable and disable delays when ENx pin control is used (BOOST_DELAY register)
- Output pulldown resistor enable or disable when boost is disabled (BOOST_RDIS_EN bit, discharge is enabled by default)
- Output voltage monitoring enable or disable and monitoring window thresholds

The boost converter operates in forced PWM mode with fixed switching frequency across all load currents. When boost is disabled, boost output is isolated from the input voltage rail.

Boost converter supports an alternative operating mode as a bypass or load switch, with input voltage range from 4.5 V to 5.5 V. Operating mode is selected in OTP and is fixed; changing the mode on-the-fly is not supported.

7.3.3 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP87702 device supports the spread-spectrum switching frequency modulation mode that is register controlled. This mode minimizes the need for output filters, ferrite beads, or chokes. The switching frequency varies between 0.85 × f_{SW} and f_{SW} in spread spectrum mode, where f_{SW} is switching the frequency selected in the OTP. Figure 7-2 shows how the spread spectrum modulation reduces conducted and radiated emissions by the converter and associated passive components and PCB traces. This feature is available only when internal RC oscillator is used (EN_PLL is 0 in PLL_CTRL register) and it is enabled with the EN_SPREAD_SPEC bit in CONFIG register, and it affects both buck converters and the boost converter.



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP87702 spreads that energy over a large bandwidth.

Figure 7-2. Spread Spectrum Modulation

7.3.4 Sync Clock Functionality

The LP87702 device contains a CLKIN input to synchronize buck and boost converters' switching clock with the external clock. Figure 7-3 shows the block diagram of the clocking and PLL module. Table 7-2 shows how the external clock is selected and interrupt is generated depending on the EN_PLL bit in PLL_CTRL register and the external clock availability. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK_1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits in PLL_CTRL register and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection.

The SYNC_CLK_INT interrupt in INT_TOP_1 register is also generated in cases the external clock is expected but it is not available. These cases are Startup (Read OTP-to-standby transition) when EN_PLL = 1 and buck or boost converter is enabled (standby-to-active transition) when EN_PLL = 1.

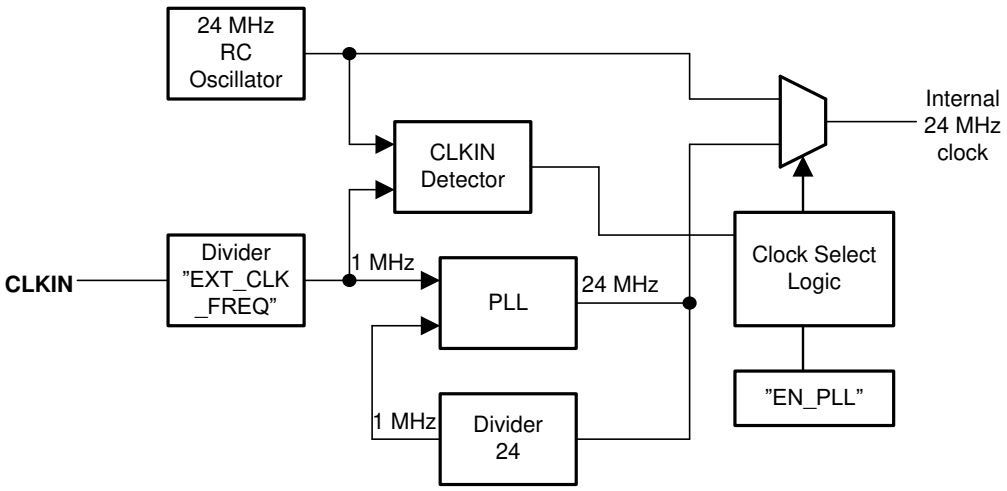


Figure 7-3. Clock and PLL Module

Table 7-2. PLL Operation

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC
STANDBY	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available
ACTIVE	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available

7.3.5 Power-Up

The power-up sequence for the LP87702 is as follows:

- VANA (and VIN_Bx) reach minimum recommended levels (V_{VANA} > $VANA_{UVLO}$).
- Driving the NRST input high initiates OTP read and enables the system I/O interface. Minimum delay from the NRST reset input rising edge to I2C write or read access is 1.2 ms.
- Device enters STANDBY mode. Watchdog operation starts.
- The host can change the default register setting by I^2C if needed.
- The converters can be enabled or disabled and the GPOx signals can be controlled by ENx pins and by I^2C interface.

7.3.6 Buck and Boost Control

7.3.6.1 Enabling and Disabling Converters

The buck converters can be enabled when the device is in STANDBY or ACTIVE state. There are two ways to enable and disable the buck converters:

- Using BUCKx_EN bit in BUCKx_CTRL_1 register (BUCKx_EN_PIN_CTRL bit is 00 in BUCKx_CTRL_1 register)
- Using ENx control pin (BUCKx_EN bit is 1 in BUCKx_CTRL_1 register *and* BUCKx_EN_PIN_CTRL bit is not 00 in BUCKx_CTRL_1 register)

Similarly there are two ways to enable and disable the boost converter:

- Using BOOST_EN bit in BOOST_CTRL register (BOOST_EN_PIN_CTRL bit is 0 in BOOST_CTRL register)
- Using ENx control pin (BOOST_EN bit is 1 in BOOST_CTRL register *and* BOOST_EN_PIN_CTRL bit is not 00 in BOOST_CTRL register)

If the ENx control pin is used to enable and disable, then the delay from the control signal rising edge to start-up is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_STARTUP_DELAY[3:0] bits in BOOST_DELAY register. The delay from falling edge of control signal to shutdown is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_SHUTDOWN_DELAY[3:0] bits in BOOST_DELAY register. The delays are valid only when ENx pin control is used, not when converters are enabled by I^2C write to BUCKx_EN and BOOST_EN bits.

The control of the converters (with 0-ms delays) is shown in Table 7-3.

Table 7-3. Converter Control

	BUCKx_EN / BOOST_EN	BUCKx_EN_PIN_CTRL / BOOST_EN_PIN_CTRL	EN1 PIN	EN2 PIN	EN3 PIN	BUCKx OUTPUT VOLTAGE / BOOST OUTPUT VOLTAGE
Enable or disable control with BUCKx_EN/ BOOST_EN bit	0	Don't Care	Don't Care	Don't Care	Don't Care	Disabled
	1	00	Don't Care	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable or disable control with EN1 pin	1	01	Low	Don't Care	Don't Care	Disabled
	1	01	High	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN2 pin	1	10	Don't Care	Low	Don't Care	Disabled
	1	10	Don't Care	High	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable or disable control with EN3 pin	1	11	Don't Care	Don't Care	Low	Disabled
	1	11	Don't Care	Don't Care	High	BUCKx_VSET[7:0] / BOOST_VSET[1:0]

Figure 7-4 shows how the BUCKx converter is enabled by an ENx pin or by I^2C write access. The soft-start circuit limits the in-rush current during start-up. The output voltage increase rate is typically 30 mV/µsec during soft start. The output voltage becomes slew-rate controlled when the output voltage rises to 0.35-V level. If there is a short circuit at the output and the output voltage does not increase above a 0.35-V level in 1 ms, the converter is disabled, and interrupt is set. When the output voltage rises above the undervoltage power-good threshold level the BUCKx_PG_INT interrupt flag in the INT_BUCK register is set.

Power-good thresholds are defined by BUCKx_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection. The powergood interrupt flag can be masked using the BUCKx_PGR_MASK bit in the BUCK_MASK register when reaching the valid output voltage. The power-good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx_PGF_MASK bit in BUCK_MASK register. When the window monitoring (under and overvoltage monitoring) is selected, the mask bits apply when voltage is crossing either threshold. A BUCKx_PG_STAT bit in BUCK_STAT register shows always the validity of the output voltage; '1' means valid, and '0' means invalid output voltage.

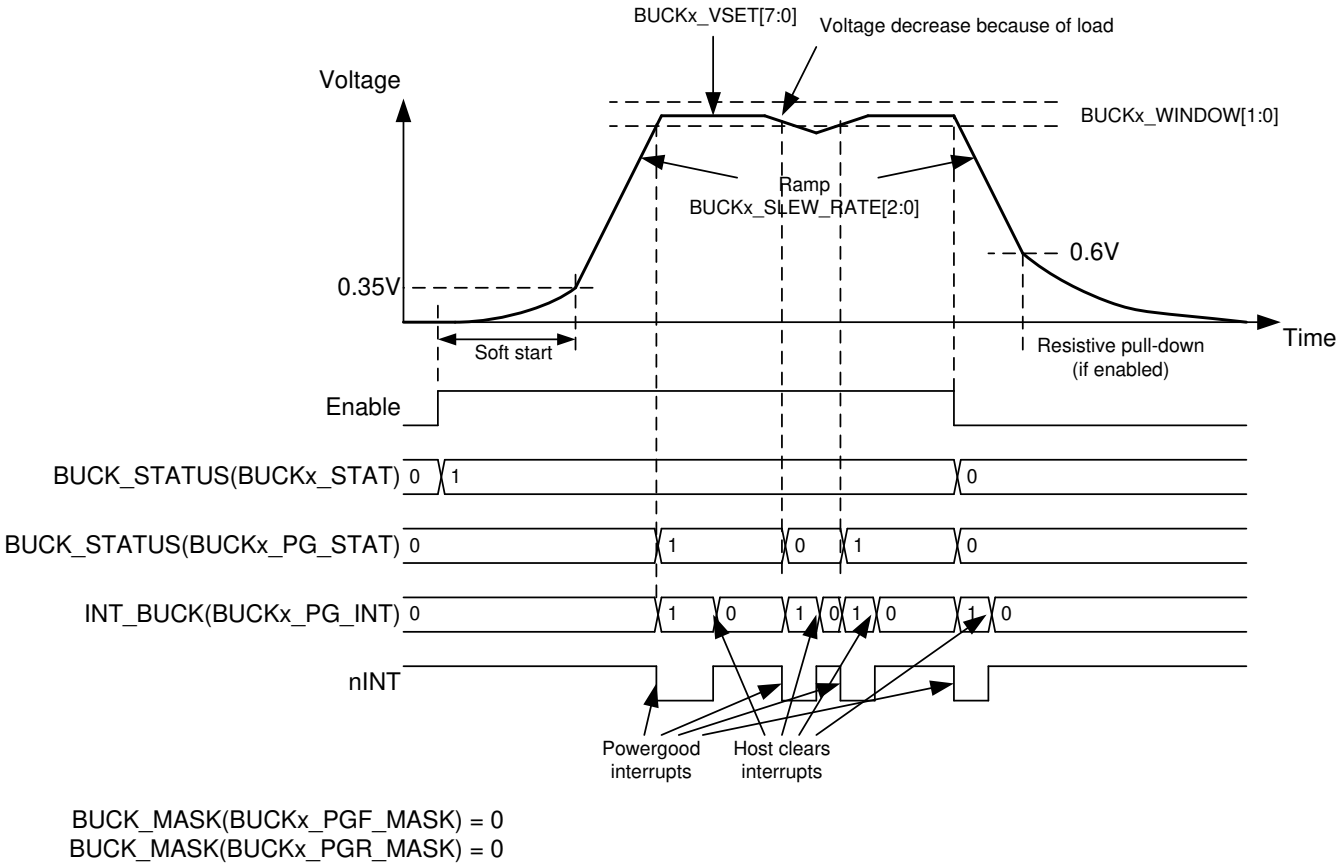


Figure 7-4. Buck Converter Enable and Disable

Figure 7-5 shows how the boost converter is enabled by an ENx pin or by I^{2}C write access. The soft-start circuit limits the in-rush current during start-up. The output voltage increase rate is less than 100 mV/µsec during soft start. If there is a short circuit at the output and the output voltage does not reach the input voltage level in 1 ms, the converter is disabled, and the interrupt is set. When the output voltage reaches the power-good threshold level, the BOOST_PG_INT interrupt flag in INT_BOOST register is set.

Power-good thresholds are defined by BOOST_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid boost output voltage, either undervoltage detection or undervoltage and overvoltage detection. The power-good interrupt flag, when reaching valid output voltage, can be masked using BOOST_PGR_MASK bit in BOOST_MASK register. The power-good interrupt flag can also be generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by the BOOST_PGF_MASK bit in BOOST_MASK register. A BOOST_PG_STAT bit in the BOOST_STAT register always shows the validity of the output voltage; '1' means valid and '0' means invalid output voltage.

The ENx input pins have integrated pulldown resistors. The pulldown resistors are enabled by default and host can disable those with ENx_PD bits in CONFIG register.

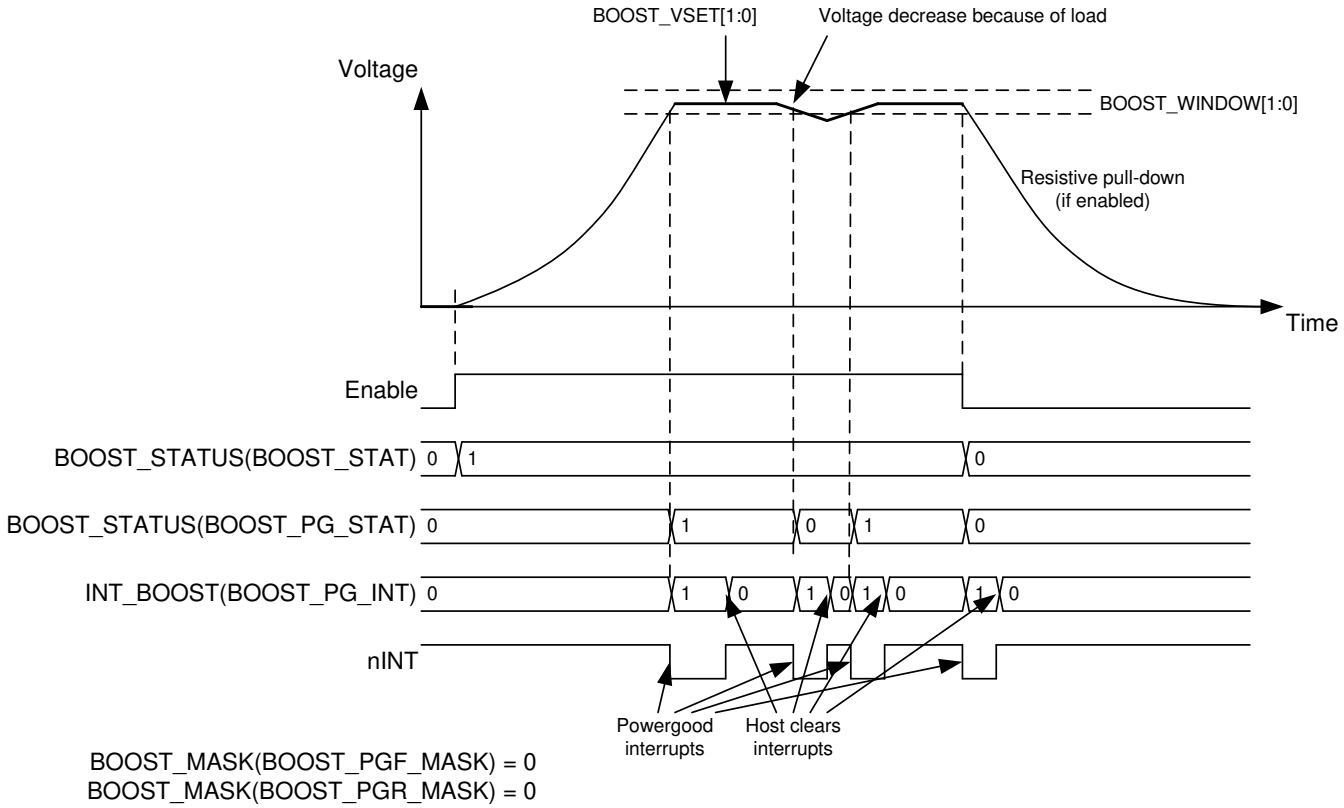


Figure 7-5. Boost Converter Enable and Disable

7.3.6.2 Changing Buck Output Voltage

The output voltage of BUCKx converter can be changed by writing to the BUCKx_VOUT register. The voltage change for buck converter is always slew-rate controlled, and the slew-rate is defined by the BUCKx_SLEW_RATE[2:0] bits in BUCKx_CTRL_2 register. The forced PWM mode is used automatically during a voltage change. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx_FPWM bit.

Figure 7-6 shows the voltage change and power-good interrupts.

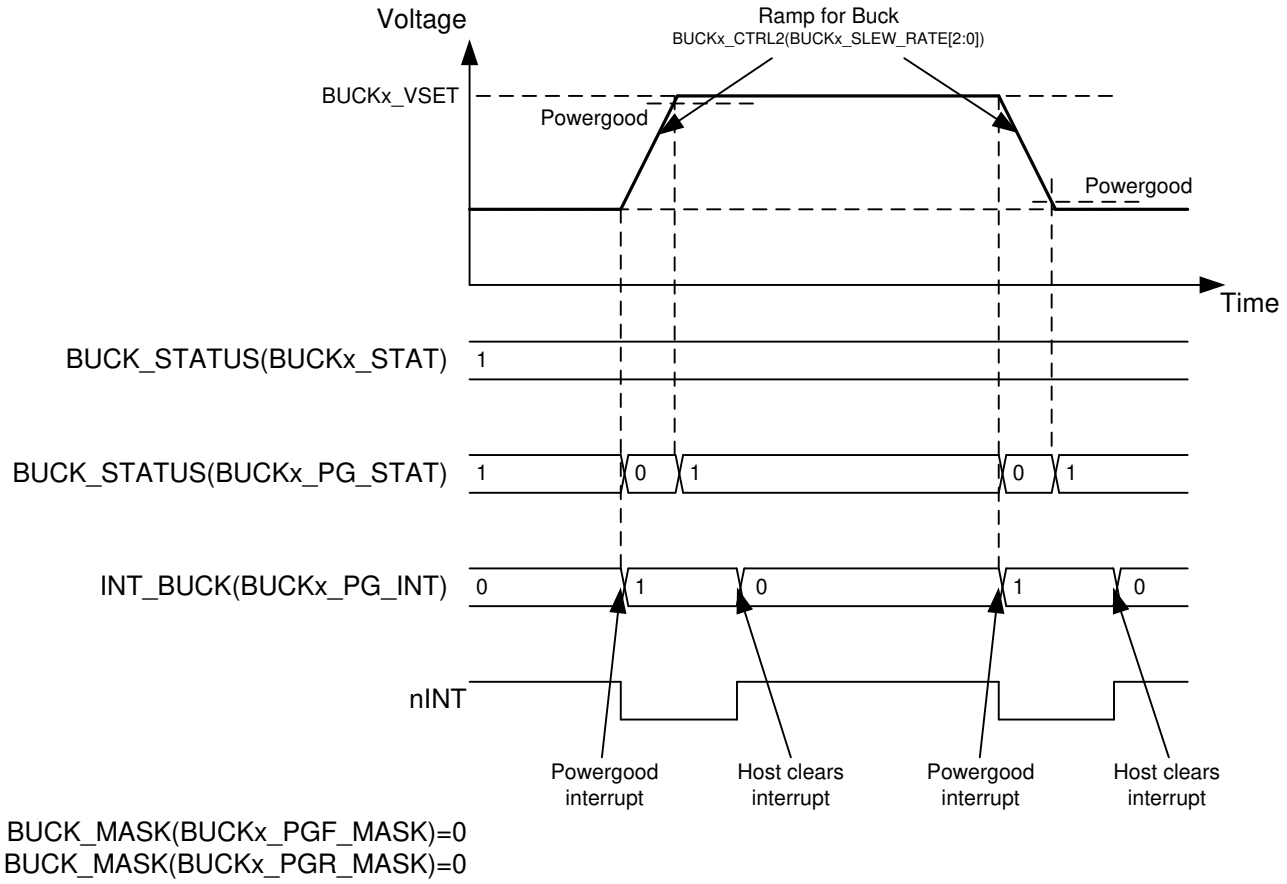


Figure 7-6. Buck Output Voltage Change

7.3.7 Enable and Disable Sequences

The LP87702 device supports programmable start-up and shutdown sequencing. An enable control signal is used to initiate the start-up sequence and to turn off the device according to the programmed shutdown sequence. Up to three enable inputs are available: EN1 is a dedicated enable input; EN2 and EN3 are multiplexed with I2C interface. The buck converter is selected for sequence control with:

- BUCKx_CTRL_1(BUCKx_EN) = 1
- BUCKx_CTRL_1(BUCKx_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BUCKx_VOUT.(BUCKx_VSET[7:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BUCKx_DELAY(BUCKx_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BUCKx_DELAY(BUCKx_SHUTDOWN_DELAY[3:0])

In the same way the boost converter is selected for delayed control with:

- BOOST_CTRL(BOOST_EN) = 1
- BOOST_CTRL(BOOST_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1. EN2, or EN3 control (respectively)
- BOOST_CTRL(BOOST_VSET[2:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the converter enable is set by BOOST_DELAY(BOOST_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the converter disable is set by BOOST_DELAY(BOOST_SHUTDOWN_DELAY[3:0])

An example of start-up and shutdown sequences for buck converters are shown in Figure 7-7. The start-up and shutdown delays for Buck0 converter are 1 ms and 4 ms and for Buck1 converter 3 ms and 1 ms. The delay settings are used only for enable or disable control with the EN signal.

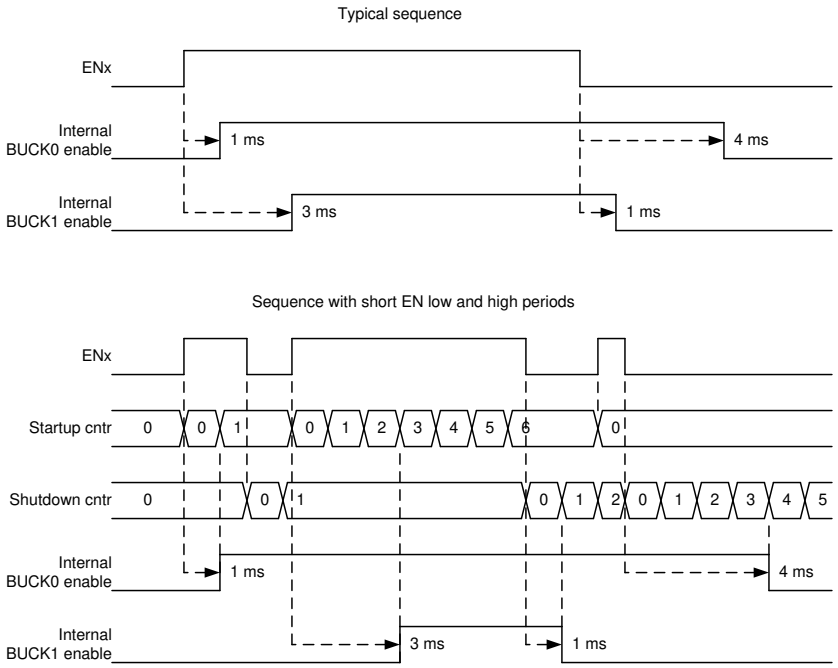


Figure 7-7. Start-up and Shutdown Sequencing Example

7.3.8 Window Watchdog

Figure 7-8 shows the LP87702 watchdog's operation (for an example, when the ENx pin is used for controlling power sequence and ENx pin is active).

WDI is the watchdog function input pin, and WD_RESET is the reset output. The WDI pin needs pulsed within a certain timing window to avoid a watchdog expiration. The minimum pulse width is 100 µs. The watchdog expiration always causes a reset pulse at WD_RESET output, otherwise the device behavior after watchdog expiration is programmable. WD_RESET output polarity and mode, push-pull or open drain, are also programmable.

Watchdog default settings are read from OTP during device start-up. Default settings in WD_CTRL_1 and WD_CTRL_2 register can be over-written through the I2C (as long as WD_LOCK bit is not set to 1). Writing WD_LOCK = 1 in WD_CTRL_2 register locks watchdog settings until NRST input is driven low, power cycle or register reset by SW_RESET.

Table 7-4 shows how the long open, close, and open window periods are independently programmable. The watchdog enters the WD Reset state when the long open or open window expires before the WDI input is received. Also, the watchdog enters the WD Reset when the WDI is received during close window. Long open period can be extended by a I2C write to WD_CTRL_1 or WD_CTRL_2 register; the register access initializes the long open counter and the long open period restarts (except in Stop mode).

LP87702 behavior after WD expiration is programmable:

- When WD_RESET_CNTR_SEL = 00, system restart is disabled and converters are maintained ON. WD_RESET pin is active for 10 ms. Watchdog returns to Long Open mode.
- When WD_RESET_CNTR_SEL = 01 (restart after first reset pulse), LP87702 performs shutdown sequence followed by start-up sequence so the converters are disabled and re-enabled according to the OTP programmed sequences. The device reloads OTP defaults when WD_EN_OTP_READ = 1 during start-up. Settings valid before shutdown are maintained when the WD_EN_OTP_READ = 0. WD_RESET output pin is active for a period of (10 ms + maximum shutdown delay). Maximum shutdown delay can be selected as 7.5

ms (SHUTDOWN_DELAY_SEL = 0) or 15 ms (SHUTDOWN_DELAY_SEL = 1). After the restart watchdog returns to Long Open mode.

- The status bit (WD_SYSTEM_RESTART_FLAG) is set to indicate that a system restart has happened. The status can be cleared by writing *1* to WD_CLR_SYSTEM_RESTART_FLAG. WD_RESET_CNTR_SEL can be set to 10 or 11 to select restart after 2 or 4 WD expirations, respectively. The current status of the reset counter is available in WD_RESET_CNTR_STATUS. The reset counter can be cleared by writing WD_CLR_RESET_CNTR to 1.

Watchdog settings in WD_CTRL_1 and WD_CTRL_2 registers are locked by setting the WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK = 1.

Description above is for a case where ENx pin is used for controlling power sequence and ENx pin is active. Watchdog behavior can be slightly different depending on the OTP settings and the ENx pin state, which follows:

- When the ENx pin is used for controlling the power sequence and the ENx pin is not active, the shutdown sequence cannot be performed. WD_RESET pulse length is fixed 31 ms.
- There is no OTP defined power sequence when the ENx pins are not used for power sequence control, and all converters and GPOs are enabled through the I2C. WD expiration does not cause a converter disable or enable sequence even when the OTP settings for the watchdog enable restart. In this case WD_RESET pulse is 11 ms.

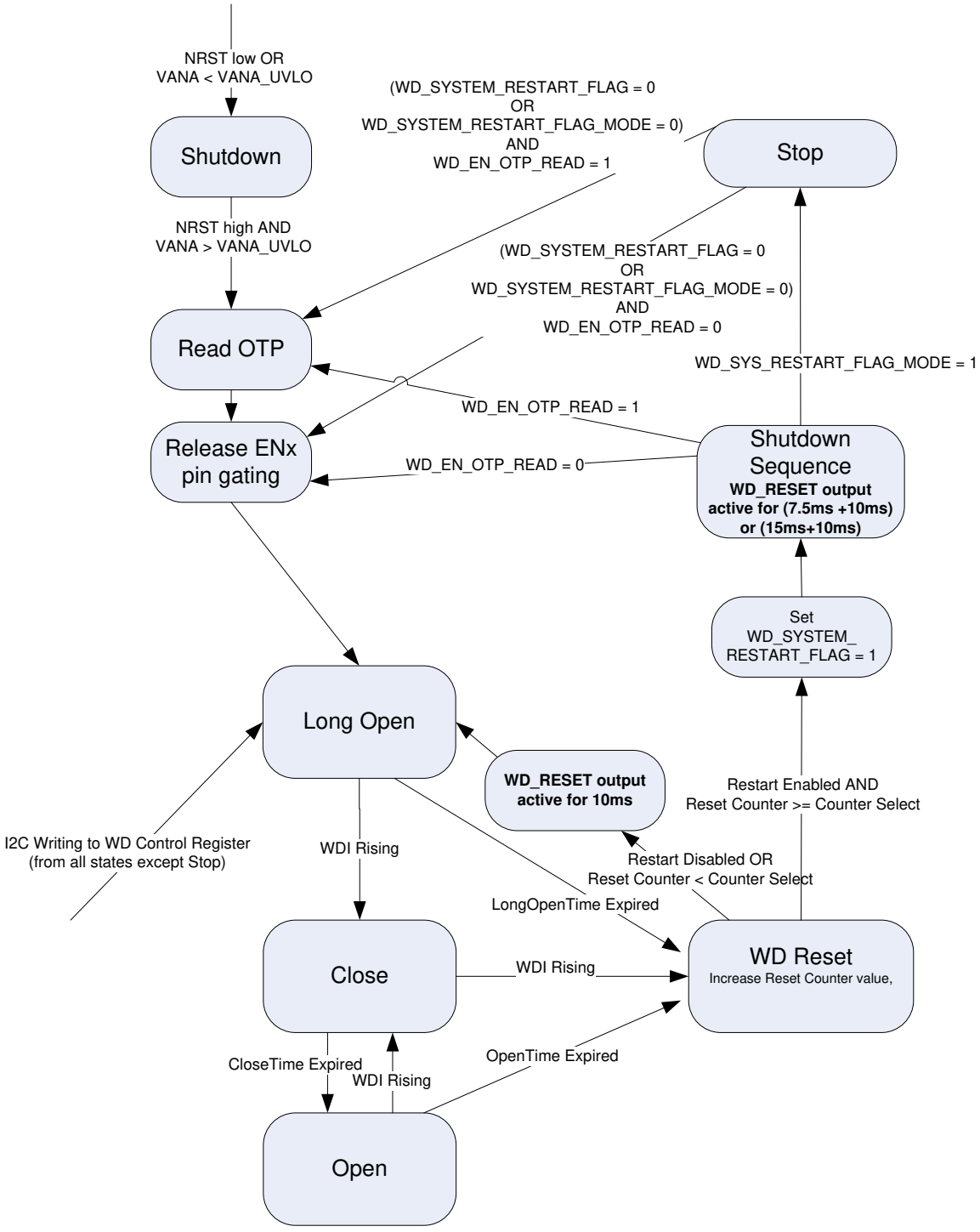


Figure 7-8. Watchdog Operation

Table 7-4. Watchdog Window Periods

CONTROL BIT	DEFAULT	VALUES
WD_LONG_OPEN_TIME	OTP	00 – 200 ms 01 – 600 ms 10 – 2000 ms 11 – 5000 ms
WD_CLOSE_TIME	OTP	00 – 10 ms 01 – 20 ms 10 – 50 ms 11 – 100 ms

7.3.9 Device Reset Scenarios

There are four reset methods implemented on the LP87702:

- Software reset with the SW_RESET bit in the RESET register
- NRST input signal low
- Undervoltage lockout (UVLO) reset from VANA supply
- Watchdog expiration (depending on the watchdog settings)

A SW reset occurs when the SW_RESET bit is set to 1. The bit is automatically cleared after writing. Figure 7-14shows how this event disables all the converters immediately, drives GPO signals low, resets all the register bits to the default values and the OTP bits are loaded. I^2C interface is not reset during a software reset. The host must wait at least 1.2 ms after writing SW reset until making a new I2C read or write to the device.

If VANA supply voltage falls below the UVLO threshold level or the NRST signal is set low, then all the converters are disabled immediately, the GPOx signals are driven low, and all the register bits are reset to the default values. When the VANA supply voltage rises above the UVLO threshold level and the NRST signal rises above the threshold level, the OTP bits are loaded to the registers and a start-up is initiated according to the register settings. The host must wait at least 1.2 ms before reading or writing to the I2C interface.

Depending on the watchdog settings, the watchdog expiration can reset the device to the OTP default values.

7.3.10 Diagnostics and Protection Features

The LP87702 provides four levels of protection features:

- Input and output voltage information. Non-valid voltage sets interrupt or PGx signal:
  - Validity of the output voltage of BUCK or BOOST converters
  - Validity of VANA, VMON1, and VMON2 input voltages
- Warnings causing interrupt:
  - Peak current limit detection in BUCK or BOOST converters
  - Thermal warning
- Protection events which are disabling the converters:
  - Short-circuit and overload protection for BUCK and BOOST converters
  - Input overvoltage protection ($VANA_{OVP}$)
  - Watchdog expiration (optional, depends on the watchdog settings)
  - Thermal shutdown
- Protection events which are causing the device to shutdown:
  - Undervoltage lockout ($VANA_{UVLO}$)
- Protections not causing interrupt or converter disable:
  - Negative current limit detection in the BUCK or BOOST converters

7.3.10.1 Voltage Monitorings

The LP87702 device has programmable voltage monitoring for the BUCKx and BOOST converter output voltages and for VANA, VMON1, and VMON2 inputs. Monitoring of each signal is independently enabled in the PGOOD_CTRL register. Voltage monitoring can be under-voltage monitoring only (PGOOD_WINDOW = 0) or overvoltage and undervoltage monitoring (PGOOD_WINDOW = 1). This selection is common for all

enabled monitorings. *Section 7.3.10.3*describes how the enabled monitoring signals are combined to generate power-good (PG0 and PG1) and interrupts. Monitoring comparators have a dedicated reference and bias block, which is independent of the main reference and bias block.

Nominal level for the output voltage of BUCKx converter is set with BUCKx_VSET in the BUCKx_VOUT register. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BUCKx_WINDOW as ± 30 mV, ± 50 mV, ± 70 mV or ± 90 mV. Nominal level for the output voltage of the BOOST converter is set with BOOST_VSET in the BOOST_CTRL register. Available levels are 4.9 V, 5 V, 5.1 V, and 5.2 V. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BOOST_WINDOW as ± 2%, ± 4%, ± 6% or ± 8%. Converter monitoring window selection bits are in the PGOOD_LEVEL_3 register.

Input voltage of LP87702 is monitored at the VANA pin. Nominal level can be selected as 3.3 V or 5 V with the VANA_THRESHOLD bit. Overvoltage and undervoltage detection levels are selected with VANA_WINDOW as (nominal). VANA_THRESHOLD and VANA_WINDOW are set in the PGOOD_LEVEL_2 register.

VMON1 and VMON2 inputs can be used for monitoring external rails in the system. VMONx settings are defined in the PGOOD_LEVEL_1 and PGOOD_LEVEL_2 registers. Nominal value for the input level of VMONx is selected with VMONx_THRESHOLD, between 0.65 V to 1.8 V. Higher voltage levels or levels not directly supported can be monitored using an external resistor divider. In this case VMONx_THRESHOLD must be set as 0.65 V to have a high-impedance input, and the resistor divider must scale the monitored level down to 0.65 V at the VMONx pin. Overvoltage and undervoltage detection levels are selected with VMONx_WINDOW as ± 2%, ± 3%, ± 4% or ± 6%.

See *Section 6* for more details on the accuracy of the monitoring windows and deglitch filtering.

7.3.10.2 Interrupts

The LP87702 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. The nINT output pin is driven high after all the flag bits and pending interrupts are cleared.

Fault detection is indicated by the RESET_REG_INT interrupt flag bit set in the INT_TOP_2 register after the start-up event.

Table 7-5. Summary of Interrupt Signals

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck current limit triggered (20-µs debounce)	No effect	BUCK_INT = 1 BUCKx_ILIM_INT = 1	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to the BUCKx_ILIM_INT bit Interrupt is not cleared if the current limit is active.
Boost current limit triggered	No effect	BOOST_INT = 1 BOOST_ILIM_INT = 1	BOOST_ILIM_MASK	BOOST_ILIM_STAT	Write 1 to the BOOST_ILIM_INT bit. Interrupt is not cleared if the current limit is active.
Buck short circuit (V_{VOUT} < 0.35V at 1 ms after enable) or Overload (V_{VOUT} decreasing below 0.35 V during operation, 1 ms debounce)	Converter disable	BUCKx_INT = 1 BUCKx_SC_INT = 1	N/A	N/A	Write 1 to the BUCKx_SC_INT bit.
Boost short circuit	Converter disable	BOOST_INT = 1 BOOST_SC_INT = 1	N/A	N/A	Write 1 to the BOOST_SC_INT bit.
Thermal warning	No effect	TDIE_WARN_INT) = 1	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to the TDIE_WARN_INT bit. Interrupt is not cleared if the temperature is above the thermal warning level.
Thermal shutdown	All converters disabled immediately and GPOx set to low	TDIE_SD_INT = 1	N/A	TDIE_SD_STAT	Write 1 to TDIE_SD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
VANA overvoltage ($VANA_{OVP}$)	All converters disabled immediately and GPOx set to low	OVP_INT	N/A	OVP_STAT	Write 1 to the OVP_INT bit. Interrupt is not cleared if the VANA voltage is above the $VANA_{OVP}$ level.
Buck power-good, output voltage becomes valid.	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit.
Buck power-good, output voltage becomes invalid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to the BUCKx_PG_INT bit.
Boost power-good, output voltage becomes valid.	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGR_MASK	BOOST_PG_STAT	Write 1 to the BOOST_PG_INT bit.
Boost power-good, output voltage becomes invalid.	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGF_MASK	BOOST_PG_STAT	Write 1 to the BOOST_PG_INT bit.
VMON1 power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGR_MASK	VMON1_PG_STAT	Write 1 to the VMON1_PG_INT bit.
VMON1 power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGF_MASK	VMON1_PG_STAT	Write 1 to the VMON1_PG_INT bit.
VMON2 power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGR_MASK	VMON2_PG_STAT	Write 1 to the VMON2_PG_INT bit.
VMON2 power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGF_MASK	VMON2_PG_STAT	Write 1 to the VMON2_PG_INT bit.
VANA power-good, input voltage becomes valid.	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGR_MASK	VANA_PG_STAT	Write 1 to the VANA_PG_INT bit.
VANA power-good, input voltage becomes invalid.	No effect	DIAG_INT = 1 VANA_PG_INT = 1	VANA_PGF_MASK	VANA_PG_STAT	Write 1 to the VANA_PG_INT bit.
External clock appears or disappears.	No effect to converters	SYNC_CLK_INT[1]	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to the SYNC_CLK_INT bit.
Load current measurement ready	No effect	I_MEAS_INT = 1	I_MEAS_MASK	N/A	Write 1 to the I_MEAS_INT bit.
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown, registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Start-up, registers reset to default values and OTP bits loaded	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit.

Table 7-5. Summary of Interrupt Signals (continued)

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Software requested reset	Immediate shutdown followed by powerup, registers reset to default values	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to the RESET_REG_INT bit.

(1) Interrupt generated during the Clock Detector operation and in case the Clock is not available when the Clock Detector is enabled.

7.3.10.3 Power-Good Information to Interrupt, PG0, and PG1 Pins

LP87702 supports both interrupt based indication of the power-good levels for various voltage settings and uses two power-good signals, PG0 and PG1. The selection of monitored signals is independent for the interrupt (nINT) and PG0 and PG1 signals. Each signal can include the following:

- The output voltage of one or both BUCKx converters
- The output voltage of the BOOST converter
- Input voltage of VANA
- Input voltage of VMON1 and VMON2 or both
- Thermal warning

Figure 7-9 shows the block diagram for power-good connections to PG0 and PG1 pins and interrupt.

Monitored signals are enabled in the PGOOD_CTRL register. Converter output voltage monitoring (not current limit monitoring) can be selected for the indication. Monitoring is enabled by the EN_PGOOD_BUCKx and EN_PGOOD_BOOST bits. The monitoring is automatically masked to prevent it from forcing PGx inactive or causing an interrupt when a converter is disabled. Also, monitoring of VANA, VMON1, and VMON2 inputs can be independently enabled through the PGOOD_CTRL register. The type of voltage monitoring for the PGx signals and nINT is selected by the PGOOD_WINDOW bit. Only the undervoltage is monitored if the bit is 0 and the undervoltage and overvoltage are monitored if the bit is 1. See *Section 7.3.10.1* for voltage monitoring thresholds.

Monitoring interrupts from all the output rails, input rails, and thermal warning are combined to the nINT pin. Dedicated mask bits are used to select which interrupts control the state of the nINT pin. See Table 7-5 for summary of the interrupts, mask bits, and interrupt clearing.

Similarly, enabled monitoring signals from all the output rails, input rails, and thermal warning are combined to PG0 and PG1 output pins. Register bits (SEL_PGx_x in PG0_CTRL and PG1_CTRL) select which of the signals control the state of PG0 and PG1, respectively. The polarity and the output type (push-pull or open-drain) of PG0 and PG1 are selected by the PGx_POL and PGx_OD bits in the PG_CTRL register.

PGx is only *active* or *asserted* when all monitored input voltages and all output voltages of the monitored and enabled converters are within the specified tolerance of the set target value.

PGx is *inactive* or *de-asserted* if any of the monitored input voltages or output voltages of the monitored and enabled converters are outside the specified tolerance of the set target value.

When PGx_RISE_DELAY = 1, PGx is set as *active* or *asserted* with 11 ms delay from the point of time where all the enabled power resource output voltages are within the specified tolerance for each requested or programmed output voltage.

Thermal shutdown and VANA overvoltage protection events force the PGx to the default state (the PGx are driven low, assuming the PGx polarity set in the OTP is active high).

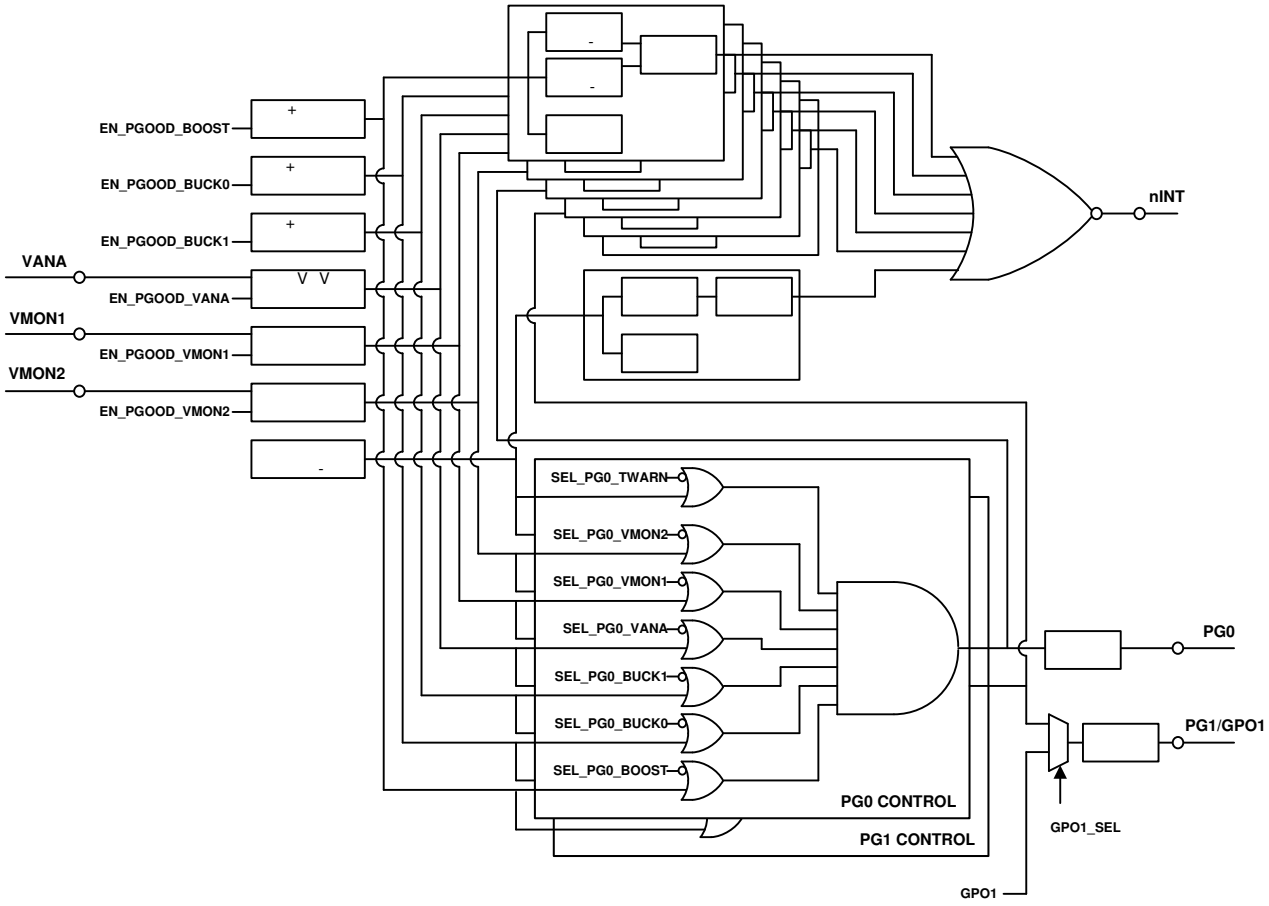


Figure 7-9. Block Diagram of Power-Good Connections

LP87702 power-good detection has two operating modes selected in the OTP: gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation. These modes are described in *Section 7.3.10.3.1* and in *Section 7.3.10.3.2*.

7.3.10.3.1 PGx Pin Gated (Unusual) Mode

The PGx signal detects unexpected or unusual situations in this mode. Mode is selected by setting the PGx_MODE bit to 0 in the PG_CTRL register.

For the gated mode of operation, the PGx behaves as follows:

- PGx is set to active or asserted state upon exiting the OTP configuration as an initial default state.
- The PGx status is *active* or *asserted* during an 800-µs gated time period from the enable activation for each enabled rail, thereby *gating-off* the status indication.
- The PGx state typically remains *active* or *asserted* for normal conditions during normal power-up sequencing and requested voltage changes.
- The PGx status could change to *inactive* or *de-asserted* after an 800-µs gated time period if any output voltage is outside of regulation range during an abnormal power-up sequencing and requested voltage changes.
- Using the gated mode of operation could allow the PGx signal to initiate an immediate power shutdown sequence if the PGx signal is wired-OR with signal connected to the EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

PGx signal is set inactive if the output voltage of a monitored buck or boost converter is invalid or the output voltage is not valid at 800 µs from the enable of the converter, which should be considered when selecting the BUCKx_SLEW_RATE setting. Keep the sum of the soft start time and slew rate controlled part of the voltage

ramp below 800 µs to avoid PGx triggering at start-up. In addition, the PGx is inactive when the invalid input voltage at VANA, VMON1, or VMON2 pin is detected.

Detected fault sets the corresponding fault bit in PG0_FAULT or in PG1_FAULT register. The detected fault must be cleared to continue the PGx monitoring. The over-voltage and thermal faults are cleared by writing 1 to the corresponding interrupt bits in INT_TOP_1 register. Converter, VMONx and VANA faults are cleared by writing 1 to the corresponding register bit in INT_BUCK, INT_BOOST, and INT_DIAG register, respectively. An example of the PGx pin operation in gated mode is shown in Figure 7-10 and the different use cases for the PGx signal operation are summarized in Table 7-6.

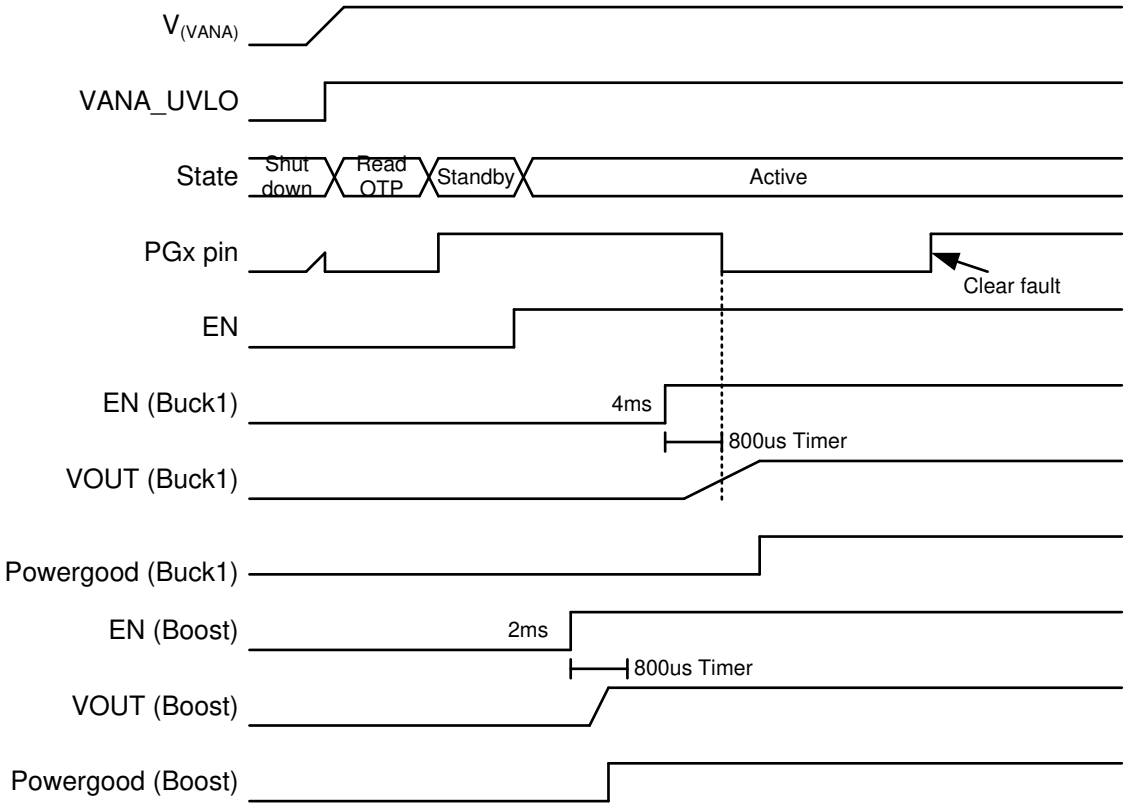


Figure 7-10. PGx Pin Operation in Gated Mode.

7.3.10.3.2 PGx Pin Operation in Continuous Mode

In this mode the PGx signal shows the validity of the requested voltages continuously. Mode is selected by setting the PGx_MODE bit to 1 in the PG_CTRL register.

For the continuous mode of operation, the PGx behaves as follows:

- PGx is set to *active* or *asserted* state upon exiting the OTP configuration as an initial default state.
- PGx is set to *inactive* or *de-asserted* as soon as the converter is enabled.
- PGx status begins indicating the output voltage regulation status immediately and continuously.
- PGx state changes between *inactive* or *deasserted* and active or asserted during power-up sequencing and requested voltage changes, depending on the output voltages being outside or inside of the regualtion ranges.

When an invalid output voltage of monitored converter is detected, the corresponding bit in the PG0_FAULT or PG1_FAULT register is set to 1 and the PGx signal becomes inactive. The PG0_FAULT and PG1_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGx signal also indicates the interrupts from VANA, VMON1, and VMON2 inputs and thermal warning and shutdown. All are cleared by clearing the interrupt bits.

The PGx signal is set inactive when the converter voltage is transitioning from one target voltage to another.

The source for the fault can be read from PGx_FAULT register when PGx signal becomes inactive. If the invalid output voltage becomes valid again the PGx signal becomes active. Thus the PGx signal shows all the time if the monitored output voltages are valid. Figure 7-11 shows an example of the PGx pin operation in continuous mode.

The PGx signal can also be configured so that it maintains the inactive state even when the monitored outputs are valid, but there are PG_FAULT_x bits pending clearance. This type of operation is selected by setting the PGOOD_FAULT_GATES_PGx bit to 1.

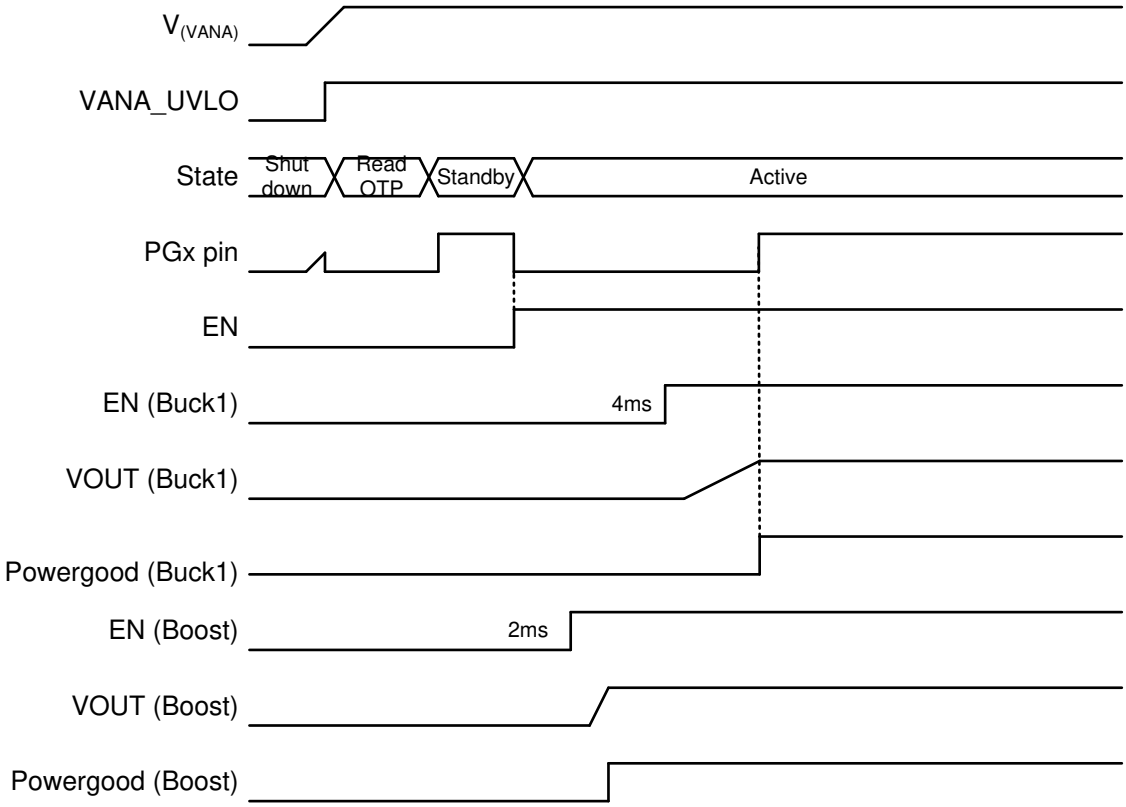


Figure 7-11. PGx Pin Operation in Continuous Mode

7.3.10.3.3 Summary of PG0, PG1 Gated, and Continuous Operating Modes

Table 7-6 summarizes the PGx behavior in different application scenarios, for the gated and continuous operating modes.

Table 7-6. PGx Operation

STATUS / USE CASE	CONDITION	PGx SIGNAL(1) (2)	
		GATED MODE PGx_MODE = 0	CONTINUOUS MODE PGx_MODE = 1
Device start-up	Until device state is STANDBY	Low	Low
Converter not selected for PGx monitoring	EN_PGOOD_x = 0	OK	OK
Converter selected for PGx monitoring and disabled by host	BUCKx_EN / BOOST_EN = 0 OR (Pin ctrl AND EN = 0)	OK	OK
Converter start-up delay ongoing	EN = 1	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage reached in 800 µs	OK	NOK
Converter start-up until valid output voltage reached	Valid output voltage not reached at 800 µs	NOK	NOK
Output voltage within window limits after start-up	Must be inside limits longer than debounce time	OK	OK
Output voltage spikes (over/ undervoltage)	If spikes are outside voltage monitoring threshold(s) longer than debounce time	NOK	NOK
Voltage setting change, output voltage ramp		OK (if new voltage reached in 800 µs) NOK after 800 µs (if new voltage not reached at 800 µs)	NOK
Output voltage within window limits after voltage change	Must be inside limits longer than debounce time	OK	OK
Converter shutdown delay ongoing		OK	OK
Buck converter disabled by host, slew-rate controlled ramp down ongoing		OK	OK
Converter disabled by host, pulldown resistor active (if selected)		OK	OK
Converter short-circuit interrupt pending (converter selected for PGx monitoring)	Faulty converter disabled by short-circuit detection BUCKx_SC_INT / BOOST_SC_INT = 1	NOK	NOK
Thermal shutdown interrupt pending	Converters disabled by thermal shutdown detection TDIE_SD_INT = 1	NOK	NOK
Input (VANA) overvoltage interrupt pending	Converters disabled by overvoltage detection OVP_INT = 1	NOK	NOK
Supply voltage below $VANA_{UVLO}$		Low	Low

(1) NOK (Not OK) means faulty situation. PGx pin is inactive if at least one NOK situation is detected.

(2) PGx pin is generated from PG_FAULT register bits and INT_TOP_1 register bits TDIE_SD_INT, OVP_INT and INT_TOP_2(RESET_REG_INT) bit.

7.3.10.4 Warning Interrupts for System Level Diagnostics

7.3.10.4.1 Output Power Limit

The buck converters have programmable output peak current limits. The limits are individually programmed for both converters with BUCKx_ILIM[2:0] bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20 µs, the LP87702 device sets the BUCKx_ILIM_INT bit and pulls the nINT pin low. The host processor can read the BUCKx_ILIM_STAT

bits to see if the converter is still in peak current regulation mode. During startup or output voltage ramp (output voltage change has been programmed) no interrupt is generated.

If the load is so high that the output voltage decreases below a 350-mV level, the LP87702 device disables the converter and sets the BUCKx_SC_INT bit. The interrupt is cleared when the host processor writes 1 to BUCKx_SC_INT bit. Figure 7-12 shows the Buck overload situation.

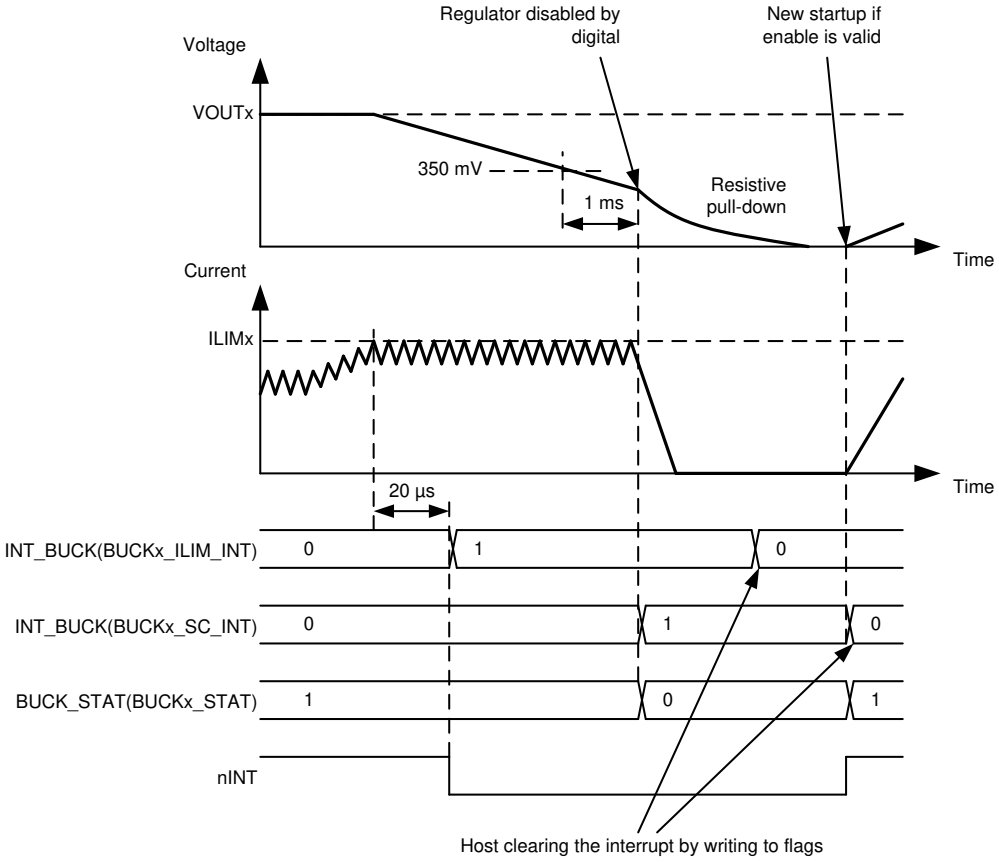


Figure 7-12. Buck Overload Situation

The boost converter has programmable output peak current limits. The limits are set with the BOOST_ILIM bits. If the load current is increased so that the current limit is triggered, the converter continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 64 µs, the LP87702 device sets the BOOST_ILIM_INT bit and pulls the nINT pin low. The host processor can read the BOOST_ILIM_STAT bits to see if the converter is still in peak current regulation mode.

If the load is so high that the output voltage decreases 150 mV (typical) below the input voltage level, then the converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, boost stops switching. After 1 ms the deglitch time boost is fully disabled and the interrupt BOOST_SC_INT bit is set. The interrupt is cleared when the host processor writes 1 to the BOOST_SC_INT bit. Figure 7-13 shows the Boost overload situation.

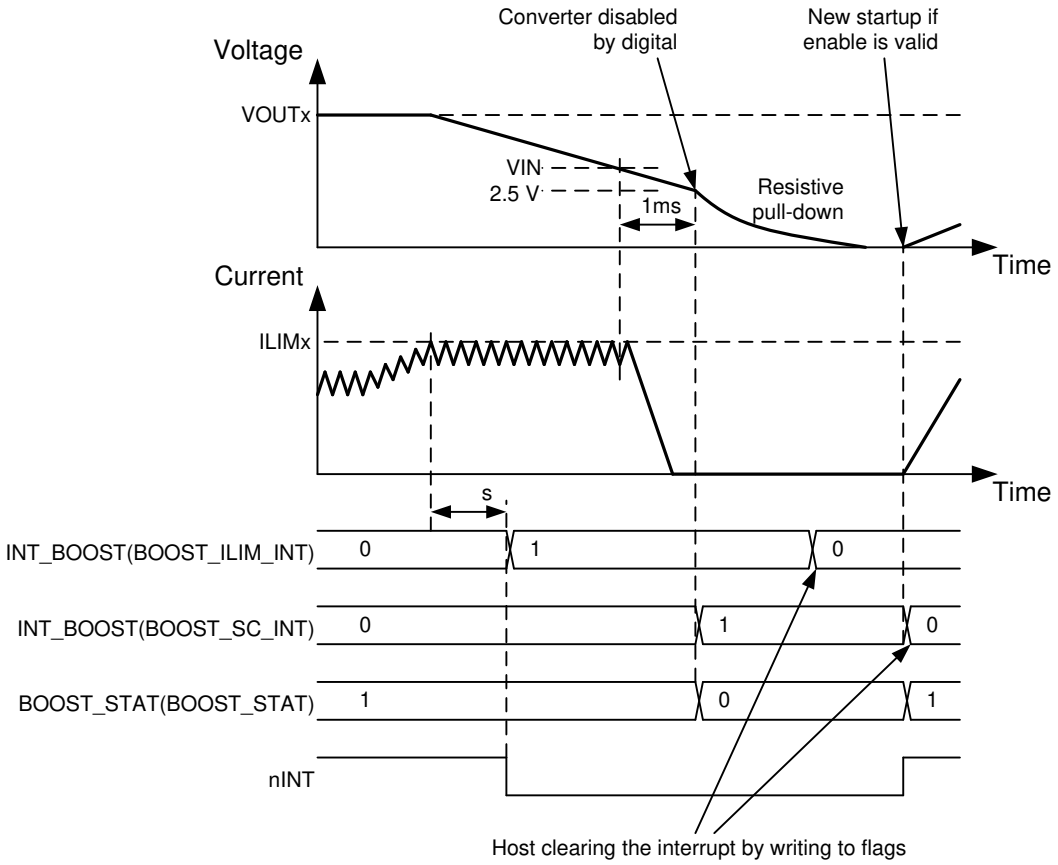


Figure 7-13. Boost Overload Situation

The buck converters have a fixed current limit for negative output peak current (I_{LIM_NEG}). When the negative coil current increases, it is limited below I_{LIM_NEG}, the converter continues to operate and no interrupt is generated. The boost converter's negative peak current limit operation is similar and the limit value is 1.4 A (typical).

7.3.10.4.2 Thermal Warning

The LP87702 device includes a protection feature against over-temperature by setting an interrupt for the host processor. The thermal warning's threshold level is selected with the TDIE_WARN_LEVEL bit.

If the LP87702 device temperature increases above the thermal warning level, the device sets the TDIE_WARN_INT bit and pulls the nINT pin low. The status of the thermal warning can be read from the TDIE_WARN_STAT bit and the interrupt is cleared by writing 1 to the TDIE_WARN_INT bit. The thermal warning interrupt can be masked by setting the TDIE_WARN_MASK bit to 1.

7.3.10.5 Protections Causing Converter Disable

If the converter is disabled because of protection or fault (short-circuit protection, thermal shutdown, overvoltage protection, or undervoltage lockout), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx_RDIS_EN and BOOST_RDIS_EN bits). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor. The pulldown resistors are active as long as the VANA voltage is above the 1.2-V level (approximately).

7.3.10.5.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87702 to protect itself and external components against short circuiting at the output or against overloading during start-up. A short-circuit at the buck converter output is detected during start-up when the output voltage is below 350 mV (typical) 1 ms after the buck converter is

enabled. The fault threshold is 150 mV (typical) below the input voltage level for boost. Boost converter is disabled if the output voltage is below the threshold level 1 ms after the boost converter is enabled.

In a similar way, the overload situation is protected during normal operation. If the feedback-pin voltage of the buck converter falls below 0.35 V and remains below the threshold level for 1 ms, the buck converter is disabled. If the output voltage of the boost converter decreases 150 mV below the input voltage level, the converter is disabled after 1 ms. If the output voltage decreases to 2.5 V, the boost is disabled immediately.

The BUCKx_SC_INT and the BUCK_INT bits are set to 1, the BUCKx_STAT bit is set to 0, and the nINT signal is pulled low in the buck converter, the short-circuit, and overload situations. The BOOST_SC_INT and the BOOST_INT bits are set to 1, the BOOST_STAT bit is set to 0, and the nINT signal is pulled low in the boost converter, short-circuit, and overload situations. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT or BOOST_SC_INT bit. The converter makes a new start-up attempt upon clearing the interrupt, if the converter is in the enabled state.

7.3.10.5.2 Overvoltage Protection

The LP87702 device monitors the input voltage from the VANA pin in the standby and active operation modes. If the input voltage rises above the $VANA_{OVP}$ voltage level, all the converters are disabled immediately (without switching ramp or shutdown delays), the pulldown resistors discharge the output voltages (BUCKx_RDIS_EN = 1 and BOOST_RDIS_EN = 1), the GPOs are set to the logic low level, the nINT signal is pulled low, the OVP_INT bit is set to 1, and BUCKx_STAT and BOOST_STAT bits are set to 0. The host processor clears the interrupt by writing 1 to the OVP_INT bit. If the input voltage is above over-voltage detection level, the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit. Converters cannot be enabled as long as the input voltage is above over-voltage detection level or the overvoltage interrupt is pending.

7.3.10.5.3 Thermal Shutdown

The LP87702 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. The converters are disabled immediately (without switching ramp or shutdown delays), the TDIE_SD_INT bit is set to 1, the nINT signal is pulled low, and the device enters STANDBY when the junction temperature exceeds around 150°C. The nINT is cleared by writing 1 to the TDIE_SD_INT bit. If the temperature is above thermal shutdown level, the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit. Converters cannot be enabled as long as the junction temperature is above the thermal shutdown level or the thermal shutdown interrupt is pending.

7.3.10.6 Protections Causing Device Power Down

7.3.10.6.1 Undervoltage Lockout

The buck and boost converters are disabled immediately (without switching ramp or without any shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the LP87702 device enters SHUTDOWN when the input voltage falls below $VANA_{UVLO}$ at the VANA pin. The device powers up to STANDBY state when the $V_{(VANA)}$ voltage is above the $VANA_{UVLO}$ threshold level.

If the reset interrupt is unmasked by default (RESET_REG_MASK = 0 in TOP_MASK_2 register), the RESET_REG_INT interrupt in the INT_TOP_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET_REG_INT bit. If the host processor reads the RESET_REG_INT flag after detecting an nINT low signal, it detects that the input supply voltage has been below the $VANA_{UVLO}$ level (or the host has requested reset with the RESET(SW_RESET) bit), and the registers are reset to the default values.

7.3.11 OTP Error Correction

LP87702 supports the OTP bit error detection and 1-bit error correction per five registers. The ECC_STATUS register bit SED is set if a single bit error was detected and corrected. DED bit is set in case two bit errors have been detected in any bank of five registers.

7.3.12 Operation of GPO Signals

The LP87702 device supports up to 3 general purpose output (GPO) signals. The GPO1 signal is multiplexed with the PG1 signal and GPO2 signal is multiplexed with the CLKIN and WD_DIS signals. The selection between signal use are set with the GPO1_SEL and GPO2_SEL bits in the GPO_CONTROL_2 register.

The type of output, either push-pull (with $V_{(VANA)}$ level) or open drain, are set with the GPO0_OD and GPO1_PG1_OD bits in the GPO_CONTROL_1 register and the GPO2_OD bit in the GPO_CONTROL_2 register.

The logic level of the GPOx pins are is set by the GPO0_OUT and GPO1_OUT bits in the GPO_CONTROL_1 register and the GPO2_OUT bit in the GPO_CONTROL_2 register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with ENx pin is selected by the GPOx_EN_PIN_CTRL bits. The delays during start-up and shutdown are set by bits in the GPOx_DELAY registers.

7.3.13 Digital Signal Filtering

The digital signals have a debounce filtering. The signal or supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

Table 7-7. Digital Signal Filtering

EVENT	SIGNAL/SUPPLY	RISING EDGE	FALLING EDGE
		LENGTH	LENGTH
Enable or Disable for BUCKx, BOOST, or GPOx	ENx	3 µs(1)	3 µs(1)
VANA undervoltage lockout	VANA	Immediate (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 µs (VANA voltage rising)	1 µs (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 µs	20 µs
Thermal shutdown	TDIE_SD_INT	20 µs	20 µs
Current limit, BUCKx		20 µs	20 µs
Current limit, BOOST		64 µs	64 µs
Overload	FB_B0, FB_B1, VOUT_BST	1 ms	N/V
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / FB_B0, FB_B1	6 µs	6 µs
PGx pin and power-good interrupt (voltage monitoring)	PG0, PG1 / VOUT_BST, VANA, VMON1, VMON2	15 µs	15 µs

(1) No glitch filtering; only synchronization.

7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN: The $V_{(VANA)}$ voltage is below the $VANA_{UVLO}$ threshold level or the NRST signal is low. All switch, reference, control, and bias circuitry of the LP87702 device are turned off.

READ OTP: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. The converters are disabled and the reference and bias circuitry of the LP87702 are enabled. The OTP bits are loaded to the registers. I2C access is not allowed during OTP read. *Section 7.3.8* shows how this also applies to the watchdog.

STANDBY: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. All registers can be read or written by the host processor through the system serial interface. Watchdog is active and the WDI input is expected to toggle to avoid watchdog expiration. The converters are disabled and the LP87702's reference, control, and bias circuitry are enabled. The converters can be enabled if needed.

ACTIVE: The main supply voltage ($V_{(VANA)}$) is above the $VANA_{UVLO}$ level and the NRST signal is high. At least one converter is enabled. All registers can be read or written by the host processor through the system's serial interface. Watchdog is active and the WDI input is expected to toggle to avoid watchdog expiration.

Figure 7-14 shows the operating modes and transitions between the modes. See *Section 7.3.8* for the window watchdog detailed operation.

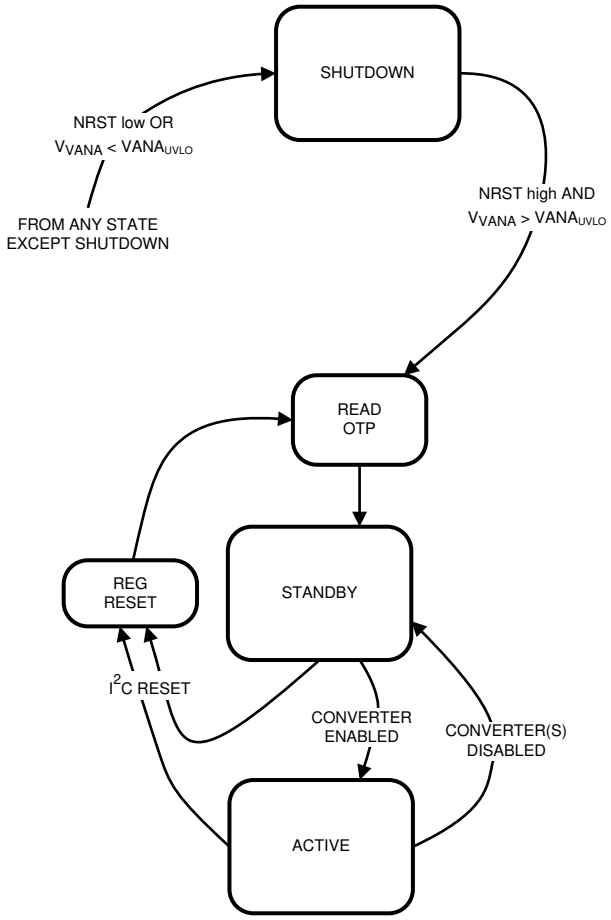


Figure 7-14. Device Operation Modes.

7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. The LP87702 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

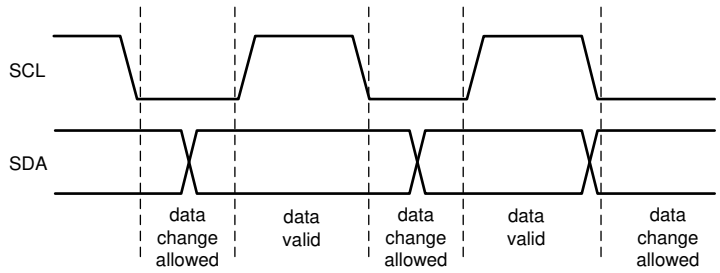


Figure 7-15. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The LP87702 is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

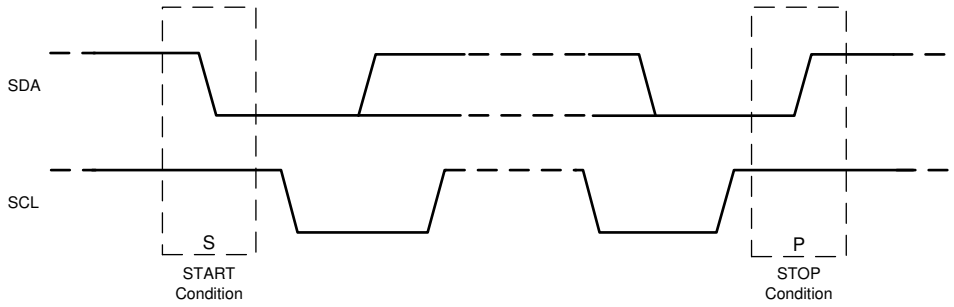


Figure 7-16. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. The I²C master can generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 7-17 shows the SDA and SCL signal timing for the I²C-Compatible Bus.

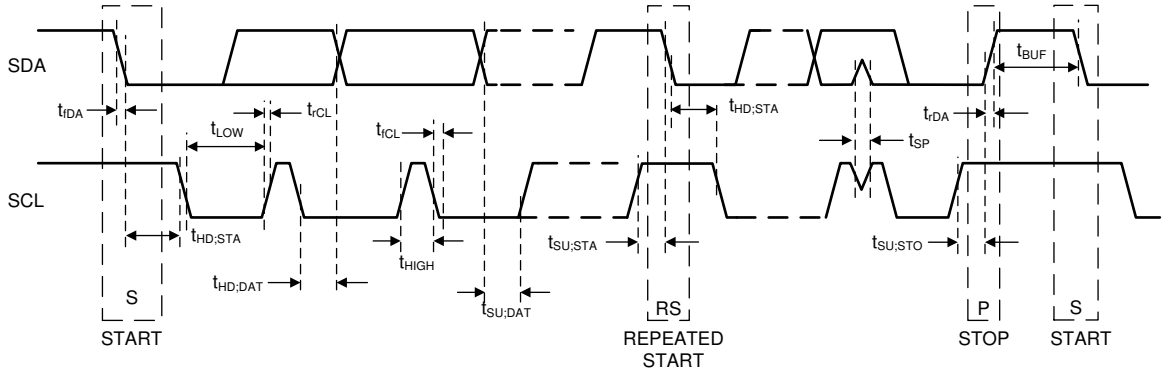


Figure 7-17. I²C-Compatible Timing

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87702 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87702 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

Note

If the $V_{(VANA)}$ voltage is below the $VANA_{UVLO}$ threshold level during I²C communication, the LP87702 device does not drive the SDA line. The ACK signal and data transfer to the master is disabled at that time.

The bus master sends a chip address after the START condition. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). A 0 indicates a WRITE and a 1 indicates a READ for the eighth bit. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

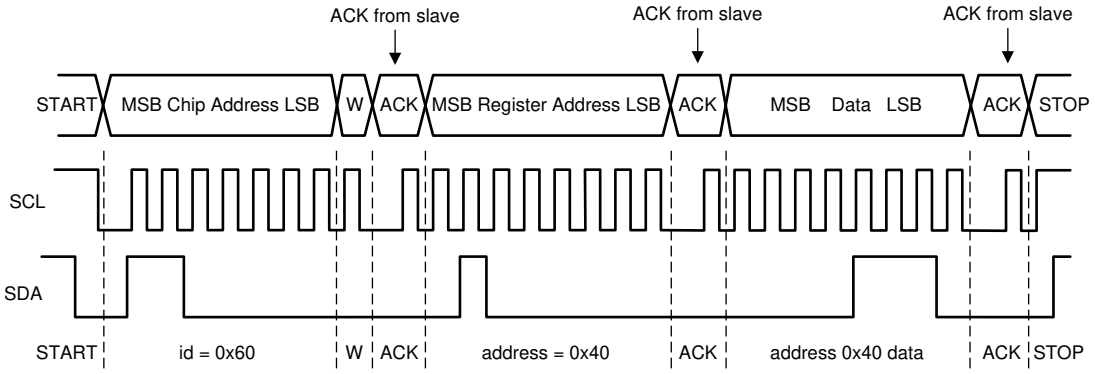
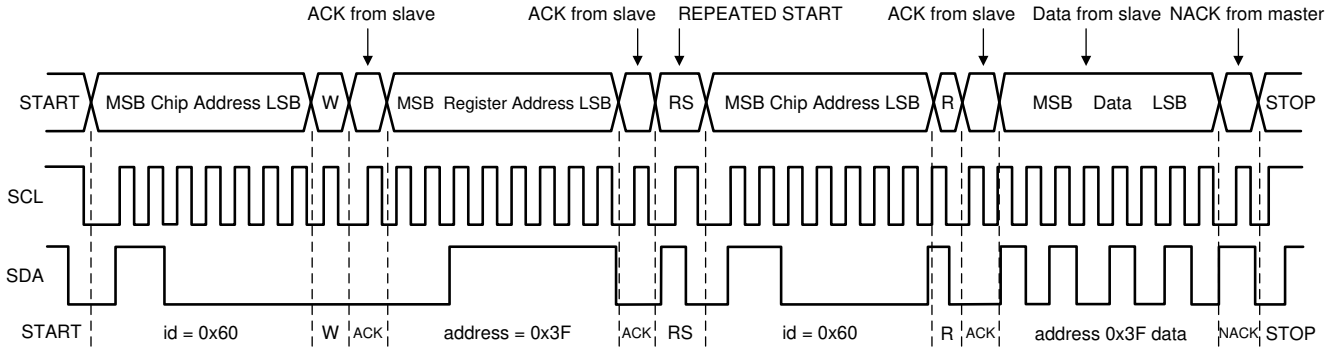


Figure 7-18. Write Cycle (w = write; SDA = 0), id = Device Address = 60Hex for LP87702

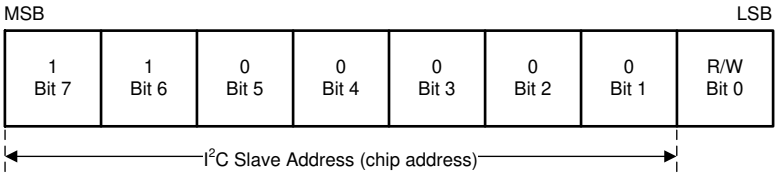


A WRITE function must precede the READ function as shown above when the READ function is accomplished.

Figure 7-19. Read Cycle (r = read; SDA = 1), id = Device Address = 60Hex for LP87702

7.5.1.4 I²C-Compatible Chip Address

The device address for the LP87702 is 0x60. After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



A. Here device address is 1100000Bin = 60Hex.

Figure 7-20. Device Address

7.5.1.5 Auto Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. The internal address index counter increments by one and the next register will be written every time an 8-bit word is sent to the LP87702. Table 7-8 below shows writing sequence to two consecutive registers. Note: the auto increment feature does not work for read.

Table 7-8. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS = 60H	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
LP87702				ACK		ACK		ACK		ACK	

7.6 Register Maps

7.6.1 Register Descriptions

The LP87702 is controlled by a set of registers through the system serial interface port. This register map describes the default values for the bits which are not read from OTP memory. The asterisk (*) marking indicates the register bits which are updated from the OTP memory during the READ OTP state. OTP values for each orderable part number are described in a separate technical reference manual TRM.

7.6.1.1 LP8770_map Registers

Table 7-9 lists the memory-mapped registers for the LP8770_map registers. All register offset addresses not listed in Table 7-9 should be considered as reserved locations and the register contents should not be modified.

Table 7-9. LP8770_MAP Registers

Offset	Acronym	Register Name	Section
0h	DEV_REV		Section 7.6.1.1.1
1h	OTP_CODE		Section 7.6.1.1.2
2h	BUCK0_CTRL_1		Section 7.6.1.1.3
3h	BUCK0_CTRL_2		Section 7.6.1.1.4
4h	BUCK1_CTRL_1		Section 7.6.1.1.5
5h	BUCK1_CTRL_2		Section 7.6.1.1.6
6h	BUCK0_VOUT		Section 7.6.1.1.7
7h	BUCK1_VOUT		Section 7.6.1.1.8
8h	BOOST_CTRL		Section 7.6.1.1.9
9h	BUCK0_DELAY		Section 7.6.1.1.10
Ah	BUCK1_DELAY		Section 7.6.1.1.11
Bh	BOOST_DELAY		Section 7.6.1.1.12
Ch	GPO0_DELAY		Section 7.6.1.1.13
Dh	GPO1_DELAY		Section 7.6.1.1.14
Eh	GPO2_DELAY		Section 7.6.1.1.15
Fh	GPO_CONTROL_1		Section 7.6.1.1.16
10h	GPO_CONTROL_2		Section 7.6.1.1.17
11h	CONFIG		Section 7.6.1.1.18
12h	PLL_CTRL		Section 7.6.1.1.19
13h	PGOOD_CTRL		Section 7.6.1.1.20
14h	PGOOD_LEVEL_1		Section 7.6.1.1.21
15h	PGOOD_LEVEL_2		Section 7.6.1.1.22
16h	PGOOD_LEVEL_3		Section 7.6.1.1.23
17h	PG_CTRL		Section 7.6.1.1.24
18h	PG0_CTRL		Section 7.6.1.1.25
19h	PG0_FAULT		Section 7.6.1.1.26
1Ah	PG1_CTRL		Section 7.6.1.1.27
1Bh	PG1_FAULT		Section 7.6.1.1.28
1Ch	WD_CTRL_1		Section 7.6.1.1.29
1Dh	WD_CTRL_2		Section 7.6.1.1.30
1Eh	WD_STATUS		Section 7.6.1.1.31
1Fh	RESET		Section 7.6.1.1.32
20h	INT_TOP_1		Section 7.6.1.1.33
21h	INT_TOP_2		Section 7.6.1.1.34
22h	INT_BUCK		Section 7.6.1.1.35

Table 7-9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
23h	INT_BOOST		Section 7.6.1.1.36
24h	INT_DIAG		Section 7.6.1.1.37
25h	TOP_STATUS		Section 7.6.1.1.38
26h	BUCK_STATUS		Section 7.6.1.1.39
27h	BOOST_STATUS		Section 7.6.1.1.40
28h	DIAG_STATUS		Section 7.6.1.1.41
29h	TOP_MASK_1		Section 7.6.1.1.42
2Ah	TOP_MASK_2		Section 7.6.1.1.43
2Bh	BUCK_MASK		Section 7.6.1.1.44
2Ch	BOOST_MASK		Section 7.6.1.1.45
2Dh	DIAG_MASK		Section 7.6.1.1.46
2Eh	SEL_I_LOAD		Section 7.6.1.1.47
2Fh	I_LOAD_2		Section 7.6.1.1.48
30h	I_LOAD_1		Section 7.6.1.1.49
31h	FREQ_SEL		Section 7.6.1.1.50
32h	BOOST_ILIM_CTRL		Section 7.6.1.1.51
33h	ECC_STATUS		Section 7.6.1.1.52
34h	WD_DIS_CTRL_CODE		Section 7.6.1.1.53
35h	WD_DIS_CONTROL		Section 7.6.1.1.54

Complex bit access types are encoded to fit into small table cells. Table 7-10 shows the codes that are used for access types in this section.

Table 7-10. LP8770_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.6.1.1.1 DEV_REV Register (Offset = 0h) [reset = 0h]

DEV_REV is shown in Figure 7-19 and described in Table 7-11.

Return to Table 7-9.

Figure 7-19. DEV_REV Register

7	6	5	4	3	2	1	0
RESERVED		DEVICE_ID					
R-0h		R-0h					

Table 7-11. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-3	DEVICE_ID	R	0h	Device specific ID code. (Default from OTP memory)

7.6.1.1.2 OTP_CODE Register (Offset = 1h) [reset = 0h]

OTP_CODE is shown in Figure 7-20 and described in Table 7-12.

Return to Table 7-9.

Figure 7-20. OTP_CODE Register

7	6	5	4	3	2	1	0
OTP_ID						OTP_REV	
R-0h						R-0h	

Table 7-12. OTP_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	OTP_ID	R	0h	Identification Code of the OTP EPROM. (Default from OTP memory)
1-0	OTP_REV	R	0h	Version number of the OTP ID. (Default from OTP memory)

7.6.1.1.3 BUCK0_CTRL_1 Register (Offset = 2h) [reset = 8h]

BUCK0_CTRL_1 is shown in Figure 7-21 and described in Table 7-13.

Return to Table 7-9.

Figure 7-21. BUCK0_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL		BUCK0_EN
R/W-0h			R/W-0h	R/W-1h	R/W-0h		R/W-0h

Table 7-13. BUCK0_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
4	BUCK0_FPWM	R/W	0h	Forces the BUCK0 converter to operate in PWM mode: 0 – Automatic transitions between PFM and PWM modes (AUTO mode). 1 – Forced to PWM operation. (Default from OTP memory)
3	BUCK0_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK0 is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.

Table 7-13. BUCK0_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	BUCK0_EN_PIN_CTRL	R/W	0h	Enable or disable control for BUCK0: 0x0 – only BUCK0_EN bit controls BUCK0 0x1 – BUCK0_EN bit AND EN1 pin control BUCK0 0x2 – BUCK0_EN bit AND EN2 pin control BUCK0 0x3 – BUCK0_EN bit AND EN3 pin control BUCK0 (Default from OTP memory)
0	BUCK0_EN	R/W	0h	Enable BUCK0 converter: 0 – BUCK0 converter is disabled 1 – BUCK0 converter is enabled. (Default from OTP memory)

7.6.1.1.4 BUCK0_CTRL_2 Register (Offset = 3h) [reset = 1Ah]

BUCK0_CTRL_2 is shown in Figure 7-22 and described in Table 7-14.

Return to Table 7-9.

Figure 7-22. BUCK0_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_ILIM			BUCK0_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

Table 7-14. BUCK0_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK0_ILIM	R/W	3h	Sets the switch peak current limit of BUCK0. Can be programmed at any time during operation: 0x0 – 1.5 A 0x1 – 2.0 A 0x2 – 2.5 A 0x3 – 3.0 A 0x4 – 3.5 A 0x5 – 4.0 A 0x6 – 4.5 A 0x7 – Reserved (Default from OTP memory)
2-0	BUCK0_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK0 converter (rising and falling edges): 0x0 – Reserved 0x1 – Reserved 0x2 – 10 mV/µs 0x3 – 7.5 mV/µs 0x4 – 3.8 mV/µs 0x5 – 1.9 mV/µs 0x6 – 0.94 mV/µs 0x7 – 0.47 mV/µs (Default from OTP memory)

7.6.1.1.5 BUCK1_CTRL_1 Register (Offset = 4h) [reset = 8h]

BUCK1_CTRL_1 is shown in Figure 7-23 and described in Table 7-15.

Return to Table 7-9.

Figure 7-23. BUCK1_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL		BUCK1_EN

Figure 7-23. BUCK1_CTRL_1 Register (continued)

R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 7-15. BUCK1_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK1_FPWM	R/W	0h	Forces the BUCK1 converter to operate in PWM mode: 0 – Automatic transitions between PFM and PWM modes (AUTO mode). 1 – Forced to PWM operation. (Default from OTP memory)
3	BUCK1_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK1 is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.
2-1	BUCK1_EN_PIN_CTRL	R/W	0h	Enable or disable control for BUCK1: 0x0 – only BUCK1_EN bit controls BUCK1 0x1 – BUCK1_EN bit AND EN1 pin control BUCK1 0x2 – BUCK1_EN bit AND EN2 pin control BUCK1 0x3 – BUCK1_EN bit AND EN3 pin control BUCK1 (Default from OTP memory)
0	BUCK1_EN	R/W	0h	Enable BUCK1 converter: 0 – BUCK1 converter is disabled 1 – BUCK1 converter is enabled. (Default from OTP memory)

7.6.1.1.6 BUCK1_CTRL_2 Register (Offset = 5h) [reset = 1Ah]

BUCK1_CTRL_2 is shown in Figure 7-24 and described in Table 7-16.

Return to Table 7-9.

Figure 7-24. BUCK1_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK1_ILIM			BUCK1_SLEW_RATE		
R/W-0h		R/W-3h			R/W-2h		

Table 7-16. BUCK1_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_ILIM	R/W	3h	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: 0x0 – 1.5 A 0x1 – 2.0 A 0x2 – 2.5 A 0x3 – 3.0 A 0x4 – 3.5 A 0x5 – 4.0 A 0x6 – 4.5 A 0x7 – Reserved (Default from OTP memory)

Table 7-16. BUCK1_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BUCK1_SLEW_RATE	R/W	2h	Sets the output voltage slew rate for BUCK1 converter (rising and falling edges): 0x0 – Reserved 0x1 – Reserved 0x2 – 10 mV/µs 0x3 – 7.5 mV/µs 0x4 – 3.8 mV/µs 0x5 – 1.9 mV/µs 0x6 – 0.94 mV/µs 0x7 – 0.47 mV/µs (Default from OTP memory)

7.6.1.1.7 BUCK0_VOUT Register (Offset = 6h) [reset = 0h]

BUCK0_VOUT is shown in Figure 7-25 and described in Table 7-17.

Return to Table 7-9.

Figure 7-25. BUCK0_VOUT Register

7	6	5	4	3	2	1	0
BUCK0_VSET							
R/W-0h							

Table 7-17. BUCK0_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK0_VSET	R/W	0h	Output voltage of BUCK0 converter: 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V – 0.73 V, 10 mV steps 0x14 – 0.7 V ... 0x17 – 0.73 V 0.73 V – 1.4 V, 5 mV steps 0x18 – 0.735 V ... 0x9D – 1.4 V 1.4 V – 3.36 V, 20 mV steps 0x9E – 1.42 V ... 0xFF – 3.36 V (Default from OTP memory)

7.6.1.1.8 BUCK1_VOUT Register (Offset = 7h) [reset = 0h]

BUCK1_VOUT is shown in Figure 7-26 and described in Table 7-18.

Return to Table 7-9.

Figure 7-26. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
BUCK1_VSET							
R/W-0h							

Table 7-18. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET	R/W	0h	Output voltage of BUCK1 converter 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V – 0.73 V, 10 mV steps 0x14 – 0.7 V ... 0x17 – 0.73 V 0.73 V – 1.4 V, 5 mV steps 0x18 – 0.735 V ... 0x9D – 1.4 V 1.4 V – 3.36 V, 20 mV steps 0x9E – 1.42 V ... 0xFF – 3.36 V (Default from OTP memory)

7.6.1.1.9 BOOST_CTRL Register (Offset = 8h) [reset = 8h]

BOOST_CTRL is shown in Figure 7-27 and described in Table 7-19.

Return to Table 7-9.

Figure 7-27. BOOST_CTRL Register

7	6	5	4	3	2	1	0
BOOST_VSET		RESERVED	RESERVED	BOOST_RDIS_EN	BOOST_EN_PIN_CTRL		BOOST_EN
R/W-0h		R/W-0h	R/W-1h	R/W-1h	R/W-0h		R/W-0h

Table 7-19. BOOST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_VSET	R/W	0h	Output voltage of Boost: 0x0 – 4.9 V 0x1 – 5.0 V 0x2 – 5.1 V 0x3 – 5.2 V (Default from OTP memory)
5	RESERVED	R/W	0h	
4	RESERVED	R/W	1h	
3	BOOST_RDIS_EN	R/W	1h	Enable output discharge resistor when BOOST is disabled: 0 – Discharge resistor disabled 1 – Discharge resistor enabled.
2-1	BOOST_EN_PIN_CTRL	R/W	0h	Enable or disable control for Boost: 0x0 – only BOOST_EN bit controls Boost 0x1 – BOOST_EN bit AND EN1 pin control Boost 0x2 – BOOST_EN bit AND EN2 pin control Boost 0x3 – BOOST_EN bit AND EN3 pin control Boost (Default from OTP memory)
0	BOOST_EN	R/W	0h	Enable Boost converter: 0 – Boost converter is disabled 1 – Boost converter is enabled. (Default from OTP memory)

7.6.1.1.10 BUCK0_DELAY Register (Offset = 9h) [reset = 0h]

BUCK0_DELAY is shown in Figure 7-28 and described in Table 7-20.

Return to Table 7-9.

Figure 7-28. BUCK0_DELAY Register

7	6	5	4	3	2	1	0
BUCK0_SHUTDOWN_DELAY				BUCK0_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-20. BUCK0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK0 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK0_STARTUP_DELAY	R/W	0h	Startup delay of BUCK0 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.11 BUCK1_DELAY Register (Offset = Ah) [reset = 0h]

BUCK1_DELAY is shown in Figure 7-29 and described in Table 7-21.

Return to Table 7-9.

Figure 7-29. BUCK1_DELAY Register

7	6	5	4	3	2	1	0
BUCK1_SHUTDOWN_DELAY				BUCK1_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-21. BUCK1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of BUCK1 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK1_STARTUP_DELAY	R/W	0h	Startup delay of BUCK1 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.12 BOOST_DELAY Register (Offset = Bh) [reset = 0h]

BOOST_DELAY is shown in Figure 7-30 and described in Table 7-22.

Return to Table 7-9.

Figure 7-30. BOOST_DELAY Register

7	6	5	4	3	2	1	0
BOOST_SHUTDOWN_DELAY				BOOST_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-22. BOOST_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BOOST_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of Boost from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BOOST_STARTUP_DELAY	R/W	0h	Startup delay of Boost from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.13 GPO0_DELAY Register (Offset = Ch) [reset = 0h]

GPO0_DELAY is shown in Figure 7-31 and described in Table 7-23.

Return to Table 7-9.

Figure 7-31. GPO0_DELAY Register

7	6	5	4	3	2	1	0
GPO0_SHUTDOWN_DELAY				GPO0_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-23. GPO0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO0_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO0 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO0_STARTUP_DELAY	R/W	0h	Startup delay of GPO0 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.14 GPO1_DELAY Register (Offset = Dh) [reset = 0h]

GPO1_DELAY is shown in Figure 7-32 and described in Table 7-24.

Return to Table 7-9.

Figure 7-32. GPO1_DELAY Register

7	6	5	4	3	2	1	0
GPO1_SHUTDOWN_DELAY				GPO1_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-24. GPO1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO1 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15b ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO1_STARTUP_DELAY	R/W	0h	Startup delay of GPO1 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.15 GPO2_DELAY Register (Offset = Eh) [reset = 0h]

GPO2_DELAY is shown in Figure 7-33 and described in Table 7-25.

Return to Table 7-9.

Figure 7-33. GPO2_DELAY Register

7	6	5	4	3	2	1	0
GPO2_SHUTDOWN_DELAY				GPO2_STARTUP_DELAY			
R/W-0h				R/W-0h			

Table 7-25. GPO2_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO2_SHUTDOWN_DELAY	R/W	0h	Shutdown delay of GPO2 from falling edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO2_STARTUP_DELAY	R/W	0h	Startup delay of GPO2 from rising edge of control signal: 0000 – 0 ms 0001 – 0.5 ms (1 ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 – 7.5 ms (15 ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.16 GPO_CONTROL_1 Register (Offset = Fh) [reset = AAh]

GPO_CONTROL_1 is shown in Figure 7-34 and described in Table 7-26.

Return to Table 7-9.

Figure 7-34. GPO_CONTROL_1 Register

7	6	5	4	3	2	1	0
GPO1_PG1_OD	GPO1_EN_PIN_CTRL		GPO1_OUT	GPO0_OD	GPO0_EN_PIN_CTRL		GPO0_OUT
R/W-1h	R/W-1h		R/W-0h	R/W-1h	R/W-1h		R/W-0h

Table 7-26. GPO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO1_PG1_OD	R/W	1h	GPO1/PG1 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
6-5	GPO1_EN_PIN_CTRL	R/W	1h	Control for GPO1 output: 0x0 – only GPO1_OUT bit controls GPO1 0x1 – GPO1_OUT bit AND EN1 pin control GPO1 0x2 – GPO1_OUT bit AND EN2 pin control GPO1 0x3 – GPO1_OUT bit AND EN3 pin control GPO1 (Default from OTP memory)
4	GPO1_OUT	R/W	0h	Control for GPO1 signal (when configured to GPO1): 0 – Logic low level 1 – Logic high level (Default from OTP memory)
3	GPO0_OD	R/W	1h	GPO0 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
2-1	GPO0_EN_PIN_CTRL	R/W	1h	Control for GPO0 output: 0x0 – only GPO0_OUT bit controls GPO0 0x1 – GPO0_OUT bit AND EN1 pin control GPO0 0x2 – GPO0_OUT bit AND EN2 pin control GPO0 0x3 – GPO0_OUT bit AND EN3 pin control GPO0 (Default from OTP memory)
0	GPO0_OUT	R/W	0h	Control for GPO0 signal: 0 – Logic low level 1 – Logic high level (Default from OTP memory)

7.6.1.1.17 GPO_CONTROL_2 Register (Offset = 10h) [reset = Ah]

GPO_CONTROL_2 is shown in Figure 7-35 and described in Table 7-27.

Return to Table 7-9.

Figure 7-35. GPO_CONTROL_2 Register

7	6	5	4	3	2	1	0
RESERVED		GPO2_SEL	GPO1_SEL	GPO2_OD	GPO2_EN_PIN_CTRL		GPO2_OUT
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h		R/W-0h

Table 7-27. GPO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPO2_SEL	R/W	0h	CLKIN/GPO2 pin function: 0 – CLKIN 1 – GPO2 (Default from OTP memory)
4	GPO1_SEL	R/W	0h	PG1/GPO1 pin function: 0 – PG1 1 – GPO1 (Default from OTP memory)
3	GPO2_OD	R/W	1h	GPO2 signal type (when configured to GPO2): 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)

Table 7-27. GPO_CONTROL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	GPO2_EN_PIN_CTRL	R/W	1h	Control for GPO2 output: 0x0 – only GPO2_OUT bit controls GPO2 0x1 – GPO2_OUT bit AND EN1 pin control GPO2 0x2 – GPO2_OUT bit AND EN2 pin control GPO2 0x3 – GPO2_OUT bit AND EN3 pin control GPO2 (Default from OTP memory)
0	GPO2_OUT	R/W	0h	Control for GPO2 signal (when configured to GPO2): 0 – Logic low level 1 – Logic high level (Default from OTP memory)

7.6.1.1.18 CONFIG Register (Offset = 11h) [reset = 3Ch]

CONFIG is shown in Figure 7-36 and described in Table 7-28.

Return to Table 7-9.

Figure 7-36. CONFIG Register

7	6	5	4	3	2	1	0
STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PD	EN3_PD	EN2_PD	EN1_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 7-28. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STARTUP_DELAY_SEL	R/W	0h	Startup delays from control signal: 0 – 0 ms – 7.5 ms with 0.5ms steps 1 – 0ms – 15ms with 1ms steps (Default from OTP memory)
6	SHUTDOWN_DELAY_SEL	R/W	0h	Shutdown delays from from signal: 0 – 0ms – 7.5ms with 0.5ms steps 1 – 0ms – 15ms with 1ms steps (Default from OTP memory)
5	CLKIN_PD	R/W	1h	Selects the pull down resistor on the CLKIN input pin. 0 – Pull-down resistor is disabled. 1 – Pull-down resistor is enabled. (Default from OTP memory)
4	EN3_PD	R/W	1h	Selects the pull down resistor on the EN3 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
3	EN2_PD	R/W	1h	Selects the pull down resistor on the EN2 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
2	EN1_PD	R/W	1h	Selects the pull down resistor on the EN1 pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
1	TDIE_WARN_LEVEL	R/W	0h	Thermal warning threshold level. 0 – 125°C 1 – 140°C. (Default from OTP memory)
0	EN_SPREAD_SPEC	R/W	0h	Enable spread spectrum feature for Buck and Boost converters. 0 – Disabled 1 – Enabled (Default from OTP memory)

7.6.1.1.19 PLL_CTRL Register (Offset = 12h) [reset = 2h]

PLL_CTRL is shown in Figure 7-37 and described in Table 7-29.

Return to Table 7-9.

Figure 7-37. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	EN_PLL	EN_FRAC_DIV	EXT_CLK_FREQ				
R/W-0h	R/W-0h	R/W-0h	R/W-2h				

Table 7-29. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	EN_PLL	R/W	0h	Selection of external clock and PLL operation: 0 – Forced to internal RC oscillator. PLL disabled. 1 – PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. (Default from OTP memory)
5	EN_FRAC_DIV	R/W	0h	This bit must be set to '0'.
4-0	EXT_CLK_FREQ	R/W	2h	Frequency of the external clock (CLKIN): 0x00 – 1 MHz 0x01 – 2 MHz 0x02 – 3 MHz ... 0x16 – 23 MHz 0x17 – 24 MHz 0x18...0x1F – Reserved See electrical specification for input clock frequency tolerance. (Default from OTP memory) Note: To ensure proper operation of PLL, EXT_CLK_FREQ value must not be changed when PLL is enabled.

7.6.1.1.20 PGOOD_CTRL Register (Offset = 13h) [reset = 0h]

PGOOD_CTRL is shown in Figure 7-38 and described in Table 7-30.

Return to Table 7-9.

Figure 7-38. PGOOD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	PGOOD_WINDOW	EN_PGOOD_VANA	EN_PGOOD_VMON2	EN_PGOOD_VMON1	EN_PGOOD_BOOST	EN_PGOOD_BUCK1	EN_PGOOD_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-30. PGOOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	PGOOD_WINDOW	R/W	0h	Voltage monitoring method for PG0 and PG1 signals: 0 - Only undervoltage monitoring. 1 - Overvoltage and undervoltage monitoring. (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
5	EN_PGOOD_VANA	R/W	0h	Enable powergood diagnostics for VANA 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.

Table 7-30. PGOOD_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EN_PGOOD_VMON2	R/W	0h	Enable powergood diagnostics for VMON2 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
3	EN_PGOOD_VMON1	R/W	0h	Enable powergood diagnostics for VMON1 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
2	EN_PGOOD_BOOST	R/W	0h	Enable powergood diagnostics for Boost 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
1	EN_PGOOD_BUCK1	R/W	0h	Enable powergood diagnostics for Buck1 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.
0	EN_PGOOD_BUCK0	R/W	0h	Enable powergood diagnostics for Buck0 0 – Disabled 1 – Enabled (Default from OTP memory) Note: Changing this value during operation may cause interrupt.

7.6.1.1.21 PGOOD_LEVEL_1 Register (Offset = 14h) [reset = 0h]

PGOOD_LEVEL_1 is shown in Figure 7-39 and described in Table 7-31.

Return to Table 7-9.

Figure 7-39. PGOOD_LEVEL_1 Register

7	6	5	4	3	2	1	0
RESERVED			VMON1_WINDOW		VMON1_THRESHOLD		
R/W-0h			R/W-0h		R/W-0h		

Table 7-31. PGOOD_LEVEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	VMON1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON1: 0x0 – ±2% 0x1 – ±3% 0x2 – ±4% 0x3 – ±6% (Default from OTP memory)

Table 7-31. PGOOD_LEVEL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	VMON1_THRESHOLD	R/W	0h	Threshold voltage for VMON1 input: 0x0 – 0.65V (high impedance input, external resistive divider can be used) 0x1 – 0.80 V 0x2 – 1.00 V 0x3 – 1.10 V 0x4 – 1.20 V 0x5 – 1.30 V 0x6 – 1.80 V 0x7 – 1.80 V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65 V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

7.6.1.1.22 PGOOD_LEVEL_2 Register (Offset = 15h) [reset = 0h]

PGOOD_LEVEL_2 is shown in Figure 7-40 and described in Table 7-32.

Return to Table 7-9.

Figure 7-40. PGOOD_LEVEL_2 Register

7	6	5	4	3	2	1	0
VANA_WINDOW		VANA_THRESHOLD	VMON2_WINDOW		VMON2_THRESHOLD		
R/W-0h		R/W-0h	R/W-0h		R/W-0h		

Table 7-32. PGOOD_LEVEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VANA_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VANA: 0x0 – ±4% 0x1 – ±5% 0x2 – ±10% 0x3 – ±10% (Default from OTP memory)
5	VANA_THRESHOLD	R/W	0h	Threshold voltage for VANA input: 0 – 3.3 V 1 – 5.0 V (Default from OTP memory)
4-3	VMON2_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for VMON2: 0x0 – ±2% 0x1 – ±3% 0x2 – ±4% 0x3 – ±6% (Default from OTP memory)
2-0	VMON2_THRESHOLD	R/W	0h	Threshold voltage for VMON2 input: 0x0 – 0.65 V (high impedance input, external resistive divider can be used) 0x1 – 0.80 V 0x2 – 1.00 V 0x3 – 1.10 V 0x4 – 1.20 V 0x5 – 1.30 V 0x6 – 1.80 V 0x7 – 1.80 V To monitor any other voltage level, select 0x0 and use an external resistive divider to scale down to 0.65 V. For other than 0x0 VMONx input is low impedance (internal resistive divider enabled). (Default from OTP memory)

7.6.1.1.23 PGOOD_LEVEL_3 Register (Offset = 16h) [reset = 0h]

PGOOD_LEVEL_3 is shown in Figure 7-41 and described in Table 7-33.

Return to Table 7-9.

Figure 7-41. PGOOD_LEVEL_3 Register

7	6	5	4	3	2	1	0
BOOST_WINDOW		BOOST_THRESHOLD		BUCK1_WINDOW		BUCK0_WINDOW	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-33. PGOOD_LEVEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_WINDOW	R/W	0h	Undervoltage or overvoltage threshold levels for Boost: 0x0 – ±2% 0x1 – ±4% 0x2 – ±6% 0x3 – ±8% (Default from OTP memory)
5-4	BOOST_THRESHOLD	R/W	0h	(Default from OTP memory)
3-2	BUCK1_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck1: 0x0 – ±30 mV 0x1 – ±50 mV 0x2 – ±70 mV 0x3 – ±90 mV (Default from OTP memory)
1-0	BUCK0_WINDOW	R/W	0h	Overvoltage and undervoltage threshold levels for Buck0: 0x0 – ±30 mV 0x1 – ±50 mV 0x2 – ±70 mV 0x3 – ±90 mV (Default from OTP memory)

7.6.1.1.24 PG_CTRL Register (Offset = 17h) [reset = 2h]

PG_CTRL is shown in Figure 7-42 and described in Table 7-34.

Return to Table 7-9.

Figure 7-42. PG_CTRL Register

7	6	5	4	3	2	1	0
PG1_MODE	PGOOD_FAULT_GATES_PG1	RESERVED	PG1_POL	PG0_MODE	PGOOD_FAULT_GATES_PG0	PG0_OD	PG0_POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

Table 7-34. PG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_MODE	R/W	0h	Operating mode for PG1 signal: 0 – Detecting unusual situations 1 – Showing when requested outputs are not valid. (Default from OTP memory)
6	PGOOD_FAULT_GATES_PG1	R/W	0h	Type of operation for PG1 signal: 0 – Indicates live status of monitored voltage outputs. 1 – Indicates status of PG1_FAULT register, inactive if at least one of PG1_FAULT_x bit is inactive. (Default from OTP memory)
5	RESERVED	R/W	0h	

Table 7-34. PG_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PG1_POL	R/W	0h	PG1 signal polarity. 0 – PG1 signal high when monitored outputs are valid 1 – PG1 signal low when monitored outputs are valid (Default from OTP memory)
3	PG0_MODE	R/W	0h	Operating mode for PG0 signal: 0 – Detecting unusual situations 1 – Showing when requested outputs are not valid. (Default from OTP memory)
2	PGOOD_FAULT_GATES_PG0	R/W	0h	Type of operation for PG0 signal: 0 – Indicates live status of monitored voltage outputs. 1 – Indicates status of PG0_FAULT register, inactive if at least one of PG0_FAULT_x bit is inactive. (Default from OTP memory)
1	PG0_OD	R/W	1h	PG0 signal type: 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)
0	PG0_POL	R/W	0h	PG0 signal polarity. 0 – PG0 signal high when monitored outputs are valid 1 – PG0 signal low when monitored outputs are valid (Default from OTP memory)

7.6.1.1.25 PG0_CTRL Register (Offset = 18h) [reset = 0h]

PG0_CTRL is shown in Figure 7-43 and described in Table 7-35.

Return to Table 7-9.

Figure 7-43. PG0_CTRL Register

7	6	5	4	3	2	1	0
PG0_RISE_DELAY	SEL_PG0_TWARN	SEL_PG0_VANA	SEL_PG0_VMON2	SEL_PG0_VMON1	SEL_PG0_BOOST	SEL_PG0_BUCK1	SEL_PG0_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-35. PG0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG0_RISE_DELAY	R/W	0h	0 – PG0 rise is not delayed 1 – PG0 rise is delayed 11 ms
6	SEL_PG0_TWARN	R/W	0h	PG0 control from thermal warning: 0 - Masked 1 – Affecting PGOOD (Default from OTP memory)
5	SEL_PG0_VANA	R/W	0h	PG0 signal source control from VANA 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
4	SEL_PG0_VMON2	R/W	0h	PG0 signal source control from VMON2 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
3	SEL_PG0_VMON1	R/W	0h	PG0 signal source control from VMON1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)

Table 7-35. PG0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEL_PG0_BOOST	R/W	0h	PG0 signal source control from Boost 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
1	SEL_PG0_BUCK1	R/W	0h	PG0 signal source control from Buck1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
0	SEL_PG0_BUCK0	R/W	0h	PG0 signal source control from Buck0 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)

7.6.1.1.26 PG0_FAULT Register (Offset = 19h) [reset = 0h]

PG0_FAULT is shown in Figure 7-44 and described in Table 7-36.

Return to Table 7-9.

Figure 7-44. PG0_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG0_FAULT_TWARN	PG0_FAULT_VANA	PG0_FAULT_VMON2	PG0_FAULT_VMON1	PG0_FAULT_BOOST	PG0_FAULT_BUCK1	PG0_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-36. PG0_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG0_FAULT_TWARN	R	0h	Source for PG0 inactive signal: 0 – TWARN has not set PG0 signal inactive. 1 – TWARN is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG0_FAULT_VANA	R	0h	Source for PG0 inactive signal: 0 – VANA has not set PG0 signal inactive. 1 –VANA is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG0_FAULT_VMON2	R	0h	Source for PG0 inactive signal: 0 – VMON2 has not set PG0 signal inactive. 1 – VMON2 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG0_FAULT_VMON1	R	0h	Source for PG0 inactive signal: 0 – VMON1 has not set PG0 signal inactive. 1 – VMON1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG0_FAULT_BOOST	R	0h	Source for PG0 inactive signal: 0 – Boost has not set PG0 signal inactive. 1 – Boost is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG0_FAULT_BUCK1	R	0h	Source for PG0 inactive signal: 0 – Buck1 has not set PG0 signal inactive. 1 – Buck1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.

Table 7-36. PG0_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PG0_FAULT_BUCK0	R	0h	Source for PG0 inactive signal: 0 – Buck0 has not set PG0 signal inactive. 1 – Buck0 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.27 PG1_CTRL Register (Offset = 1Ah) [reset = 0h]

PG1_CTRL is shown in Figure 7-45 and described in Table 7-37.

Return to Table 7-9.

Figure 7-45. PG1_CTRL Register

7	6	5	4	3	2	1	0
PG1_RISE_DELAY	SEL_PG1_TWARN	SEL_PG1_VANA	SEL_PG1_VMON2	SEL_PG1_VMON1	SEL_PG1_BOOST	SEL_PG1_BUCK1	SEL_PG1_BUCK0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-37. PG1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_RISE_DELAY	R/W	0h	0 – PG1 rise is not delayed 1 – PG1 rise is delayed 11ms
6	SEL_PG1_TWARN	R/W	0h	PG1 control from thermal warning: 0 – Masked 1 – Affecting PGOOD (Default from OTP memory)
5	SEL_PG1_VANA	R/W	0h	PG1 signal source control from VANA 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
4	SEL_PG1_VMON2	R/W	0h	PG1 signal source control from VMON2 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
3	SEL_PG1_VMON1	R/W	0h	PG1 signal source control from VMON1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
2	SEL_PG1_BOOST	R/W	0h	PG1 signal source control from Boost 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
1	SEL_PG1_BUCK1	R/W	0h	PG1 signal source control from Buck1 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)
0	SEL_PG1_BUCK0	R/W	0h	PG1 signal source control from Buck0 0 – Masked 1 – Powergood threshold voltage (Default from OTP memory)

7.6.1.1.28 PG1_FAULT Register (Offset = 1Bh) [reset = 0h]

PG1_FAULT is shown in Figure 7-46 and described in Table 7-38.

Return to Table 7-9.

Figure 7-46. PG1_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG1_FAULT_TWARN	PG1_FAULT_VANA	PG1_FAULT_VMON2	PG1_FAULT_VMON1	PG1_FAULT_BOOST	PG1_FAULT_BUCK1	PG1_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-38. PG1_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG1_FAULT_TWARN	R	0h	Source for PG1 inactive signal: 0 – TWARN has not set PG1 signal inactive. 1 – TWARN is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG1_FAULT_VANA	R	0h	Source for PG1 inactive signal: 0 – VANA has not set PG1 signal inactive. 1 – VANA is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG1_FAULT_VMON2	R	0h	Source for PG1 inactive signal: 0 – VMON2 has not set PG1 signal inactive. 1 – VMON2 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG1_FAULT_VMON1	R	0h	Source for PG1 inactive signal: 0 – VMON1 has not set PG1 signal inactive. 1 – VMON1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG1_FAULT_BOOST	R	0h	Source for PG1 inactive signal: 0 – Boost has not set PG1 signal inactive. 1 – Boost is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG1_FAULT_BUCK1	R	0h	Source for PG1 inactive signal: 0 – Buck1 has not set PG1 signal inactive. 1 – Buck1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG1_FAULT_BUCK0	R	0h	Source for PG1 inactive signal: 0 – Buck0 has not set PG1 signal inactive. 1 – Buck0 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.29 WD_CTRL_1 Register (Offset = 1Ch) [reset = 0h]

WD_CTRL_1 is shown in Figure 7-47 and described in Table 7-39.

Return to Table 7-9.

Figure 7-47. WD_CTRL_1 Register

7	6	5	4	3	2	1	0
WD_CLOSE_TIME		WD_OPEN_TIME		WD_LONG_OPEN_TIME		WD_RESET_CNTR_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-39. WD_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CLOSE_TIME	R/W	0h	Watchdog close window time select. 00 – 10 ms 01 – 20 ms 10 – 50 ms 11 – 100 ms (Default from OTP memory)
5-4	WD_OPEN_TIME	R/W	0h	Watchdog open window time select. 00 – 20 ms 01 – 100 ms 10 – 200 ms 11 – 600 ms (Default from OTP memory)
3-2	WD_LONG_OPEN_TIME	R/W	0h	Watchdog long open window time select. 00 – 200 ms 01 – 600 ms 10 – 2000 ms 11 – 5000 ms (Default from OTP memory)
1-0	WD_RESET_CNTR_SEL	R/W	0h	Watchdog reset counter threshold select. After the selected number of reset (WDR) pulses system restart sequence is initiated. 00 – system restart disabled 01 – 1 10 – 2 11 – 4 (Default from OTP memory)

7.6.1.1.30 WD_CTRL_2 Register (Offset = 1Dh) [reset = 1h]

WD_CTRL_2 is shown in Figure 7-48 and described in Table 7-40.

Return to Table 7-9.

Figure 7-48. WD_CTRL_2 Register

7	6	5	4	3	2	1	0
WD_LOCK	RESERVED		WD_SYS_RESTART_FLAG_MODE	WD_EN_OTP_READ	WDI_PD	WDR_POL	WDR_OD
R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 7-40. WD_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_LOCK	R	0h	Lock bit for watchdog controls. Locks all controls to watchdog in registers WD_CTRL_1, WD_CTRL_2. Lock bit also locks itself. Once lock bit is written 1 it cannot be written 0. Only reset can clear it. 0 – Not locked 1 – Locked WD_STATUS register is not affected by WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK=1.
6-5	RESERVED	R/W	0h	
4	WD_SYS_RESTART_FLAG_MODE	R/W	0h	WD_SYSTEM_RESTART_FLAG mode select. 0 - WD_SYSTEM_RESTART_FLAG is only a status bit. 1 – WD_SYSTEM_RESTART_FLAG prevents further system restarts until it is cleared. (Default from OTP memory)
3	WD_EN_OTP_READ	R/W	0h	Read OTP during system restart sequence 0 – OTP read not enabled during system restart sequence 1 – OTP read enabled during system restart sequence (Default from OTP memory)

Table 7-40. WD_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WDI_PD	R/W	0h	Selects the pull down resistor on the WDI pin: 0 – Pull-down resistor is disabled 1 – Pull-down resistor is enabled (Default from OTP memory)
1	WDR_POL	R/W	0h	Watchdog reset output (WDR) polarity select 0 – Active high 1 – Active low (Default from OTP memory)
0	WDR_OD	R/W	1h	Watchdog reset output (WDR) signal type 0 – Push-pull output (VANA level) 1 – Open-drain output (Default from OTP memory)

7.6.1.1.31 WD_STATUS Register (Offset = 1Eh) [reset = 0h]

WD_STATUS is shown in Figure 7-49 and described in Table 7-41.

Return to Table 7-9.

Figure 7-49. WD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			WD_CLR_SYSTEM_RESTART_FLAG	WD_SYSTEM_RESTART_FLAG	WD_CLR_RESET_CNTR	WD_RESET_CNTR_STATUS	
R/W-0h			R-0h	R-0h	R-0h	R-0h	

Table 7-41. WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	WD_CLR_SYSTEM_RESTART_FLAG	R	0h	Clear bit for WD_SYSTEM_RESTART_FLAG. Write 1 to generate a clear pulse. Reg bit value returns to 0 after clearing is finished.
3	WD_SYSTEM_RESTART_FLAG	R	0h	Watchdog requested system restart has occurred. Can be cleared by writing WD_CLR_SYSTEM_RESTART_FLAG bit 1.
2	WD_CLR_RESET_CNTR	R	0h	Watchdog reset counter clear. Write 1 to generate a clear pulse.
1-0	WD_RESET_CNTR_STATUS	R	0h	Current status of watchdog reset counter.

7.6.1.1.32 RESET Register (Offset = 1Fh) [reset = 0h]

RESET is shown in Figure 7-50 and described in Table 7-42.

Return to Table 7-9.

Figure 7-50. RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R/W-0h							R-0h

Table 7-42. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SW_RESET	R	0h	Software commanded reset. When written to 1, the registers will be reset to default values and OTP memory is read. The bit is automatically cleared.

7.6.1.1.33 INT_TOP_1 Register (Offset = 20h) [reset = 0h]

INT_TOP_1 is shown in Figure 7-51 and described in Table 7-43.

Return to Table 7-9.

Figure 7-51. INT_TOP_1 Register

7	6	5	4	3	2	1	0
I_MEAS_INT	DIAG_INT	BOOST_INT	BUCK_INT	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-43. INT_TOP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_INT	R	0h	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.
6	DIAG_INT	R	0h	Interrupt indicating that INT_DIAG register has a pending interrupt. The reason for the interrupt is indicated in INT_DIAG register. This bit is cleared automatically when INT_DIAG register is cleared to 0x00.
5	BOOST_INT	R	0h	Interrupt indicating that BOOST have a pending interrupt. The reason for the interrupt is indicated in INT_BOOST register. This bit is cleared automatically when INT_BOOST register is cleared to 0x00.
4	BUCK_INT	R	0h	Interrupt indicating that BUCK0 or BUCK1 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.
3	SYNC_CLK_INT	R	0h	Latched status bit indicating that the external clock frequency became valid or invalid. Write 1 to clear interrupt.
2	TDIE_SD_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The converters have been disabled if they were enabled. The converters cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TDIE_SD_STAT bit in TOP_STATUS register. Write 1 to clear interrupt. Clearing TSD interrupt automatically re-enables converters. Clearing this interrupt will also clear thermal warning status.
1	TDIE_WARN_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_STAT bit in TOP_STATUS register. Write 1 to clear interrupt.
0	OVP_INT	R	0h	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by OVP bit in TOP_STATUS register. Write 1 to clear interrupt.

7.6.1.1.34 INT_TOP_2 Register (Offset = 21h) [reset = 0h]

INT_TOP_2 is shown in Figure 7-52 and described in Table 7-44.

Return to Table 7-9.

Figure 7-52. INT_TOP_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_INT

Figure 7-52. INT_TOP_2 Register (continued)

R/W-0h	R-0h

Table 7-44. INT_TOP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_INT	R	0h	Latched status bit indicating that either VANA supply voltage has been below undervoltage threshold level or the host has requested a reset (SW_RESET bit in RESET register). The converters have been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.

7.6.1.1.35 INT_BUCK Register (Offset = 22h) [reset = 0h]

INT_BUCK is shown in Figure 7-53 and described in Table 7-45.

Return to Table 7-9.

Figure 7-53. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	RESERVED	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h

Table 7-45. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	BUCK1_PG_INT	R	0h	Latched status bit indicating that BUCK1 powergood event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R	0h	Latched status bit indicating that the BUCK1 output voltage has fallen below 0.35 V level during operation or BUCK1 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
4	BUCK1_ILIM_INT	R	0h	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
3	RESERVED	R/W	0h	
2	BUCK0_PG_INT	R	0h	Latched status bit indicating that BUCK0 powergood event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R	0h	Latched status bit indicating that the BUCK0 output voltage has fallen below 0.35 V level during operation or BUCK0 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
0	BUCK0_ILIM_INT	R	0h	Latched status bit indicating that BUCK0 output current limit has been triggered. Write 1 to clear.

7.6.1.1.36 INT_BOOST Register (Offset = 23h) [reset = 0h]

INT_BOOST is shown in Figure 7-54 and described in Table 7-46.

Return to Table 7-9.

Figure 7-54. INT_BOOST Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_PG_INT	BOOST_SC_INT	BOOST_ILIM_INT
R/W-0h					R-0h	R-0h	R-0h

Table 7-46. INT_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_PG_INT	R	0h	Latched status bit indicating that Boost powergood event has been detected. Write 1 to clear.
1	BOOST_SC_INT	R	0h	Latched status bit indicating that the Boost output voltage has fallen to input voltage level or below 2.5 V level during operation or BOOST output didn't reach 2.5 V level in 1 ms from enable. Write 1 to clear.
0	BOOST_ILIM_INT	R	0h	Latched status bit indicating that Boost output current limit has been triggered. Write 1 to clear.

7.6.1.1.37 INT_DIAG Register (Offset = 24h) [reset = 0h]

INT_DIAG is shown in Figure 7-55 and described in Table 7-47.

Return to Table 7-9.

Figure 7-55. INT_DIAG Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_INT	RESERVED	VMON1_PG_INT	RESERVED	VANA_PG_INT
R/W-0h			R-0h	R/W-0h	R-0h	R/W-0h	R-0h

Table 7-47. INT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	VMON2_PG_INT	R	0h	Latched status bit indicating that VMON2 powergood event has been detected. Write 1 to clear.
3	RESERVED	R/W	0h	
2	VMON1_PG_INT	R	0h	Latched status bit indicating that VMON1 powergood event has been detected. Write 1 to clear.
1	RESERVED	R/W	0h	
0	VANA_PG_INT	R	0h	Latched status bit indicating that VANA powergood event has been detected. Write 1 to clear.

7.6.1.1.38 TOP_STATUS Register (Offset = 25h) [reset = 0h]

TOP_STATUS is shown in Figure 7-56 and described in Table 7-48.

Return to Table 7-9.

Figure 7-56. TOP_STATUS Register

7	6	5	4	3	2	1	0

Figure 7-56. TOP_STATUS Register (continued)

RESERVED	SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT
R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-48. TOP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	SYNC_CLK_STAT	R	0h	Status bit indicating the status of external clock (CLKIN): 0 – External clock frequency is valid 1 – External clock frequency is not valid.
2	TDIE_SD_STAT	R	0h	Status bit indicating the status of thermal shutdown: 0 – Die temperature below thermal shutdown level 1 – Die temperature above thermal shutdown level.
1	TDIE_WARN_STAT	R	0h	Status bit indicating the status of thermal warning: 0 – Die temperature below thermal warning level 1 – Die temperature above thermal warning level.
0	OVP_STAT	R	0h	Status bit indicating the status of input overvoltage monitoring: 0 – Input voltage below overvoltage threshold level 1 – Input voltage above overvoltage threshold level.

7.6.1.1.39 BUCK_STATUS Register (Offset = 26h) [reset = 0h]

BUCK_STATUS is shown in Figure 7-57 and described in Table 7-49.

Return to Table 7-9.

Figure 7-57. BUCK_STATUS Register

7	6	5	4	3	2	1	0
BUCK1_STAT	BUCK1_PG_STAT		BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT		BUCK0_ILIM_STAT
R-0h	R-0h		R-0h	R-0h	R-0h		R-0h

Table 7-49. BUCK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_STAT	R	0h	Status bit indicating the enable or disable status of BUCK1: 0 – BUCK1 converter is disabled 1 – BUCK1 converter is enabled.
6	BUCK1_PG_STAT	R	0h	Status bit indicating BUCK1 output voltage validity (raw status) 0 – BUCK1 output is not valid 1 – BUCK1 output is valid.
4	BUCK1_ILIM_STAT	R	0h	Status bit indicating BUCK1 current limit status (raw status) 0 – BUCK1 output current is below current limit threshold level 1 – BUCK1 output current is at current limit threshold level.
3	BUCK0_STAT	R	0h	Status bit indicating the enable or disable status of BUCK0: 0 – BUCK0 converter is disabled 1 – BUCK0 converter is enabled.
2	BUCK0_PG_STAT	R	0h	Status bit indicating BUCK0 output voltage validity (raw status) 0 – BUCK0 output is not valid 1 – BUCK0 output is valid.
0	BUCK0_ILIM_STAT	R	0h	Status bit indicating BUCK0 current limit status (raw status) 0 – BUCK0 output current is below current limit threshold level 1 – BUCK0 output current is at current limit threshold level.

7.6.1.1.40 BOOST_STATUS Register (Offset = 27h) [reset = 0h]

BOOST_STATUS is shown in Figure 7-58 and described in Table 7-50.

Return to Table 7-9.

Figure 7-58. BOOST_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_STAT	BOOST_PG_STAT		BOOST_ILIM_STAT
R-0h				R-0h	R-0h		R-0h

Table 7-50. BOOST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BOOST_STAT	R	0h	Status bit indicating the enable/disable status of Boost: 0 – Boost converter is disabled 1 – Boost converter is enabled.
2	BOOST_PG_STAT	R	0h	Status bit indicating Boost output voltage validity (raw status) 0 – Boost output is not valid 1 – Boost output is valid.
0	BOOST_ILIM_STAT	R	0h	Status bit indicating Boost current limit status (raw status) 0 – Boost output current is below current limit threshold level 1 – Boost output current is at current limit threshold level.

7.6.1.1.41 DIAG_STATUS Register (Offset = 28h) [reset = 0h]

DIAG_STATUS is shown in Figure 7-59 and described in Table 7-51.

Return to Table 7-9.

Figure 7-59. DIAG_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_STAT	RESERVED	VMON1_PG_STAT	RESERVED	VANA_PG_STAT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-51. DIAG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	VMON2_PG_STAT	R	0h	Status bit indicating VMON2 input voltage validity (raw status) 0 – VMON2 voltage is not valid 1 – VMON2 voltage is valid.
3	RESERVED	R	0h	
2	VMON1_PG_STAT	R	0h	Status bit indicating VMON1 input voltage validity (raw status) 0 – VMON1 voltage is not valid 1 – VMON1 voltage is valid.
1	RESERVED	R	0h	
0	VANA_PG_STAT	R	0h	Status bit indicating VANA input voltage validity (raw status) 0 – VANA voltage is not valid 1 – VANA voltage is valid.

7.6.1.1.42 TOP_MASK_1 Register (Offset = 29h) [reset = 0h]

TOP_MASK_1 is shown in Figure 7-60 and described in Table 7-52.

Return to Table 7-9.

Figure 7-60. TOP_MASK_1 Register

7	6	5	4	3	2	1	0
I_MEAS_MASK	RESERVED			SYNC_CLK_MASK	RESERVED	TDIE_WARN_MASK	RESERVED
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-52. TOP_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_MASK	R/W	0h	Masking for load current measurement ready interrupt I_MEAS_INT in INT_TOP_1 register. 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)
6-4	RESERVED	R/W	0h	
3	SYNC_CLK_MASK	R/W	0h	Masking for external clock detection interrupt SYNC_CLK_INT in INT_TOP_1 register: 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)
2	RESERVED	R/W	0h	
1	TDIE_WARN_MASK	R/W	0h	Masking for thermal warning interrupt TDIE_WARN_INT in INT_TOP_1 register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect TDIE_WARN_STAT status bit in TOP_STATUS register. (Default from OTP memory)
0	RESERVED	R/W	0h	

7.6.1.1.43 TOP_MASK_2 Register (Offset = 2Ah) [reset = 1h]

TOP_MASK_2 is shown in Figure 7-61 and described in Table 7-53.

Return to Table 7-9.

Figure 7-61. TOP_MASK_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_MASK
R/W-0h							R/W-1h

Table 7-53. TOP_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_MASK	R/W	1h	Masking for register reset interrupt RESET_REG_INT in INT_TOP_2 register: 0 – Interrupt generated 1 – Interrupt not generated. (Default from OTP memory)

7.6.1.1.44 BUCK_MASK Register (Offset = 2Bh) [reset = 0h]

BUCK_MASK is shown in Figure 7-62 and described in Table 7-54.

Return to Table 7-9.

Figure 7-62. BUCK_MASK Register

7	6	5	4	3	2	1	0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	RESERVED	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	RESERVED	BUCK0_ILIM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-54. BUCK_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
6	BUCK1_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	BUCK1_ILIM_MASK	R/W	0h	Masking for BUCK1 current monitoring interrupt BUCK1_ILIM_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK1_ILIM_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
3	BUCK0_PGF_MASK	R/W	0h	Masking of powergood invalid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
2	BUCK0_PGR_MASK	R/W	0h	Masking of powergood valid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STATUS register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BUCK0_ILIM_MASK	R/W	0h	Masking for BUCK0 current monitoring interrupt BUCK0_ILIM_INT in INT_BUCK register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BUCK0_ILIM_STAT status bit in BUCK_STATUS register. (Default from OTP memory)

7.6.1.1.45 BOOST_MASK Register (Offset = 2Ch) [reset = 0h]

BOOST_MASK is shown in Figure 7-63 and described in Table 7-55.

Return to Table 7-9.

Figure 7-63. BOOST_MASK Register

7	6	5	4	3	2	1	0

Figure 7-63. BOOST_MASK Register (continued)

RESERVED	BOOST_PGF_MASK	BOOST_PGR_MASK	RESERVED	BOOST_ILIM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-55. BOOST_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BOOST_PGF_MASK	R/W	0h	Masking of powergood invalid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STATUS register. (Default from OTP memory)
2	BOOST_PGR_MASK	R/W	0h	Masking of powergood valid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STATUS register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BOOST_ILIM_MASK	R/W	0h	Masking for Boost current monitoring interrupt BOOST_ILIM_INT in INT_BOOST register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect BOOST_ILIM_STAT status bit in BOOST_STATUS register. (Default from OTP memory)

7.6.1.1.46 DIAG_MASK Register (Offset = 2Dh) [reset = 0h]

DIAG_MASK is shown in Figure 7-64 and described in Table 7-56.

Return to Table 7-9.

Figure 7-64. DIAG_MASK Register

7	6	5	4	3	2	1	0
RESERVED		VMON2_PGF_MASK	VMON2_PGR_MASK	VMON1_PGF_MASK	VMON1_PGR_MASK	VANA_PGF_MASK	VANA_PGR_MASK
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-56. DIAG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	VMON2_PGF_MASK	R/W	0h	Masking of VMON2 invalid detection for powergood interrupt VMON2_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)

Table 7-56. DIAG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VMON2_PGR_MASK	R/W	0h	Masking of VMON2 valid detection for powergood interrupt VMON2_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
3	VMON1_PGF_MASK	R/W	0h	Masking of VMON1 invalid detection for powergood interrupt VMON1_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
2	VMON1_PGR_MASK	R/W	0h	Masking of VMON1 valid detection for powergood interrupt VMON1_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
1	VANA_PGF_MASK	R/W	0h	Masking of VANA invalid detection for powergood interrupt VANA_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)
0	VANA_PGR_MASK	R/W	0h	Masking of VANA valid detection for powergood interrupt VANA_PG_INT in INT_DIAG register: 0 – Interrupt generated 1 – Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in DIAG_STATUS register. (Default from OTP memory)

7.6.1.1.47 SEL_I_LOAD Register (Offset = 2Eh) [reset = 0h]

SEL_I_LOAD is shown in Figure 7-65 and described in Table 7-57.

Return to Table 7-9.

Figure 7-65. SEL_I_LOAD Register

7	6	5	4	3	2	1	0
RESERVED						LOAD_CURRENT_BUCK_SELECT	
R/W-0h						R/W-0h	

Table 7-57. SEL_I_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	LOAD_CURRENT_BUCK_SELECT	R/W	0h	Start the current measurement on the selected Buck converter: 0 – BUCK0 1 – BUCK1 2 – BUCK0 3 – BUCK1 The measurement is started when register is written.

7.6.1.1.48 I_LOAD_2 Register (Offset = 2Fh) [reset = 0h]

I_LOAD_2 is shown in Figure 7-66 and described in Table 7-58.

Return to Table 7-9.

Figure 7-66. I_LOAD_2 Register

7	6	5	4	3	2	1	0
RESERVED							BUCK_LOAD_CURRENT_8
R-0h							R-0h

Table 7-58. I_LOAD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	BUCK_LOAD_CURRENT_8	R	0h	This register describes the MSB bit of the average load current on selected converter with a resolution of 20 mA per LSB and maximum 10 A current.

7.6.1.1.49 I_LOAD_1 Register (Offset = 30h) [reset = 0h]

I_LOAD_1 is shown in Figure 7-67 and described in Table 7-59.

Return to Table 7-9.

Figure 7-67. I_LOAD_1 Register

7	6	5	4	3	2	1	0
BUCK_LOAD_CURRENT_7_0							
R-0h							

Table 7-59. I_LOAD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK_LOAD_CURRENT_7_0	R	0h	This register describes 8 LSB bits of the average load current on selected converter with a resolution of 20 mA per LSB and maximum 10 A current.

7.6.1.1.50 FREQ_SEL Register (Offset = 31h) [reset = 0h]

FREQ_SEL is shown in Figure 7-68 and described in Table 7-60.

Return to Table 7-9.

Figure 7-68. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_FREQ_SEL	BUCK_FREQ_SEL	
R/W-0h					R-0h	R-0h	

Table 7-60. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_FREQ_SEL	R	0h	Boost switching frequency: 0 – 2 MHz 1 – 4 MHz (Default from OTP memory)

Table 7-60. FREQ_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	BUCK_FREQ_SEL	R	0h	Buck0 and Buck1 switching frequency: 0x0 – 2 MHz 0x1 – 3 MHz 0x2 – 4 MHz 0x3 – 4 MHz (Default from OTP memory)

7.6.1.1.51 BOOST_ILIM_CTRL Register (Offset = 32h) [reset = 0h]

BOOST_ILIM_CTRL is shown in Figure 7-69 and described in Table 7-61.

Return to Table 7-9.

Figure 7-69. BOOST_ILIM_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						BOOST_ILIM	
R/W-0h						R/W-0h	

Table 7-61. BOOST_ILIM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	BOOST_ILIM	R/W	0h	Sets the current limit of Boost. 00 – 1.0 A 01 – 1.4 A 10 – 1.9 A 11 – 2.8 A (Default from OTP memory)

7.6.1.1.52 ECC_STATUS Register (Offset = 33h) [reset = 0h]

ECC_STATUS is shown in Figure 7-70 and described in Table 7-62.

Return to Table 7-9.

Figure 7-70. ECC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						DED	SED
R-0h						R-0h	R-0h

Table 7-62. ECC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	DED	R	0h	OTP error correction status: 0 – No dual errors detected 1 – Dual errors detected and not corrected
0	SED	R	0h	OTP error correction status: 0 – No single errors detected 1 – Single errors detected and corrected

7.6.1.1.53 WD_DIS_CTRL_CODE Register (Offset = 34h) [reset = 0h]

WD_DIS_CTRL_CODE is shown in Figure 7-71 and described in Table 7-63.

Return to Table 7-9.

Figure 7-71. WD_DIS_CTRL_CODE Register

7	6	5	4	3	2	1	0
WD_DIS_UNLOCK_CODE							
R-0h							

Table 7-63. WD_DIS_CTRL_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_DIS_UNLOCK_CODE	R	0h	Unlocking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=0 by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register. Locking WD_DIS_CTRL bit: Set WD_DIS_CTRL_LOCK=1 by writing anything to WD_DIS_CTRL_CODE register or write WD_LOCK=1. Reading this address returns always 0x00. WD_DIS_CTRL can be unlocked only if WD_LOCK=0.

7.6.1.1.54 WD_DIS_CONTROL Register (Offset = 35h) [reset = 0h]

WD_DIS_CONTROL is shown in Figure 7-72 and described in Table 7-64.

Return to Table 7-9.

Figure 7-72. WD_DIS_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						WD_DIS_CTRL_LOCK	WD_DIS_CTRL
R/W-0h						R-1h	R/W-0h

Table 7-64. WD_DIS_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	WD_DIS_CTRL_LOCK	R	1h	Lock status for WD_DIS_CTRL bit. 0 – Not locked, WD_DIS_CTRL bit can be written. 1 – Locked, WD_DIS_CTRL bit is locked and cannot be changed. Lock can be opened by writing 0x87, 0x65, 0x1B by 3 consecutive I2C write sequences to WD_DIS_CTRL_CODE register if WD_LOCK=0. Lock can be closed by writing anything to WD_DIS_CTRL_CODE register or writing WD_LOCK=1.
0	WD_DIS_CTRL	R/W	0h	Watchdog disable pin control. 0 – Watchdog cannot be disabled by WD_DIS pin. 1 – Watchdog can be disabled by WD_DIS pin. (Default from OTP memory) This bit can be written 1 only if WD_LOCK=0 and WD_DIS_CTRL_LOCK=0.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP87702 is a power-management unit including a boost converter, two step-down converters, and three general-purpose digital output signals.

8.2 Typical Application

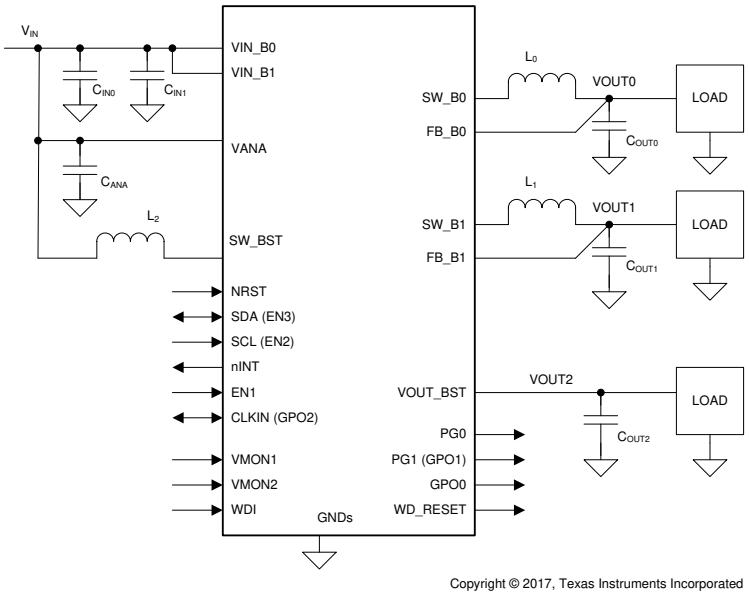


Figure 8-1. LP87702 Typical Application

8.2.1 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltages	1.8 V, 1.24 V, 5 V
Switching frequency	4 MHz

8.2.2 Detailed Design Procedure

The performance of the LP87702 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from the system power rail while turning on the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck converter power pins VIN_Bx are not connected together internally. The VIN_Bx power connections shall be connected together outside the package using a power plane construction.

8.2.2.1 Application Components

8.2.2.1.1 Inductor Selection

Section 8.2 shows the inductors L_0, L_1, and L_2. The inductor's inductance and DCR affects the buck and boost converter's control loop. Table 8-2 lists the recommended inductors, or similar ones, that should be used. Pay attention to the inductor's saturation current and temperature rise current. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. Section 6 shows the minimum effective inductance that ensures good performance. The inductor's DC resistance should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

Table 8-2. Recommended Inductors for Buck Converters

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W x× H (mm)	RATED DC CURRENT, I_{SAT} max / I_{TEMP} max (A)	DCR typ / max (mΩ)
MURATA	DFE20162E-R47M	0.47 µH (20%)	2 × 1.6 × 1.2	5.5 / 4.5(1)	- / 26
MURATA	DFE252012F-R47M	0.47 µH (20%)	2.5 × 2 × 1.2	6.7 / 4.9(1)	- / 23

(1) Operating temperature range is up to 125°C including self temperature rise.

Table 8-3. Recommended Inductor for Boost Converters

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W x× H (mm)	RATED DC CURRENT, I_{SAT} max / I_{TEMP} max (A)	DCR typ / max (mΩ)
MURATA	DFE201612E-1R0M	1 µH (20%)	2 × 1.6 × 1.2	4.0 / 2.9 (1)	- / 42
MURATA	DFE252012F-1R0M	1 µH (20%)	2.5 × 2 × 1.2	4.2 / 3.3 (1)	- / 40

8.2.2.1.2 Buck Input Capacitor Selection

Section 8.2 shows the input capacitors C_{IN0} and C_{IN1}. A ceramic input bypass capacitor of 10 µF is required for both converters. Place the input capacitor as close as possible to the device's VIN_Bx pin and PGND_Bx pin. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. The capacitor's DC bias characteristics must also be considered. Minimum effective input capacitance to ensure good performance is 1.9 µF per buck input at the maximum input voltage including tolerances and ambient temperature range. In addition, Table 8-4 shows how there must be at least 22 µF of additional capacitance common for all the power input pins on the system power rail.

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces the voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition, ferrite can be used in front of the input capacitor to reduce the EMI.

Table 8-4. Recommended Buck Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GRM21BR71A06KA73	10 µF (10%)	0805	2 × 1.25 × 1.25	10 V
TDK	C2012X7R1A106K125AC	10 µF (10%)	0805	2 × 1.25 × 1.25	10 V

8.2.2.1.3 Buck Output Capacitor Selection

Section 8.2 shows the output capacitor C_{OUT0} and C_{OUT1}. A ceramic local output capacitor of 22 µF is required for both outputs. Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out the current flow from the inductor to the load, whic helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance for good performance is 15 µF for each buck, including the DC voltage roll-off, tolerances, aging, and temperature effects.

The output voltage ripple is caused by charging and discharging the output capacitor, and is also due to its R_{ESR}. Table 8-5 shows how the R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the part's switching frequency.

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior, reduces the output voltage ripple, and decreases the PFM switching frequency. Note: the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (100-µF range) output capacitors. The output voltage might be slower than the programmed ramp rate at voltage transitions for large output capacitors, because of the higher energy stored on the output capacitance. Also, the time required to charge the output capacitor to target value might be longer at start-up. The output voltage is discharged to 0.6 V level using forced-PWM operation at shutdown. This can increase the input voltage if the load current is small and the output capacitor is large compared to the input capacitor. The output capacitor is discharged by the internal discharge resistor when below the 0.6 V level, and more time is required to settle VOUT down with a large capacitor because of the increased time constant.

Table 8-5. Recommended Buck Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GRM21BD71A226ME44	22 µF (10%)	0805	2 × 1.25 × 1.25	10 V
TDK	C2012X7S1A226M125AC	22 µF (20%)	0805	2 × 1.25 × 1.25	10 V

8.2.2.1.4 Boost Input Capacitor Selection

A ceramic input capacitor of 10 µF is sufficient for most applications. Place the input capacitor close to the SW_BST pin of the device. Use X7R types, do not use Y5V or F. See Table 8-6.

Table 8-6. Recommended Boost Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GRM21BR71A06KA73	10 µF (10%)	0805	2.0 × 1.25 × 1.25	10 V

8.2.2.1.5 Boost Output Capacitor Selection

Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. Place the output capacitor as close as possible to the device's VOUT_BST pin and PGND_BST pin. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to support load transients. See Table 8-7.

Table 8-7. Recommended Boost Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GRM21BD71A226ME44	22 µF (10%)	0805	2 × 1.25 × 1.25	10 V

8.2.2.1.6 Supply Filtering Components

The VANA input is used to supply analog and digital circuits in the device. See Table 8-8 recommended components from for VANA input supply filtering.

Table 8-8. Recommended Supply Filtering Components

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L×W×H (mm)	VOLTAGE RATING
Murata	GRT033C71C104KE01	0.1 nF (10%)	0201	0.6 × 0.3 × 0.3	16 V
Murata	GCM155R71C104KA55D	0.1 nF (10%)	0402	1.0 × 0.5 × 0.5	16 V

8.2.3 Current Limit vs Maximum Output Current

The current limit must be set high enough to account for the inductor ripple current on top of the maximum output current for the buck converters and boost. The forward current limit for the buck converters is set by BUCK0_ILIM, BUCK1_ILIM and for boost it is set by BOOST_ILIM.

For the buck converter the inductor current ripple can be calculated using Equation 1 and Equation 2:

$$D = \frac{V_{OUT}}{V_{IN(max)} \times \eta} \quad (1)$$

$$\Delta I_L = \frac{(V_{IN(max)} - V_{OUT}) \times D}{f_{SW} \times L} \quad (2)$$

Example using Equation 1 and Equation 2:

$V_{IN(max)}$ = 5.5 V
V_{OUT} = 1 V
η = 0.75
f_{SW} = 1.8 MHz
L = 0.38 µH
then D = 0.242 and ΔI_L = 1.59 A

Peak current is half of the current ripple. If $I_{LIM\_FWD\_SET\_OTP}$ is 3 A, the minimum forward current limit would be 2.85 A when taking the –5% tolerance into account. In this case the difference between set peak current and maximum load current = 0.795 A + 0.15 A = 0.945 A.

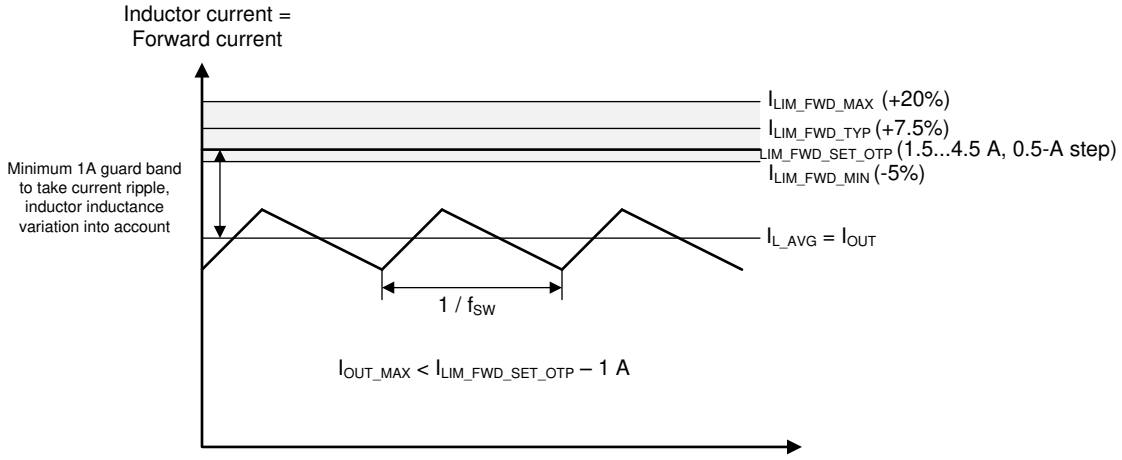


Figure 8-2. Current Limit vs Maximum Output Current

8.2.4 Application Curves

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT_BUCK} = 1 V, V_{OUT_BOOST} = 5 V, T_A = 25°C, f_{SW}-setting 4 MHz, L0 = L1 = 0.47 µH (TOKO DFE252012PD-R47M), L2 = 1 µH (TFM252012ALMA1R0), C_{OUT_BUCK}, C_{POL_BUCK}, and C_{OUT_BOOST} = 22 µF. Measurements are done using connections in Figure 8-1.

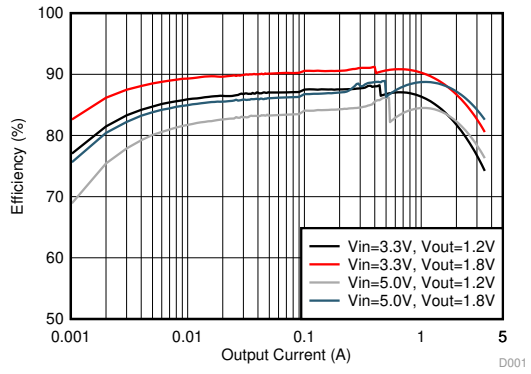
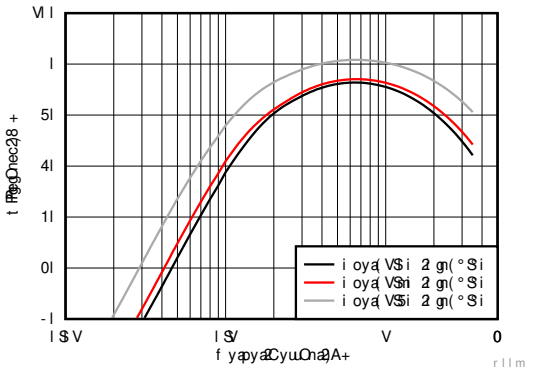
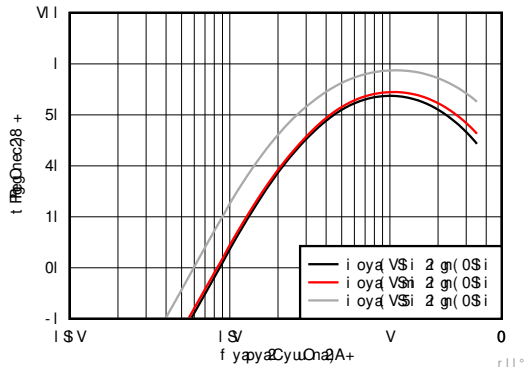


Figure 8-3. Buck Efficiency in AUTO (PFM/PWM) Mode



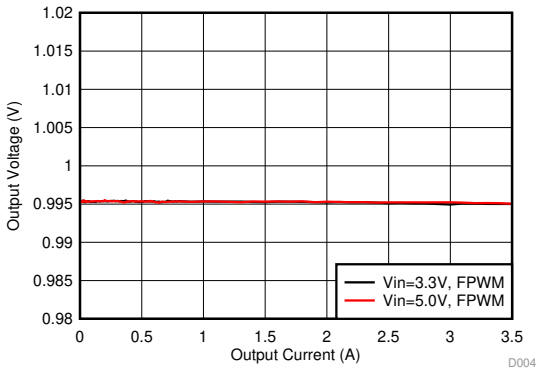
V_{IN} = 3.3 V

Figure 8-4. Buck Efficiency in Forced PWM Mode



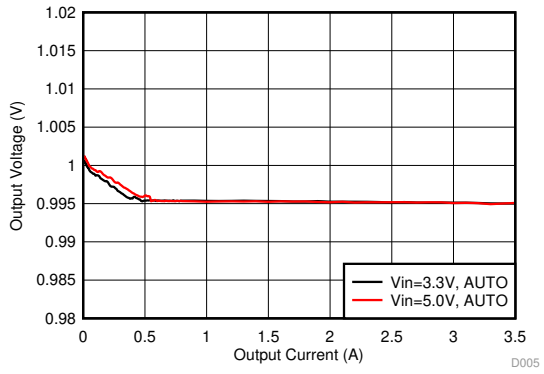
V_{IN} = 5 V

Figure 8-5. Buck Efficiency in Forced PWM Mode



V_{OUT} = 1 V

Figure 8-6. Buck Output Voltage vs Load Current in Forced PWM Mode



V_{OUT} = 1 V

Figure 8-7. Buck Output Voltage vs Load Current in AUTO Mode

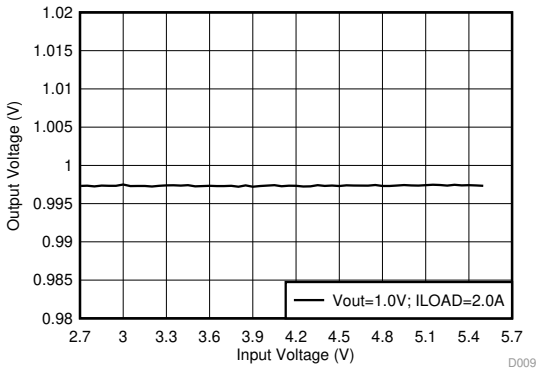


Figure 8-8. Buck Output Voltage vs Input Voltage in PWM Mode

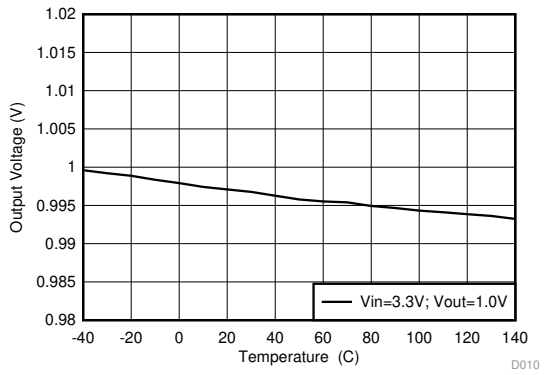
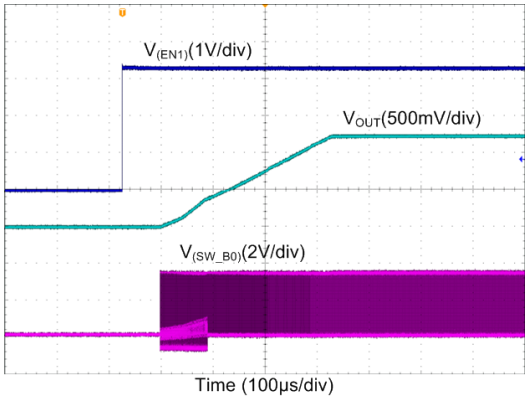
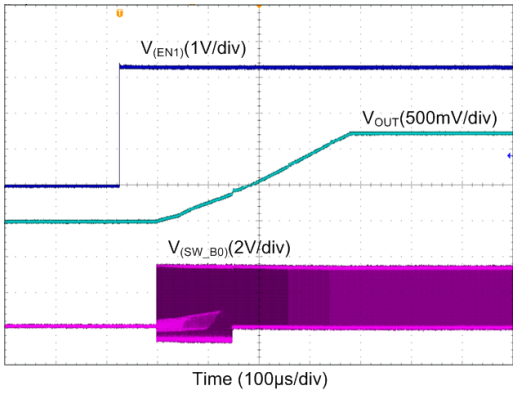


Figure 8-9. Buck Output Voltage vs Temperature



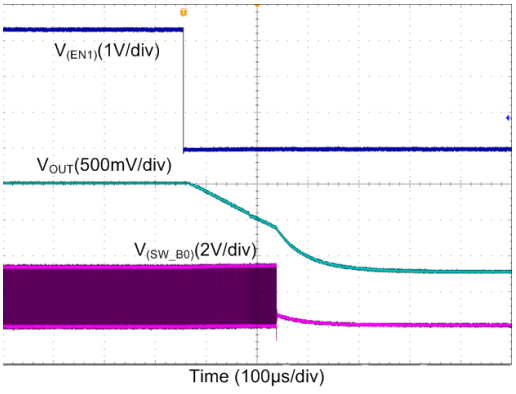
I_{OUT} = 0 A

Figure 8-10. Buck Start-up with EN1, Forced-PWM



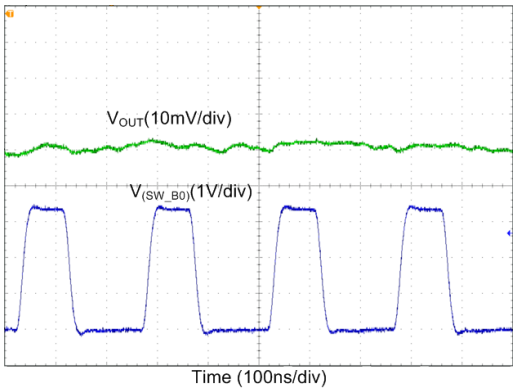
R_{LOAD} = 1 Ω

Figure 8-11. Buck Start-up with EN1, Forced-PWM



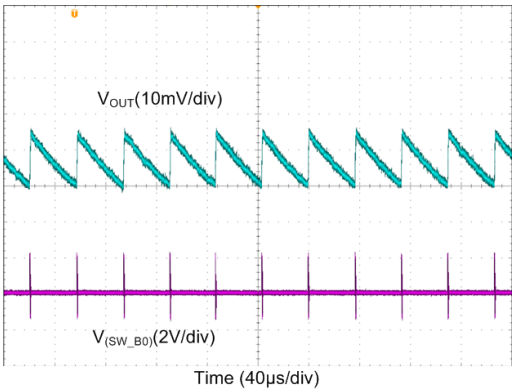
R_{LOAD} = 1 Ω

Figure 8-12. Buck Shutdown with EN1, Forced-PWM



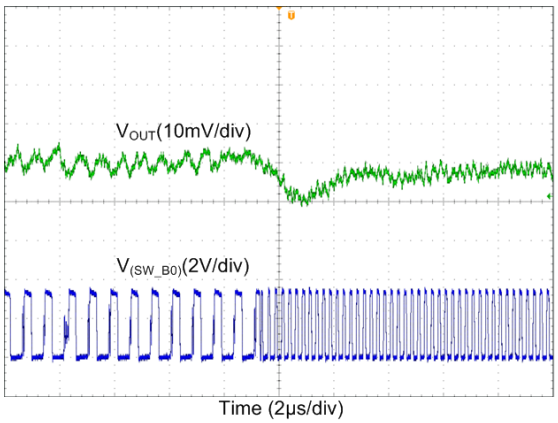
V_{OUT} = 1.2 V I_{OUT} = 500 mA

Figure 8-13. Buck Output Voltage Ripple, Forced-PWM Mode



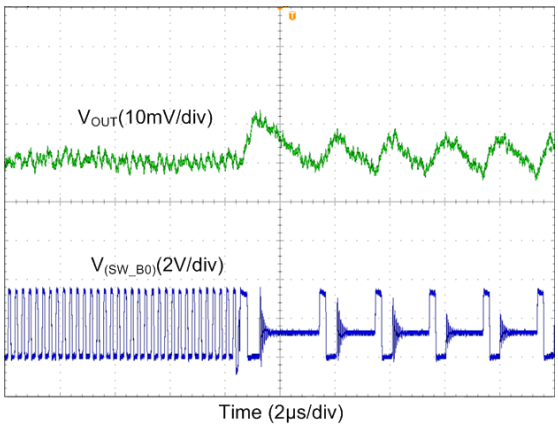
V_{OUT} = 1.2 V I_{OUT} = 10 mA

Figure 8-14. Buck Output Voltage Ripple, PFM Mode



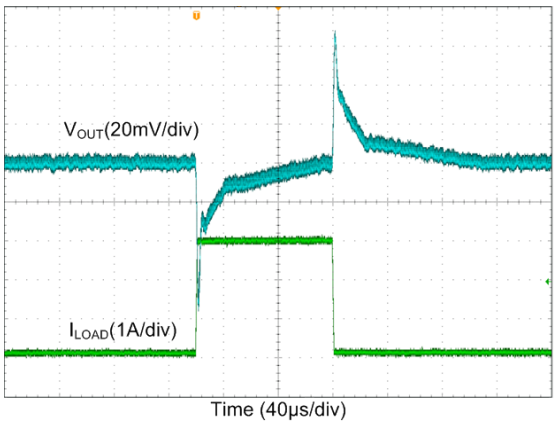
V_{OUT} = 1.2 V

Figure 8-15. Buck Transient from PFM-to-PWM Mode



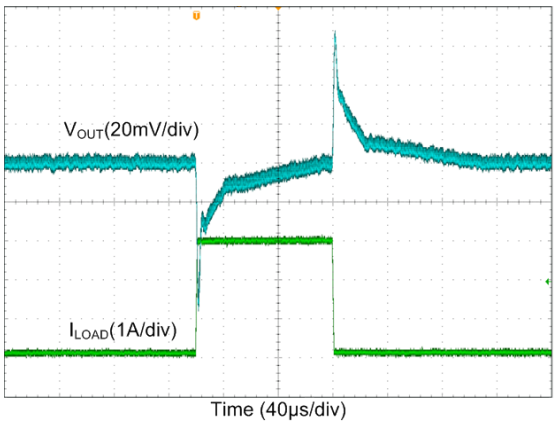
V_{OUT} = 1.2 V

Figure 8-16. Buck Transient from PWM-to-PFM Mode



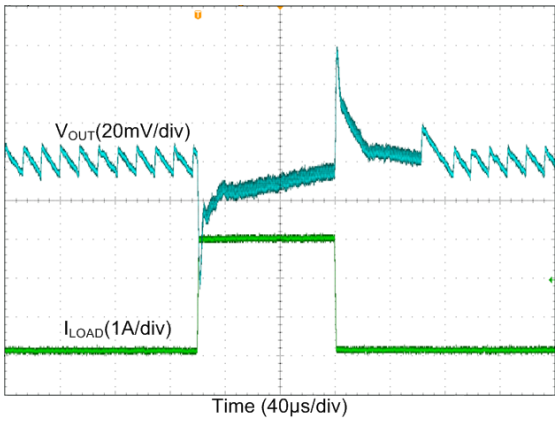
I_{OUT} = 0 A → 3 A → 0 A $T_R = T_F$ = 1 µs V_{OUT} = 1 V

Figure 8-17. Buck Transient Load Step Response, Forced-PWM Mode



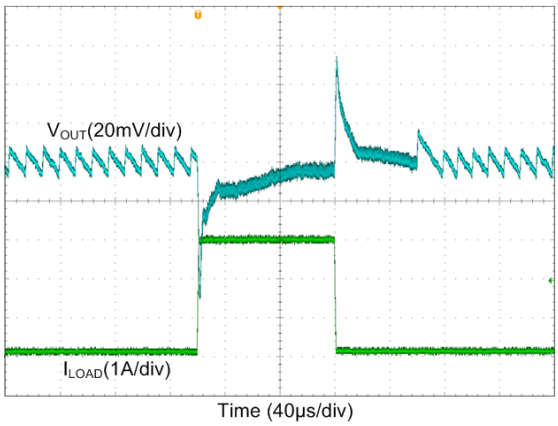
I_{OUT} = 0 A → 3 A → 0 A $T_R = T_F$ = 1 µs V_{OUT} = 1.2 V

Figure 8-18. Buck Transient Load Step Response, Forced-PWM Mode



I_{OUT} = 0 A → 3 A → 0 A T_R = T_F = 1 µs V_{OUT} = 1 V

Figure 8-19. Buck Transient Load Step Response, Auto Mode



V_{OUT} = 1.2 V

Figure 8-20. Buck Transient Load Step Response, Auto Mode

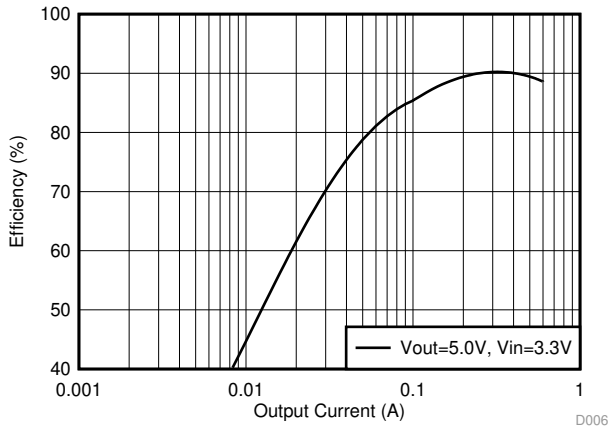


Figure 8-21. Boost Efficiency

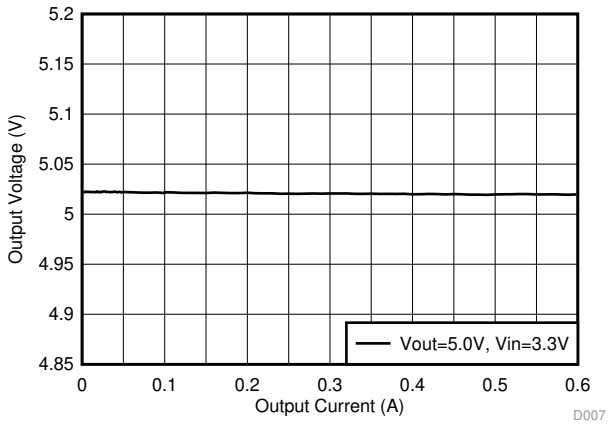
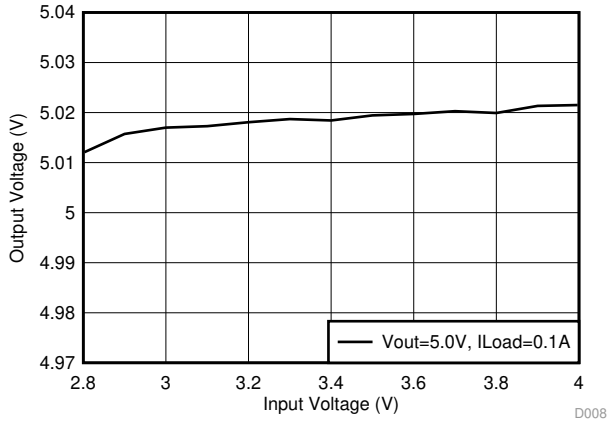
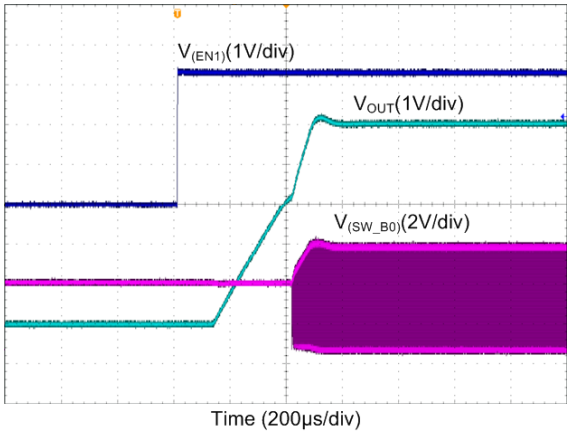


Figure 8-22. Boost Output Voltage vs Load Current



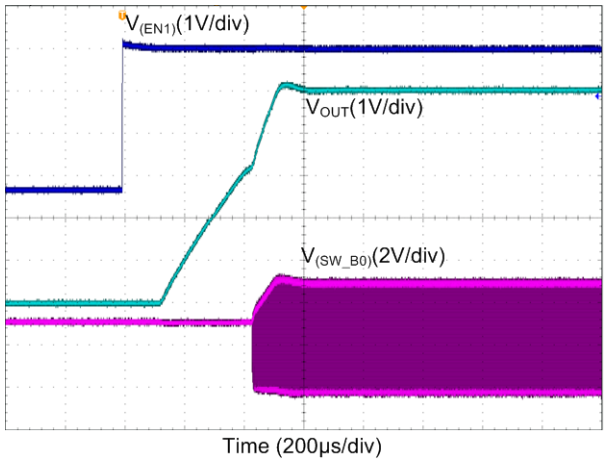
I_{OUT} = 0.1 A

Figure 8-23. Boost Output Voltage vs Input Voltage



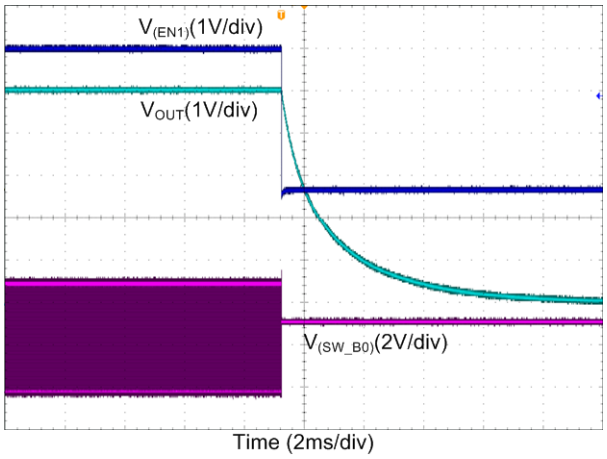
I_{OUT} = 0 A

Figure 8-24. Boost Start-up With EN1, Forced-PWM



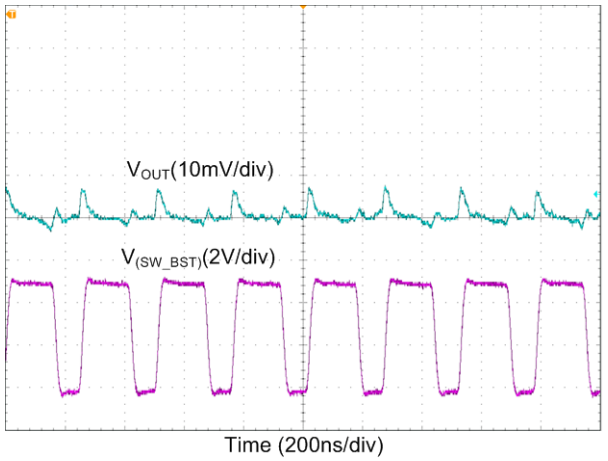
R_{LOAD} = 50 Ω

Figure 8-25. Boost Start-up With EN1, Forced-PWM



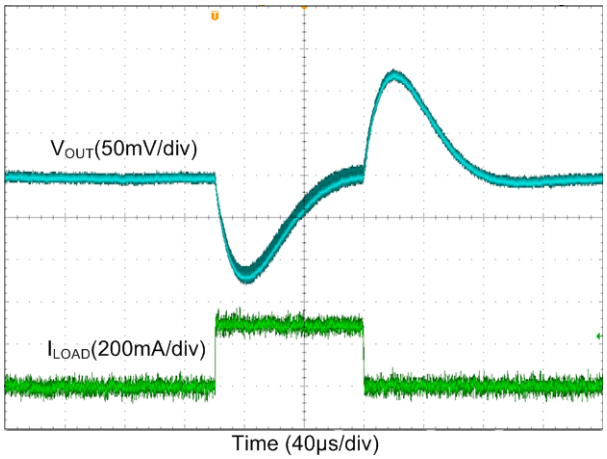
R_{LOAD} = 50 Ω

Figure 8-26. Boost Shutdown With EN1, Forced-PWM



I_{OUT} = 0.1 A

Figure 8-27. Boost Output Voltage Ripple



I_{OUT} = 0 A → 0.25 A → 0 A $T_R = T_F$ = 1 µs

Figure 8-28. Boost Transient Load Step Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high of a drop in the LP87702 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87702, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LP87702 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and one or more of the device VIN_Bx pins, as well as the trace between the negative node of the input capacitor and one or more of the power PGND_Bx pins must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor – parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of L and C_{OUT}, converts the switching signal at SW_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP87702 devices output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the device feedback pins FB_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C. Avoid capacitive and inductive coupling by keeping the sense lines short and direct. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane (if possible).
5. PGND_Bx, VIN_Bx and SW_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bx, VIN_Bx and SW_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances, which reduces the device junction temperature (T_J). TI strongly recommends performing a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

10.2 Layout Example

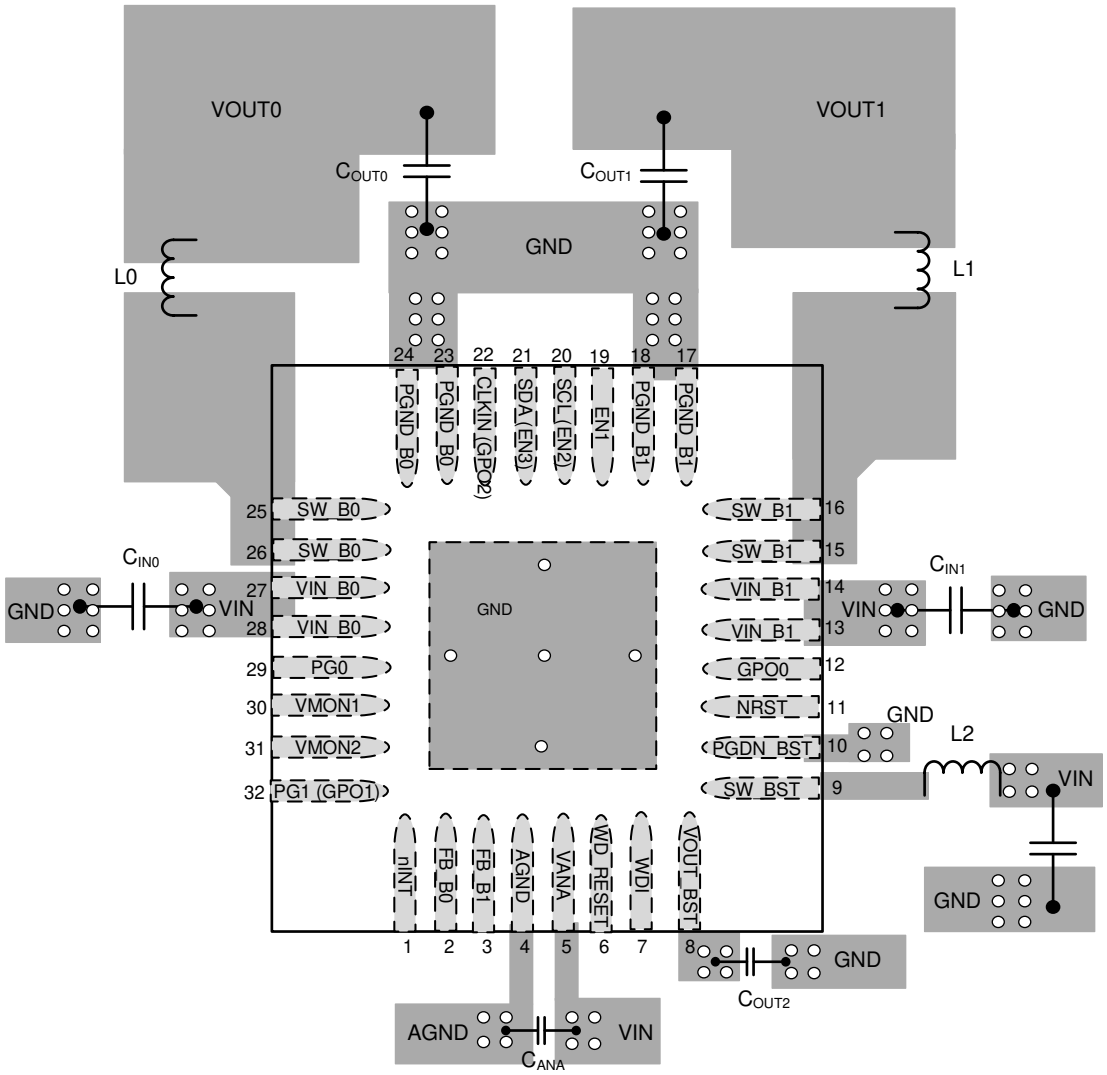


Figure 10-1. LP87702 Board Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, go to the device product folder on ti.com. In the upper right corner, click *Alert me* to register for a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP87702KRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 105	LP8770 2K RHB	Samples
LP87702KRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 105	LP8770 2K RHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LP87702 :

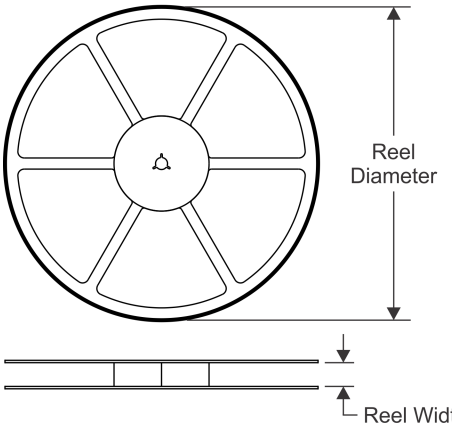
- Automotive : LP87702-Q1

NOTE: Qualified Version Definitions:

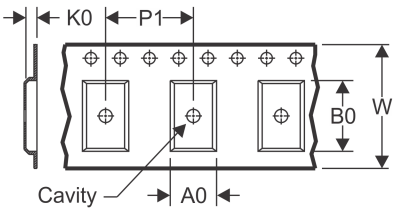
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

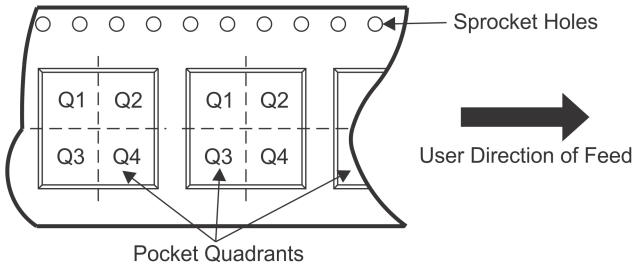


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

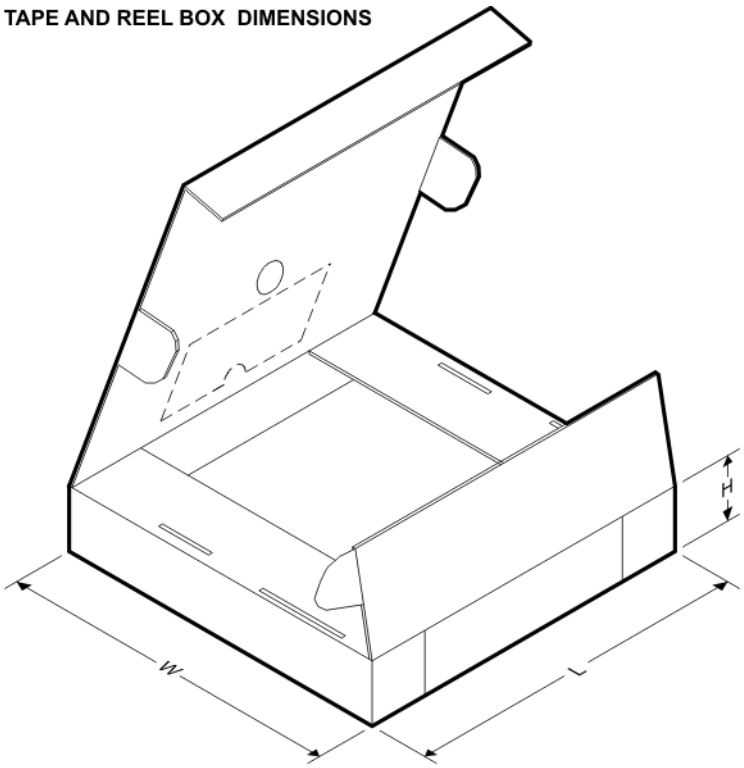
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP87702KRHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
LP87702KRHBT	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP87702KRHBR	VQFN	RHB	32	3000	367.0	367.0	38.0
LP87702KRHBT	VQFN	RHB	32	250	213.0	191.0	35.0

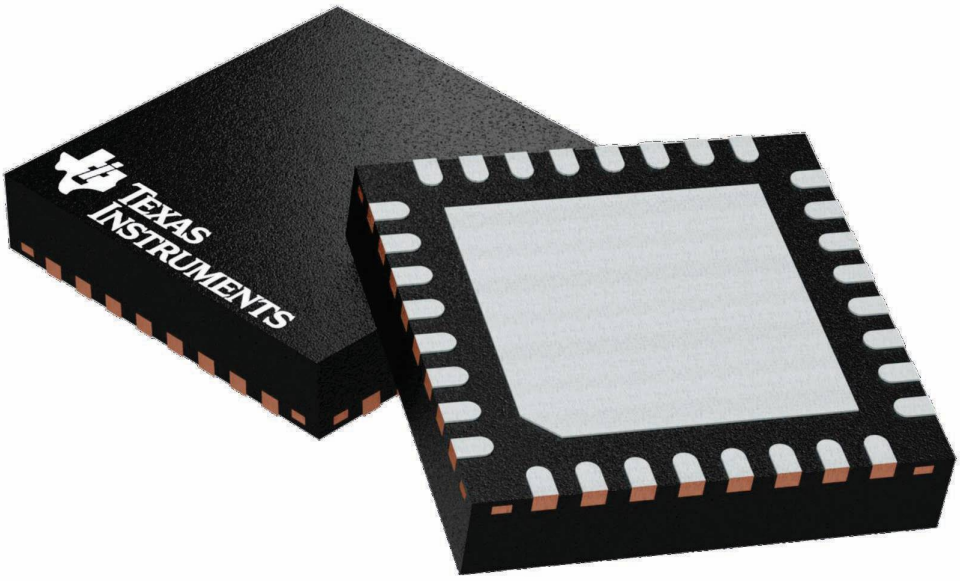
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

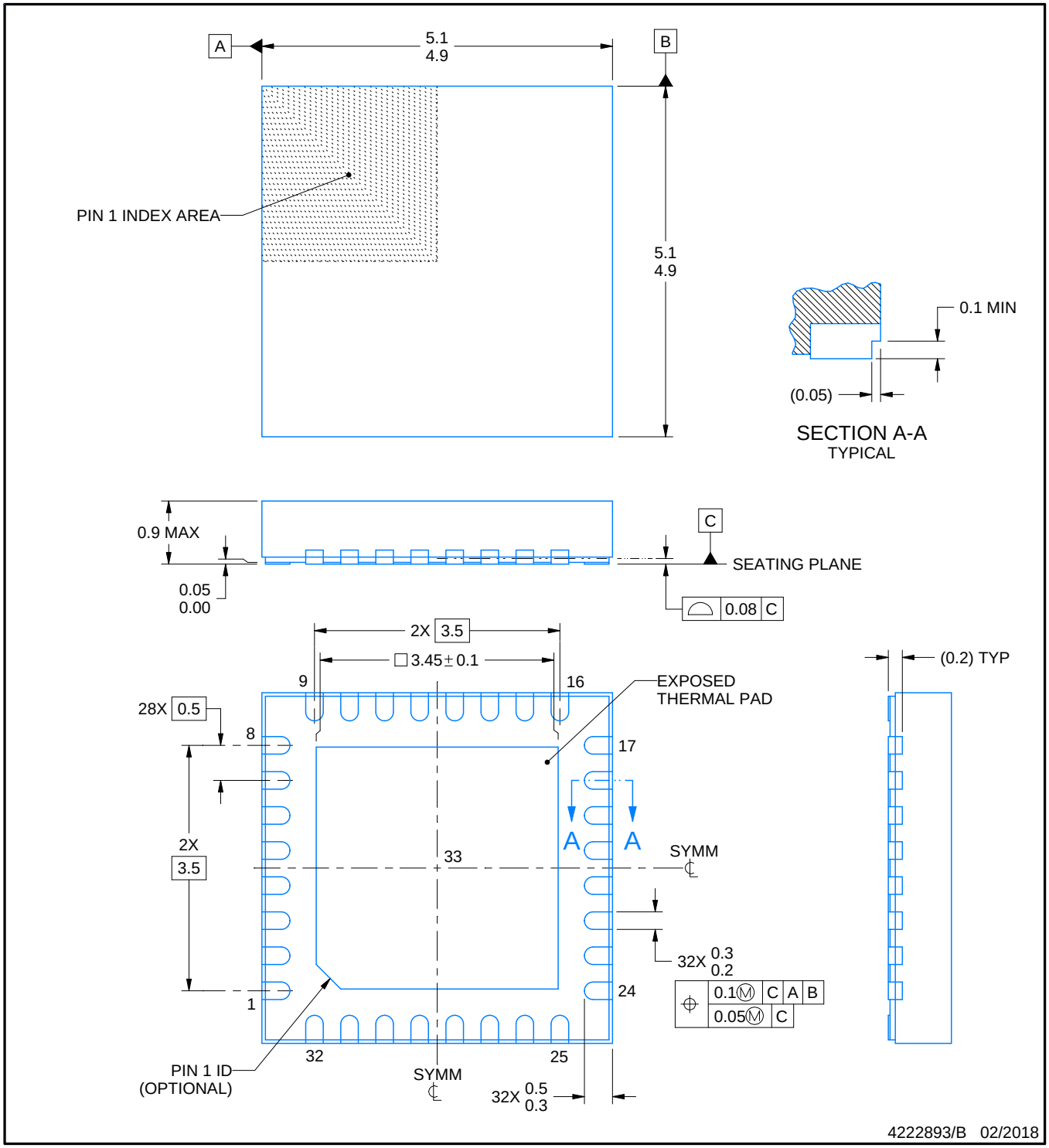
4224745/A

RHB0032N

PACKAGE OUTLINE

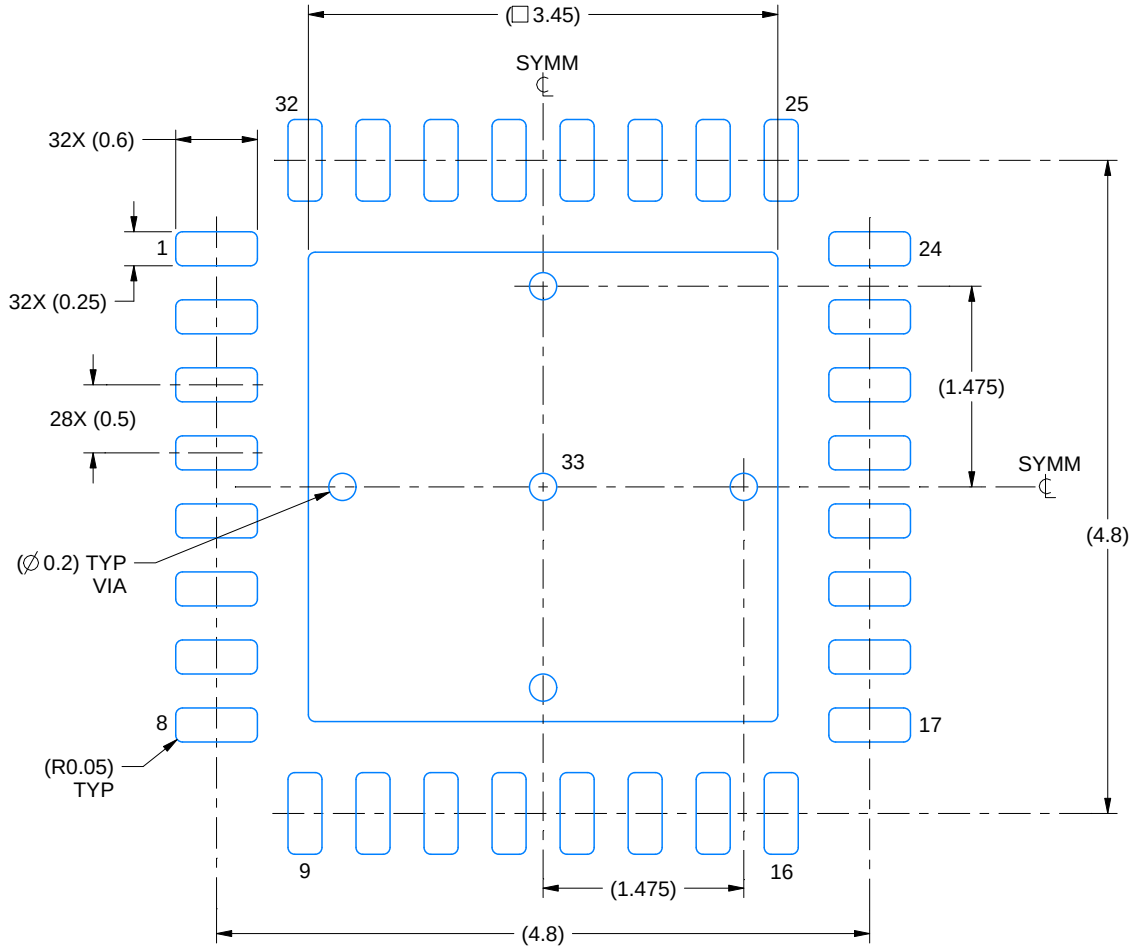
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

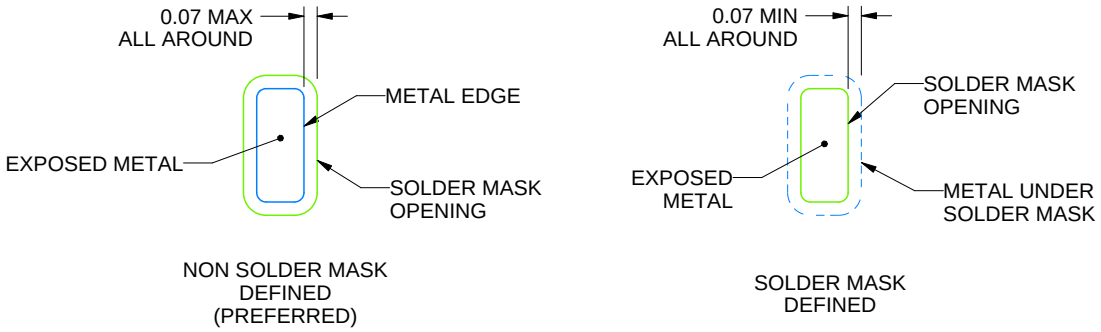


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

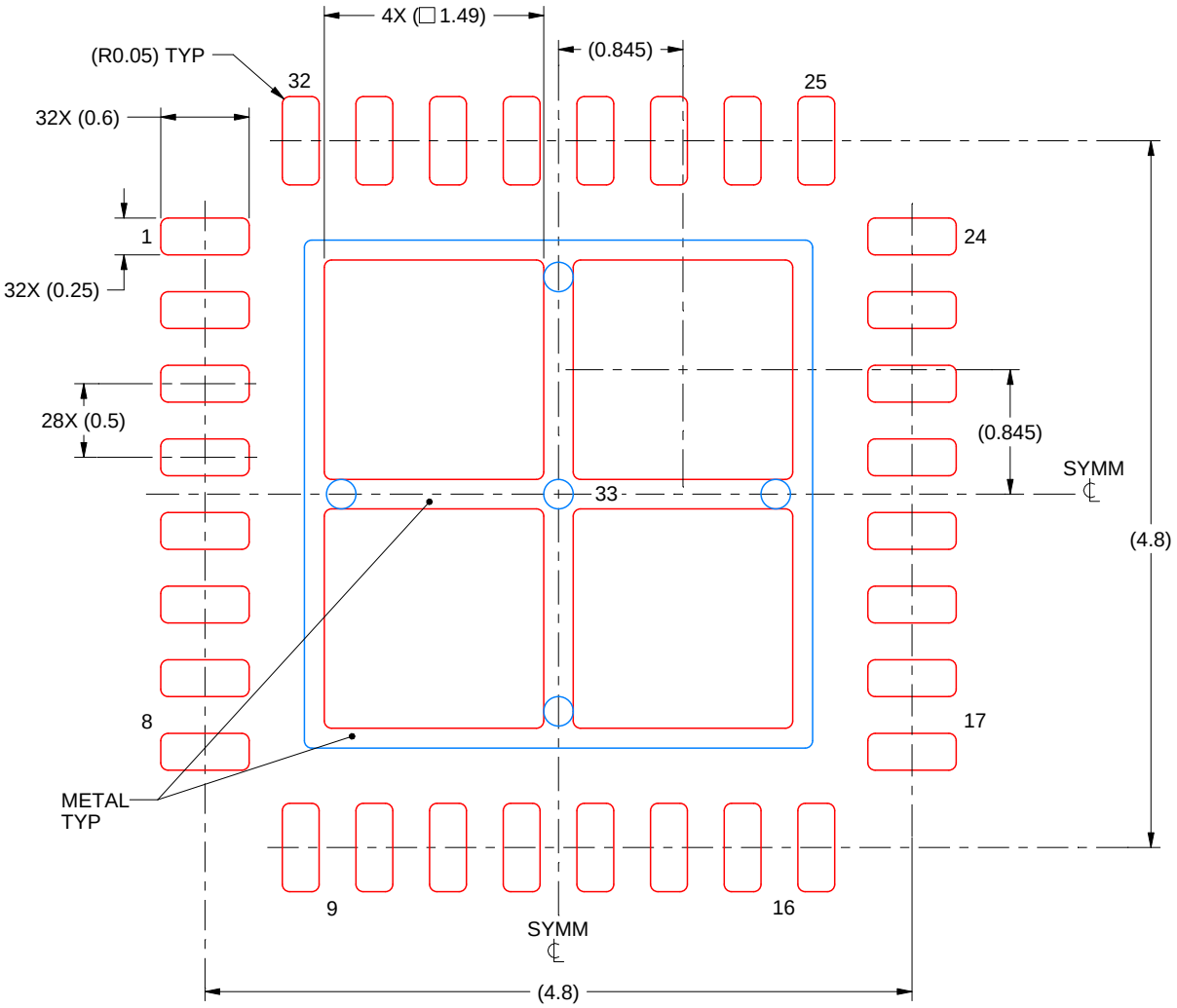


SOLDER MASK DETAILS

4222893/B 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222893/B 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

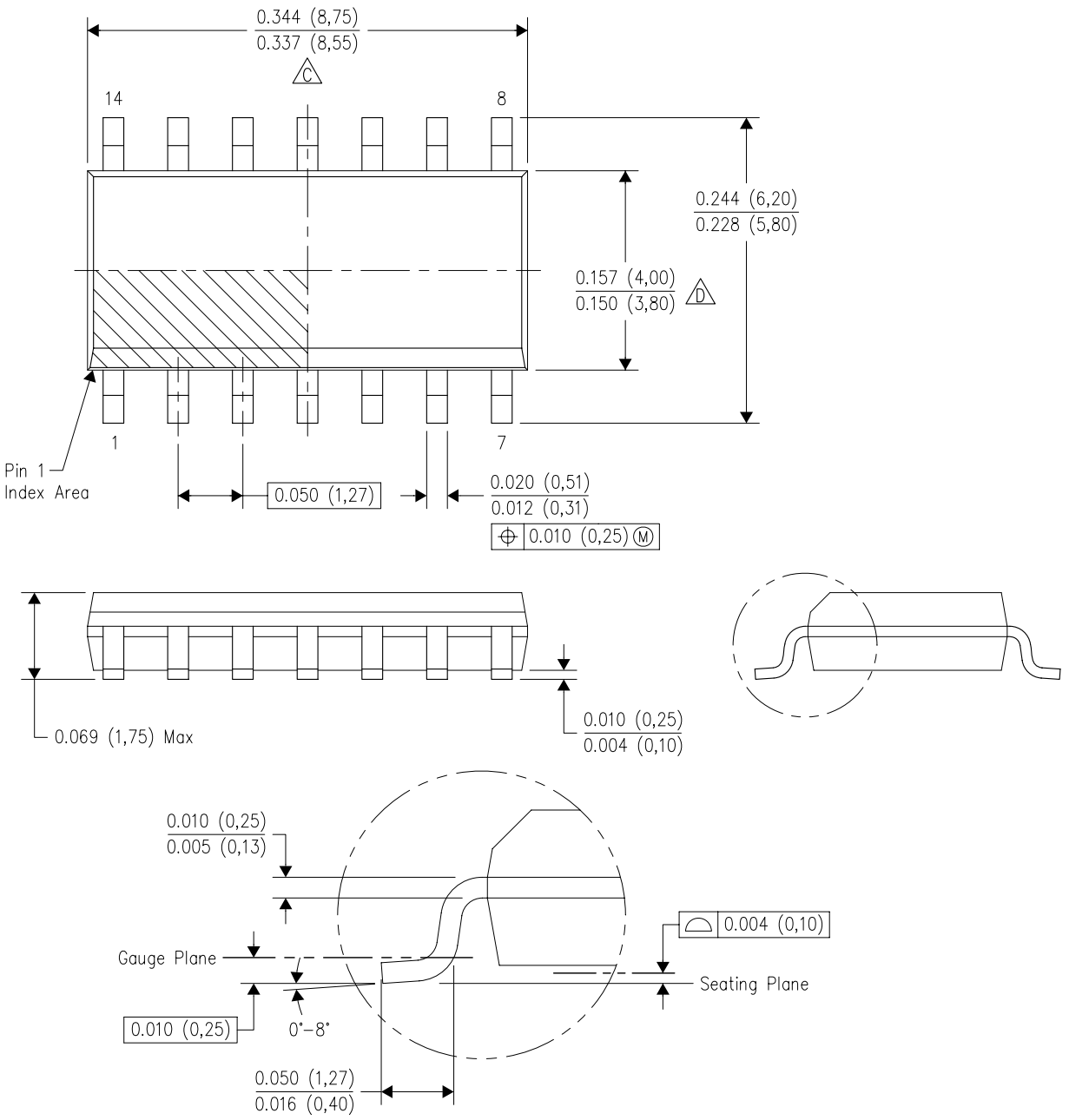
TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

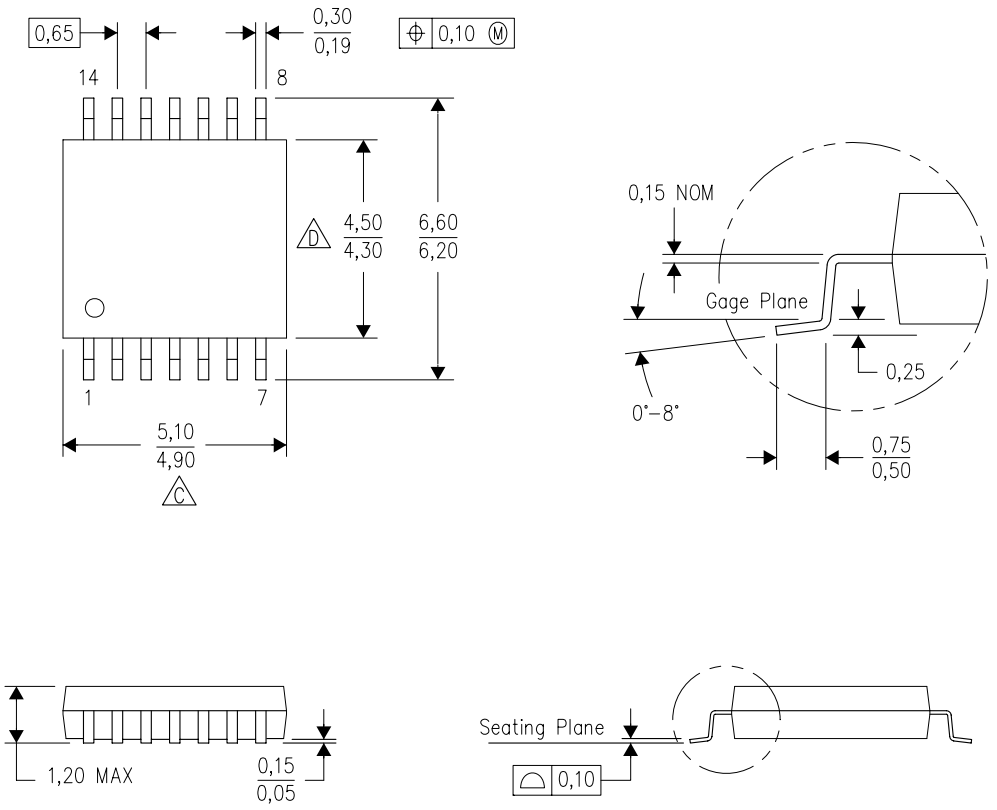
Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

TI E2E Community Home Page e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
OPA863, OPA2863, OPA4863
SBOS982F – JUNE 2020 – REVISED APRIL 2022

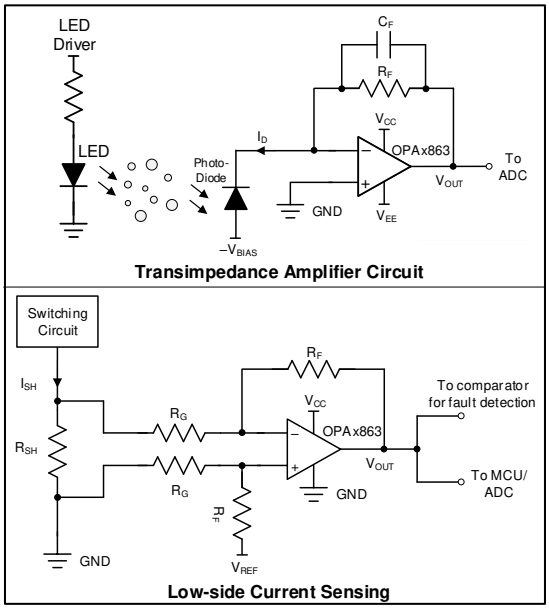
OPAx863 Low-Power, 110-MHz, Rail-to-Rail Input and Output Amplifier

1 Features

- Wide-bandwidth
  - Unity-gain bandwidth: 110-MHz (A_V= 1 V/V)
  - Gain-bandwidth product: 50-MHz
- Low power
  - Quiescent current: 700-µA/ch (typical)
  - Power down mode: 1.5-µA (maximum, V_S= 3 V)
  - Supply voltage: 2.7-V to 12.6-V
- Input voltage noise: 5.9-nV/√Hz
- Slew rate: 105-V/µs
- Rail-to-rail input and output
- HD_2/HD_3: –129 dBc/–138 dBc at 20 kHz (2-V_{PP})
- Operating temperature range: –40°C to +125°C
- Additional features:
  - Overload power limit
  - Output short-circuit protection

2 Applications

- Low-power SAR and ΔΣ ADC driver
- ADC reference buffer
- Low-side current sensing
- Photodiode TIA interface
- Inductive sensing
- Ultrasonic flow meters
- Multi-function printers
- MDAC output buffer
- Gain and active filter stages



Application Circuits Using OPAx863

3 Description

The OPAx863 devices are low-power, unity-gain stable, rail-to-rail input and output, voltage-feedback operational amplifiers designed to operate over a power supply range of 2.7-V to 12.6-V. Consuming only 700-µA per channel, the OPAx863 devices offer a gain-bandwidth product of 50-MHz, slew rate of 105-V/µs with a voltage noise density of 5.9-nV/√Hz.

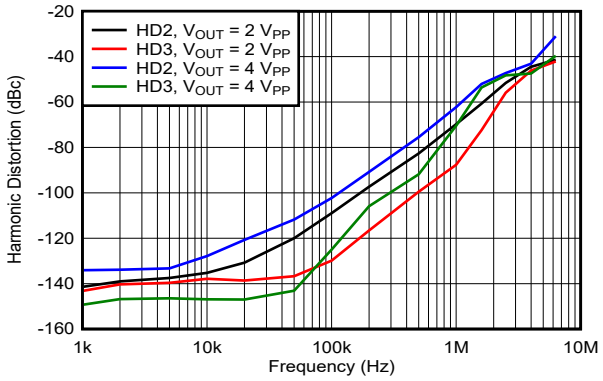
The rail-to-rail input stage with 2.7-V supply operation is useful in portable battery powered applications. The rail-to-rail input stage is well matched for gain-bandwidth product and noise across the full input common-mode voltage range, enabling superior performance with wide-input dynamic range. The OPA863 features a power-down (PD) mode with a PD quiescent current (I_Q) of 1.5-µA (maximum) with turn-on or turn-off within 6.5-µs with a 3-V supply.

The OPAx863 devices include overload power limiting to limit the increase in I_Q with saturated outputs, thereby preventing excessive power dissipation in power conscious battery-operated systems. The output stage is short-circuit protected, making it conducive to ruggedized environments.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA863	SOT23 (6)	2.90 mm × 1.60 mm
OPA2863	VSSOP (8)	3.00 mm × 3.00 mm
	WQFN (10)(2)	2.00 mm × 2.00 mm
	SOIC (8)(2)	4.90 mm × 3.91 mm
OPA4863	TSSOP (14)(2)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview packages.



Distortion Performance in G = 1 V/V

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2021) to Revision F (April 2022)	Page
• Added the D package, 8-pin SOIC and RUN package, 10-pin WQFN to the data sheet	1

Changes from Revision D (July 2021) to Revision E (November 2021)	Page
• Updated the title of the data sheet	1
• Updated the *Description* section	1
• Changed the status of the DBV Package, from: *preview* to: *production*	4
• Removed footnote from Electrical Characteristics: 10 V and Electrical Characteristics: 3 V tables	9
• Removed the links to the *Noninverting* and *Inverting Amplifier* figures in the *Typical Characteristics: V_S = 10 V*, *Typical Characteristics: V_S = 3 V*, and *Typical Characteristics: V_S = 3 V to 10 V* sections	13
• Updated the title of the *Frequency Response vs Load Capacitance*, *Frequency Response vs Ambient Temperature*, and *Frequency Response vs Output Voltage* figures in the *Typical Characteristics: V_S = 10 V* section	13
• Added the *Quiescent Current Distribution*, *Input Bias Current Distribution*, *Input Offset Voltage Distribution*, *Input Offset Voltage Drift Distribution*, *Input Offset Voltage Drift Distribution*, *Quiescent Current vs Ambient Temperature*, *Input Bias Current vs Ambient Temperature*, *Input Offset Voltage vs Ambient Temperature*, *Turn-On Time to DC InputTurn-Off Time to DC Input*, *Power-Down Quiescent Current Distribution*, and *Power-Down I_Q vs Ambient Temperature* figures to the *Typical Characteristics: V_S = 10 V* section	13
• Updated the titles to the *Frequency Response vs Supply Voltage* figures in the *Typical Characteristics: V_S = 3 V to 10 V* section	20
• Removed the *units* from the *Quiescent Current Distribution*, *Input Bias Current Distribution*, and *Input Offset Voltage Distribution* figures in the *Typical Characteristics: V_S = 3 V to 10 V* section	20
• Removed the *DGK package* from the *Quiescent Current vs Ambient Temperature* and *Input Bias Current vs Ambient Temperature* figures in the *Typical Characteristics: V_S = 3 V to 10 V* section	20
• Updated the *Common-Mode Rejection Ratio vs Frequency*, *Power Supply Rejection Ratio vs Frequency*, and *Open-Loop Gain and Phase vs Frequency* figures in the *Typical Characteristics: V_S = 3 V to 10 V* section	20

- Removed the *Quiescent Current Distribution*, *Input Bias Current Distribution*, *Input Offset Voltage Distribution*, *Input Offset Voltage Drift Distribution*, *Quiescent Current vs Ambient Temperature*, *Input Bias Current vs Ambient Temperature*, and *Input Offset Voltage vs Ambient Temperature* figures from the *Typical Characteristics: V_S = 3 V to 10 V* section....20
- Updated the *Overview* section....22
- Updated the *Input Stage* section....23
- Updated the *ESD Protection* section....24
- Updated the *Power-Down Mode* section....24
- Removed the *Split-Supply Operation (±1.35 V to ±6.3 V)*, *Single-Supply Operation (2.7 V to 12.6 V)*, *Amplifier Gain Configurations*, *Transimpedance Amplifier*, *Design Requirements*, *Detailed Design Procedure*, and *Application Curves* sections....25
- Updated the *Clamp-On Ultrasonic Flow Meter* section....28
- Updated the *Layout Guidelines* section....29
- Updated the *Thermal Considerations* section....30
- Updated the *Layout Recommendation* figure title in the *Layout Example* section....30

Changes from Revision C (April 2021) to Revision D (July 2021) **Page**

- Added Thermal Information for OPA4863PW to the Specifications section....8

Changes from Revision B (April 2021) to Revision C (April 2021) **Page**

- Removed A from the device name OPAx863 in the *Description* section....1
- Removed A from the device name OPAx863 in the *Device Comparison Table* section....4
- Added power-down mode information for DBV package to the datasheet....9

Changes from Revision A (June 2020) to Revision B (April 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Changed the status of the data sheet from: advanced information to: production data....1

5 Device Comparison Table

DEVICE	±V_S (V)	I_Q / CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPAx863	±6.3	0.70	50	105	5.9	Unity-gain stable RRIO Bipolar Amplifier
LMH6643	±6.4	2.7	65	130	17	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx810	±13.5	3.6	70	200	6.3	Unity-gain stable RRIO FET-Input Amplifier
OPAx837	±2.7	0.6	50	105	4.7	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx607	±2.75	0.9	50	24	3.8	Decompensated Gain of 6 V/V stable CMOS Amplifier

6 Pin Configuration and Functions

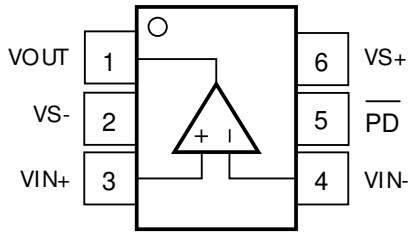


Figure 6-1. DBV Package, 6-Pin SOT-23 (Top View)

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	OPA863 SOT-23		
$\overline{PD}$	5	I	Power down. Low = disabled, high = normal operation (pin must be driven).
VIN+	3	I	Noninverting input pin
VIN–	4	I	Inverting input pin
VOUT	1	O	Output pin
VS–	2	P	Negative power-supply pin
VS+	6	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

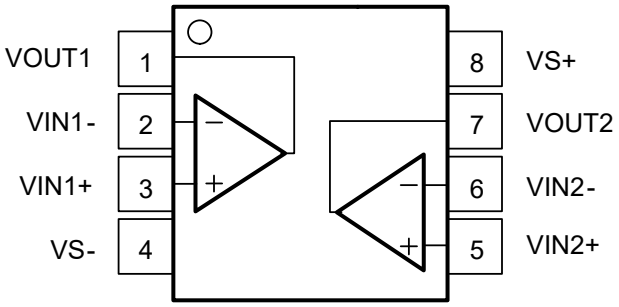


Figure 6-2. D Package (Preview), 8-Pin SOIC and DGK Package, 8-Pin VSSOP, (Top View)

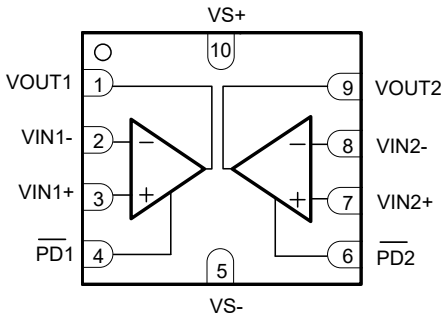


Figure 6-3. RUN Package (Preview), 10-Pin WQFN (Top View)

Table 6-2. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	OPA2863			
	SOIC, VSSOP	WQFN		
$\overline{PD1}$	—	4	I	Amplifier 1 power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD2}$	—	6	I	Amplifier 2 power down. Low = disabled, high = normal operation (pin must be driven).
VIN1–	2	2	I	Amplifier 1 inverting input pin
VIN1+	3	3	I	Amplifier 1 noninverting input pin
VIN2–	6	8	I	Amplifier 2 inverting input pin
VIN2+	5	7	I	Amplifier 2 noninverting input pin
VOUT1	1	1	O	Amplifier 1 output pin
VOUT2	7	9	O	Amplifier 2 output pin
VS–	4	5	P	Negative power-supply pin
VS+	8	10	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

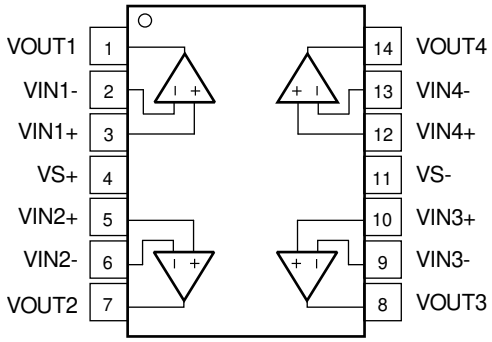


Figure 6-4. PW Package, Preview 14-Pin TSSOP (Top View)

Table 6-3. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	OPA4863 TSSOP		
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2–	6	I	Amplifier 2 inverting input pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VIN3–	9	I	Amplifier 3 inverting input pin
VIN3+	10	I	Amplifier 3 noninverting input pin
VIN4–	13	I	Amplifier 4 inverting input pin
VIN4+	12	I	Amplifier 4 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	7	O	Amplifier 2 output pin
VOUT3	8	O	Amplifier 3 output pin
VOUT4	14	O	Amplifier 4 output pin
VS–	11	P	Negative power-supply pin
VS+	4	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt, DBV package		0.1	V/µs
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across it to 1 V with this continuous input current flowing through it.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply positive voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information: OPA863

THERMAL METRIC(1)		OPA863 DBV (SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	42.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2863

THERMAL METRIC(1)		OPA2863 DGK (VSSOP) 8 PINS	OPA2863 D (SOIC) 8 PINS	OPA2863 RUN (WQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	120.0	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.5	63.3	66.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.9	63.2	43.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	17.2	2.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	100.1	62.5	43.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4863

THERMAL METRIC(1)		OPA4863 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		110		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2–V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200–mV step		9		ns
	Settling time to 0.1%	V_{OUT} = 2–V step		57		ns
	Settling time to 0.01%			70		
	Overshoot/undershoot	V_{OUT} = 2–V step		1		%
	Overdrive recovery time	G = –1, 0.5 V overdrive beyond supplies		70		ns
		G = 1, 0.5 V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion			–138		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion			–125		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		5.9		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}		–124		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = –40°C to +125°C, DGK package	–3.5	±1	3.5	µV/°C
		T_A = 0°C to +85°C, DBV package	–4.4	±1	4.4	
		T_A = –40°C to +125°C, DBV package	–4.9	±1	4.9	
	Input bias current	T_A ≈ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.6	nA/°C
	Input offset current		-30	±10	30	nA
INPUT						
	Input common-mode voltage range		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM}=$V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	100	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≈ 25°C		$V_{S–}$+0.14	$V_{S–}$+0.2	V
		T_A = –40°C to +125°C		$V_{S–}$+0.15	$V_{S–}$+0.22	
V_{OH}	Output voltage, high	T_A ≈ 25°C	V_{S+}–0.2	V_{S+}–0.14		V
		T_A = –40°C to +125°C	V_{S+}–0.2	V_{S+}–0.15		
	Linear output drive (sourcing/sinking)	V_{OUT} = ±2.5 V, ΔV_{IO} < 1 mV(2)	25	30		mA
	Short-circuit current			45		mA

7.7 Electrical Characteristics: 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≈ 25°C		700	970	μA
		T_A = –40°C to +125°C			1280	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(1)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+}–0.5 V			4.5	V
	Disable voltage threshold	Specified *off* below V_{S+}–1.5 V	3.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+}–1.5 V		2	3.3	μA
	Power-down pin bias current			2	50	nA
	Turn-on time delay			6		μs
	Turn-off time delay			4.5		μs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≈ 25°C		0.2	0.6	μA
		T_A = –40°C to +125°C		0.2	1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	120		dB

(1) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.
(2) Change in input offset voltage from no-load condition.

7.8 Electrical Characteristics: 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		97		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		26		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1–V step, Gain = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200–mV step		10		ns
	Settling time to 0.1%	V_{OUT} = 1–V step		58		ns
	Settling time to 0.01%			90		
	Overshoot	V_{OUT} = 1–V step		2		%
	Undershoot			16		
	Overdrive recovery time	G = –1, 0.5V overdrive beyond supplies		95		ns
		G = 1, 0.5V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–123		dBc
HD3	Third-order harmonic distortion			–132		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–109		dBc
HD3	Third-order harmonic distortion			–129		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}		–127		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		–1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = –40°C to +125°C, DGK package	–3.5	±1	3.5	uV/°C
		T_A = 0°C to +85°C, DBV package	–4.4	±1	4.4	
		T_A = –40°C to +125°C, DBV package	–5	±1	5	
	Input bias current	T_A ≈ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.56	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.4	nA/°C
	Input offset current		-30	±10	30	nA
INPUT						
	Input common-mode voltage range		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	94	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≈ 25°C		$V_{S–}$+ 0.13	$V_{S–}$+ 0.15	V
		T_A = –40°C to +125°C		$V_{S–}$+ 0.13	$V_{S–}$+ 0.16	
V_{OH}	Output voltage, high	T_A ≈ 25°C	V_{S+}–0.15	V_{S+}–0.13		V
		T_A = –40°C to +125°C	V_{S+}–0.15	V_{S+}–0.13		

7.8 Electrical Characteristics: 3 V (continued)

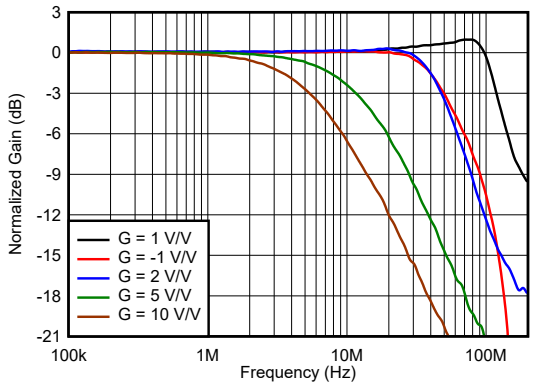
at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≈ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linear output drive (sourcing/sinking)	V_{OUT} = ±0.7 V, ΔV_{IO} < 1 mV(2)	23	33		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≈ 25°C		690	910	µA
		T_A = –40°C to +125°C			1180	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(1)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			2.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	1.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+} – 1.5 V		0.8	1.5	µA
	Power-down pin bias current			1	50	nA
	Turn-on time delay			6.5		µs
	Turn-off time delay			5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≈ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.4	1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	115		dB

(1) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.
(2) Change in input offset voltage from no-load condition.

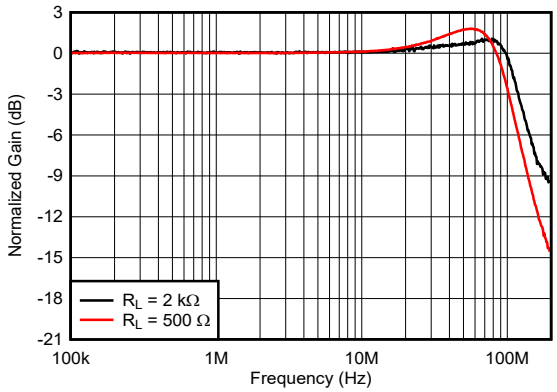
7.9 Typical Characteristics: V_S = 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



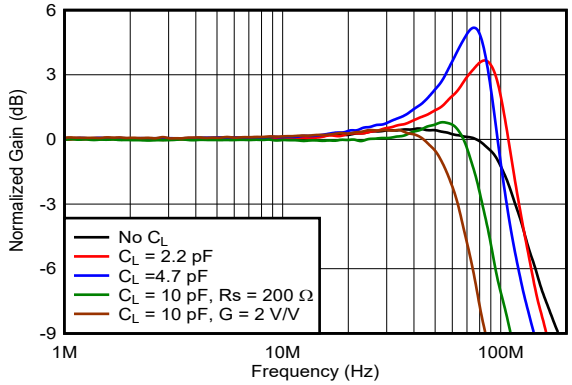
V_{OUT} = 20 mV_{PP}

Figure 7-1. Small-Signal Frequency Response vs Gain



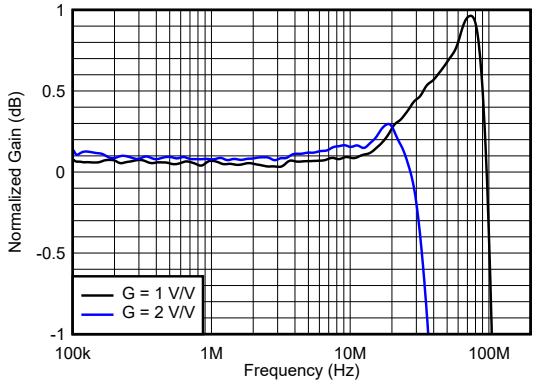
V_{OUT} = 20 mV_{PP}

Figure 7-2. Small-Signal Frequency Response vs Output Load



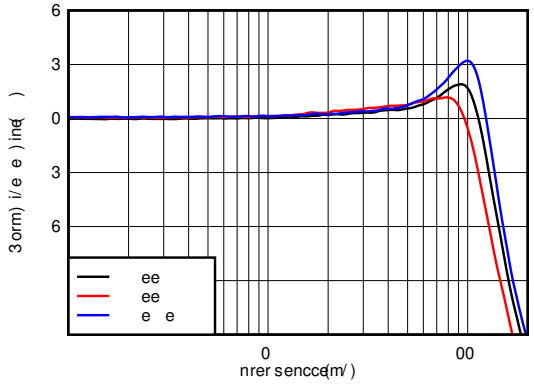
V_{OUT} = 20 mV_{PP}

Figure 7-3. Frequency Response vs Load Capacitance



V_{OUT} = 20 mV_{PP}

Figure 7-4. Small-Signal Response Flatness vs Gain



V_{OUT} = 20 mV_{PP}

Figure 7-5. Frequency Response vs Ambient Temperature

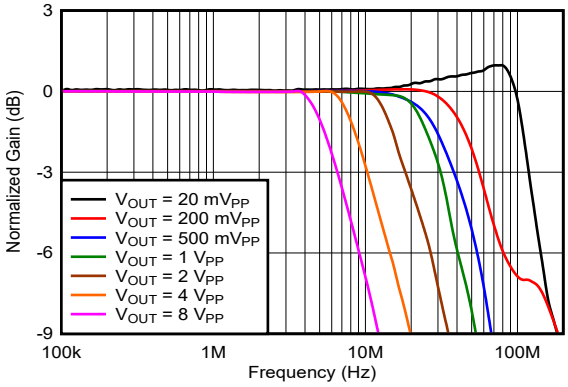
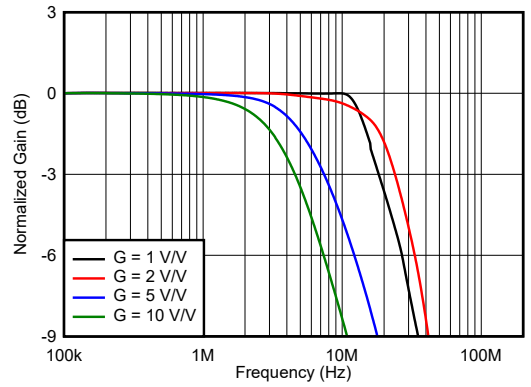


Figure 7-6. Frequency Response vs Output Voltage

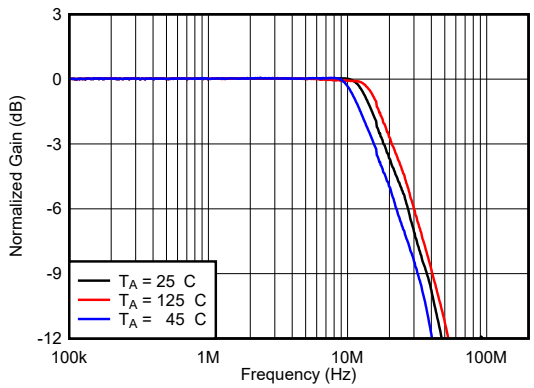
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



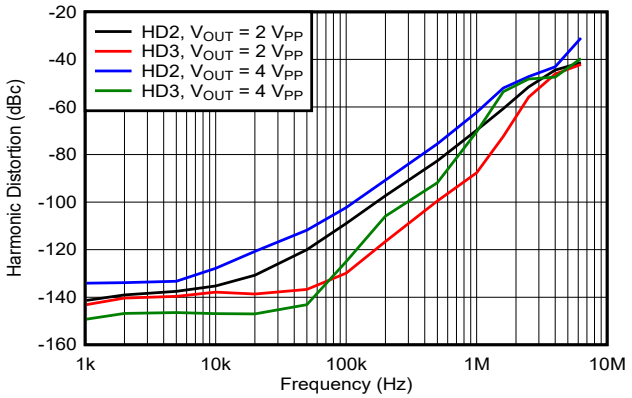
V_{OUT} = 2 V_{PP}

Figure 7-7. Large-Signal Frequency Response vs Gain



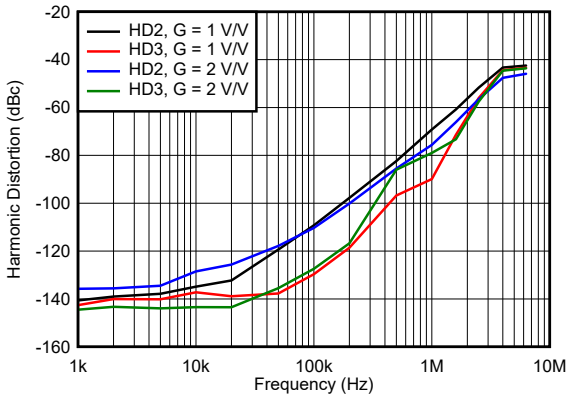
V_{OUT} = 2 V_{PP}

Figure 7-8. Frequency Response vs Ambient Temperature



G = 1 V/V

Figure 7-9. Harmonic Distortion vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-10. Harmonic Distortion vs Gain

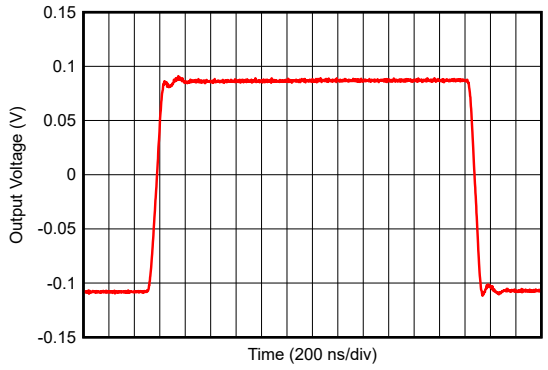


Figure 7-11. Small-Signal Transient Response

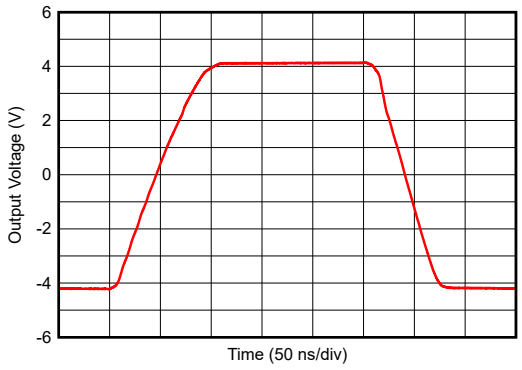


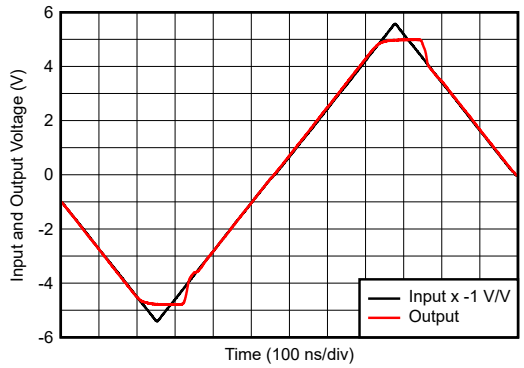
Figure 7-12. Large-Signal Transient Response

7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

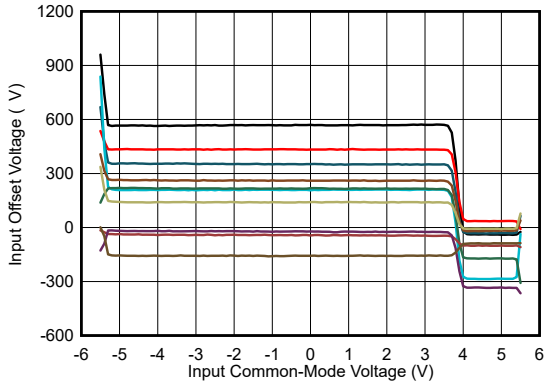
Gain = 1 V/V

Figure 7-13. Input Overdrive Recovery



Gain = -1 V/V

Figure 7-14. Output Overdrive Recovery



Measured for 10 units

Figure 7-15. Input Offset Voltage vs Input Common-Mode Voltage

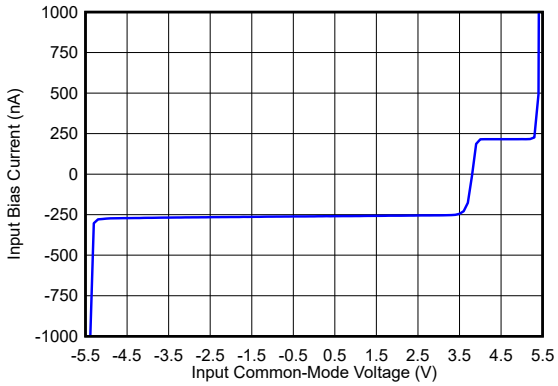


Figure 7-16. Input Bias Current vs Input Common-Mode Voltage

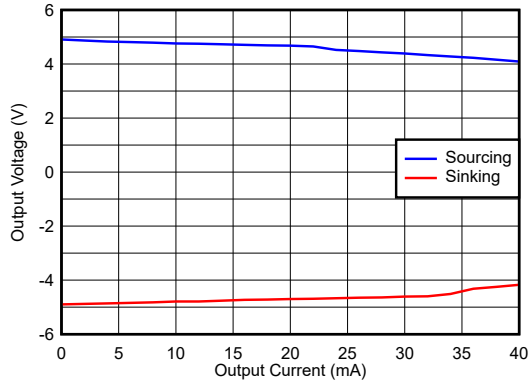
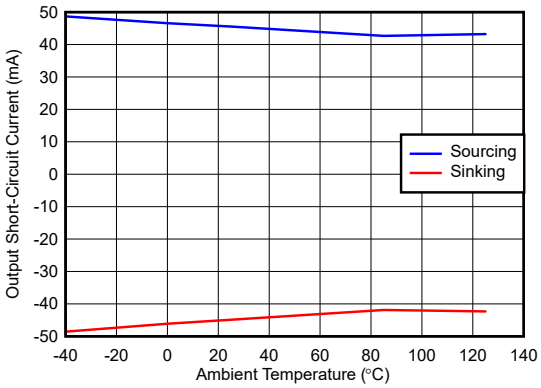


Figure 7-17. Output Voltage vs Load Current

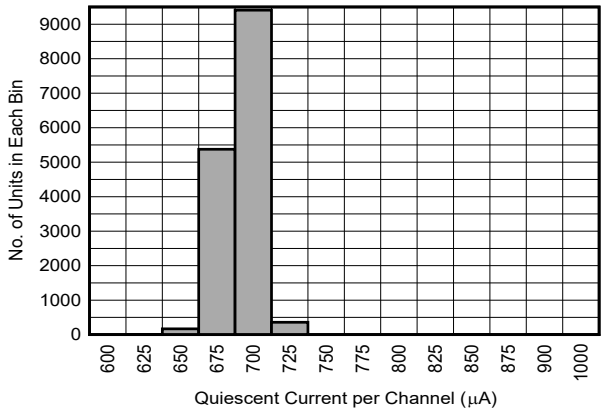


Output saturated and then short-circuited to opposite supply

Figure 7-18. Output Short-Circuit Current vs Ambient Temperature

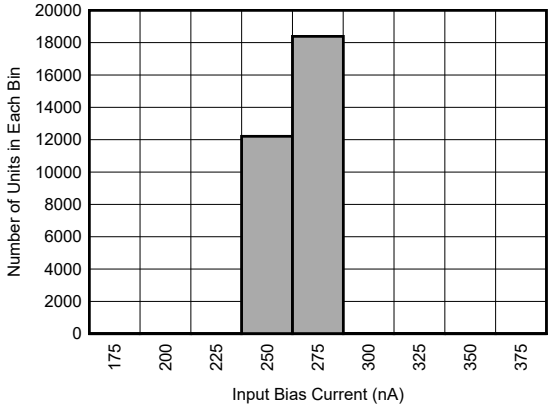
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



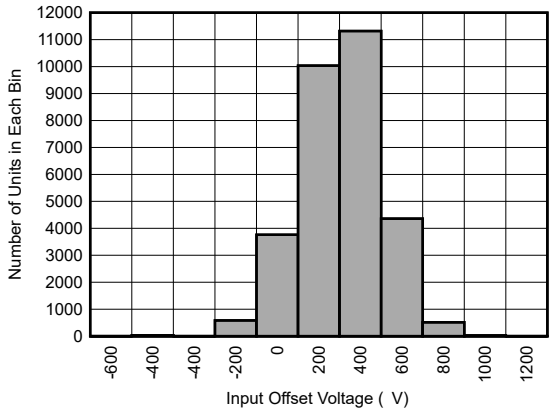
µ = 678 µA, σ = 13 µA

Figure 7-19. Quiescent Current Distribution



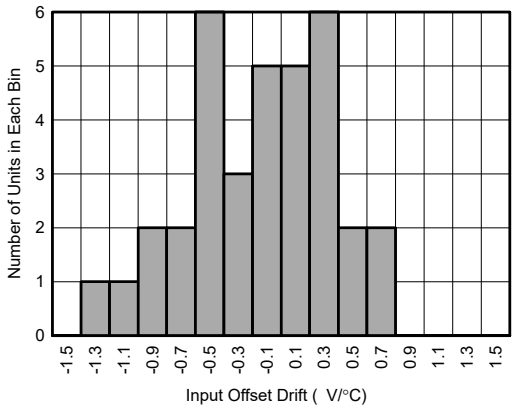
µ = 251 nA, σ = 5.6 nA

Figure 7-20. Input Bias Current Distribution



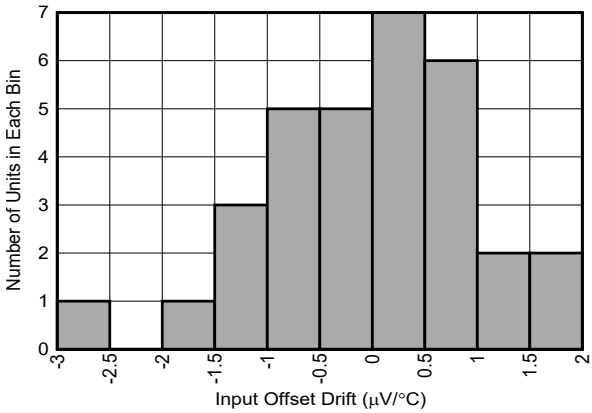
µ = 209 µV, σ = 193 µV

Figure 7-21. Input Offset Voltage Distribution



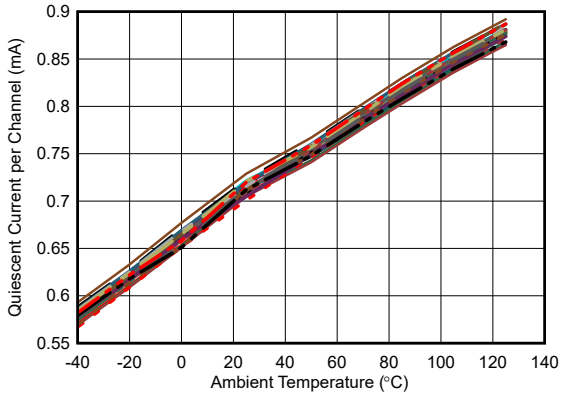
35 units, µ = -0.26 µV/°C, σ = 0.49 µV/°C, DGK package

Figure 7-22. Input Offset Voltage Drift Distribution



32 units, µ = -0.02 µV/°C, σ = 0.98 µV/°C, DBV package

Figure 7-23. Input Offset Voltage Drift Distribution

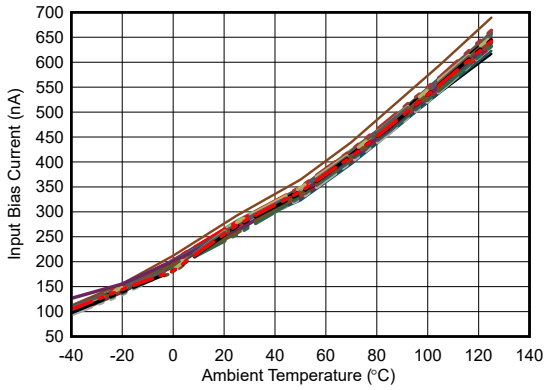


35 units

Figure 7-24. Quiescent Current vs Ambient Temperature

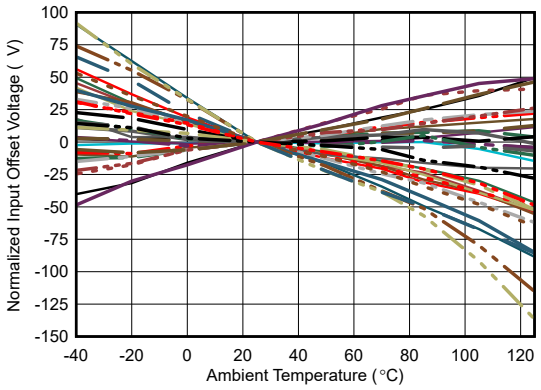
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



35 units

Figure 7-25. Input Bias Current vs Ambient Temperature



Normalized to 25 °C values, 35 units, DGK package

Figure 7-26. Input Offset Voltage vs Ambient Temperature

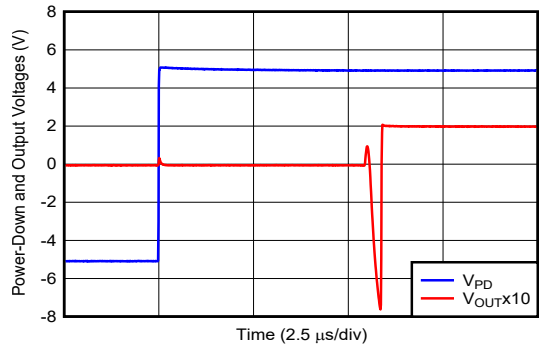


Figure 7-27. Turn-On Time to DC Input

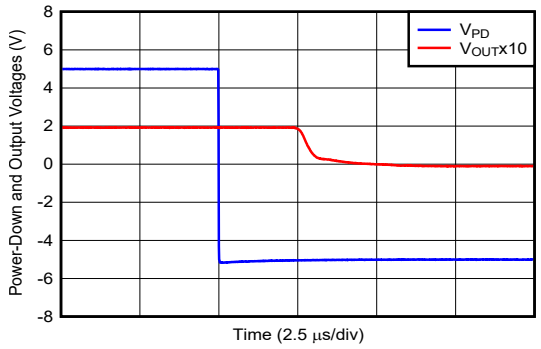
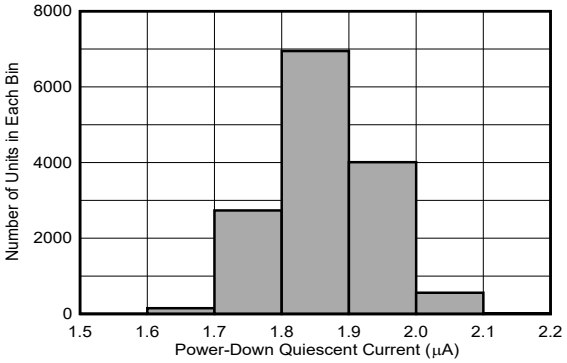


Figure 7-28. Turn-Off Time to DC Input



μ = 1.86 µA, σ = 0.076 µA

Figure 7-29. Power-Down Quiescent Current Distribution

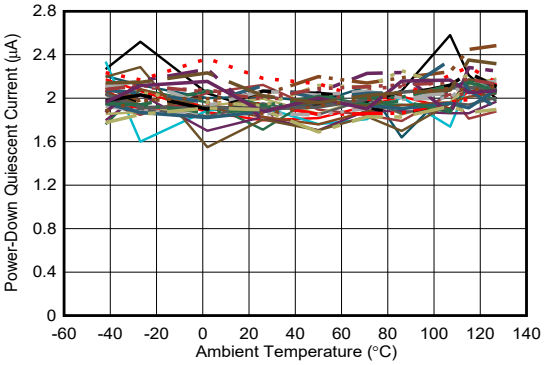
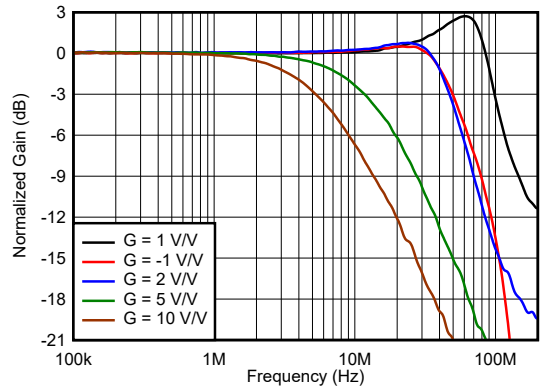


Figure 7-30. Power-Down I_Q vs Ambient Temperature

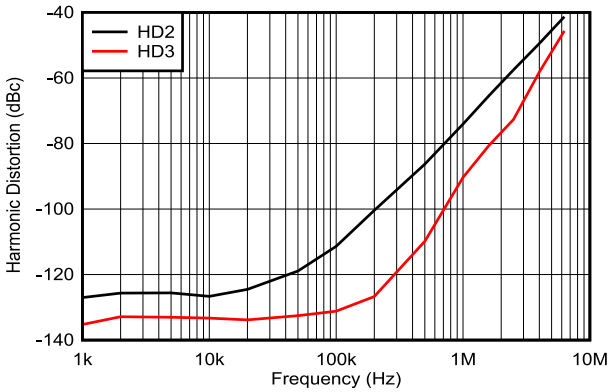
7.10 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≈ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-31. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

Figure 7-32. Harmonic Distortion vs Frequency

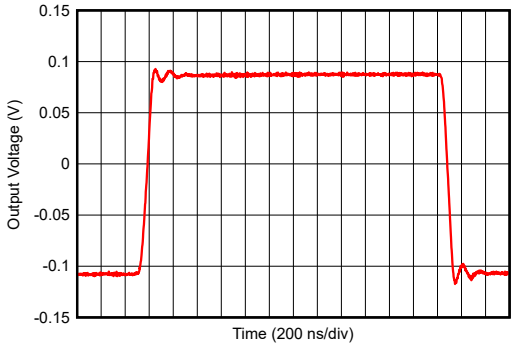


Figure 7-33. Small-Signal Transient Response

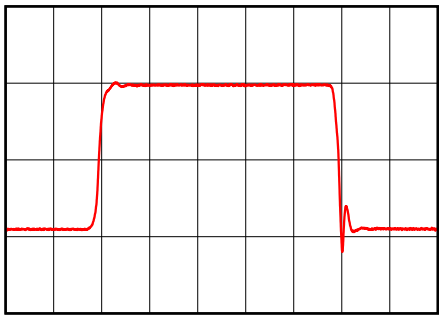
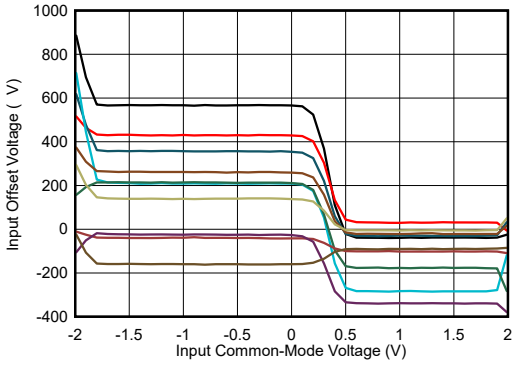


Figure 7-34. Large-Signal Transient Response



Measured for 10 units

Figure 7-35. Input Offset Voltage vs Input Common-Mode Voltage

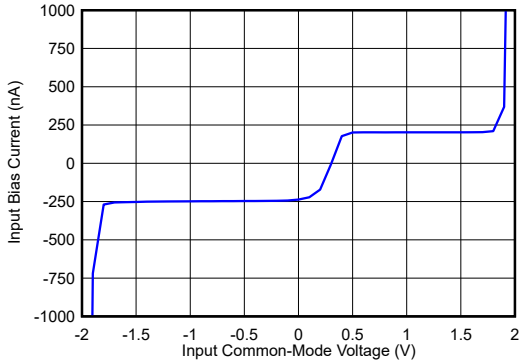


Figure 7-36. Input Bias Current vs Input Common-Mode Voltage

7.10 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≈ 25°C (unless otherwise noted)

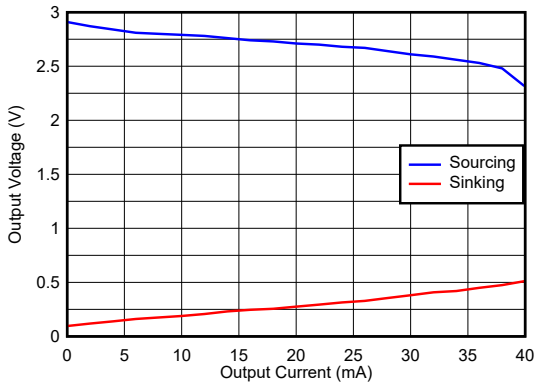
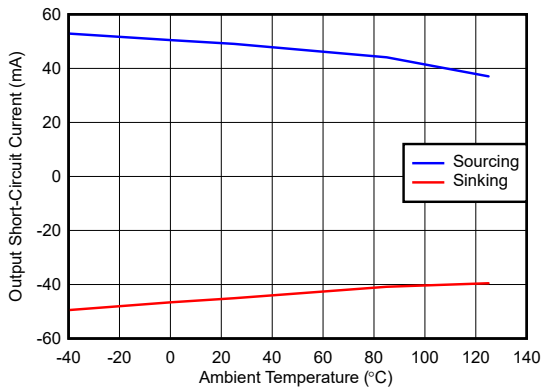


Figure 7-37. Output Voltage vs Load Current



Output saturated and then short-circuited to other supply

Figure 7-38. Output Short-Circuit Current vs Ambient Temperature

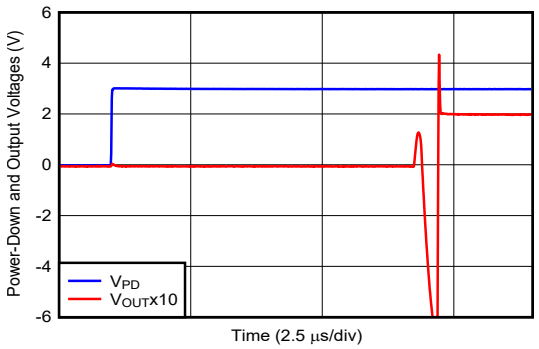


Figure 7-39. Turn-On Time to DC Input

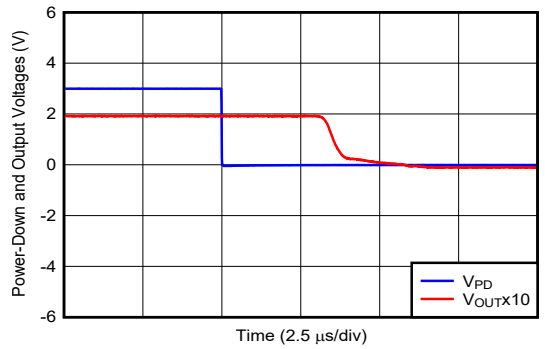
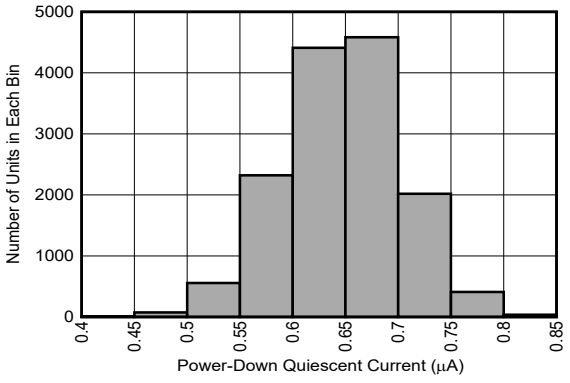


Figure 7-40. Turn-Off Time to DC Input



µ = 0.64 µA, σ = 0.056 µA

Figure 7-41. Power-Down Quiescent Current Distribution

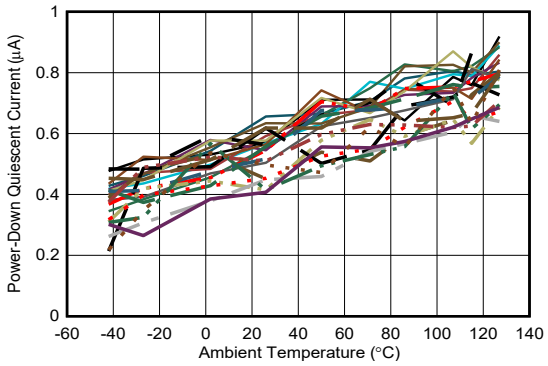
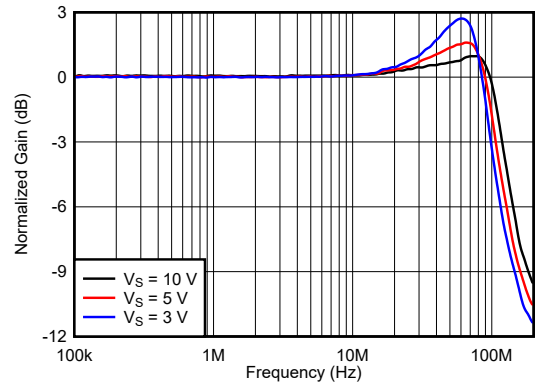


Figure 7-42. Power-Down I_Q vs. Ambient Temperature

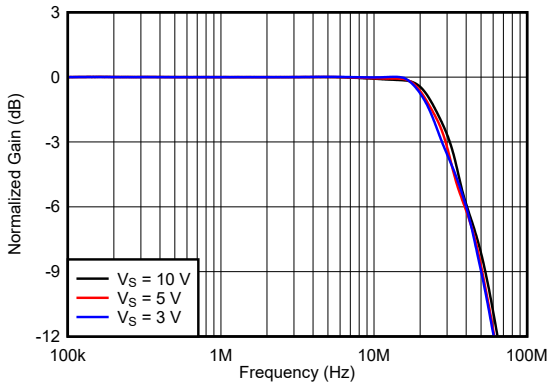
7.11 Typical Characteristics: V_S = 3 V to 10 V

At V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-43. Frequency Response vs Supply Voltage



V_{OUT} = 1 V_{PP}

Figure 7-44. Frequency Response vs Supply Voltage

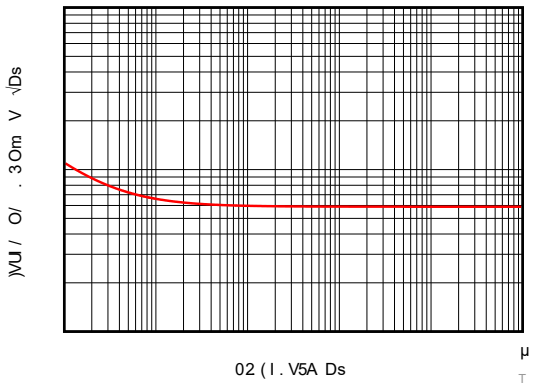


Figure 7-45. Input Voltage Noise Density vs Frequency

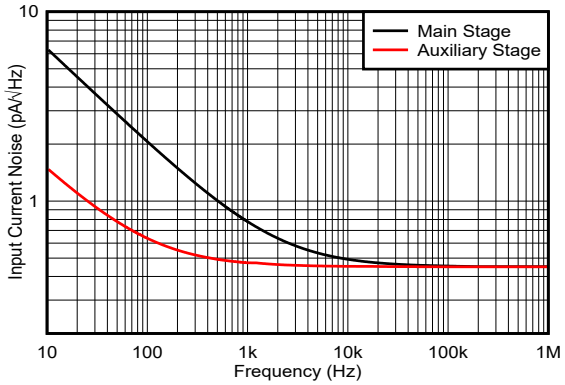


Figure 7-46. Input Current Noise Density vs Frequency

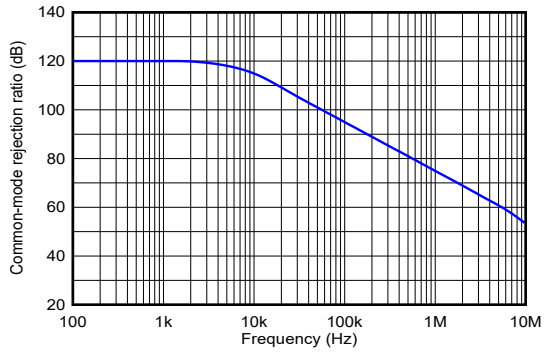


Figure 7-47. Common-Mode Rejection Ratio vs Frequency

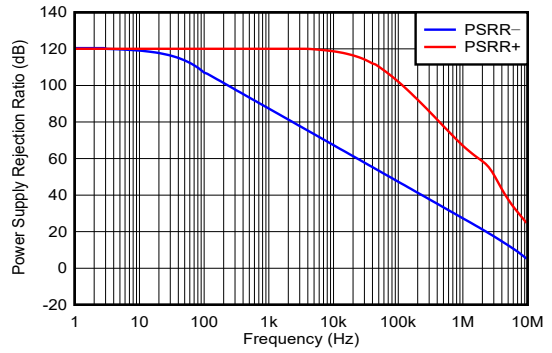


Figure 7-48. Power Supply Rejection Ratio vs Frequency

7.11 Typical Characteristics: V_S = 3 V to 10 V (continued)

At V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

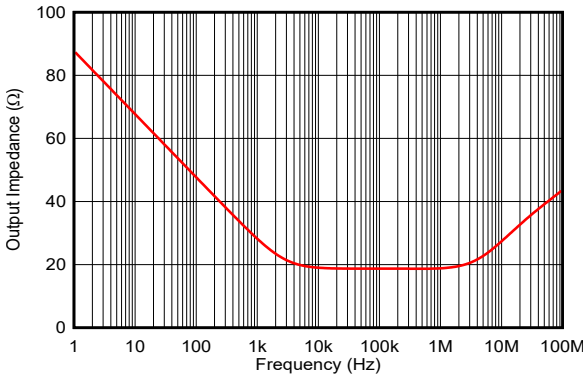
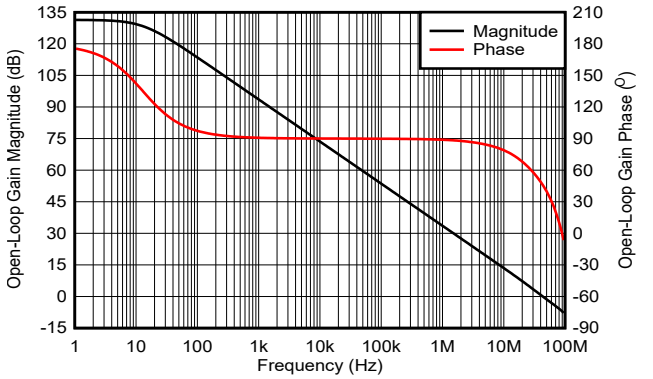
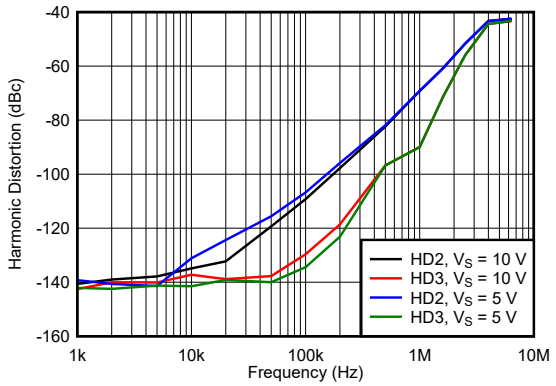


Figure 7-49. Open-Loop Output Impedance vs Frequency



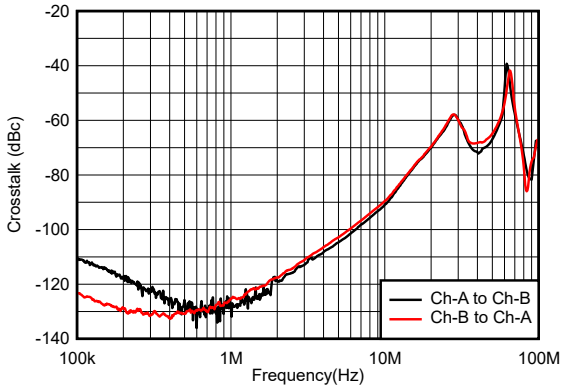
Small-signal response

Figure 7-50. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-51. Harmonic Distortion vs Supply Voltage



DGK package

Figure 7-52. Crosstalk vs Frequency

8 Detailed Description

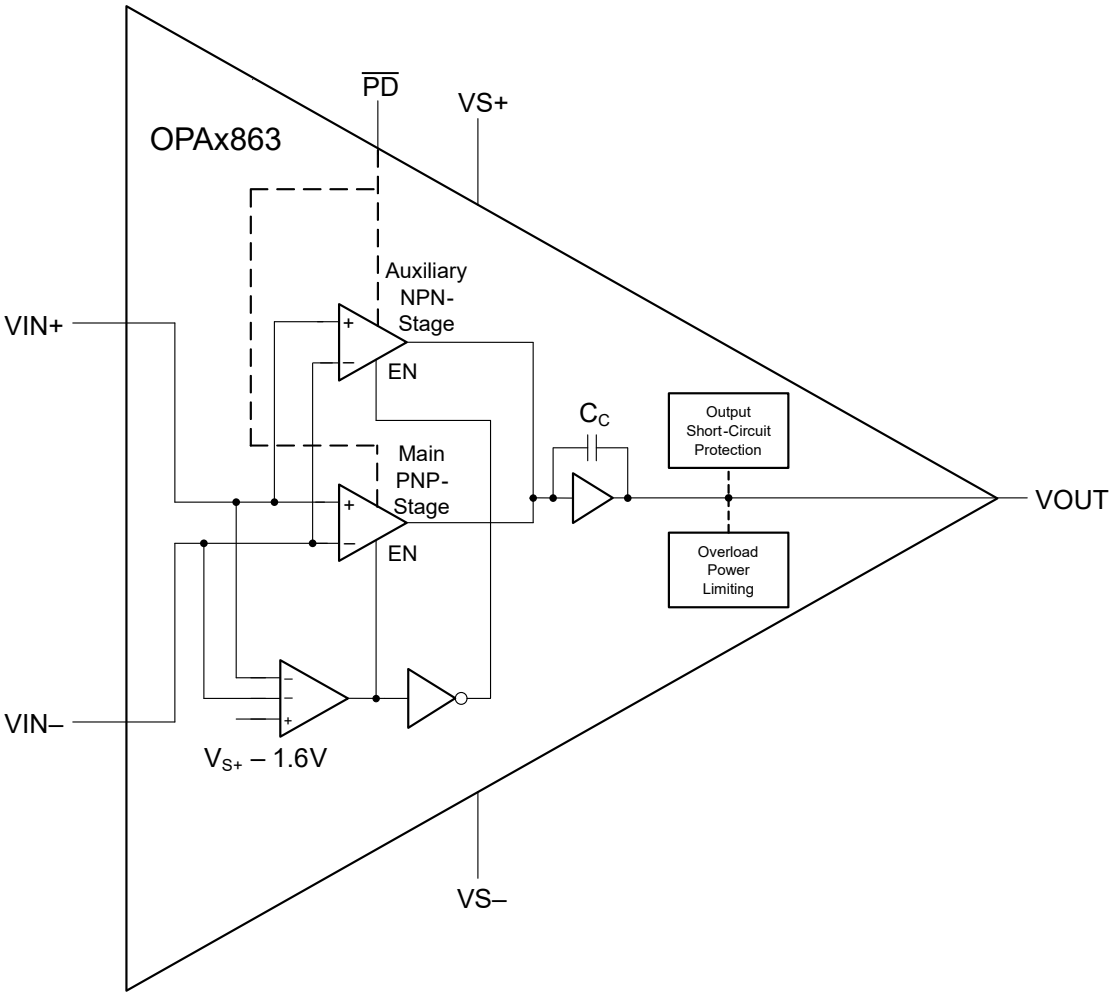
8.1 Overview

The OPAx863 devices are low-power, 50 MHz, rail-to-rail input and output (RRIO) bipolar voltage-feedback operational amplifiers with a voltage noise density of 5.9 nV/√Hz and 1/f noise corner at 25 Hz. The OPAx863 devices work in a wide-supply voltage range from 2.7 V to 12.6 V and consumes only 700 µA quiescent current. The OPAx863 devices operate with 2.7 V supply, are RRIO capable, consume low-power, and offer a power-down mode, which makes them ideal amplifiers for 3.3-V or lower voltage applications that need superior AC performance. The amplifier's main and auxiliary input stages are matched for gain bandwidth product (GBW), noise and offset voltage suitable for applications which require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. See Section 8.3.2.1 for more details of this overload power limit feature. The amplifier's output is protected against short-circuit fault conditions.

The OPAx863 devices feature a power-down (PD) mode with a PD quiescent current of 1.5 µA (maximum) with a 3 V supply, with turn-on and turn-off time within less than 6.5 µs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The OPAx863 devices include a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from $V_{S–}$ – 0.2 V till V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 5.9 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The NPN input stage does not use the slew boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages will cause a crossover distortion which needs to be considered in high-frequency applications requiring superior linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

Since the OPAx863 devices are bipolar amplifiers, the two inputs are protected with anti-parallel back-to-back diodes between them, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the anti-parallel diodes begin to conduct in very fast input or output transient conditions. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPAx863 devices feature a rail-to-rail output stage with possible signal swing from $V_{S–}$+ 0.2 V to V_{S+}– 0.2 V. Violating the output headroom to either of the supplies will cause output signal clipping and introduce distortion.

The OPAx863 devices integrate an output short-circuit protection circuit, which makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPAx863 devices include overload power limiting which limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier's output saturates, its two inputs are pulled apart which may enable the slew boost circuit. The input differential voltage is an error voltage in negative feedback, which the amplifier core nullifies by engaging the slew boost circuit and driving the output stage deeper into saturation. Once the input to an amplifier attains a value large enough to saturate its output, any further increase in this input excitation results in a finite input differential voltage. As the output stage transistor is pushed deeper into saturation, its h_{FE} (base-to-collector current gain) drops with increase in its base and collector current, increasing the device quiescent current. This may cause a catastrophic failure in multi-channel, high-gain, high-density front-end designs and reduce operating lifetime in portable battery powered systems. The OPAx863 devices overload power limiting includes an intelligent output saturation detection circuit which limits the device's quiescent current to 2.2-mA per channel under DC overload conditions. This increase in quiescent current is smaller with AC input or output and output saturation duration for only a fraction of the overall signal time period. Table 8-1 compares the increase in quiescent current with 50 mV input overdrive for OPAx863 devices and other voltage feedback amplifiers without overload power limit.

Table 8-1. Quiescent Current with Saturated Outputs

Device	Input Differential Voltage	Quiescent Current	Increase in I_Q from steady-state condition
OPAx863 with overload power limit	50 mV	1.1 mA	1.57x
Competitor amplifier without overload power limit	50 mV	1.96 mA	3.43x

8.3.3 ESD Protection

As Figure 8-1 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which ensures the current through the ESD diodes remains within their rated value. Since OPAx863 is a bipolar amplifier, the two inputs are protected with anti-parallel back-to-back diodes between them which limits the maximum input differential voltage to approximately 1 V. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

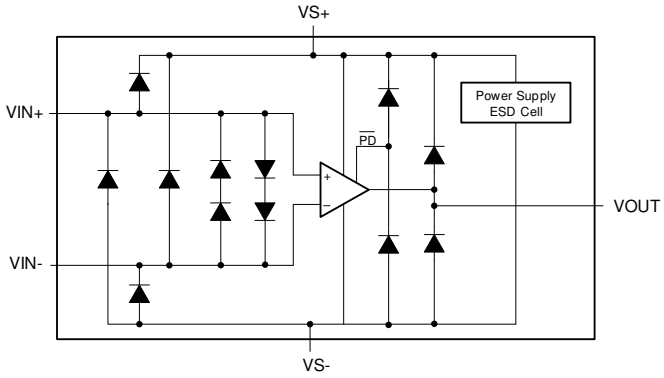


Figure 8-1. Internal ESD Protection

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The OPAx863 includes a power-down mode for low-power standby operation with a quiescent current of only 1.5 µA (maximum) with a 3-V supply and high output impedance. Many low-power systems are active for only a small time interval when the parameters of interest are measured and remain in low-power standby mode for a majority of the time for an overall small average power consumption. The OPAx863 enables such a low-power operation with quick turn-on within less than 6.5 µsec. Refer to the electrical characteristics tables for power-down pin control thresholds.

The $\overline{PD}$ pin always needs to be driven to avoid false triggering and oscillations. If use of power-down mode is not necessary, the $\overline{PD}$ pin should be connected to V_{S+}. For applications which need the power-down mode, an external pull-up resistor from $\overline{PD}$ pin to V_{S+}, driven with an open-collector power-down control logic may be used.

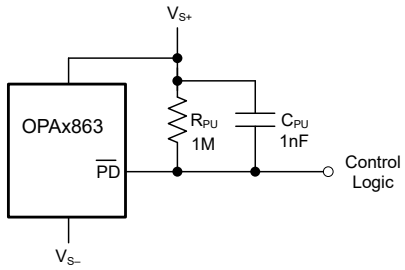


Figure 8-2. Power Down Control

The choice of value of the pull-up resistor R_{PU} in Figure 8-2 impacts the current consumption in power-down mode. Using a large R_{PU} reduces the power consumption, but increases the noise at the $\overline{PD}$ pin which could cause the amplifier to power-down. A 1 nF capacitor may be used in parallel with R_{PU} to avoid couping of external noise and false triggering. For the case of $\overline{PD}$ pin driven to V_{S-}, the current I_{PU} through R_{PU} is given as,

$$I_{PU} = \frac{V_{S+} - V_{S-}}{R_{PU}}$$

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Low-Side Current Sensing

Power converters use current-mode feedback control for superior transient response and multi-phase load sharing. Inverter stages control the phase currents for torque control in motor drives. Due to its simplicity and low-cost, many of these topologies use difference amplifier based low-side current sensing. Figure 9-1 shows the use of OPAx863 in a difference amplifier circuit for low-side current sensing.

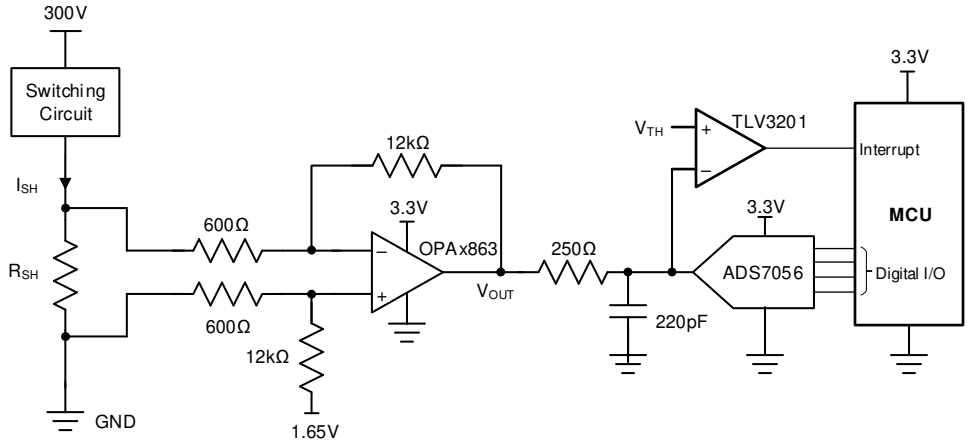


Figure 9-1. Low-Side Current Sensing in Power Converters

9.2.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

In a difference amplifier circuit, the output voltage is given by,

$$V_O = \frac{R_F}{R_G} V_{IN} - V_{REF}$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10 V here) seen by the circuit, and is given by,

$$R_S = \frac{V_{IN(maximum)} - V_D}{I_{D(maximum)}}$$

Where,

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit
- V_D is the forward voltage drop of ESD diodes at the amplifier input
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input

For a difference amplifier gain of 20 V/V, R_F and R_G of 12k Ω and 600 Ω are used, respectively. With a clock frequency of 40 MHz and ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. Figure 9-2 shows the simulation results for the circuit in Figure 9-1. The worst-case peak-to-peak input transient condition is simulated. The OPAx863 devices output settles to within 0.1% accuracy within 543 ns. If use of a slower clock frequency with the ADC is desired, the acquisition time reduces with the same sampling rate, which degrades measurement accuracy. Alternatively, the sampling rate may be reduced to recover the required acquisition time and 0.1% accuracy.

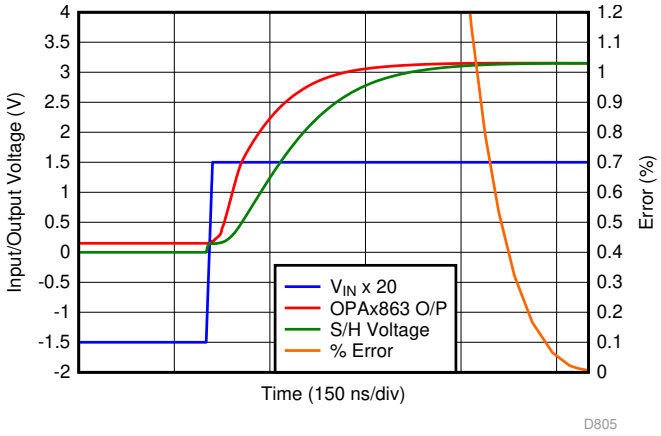


Figure 9-2. 0.1% Settling Performance

9.3 Front-End Gain and Filtering

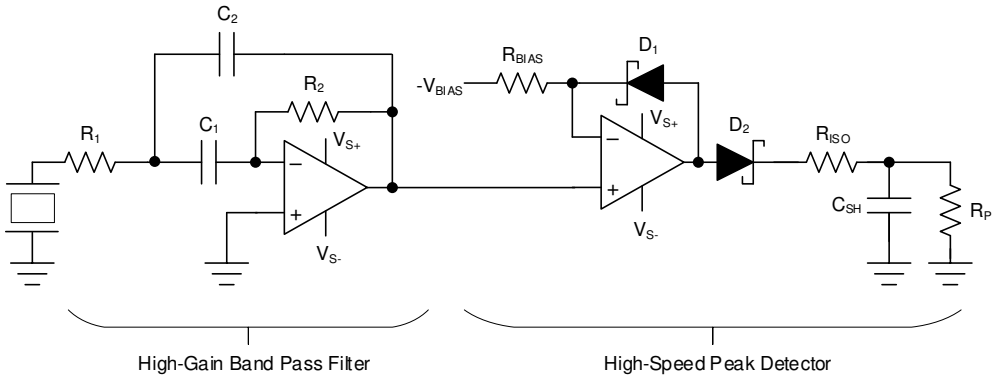


Figure 9-3. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. Figure 9-3 shows a high-gain narrow bandpass filter and peak detector circuit using any of the OPAx863 devices. The signal at the frequency of interest is filtered out, gained, and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPAx863 devices are used with its 50-MHz GBW to add a single-stage gain, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

9.4 Low-Power SAR ADC Driver and Reference Buffer

Figure 9-4 shows the use of the OPAx863 devices as a SAR ADC input driver and reference buffer driving the ADS7945. Sensors, which are used for interface with the physical environment, exhibit high output impedance and cannot drive SAR ADC inputs directly. A wide-GBW amplifier like the OPAx863 devices are needed to charge the switching capacitors at the SAR ADC input and to settle fast to the required accuracy within the given acquisition time. The ADC core draws transient current from the reference input during the conversion (digitization) phase, which needs to be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for superior digitization performance. The OPAx863 devices reference buffer is used in a composite loop with the OPA378 precision amplifier due to limitations in precision performance of wide-GBW amplifiers. The precision amplifier maintains low-offset output, whereas the OPAx863 devices provide the output drive and fast-settling performance.

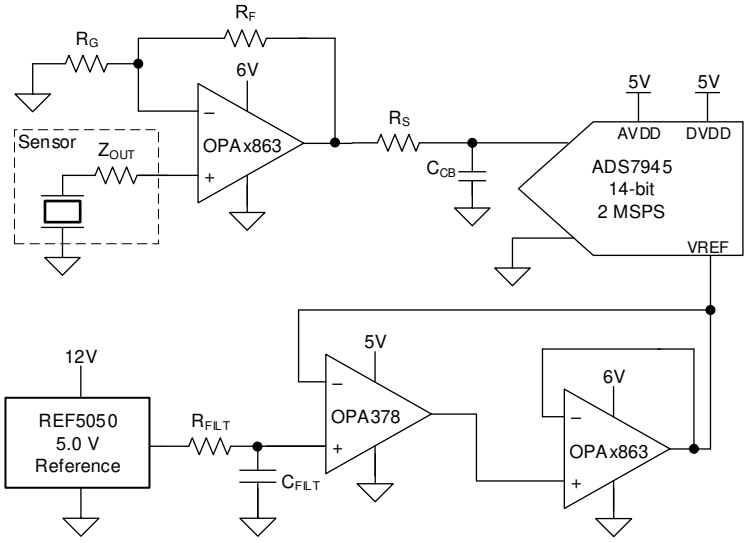


Figure 9-4. OPAx863 as Low-Power SAR ADC Driver

9.5 Variable Reference Generator Using MDAC

High-speed amplifiers may be used as a voltage buffer at MDAC output to generate a fast settling variable reference voltage. Figure 9-5 shows a representative circuit using DAC8801 and OPAx863.

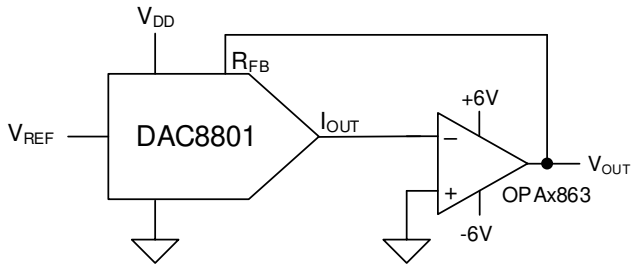


Figure 9-5. Variable Reference Generator Using MDAC and OPAx863

9.6 Clamp-On Ultrasonic Flow Meter

Figure 9-6 shows how ultrasonic flow meters measure the rate of flow of a liquid using transit-time difference (t_{12}–t_{21}), which depends on the flow rate. Figure 9-6 shows a representative schematic for a non-intrusive ultrasonic flow meter using the OPAx863 devices and 12-V transducer excitation. The OPAx863 devices are used for the forward path as a unity-gain buffer for 12-V pulsed transducer excitation at Node 1. At the same time, the receiver circuit at Node 2, also using the OPAx863 devices, first provides an AC-gain followed by a DC-level shift to lead to the PGA, ADC and processing within the MSP430 microcontroller.

Node 2 and Node 1 use similar transmit and receive circuits (discussed above) for the reverse path. The OPAx863 devices wide GBW of 50 MHz introduces minimal phase-delay and low-noise for superior flow rate measurement. The amplifier stays in power-down mode for a majority of the time in battery powered systems, resulting in very small average system-level power consumption and prolonged battery lifetime with its 1.5 µA (maximum) power-down mode quiescent current with a 3-V supply. Since the transmit and receive signal chains are connected to the same point at the respective node transducers, the OPAx863's 12.6-V supply voltage capability enables 12-V transducer excitation without any damage to the front-end or need for external switches which makes a compact solution. This makes the OPAx863 devices suitable for flow measurements in large diameter pipes and non-intrusive flow meters. The TIDM-02003 reference design discusses an ultrasonic gas flow sensing subsystem which uses high-speed amplifiers for front-end amplification.

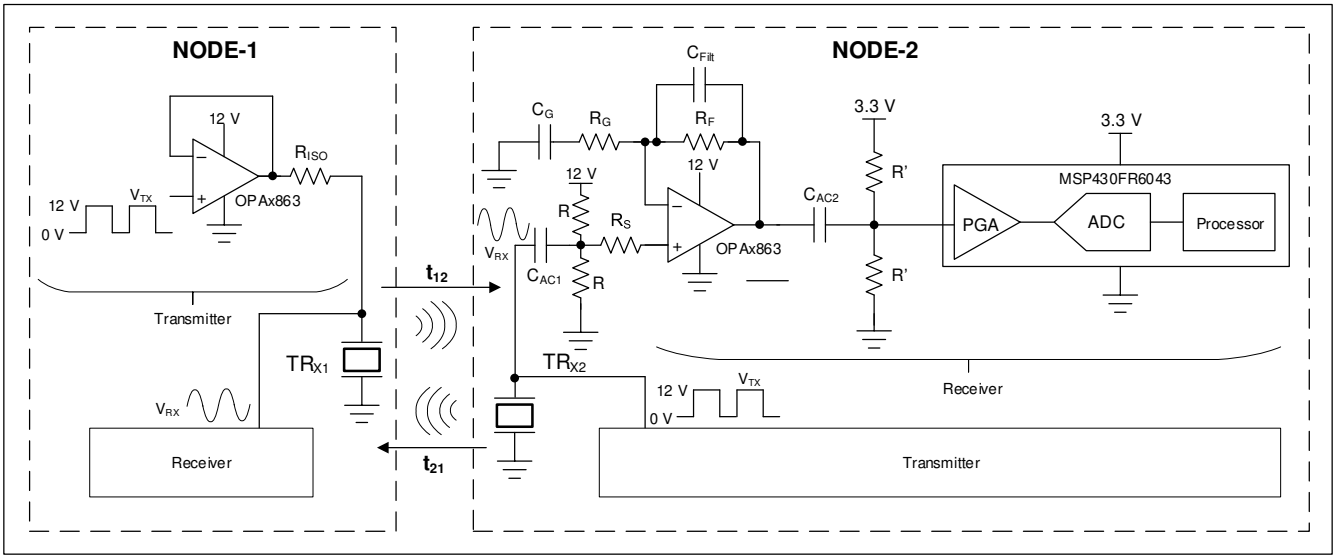


Figure 9-6. Non-Intrusive Ultrasonic Flow Meter

10 Power Supply Recommendations

The OPAx863 devices are intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPAx863 devices may operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. The DC errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPAx863 devices) require careful attention to board layout parasitics and external component types. The *OPA2863 DGK Evaluation Module* user's guide can be used as a reference when designing the circuit board. Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high frequency performance of the OPAx863 devices.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Keep resistor values as low as possible and consistent with load driving considerations. Lowering the resistor values keep the resistor noise terms low, and minimize the effect of its parasitic capacitance; lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network.

11.1.1 Thermal Considerations

The OPAx863 does not require heat sinking or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by,

$T_J = T_A + P_D \times R_{\Theta JA}$

where,

- T_A is the ambient temperature
- P_D is the total power dissipation internal to the amplifier
- $R_{\Theta JA}$ is the juntion-to-ambient thermal resistance

The total power dissipation $P_D = P_{DQ} + P_{DL}$

where, $P_{DQ} = (V_{S+} - V_{S-}) \times I_Q$, is the power dissipation due to amplifier's quiescent current

and $P_{DL}(max) = V_S{}^2 / (4 \times R_L)$, is the internal power dissipation due to output load current

As a worst-case example, compute the maximum T_J using an OPA2863-DGK (VSSOP package) configured as a unity gain buffer, operating on ±6-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$P_D = 12\ V \times 2\ mA + 6^2 / (4 \times 500\ \Omega) = 42\ mW$

Maximum T_J = 25°C + (0.042 W × 180.3°C/W) = 33°C, which is well below the maximum allowed junction temperature of 150°C.

11.2 Layout Example

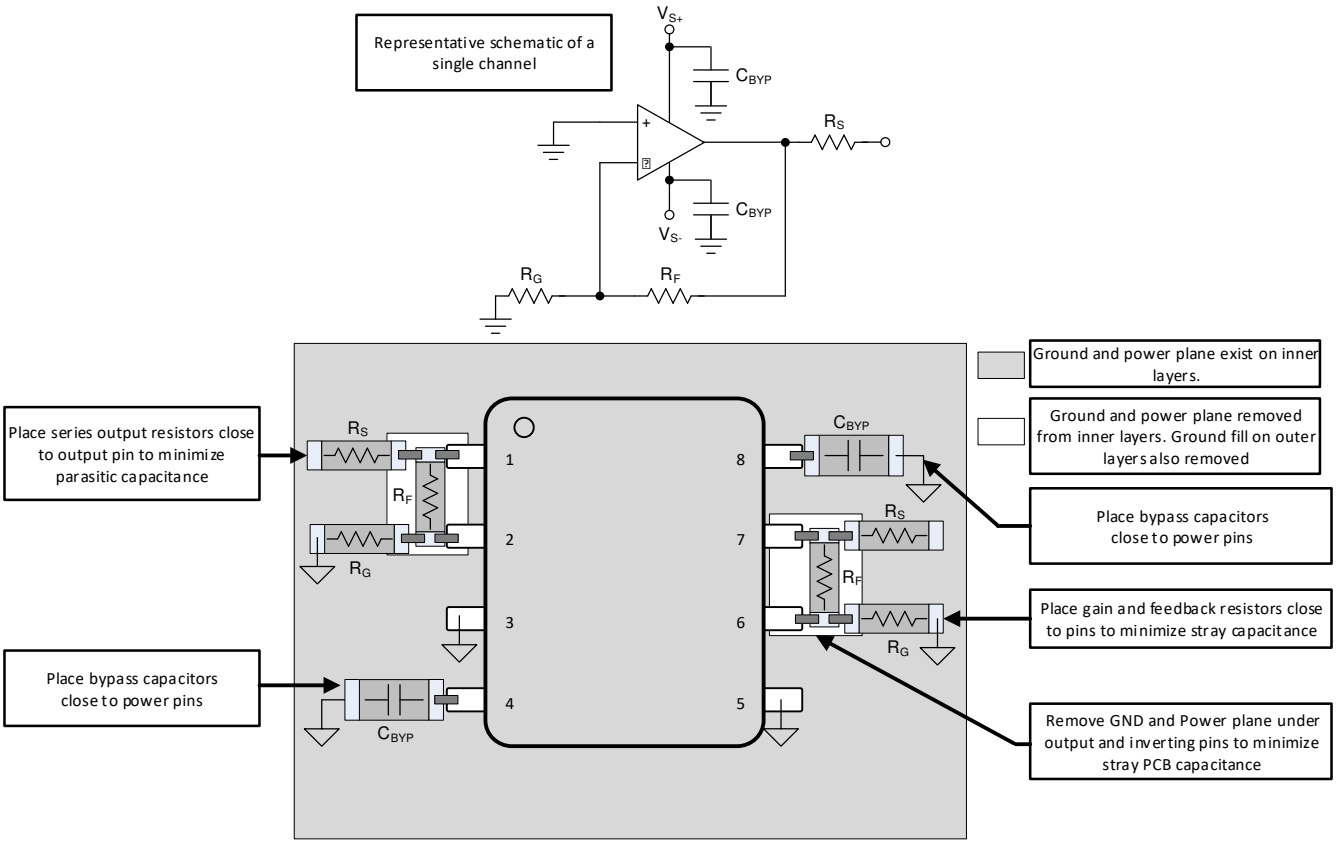


Figure 11-1. Layout Recommendation for Dual-Channel DGK Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA2863ADGK Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2863IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FJ4	Samples
OPA863SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	O863	Samples
POPA2863DR	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA2863RUNR	ACTIVE	QFN	RUN	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA4863IPWR	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA863IDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

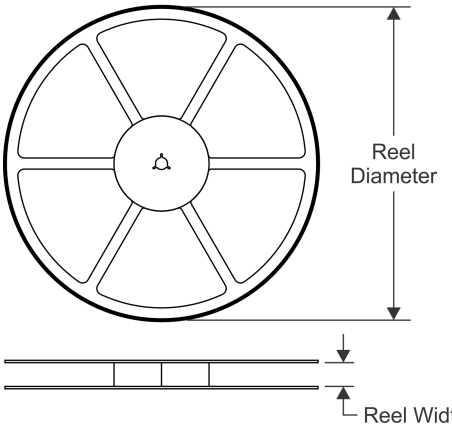
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

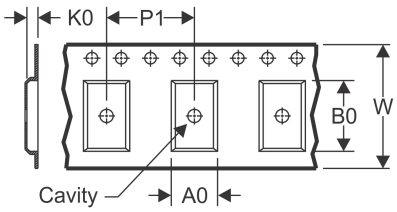
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

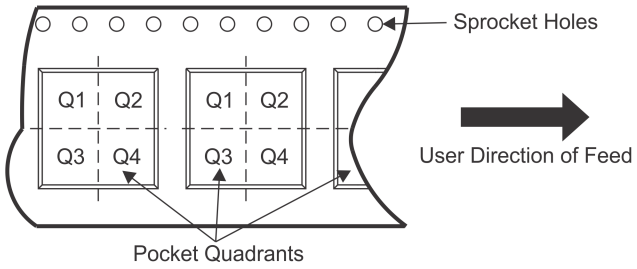


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

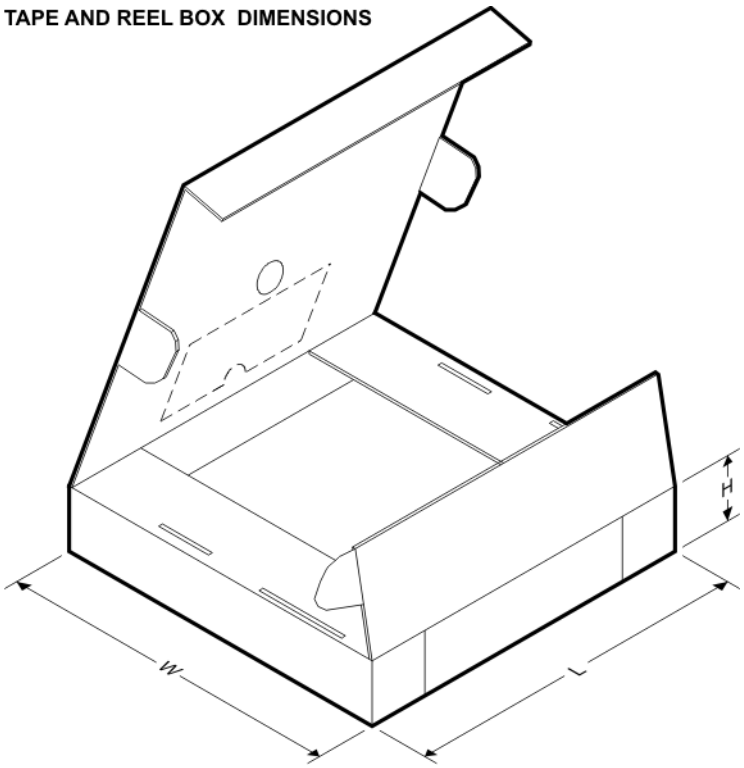
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2863IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA863SIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

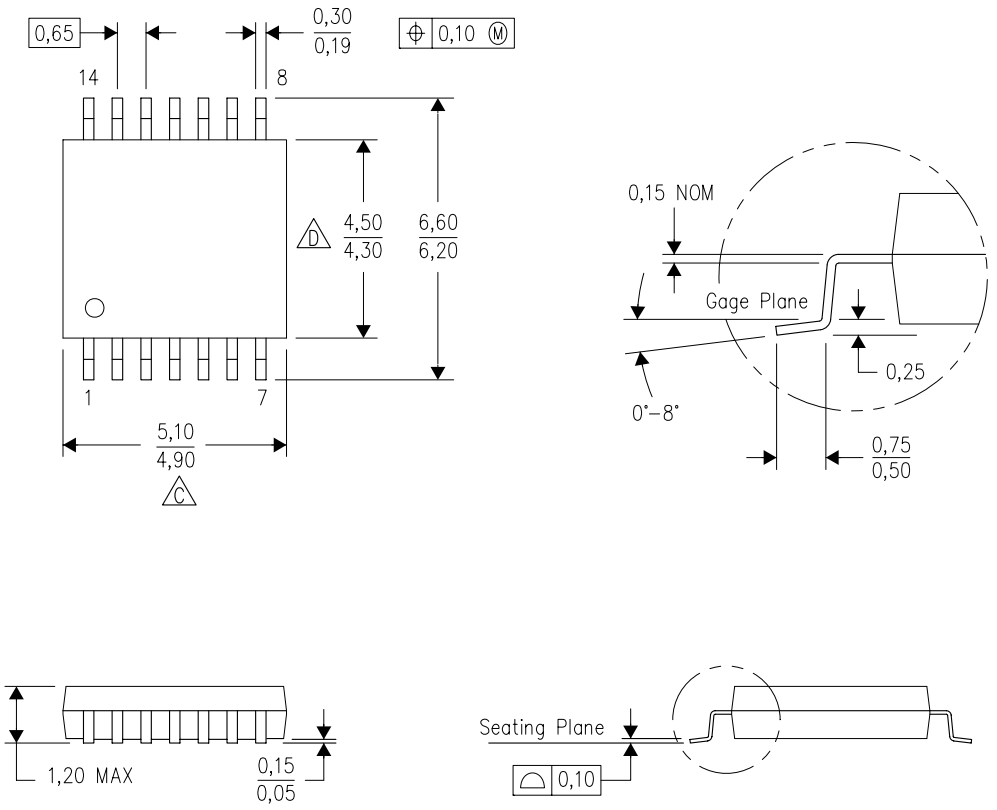
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2863IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA863SIDBVR	SOT-23	DBV	6	3000	190.0	190.0	30.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

GENERIC PACKAGE VIEW

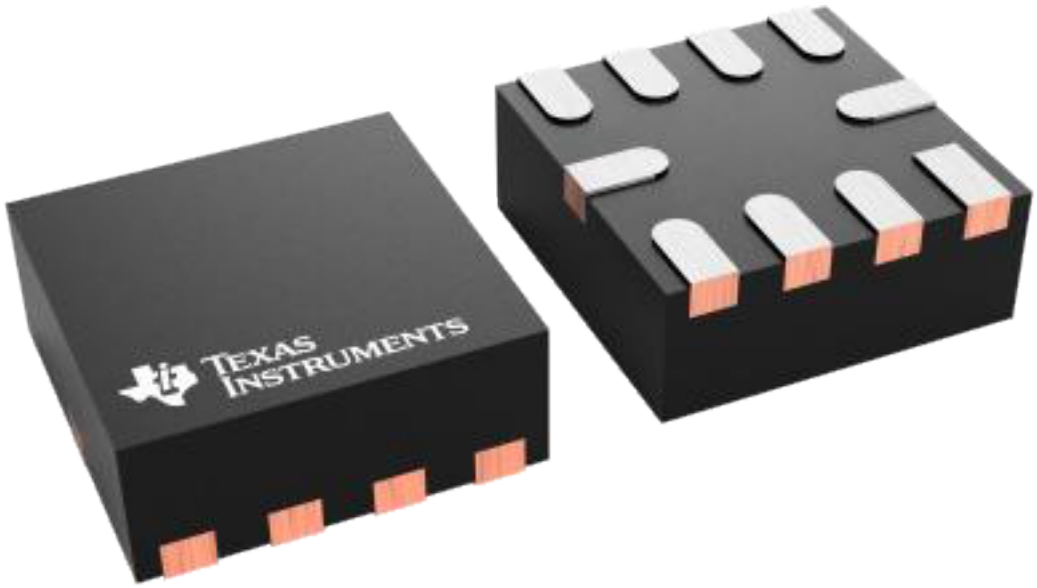
RUN 10

WQFN - 0.8 mm max height

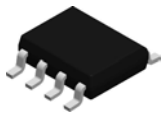
2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228249/A

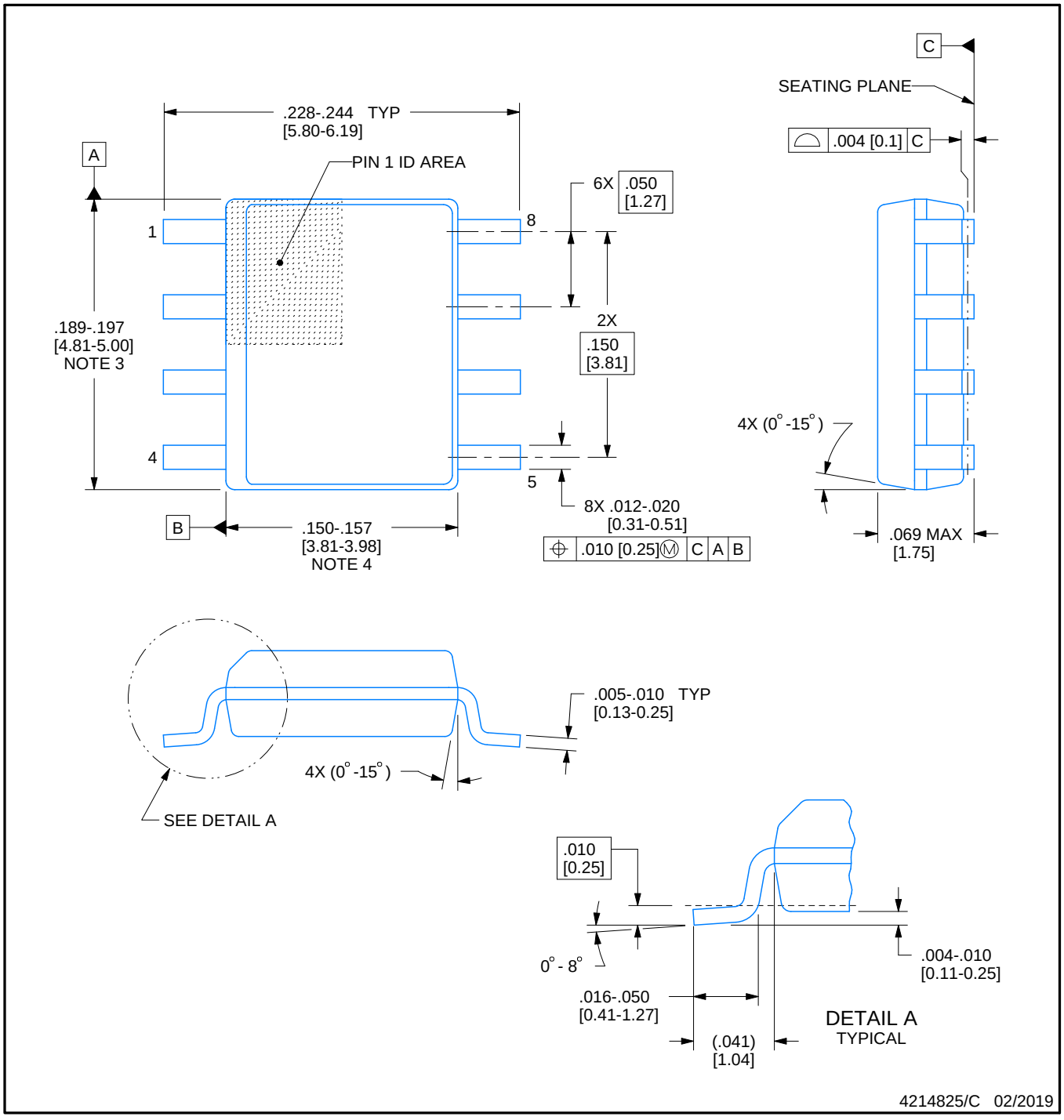


PACKAGE OUTLINE

D0008A

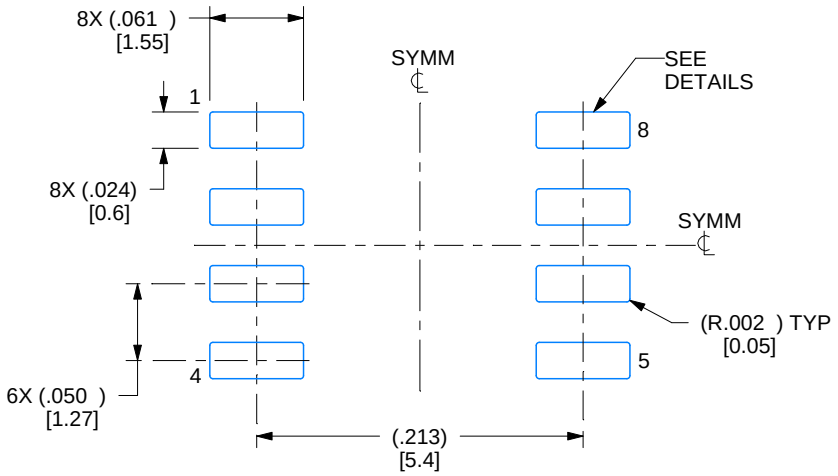
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

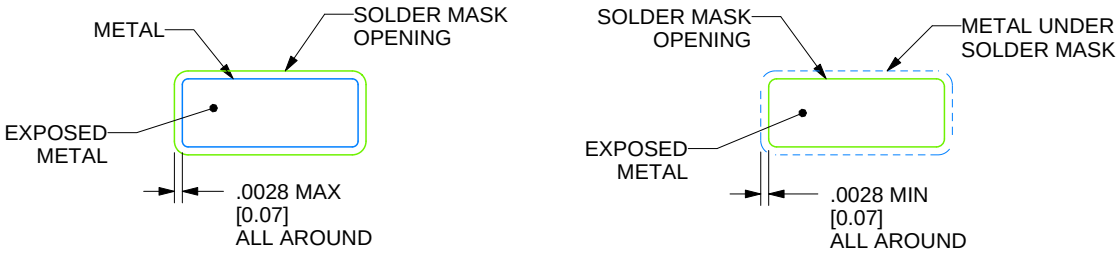


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

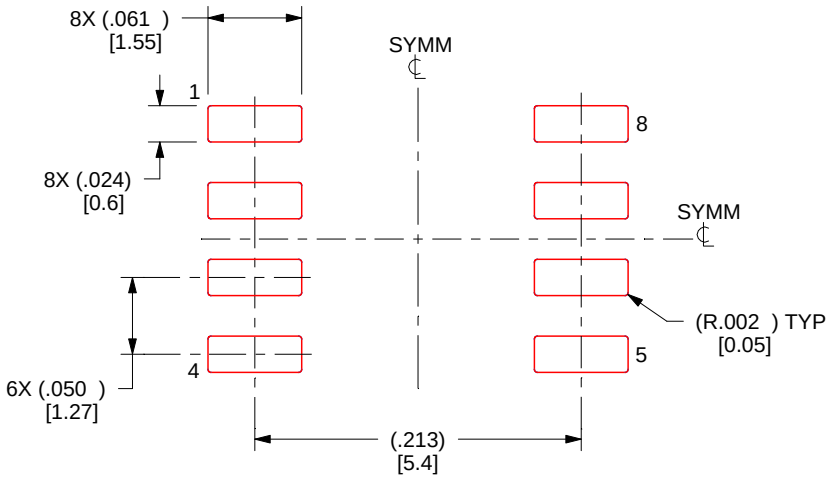
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

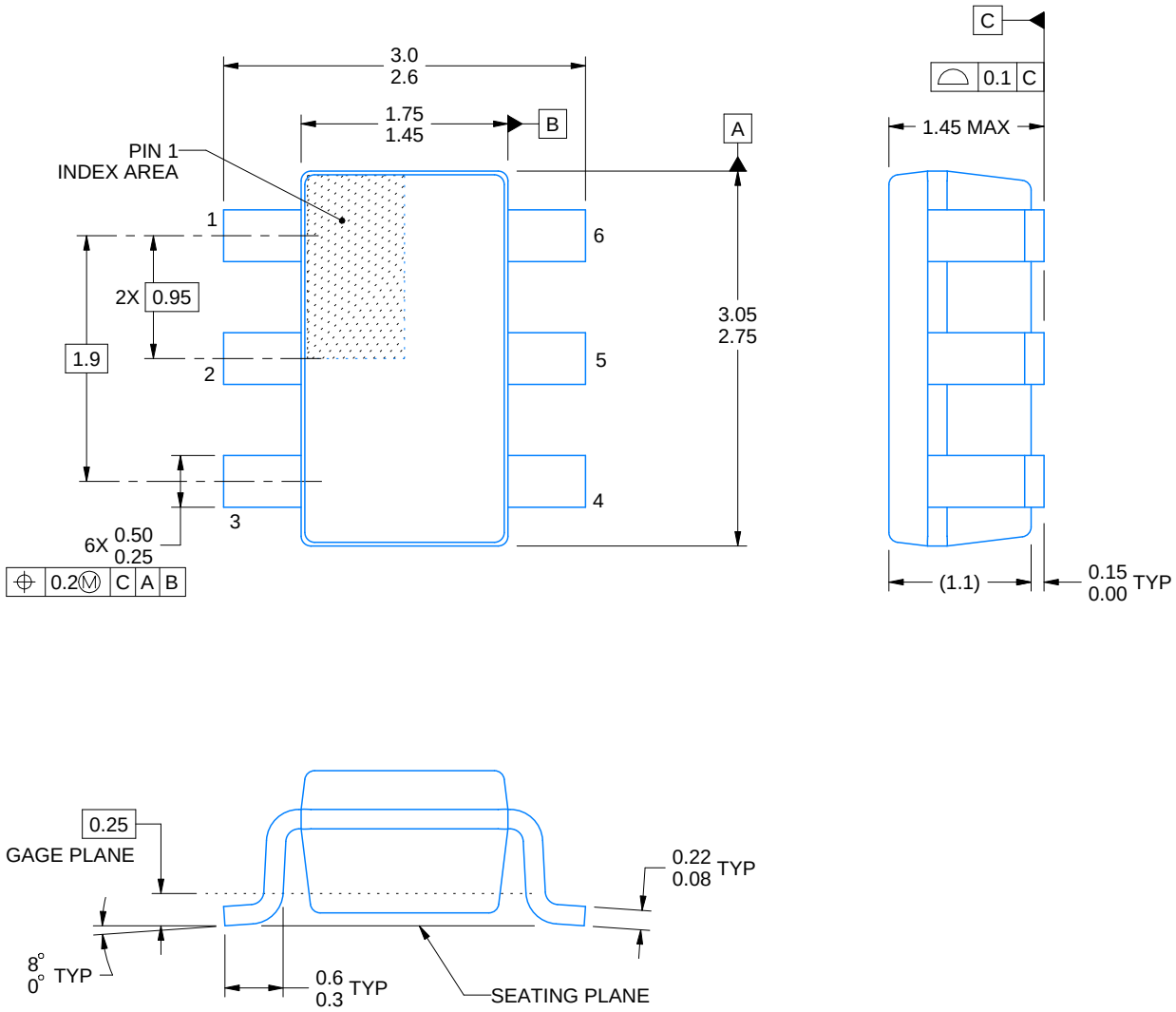
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

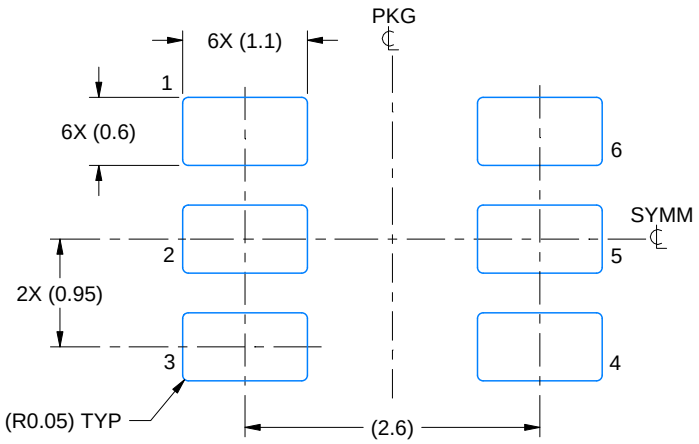
SMALL OUTLINE TRANSISTOR



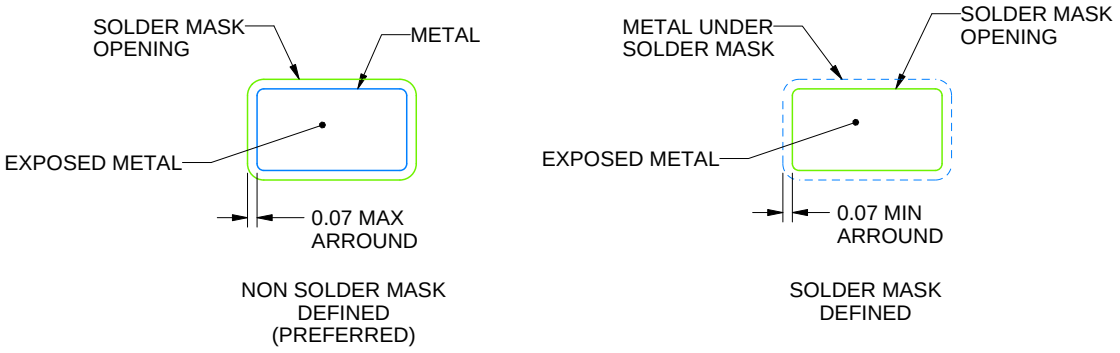
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

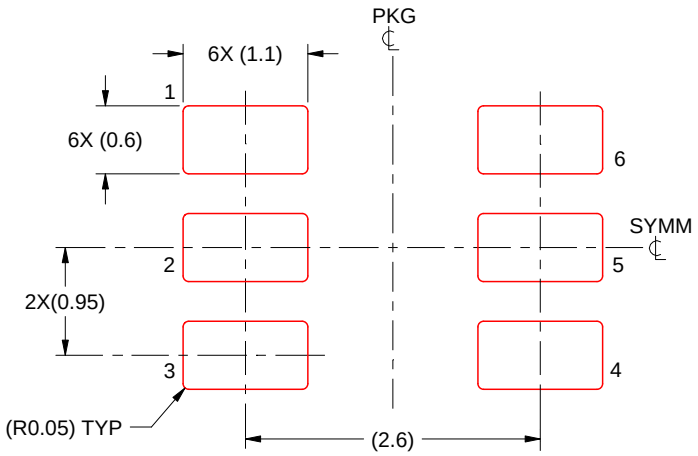


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



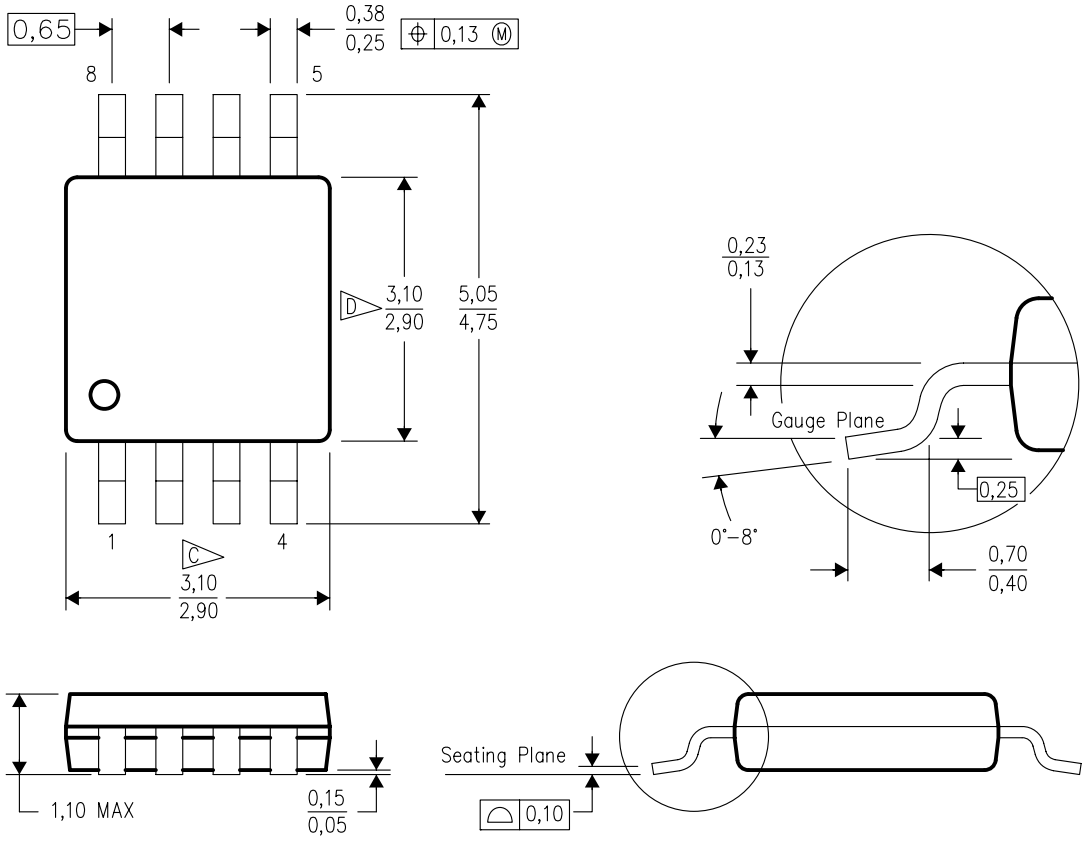
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

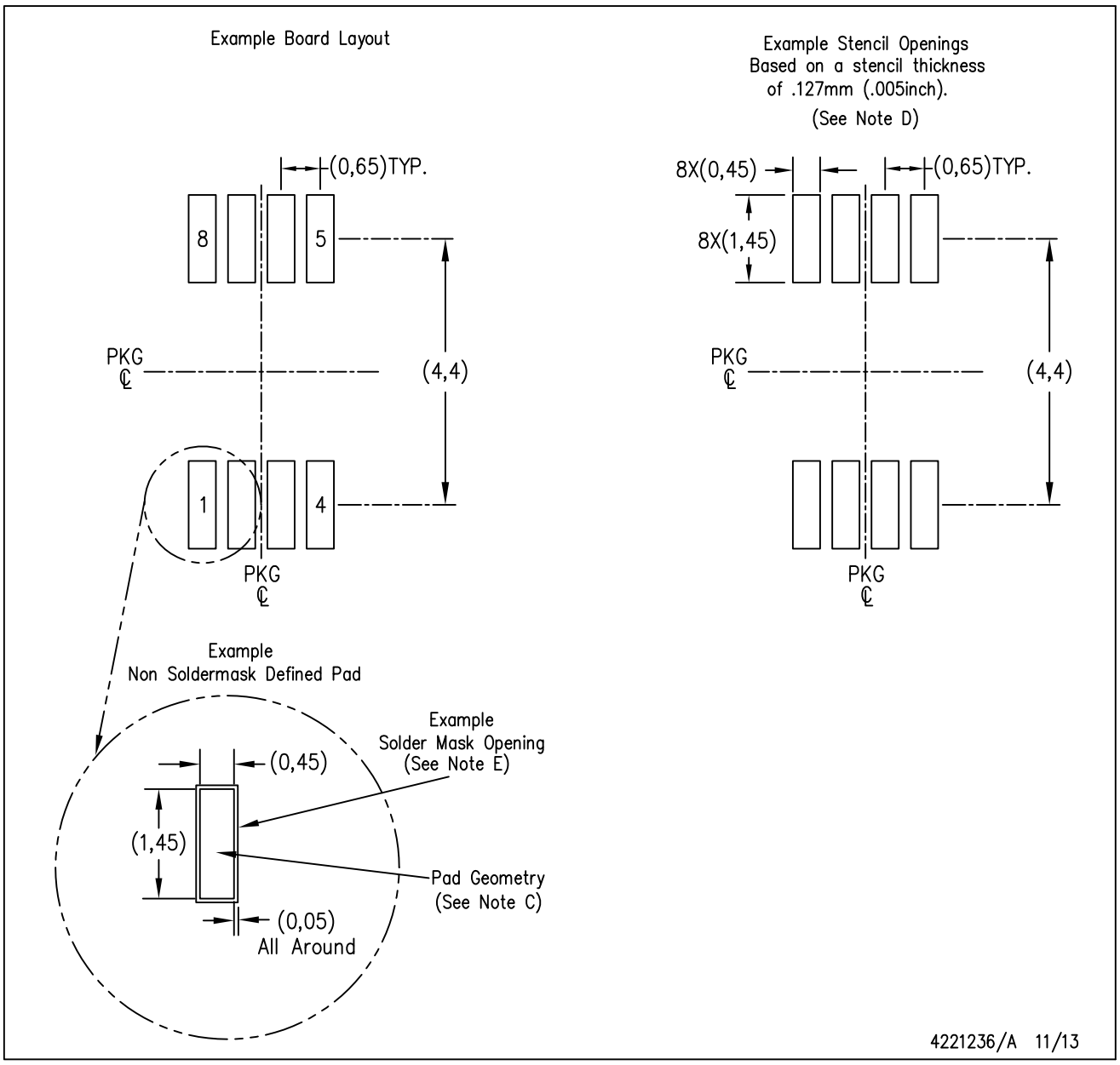
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

OPA2186 Precision, Rail-to-Rail Input and Output, 24-V, Zero-Drift Operational Amplifier

1 Features

8
O 80U01 VVC
L 81 V
L 890 A
8
G 8 750
S 80U35 VV
R 8
RFIV MI
RTT V
S 84U5 V 24 V
T 8 40 C R125 C

2 Applications

PC PSU
M DCVDC
F
P
M

3 Description

T OPA2186 T S24TVS T T
T N QU
T 8 V
N O 0U04 VVC
N QUT
S S
U

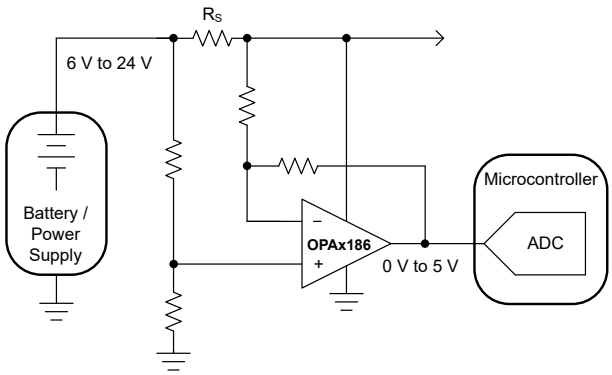
L N90 AO
OPA2186 T
S T
U

M S T
T
U T
SD S
S U

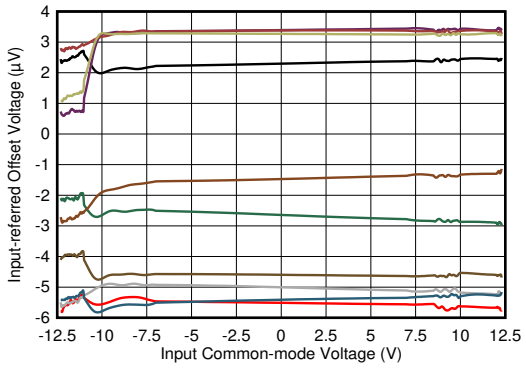
Device Information

PART NUMBER	PACKAGENO	BODY SIZE (NOM)
OPA2186	SOT23 N8O	2U90 1U60

NO F S
U



High-Side Current Shunt Monitor Application



V_{OS} vs Input Common Mode Voltage

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
J 2022	P	I R

ADVANCE INFORMATION

5 Pin Configuration and Functions

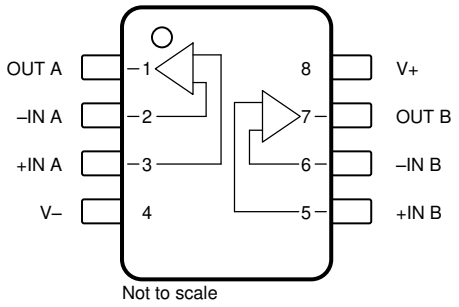


Figure 5-1. DDF (8-Pin SOT-23) Package, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN A	2	I	I A
RIN A	3	I	N A
IN B	6	I	I B
RIN B	5	I	N B
OUT A	1	O	O A
OUT B	7	O	O B
V	4	P	N
VR	8	P	P

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

T N O [1]

			MIN	MAX	UNIT
V_S	S S V_S N/RO N/O			26	V
	I	CT	N/O 0.5	N/RO 0.5	V
		D		N/RO N/O 0.2	
	O T [2]		C		
T_J	O		T40	150	C
T	S		T65	150	C

N[1] O A M R U A M R
R O CU
I R O C A M RS
S S S S U
N[2] O ST S U

6.2 ESD Ratings

			VALUE	UNIT
$V_{N SDO}$		T N BMOS ANSI/ SDA/J D C JST001 [1]	4000	V
		CT NCDMOS JANSI/ SDA/J D C JST002 [2]	1500	

N[1] J D C J P155 500T/ BM SD U
N[2] J D C J P157 250T/ CDM SD U

6.3 Recommended Operating Conditions

T N O

			MIN	NOM	MAX	UNIT
V_S	S V	S	4.5		24	V
		D	2.25		12	
T_A	S		40		125	C

6.4 Thermal Information

THERMAL METRIC [1]		OPA2186 DDF (SOT-23) 8 PINS	UNIT
R_{JA}	JTT	150.4	C/W
$R_{JCN O}$	JTT NO	85.6	C/W
R_{JB}	JTT	70.0	C/W
JT	JTT	8.1	C/W
JB	JTT	69.6	C/W
$R_{JCN O}$	JTT NO	N/A	C/W

N[1] O F S *Semiconductor and IC Package Thermal Metrics*
U

6.5 Electrical Characteristics

T_A 25 C V_S 2.25 V 12 V R_L 10 V_S V2 V_{CM} V_S V2 V_{OUT} V_S V2 N O

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	I				1	8	V
V_{OS} T	I	T_A 40 C R125 C			0.01	0.04	V/C
PSRR	PT	T_A 40 C R125 C			0.02	0.1	V/V
INPUT BIAS CURRENT							
I_B	I	V_S 12 V			5	30	A
			T_A 40 C R85 C			500	
			T_A 40 C R125 C			4.8	A
I_{OS}	I				10	70	A
		T_A 40 C R85 C				1	A
		T_A 40 C R125 C				1.2	
NOISE							
	I	0.1 10			125		V_{RMS}
N	I	1			38		V/ $\sqrt{Hz}$
N	I	1			120		A/ $\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	CT			NV O 0.2		NV R 0.2	V
CMRR	CT	NV O 0.1 V_{CM} NV R 0.1 V S T_A 40 C R125 C	V_S 2.25 V	108	126		B
			V_S 12 V	110	134		
		NV O 0.1 V_{CM} NV R 0.1 V S T_A 40 C R125 C	V_S 2.25 V	106	114		
			V_S 12 V	106	120		
FREQUENCY RESPONSE							
GBW	GT				750		
SR	S	1 V S G 1			0.35		V/
S	S	T 0.1 J S 1 V SG 1			7.5		
	O	V_{IN} V_S			10		
INPUT CAPACITANCE							
ID	D				100 5		M F
ICM	CT				50 2.5		G F
OPEN-LOOP VOLTAGE GAIN							
A_{OL}	OT	V_S 12 V R_L 10 S NV O R 0.3 V V_O NV R O 0.3 V		120	140		B
			T_A 40 C R125 C	120	134		
		V_S 12 V R_L 2 S NV O R 0.65 V V_O NV R O 0.65 V		120	140		
			T_A 40 C R125 C	120	134		
OUTPUT							
V_O	V	N			5	20	V
		R_L 10			60	100	
		R_L 2			340	500	
		R_L 10 ST $_A$ 40 C R125 C			90	115	
I_{SC}	ST				20		A
C_{LOAD}	C			S			
R_O	OT			S			
POWER SUPPLY							
I		V_S 2.25 V 12 V			90	130	A
			T_A 40 C R125 C			150	

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

T OPA2186 S

UT

0 01 VVC 40 C R125 CUI S

CMRRSPSRRS A_{OL}UA S

T UI

S0U T F US *Section 8.4.1* U

T OPA2186 T SMU T S T T UT

4 5 V 24 VS T S T

UT T T T

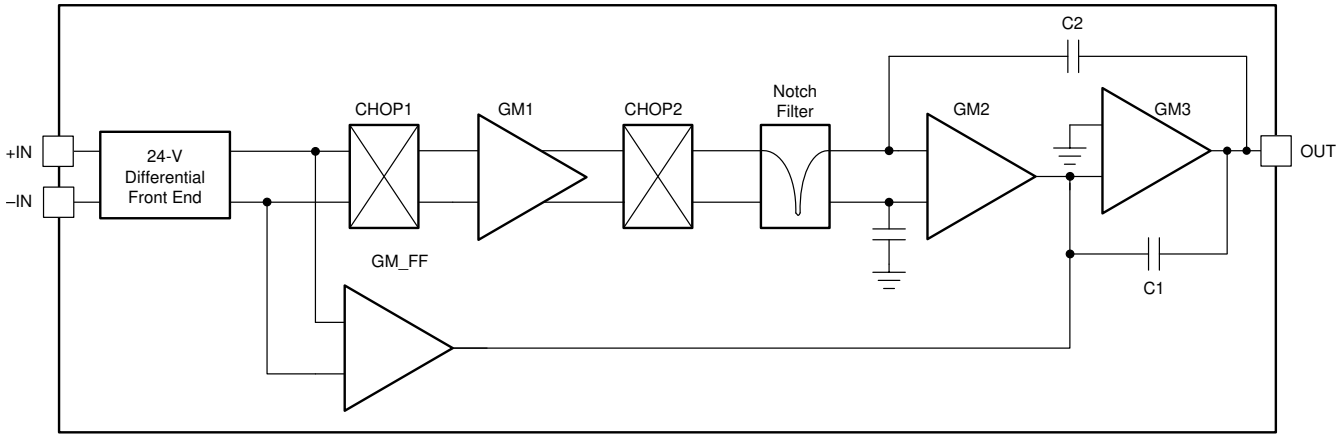
UT

S T S S

U

T OPA2186 U

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

T OPA2186
UT T T S T S
S MI S MU T I U

7.3.1 Rail-to-Rail Inputs

U S OPA2186 T T T
S 200 VUT T
U

T OPA2186 45 V 24 V N2125 V 12 VO T T UM
40 C R125 CU

7.3.2 Phase-Reversal Protection

T OPA2186 T US
T UT
T S
UT OPA2186 T UI S
U F 7T1 U

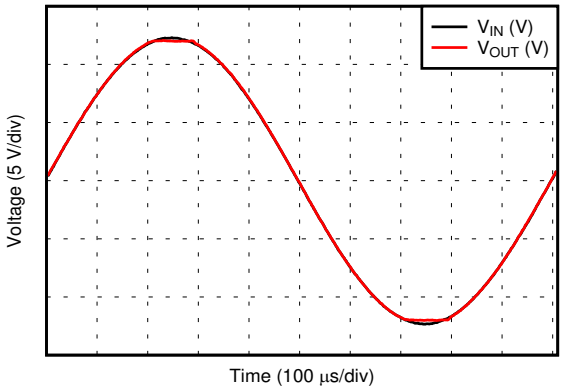


Figure 7-1. No Phase Reversal

7.3.3 Input Bias Current Clock Feedthrough

T OPA2186
UC
UT
9 S
UT
T S RC U

ADVANCE INFORMATION

7.3.4 EMI Rejection

T OPA2186 N MIO MI
T
U MI 9
OPA2186 UT I

10 M 6 G UF 7T2 OPA2186UT 7T1 MIRR RIN
OPA2186 T UT 7T1
US *EMI*
Rejection Ratio of Operational Amplifiers S UU U

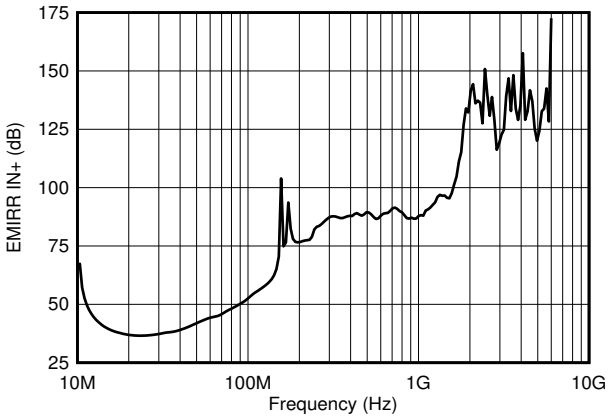


Figure 7-2. EMIRR Testing

Table 7-1. OPA2186 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 M	M S S S S S T NU FO	48l4 B
900 M	G NGSMOS S S GPS N 1U6 GOS GSMS S U F	52l8 B
1l8 G	GSM S S S S LT N1 G 2 GO	69U1 B
2l4 G	802U11 S802U11 S802U11 SB S S S NSMO S S ST N2 G 4 GO	88l9 B
3U6 G	RS S S S ST	82l5 B
5 G	802U11 S802U11 S S S S CT N4 G 8 GO	95l5 B

T N MIO S MIRRS MI
UA
RF UA MI
MIRR UM MIRR S
MIRR RINS MIRR RF
UI S MIRR
8
O MIS RF
U
T
MIRR
MIRR
PCBUT RF
PCB U
T
S
UC MI S S S
S UT
U

F 712 MIRR RIN OPA2186 UT OPA2186 T
750 U MIRR T
U

7.3.4.1 EMIRR +IN Test Configuration

F 713 MIRR RINUA RF T
UT T
T NLPFO NDMMQUA
9 S
MIRR INRUT UT LPF
RF U

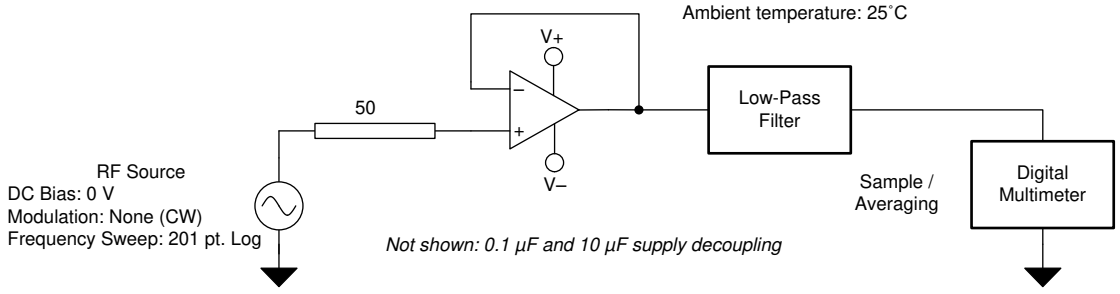
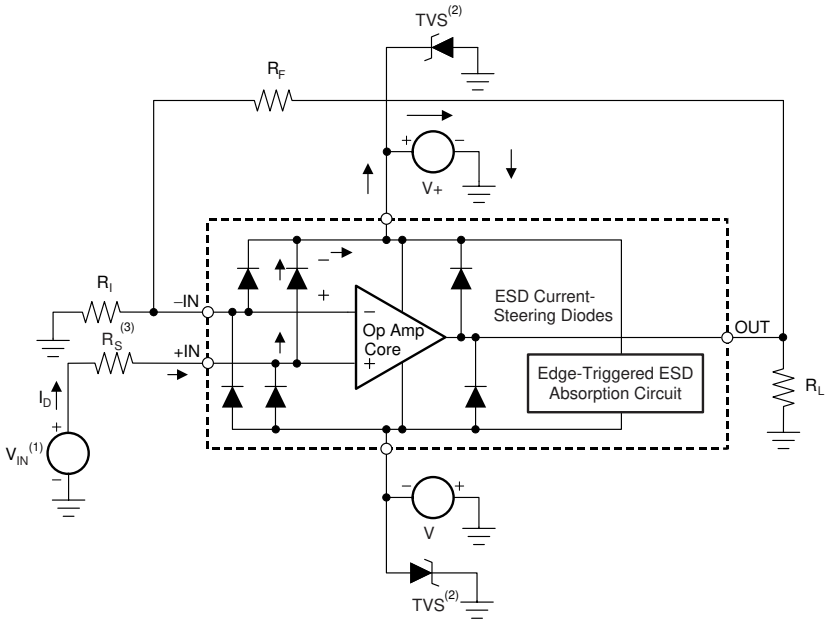


Figure 7-3. EMIRR +IN Test Configuration

ADVANCE INFORMATION

7.3.5 Electrical Overstress

D U
T S
U
U
A S N SDO
SD U
SD
U F 7T4 SD OPA2186 N
QUT SD T
T S
UT
U
A SD T S T T S T
UT SD
UT
U
W SD S
UD S UT
OPA2186S UW S
U
F 7T4 S SD
S U S
UI
S SD S
UA T U



N OVIN N VROR 500 V
N2 OTVS826 V $V_{TVSBR\ NO}$ VRS $V_{TVSBR\ NO}$
U
N3 OS 5 U

Figure 7-4. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

ADVANCE INFORMATION

F 7T4 NV$_{IN}$O NVRO
500 V UM UI VR
S RV$_S$U
V$_{IN}$UA S
10 AU

I SV$_{IN}$ S
UT
U

A
VR V 0 VUA S 0 VS
UI S
T UT

UI S
UT S
U

I S
9 F 7T4UT
U S
U

7.3.6 MUX-Friendly Inputs

T OPA2186
UT S T CMOS T
V$_{GS}$
UL V$_{GS}$
S S U

T OPA2186 T
UT
S RC
UT OPA2186
T T UT OPA2186 UD
T U

7.4 Device Functional Modes

T OPA2186 S T
4L5 V N 2U25 VOUT OPA2186 24 V N 12 VOU

ADVANCE INFORMATION

8 Application and Implementation

Note

I TI S
TI U TI
S
U

8.1 Application Information

T OPA2186 S
UT 0U01
VVC UI S CMRRSPSRRS
A_{OL} T UA S
T UI S0U1T F
U

8.1.1 Basic Noise Calculations

L T UI S
9 T UT
TT U

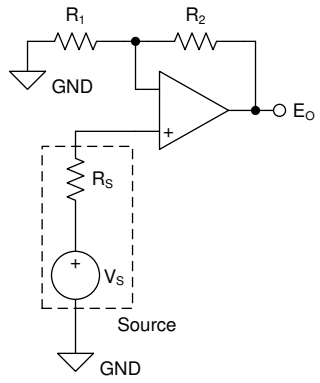
T
UT 9 S
U

F 8T1 *(A)* *(B)* T UI
S UI S
U S
OPA2186 U

T UL
U T

U

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$E_O = \left(1 + \frac{R_2}{R_1}\right)\sqrt{e_n^2 + e_{R_1 \| R_2}^2 + e_{R_S}^2 \left(\frac{R_1 \| R_2}{R_1 + R_2}\right)^2} \quad \text{V}/\sqrt{\text{Hz}}$$

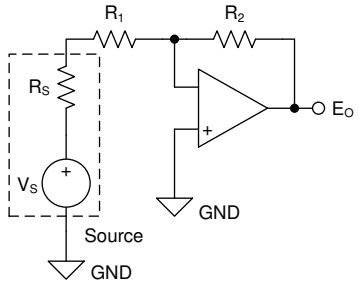
$$e_{R_S} = \sqrt{4 k T(K) R_S} \quad \text{V}/\sqrt{\text{Hz}} \qquad \text{Thermal noise of } R_S$$

$$e_{R_1 \| R_2} = \sqrt{4 k T(K) \left(R_1 \| R_2\right)} \quad \text{V}/\sqrt{\text{Hz}} \qquad \text{Thermal noise of } R_1 \| R_2$$

$$k = 1.38065 \times 10^{-23} \quad \text{J}/\text{K} \qquad \text{Boltzmann Constant}$$

$$T(K) = 237.15 + T(°C) \quad \text{K} \qquad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$E_O = \left(1 + \frac{R_2}{R_S + R_1}\right)\sqrt{e_n^2 + e_{R_1+R_S \| R_2}^2 + e_{R_S}^2 \left(\frac{R_S + R_1 \| R_2}{R_S + R_1 + R_2}\right)^2} \quad \text{V}/\sqrt{\text{Hz}}$$

$$e_{R_1+R_S \| R_2} = \sqrt{4 k T(K) \frac{R_S + R_1 \| R_2}{R_S + R_1 + R_2} \left(R_S + R_1 \| R_2\right)} \quad \text{V}/\sqrt{\text{Hz}} \qquad \text{Thermal noise of } (R_1 + R_S) \| R_2$$

$$k = 1.38065 \times 10^{-23} \quad \text{J}/\text{K} \qquad \text{Boltzmann Constant}$$

$$T(K) = 237.15 + T(°C) \quad \text{K} \qquad \text{Temperature in kelvins}$$

W UF OPA2186 S 38 VV 1 U
NOT8 F S *TI Precision Labs*U

Figure 8-1. Noise Calculation in Gain Configurations

ADVANCE INFORMATION

8.2 Typical Applications

8.2.1 High-Side Current Sensing

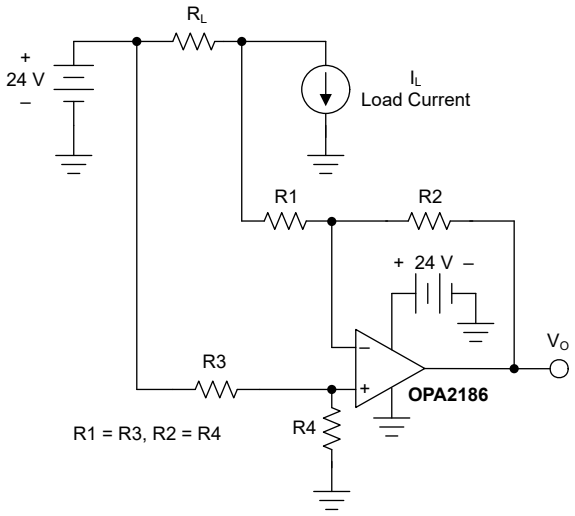


Figure 8-2. High-Side Current Monitor

8.2.1.1 Design Requirements

A S UM

U

F S T T V

OPA2186UT T NV_{CM}O

200 V U

T OPA2186 UT

UT

UC S T

UF 8T2 OPA2186 UL T

U

U 8

S 824 V

L 80L3 V 3L3 V

I 81 A 11 A

T

U

8.2.1.2 Detailed Design Procedure

D T
UO S
NADCO S
U

C OPA2186 T
ADC 3U3 VS UT T
0 V 3U3 VUT OPA2186 24-V S
UA OPA2186 T T V NRRIOO S
N O UT
U

T OPA2186 24 V9 S 3U3TV S
ADC U S OPA2186
0 VS U

T T NA$_{OL}$O
Electrical Characteristics UT A$_{OL}$
300 V NR$_L$ 10 QUT S NV$_{MIN}$O 300 VS
3U3 V V$_{MA}$ S 118I V$_{MA}$ V$_{MIN}$ UT
U

A SI$_{LOAD}$ 10 A UI S S
10 A UT 118I V$_{MA}$ V$_{MIN}$ U
I 11 A S 3U3TV UU 118I S
1 A 300 VU

S R$_S$
UA 10TA R$_S$
10 UT 1 WS 0U1TV 10 AU

N S OPA2186 UT 11 A
10T 110 V UT
SVRS OPA2186 8

$$V_S = I_L * R_S$$
$$V_S = 11\ A * 10\ m\Omega = 110\ mV$$

NIO

T OPA2186 8

$$G_A = \frac{V_{OMAX}}{V_S}$$
$$G_A = \frac{3.3\ V}{0.11\ V} = 30\frac{V}{V}$$

N2O

N S V$_{MIN}$ I$_L$ 1 A8

$$V_{OMIN} = G_A * I_{SMIN} * R_S$$
$$V_{OMIN} = 30\frac{V}{V} * 1\ A * 10\ m\Omega = 300\ mV$$

N3O

ADVANCE INFORMATION

F 8T3 OPA2186 T UT
1 A 11 AS V_{CM} 24TV U

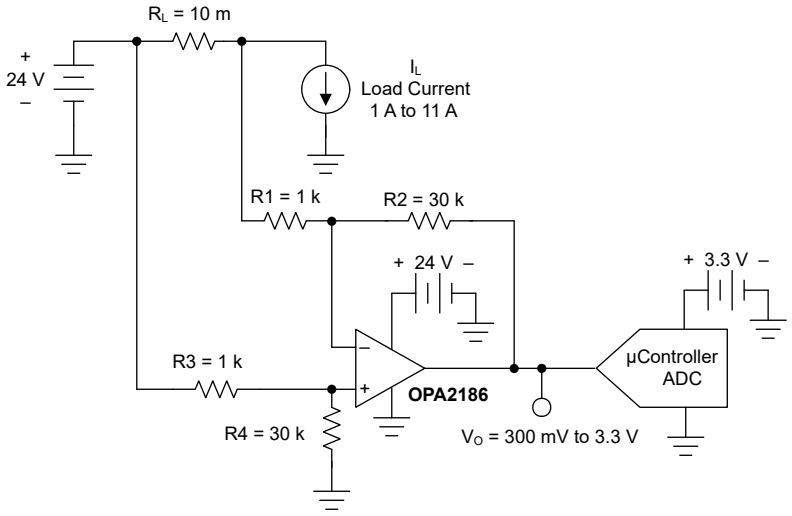


Figure 8-3. OPA2186 Configured as a High-Side Current Monitor

I S OPA2186 3U3 VU S 24TV
S T
U

T F 8T3 TINA S
OPA2186 T UT F 8T4UT
UU S V_O
1 AS V_O 300 V U

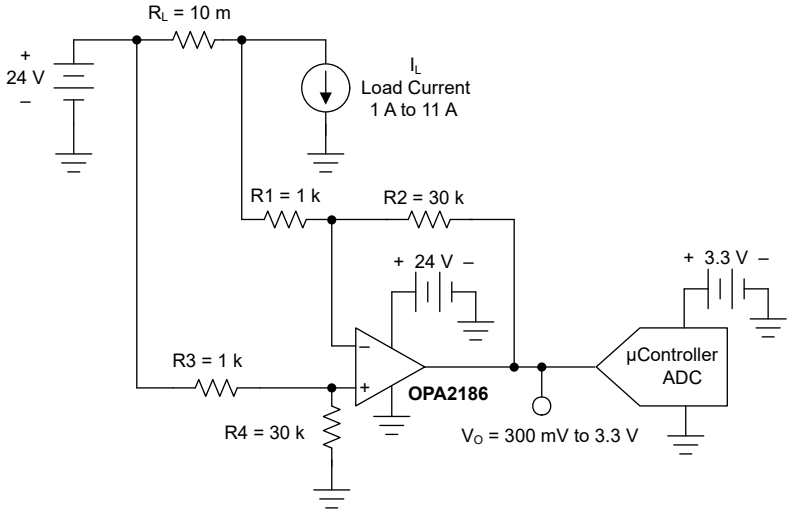


Figure 8-4. OPA2186 High-Side Current-Monitor Simulation Schematic

T OPA2186 S CMOS S 0 V
UT *Electrical Characteristics* OUTPUT V_OS
output slam UT
S UI S
S UT S T S
T 300 V U S
U

L S T 8
A UT R1 R3 R2 R4
T UU 0U1J S
UO S
U
T SGAS OPA2186
UA GA 30 VW U
A S U
T 3T B S S 8

$$f_H = \frac{GBW}{\text{Noise Gain}}$$

M4O

GBW 9750 OPA2186U
N T S 5U

$$G_{NG} = 1 + \frac{R2}{R1}$$

M5O

F OPA2186 F 8T38

$$G_{NG} = 1 + \frac{30\ k\Omega}{1\ k\Omega} = 31\frac{V}{V}$$

$$f_H = \frac{750\ kHz}{31} = 24.2\ kHz$$

M
UA S 24 V S
V_{CM} 0 VUT S
0 VU

T OPA2186 0 V V
UT LM7705 S T S 0U23TV
UP OPA2186 V 300- V
S 0 VS 0 VUT
U

T LM7705 78 A S 3 V
5U25 VUT 3U3TV 5TV ADC U

F T S T S *TI Analog Engineer's Circuit Cookbook: Amplifiers*U

ADVANCE INFORMATION

8.2.1.3 Application Curve

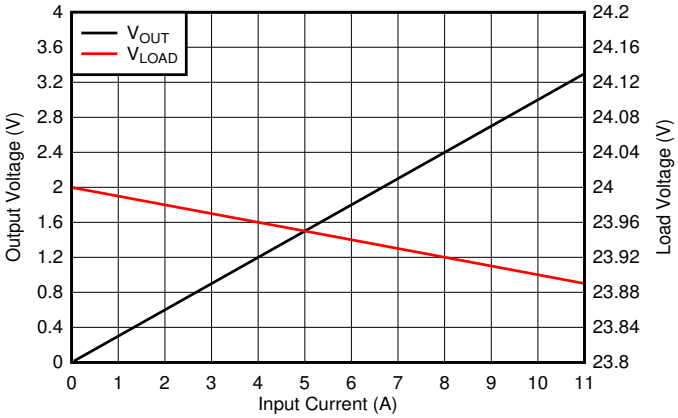


Figure 8-5. High-Side Results

8.2.2 Bridge Amplifier

F 8T6 UC TINATTI
8 *Bridge Amplifier Circuit*U

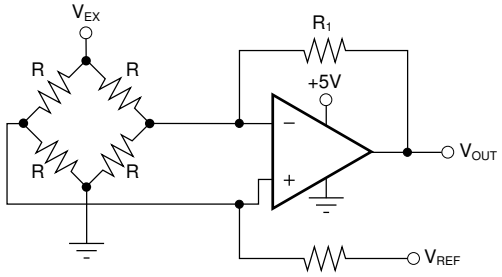


Figure 8-6. Bridge Amplifier

8.3 Power Supply Recommendations

T OPA2186 4U5 V 24 V N 2U2 25 V 12 V0 9
40 C R125 CU

CAUTION

S 40 V N *Absolute Maximum Ratings* OU

P 0U1T F T
- U F S *Section 8.4*U

ADVANCE INFORMATION

8.4 Layout

8.4.1 Layout Guidelines

F S PCB S 8
F S NS O
UA 8
U T N QJ
T U
S S U
N
UB T
U
C T SRS0U1T F S
UA VR T
U
S
UO PCB U
A MI UM
U F S
The PCB is a component of op amp design U
T S UI
S
U
P UA F 8T7 S
NR3O NR4O U
UA
U
C S T UA
U
F S PCB U
A
UF PCB S PCB
UA T S T
85 C 30 U

8.4.2 Layout Example

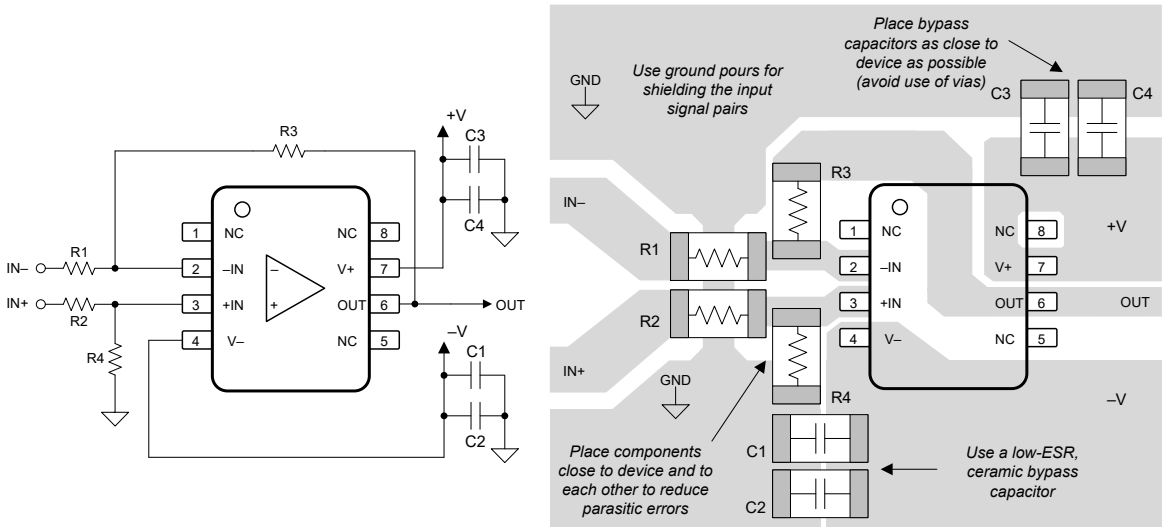


Figure 8-7. Operational Amplifier Board Layout for Difference Amplifier Configuration

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PS TI UC
S
U

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINATTI S S T T
SPIC UTINATTI S T TINA S
S UTINATTI
S S SPIC S
U

A D STINATTI
T UV
S S S
T U

Note

T TINA TINATTI UD
TINATTI TINATTI U

9.2 Documentation Support

9.2.1 Related Documentation

F 8

- T I S*Zero-drift Amplifiers: Features and Benefits*
- T I S*The PCB is a component of op amp design*
- T I S*Operational amplifier gain stability, Part 3: AC gain-error analysis*
- T I S*Operational amplifier gain stability, Part 2: DC gain-error analysis*
- T I S*Using infinite-gain, MFB filter topology in fully differential active filters*
- T I S*Op Amp Performance Analysis*
- T I S*Single-Supply Operation of Operational Amplifiers*
- T I S*Shelf-Life Evaluation of Lead-Free Component Finishes*
- T I S*Feedback Plots Define Op Amp AC Performance*
- T I S*EMI Rejection Ratio of Operational Amplifiers*
- T I S*Analog Linearization of Resistance Temperature Detectors*
- T I S*TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter*

9.3 Receiving Notification of Documentation Updates

T S U UC
Subscribe to updates UF
S U

9.4 Support Resources

TI 2 M T S
US U

L FAS ISF UT TI
TIM 9 TIM T U U

ADVANCE INFORMATION

9.5 Trademarks

TINATTI TI 2 T I U
TINA D S SI U
B B SIGSI U
PS C D S SI U
A U

9.6 Electrostatic Discharge Caution

T SDUT I
U F U
SD U P
U

9.7 Glossary

TI G T S S U

10 Mechanical, Packaging, and Orderable Information

T UT
UT
U F T S T U

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
POPA2186DDFT	ACTIVE	SOT-23-THIN	DDF	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

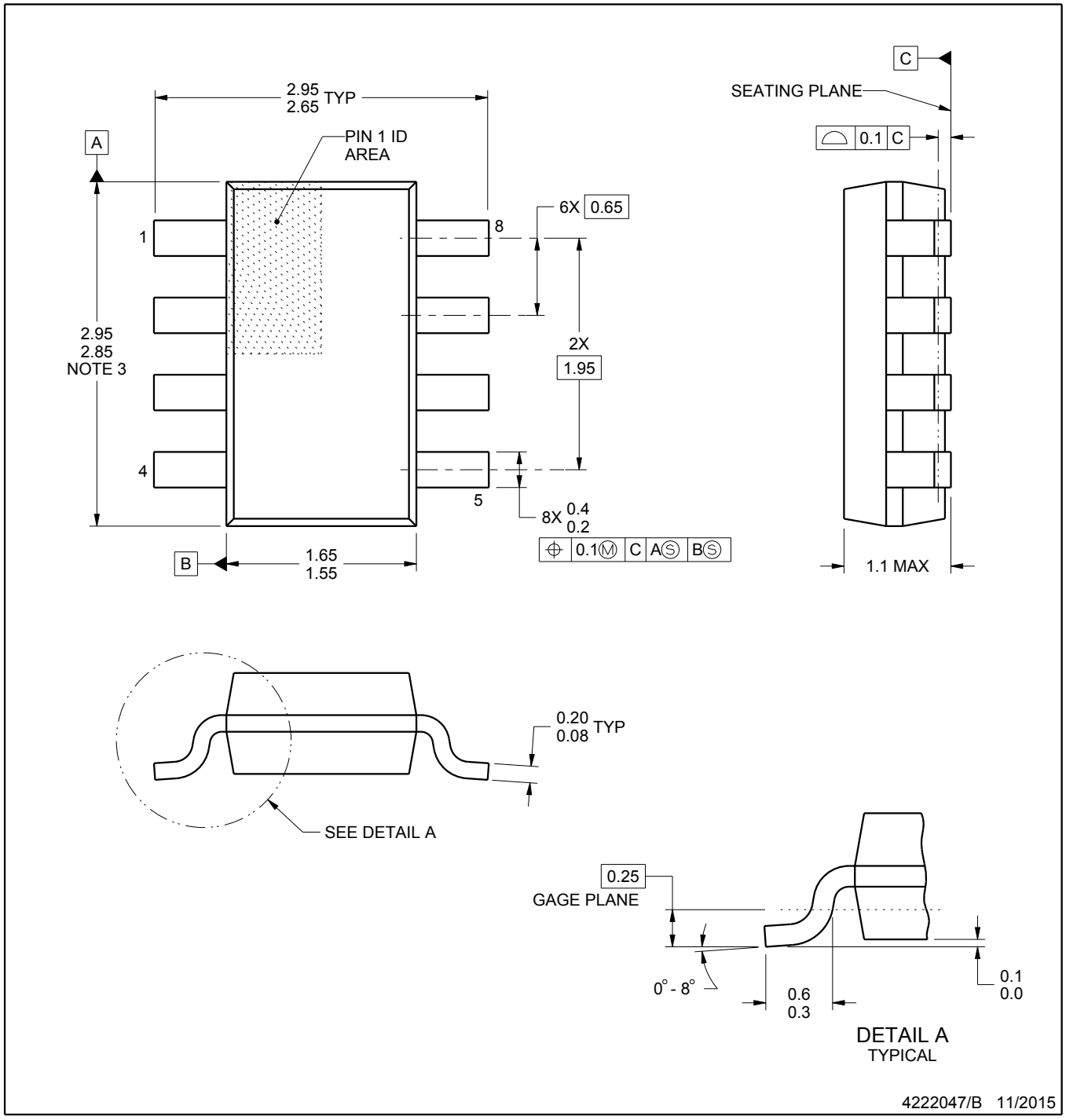
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDF0008A

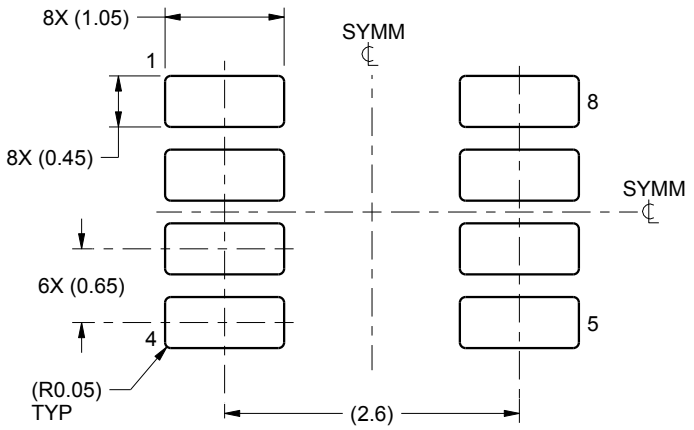
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

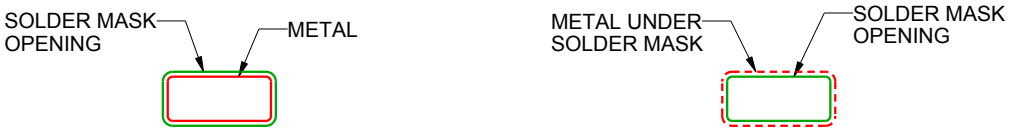


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

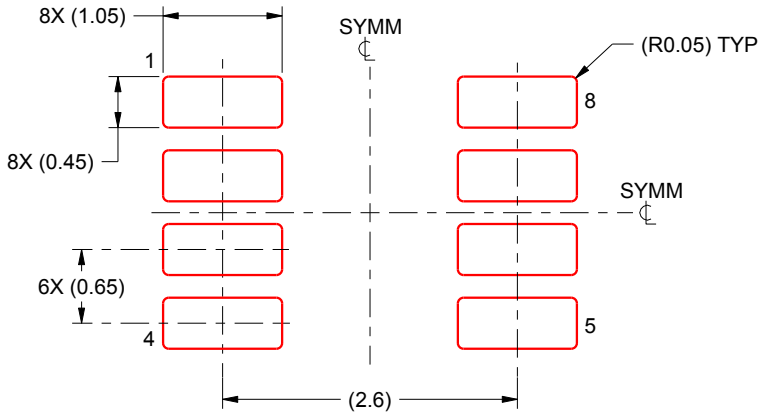
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
OPA388-Q1, OPA2388-Q1
SBOS989A – AUGUST 2020 – REVISED NOVEMBER 2021

OPAx388-Q1 Automotive, Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional-Safety Capable
  - Documentation available to aid functional safety system design (OPA388-Q1)
  - Documentation available to aid functional safety system design (OPA2388-Q1: VSSOP)
- Zero drift: ±0.005 µV/°C
- Zero crossover: 140-dB CMRR true RRIO
- Low noise: 7.0 nV/√Hz at 1 kHz
- No 1/f noise: 140 nV_{PP} (0.1 Hz to 10 Hz)
- Fast settling: 2 µs (1 V to 0.01%)
- Gain bandwidth: 10 MHz
- Single supply: 2.5 V to 5.5 V
- Dual supply: ±1.25 V to ±2.75 V
- True rail-to-rail input
- EMI and RFI filtered inputs
- Industry-standard packages: VSSOP-8, SOT-23-5

2 Applications

- HEV/EV inverter and motor control
- Battery management system (BMS)
- DC/DC converter
- Onboard (OBC) and wireless charger

3 Description

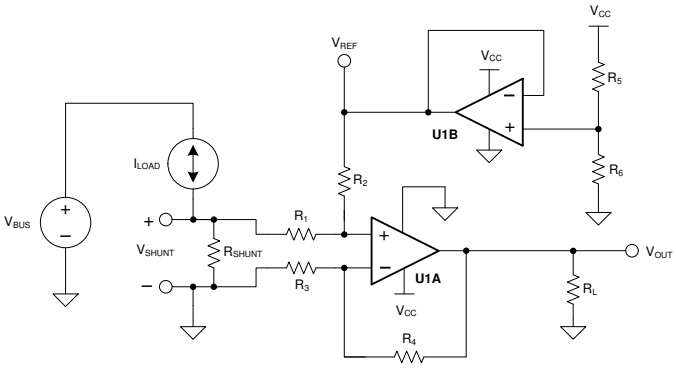
The OPA388-Q1 and OPA2388-Q1 (OPAx388-Q1) are automotive, low-noise, fast-settling, zero-drift, precision operational amplifiers that provide rail-to-rail input and output operation. Excellent ac performance, combined with only 0.25 µV of offset and 0.005 µV/°C of drift over temperature, make the OPAx388-Q1 a great choice for driving high-resolution, analog-to-digital converters (ADCs) with high accuracy. Zero-crossover technology minimizes any offset change over the common-mode range. The combination of low drift and very low 1/f noise allow the OPAx388-Q1 to monitor and detect faulty conditions without compromising signal integrity.

These devices are specified over the industrial temperature range of –40°C to +125°C.

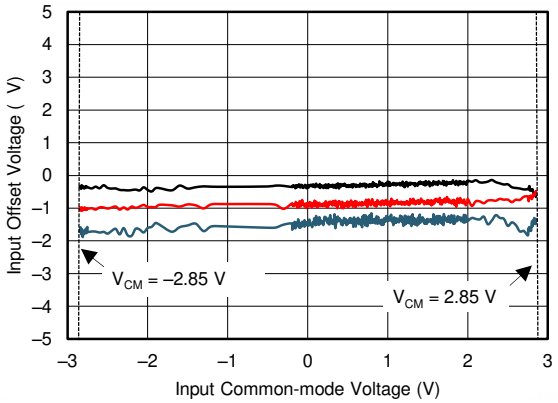
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA388-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2388-Q1	SOIC (8) - Preview	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



The OPA388-Q1 in a Bidirectional Current Shunt Monitor



The OPA388-Q1 Features Ultra-Low Offset Across the Full Common-Mode Range

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2020) to Revision A (November 2021)	Page
• Added OPA2388-Q1 production data (active) device and associated content	1

5 Pin Configuration and Functions

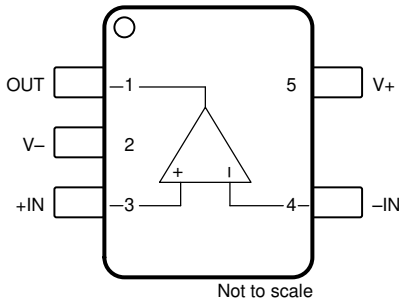


Figure 5-1. OPA388-Q1 DBV (5-Pin SOT-23) Package, Top View

Pin Functions: OPA388-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	4	Input	Inverting input
+IN	3	Input	Noninverting input
NC	—	—	No internal connection (can be left floating)
OUT	1	Output	Output
V–	2	Power	Negative (lowest) power supply
V+	5	Power	Positive (highest) power supply

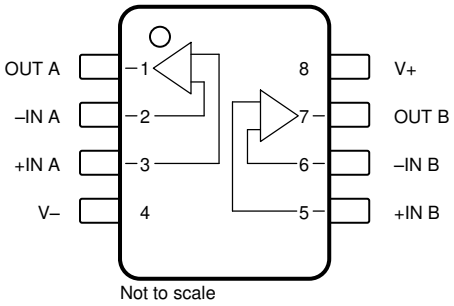


Figure 5-2. OPA2388-Q1 D (8-Pin SOIC, Preview) and DGK (8-Pin VSSOP) Packages, Top View

Pin Functions: OPA2388-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Signal input pins voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Signal input pins current			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	2.5		5.5	V
		Dual-supply	±1.25		±2.75	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA388-Q1

THERMAL METRIC[1]		OPA388-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2388-Q1

THERMAL METRIC[1]		OPA2388-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, V_S = ±1.25 V to ±2.75 V (2.5 V to 5.5 V), and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA388-Q1			±0.25	±5	μV
		OPA2388-Q1			±1.5	±5	
		T_A = –40°C to +125°C				±7.5	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.005	±0.05	μV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.1	±1	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current	R_{IN} = 100 kΩ			±30	±350	pA
			T_A = 0°C to +85°C			±400	
			T_A = –40°C to +125°C			±700	
I_{OS}	Input offset current	R_{IN} = 100 kΩ				±700	pA
			T_A = 0°C to +85°C			±800	
			T_A = –40°C to +125°C			±800	
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			0.14		$μV_{PP}$
e_N	Input voltage noise density	f = 10 Hz			7		nV/√Hz
		f = 100 Hz			7		
		f = 1 kHz			7		
		f = 10 kHz			7		
I_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	V_S = ±1.25 V	124	138		dB
			V_S = ±2.75 V	124	140		
		(V–) < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±1.25 V	114	134		
		(V–) – 0.05 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±2.75 V	124	140		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.15 V < V_O < (V+) – 0.15 V		126	148		dB
			T_A = –40°C to +125°C	120	126		
		(V–) + 0.25 V < V_O < (V+) – 0.25 V, R_{LOAD} = 2 kΩ		126	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ	T_A = –40°C to +125°C	120	148		

6.6 Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, V_S = ±1.25 V to ±2.75 V (2.5 V to 5.5 V), and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity-gain bandwidth				10		MHz
SR	Slew rate	G = 1, 4-V step			5		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}			0.0005%		
t_S	Settling time	V_S = ±2.5 V, G = 1, 1-V step	To 0.1%		0.75		µs
			To 0.01%		2		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			10		µs
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		1	15	mV
					5	20	
			R_{LOAD} = 2 kΩ		20	50	
		Negative rail	No load		5	15	
					10	20	
			R_{LOAD} = 2 kΩ		40	60	
		T_A = –40°C to +125°C, both rails, R_{LOAD} = 10 kΩ			10	25	
I_{SC}	Short-circuit current	V_S = 5.5 V			±60		mA
		V_S = 2.5 V			±30		
C_{LOAD}	Capacitive load drive				See Figure 6-25		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 6-24			100		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±1.25 V (V_S = 2.5 V), I_O = 0 A			1.7	2.4	mA
			T_A = –40°C to +125°C		1.7	2.4	
		V_S = ±2.75 V (V_S = 5.5 V), I_O = 0 A			1.9	2.6	
			T_A = –40°C to +125°C		1.9	2.6	

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

Table 6-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 6-1
Offset Voltage Drift Distribution From –40°C to +125°C	Figure 6-2
Offset Voltage vs Temperature	Figure 6-3
Offset Voltage vs Common-Mode Voltage	Figure 6-4
Offset Voltage vs Power Supply	Figure 6-5
Offset Voltage Long Term Drift	Figure 6-6
Open-Loop Gain and Phase vs Frequency	Figure 6-7
Closed-Loop Gain and Phase vs Frequency	Figure 6-8
Input Bias Current vs Common-Mode Voltage	Figure 6-9
Input Bias Current vs Temperature	Figure 6-10
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 6-11
CMRR and PSRR vs Frequency	Figure 6-12
CMRR vs Temperature	Figure 6-13
PSRR vs Temperature	Figure 6-14
0.1-Hz to 10-Hz Noise	Figure 6-15
Input Voltage Noise Spectral Density vs Frequency	Figure 6-16
THD+N Ratio vs Frequency	Figure 6-17
THD+N vs Output Amplitude	Figure 6-18
Spectral Content	Figure 6-19, Figure 6-20
Quiescent Current vs Supply Voltage	Figure 6-21
Quiescent Current vs Temperature	Figure 6-22
Open-Loop Gain vs Temperature	Figure 6-23
Open-Loop Output Impedance vs Frequency	Figure 6-24
Small-Signal Overshoot vs Capacitive Load (10-mV Step)	Figure 6-25
No Phase Reversal	Figure 6-26
Positive Overload Recovery	Figure 6-27
Negative Overload Recovery	Figure 6-28
Small-Signal Step Response (10-mV Step)	Figure 6-29, Figure 6-30
Large-Signal Step Response (4-V Step)	Figure 6-31 , Figure 6-32
Settling Time	Figure 6-33, Figure 6-34
Short-Circuit Current vs Temperature	Figure 6-35
Maximum Output Voltage vs Frequency	Figure 6-36
EMIRR vs Frequency	Figure 6-37

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

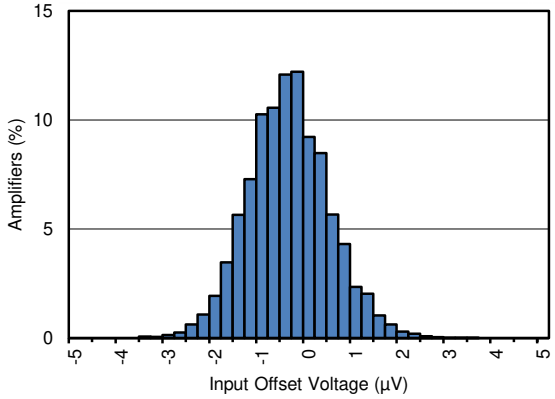
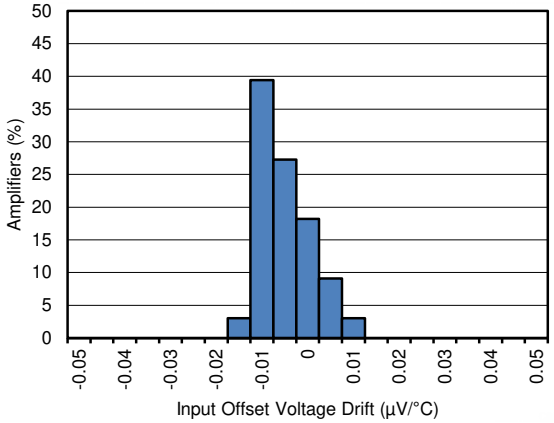


Figure 6-1. Offset Voltage Production Distribution



T_A = –40°C to +125°C

Figure 6-2. Offset Voltage Drift Distribution

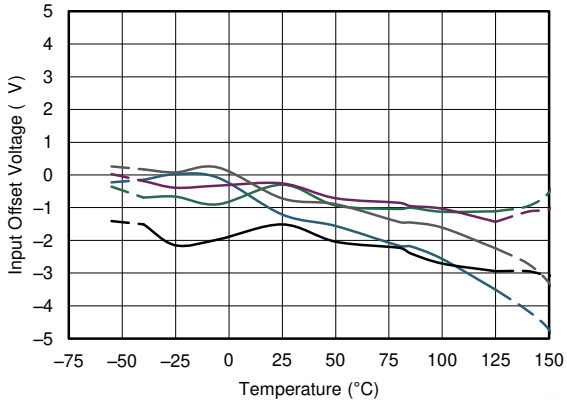


Figure 6-3. Offset Voltage vs Temperature

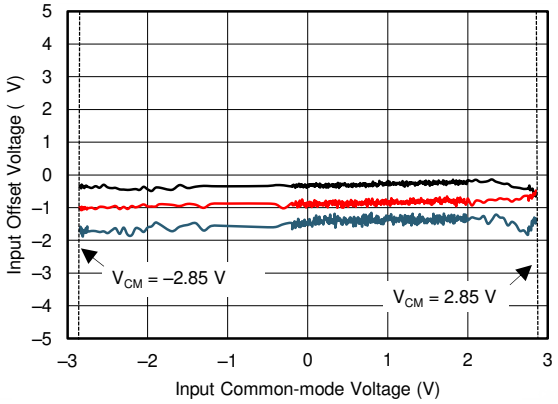


Figure 6-4. Offset Voltage vs Common-Mode Voltage

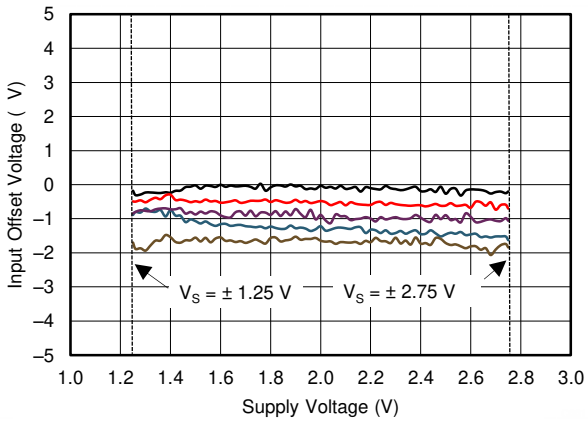
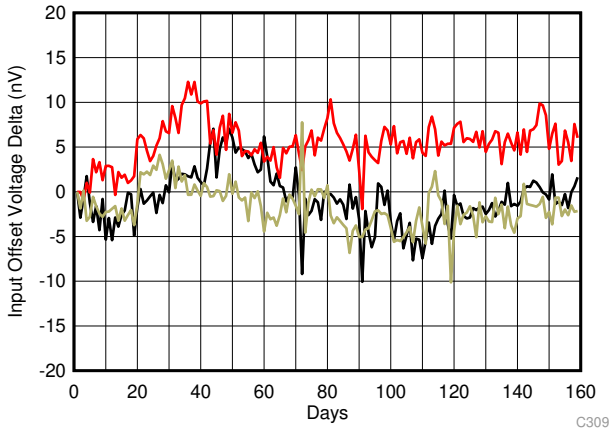


Figure 6-5. Offset Voltage vs Supply Voltage



3 typical units

Figure 6-6. Offset Voltage Long Term Drift

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

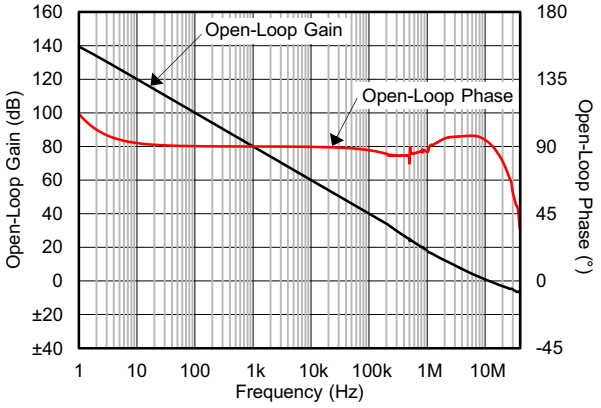


Figure 6-7. Open-Loop Gain and Phase vs Frequency

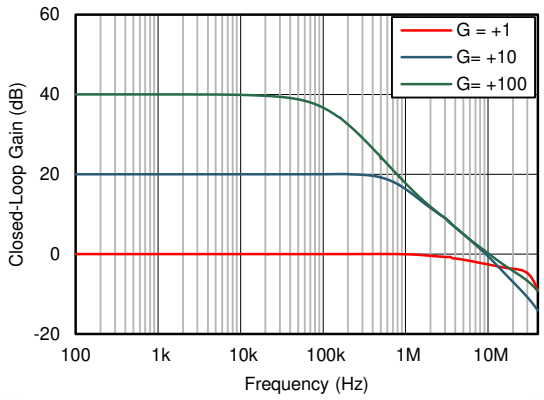


Figure 6-8. Closed-Loop Gain and Phase vs Frequency

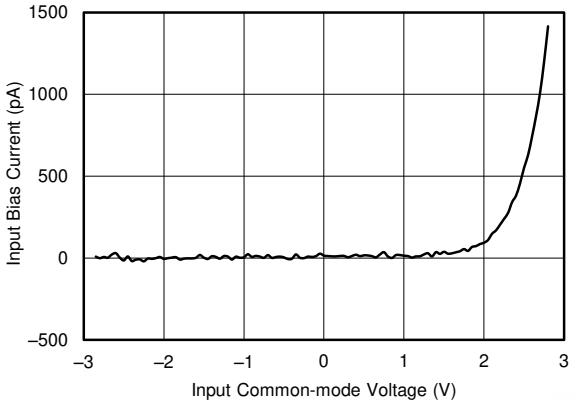


Figure 6-9. Input Bias Current vs Common-Mode Voltage

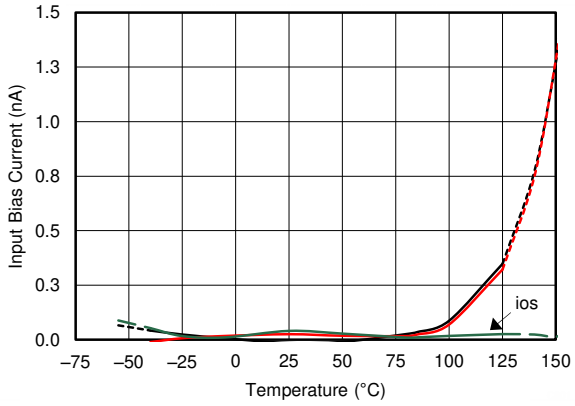


Figure 6-10. Input Bias Current vs Temperature

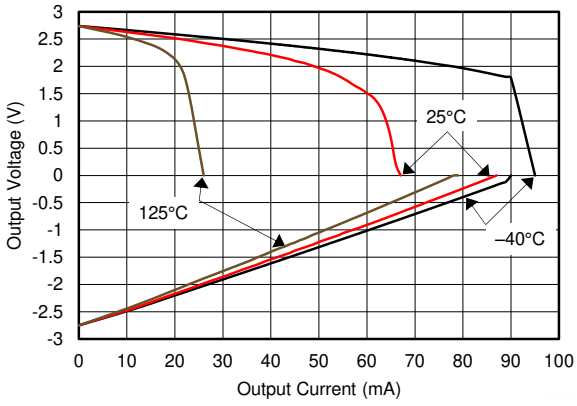


Figure 6-11. Output Voltage Swing vs Output Current (Maximum Supply)

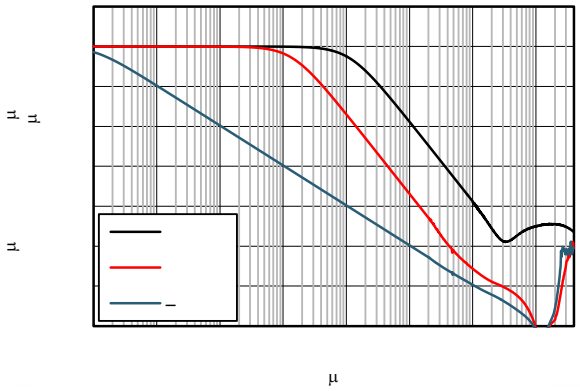


Figure 6-12. CMRR and PSRR vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

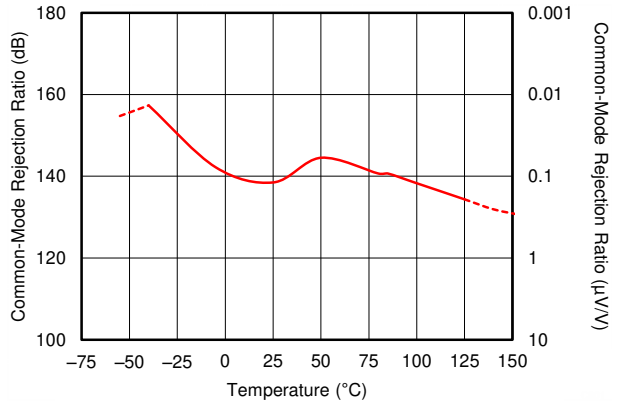


Figure 6-13. CMRR vs Temperature

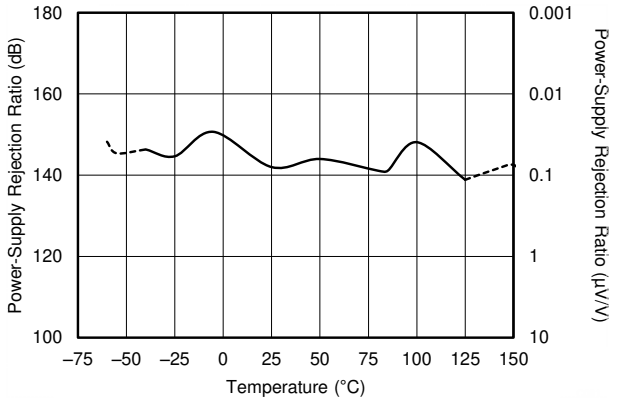


Figure 6-14. PSRR vs Temperature

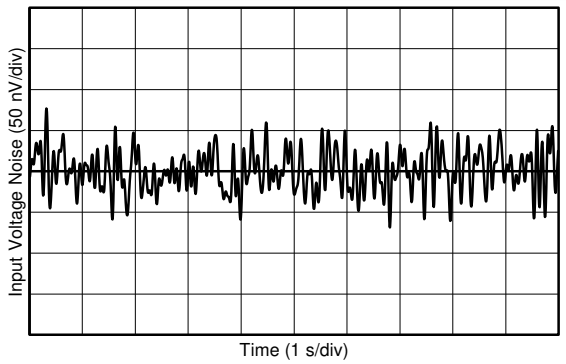


Figure 6-15. 0.1-Hz to 10-Hz Noise

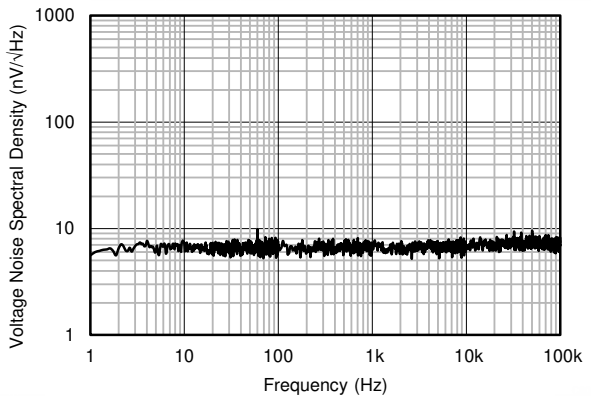


Figure 6-16. Input Voltage Noise Spectral Density vs Frequency

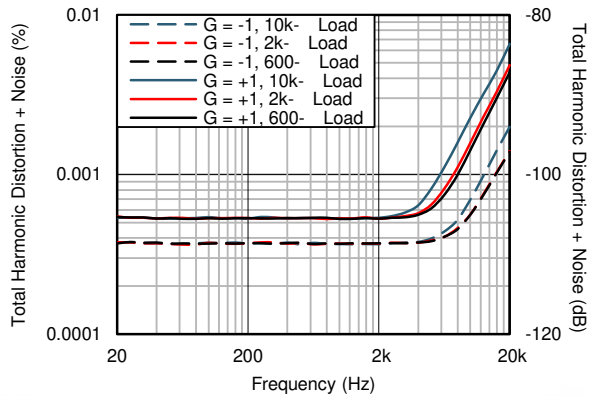


Figure 6-17. THD+N Ratio vs Frequency

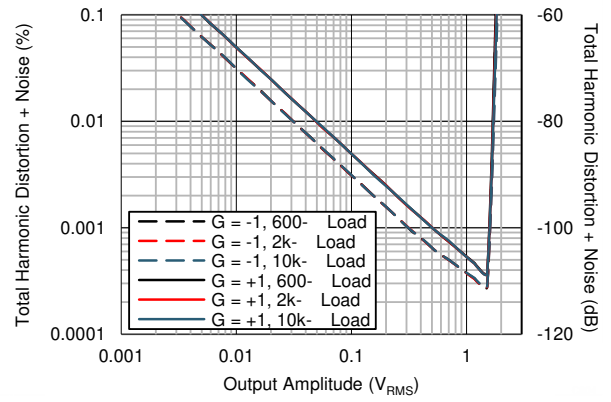
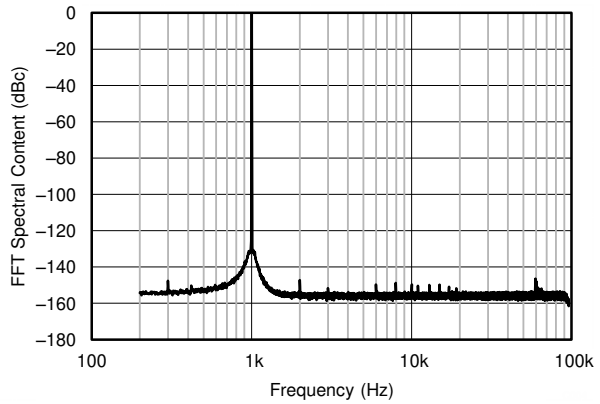


Figure 6-18. THD+N vs Output Amplitude

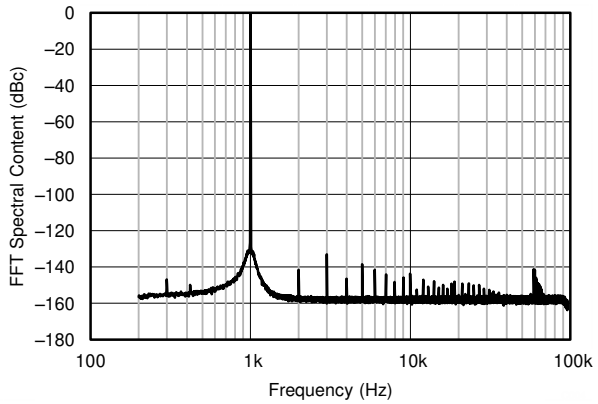
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 10 kΩ, BW = 90 kHz

Figure 6-19. Spectral Content (With 10-kΩ Load)



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 2 kΩ, BW = 90 kHz

Figure 6-20. Spectral Content (With 2-kΩ Load)

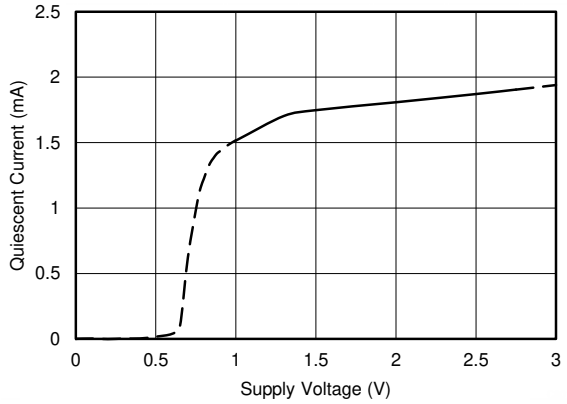


Figure 6-21. Quiescent Current vs Supply Voltage

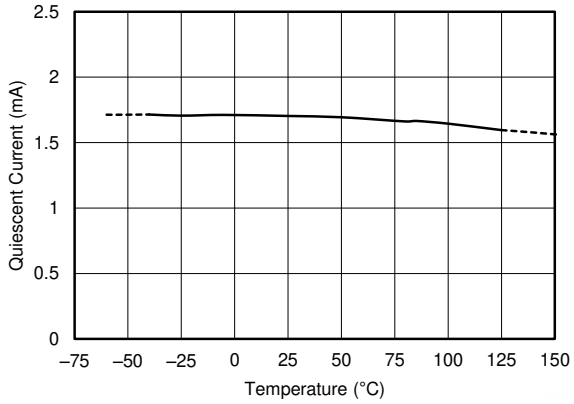


Figure 6-22. Quiescent Current vs Temperature

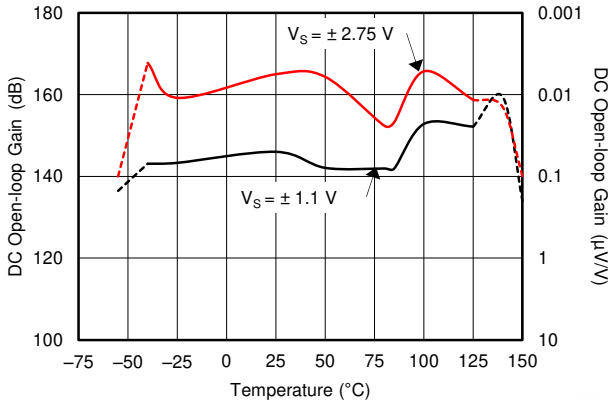


Figure 6-23. Open-Loop Gain vs Temperature

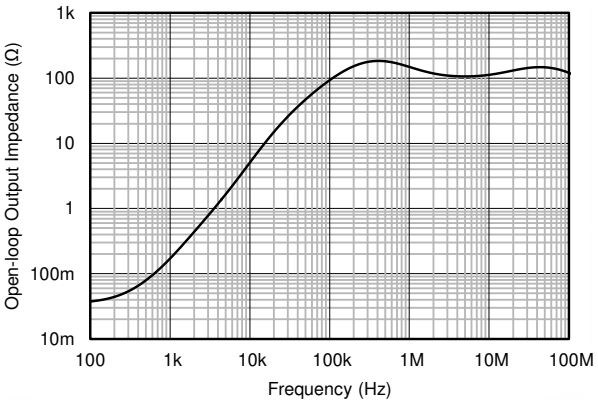


Figure 6-24. Open-Loop Output Impedance vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

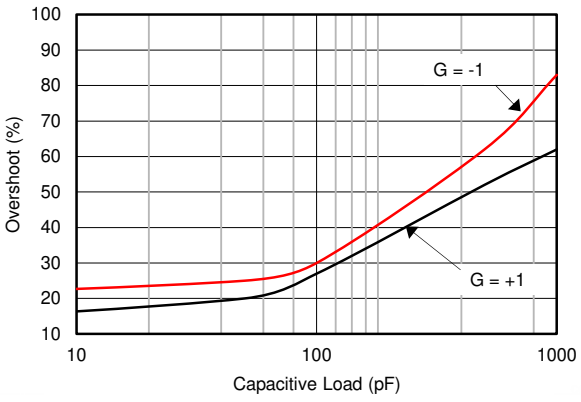


Figure 6-25. Small-Signal Overshoot vs Capacitive Load

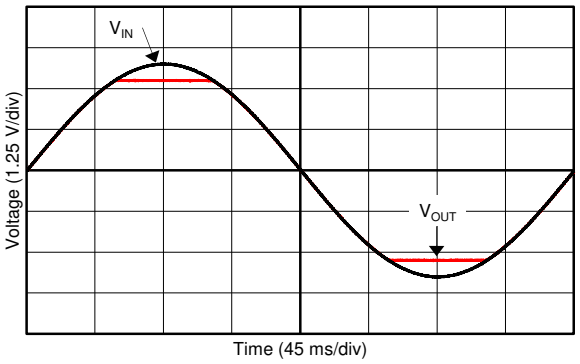


Figure 6-26. No Phase Reversal

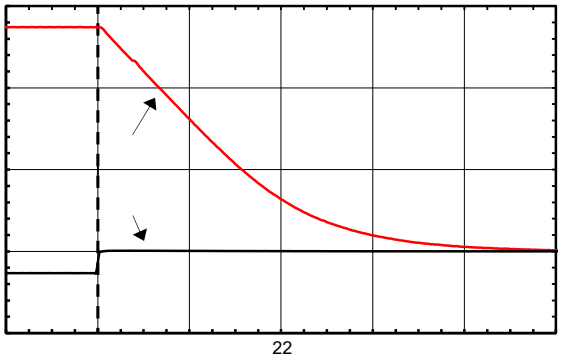


Figure 6-27. Positive Overload Recovery

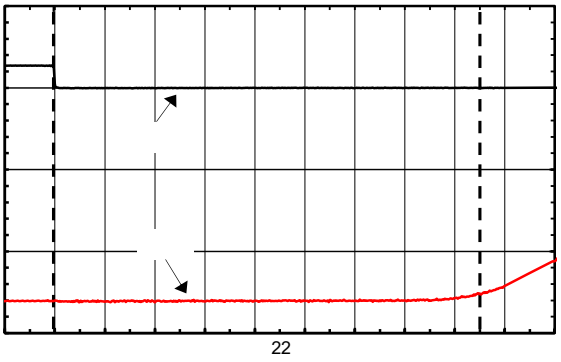
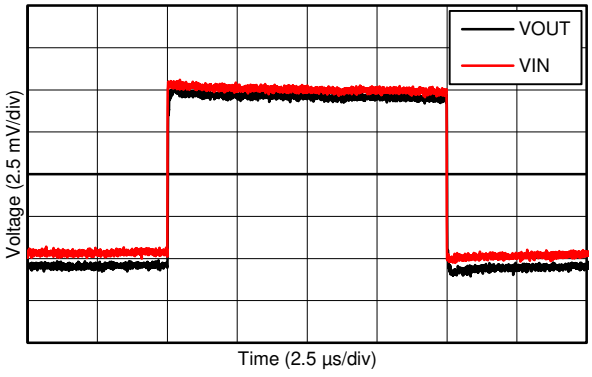
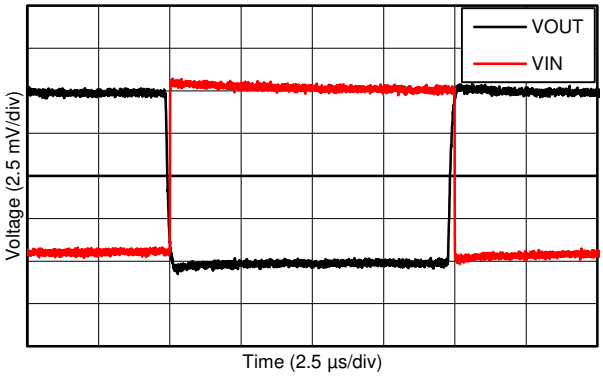


Figure 6-28. Negative Overload Recovery



G = +1, 10-mV step

Figure 6-29. Small-Signal Step Response

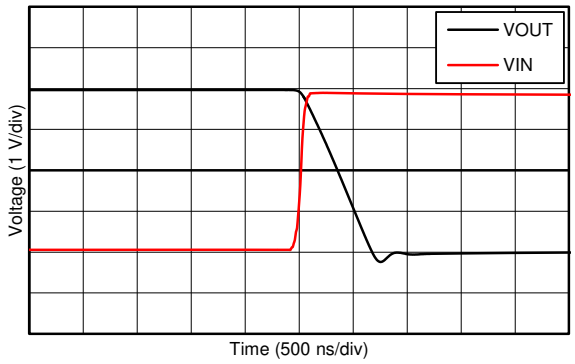


G = –1, 10-mV step

Figure 6-30. Small-Signal Step Response

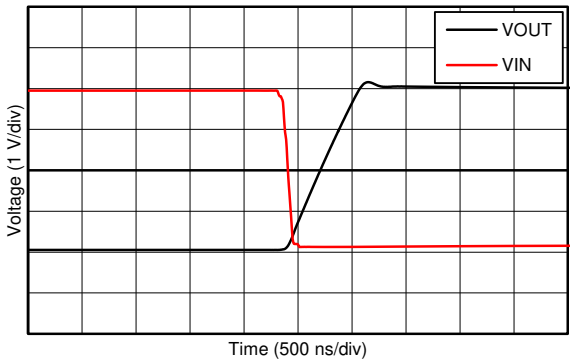
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



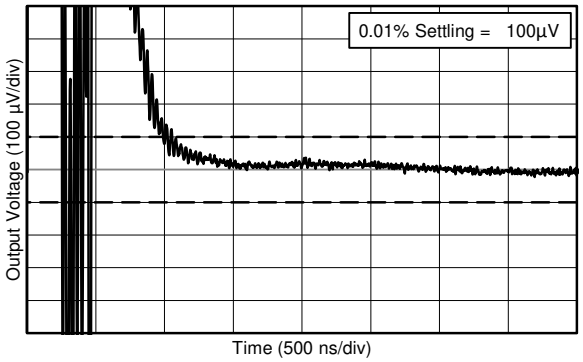
Falling output, 4-V Step

Figure 6-31. Large-Signal Step Response



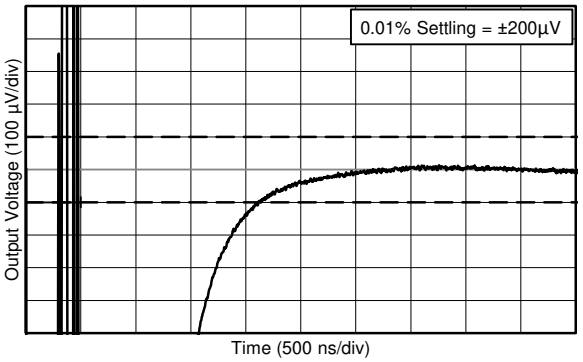
Rising output, 4-V step

Figure 6-32. Large-Signal Step Response



0.01% settling = ±100 µV, 1-V positive step

Figure 6-33. Settling Time



0.01% settling = ±200 µV, 1-V negative step

Figure 6-34. Settling Time

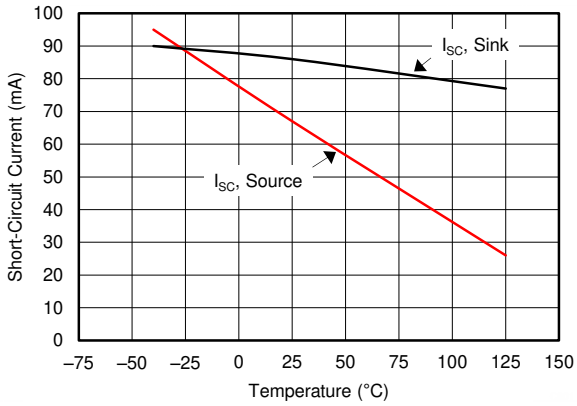


Figure 6-35. Short-Circuit Current vs Temperature

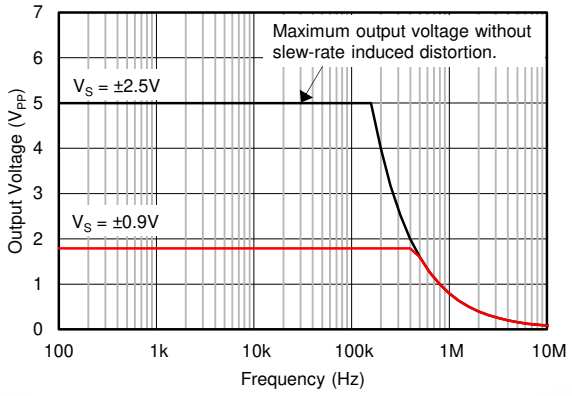
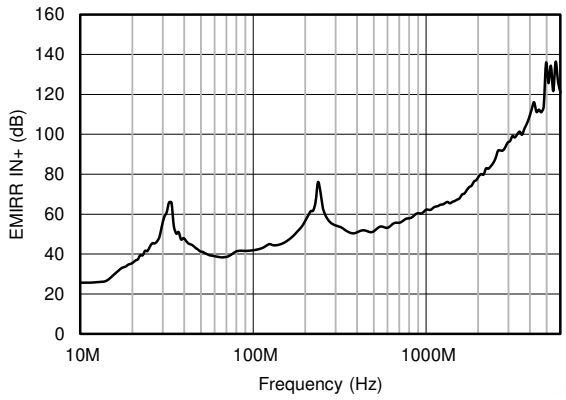


Figure 6-36. Maximum Output Voltage vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



P_{RF} = –10 dBm

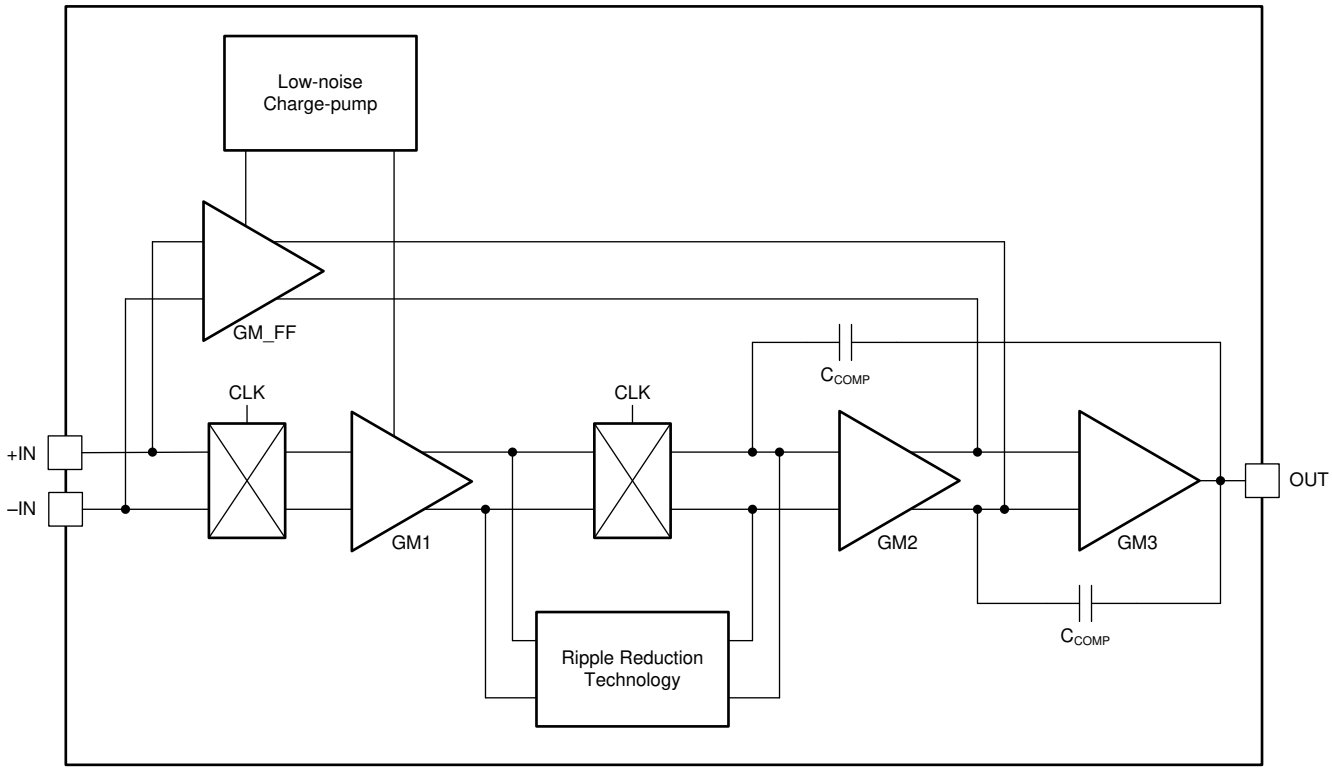
Figure 6-37. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The OPAx388-Q1 zero-drift amplifiers are engineered with the unique combination of a proprietary precision auto-calibration technique and a low-noise, low-ripple, input charge pump. These amplifiers offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx388-Q1 operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The integrated, low-noise charge pump allows true rail-to-rail input common-mode operation without distortion associated with complementary rail-to-rail input topologies (input crossover distortion). The OPAx388-Q1 strengths also include 10-MHz bandwidth, 7-nV/$\sqrt{\text{Hz}}$ noise spectral density, and no 1/f noise, making these devices an excellent choice for interfacing with sensor modules and buffering high-fidelity digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage and Zero-Crossover Functionality

The OPAx388-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. This amplifier family is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers. Operating a complementary rail-to-rail input amplifier with signals traversing the transition region results in unwanted non-linear behavior and polluted spectral content. Figure 7-1 and Figure 7-2 contrast the performance of a traditional complementary rail-to-rail input stage amplifier with the performance of the zero-crossover OPAx388-Q1. Significant harmonic content and distortion is generated during the differential pair transition (such a transition does not exist in the OPAx388-Q1). Crossover distortion is eliminated through the use of a single differential pair coupled with an internal low-noise charge pump. The OPAx388-Q1 maintain noise, bandwidth, and offset performance throughout the input common-mode range, thus reducing printed circuit board (PCB) and bill of materials (BOM) complexity through the reduction of power-supply rails.

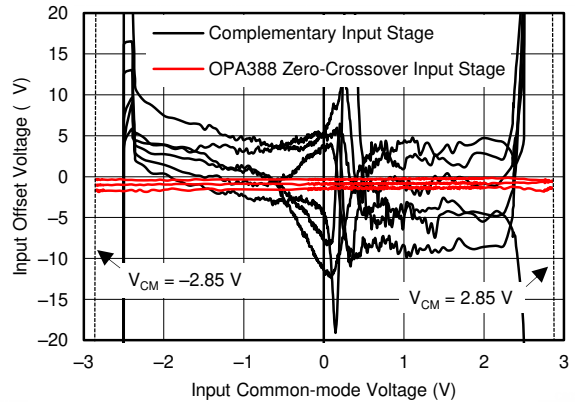


Figure 7-1. Input Crossover Distortion Nonlinearity

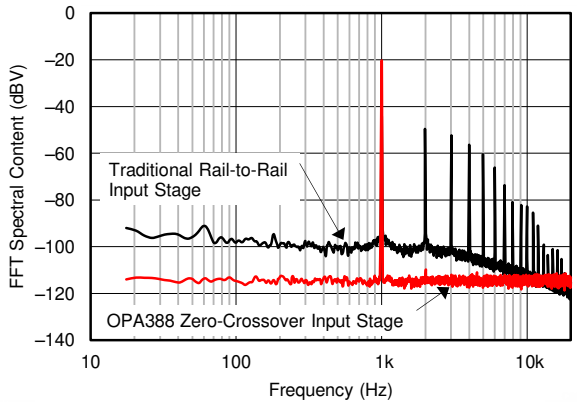


Figure 7-2. Input Crossover Distortion Spectral Content

Typically, input bias current is approximately ±30 pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 7-3.

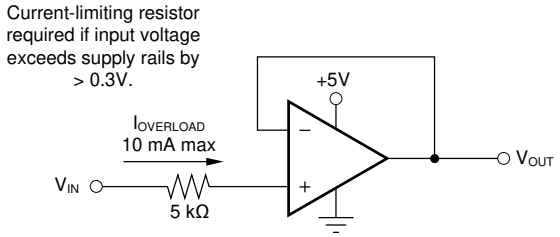


Figure 7-3. Input Current Protection

7.3.2 Input Differential Voltage

The typical input bias current of the OPAx388-Q1 during normal operation is approximately 30 pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when an operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 7-4. Notice that the input bias current remains within specification in the linear region.

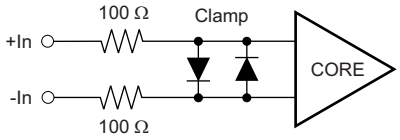


Figure 7-4. Equivalent Input Circuit

7.3.3 Internal Offset Correction

The OPAx388-Q1 operational amplifiers use an auto-calibration technique with a time-continuous, 200-kHz operational amplifier in the signal path. These amplifiers are zero-corrected every 5 µs using a proprietary technique. At power up, the amplifiers require approximately 1 ms to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx388-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.

7.4 Device Functional Modes

The OPAx388-Q1 have a single functional mode and are operational when the power-supply voltage is greater than 2.5 V (±1.25 V). The maximum specified power-supply voltage for the OPAx388-Q1 is 5.5 V (±2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx388-Q1 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPAx388-Q1 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx388-Q1 precision amplifiers are designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

8.2 Typical Application

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA388-Q1 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 8-1 shows the circuit drawing.

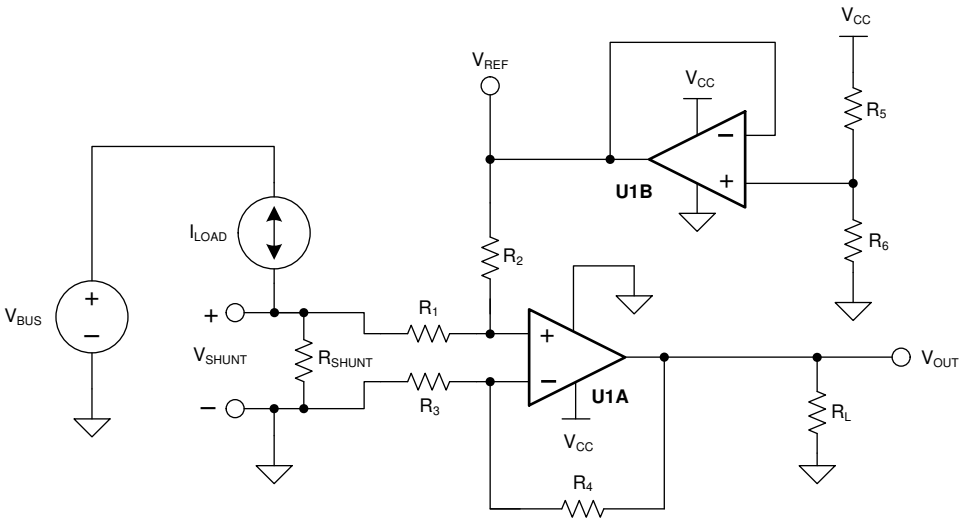


Figure 8-1. Bidirectional Current-Sensing

8.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT} \le \frac{V_{SHUNT}}{I_{LOAD}} \le \frac{100\ mV}{1\ A} \le 100\ \Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA388-Q1, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPA388-Q1 has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA388-Q1 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA388-Q1 given a 3.3-V supply.

$$-100\ \text{mV} < V_{CM} < 3.4\ \text{V} \tag{3}$$

$$100\ \text{mV} < V_{OUT} < 3.2\ \text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ \text{V} - 100\ \text{mV}}{100\ \text{m}\Omega \times [1\ \text{A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.3 Application Curve

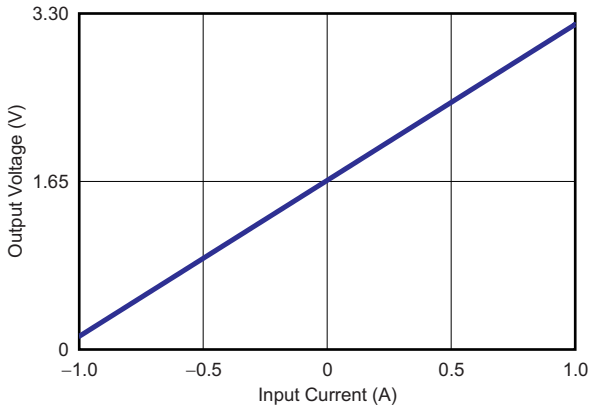


Figure 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

9 Power Supply Recommendations

The OPAx388-Q1 family of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 2.5 V (±1.25 V) up to 5.5 V (±2.75 V). Key parameters that vary over the supply voltage or temperature range are shown in *Section 6.7*.

CAUTION
Supply voltages greater than 7 V can permanently damage the device (see Section 6.1).

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short and, if possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close as possible to the device pins. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, optimize the circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by making sure these potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or greater, depending on the materials used.

10.2 Layout Example

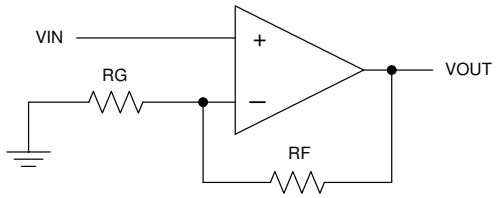


Figure 10-1. Schematic Representation

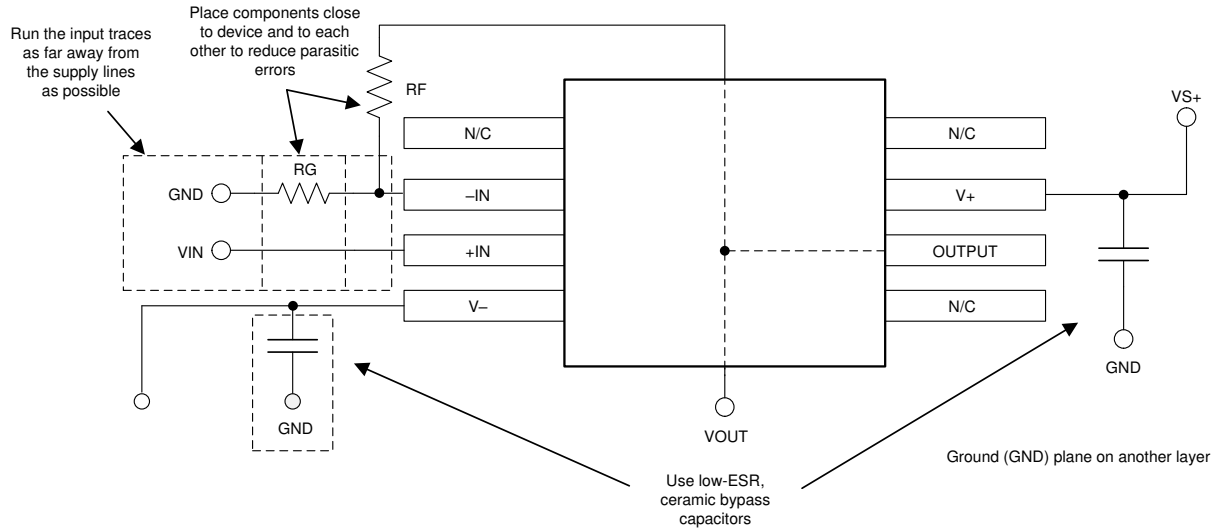


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

11.1.1.2 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

11.1.1.3 TI Precision Designs

The OPAx388-Q1 family is featured on TI Precision Designs, available online at www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following: Texas Instruments, *Circuit board layout techniques*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2388QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	O28Q	Samples
OPA388QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	388Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2388-Q1, OPA388-Q1 :

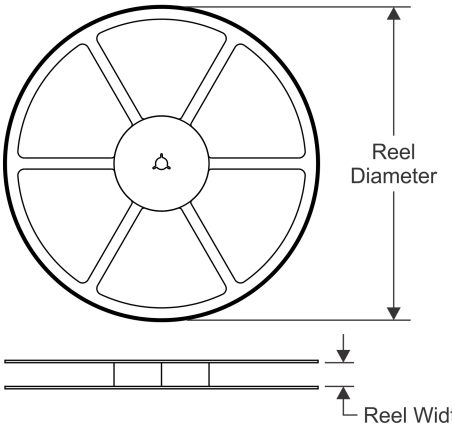
- Catalog : OPA2388, OPA388

NOTE: Qualified Version Definitions:

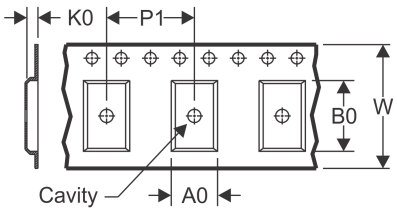
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

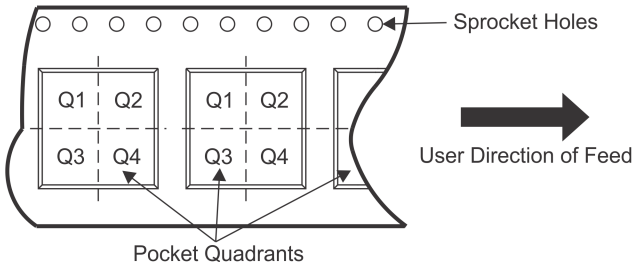


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

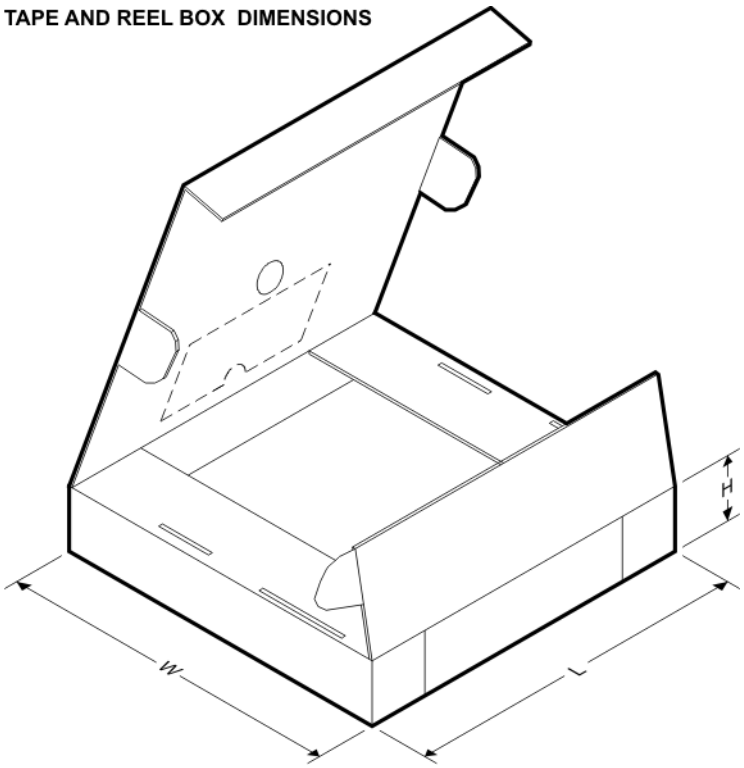
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2388QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA388QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

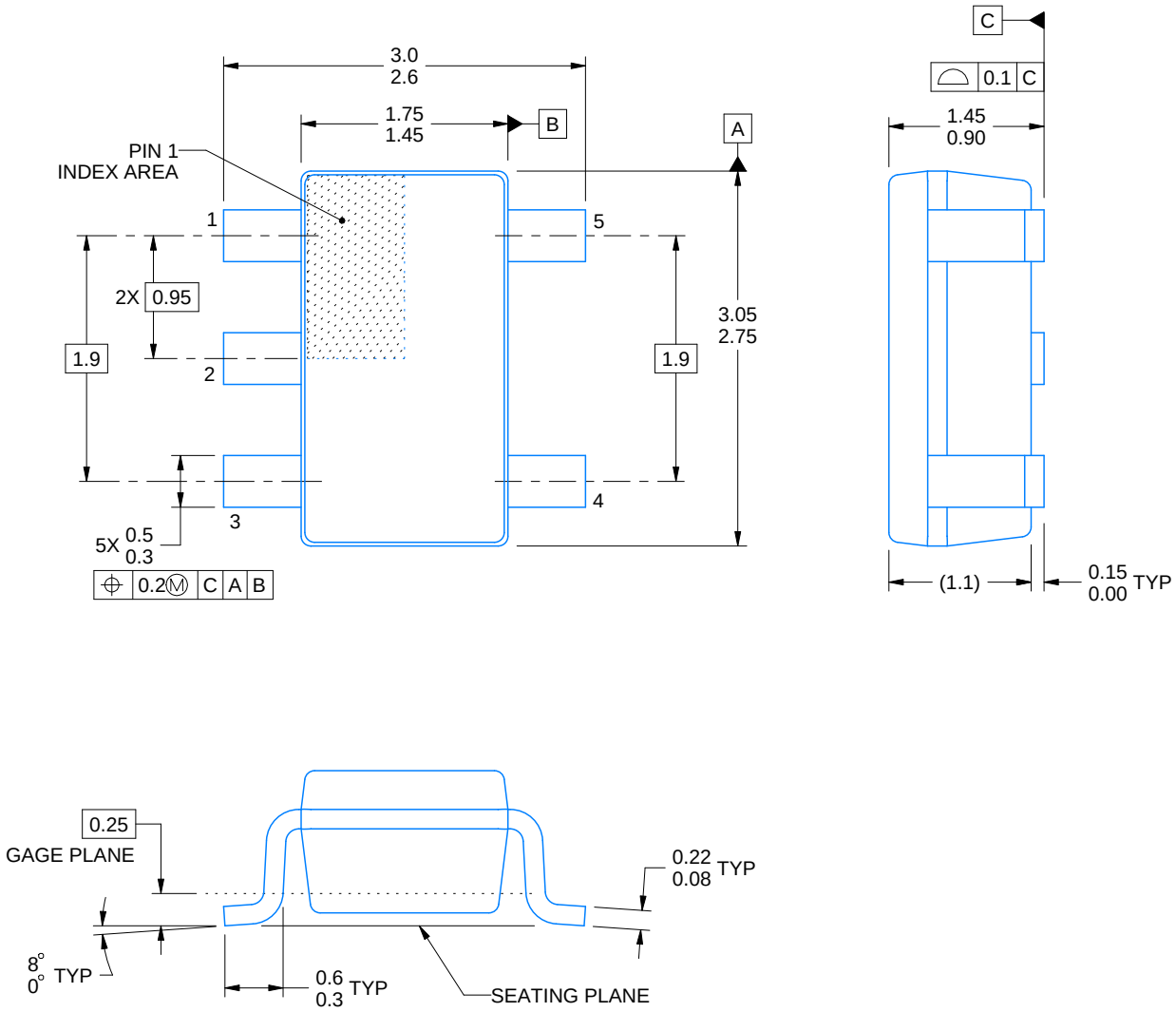
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2388QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA388QDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

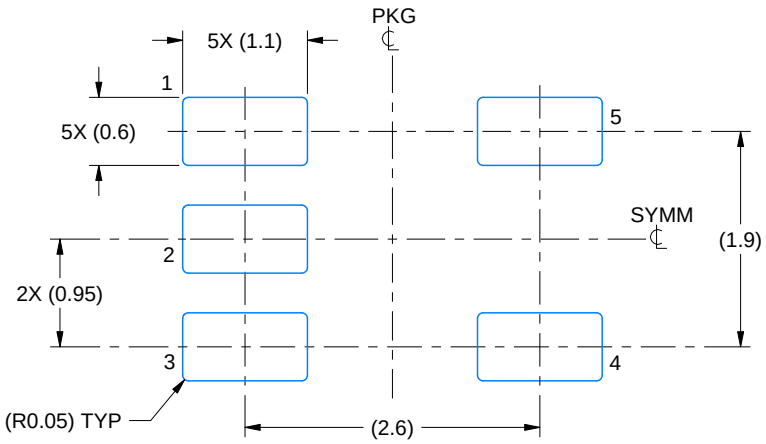
SMALL OUTLINE TRANSISTOR



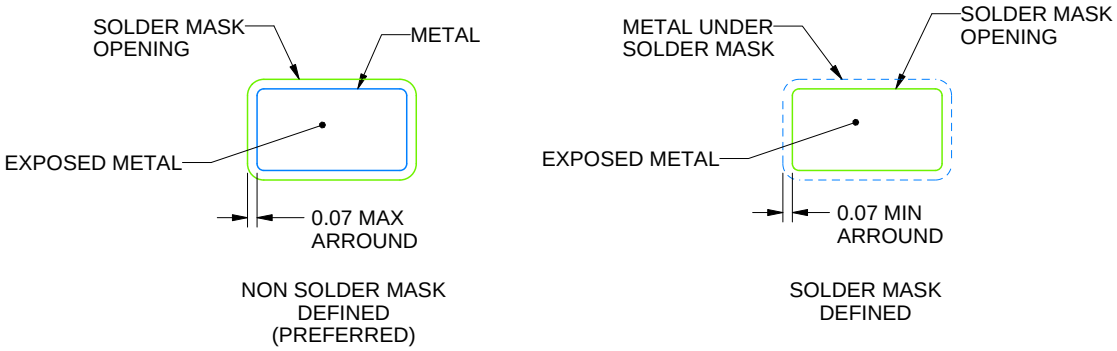
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

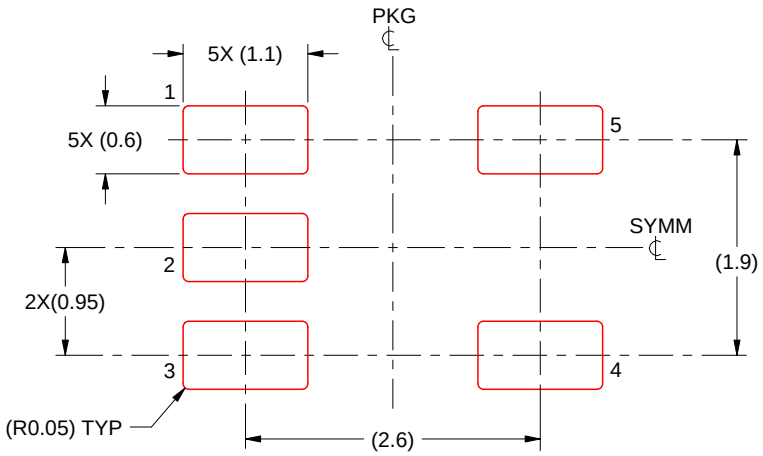


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



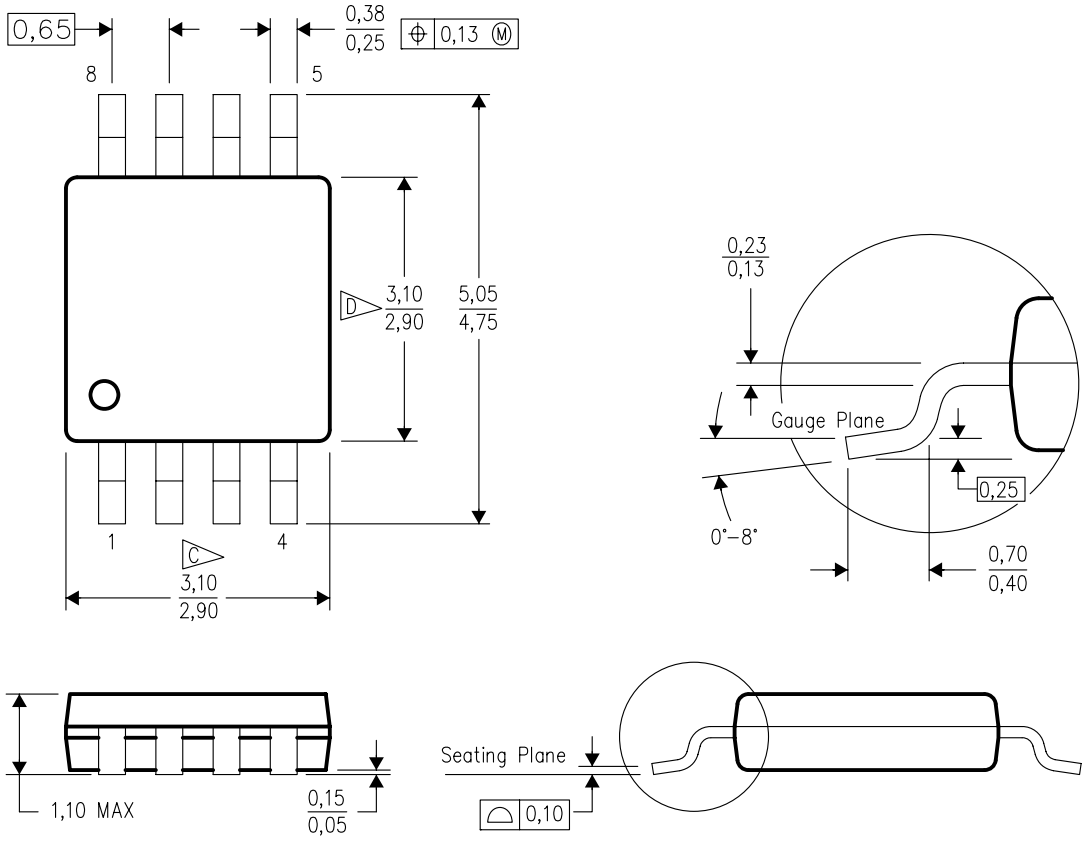
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

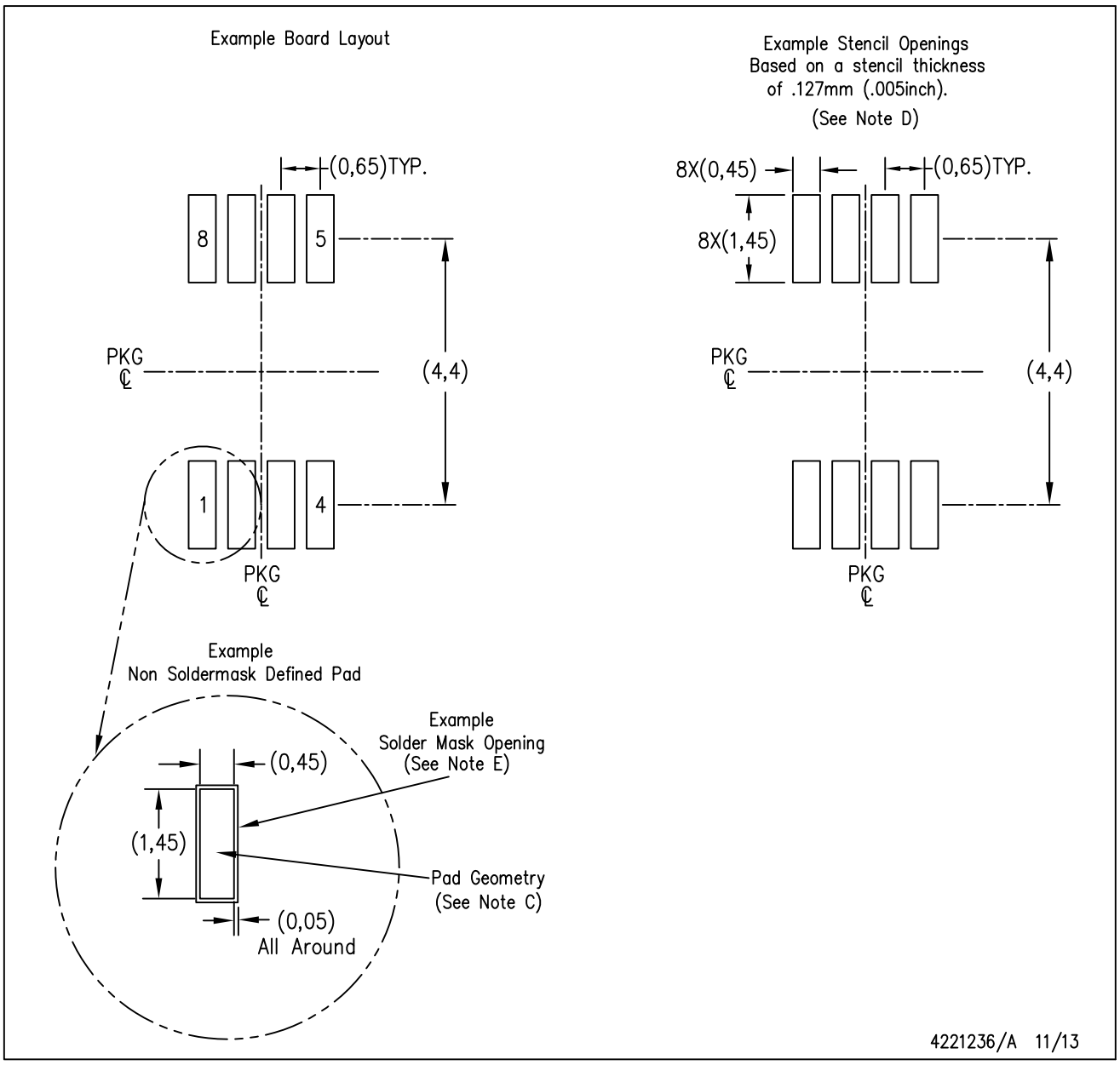
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
OPA392, OPA2392
SBOS926C – JANUARY 2021 – REVISED JULY 2022

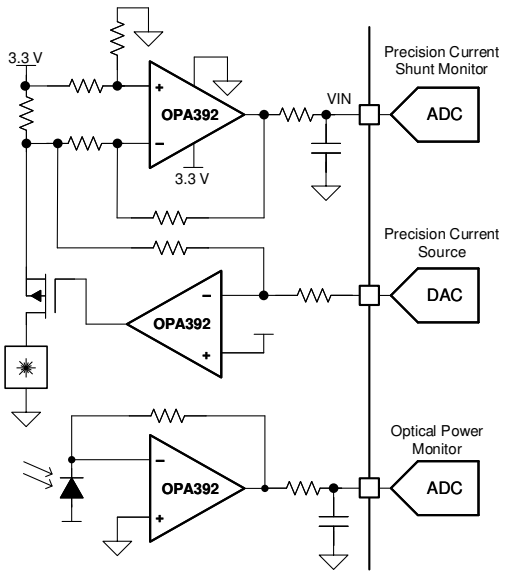
OPAx392 Precision, Low-Offset-Voltage, Low-Noise, Low-Input-Bias-Current, Rail-to-Rail I/O, e-trim™ Operational Amplifiers

1 Features

- Low offset voltage: ±10 µV (maximum)
- Low-drift: ±0.18 µV/°C
- Low input bias current: 10 fA
- Low noise: 4.4 nV/√Hz at 10 kHz
- Low 1/f noise: 2 μV_{PP} (0.1 Hz to 10 Hz)
- Low supply voltage operation: 1.7 V to 5.5 V
- Low quiescent current: 1.22 mA
- Fast settling: 0.75 µs (1 V to 0.1%)
- Fast slew rate: 4.5 V/µs
- High output current: +65/–55-mA short circuit
- Gain bandwidth: 13 MHz
- Rail-to-rail input and output
- Specified temperature range: –40°C to +125°C
- EMI and RFI filtered inputs

2 Applications

- Multiparameter patient monitor
- Electrocardiogram (ECG)
- Chemistry and gas analyzer
- Optical module
- Analog input module
- Process analytics (pH, gas, concentration, force and humidity)
- Gas detector
- Analog security camera
- Merchant DC/DC
- Pulse oximeter
- Inter-DC interconnect (long-haul, submarine)
- Data acquisition (DAQ)



OPAx392 Applications in Optical Modules

3 Description

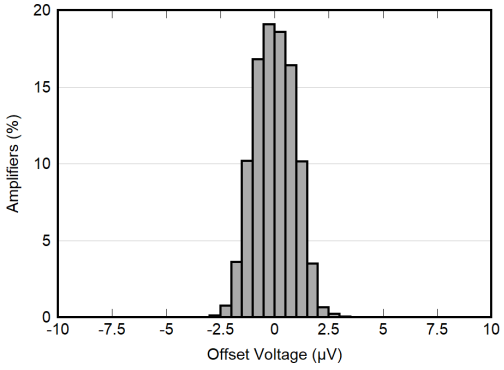
The OPAx392 family of operational amplifiers (OPA392, OPA2392, and OPA4392) features ultra-low offset, offset drift, and input bias current with rail-to-rail input and output operation. In addition to precision dc accuracy, the ac performance is optimized for low noise and fast-settling transient response. These features make the OPAx392 an excellent choice for driving high-precision analog-to-digital converters (ADCs) or buffering the output of high-resolution, digital-to-analog converters (DACs).

The OPAx392 feature TI's e-trim™ operational amplifier technology to achieve ultra-low offset voltage and offset voltage drift without any input chopping or auto-zero techniques. This technique enables ultra-low input bias current for sensor inputs or photodiode current-to-voltage measurements, creating high-performance transimpedance stages for optical modules or medical instrumentation.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA392	Single	DBV (SOT-23, 5)
	Single	DCK (SC70, 5)(3)
	Single	YBJ (DSBGA, 6)(3)
OPA2392(2)	Dual	D (SOIC, 8)(3)
	Dual	DGK (VSSOP, 8)(3)
	Dual	YBJ (DSBGA, 9)(3)
OPA4392(2)	Quad	PW (TSSOP, 14)(3)
	Quad	RTE (WQFN, 16)(3)

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) Device is preview.
(3) Package is preview.



OPAx392 Input Offset Voltage Distribution

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2021) to Revision C (July 2022)	Page
• Changed OPA2392 device to advanced information (preview)	1
• Changed Figure 6-9 Y-axis scales for clarity	10

Changes from Revision A (August 2021) to Revision B (October 2021)	Page
• Added footnote to all MIN/MAX over-temperature specifications	8
• Added footnote to input bias current and input offset current room temperature specification	8
• Added Figures 6-4, 6-5, and 6-6, *Offset Voltage vs Common-Mode Voltage*	10
• Changed Figure 6-9, *Open-Loop Gain and Phase vs Frequency*, to correct data	10
• Changed Figure 6-10, *Closed-Loop Gain and Phase vs Frequency*, to correct data	10
• Added Figure 6-14, *Input Bias Current vs Temperature*	10
• Changed Figure 6-23, *THD+N Ratio vs Frequency* to correct data	10

Changes from Revision * (January 2021) to Revision A (August 2021)	Page
• Changed OPA392 device in DBV (SOT-23-5) package from advanced information (preview) to production data (active)	1

5 Device Comparison Table

DEVICE	CHANNELS	SHUTDOWN	PACKAGE
OPA392	Single	No	DBV (SOT-23, 5)
		No	DCK (SC70, 5)
		Yes	YBJ (DSBGA, 6)
OPA2392 (preview)	Dual	No	D (SOIC, 8)
		No	DGK (VSSOP, 8)
		Yes	YBJ (DSBGA, 9)
OPA4392 (preview)	Quad	No	PW (TSSOP, 14)
		Yes	RTE (WQFN, 16)

6 Pin Configuration and Functions

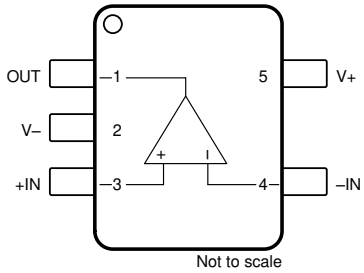


Figure 6-1. OPA392 DBV Package (5-Pin SOT-23), Top View

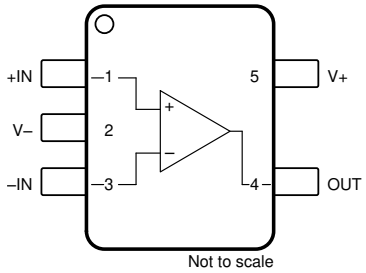


Figure 6-2. OPA392 DCK Package (5-Pin SC70, Preview), Top View

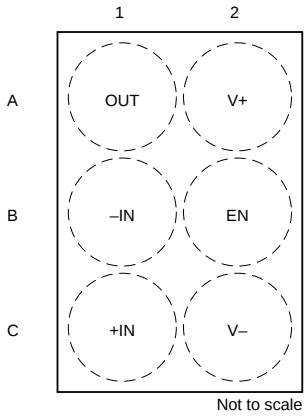


Figure 6-3. OPA392 YBJ Package (6-Pin DSBGA, Preview), Top View

Table 6-1. Pin Functions: OPA392

PIN				TYPE	DESCRIPTION
NAME	NO.				
	DBV (SOT-23)	DCK (SC70)	YBJ (DSBGA)		
EN	—	—	B2	Input	Enable pin. High = amplifier enabled.
–IN	4	3	B1	Input	Inverting input
+IN	3	1	C1	Input	Noninverting input
OUT	1	4	A1	Output	Output
V–	2	2	C2	Power	Negative (lowest) power supply
V+	5	5	A2	Power	Positive (highest) power supply

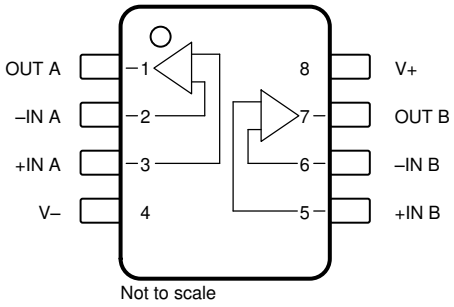


Figure 6-4. OPA2392 D (8-Pin SOIC, Preview) and DGK (8-Pin VSSOP, Preview) Packages, Top View

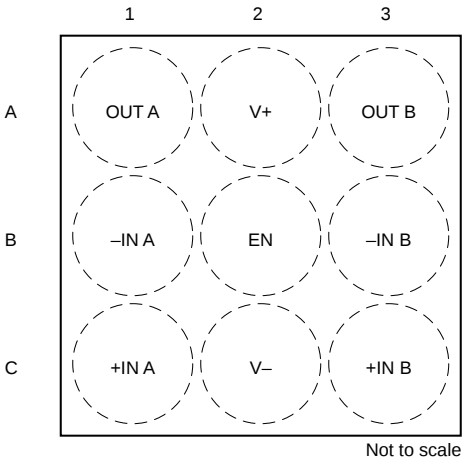


Figure 6-5. OPA2392 YBJ (9-Pin DSBGA, Preview) Package, Top View

Table 6-2. Pin Functions: OPA2392

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	YBJ (DSBGA)		
EN	—	B2	Input	Enable pin. High = both amplifiers enabled.
–IN A	2	B1	Input	Inverting input, channel A
+IN A	3	C1	Input	Noninverting input, channel A
–IN B	6	B3	Input	Inverting input, channel B
+IN B	5	C3	Input	Noninverting input, channel B
OUT A	1	A1	Output	Output, channel A
OUT B	7	A3	Output	Output, channel B
V–	4	C2	Power	Negative (lowest) power supply
V+	8	A2	Power	Positive (highest) power supply

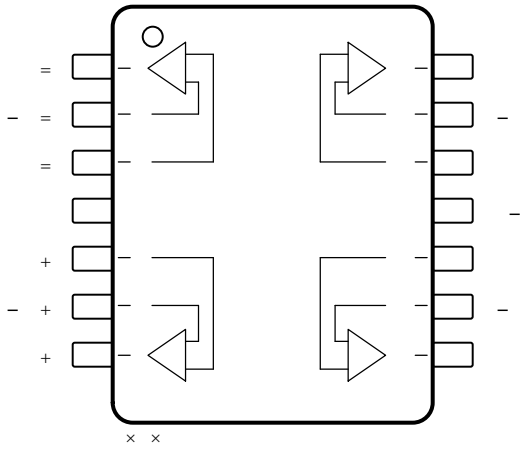


Figure 6-6. OPA4392 PW (14-Pin TSSOP, Preview) Package, Top View

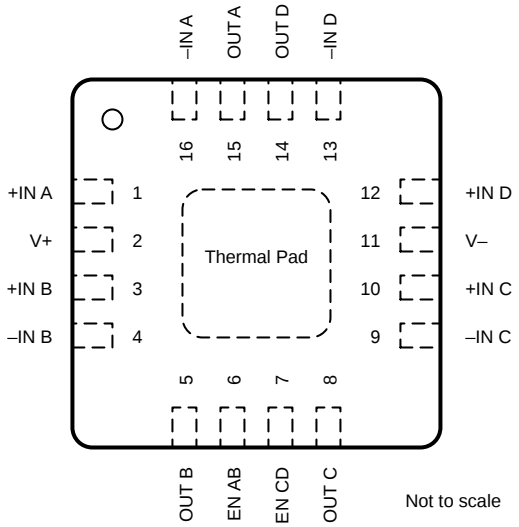


Figure 6-7. OPA4392 RTE (16-Pin WQFN, Preview) Package, Top View

Table 6-3. Pin Functions: OPA4392

PIN			TYPE	DESCRIPTION
NAME	NO.			
	PW (TSSOP)	RTE (WQFN)		
EN AB	—	6	Input	Enable pin for A and B amplifiers. High = amplifiers A and B are enabled.
EN CD	—	7	Input	Enable pin for C and D amplifiers. High = amplifiers C and D are enabled.
–IN A	2	16	Input	Inverting input, channel A
+IN A	3	1	Input	Noninverting input, channel A
–IN B	6	4	Input	Inverting input, channel B
+IN B	5	3	Input	Noninverting input, channel B
–IN C	9	9	Input	Inverting input, channel C
+IN C	10	10	Input	Noninverting input, channel C
–IN D	13	13	Input	Inverting input, channel D
+IN D	12	12	Input	Noninverting input, channel D
OUT A	1	15	Output	Output, channel A
OUT B	7	5	Output	Output, channel B
OUT C	8	8	Output	Output, channel C
OUT D	14	14	Output	Output, channel D
Thermal Pad	—	Thermal Pad	Power	Connect thermal pad to V–
V–	11	11	Power	Negative (lowest) power supply
V+	4	2	Power	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Input voltage, all pins	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Input current, all pins			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply	1.7		5.5	V
		Dual-supply	±0.85		±2.75	
T_A	Specified temperature		–40		125	°C

7.4 Thermal Information: OPA392

THERMAL METRIC[1]		OPA392 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2392

THERMAL METRIC[1]		OPA2392 YBJ (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

at T_A = 25°C, V_S = 1.7 V to 5.5 V (single-supply) or V_S = ±0.85 V to ±2.75 V (dual-supply), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5.0 V			±1	±10	µV
			V_{CM} = (V+) – 200 mV		±2	±30	
			T_A = –40°C to +125°C(1)			±100	
		V_{CM} = (V–), T_A = –40°C to 125°C(1)				±125	
dV_{OS}/dT	Input offset voltage drift	V_S = 5.0 V	T_A = 0°C to 85°C		±0.16		µV/°C
			T_A = –40°C to +125°C(1)			±0.6	
			V_{CM} = 5.0 V, T_A = –40°C to +125°C(1)		±0.18	±0.9	
PSRR	Power supply rejection ratio	V_{CM} = (V–)				±30	µV/V
			T_A = –40°C to +125°C(1)			±80	
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±0.01	±0.8	pA
		T_A = –40°C to +85°C				±5	
		T_A = –40°C to +125°C				±30	
I_{OS}	Input offset current(1)				±0.01	±0.8	pA
		T_A = –40°C to +85°C				±5	
		T_A = –40°C to +125°C				±30	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			2.0		$µV_{PP}$
			V_{CM} = (V+) – 0.3		3.2		
e_N	Input voltage noise density	f = 10 Hz			42		$nV/\sqrt{Hz}$
			V_{CM} = (V+) – 0.3		80		
		f = 1 kHz			6.5		
			V_{CM} = (V+) – 0.3		10.4		
		f = 10 kHz			4.4		
			V_{CM} = (V+) – 0.3		5.8		
i_N	Input current noise density	f = 1 kHz	OPA392		70		$fA/\sqrt{Hz}$
			OPA2392		25		
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V		75	120		dB
			T_A = –40°C to +125°C		113		
		(V–) < V_{CM} < (V+), T_A = –40°C to +125°C(1)		66	97		
			V_S = 5.5 V	88	111		
INPUT CAPACITANCE							
Z_{ID}	Differential				10^{13} || 2.8		Ω || pF
Z_{ICM}	Common-mode				10^{13} || 3.5		Ω || pF

7.6 Electrical Characteristics (continued)

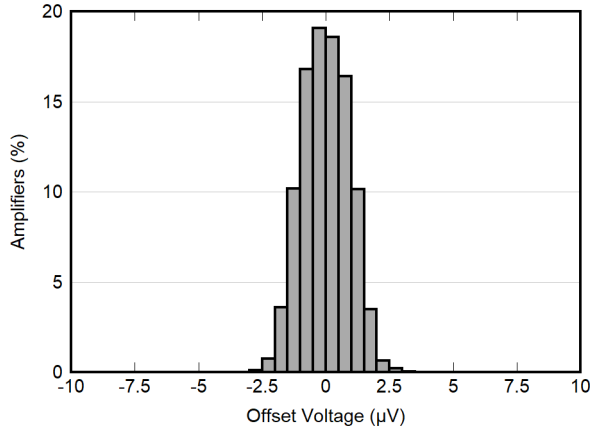
at T_A = 25°C, V_S = 1.7 V to 5.5 V (single-supply) or V_S = ±0.85 V to ±2.75 V (dual-supply), R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5 V	(V–) + 50 mV < V_{OUT} < (V+) – 50 mV	115	132		dB
			(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ	110	128		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, T_A = –40°C to +125°C(1)	100			
		V_S = 1.7 V	(V–) + 50 mV < V_{OUT} < (V+) – 50 mV, V_{CM} = (V+) – 1.15 V	106	124		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, V_{CM} = (V+) – 1.15 V	106	124		
			(V–) + 100 mV < V_{OUT} < (V+) – 100 mV, R_L = 2 kΩ, V_{CM} = (V+) – 1.15 V, T_A = –40°C to +125°C(1)	100			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	A_V = 1000 V/V			13		MHz
SR	Slew rate	4-V step, gain = +1	falling		4.5		V/µs
			rising		3.5		
	Phase margin	C_L = 100 pF			45		°
t_S	Settling time	To 0.1%, 2-V step, gain = +1			0.75		µs
		To 0.01%, 2-V step, gain = +1			1		
	Overload recovery time	V_{IN} × gain > V_S			0.45		µs
THD+N	Total harmonic distortion + noise	V_{OUT} = 1 V_{RMS}, gain = +1, f = 1 kHz, V_{CM} = (V–) + 1.5 V			–112		dB
					0.00025		%
OUTPUT							
	Voltage output swing from both rails	V_S = 1.7 V				20	mV
			R_L = 2 kΩ			30	
		V_S = 5.5 V				20	
			R_L = 2 kΩ			35	
I_{SC}	Short-circuit current	Sinking, V_S = 5.5 V			–55		mA
		Sourcing, V_S = 5.5 V			65		
R_O	Open-loop output impedance	f = 1 MHz			120		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 mA			1.22	1.4	mA
			T_A = –40°C to +125°C(1)			1.5	
SHUTDOWN (YBJ and RTE Packages Only)							
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, EN = (V–)			6		µA
V_{IH}	High-level input voltage	Amplifier enabled		(V+) – 0.5			V
V_{IL}	Low-level input voltage	Amplifier disabled				(V–) + 0.5	V
t_{ON}	Amplifier enable time	G = 1, V_{OUT} = 0.9 × V_S/2, two amplifiers enabled			9.5		µs
t_{OFF}	Amplifier disable time	G = 1, V_{OUT} = 0.1 × V_S/2, two amplifiers disabled			7.8		µs

(1) Specification established from device population bench system measurements across multiple lots.

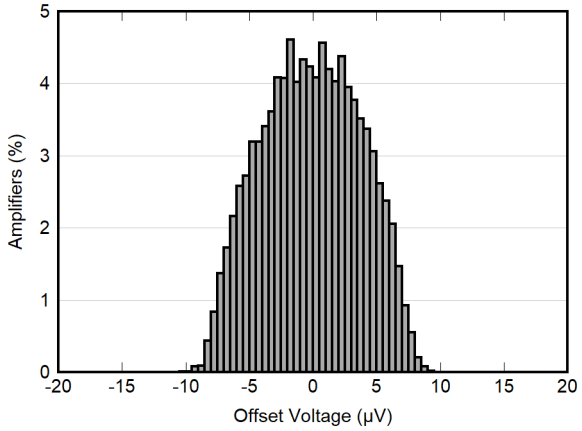
7.7 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



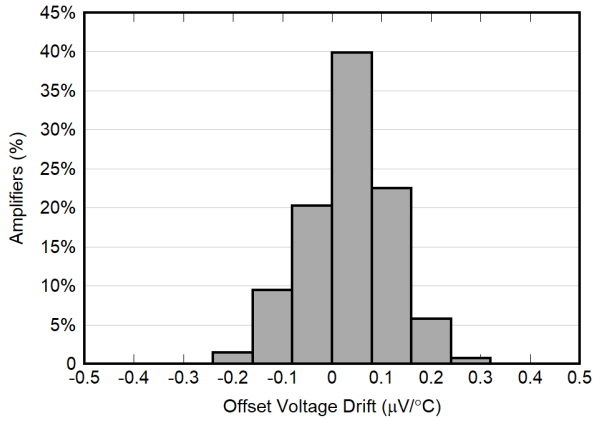
V_S = 5.0 V

Figure 7-1. Offset Voltage Distribution



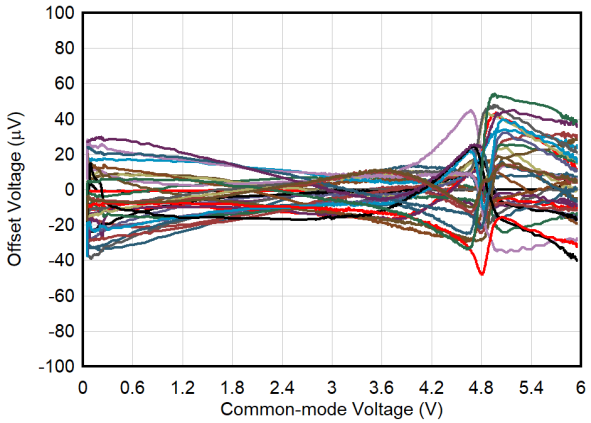
V_S = 5.0 V, V_{CM} = 4.8 V

Figure 7-2. Offset Voltage Distribution



V_S = 5.0 V

Figure 7-3. Offset Voltage Distribution



T_A = –40°C

Figure 7-4. Offset Voltage vs Common-Mode Voltage

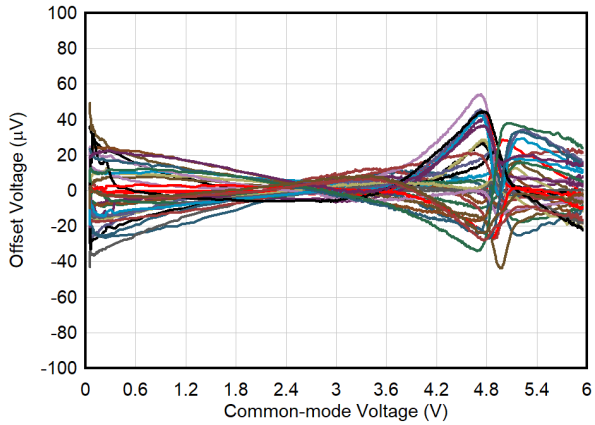
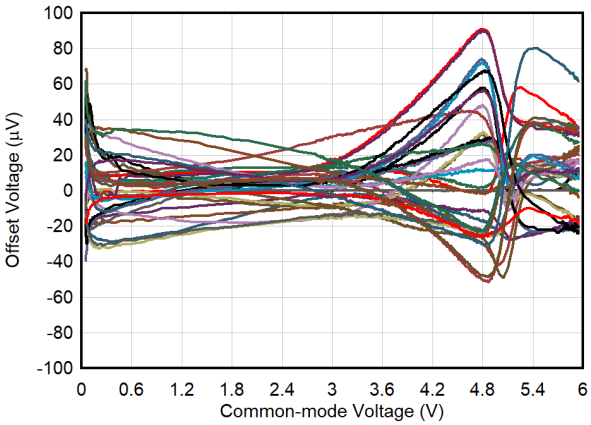


Figure 7-5. Offset Voltage vs Common-Mode Voltage



T_A = +125°C

Figure 7-6. Offset Voltage vs Common-Mode Voltage

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

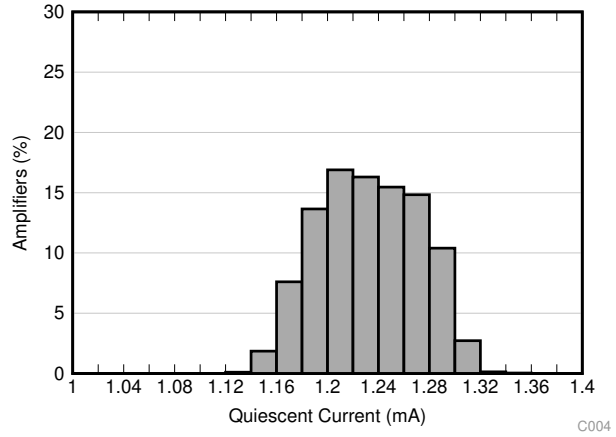
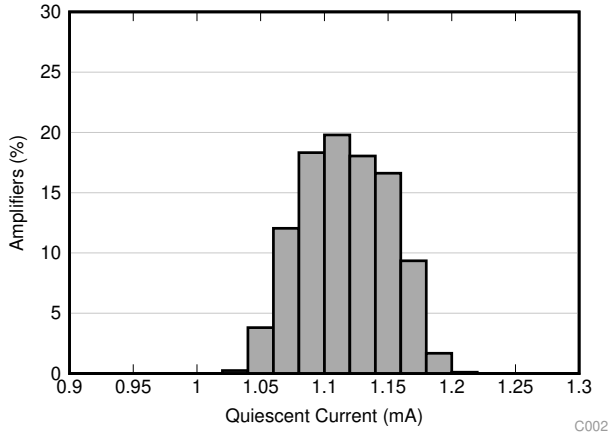


Figure 7-7. Quiescent Current Distribution



V_S = 1.7 V

Figure 7-8. Quiescent Current Distribution

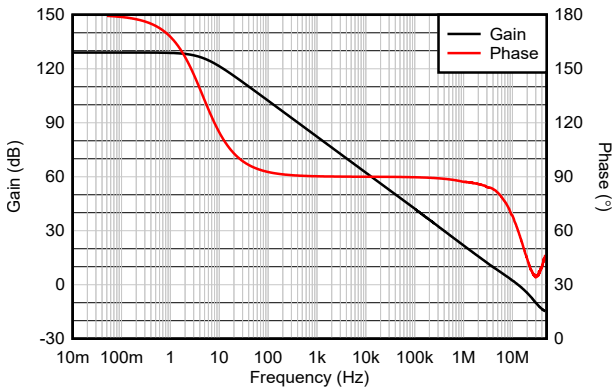


Figure 7-9. Open-Loop Gain and Phase vs Frequency

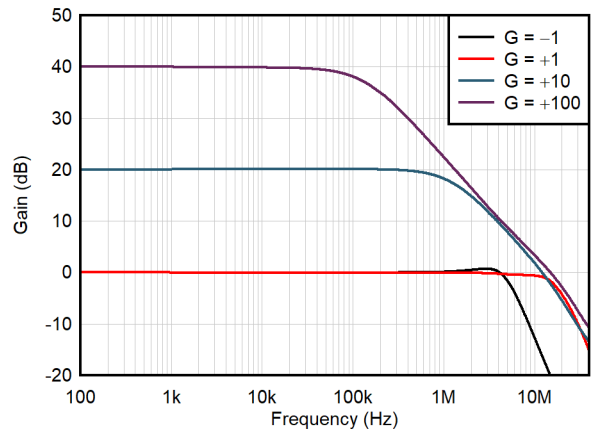
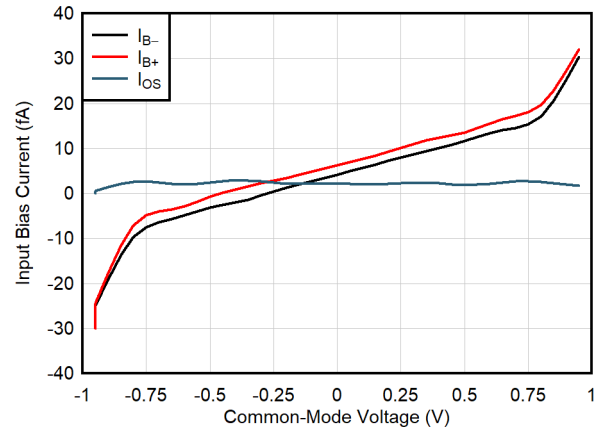
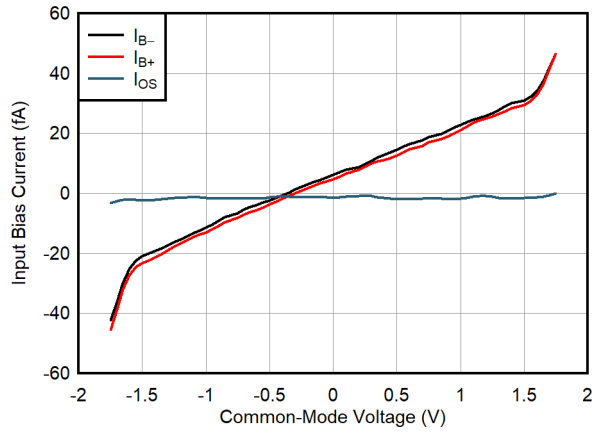


Figure 7-10. Closed-Loop Gain vs Frequency



V_S = 1.7 V

Figure 7-11. Input Bias Current vs Common-Mode Voltage



V_S = 3.3 V

Figure 7-12. Input Bias Current vs Common-Mode Voltage

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

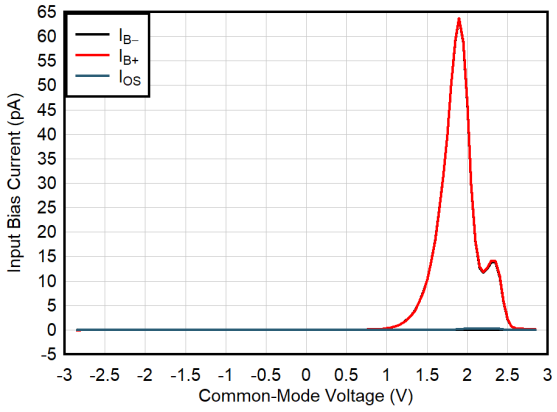


Figure 7-13. Input Bias Current vs Common-Mode Voltage

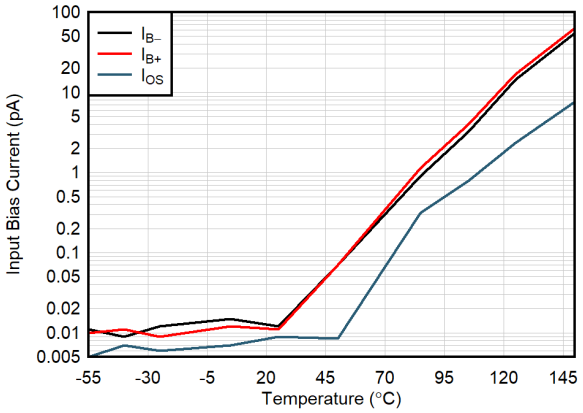


Figure 7-14. Input Bias Current vs Temperature

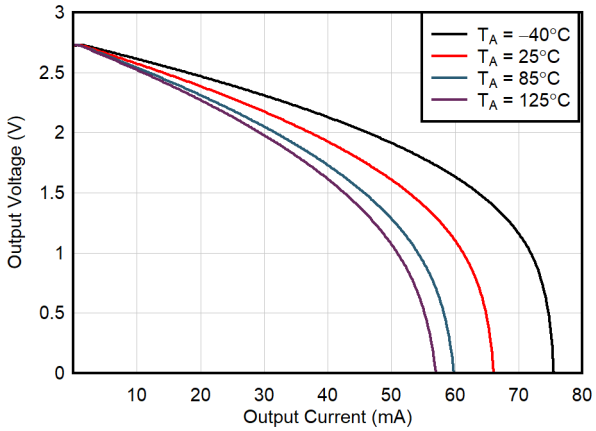


Figure 7-15. Output Voltage Swing vs Output Current (Sourcing)

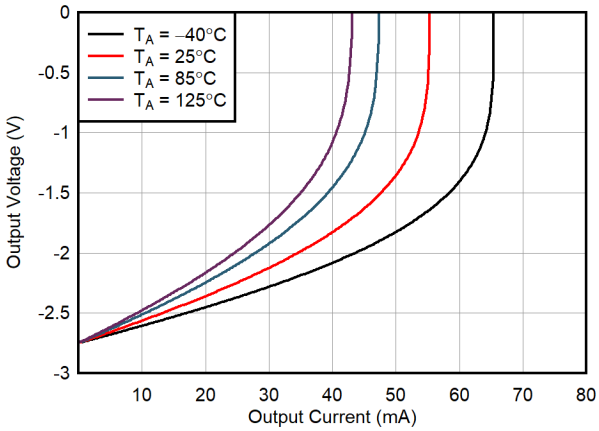
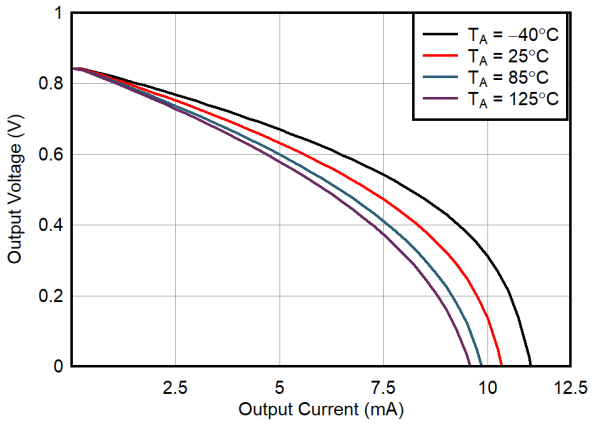
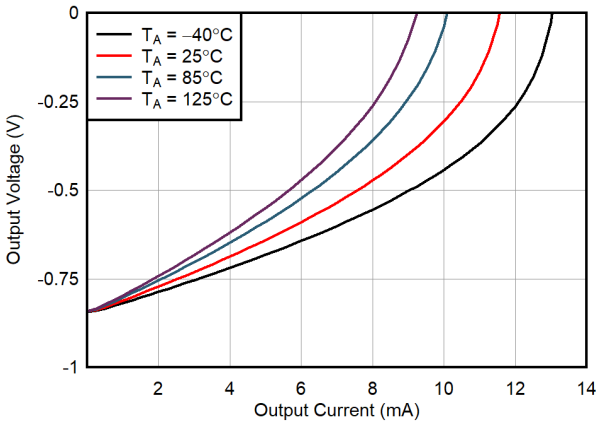


Figure 7-16. Output Voltage Swing vs Output Current (Sinking)



V_S = ±0.85 V

Figure 7-17. Output Voltage Swing vs Output Current (Sourcing)



V_S = ±0.85 V

Figure 7-18. Output Voltage Swing vs Output Current (Sinking)

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

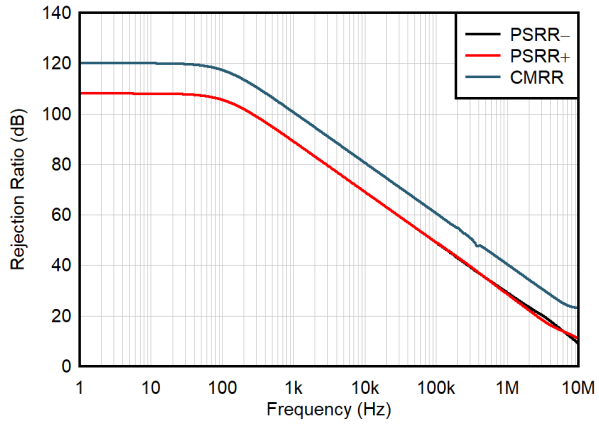
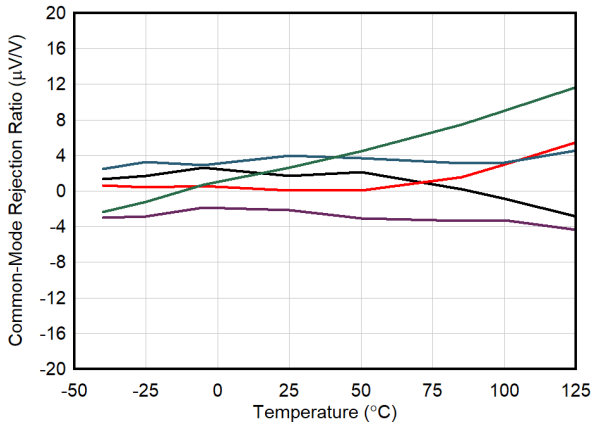
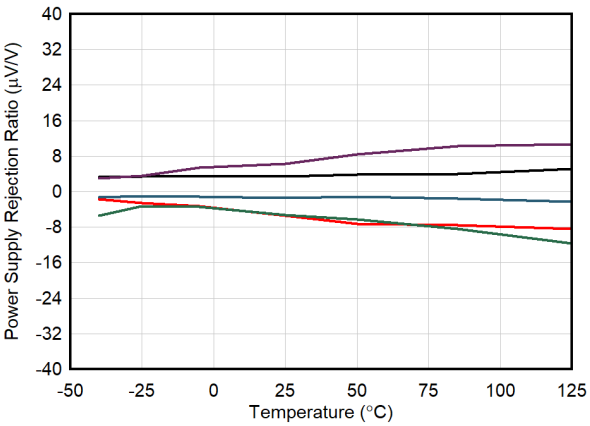


Figure 7-19. CMRR and PSRR vs Frequency



5 Units

Figure 7-20. CMRR vs Temperature



5 Units

Figure 7-21. PSRR vs Temperature

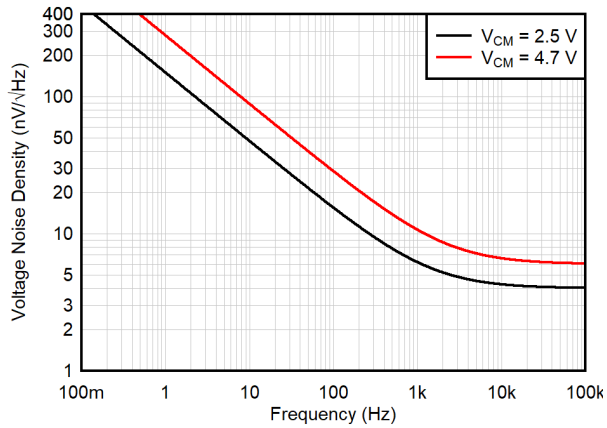
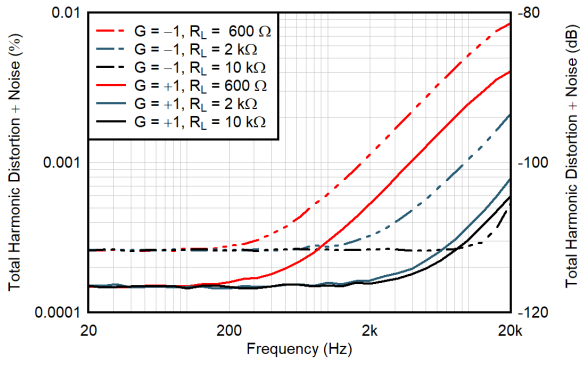
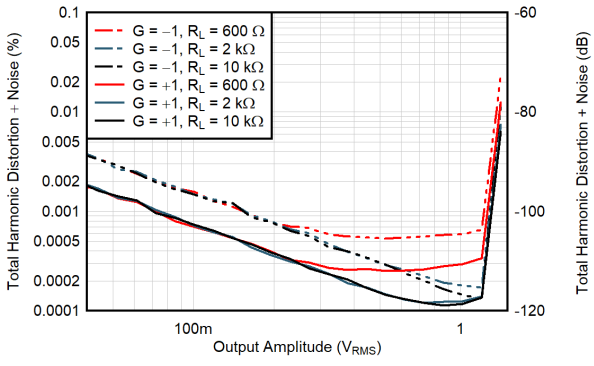


Figure 7-22. Voltage Noise vs Frequency



V_{OUT} = 1 V_{RMS}

Figure 7-23. THD+N Ratio vs Frequency



f = 1 kHz

Figure 7-24. THD+N vs Output Amplitude

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

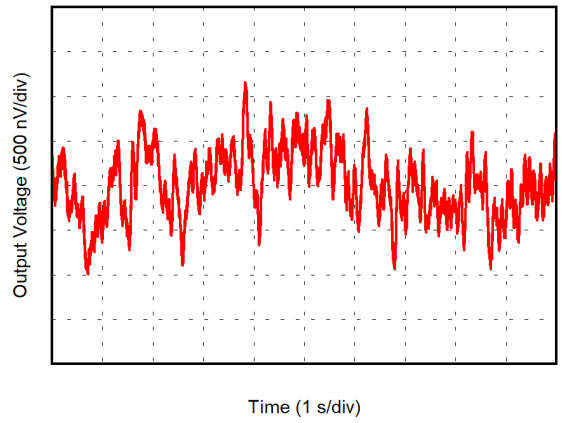


Figure 7-25. 0.1-Hz to 10-Hz Noise

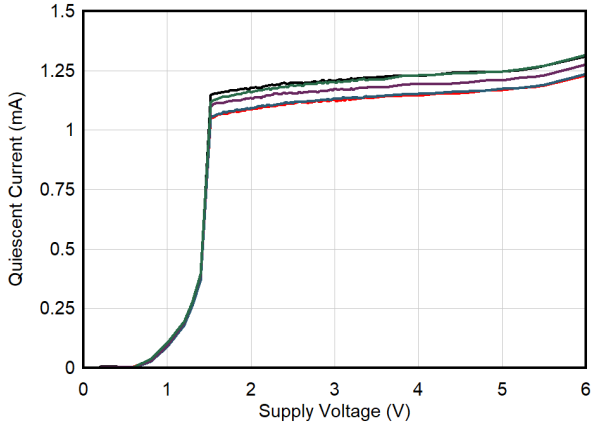


Figure 7-26. Quiescent Current vs Supply Voltage

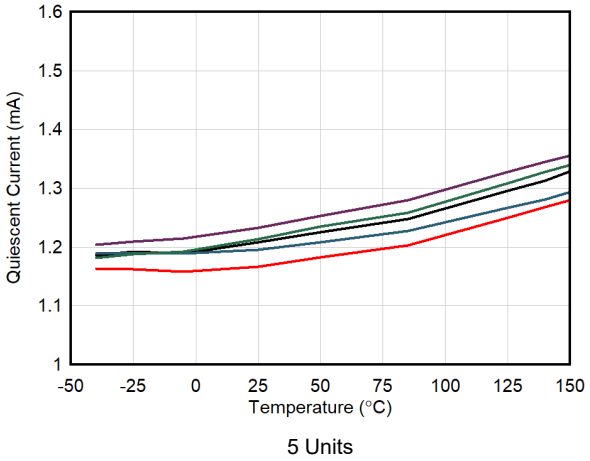


Figure 7-27. Quiescent Current vs Temperature

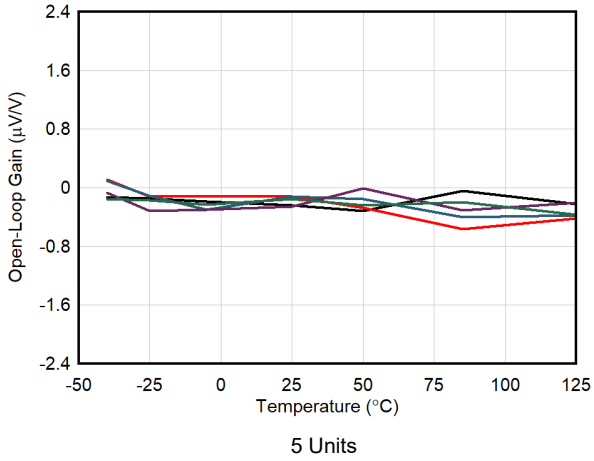


Figure 7-28. Open-Loop Gain vs Temperature

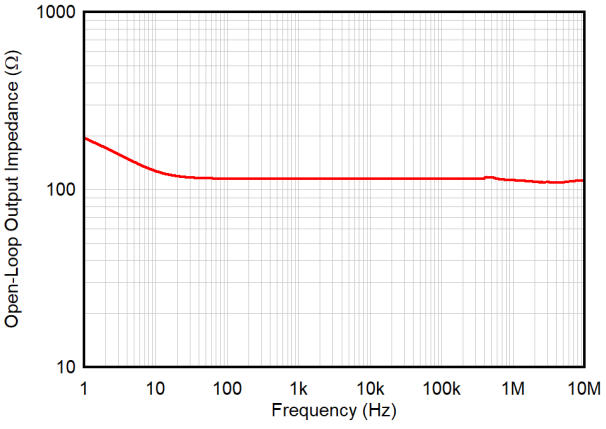


Figure 7-29. Open-Loop Output Impedance vs Frequency

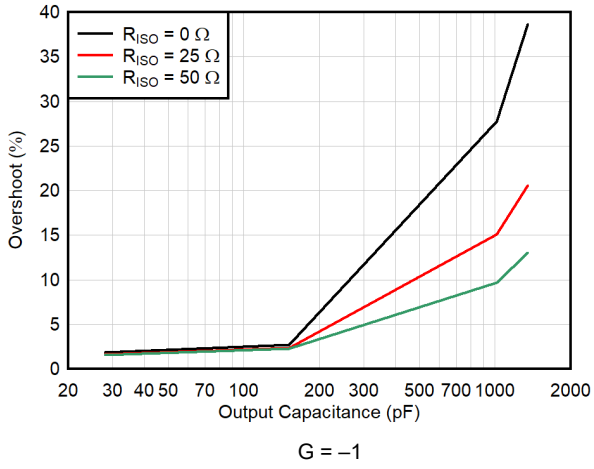
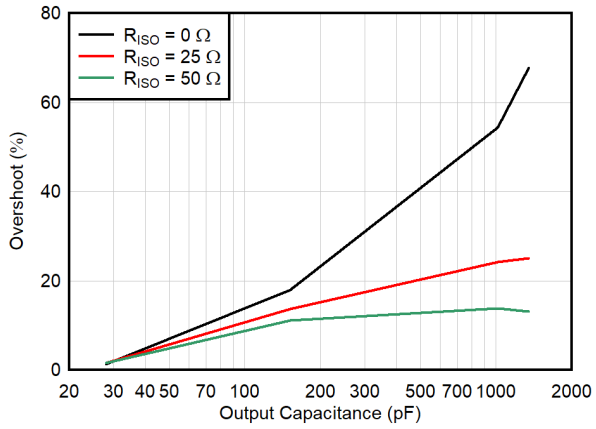


Figure 7-30. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = 1

Figure 7-31. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

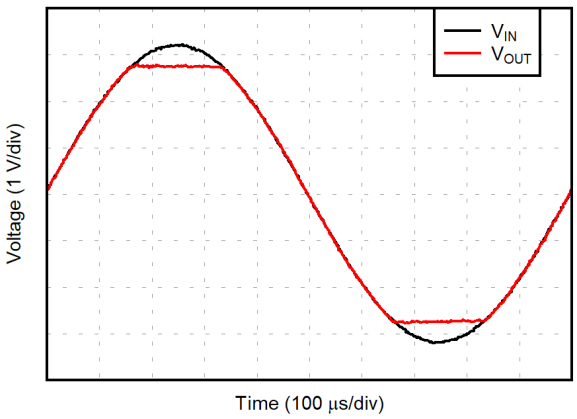


Figure 7-32. No Phase Reversal

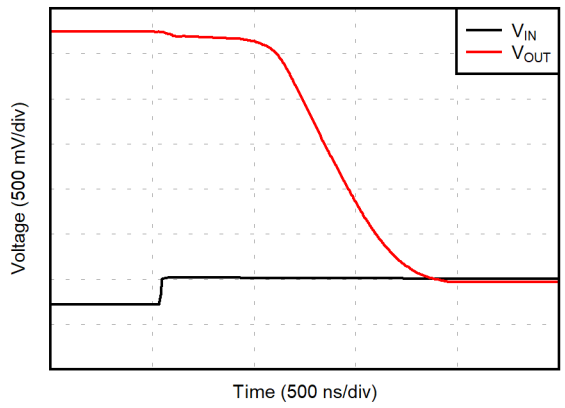


Figure 7-33. Positive Overload Recovery

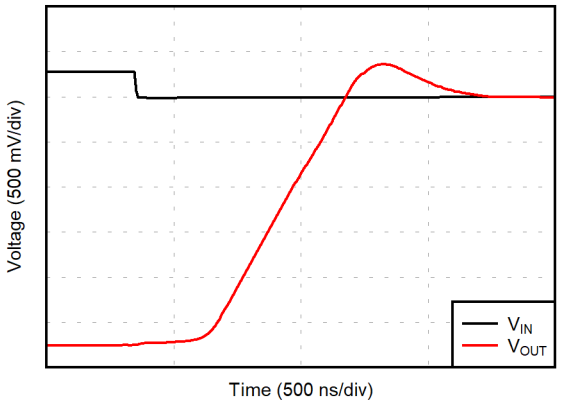
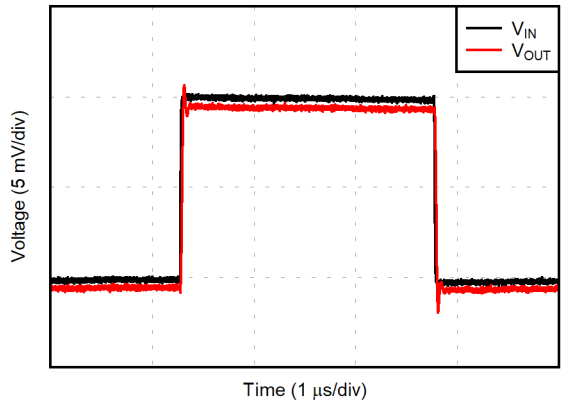
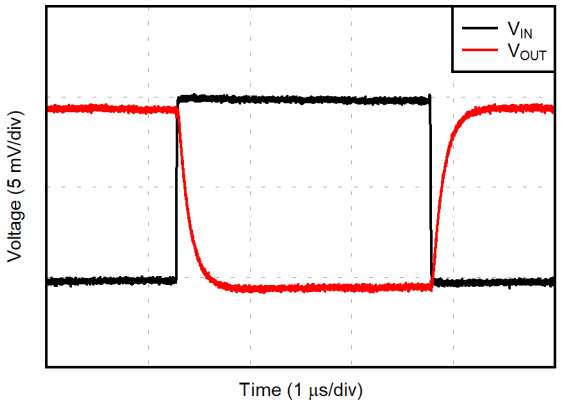


Figure 7-34. Negative Overload Recovery



G = 1

Figure 7-35. Small-Signal Step Response (10-mV Step)

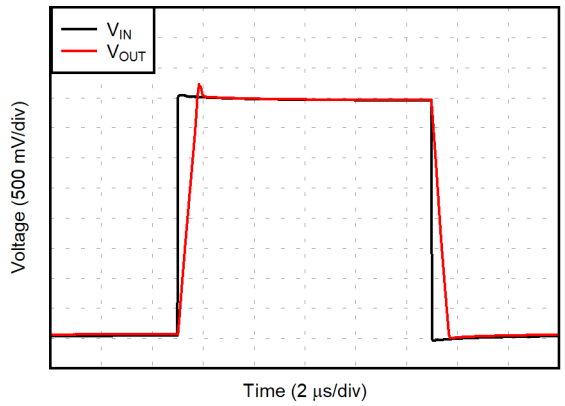


G = –1

Figure 7-36. Small-Signal Step Response (10-mV Step)

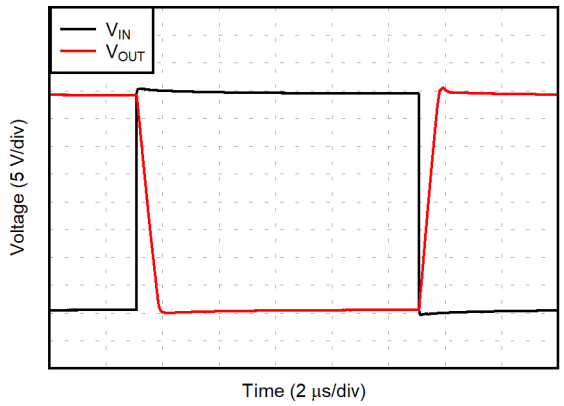
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = 1

Figure 7-37. Large-Signal Step Response (4-V Step)



G = –1

Figure 7-38. Large-Signal Step Response (4-V Step)

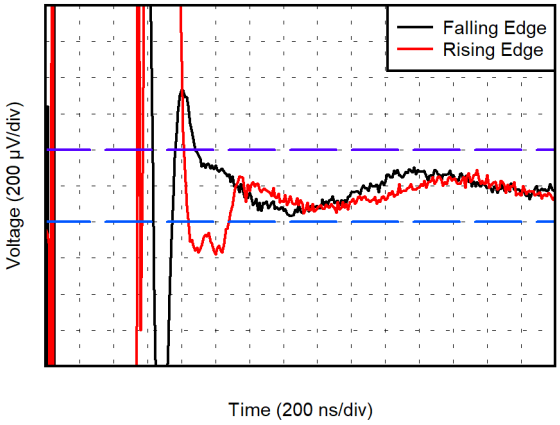
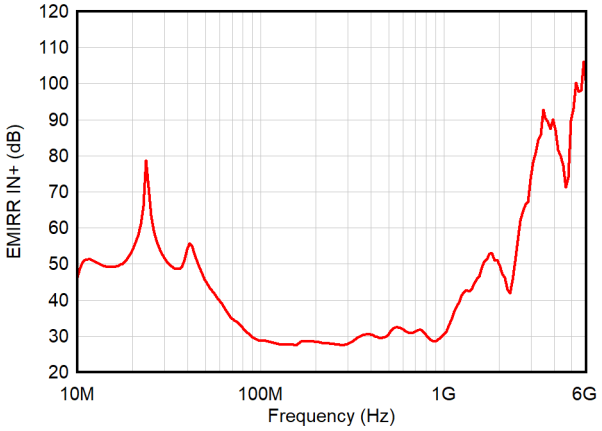


Figure 7-39. Settling Time



P_{RF} = –10 dBm

Figure 7-40. EMIRR vs Frequency

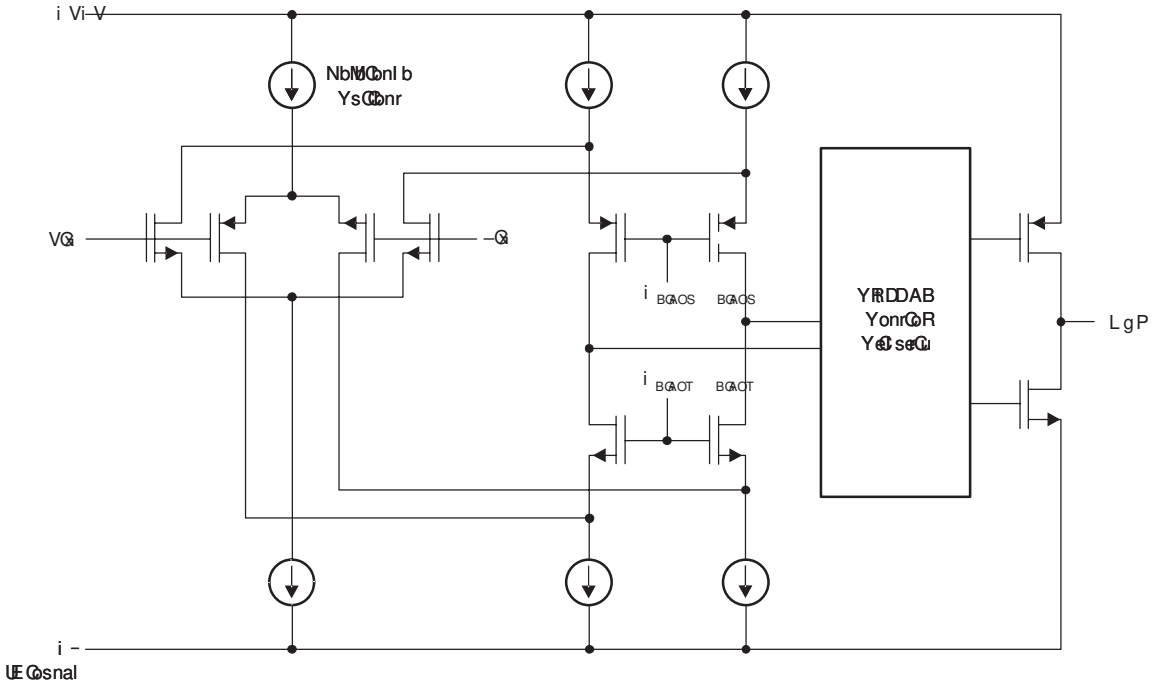
8 Detailed Description

8.1 Overview

The OPAx392 is a family of low offset, low-noise e-trim operational amplifiers (op amps) that uses a proprietary offset trim technique. These op amps offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx392 operate from 1.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve extremely low input bias current, wide input and output voltage ranges, high loop gain, and low, flat output impedance in small package options. The OPAx392 strengths also include 13-MHz bandwidth, 4.4-nV/$\sqrt{\text{Hz}}$ noise spectral density, and low 1/f noise. These features make the OPAx392 an exceptional choice for interfacing with sensors, photodiodes, and high-performance analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Operating Voltage

The OPAx392 family can be used with single or dual supplies from an operating range of V_S = 1.7 V (±0.85 V) up to 5.5 V (±2.75 V). The offset voltage is trimmed at 5.0 V, however, the device maintains ultra-low offset voltages down to V_S = 1.7 V.

Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics*.

8.3.2 Low Input Bias Current

The typical input bias current of the OPAx392 is extremely low (typically 10 fA). Input bias current is dominated by leakage current from the ESD protection diodes, which is proportional to the area of the diode. The OPAx392 is able to achieve ultra-low input bias current as a result of modern process technology and advanced electrostatic discharge (ESD) protection design that minimizes the area of the diode.

In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in the forward-biasing of the ESD cells. Figure 8-1 shows the equivalent circuit.

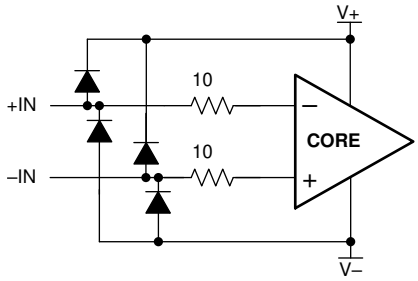


Figure 8-1. Equivalent Input Circuit

8.4 Device Functional Modes

The OPAx392 family is operational when the power-supply voltage is greater than 1.7 V (±0.85 V). For devices that use the EN function (see *Section 6*), the devices are disabled when the EN pin is low. In this state, quiescent current is significantly reduced, and the output is high impedance. The maximum specified power-supply voltage for the OPAx392 is 5.5 V (±2.75 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx392 is a unity-gain stable, precision operational amplifier family free from unexpected output and phase reversal. The use of proprietary e-trim operational amplifier technology gives the benefit of low input offset voltage over time and temperature, along with ultra-low input bias current. The OPAx392 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range to the supply rail, with low offset across the supply range, and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx392 precision amplifiers are designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

9.2 Typical Application

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA392 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 9-1 shows the schematic.

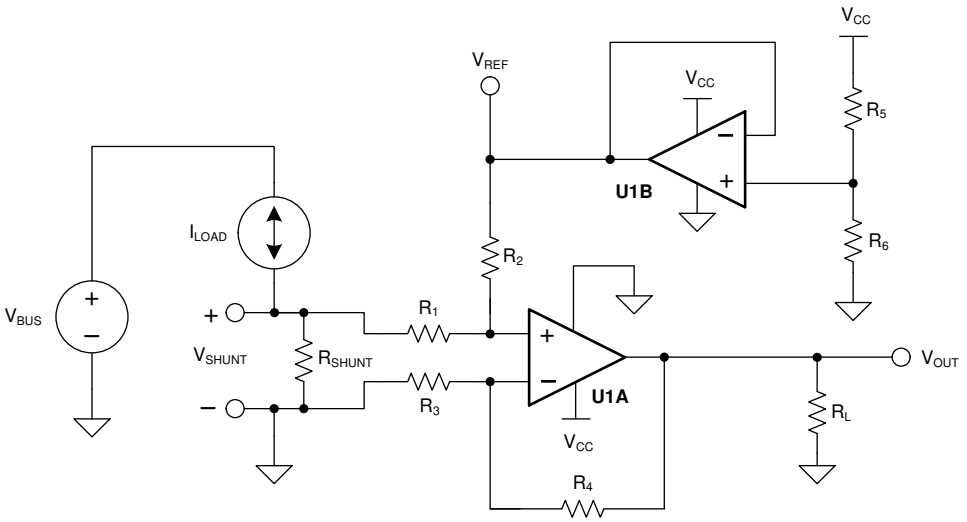


Figure 9-1. Bidirectional Current-Sensing Schematic

9.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to +1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

9.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor, R_{SHUNT}, to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

———— ———— Ω (2)

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% is selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to +100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA392, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPA392 has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% is selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA392 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA392 given a 3.3-V supply.

$$-100\ \text{mV} < V_{CM} < 3.4\ \text{V} \tag{3}$$

$$100\ \text{mV} < V_{OUT} < 3.2\ \text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5:

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ \text{V} - 100\ \text{mV}}{100\ \text{m}\Omega \times [1\ \text{A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 is 1 kΩ. 15.4 kΩ is selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors are selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

9.2.3 Application Curve

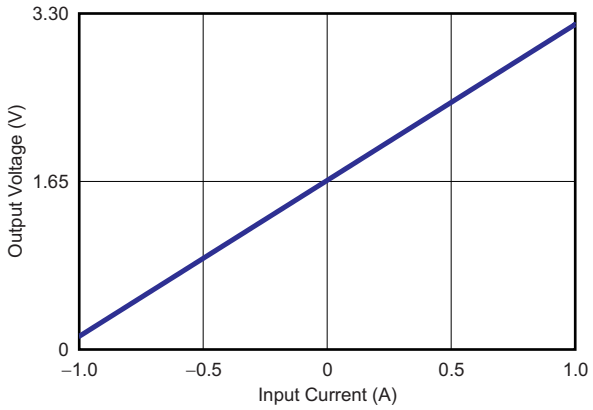


Figure 9-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

9.3 Power Supply Recommendations

The OPAx392 are specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V).

CAUTION

Exceeding supply voltages listed in the *Absolute Maximum Ratings* table can permanently damage the device.

9.4 Layout

9.4.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short, and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by making sure these potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Use guard traces to minimize leakage current when ultra-low bias current is required.
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

9.4.2 Layout Example

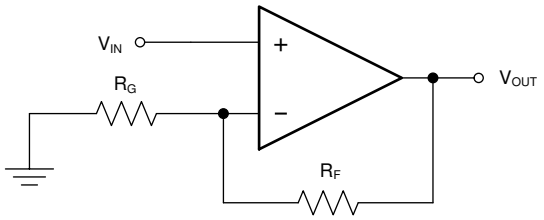


Figure 9-3. OPA392 Layout Schematic

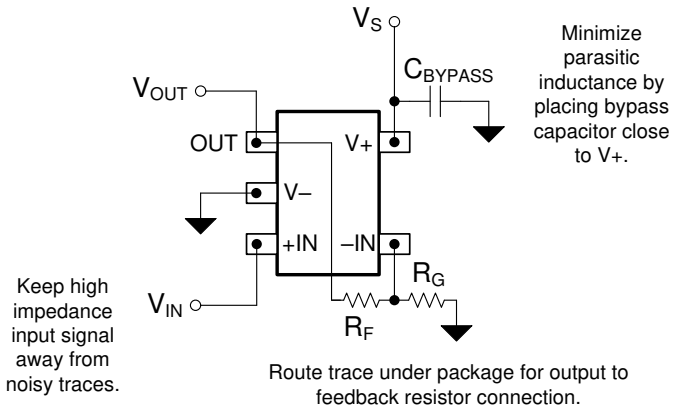


Figure 9-4. OPA392 Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

10.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Amplifier Input Common-Mode and Output-Swing Limitations* application note
- Texas Instruments, *Offset Correction Methods: Laser Trim, e-Trim™, and Chopper* application brief

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

e-trim™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA392DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23GT	Samples
OPA392DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23GT	Samples
XOPA2392YBJR	ACTIVE	DSBGA	YBJ	9	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

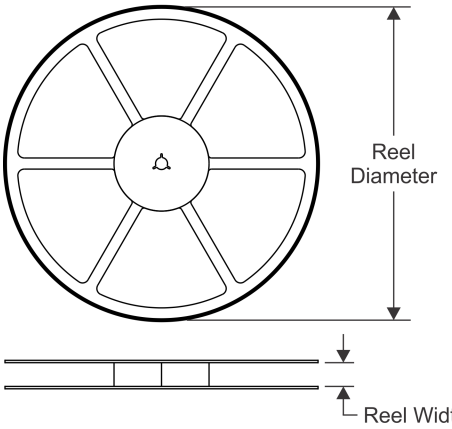
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

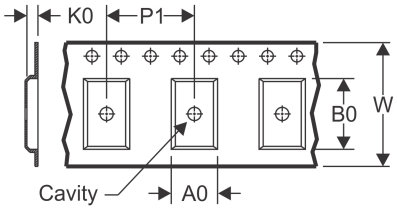
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

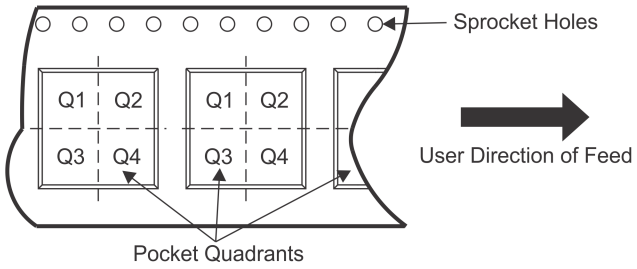


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

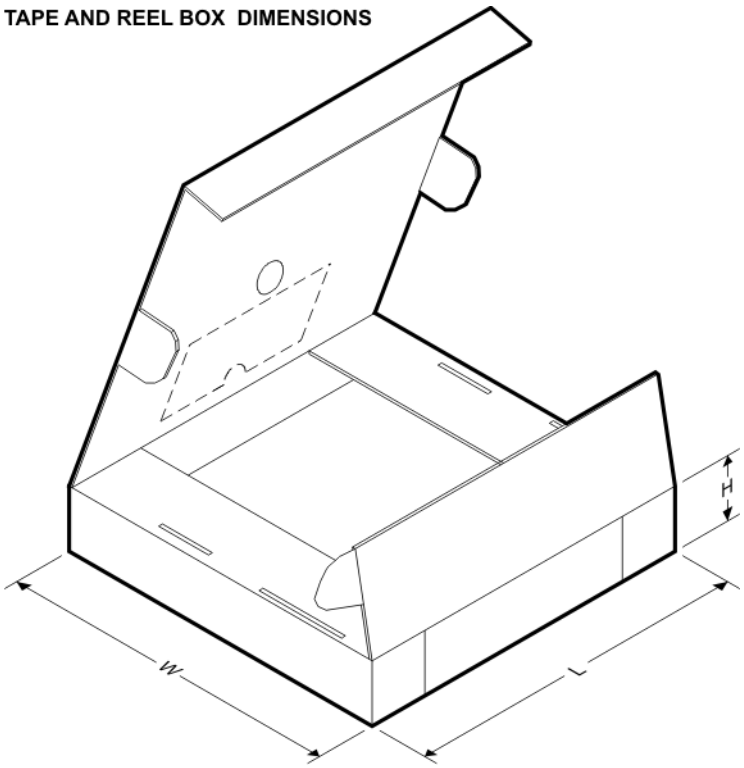
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA392DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA392DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

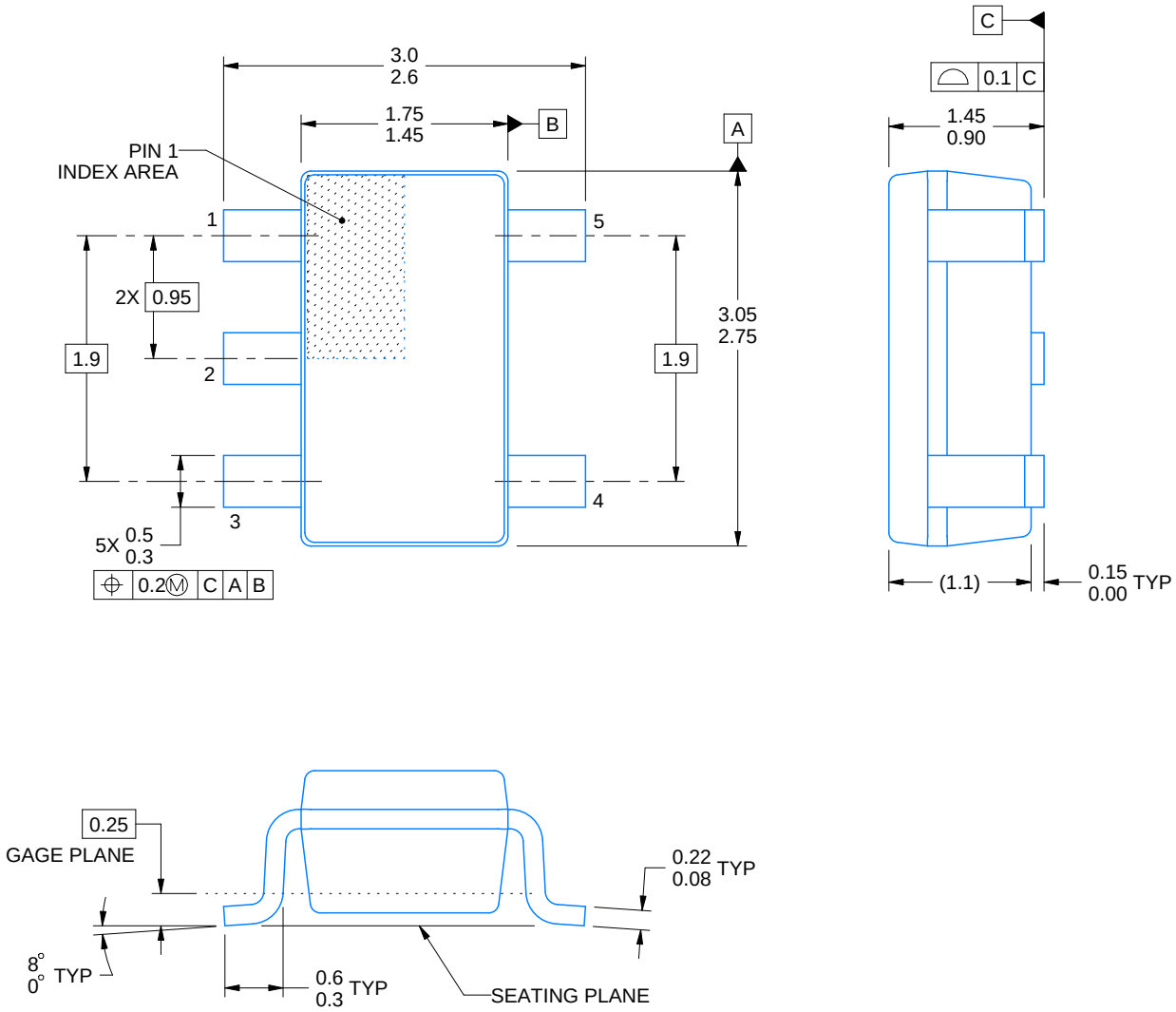
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA392DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA392DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

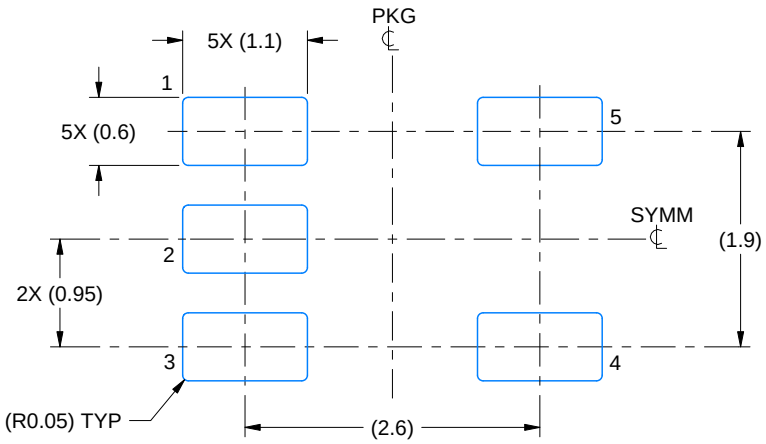
SMALL OUTLINE TRANSISTOR



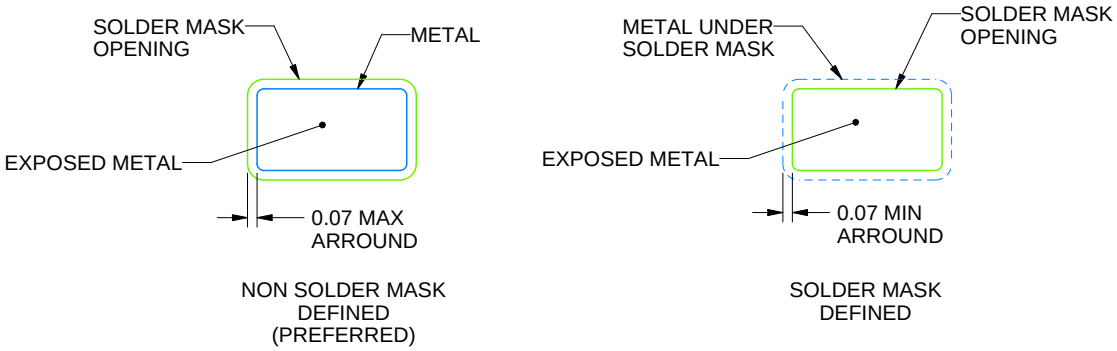
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

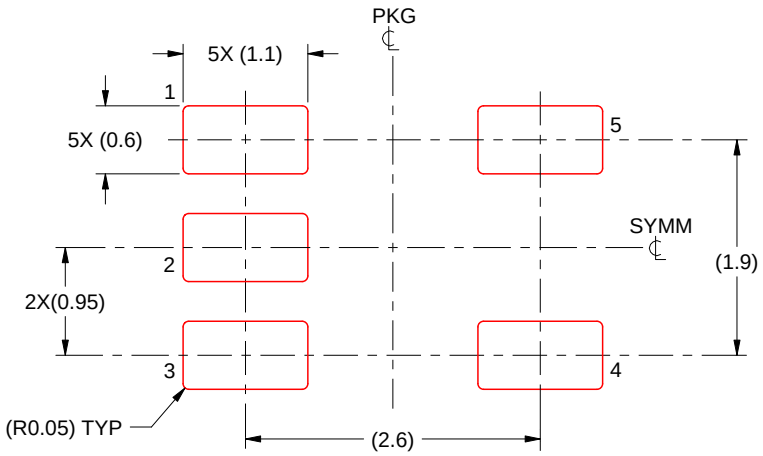


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS
PCM6120-Q1
SBASAH2A – APRIL 2022 – REVISED AUGUST 2022

PCM6120-Q1 2-Channel, 768-kHz, Burr-Brown™ Audio ADC

1 Features

- Multichannel high-performance ADC:
  - 2-channel analog microphones or line-in
  - 4-channel digital PDM microphones
  - Up to 2 analog and up to 2 digital microphone channels
- ADC line and microphone differential input performance:
  - Dynamic range (DR):
    - 123-dB, dynamic range enhancer (DRE) enabled
    - 113-dB, DRE disabled
  - THD+N: –95 dB
- ADC channel summing mode, DR performance:
  - 116-dB, DRE disabled, 2-channel summing
- ADC input voltage:
  - Differential, 2-V_{RMS} full-scale inputs
  - Single-ended, 1-V_{RMS} full-scale inputs
- ADC sample rate (f_S) = 8 kHz to 768 kHz
- Programmable channel settings:
  - Channel gain: 0 dB to 42 dB, 0.5-dB steps
  - Digital volume control: –100 dB to 27 dB
  - Gain calibration with 0.1-dB resolution
  - Phase calibration with 163-ns resolution
- Programmable microphone bias or supply voltage generation
- Low-latency signal processing filter selection
- Programmable HPF and biquad digital filters
- Automatic gain controller (AGC)
- Voice activity detection (VAD)
- I^2C control interface
- Integrated high-performance audio PLL
- Automatic clock divider setting configurations
- Audio serial data interface:
  - Format: TDM, I^2S, or left-justified (LJ)
  - Word length: 16 bits, 20 bits, 24 bits, or 32 bits
  - Master or slave interface
- Single-supply operation: 3.3 V or 1.8 V
- I/O-supply operation: 3.3 V or 1.8 V
- Power consumption for 1.8-V AVDD supply:
  - 9.5 mW/channel at 48-kHz sample rate

2 Applications

- Automotive Active Noise Cancellation
- Automotive Head Unit
- Rear Seat Entertainment
- Digital Cockpit Processing Unit
- Telematics Control Unit

3 Description

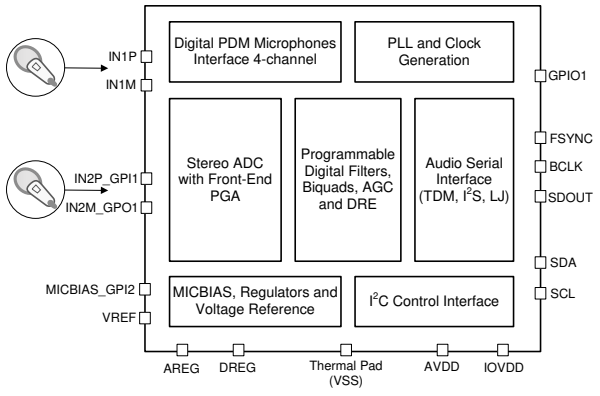
The PCM6120-Q1 is a Burr-Brown™ high-performance, audio analog-to-digital converter (ADC) that supports simultaneous sampling of up to two analog channels or four digital channels for the pulse density modulation (PDM) microphone input. The device supports line and microphone inputs, and allows for both single-ended and differential input configurations. The device integrates programmable channel gain, digital volume control, a programmable microphone bias voltage, a phase-locked loop (PLL), a programmable high-pass filter (HPF), biquad filters, low-latency filter modes, and allows for sample rates up to 768 kHz. The device supports time-division multiplexing (TDM), I^2S, or left-justified (LJ) audio formats, and can be controlled with the I^2C interface. These integrated high-performance features, along with the ability to be powered from a single-supply of 3.3 V or 1.8 V, make the device an excellent choice for space-constrained audio systems in far-field microphone recording applications.

The PCM6120-Q1 is specified from –40°C to +125°C, and is offered in a 20-pin WQFN package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
PCM6120-Q1	WQFN (20)	3.00 mm × 3.00 mm with 0.5-mm pitch

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (August 2022)	Page
• Changed document status from advanced information to production data	1

5 Device Comparison Table

FEATURE	PCM1821-Q1	PCM1820-Q1	PCM1822-Q1	PCM3120-Q1	PCM5120-Q1	PCM6120-Q1
Control interface	Pin control			I^2C		
Digital audio serial interface	TDM or I^2S			TDM or I^2S or left-justified (LJ)		
Audio analog channel	2					
Digital microphone channel	Not available			4		
Programmable MICBIAS voltage	N/A			Yes		
Dynamic range (DRE disabled)	106 dB	113 dB	111 dB	106 dB	108 dB	113 dB
Dynamic range (DRE enabled)	Not available	123 dB	117 dB	Not available	120 dB	123 dB
ADC SNR with DRE	N/A	123 dB	117 dB	N/A	120 dB	123 dB
Input Voltage	2 V_{rms}		1 V_{rms}	2 V_{rms}		
Input Type	Differential/Single-Ended	Differential	Differential/Single-Ended			
Input impedance	10 kΩ	2.5 kΩ		2.5 kΩ, 10 kΩ, 20 kΩ		
Compatibility	Pin-to-pin, package, drop-in replacements of each other			Pin-to-pin, package, and control registers compatible; drop-in replacements of each other		
Package	WQFN (RTE), 20-pin, 3.00 mm × 3.00 mm (0.5-mm pitch)					

6 Pin Configuration and Functions

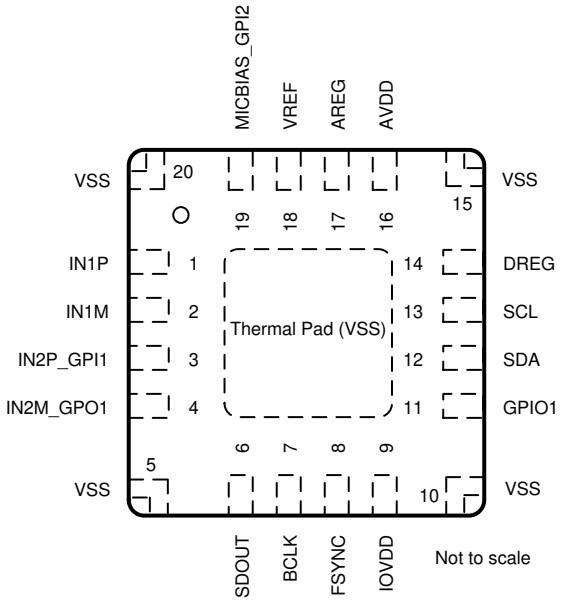


Figure 6-1. RTE Package, 20-Pin WQFN With Exposed Thermal Pad, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN1P	Analog input	Analog input 1P pin.
2	IN1M	Analog input	Analog input 1M pin.
3	IN2P_GPI1	Analog input/digital input	Analog input 2P pin or general-purpose digital input 1 (multipurpose functions such as digital microphones data, PLL input clock source, and so forth).
4	IN2M_GPO1	Analog input/digital output	Analog input 2M pin or general-purpose digital output 1 (multipurpose functions such as digital microphone clock, interrupt, and so forth).
5	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions.
6	SDOUT	Digital output	Audio serial data interface bus output.
7	BCLK	Digital I/O	Audio serial data interface bus bit clock.
8	FSYNC	Digital I/O	Audio serial data interface bus frame synchronization signal.
9	IOVDD	Digital supply	Digital I/O power supply (1.8 V or 3.3 V, nominal).
10	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions.
11	GPIO1	Digital I/O	General-purpose digital input/output 1 (multipurpose functions such as digital microphones clock or data, PLL input clock source, interrupt, and so forth).
12	SDA	Digital I/O	Data pin for I^2C control bus.
13	SCL	Digital input	Clock pin for I^2C control bus.
14	DREG	Digital supply	Digital regulator output voltage for digital core supply (1.5 V, nominal). Connect a 10-µF and 0.1-µF low ESR capacitor in parallel to device ground (VSS).
15	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions.
16	AVDD	Analog supply	Analog power (1.8 V or 3.3 V, nominal).

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
17	AREG	Analog supply	Analog on-chip regulator output voltage for analog supply (1.8 V, nominal) or external analog power (1.8 V, nominal). Connect a 10-µF and 0.1-µF low ESR capacitor in parallel to analog ground (AVSS).
18	VREF	Analog	Analog reference voltage filter output. Connect a 1-µF capacitor to analog ground (AVSS).
19	MICBIAS_GPI2	Analog output/digital input	MICBIAS output or general-purpose digital input 2 (multipurpose functions such as digital microphones data, PLL input clock source, and so forth). If used as MICBIAS output, then connect a 1-µF capacitor to analog ground (AVSS).
20	VSS	Ground supply	Device ground internally shorted to thermal pad. Short this package corner pin directly to the board ground plane. See the package drawings at the end of this document for corner pin dimensions.
Thermal Pad	Thermal Pad (VSS)	Ground supply	Thermal pad shorted to internal device ground. Short the thermal pad directly to the board ground plane.

7 Specifications

7.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	AREG to AVSS	–0.3	2.0	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input except IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
	Digital input IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)	–0.3	AVDD + 0.3	
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD, AREG(1)	Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator): AVDD 3.3-V operation	3.0	3.3	3.6	V
	Analog supply voltage AVDD and AREG to AVSS (AREG internal regulator is shutdown): AVDD 1.8-V operation	1.7	1.8	1.9	
IOVDD	IO supply voltage to VSS (thermal pad): IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad): IOVDD 1.8-V operation	1.65	1.8	1.95	
INPUTS					
	Analog input pins voltage to AVSS	0		AVDD	V
	Digital input except IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)	0		IOVDD	V
	Digital input IN2P_GPI1 and MICBIAS_GPI2 pins voltage to VSS (thermal pad)	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C
OTHERS					
	GPIOx or GPIx (used as MCLK input) clock frequency			36.864	MHz
C_b	SCL and SDA bus capacitance for I^2C interface supports standard-mode and fast-mode			400	pF
	SCL and SDA bus capacitance for I^2C interface supports fast-mode plus			550	
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

Thermal Information

THERMAL METRIC(1)		PCM6120-Q1 RTE (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.4 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CONFIGURATION						
	AC input impedance	Input pins INxP or INxM, 2.5-kΩ input impedance selection		2.5		kΩ
		Input pins INxP or INxM, 10-kΩ input impedance selection		10		
		Input pins INxP or INxM, 20-kΩ input impednace selection		20		
	Channel gain range	Programmable range with 0.5-dB steps	0		42	dB
ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 3.3-V OPERATION						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection	115	122		dB
		IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		117		
		IN1 differential input selected and AC signal shorted to ground, DRE disabled, 2.5-kΩ input impedance selection, 0-dB channel gain	106	112		
		IN1 differential input selected and AC signal shorted to ground, DRE disabled, 2.5-kΩ input impedance selection, 12-dB channel gain		108		
DR	Dynamic range, A-weighted(2)	IN1 differential input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection		123		dB
		IN1 differential input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		118		
		IN1 differential input selected and –60-dB full-scale AC signal input, DRE disabled, 2.5-kΩ input impedance selection, 0-dB channel gain		113		
		IN1 differential input selected and –72-dB full-scale AC signal input, DRE disabled, 2.5-kΩ input impedance selection, 12-dB channel gain		108		
THD+N	Total harmonic distortion(2) (3)	IN1 differential input selected and –1-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection		–95	–80	dB
		IN1 differential input selected and –1-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		–95		
		IN1 differential input selected and –1-dB full-scale AC signal input, DRE disabled, 2.5-kΩ input impedance selection, 0-dB channel gain		–95		
		IN1 differential input selected and –13-dB full-scale AC signal input, DRE disabled, 2.5-kΩ input impedance selection, 12-dB channel gain		–93		
ADC PERFORMANCE FOR LINE/MICROPHONE INPUT RECORDING : AVDD 1.8-V OPERATION						
	Differential input full-scale AC signal voltage	AC-coupled Input		1		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled Input		0.5		V_{RMS}

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection		116		dB
		IN1 differential input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		111		
		IN1 differential input selected and AC signal shorted to ground, DRE disabled, 2.5-kΩ input impedance selection, 0-dB channel gain		105		
DR	Dynamic range, A-weighted(2)	IN1 differential input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection		117		dB
		IN1 differential input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		112		
		IN1 differential input selected and –60-dB full-scale AC signal input, DRE disabled, 2.5-kΩ input impedance selection, 0-dB channel gain		106		
THD+N	Total harmonic distortion(2) (3)	IN1 differential input selected and –2-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 2.5-kΩ input impedance selection		–90		dB
		IN1 differential input selected and –2-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 24 dB), 10-kΩ input impedance selection		–90		
		IN1 differential input selected and –2-dB full-scale AC signal Input, DRE disabled, 2.5-kΩ input impedance selection, 0 dB channel gain		–90		
ADC OTHER PARAMETERS						
	Digital volume control range	Programmable 0.5-dB steps	–100		27	dB
	Output data sample rate	Programmable	7.35		768	kHz
	Output data sample word length	Programmable	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		12		Hz
	Interchannel isolation	–1-dB full-scale AC-signal input to non measurement channel		–124		dB
	Interchannel gain mismatch	–6-dB full-scale AC-signal input and 0-dB channel gain		0.1		dB
	Gain drift(4)	0-dB channel gain, across temperature range –40°C to 125°C		36.8		ppm/°C
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.02		Degrees
	Phase drift(5)	1-kHz sinusoidal signal, across temperature range –40°C to 125°C		0.0005		Degrees/°C
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		102		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 0-dB channel gain, 100-mV_{PP}, 1-kHz signal on both pins and measure level at output in high CMRR Mode		80		dB
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS		2.1		$µV_{RMS}$

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	MICBIAS voltage	MICBIAS programmed to VREF and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V		VREF		V
		MICBIAS programmed to VREF × 1.096 and VREF programmed to either 2.75 V, 2.5 V, or 1.375 V		VREF × 1.096		
		Bypass to AVDD with 5-mA load		AVDD – 0.2		
	MICBIAS current drive				5	mA
	MICBIAS load regulation	MICBIAS programmed to either VREF or VREF × 1.096, measured up to max load	0	0.6	1	%
	MICBIAS over current protection threshold		6.1			mA
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 1.8-V operation	–0.3		0.35 × IOVDD	V
		All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 1.8-V operation	0.65 × IOVDD		IOVDD + 0.3	V
		All digital pins except IN2P_GPI1 and MICBIAS_GPI2, SDA and SCL, IOVDD 3.3-V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins except IN2M_GPO1, SDA and SCL, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins except IN2M_GPO1, SDA and SCL, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins except IN2M_GPO1, SDA and SCL, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins except IN2M_GPO1, SDA and SCL, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold	SDA and SCL	–0.5		0.3 x IOVDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold	SDA and SCL	0.7 x IOVDD		IOVDD + 0.5	V
$V_{OL1(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –3 mA, IOVDD > 2 V			0.4	V
$V_{OL2(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –2 mA, IOVDD ≤ 2 V			0.2 x IOVDD	V
$I_{OL(I2C)}$	Low-level digital output current	SDA, $V_{OL(I2C)}$ = 0.4 V, standard-mode or fast-mode	3			mA
		SDA, $V_{OL(I2C)}$ = 0.4 V, fast-mode plus	20			
I_{IH}	Input logic-high leakage for digital inputs	All digital pins except IN2P_GPI1 and MICBIAS_GPI2 pins, input = IOVDD	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins except IN2P_GPI1 and MICBIAS_GPI2 pins, input = 0 V	–5	0.1	5	µA
$V_{IL(GPIx)}$	Low-level digital input logic voltage threshold	IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 1.8-V operation	–0.3		0.35 × AVDD	V
		IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 3.3-V operation	–0.3		0.8	
$V_{IH(GPIx)}$	High-level digital input logic voltage threshold	IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 1.8-V operation	0.65 × AVDD		AVDD + 0.3	V
		IN2P_GPI1 and MICBIAS_GPI2 digital pins, AVDD 3.3-V operation	2		AVDD + 0.3	
$V_{OL(GPOx)}$	Low-level digital output voltage	IN2M_GPO2 digital pin, I_{OL} = –2 mA, AVDD 1.8-V operation			0.45	V
		IN2M_GPO2 digital pin, I_{OL} = –2 mA, AVDD 3.3-V operation			0.4	
$V_{OH(GPOx)}$	High-level digital output voltage	IN2M_GPO2 digital pin, I_{OH} = 2 mA, AVDD 1.8-V operation	AVDD – 0.45			V
		IN2M_GPO2 digital pin, I_{OH} = 2 mA, AVDD 3.3-V operation	2.4			

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH(GPIx)}$	Input logic-high leakage for digital inputs	IN2P_GPI1 and MICBIAS_GPI2 digital pins, input = AVDD	–5	0.1	5	µA
$I_{IL(GPIx)}$	Input logic-high leakage for digital inputs	IN2P_GPI1 and MICBIAS_GPI2 digital pins, input = 0 V	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All external clocks stopped, AVDD = 3.3 V, internal AREG		5		µA
I_{AVDD}		All external clocks stopped, AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		29		
I_{IOVDD}		All external clocks stopped, IOVDD = 3.3 V		0.5		
I_{IOVDD}		All external clocks stopped, IOVDD = 1.8 V		0.5		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48-kHz, PLL off, BCLK = 512 × f_S and DRE disable	AVDD = 3.3 V, internal AREG		11.3		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		10.6		
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 16-kHz, PLL on, BCLK = 256 × f_S and DRE disable	AVDD = 3.3 V, internal AREG		11.5		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		10.8		
I_{IOVDD}		IOVDD = 3.3 V		0.05		
I_{IOVDD}		IOVDD = 1.8 V		0.02		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48-kHz, PLL on, BCLK = 256 × f_S and DRE disable	AVDD = 3.3 V, internal AREG		12.4		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		11.7		
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48-kHz, PLL on, BCLK = 256 × f_S and DRE enable	AVDD = 3.3 V, internal AREG		13.8		mA
I_{AVDD}		AVDD = 1.8 V, external AREG supply (AREG shorted to AVDD)		13.1		
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) For best distortion performance, use input AC-coupling capacitors with low-voltage coefficient.
(4) Gain drift = gain variation (in temperature range) / typical gain value (gain at room temperature) / temperature range × 10^6 measured with gain in linear scale.
(5) Phase drift = phase deviation (in temperature range) / (temperature range).

7.5 Timing Requirements: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 7-1 for timing diagram

		MIN	NOM	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HIGH}	High period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time	0		3.45	µs
$t_{SU;DAT}$	Data setup time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Setup time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST-MODE					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0		0.9	µs
$t_{SU;DAT}$	Data setup time	100			ns
t_r	SDA and SCL rise time	20		300	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		300	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HIGH}	High period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time	0			µs
$t_{SU;DAT}$	Data setup time	50			ns
t_r	SDA and SCL rise time			120	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		120	ns
$t_{SU;STO}$	Setup time for STOP condition	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

7.6 Switching Characteristics: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see Figure 7-1 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDA)}$	SCL to SDA delay	Standard-mode	250		1250	ns
		Fast-mode	250		850	
		Fast-mode plus			400	

7.7 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-2 for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		25			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		25			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time(2)			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time(2)			10	ns

(1) The BCLK minimum high or low pulse duration can be relaxed to 14 ns (to meet the timing specifications), if the SDOUT data line is latched on the same BCLK edge polarity as the edge used by the device to transmit SDOUT data.
(2) The BCLK maximum rise and fall time can be relaxed to 13 ns if the BCLK frequency used in the system is below 20 MHz. Relaxing the BCLK rise and fall time can cause noise to increase because of higher clock jitter.

7.8 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-2 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT	3		18	ns
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT			18	ns
$f_{(BCLK)}$	BCLK output clock frequency: master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration: master mode		14			ns
$t_{L(BCLK)}$	BCLK low pulse duration: master mode		14			ns
$t_{d(FSYNC)}$	BCLK to FSYNC delay: master mode	50% of BCLK to 50% of FSYNC	3		18	ns
$t_{r(BCLK)}$	BCLK rise time: master mode	10% - 90% rise time			8	ns
$t_{f(BCLK)}$	BCLK fall time: master mode	90% - 10% fall time			8	ns

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

Timing Requirements: PDM Digital Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-3 for timing diagram

		MIN	NOM	MAX	UNIT
$t_{SU(PDMDINx)}$	PDMDINx setup time	30			ns
$t_{HLD(PDMDINx)}$	PDMDINx hold time	0			ns

7.9 Switching Characteristics: PDM Digial Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-3 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(PDMCLK)}$	PDMCLK clock frequency		0.768		6.144	MHz
$t_{H(PDMCLK)}$	PDMCLK high pulse duration		72			ns
$t_{L(PDMCLK)}$	PDMCLK low pulse duration		72			ns
$t_{r(PDMCLK)}$	PDMCLK rise time	10% - 90% rise time			18	ns

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see Figure 7-3 for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{f(PDMCLK)}$	PDMCLK fall time	90% - 10% fall time			18	ns

7.10 Timing Diagrams

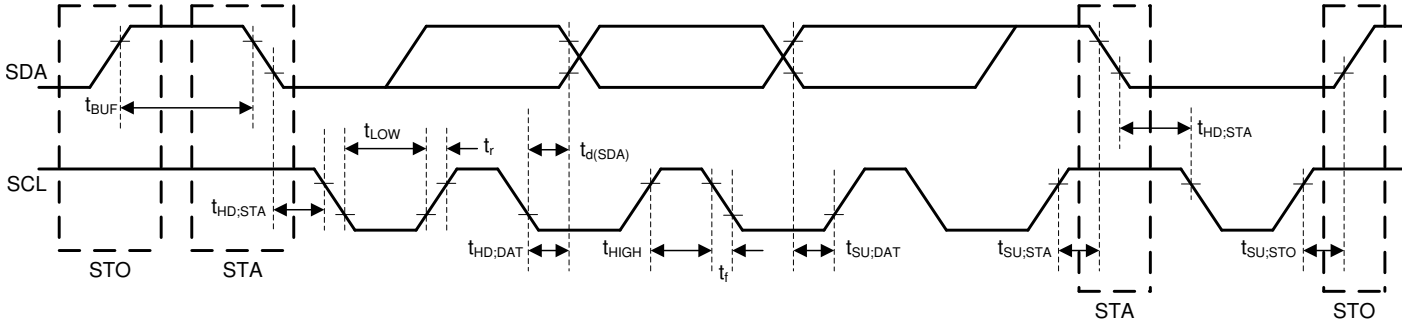


Figure 7-1. I²C Interface Timing Diagram

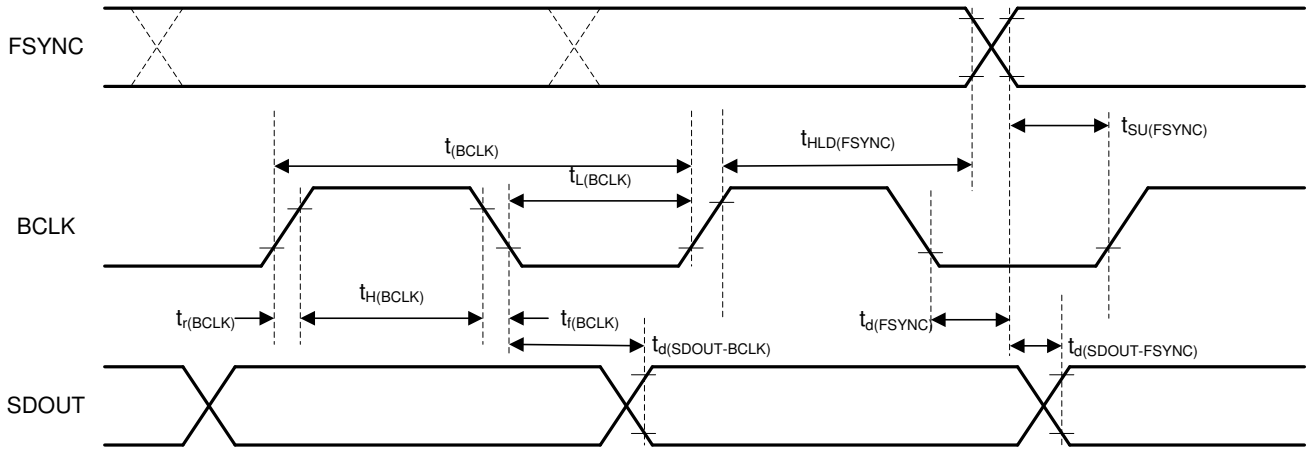


Figure 7-2. TDM (With BCLK_POL = 1), I²S, and LJ Interface Timing Diagram

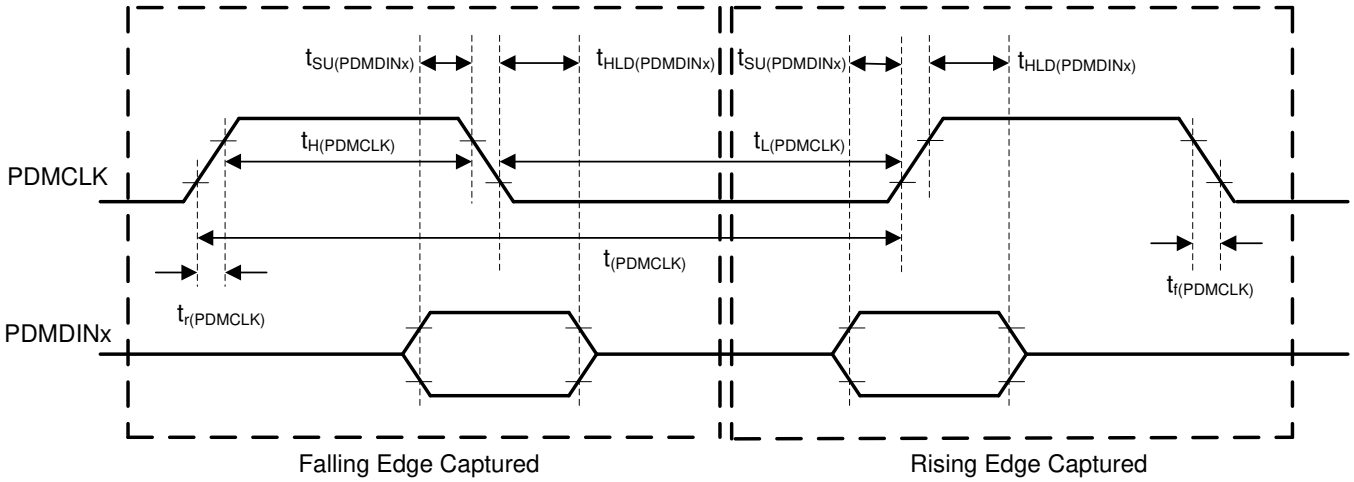
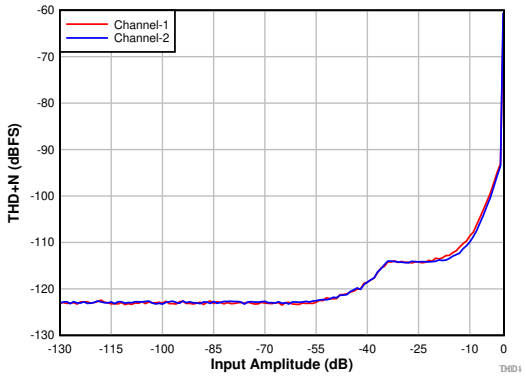


Figure 7-3. PDM Digital Microphone Interface Timing Diagram

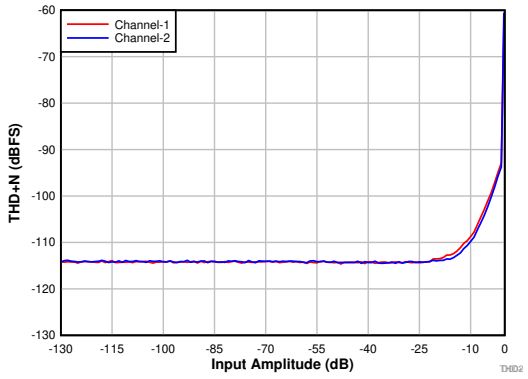
7.11 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter



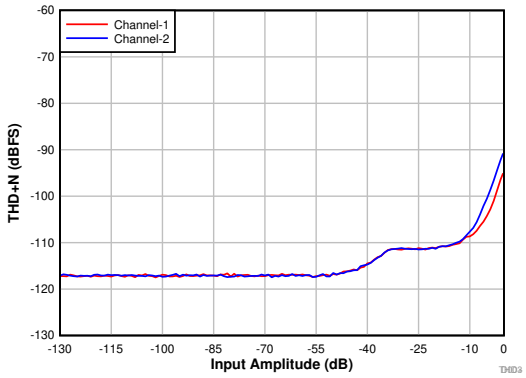
Differential input

Figure 7-4. THD+N vs Input Amplitude With DRE Enabled



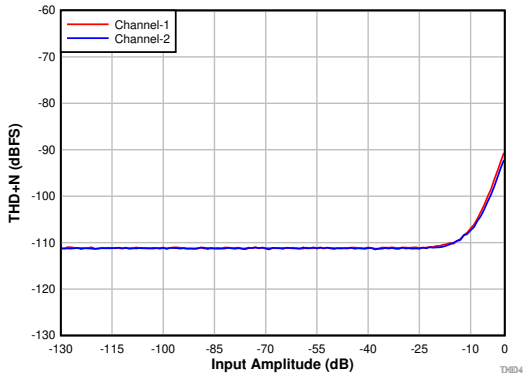
Differential input

Figure 7-5. THD+N vs Input Amplitude With DRE Disabled



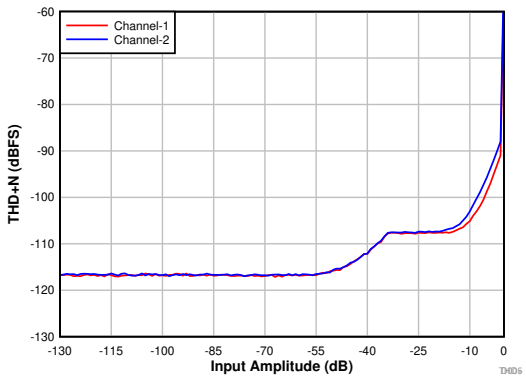
Single-ended input

Figure 7-6. THD+N vs Input Amplitude With DRE Enabled



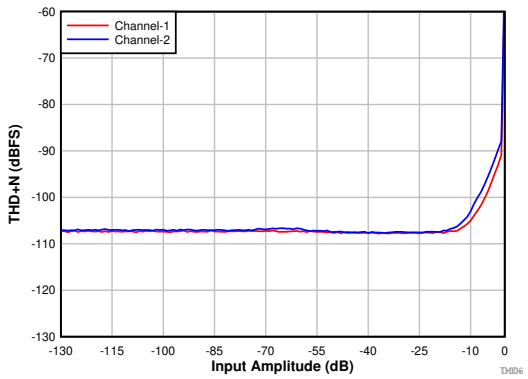
Single-ended input

Figure 7-7. THD+N vs Input Amplitude With DRE Disabled



Differential input with AVDD = 1.8 V and VREF = 1.375 V

Figure 7-8. THD+N vs Input Amplitude With DRE Enabled



Differential input with AVDD = 1.8 V and VREF = 1.375 V

Figure 7-9. THD+N vs Input Amplitude With DRE Disabled

7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

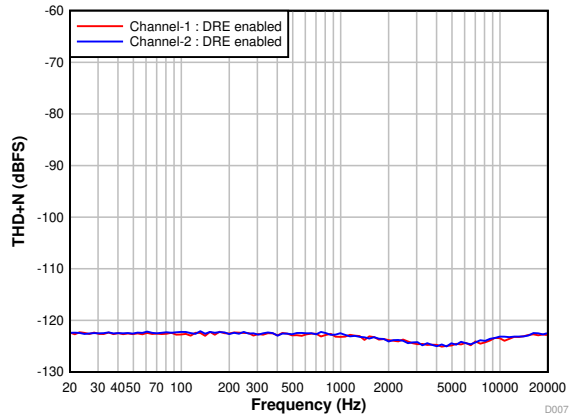


Figure 7-10. THD+N vs Input Frequency at –60-dBr Input With DRE Enabled

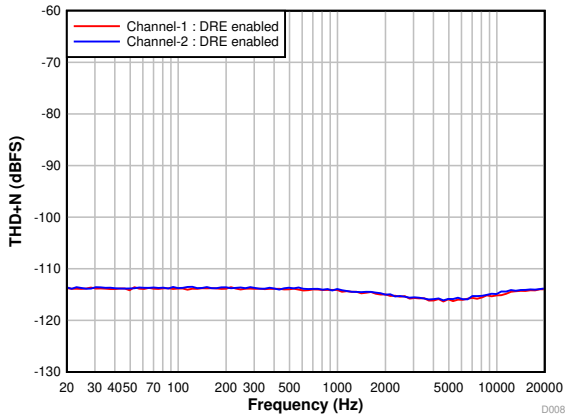


Figure 7-11. THD+N vs Input Frequency at –60-dBr Input With DRE Disabled

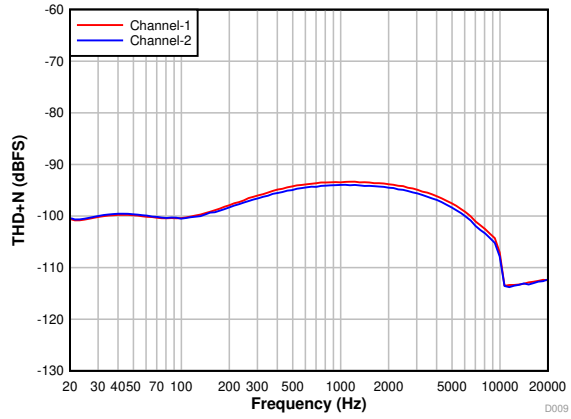
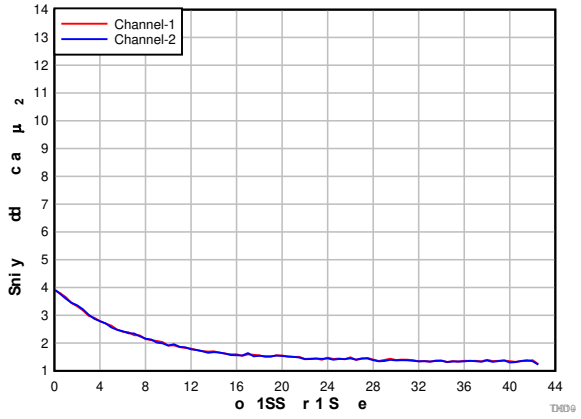
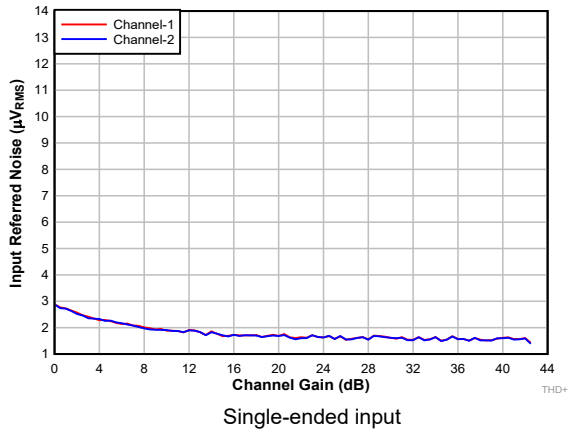


Figure 7-12. THD+N vs Input Frequency at –1-dBr Input With DRE Disabled



Differential input

Figure 7-13. Input-Referred Noise vs Channel Gain



Single-ended input

Figure 7-14. Input-Referred Noise vs Channel Gain

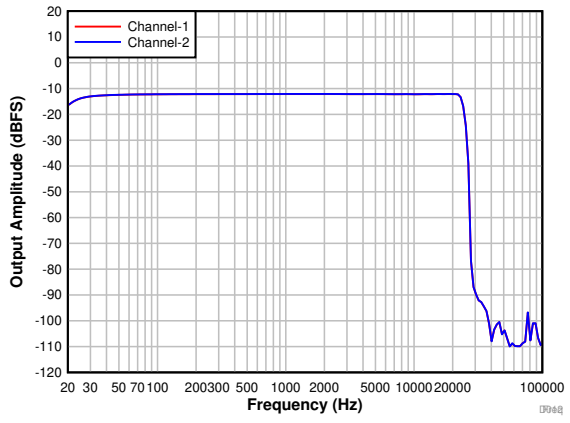


Figure 7-15. Frequency Response With a –12-dBr Input

7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

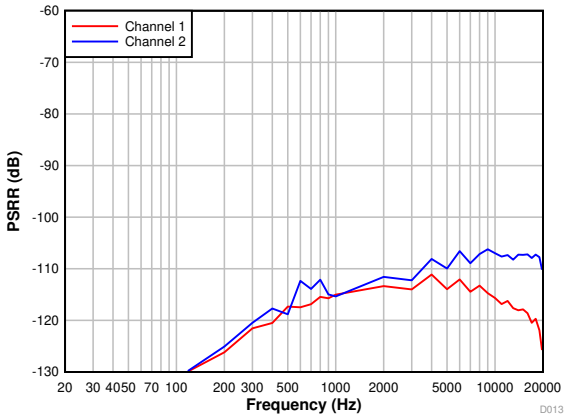


Figure 7-16. Power-Supply Rejection Ratio vs Ripple Frequency With 100-mV_{PP} Amplitude

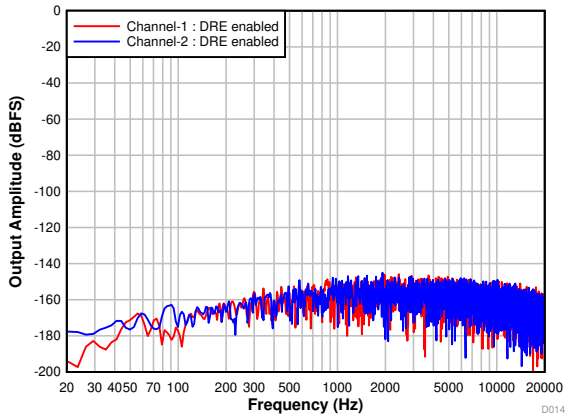


Figure 7-17. Differential FFT With Idle Input With DRE Enabled

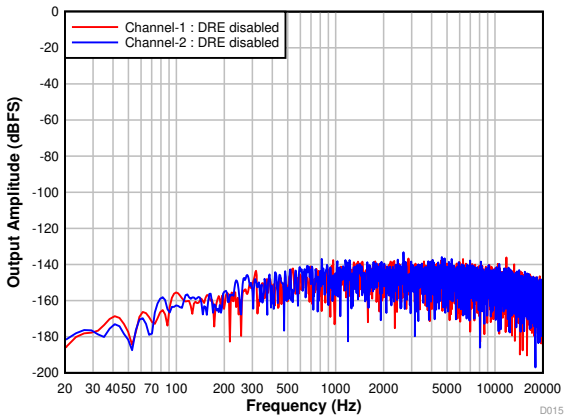


Figure 7-18. Differential FFT With Idle Input With DRE Disabled

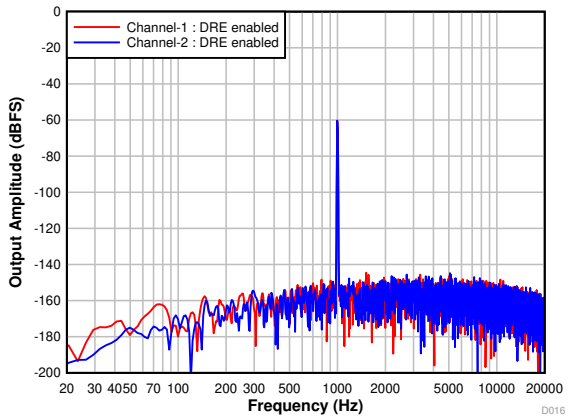


Figure 7-19. Differential FFT With a –60-dBr Input With DRE Enabled

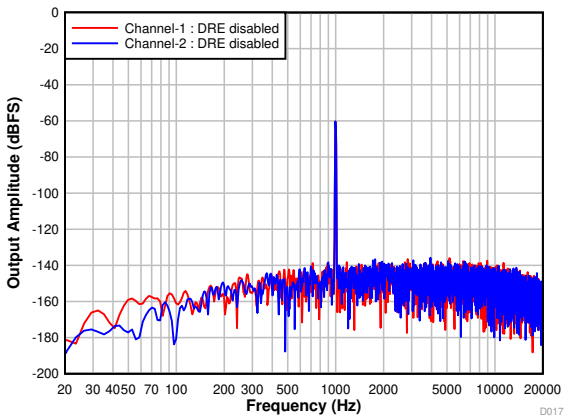


Figure 7-20. Differential FFT With a –60-dBr Input With DRE Disabled

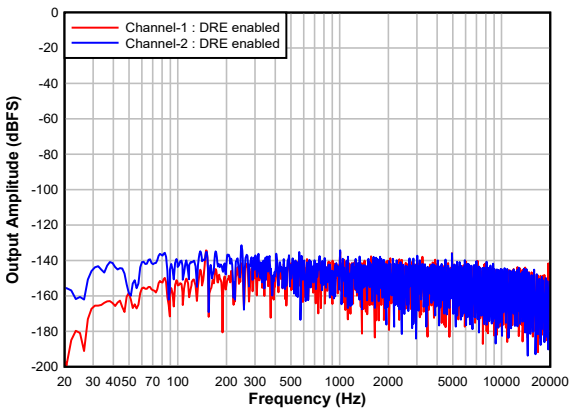


Figure 7-21. Single Ended FFT With Idle Input With DRE Enabled

7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

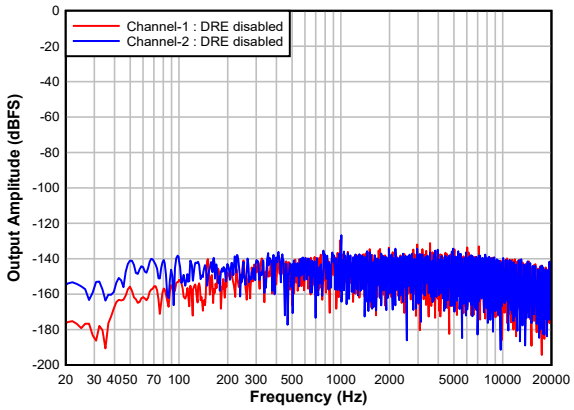


Figure 7-22. Single Ended FFT With Idle Input With DRE Disabled

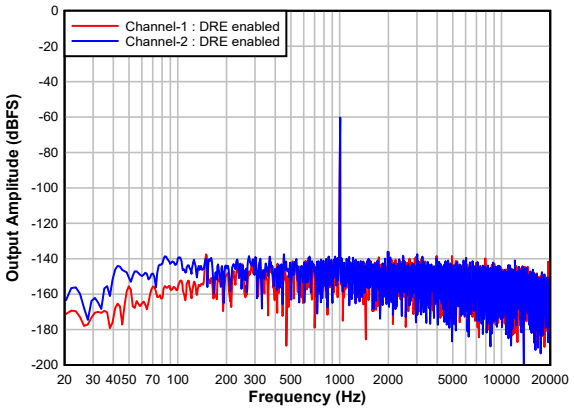


Figure 7-23. Single Ended FFT With a –60-dBr Input With DRE Enabled

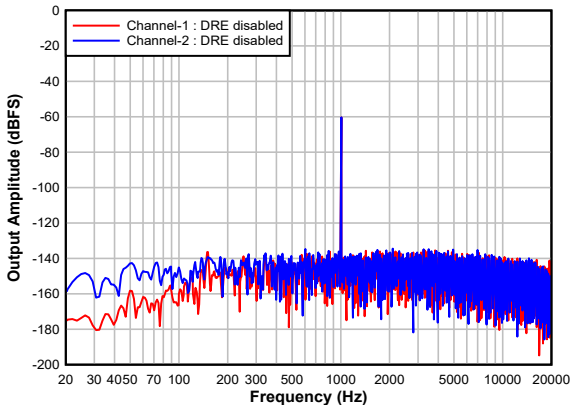


Figure 7-24. Single Ended FFT With a –60-dBr Input With DRE Disabled

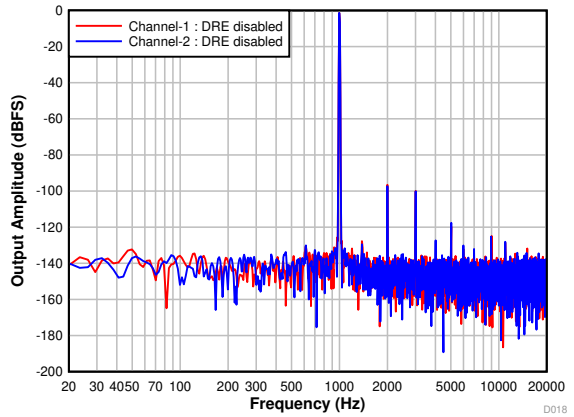
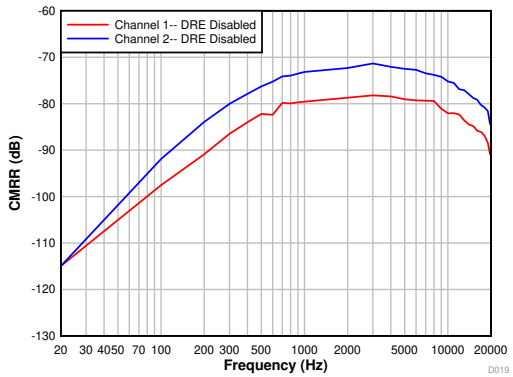
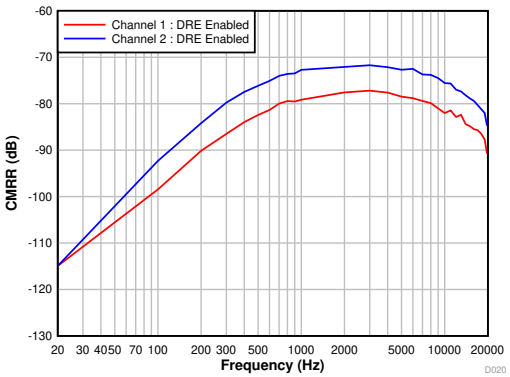


Figure 7-25. Differential FFT With a –1-dBr Input With DRE Disabled



High CMRR mode

Figure 7-26. Common-Mode Rejection Ratio vs Ripple Frequency With 100-mV_{PP} Amplitude and DRE Disabled

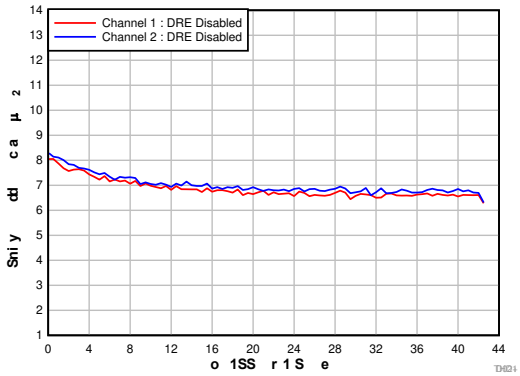


High CMRR mode

Figure 7-27. Common-Mode Rejection Ratio vs Ripple Frequency With 100-mV_{PP} Amplitude and DRE Enabled

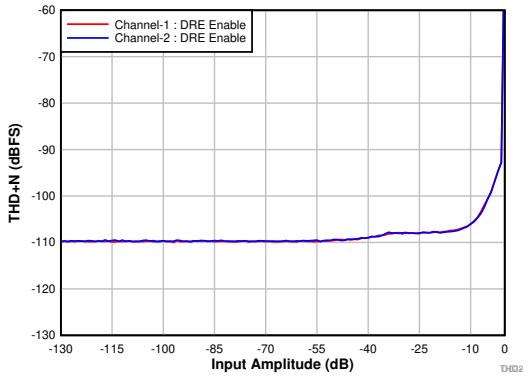
7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter



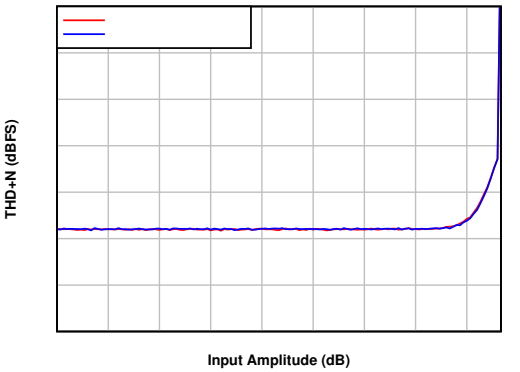
High CMRR mode

Figure 7-28. Input-Referred Noise vs Channel Gain



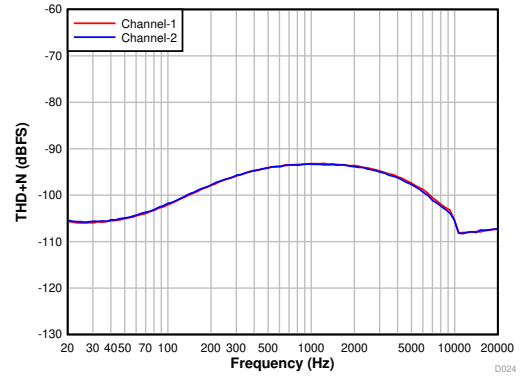
Differential input with high CMRR mode

Figure 7-29. THD+N vs Input Amplitude With DRE Enabled



Differential input with high CMRR mode

Figure 7-30. THD+N vs Input Amplitude With DRE Disabled



Differential input with high CMRR mode

Figure 7-31. THD+N vs Input Frequency at –1-dBr Input With DRE Disabled

8 Detailed Description

8.1 Overview

The PCM6120-Q1 is a high-performance, low-power, flexible, 2-channel, audio analog-to-digital converter (ADC) with extensive feature integration. This device is intended for applications in voice-activated systems, professional microphones, audio conferencing, portable computing, communication, and entertainment applications. The high dynamic range of the device enables far-field audio recording with high fidelity. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications.

The PCM6120-Q1 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADC
- Configurable single-ended or differential audio inputs
- Low-noise, programmable microphone bias output
- Dynamic range enhancer (DRE) to support a 123-dB dynamic range
- Automatic gain controller (AGC)
- Programmable decimation filters with a linear-phase filter or a low-latency filter
- Programmable channel gain, volume control, biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF), and digital channel mixer
- Pulse density modulation (PDM) microphone 4-channel interface with a high-performance decimation filter
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the PCM6120-Q1 for configuring the control registers is supported using an I^2C interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I^2S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

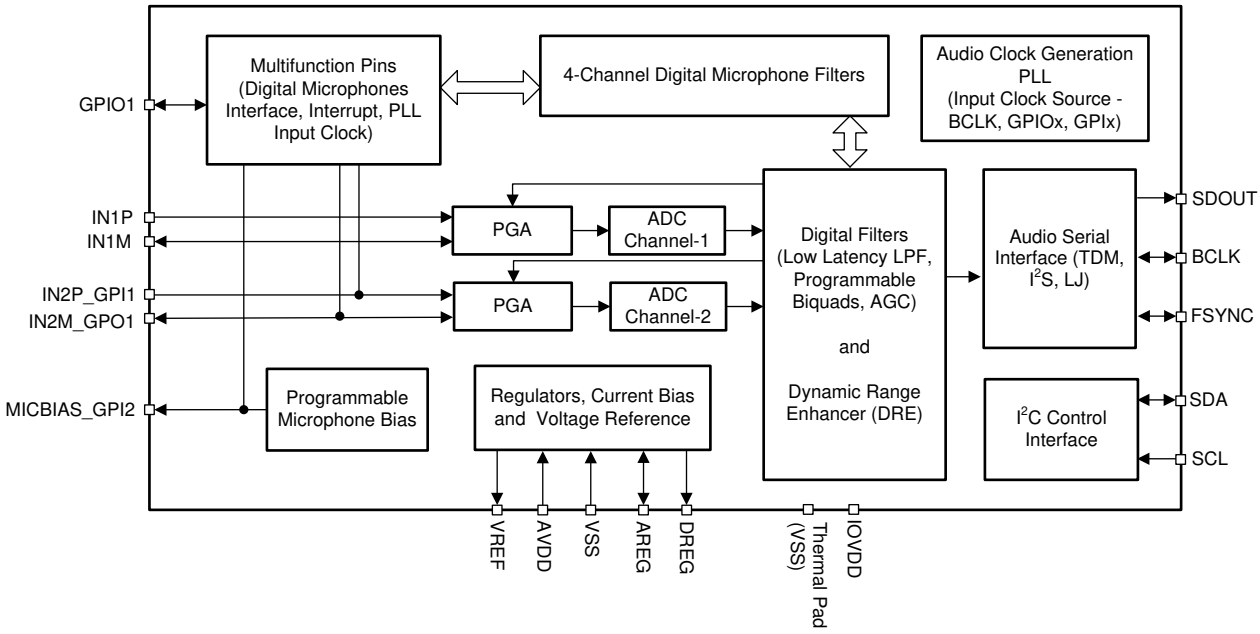
The PCM6120-Q1 can support multiple devices by sharing the common TDM bus across devices. Moreover, the device includes a daisy-chain feature as well. These features relax the shared TDM bus timing requirements and board design complexities when operating multiple devices for applications requiring high audio data bandwidth.

Table 8-1 lists the reference abbreviations used throughout this document to registers that control the device.

Table 8-1. Abbreviations for Register References

REFERENCE	ABBREVIATION	DESCRIPTION	EXAMPLE
Page y, register z, bit k	Py_Rz_Dk	Single data bit. The value of a single bit in a register.	Page 4, register 36, bit 0 = P4_R36_D0
Page y, register z, bits k-m	Py_Rz_D[k:m]	Range of data bits. A range of data bits (inclusive).	Page 4, register 36, bits 3-0 = P4_R36_D[3:0]
Page y, register z	Py_Rz	One entire register. All eight bits in the register as a unit.	Page 4, register 36 = P4_R36
Page y, registers z-n	Py_Rz-Rn	Range of registers. A range of registers in the same page.	Page 4, registers 36, 37, 38 = P4_R36-R38

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

8.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All registers can be accessed using I^2C communication to the device. For more information, see *Section 8.5* for further details.

8.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCM6120-Q1 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^2S or left-justified protocols format, programmable data length options, very flexible master-slave configurability for bus clock lines, and the ability to communicate with multiple devices within a system directly.

The bus protocol TDM, I²S, or left-justified (LJ) format can be selected by using the ASI_FORMAT[1:0] (P0_R7_D[7:6]) register bits. As shown in Table 8-2 and Table 8-3, these modes are all most significant bit (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the ASI_WLEN[1:0] (P0_R7_D[5:4]) register bits.

Table 8-2. Audio Serial Interface Format

P0_R7_D[7:6] : ASI_FORMAT[1:0]	AUDIO SERIAL INTERFACE FORMAT
00 (default)	Time division multiplexing (TDM) mode
01	Inter IC sound (I²S) mode
10	Left-justified (LJ) mode
11	Reserved (do not use this setting)

Table 8-3. Audio Output Channel Data Word-Length

P0_R7_D[5:4] : ASI_WLEN[1:0]	AUDIO OUTPUT CHANNEL DATA WORD-LENGTH
00	Output channel data word-length set to 16 bits
01	Output channel data word-length set to 20 bits
10	Output channel data word-length set to 24 bits
11 (default)	Output channel data word-length set to 32 bits

The frame sync pin, FSYNC, is used to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate all active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 64) on the audio bus. This allows for either a single device or multiple PCM6120-Q1 devices sharing the same bus. The device supports up to four output channels that can be configured to place their audio data on bus slot 0 to slot 63. Table 8-4 lists the output channel slot configuration settings. In I²S and LJ mode, the slots are divided into two sets, left-channel slots and right-channel slots, as described in *Section 8.3.1.2.2* and *Section 8.3.1.2.3* .

Table 8-4. Output Channel Slot Assignment Settings

P0_R11_D[5:0] : CH1_SLOT[5:0]	OUTPUT CHANNEL 1 SLOT ASSIGNMENT
00 0000 = 0d (default)	Slot 0 for TDM or left slot 0 for I²S, LJ.
00 0001 = 1d	Slot 1 for TDM or left slot 1 for I²S, LJ.
…	…
01 1111 = 31d	Slot 31 for TDM or left slot 31 for I²S, LJ.
10 0000 = 32d	Slot 32 for TDM or right slot 0 for I²S, LJ.
…	…
11 1110 = 62d	Slot 62 for TDM or right slot 30 for I²S, LJ.
11 1111 = 63d	Slot 63 for TDM or right slot 31 for I²S, LJ.

Similarly, the slot assignment setting for output channel 2 to channel 8 can be done using the CH2_SLOT (P0_R12) to CH8_SLOT (P0_R18) registers, respectively.

The slot word length is the same as the output channel data word length set for the device. The output channel data word length must be set to the same value for all PCM6120-Q1 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

The device also includes a feature that offsets the start of the slot data transfer with respect to the frame sync by up to 31 cycles of the bit clock. Table 8-5 lists the programmable offset configuration settings.

Table 8-5. Programmable Offset Settings for the ASI Slot Start

P0_R8_D[4:0] : TX_OFFSET[4:0]	PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START
0 0000 = 0d (default)	The device follows the standard protocol timing without any offset.
0 0001 = 1d	Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing.
.....	.....
1 1110 = 30d	Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.
1 1111 = 31d	Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the FSYNC_POL (P0_R7_D3) register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the BCLK_POL (P0_R7_D2) register bit.

8.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 8-1 to Figure 8-4 illustrate the protocol timing for TDM operation with various configurations.

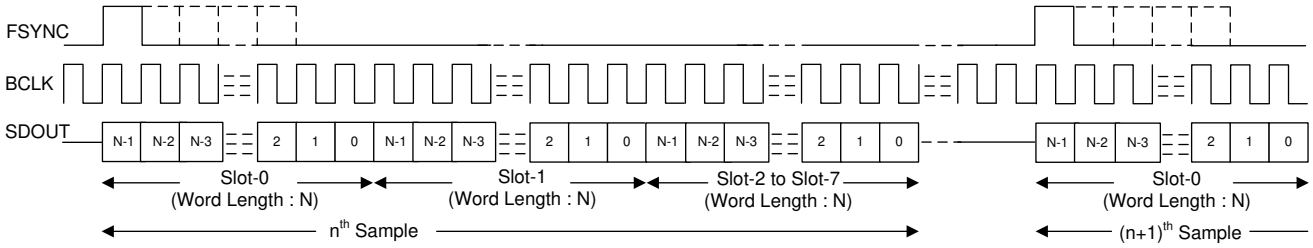


Figure 8-1. TDM Mode Standard Protocol Timing (TX_OFFSET = 0)

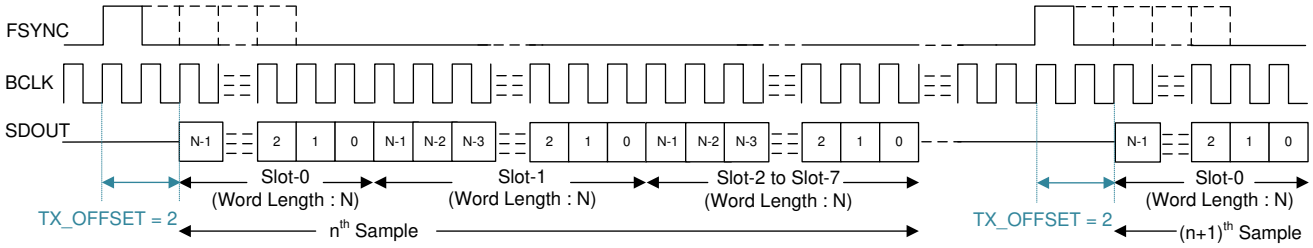


Figure 8-2. TDM Mode Protocol Timing (TX_OFFSET = 2)

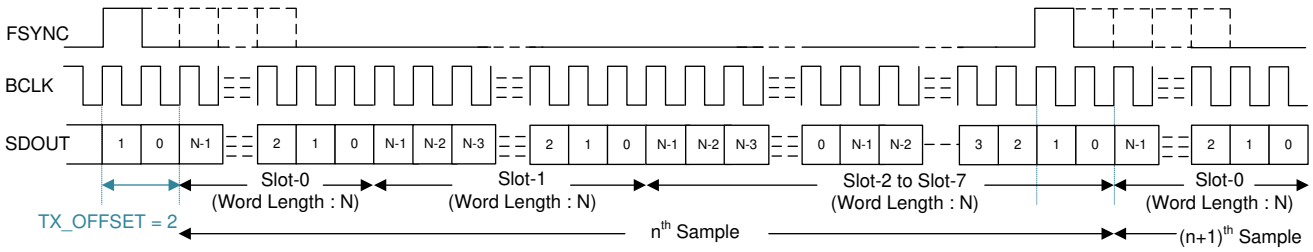


Figure 8-3. TDM Mode Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 2)

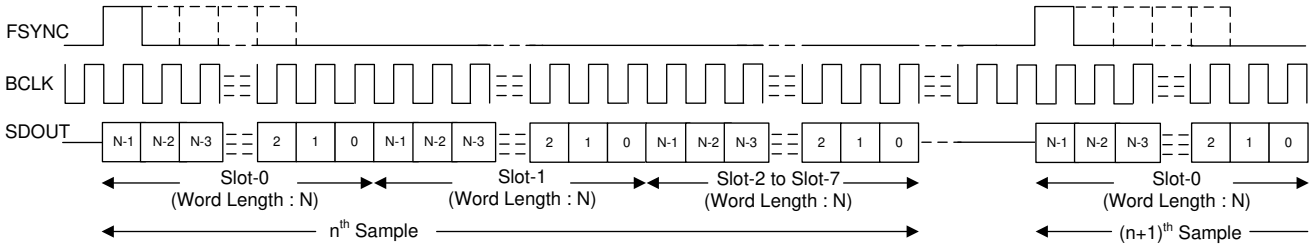


Figure 8-4. TDM Mode Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a TX_OFFSET value higher than 0 is recommended.

8.3.1.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. Figure 8-5 to Figure 8-8 illustrate the protocol timing for I^2S operation with various configurations.

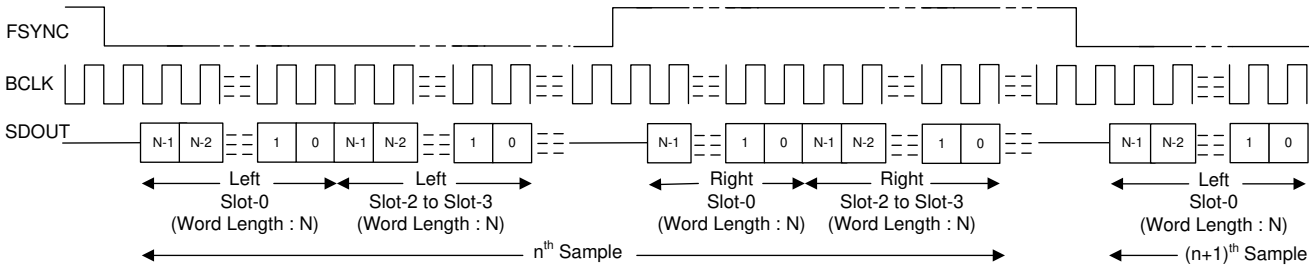


Figure 8-5. I^2S Mode Standard Protocol Timing (TX_OFFSET = 0)

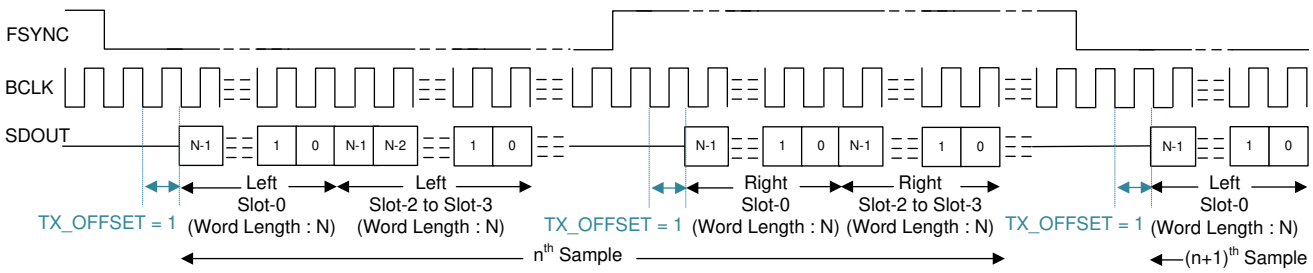


Figure 8-6. I^2S Protocol Timing (TX_OFFSET = 1)

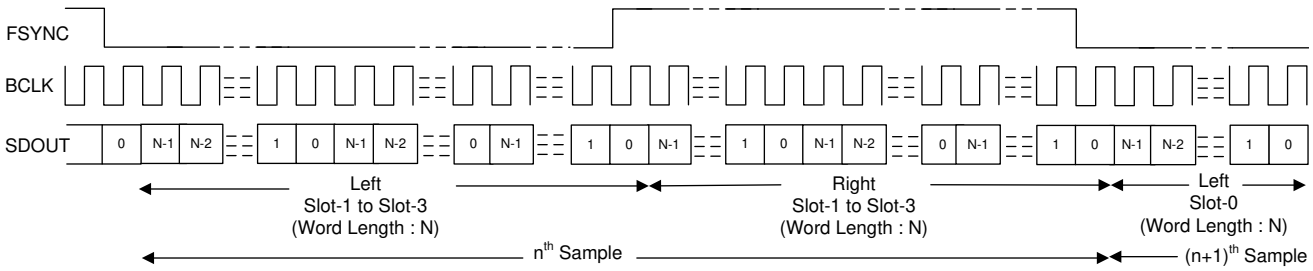


Figure 8-7. I²S Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

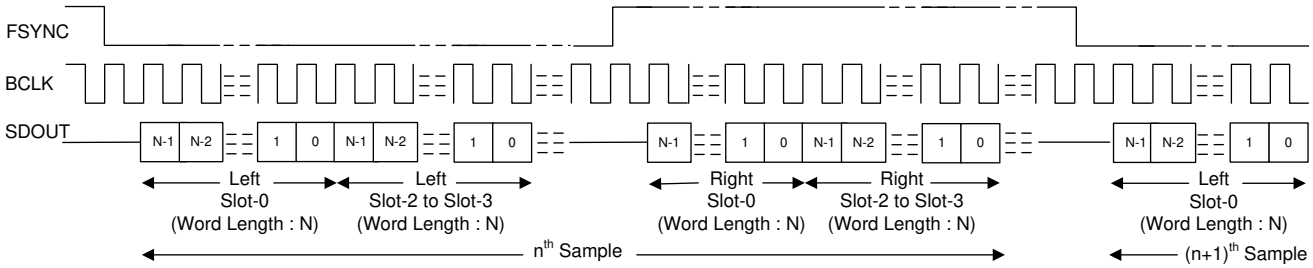


Figure 8-8. I²S Protocol Timing (TX_OFFSET = 0 and BCLK_POL = 1)

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

8.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. Figure 8-9 to Figure 8-12 illustrate the protocol timing for LJ operation with various configurations.

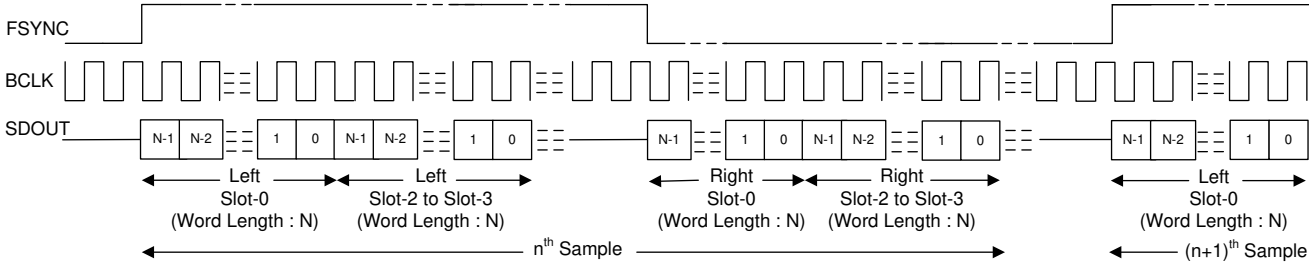


Figure 8-9. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)

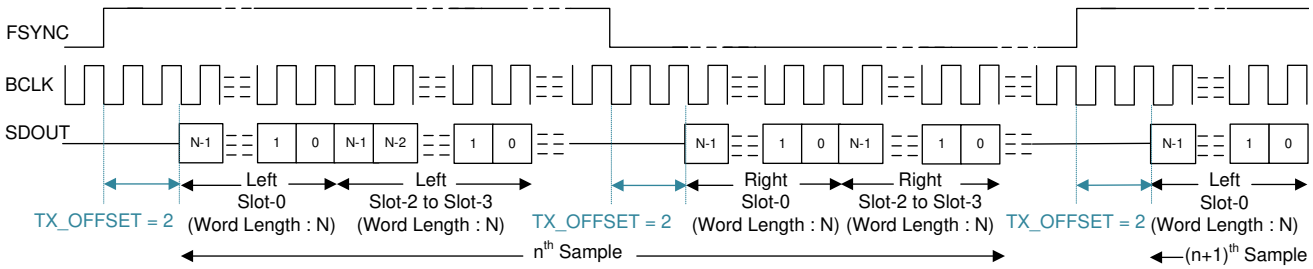


Figure 8-10. LJ Protocol Timing (TX_OFFSET = 2)

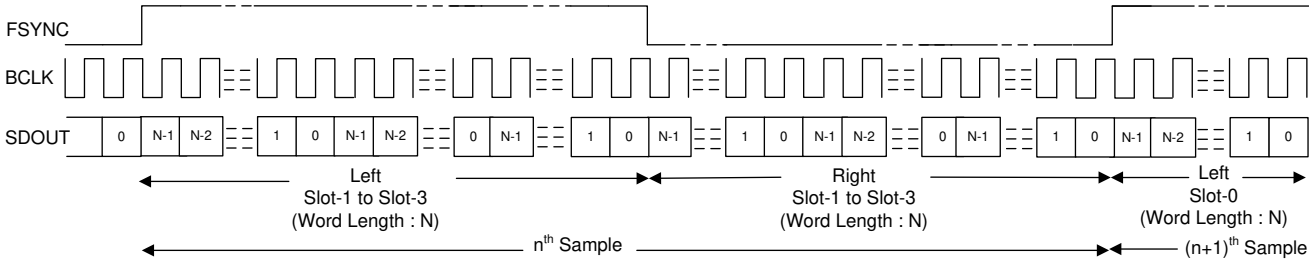


Figure 8-11. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

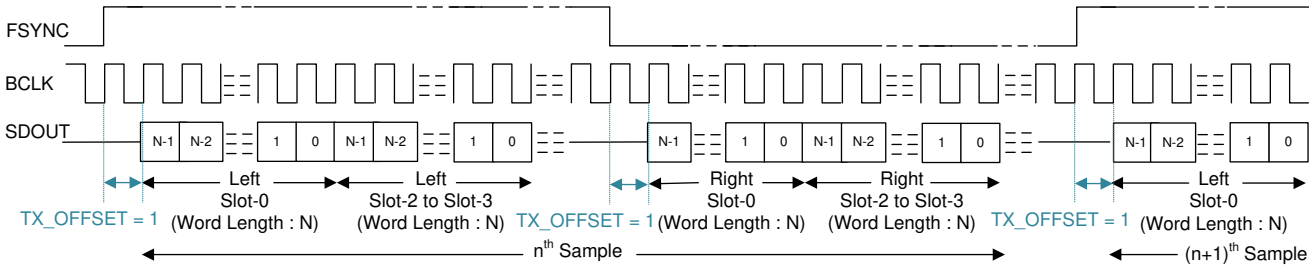


Figure 8-12. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

8.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect the PCM6120-Q1 and any other audio device by sharing a single common I²C control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone array for beam-forming operations, audio conferencing, noise cancellation, and so forth. Figure 8-13 shows a diagram of the PCM6120-Q1 and PCMx140-Q1 devices in a configuration where the control and audio data buses are shared.

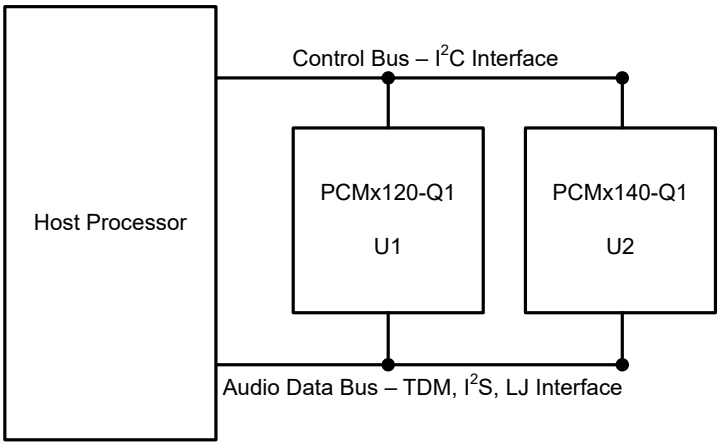


Figure 8-13. Multiple Devices With Shared Control and Audio Data Buses

The PCM6120-Q1 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- I²C broadcast simultaneously writes to (or triggers) all PCM6120-Q1 and PCMx140-Q1 devices
- Supports up to 64 configuration output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIO1 or GPOx pin can be configured as a secondary output data lane for the audio serial interface
- The GPIO1 or GPIx pin can be used in a daisy-chain configuration of multiple devices
- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable master and slave options for the audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices

See the *Multiple TLV320ADCx140 Devices With Shared TDM and I²C Bus* application report for further details.

8.3.2 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the ADC modulator and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio bus.

The device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 8-6 and Table 8-7 list the supported FSYNC and BCLK frequencies.

Table 8-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)	FSYNC (384 kHz)	FSYNC (768 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072	6.144	12.288
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608	9.216	18.432
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144	12.288	24.576
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216	18.432	**Reserved**
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288	24.576	**Reserved**
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432	**Reserved**	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576	**Reserved**	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	8.192	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	16.384	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

Table 8-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224	5.6448	11.2896
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336	8.4672	16.9344
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448	11.2896	22.5792
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672	16.9344	**Reserved**
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896	22.5792	**Reserved**
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344	**Reserved**	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792	**Reserved**	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	7.5264	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	15.0528	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

The status register ASI_STS (P0_R21), captures the device auto detect result for the FSYNC frequency and the BCLK to FSYNC ratio. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes the record channels accordingly.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks. The device also supports an option

to use BCLK, GPIO1, or the GPIx pin (as MCLK) as the audio clock source without using the PLL to reduce power consumption. However, the ADC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the *TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios* application report.

The device also supports an audio bus master mode operation using the GPIO1 or GPIx pin (as MCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on master mode configuration and operation are discussed in the *Configuring and Operating TLV320ADCx120 as an Audio Bus Master* application report.

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the ASI_ERR (P0_R9_D5) and AUTO_CLK_CFG (P0_R19_D6) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the *ADCx120EVM-PDK Evaluation module* user's guide and the PurePath™ console graphical development suite.

8.3.3 Input Channel Configurations

The device consists of two pairs of analog input pins (INxP and INxM) that can be configured as differential inputs or single-ended inputs for the recording channel. The device supports simultaneous recording of up to two channels using the high-performance multichannel ADC. The input source for the analog pins can be from electret condenser analog microphones, micro-electro-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board. Additionally, if the application uses digital PDM microphones for the recording, then the IN2P_GPI1, IN2M_GPO1, GPIO1, and MICBIAS_GPI2 pins can be reconfigured in the device to support up to four channels for the digital microphone recording. The device can also support simultaneous recording on two analog and two digital microphone channels. Table 8-8 shows the input source selection for the record channel.

Table 8-8. Input Source Selection for the Record Channel

P0_R60_D[6:5] : CH1_INSRC[1:0]	INPUT CHANNEL 1 RECORD SOURCE SELECTION
00 (default)	Analog differential input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled)
01	Analog single-ended input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled)
10	Digital PDM input for channel 1 (configure the GPIx and GPOx pin accordingly for PDMDIN1 and PDMCLK)
11	Reserved (do not use this setting)

Similarly, the input source selection setting for input channel 2, channel 3, and channel 4 can be configured using the CH2_INSRC[1:0] (P0_R65_D[6:5]), CH3_INSRC[1:0] (P0_R70_D[6:5]), and CH4_INSRC[1:0] (P0_R75_D[6:5]) register bits, respectively.

Typically, voice or audio signal inputs are capacitively coupled (AC coupled) to the device; however, the device also supports an option for DC-coupled inputs to save board space. This configuration can be done independently for each channel by setting the CH1_DC (P0_R60_D4), CH2_DC (P0_R65_D4), CH3_DC (P0_R70_D4), and CH4_DC (P0_R75_D4) register bits. The INxM pin can be directly grounded in DC-coupled mode (see Figure 8-14), but the INxM pin must be grounded after the AC-coupling capacitor in AC-coupled mode (see Figure 8-15) for the single-ended input configuration. For the best dynamic range performance, the differential AC-coupled input must be used with the DRE enabled.

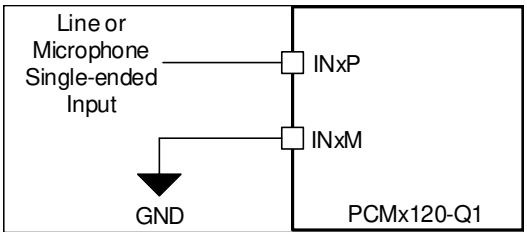


Figure 8-14. Single-Ended, DC-Coupled Input Connection

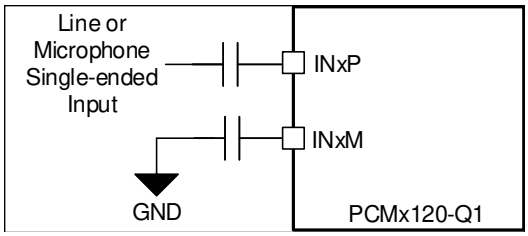


Figure 8-15. Single-Ended, AC-Coupled Input Connection

The device allows for flexibility in choosing the typical input impedance on INxP or INxM from 2.5 kΩ (default), 10 kΩ, and 20 kΩ based on the input source impedance. The higher input impedance results in slightly higher noise or lower dynamic range. Table 8-9 lists the configuration register settings for the input impedance for the record channel.

Table 8-9. Input Impedance Selection for the Record Channel

P0_R60_D[3:2] : CH1_IMP[1:0]	CHANNEL 1 INPUT IMPEDANCE SELECTION
00 (default)	Channel 1 input impedance typical value is 2.5 kΩ on INxP or INxM
01	Channel 1 input impedance typical value is 10 kΩ on INxP or INxM
10	Channel 1 input impedance typical value is 20 kΩ on INxP or INxM
11	Reserved (do not use this setting)

Similarly, the input impedance selection setting for input channel 2 can be configured using the CH2_IMP[1:0] (P0_R65_D[3:2]) register bits.

The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power up. To enable quick charging, the device has modes to speed up the charging of the coupling capacitor. The default value of the quick-charge timing is set for a coupling capacitor up to 1 µF. However, if a higher-value capacitor is used in the system, then the quick-charging timing can be increased by using the INCAP_QCHG (P0_R5_D[5:4]) register bits. For best distortion performance, use the low-voltage coefficient capacitors for AC coupling.

The PCM6120-Q1 can also support a higher input common-mode tolerance at the expense of noise performance by a few decibels. The device supports three different modes with different common-mode tolerances, which can be configured using the CH1_INP_CM_TOL_CFG[1:0] (P0_R58_D[7:6]) register bits. Table 8-10 lists the configuration register settings for the input impedance for the record channel.

Table 8-10. Common-Mode Tolerance Mode Selection for Record Channel

P0_R58_D[7:6] : CH1_INP_CM_TOL_CFG[1:0]	CHANNEL 1 INPUT COMMON-MODE TOLERANCE
00 (default)	Channel 1 input common-mode tolerance of: AC-coupled input = 100 mV_{PP}, DC-coupled input = 2.82 V_{PP}.
01	Channel 1 input common-mode tolerance of: AC/DC-coupled input = 1 V_{PP}.
10 (high CMRR mode)	Channel 1 input common-mode tolerance of: AC/DC-coupled input = 0-AVDD (supported only with an input impedance of 10 kΩ and 20 kΩ). For input impedance of 2.5 kΩ, the input common-mode tolerance is 0.4 V to 2.6 V.
11	Reserved (do not use this setting)

Similarly, the common-mode tolerance setting for input channel 2 can be configured using the CH2_INP_CM_TOL_CFG[1:0] (P0_R58_D[5:4]) register bits. See the *Input Common Mode Tolerance and High CMRR modes for TLV320ADCx120 Devices* application report for further details.

8.3.4 Reference Voltage

All audio data converters require a DC reference voltage. The PCM6120-Q1 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (AVSS).

The value of this reference voltage can be configured using the P0_R59_D[1:0] register bits and must be set to an appropriate value based on the desired full-scale input for the device and the AVDD supply voltage available in the system. The default VREF value is set to 2.75 V, which in turn supports a 2-V_{RMS} differential full-scale input to the device. The required minimum AVDD voltage for this mode is 3 V. Table 8-11 lists the various VREF settings supported along with required AVDD range and the supported full-scale input signal for that configuration.

Table 8-11. VREF Programmable Settings

P0_R59_D[1:0] : ADC_FSCALE[1:0]	VREF OUTPUT VOLTAGE (Same as Internal ADC VREF)	DIFFERENTIAL FULL-SCALE INPUT SUPPORTED	SINGLE-ENDED FULL-SCALE INPUT SUPPORTED	AVDD RANGE REQUIREMENT
00 (default)	2.75 V	2 V_{RMS}	1 V_{RMS}	3 V to 3.6 V
01	2.5 V	1.818 V_{RMS}	0.909 V_{RMS}	2.8 V to 3.6 V
10	1.375 V	1 V_{RMS}	0.5 V_{RMS}	1.7 V to 1.9 V
11	Reserved	Reserved	Reserved	Reserved

To achieve low-power consumption, this audio reference block is powered down as described in the *Section 8.4.1* section. When exiting sleep mode, the audio reference block is powered up using the internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1-µF decoupling capacitor. If a higher-value decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG (P0_R2_D[4:3]) register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

8.3.5 Programmable Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 5 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine tuned for specific microphone combinations.

When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. Table 8-12 shows the available microphone bias programmable options.

Table 8-12. MICBIAS Programmable Settings

P0_R59_D[6:4] : MBIAS_VAL[2:0]	P0_R59_D[1:0] : ADC_FSCALE[1:0]	MICBIAS OUTPUT VOLTAGE
000 (default)	00 (default)	2.75 V (same as the VREF output)
	01	2.5 V (same as the VREF output)
	10	1.375 V (same as the VREF output)
001	00 (default)	3.014 V (1.096 times the VREF output)
	01	2.740 V (1.096 times the VREF output)
	10	1.507 V (1.096 times the VREF output)
010 to 101	XX	Reserved (do not use these settings)
110	XX	Same as AVDD
111	XX	Reserved (do not use this setting)

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ (P0_R117_D7) register bit. Additionally, the device provides an option to configure the GPIO1 or GPIx pin to directly control the microphone bias output powering on or off. This feature is useful to control the microphone directly without engaging the host for I^2C communication. The MICBIAS_PDZ (P0_R117_D7) register bit value is ignored if the GPIO1 or GPIx pin is configured to set the microphone bias on or off.

8.3.6 Signal-Chain Processing

The PCM6120-Q1 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the PCM6120-Q1 optimized for a variety of end-equipments and applications that require multichannel audio capture. Figure 8-16 shows a conceptual block diagram that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain.

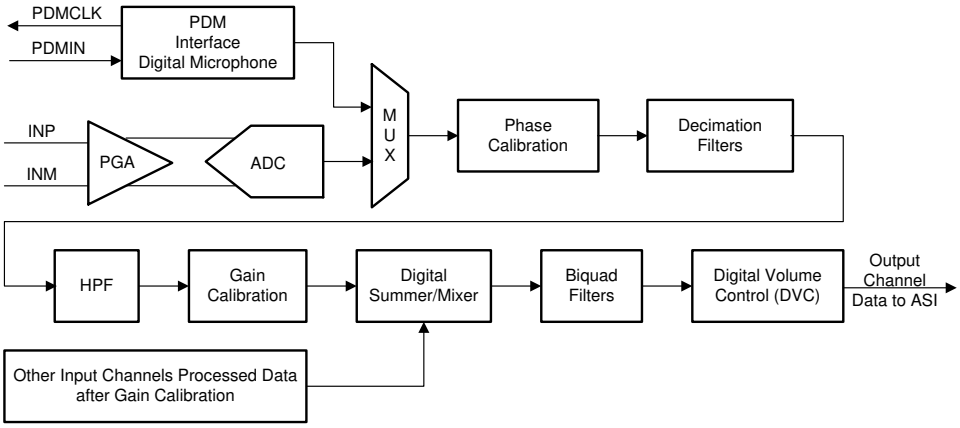


Figure 8-16. Signal-Chain Processing Flowchart

The front-end PGA is very low noise, with a 123 -dB dynamic range performance. Along with a low-noise and low-distortion, multibit, delta-sigma ADC, the front-end PGA enables the PCM6120-Q1 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device also has an integrated programmable biquad filters that allows for custom low-pass, high-pass, or any other desired frequency shaping. Thus, the overall signal chain architecture removes the requirement to add external components for antialiasing low-pass filtering, and thus saves drastically on the external system component cost and board space. See the *TLV320ADCx140 Integrated Analog Anti-Aliasing Filter and Flexible Digital Filter* application report for further details.

The signal chain also consists of various highly programmable digital processing blocks such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, and volume control. The details on these processing blocks are discussed further in this section. The device also supports up to four digital PDM microphone recording channels when the analog record channels are not used. Channels 1 to 2 in the signal chain block diagram of Figure 8-16 are as described in this section, however, channels 3 to 4 only support the digital microphone recording option and do not support the digital summer or mixer option.

The desired input channels for recording can be enabled or disabled by using the IN_CH_EN (P0_R115) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI_OUT_EN (P0_R116) register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel recording is on, then that use case is supported by setting the DYN_CH_PUPD_EN (P0_R117_D4) register bit to 1'b1.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

For output sample rates of 48 kHz or lower, the device supports all features for 4-channel recording and various programmable processing blocks. However, for output sample rates higher than 48 kHz, there are limitations in the number of simultaneous channel recordings supported and the number of biquad filters and such. See the *TLV320ADCx140 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

8.3.6.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each input channel that can be set to the appropriate value based on the maximum input signal expected in the system and the ADC VREF setting used (see the *Section 8.3.4* section), which determines the ADC full-scale signal level.

Configure the desired channel gain setting before powering up the ADC channel and do not change this setting when the ADC is powered on. The programmable range supported for each channel gain is from 0 dB to 42 dB in steps of 0.5 dB. To achieve low-noise performance, the device internal logic first maximizes the gain for the front-end, low-noise analog PGA, which supports a dynamic range of 120 dB, and then applies any residual programmed channel gain in the digital processing block.

Table 8-13 shows the programmable options available for the channel gain.

Table 8-13. Channel Gain Programmable Settings

P0_R61_D[7:1] : CH1_GAIN[6:0]	CHANNEL GAIN SETTING FOR INPUT CHANNEL 1
000 0000 = 0d (default)	Input channel 1 gain is set to 0 dB
000 0001 = 1d	Input channel 1 gain is set to 0.5 dB
000 0010 = 2d	Input channel 1 gain is set to 1 dB
…	…
101 0011 = 83d	Input channel 1 gain is set to 41.5 dB
101 0100 = 84d	Input channel 1 gain is set to 42 dB
101 0101 to 111 1111 = 85d to 127d	Reserved (do not use these settings)

Similarly, the channel gain setting for input channel 2 can be configured using the CH2_GAIN (P0_R66_D[7:1]) register bits. The channel gain feature is not available for the digital microphone record path.

The device also supports gain change when the ADC is enabled. The device supports multiple configurations to limit the audible artifacts during dynamic gain change. This feature can be configured by using the OTF_GAIN_CHANGE_CFG (P0_R113_D[7:6]) register bits.

The device also has a programmable digital volume control with a range from –100 dB to +27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically when the ADC channel is powered up and recording. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang-up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the DVOL_GANG (P0_R108_D7) register bit.

Table 8-14 shows the programmable options available for the digital volume control.

Table 8-14. Digital Volume Control (DVC) Programmable Settings

P0_R62_D[7:0] : CH1_DVOL[7:0]	DVC SETTING FOR OUTPUT CHANNEL 1
0000 0000 = 0d	Output channel 1 DVC is set to mute
0000 0001 = 1d	Output channel 1 DVC is set to –100 dB
0000 0010 = 2d	Output channel 1 DVC is set to –99.5 dB
0000 0011 = 3d	Output channel 1 DVC is set to –99 dB
…	…
1100 1000 = 200d	Output channel 1 DVC is set to –0.5 dB
1100 1001 = 201d (default)	Output channel 1 DVC is set to 0 dB
1100 1010 = 202d	Output channel 1 DVC is set to 0.5 dB
…	…
1111 1101 = 253d	Output channel 1 DVC is set to 26 dB
1111 1110 = 254d	Output channel 1 DVC is set to 26.5 dB
1111 1111 = 255d	Output channel 1 DVC is set to 27 dB

Similarly, the digital volume control setting for output channel 2 to channel 4 can be configured using the CH2_DVOL (P0_R67) to CH4_DVOL (P0_R77) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the DISABLE_SOFT_STEP (P0_R108_D4) register bit.

8.3.6.2 Programmable Channel Gain Calibration

Along with the programmable channel gain and digital volume, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. Table 8-15 shows the programmable options available for the channel gain calibration.

Table 8-15. Channel Gain Calibration Programmable Settings

P0_R63_D[7:4] : CH1_GCAL[3:0]	CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 = 0d	Input channel 1 gain calibration is set to –0.8 dB
0001 = 1d	Input channel 1 gain calibration is set to –0.7 dB
…	…
1000 = 8d (default)	Input channel 1 gain calibration is set to 0 dB
…	…
1110 = 14d	Input channel 1 gain calibration is set to 0.6 dB
1111 = 15d	Input channel 1 gain calibration is set to 0.7 dB

Similarly, the channel gain calibration setting for input channel 2 to channel 4 can be configured using the CH2_GCAL (P0_R68) to CH4_GCAL (P0_R78) register bits, respectively.

8.3.6.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error of the analog microphone. The modulator clock, which is the same clock used for ADC_MOD_CLK, is 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz). For the digital microphone interface, the phase calibration clock is dependent on the PDM clock used. For a PDM_CLK of 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz), the phase calibration clock is the same as PDM_CLK. For a PDM_CLK equal to or lower than 3.072 MHz (the output data sample rate is multiples or submultiples of 48 kHz), the phase calibration clock used is 3.072 MHz. Similarly, for a PDM_CLK of 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (the output data sample rate is multiples or submultiples of 44.1 kHz), and the phase calibration clock used is 2.8224 MHz. This feature is very useful for applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. Table 8-16 shows the available programmable options for channel phase calibration for the analog or digital microphone with a PDM_CLK of 6.144 MHz or 5.6448 MHz.

Table 8-16. Channel Phase Calibration Programmable Settings

P0_R64_D[7:0] : CH1_PCAL[7:0]	CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 0000 = 0d (default)	Input channel 1 phase calibration with no delay
0000 0001 = 1d	Input channel 1 phase calibration delay is set to one cycle of the modulator clock
0000 0010 = 2d	Input channel 1 phase calibration delay is set to two cycles of the modulator clock
…	…
1111 1110 = 254d	Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock
1111 1111 = 255d	Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock

For a digital microphone interface with a PDM_CLK frequency below 3.072 MHz, the phase calibration range is from 0 to 127 of the phase calibration clock (3.072 MHz for the output data sample rate is multiples or submultiples of 48 kHz and 2.8224 MHz for the output data sample rate is multiples or submultiples of 44.1 kHz). This range can be configured using CH1_PCAL[7:1] for channel 1.

Similarly, the channel phase calibration setting for input channel 2 to channel 4 can be configured using the CH2_PCAL (P0_R69) to CH4_PCAL (P0_R79) register bits, respectively.

The phase calibration feature must not be used when the analog input and PDM input are used together for simultaneous conversion.

8.3.6.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. Table 8-17 shows the predefined –3-dB cutoff frequencies available that can be set by using the HPF_SEL[1:0] register bits of P0_R107. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF_SEL[1:0] register bits are set to 2'b00. Figure 8-17 shows a frequency response plot for the HPF filter.

Table 8-17. HPF Programmable Settings

P0_R107_D[1:0] : HPF_SEL[1:0]	-3-dB CUTOFF FREQUENCY SETTING	-3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	-3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
00	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter
01 (default)	$0.00025 \times f_S$	4 Hz	12 Hz
10	$0.002 \times f_S$	32 Hz	96 Hz
11	$0.008 \times f_S$	128 Hz	384 Hz

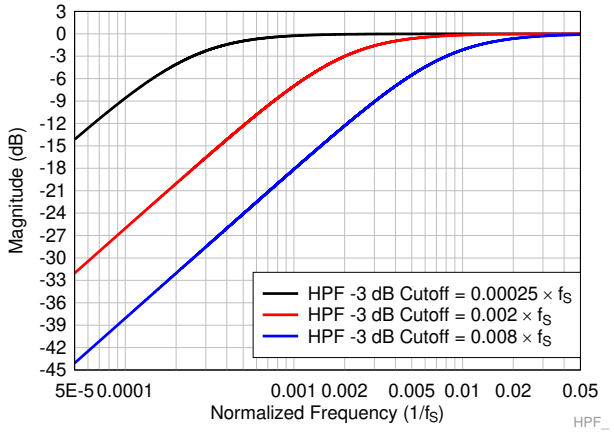


Figure 8-17. HPF Filter Frequency Response Plot

Equation 1 gives the transfer function for the first-order programmable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (1)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in Table 8-18 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any ADC channel for recording. Table 8-18 shows the filter coefficients for the first-order IIR filter.

Table 8-18. 1st-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	DEFAULT COEFFICIENT VALUE	COEFFICIENT REGISTER MAPPING
Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter)	N_0	0x7FFFFFFF	P4_R72-R75
	N_1	0x00000000	P4_R76-R79
	D_1	0x00000000	P4_R80-R83

8.3.6.5 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters. These highly efficient filters achieve the desired frequency response. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. Equation 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{b_0 + 2b_1 z^{-1} + b_2 z^{-2}}{2^{31} - 2a_1 z^{-1} - a_2 z^{-2}} \quad (2)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in *Section 8.6.4.1* and *Section 8.6.4.2* . If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. As described in Table 8-19, these biquad filters can be allocated for each output channel based on the BIQUAD_CFG[1:0] register setting of P0_R108. By setting BIQUAD_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional filtering is required for the system application. See the *TLV320ADCx140 Programmable Biquad Filter Configuration and Applications* application report for further details.

Table 8-19. Biquad Filter Allocation to the Record Output Channel

PROGRAMMABLE BIQUAD FILTER	RECORD OUTPUT CHANNEL ALLOCATION USING P0_R108_D[6:5] REGISTER SETTING		
	BIQUAD_CFG[1:0] = 2'b01 (1 Biquad per Channel)	BIQUAD_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	BIQUAD_CFG[1:0] = 2'b11 (3 Biquads per Channel)
Biquad filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 5	Not used	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 6	Not used	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 7	Not used	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 8	Not used	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 9	Not used	Not used	Allocated to output channel 1
Biquad filter 10	Not used	Not used	Allocated to output channel 2
Biquad filter 11	Not used	Not used	Allocated to output channel 3
Biquad filter 12	Not used	Not used	Allocated to output channel 4

Table 8-20 shows the biquad filter coefficients mapping to the register space.

Table 8-20. Biquad Filter Coefficients Register Mapping

PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING	PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING
Biquad filter 1	P2_R8-R27	Biquad filter 7	P3_R8-R27
Biquad filter 2	P2_R28-R47	Biquad filter 8	P3_R28-R47
Biquad filter 3	P2_R48-R67	Biquad filter 9	P3_R48-R67
Biquad filter 4	P2_R68-R87	Biquad filter 10	P3_R68-R87
Biquad filter 5	P2_R88-R107	Biquad filter 11	P3_R88-R107
Biquad filter 6	P2_R108-R127	Biquad filter 12	P3_R108-R127

8.3.6.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise. Table 8-21 lists the configuration settings available for channel summing mode.

Table 8-21. Channel Summing Mode Programmable Settings

P0_R107_D[3:2] : CH_SUM[1:0]	CHANNEL SUMMING MODE FOR INPUT CHANNELS	SNR AND DYNAMIC RANGE BOOST
00 (default)	Channel summing mode is disabled	Not applicable
01	Output channel 1 = (input channel 1 + input channel 2) / 2	Around 3-dB boost in SNR and dynamic range
	Output channel 2 = (input channel 1 + input channel 2) / 2	
10	Reserved (do not use this setting)	Not applicable
11	Reserved (do not use this setting)	Not applicable

The device additionally supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. The programmable mixer feature is available only if CH_SUM[1:0] is set to 2'b00. The mixer function is supported for all input channels. Figure 8-18 shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the *Section 8.6.4.3* section.

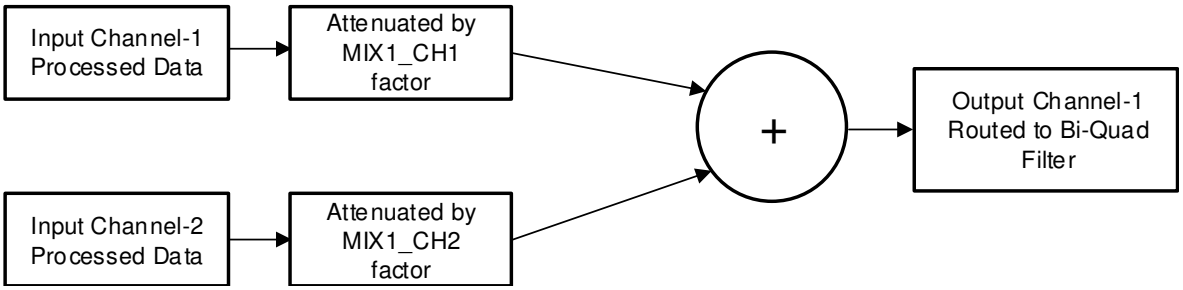


Figure 8-18. Programmable Digital Mixer Block Diagram

A similar mixer operation is performed by mixer 2 to generate output channel 2.

8.3.6.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. As illustrated in Figure 8-16, this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the DECI_FILT (P0_R107_D[5:4]) register bits. Table 8-22 shows the configuration register setting for the decimation filter mode selection for the record channel.

Table 8-22. Decimation Filter Mode Selection for the Record Channel

P0_R107_D[5:4] : DECI_FILT[1:0]	DECIMATION FILTER MODE SELECTION
00 (default)	Linear phase filters are used for the decimation
01	Low latency filters are used for the decimation
10	Ultra-low latency filters are used for the decimation
11	Reserved (do not use this setting)

8.3.6.7.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

8.3.6.7.1.1 Sampling Rate: 7.35 kHz to 8 kHz

Figure 8-19 and Figure 8-20 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 7.35 kHz to 8 kHz. Table 8-23 lists the specifications for a decimation filter with a 7.35-kHz to 8-kHz sampling rate.

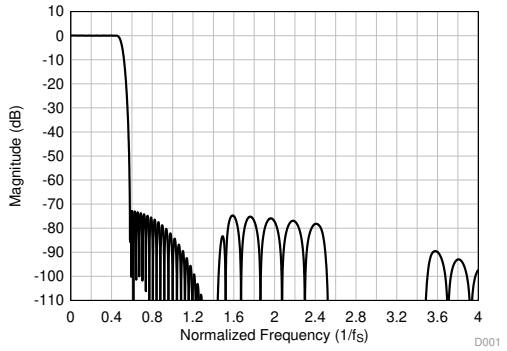


Figure 8-19. Linear Phase Decimation Filter Magnitude Response

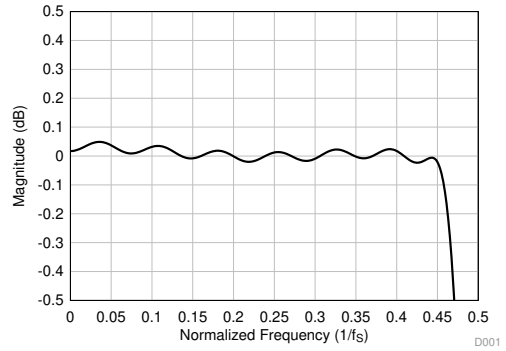


Figure 8-20. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-23. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.6.7.1.2 Sampling Rate: 14.7 kHz to 16 kHz

Figure 8-21 and Figure 8-22 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 14.7 kHz to16 kHz. Table 8-24 lists the specifications for a decimation filter with a 14.7 kHz to 16-kHz sampling rate.

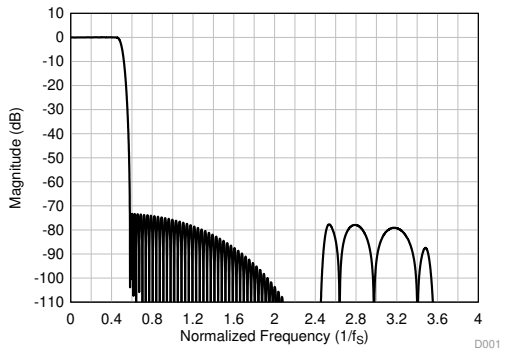


Figure 8-21. Linear Phase Decimation Filter Magnitude Response

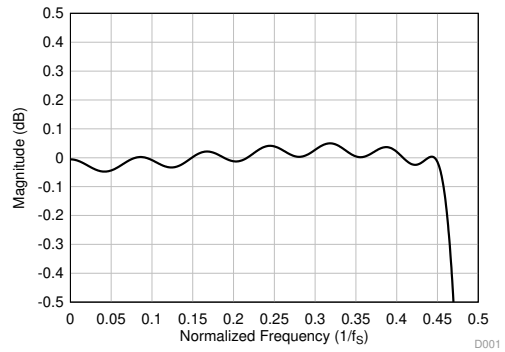


Figure 8-22. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-24. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		1/f_S

8.3.6.7.1.3 Sampling Rate: 22.05 kHz to 24 kHz

Figure 8-23 and Figure 8-24 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 8-25 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

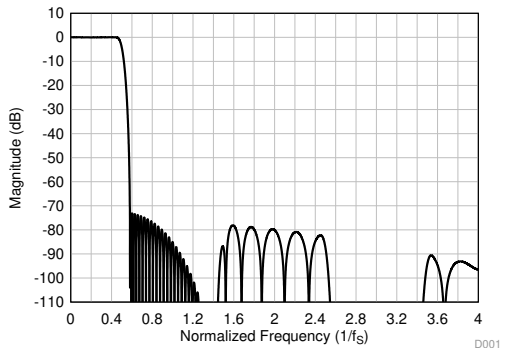


Figure 8-23. Linear Phase Decimation Filter Magnitude Response

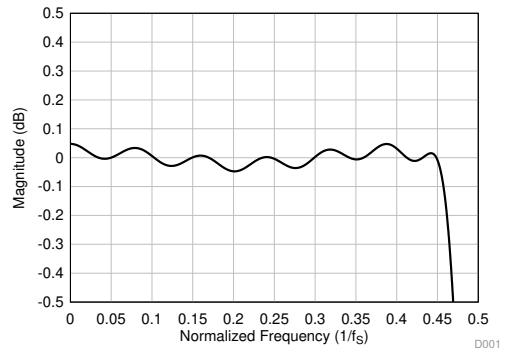


Figure 8-24. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-25. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		1/f_S

8.3.6.7.1.4 Sampling Rate: 29.4 kHz to 32 kHz

Figure 8-25 and Figure 8-26 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 8-26 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

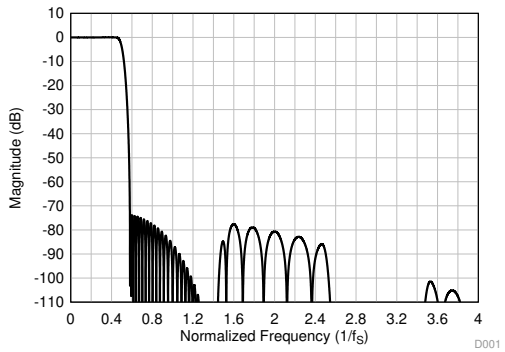


Figure 8-25. Linear Phase Decimation Filter Magnitude Response

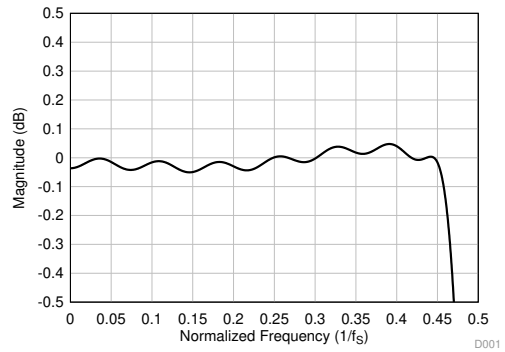


Figure 8-26. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-26. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		1/f_S

8.3.6.7.1.5 Sampling Rate: 44.1 kHz to 48 kHz

Figure 8-27 and Figure 8-28 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 8-27 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

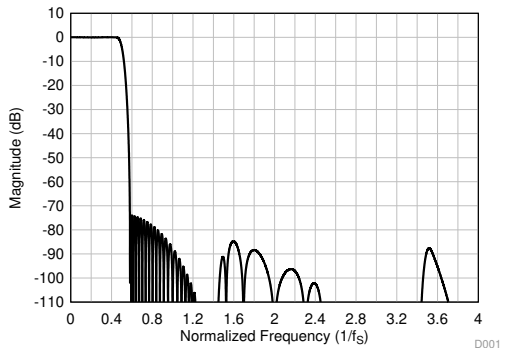


Figure 8-27. Linear Phase Decimation Filter Magnitude Response

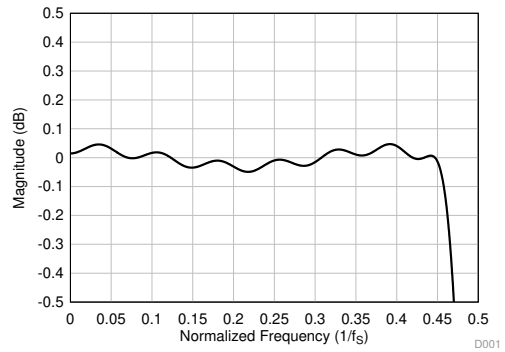


Figure 8-28. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-27. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.6.7.1.6 Sampling Rate: 88.2 kHz to 96 kHz

Figure 8-29 and Figure 8-30 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 8-28 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

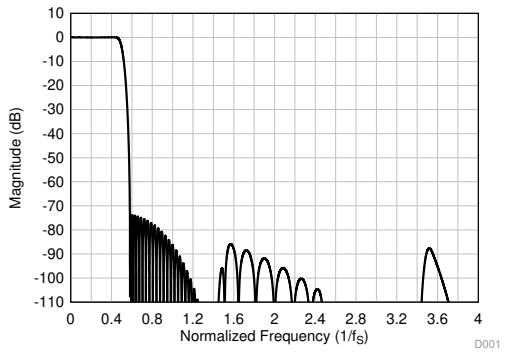


Figure 8-29. Linear Phase Decimation Filter Magnitude Response

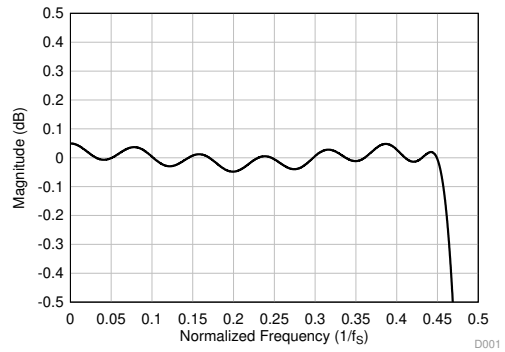


Figure 8-30. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-28. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.6.7.1.7 Sampling Rate: 176.4 kHz to 192 kHz

Figure 8-31 and Figure 8-32 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 8-29 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

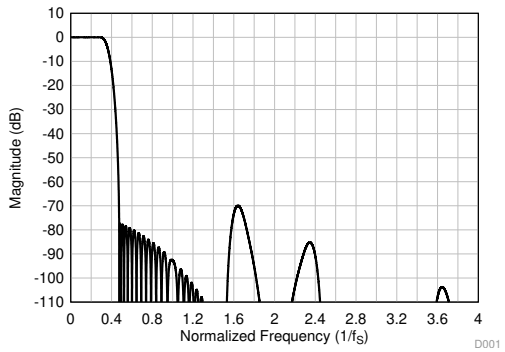


Figure 8-31. Linear Phase Decimation Filter Magnitude Response

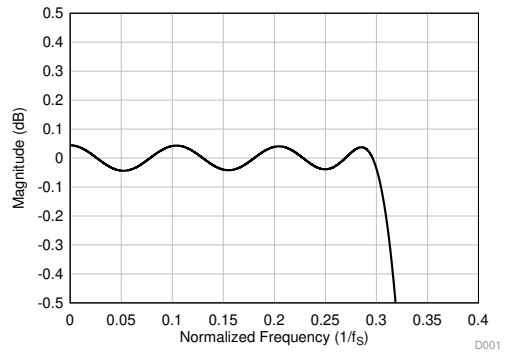


Figure 8-32. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-29. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		1/f_S

8.3.6.7.1.8 Sampling Rate: 352.8 kHz to 384 kHz

Figure 8-33 and Figure 8-34 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. Table 8-30 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

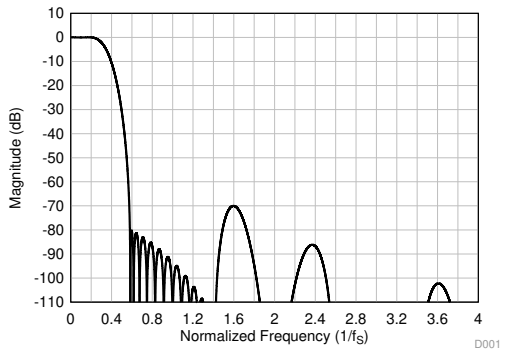


Figure 8-33. Linear Phase Decimation Filter Magnitude Response

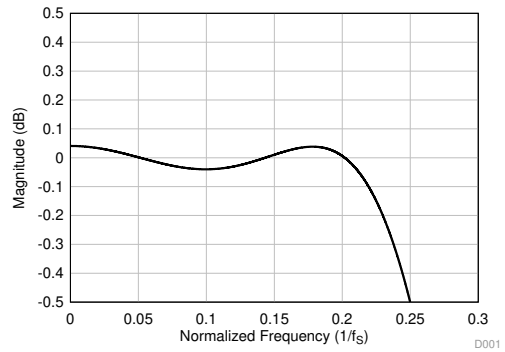


Figure 8-34. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-30. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.212 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	108.8			
Group delay or latency	Frequency range is 0 to 0.212 × f_S		7.2		1/f_S

8.3.6.7.1.9 Sampling Rate: 705.6 kHz to 768 kHz

Figure 8-35 and Figure 8-36 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 705.6 kHz to 768 kHz. Table 8-31 lists the specifications for a decimation filter with a 705.6-kHz to 768-kHz sampling rate.

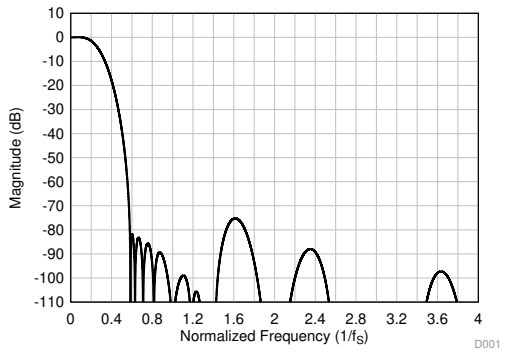


Figure 8-35. Linear Phase Decimation Filter Magnitude Response

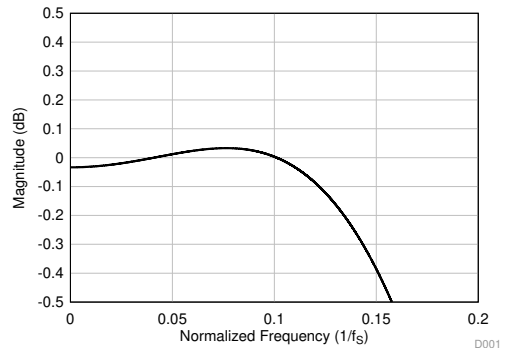


Figure 8-36. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-31. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.113 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 2 × f_S	75.0			dB
	Frequency range is 2 × f_S onwards	88.0			
Group delay or latency	Frequency range is 0 to 0.113 × f_S		5.9		1/f_S

8.3.6.7.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCM6120-Q1 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

8.3.6.7.2.1 Sampling Rate: 14.7 kHz to 16 kHz

Figure 8-37 shows the magnitude response and Figure 8-38 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. Table 8-32 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

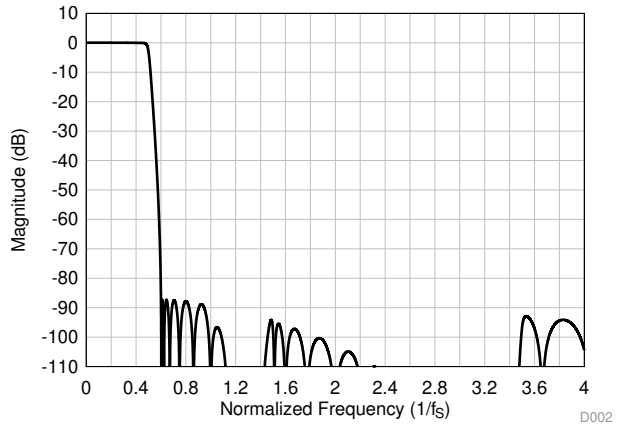


Figure 8-37. Low-Latency Decimation Filter Magnitude Response

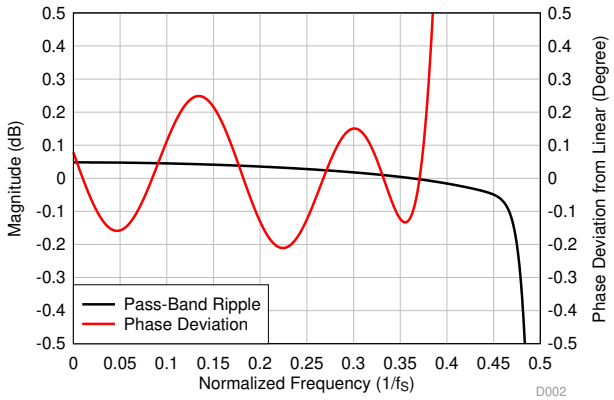


Figure 8-38. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-32. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

8.3.6.7.2.2 Sampling Rate: 22.05 kHz to 24 kHz

Figure 8-39 shows the magnitude response and Figure 8-40 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 8-33 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

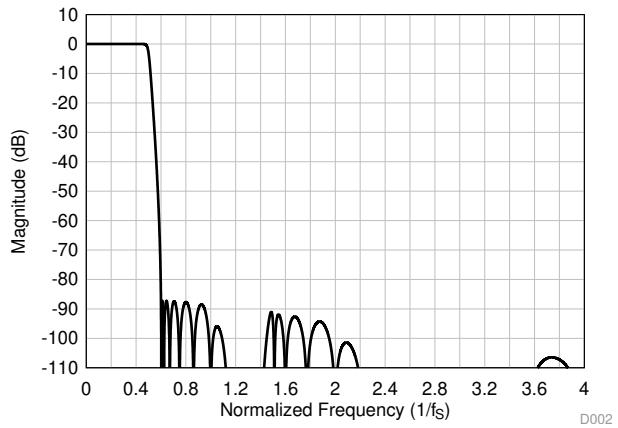


Figure 8-39. Low-Latency Decimation Filter Magnitude Response

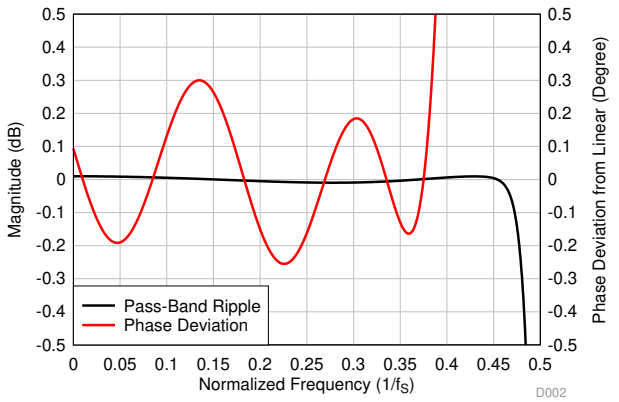


Figure 8-40. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-33. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.6.7.2.3 Sampling Rate: 29.4 kHz to 32 kHz

Figure 8-41 shows the magnitude response and Figure 8-42 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 8-34 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

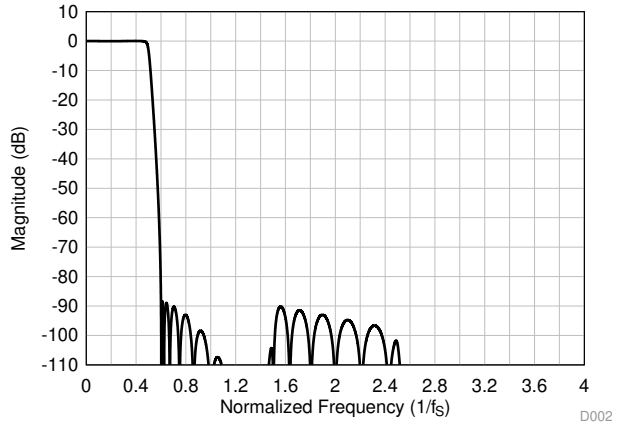


Figure 8-41. Low-Latency Decimation Filter Magnitude Response

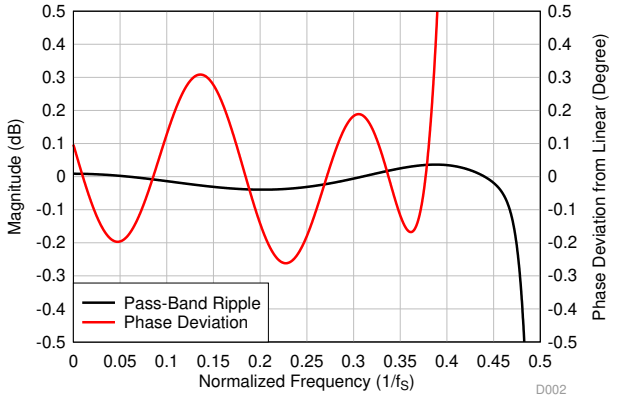


Figure 8-42. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-34. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

8.3.6.7.2.4 Sampling Rate: 44.1 kHz to 48 kHz

Figure 8-43 shows the magnitude response and Figure 8-44 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 8-35 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

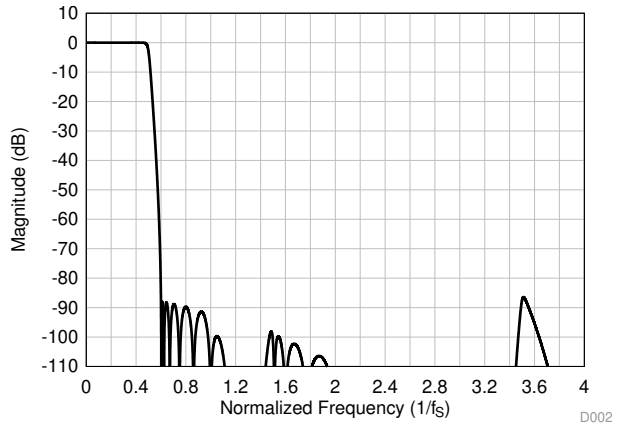


Figure 8-43. Low-Latency Decimation Filter Magnitude Response

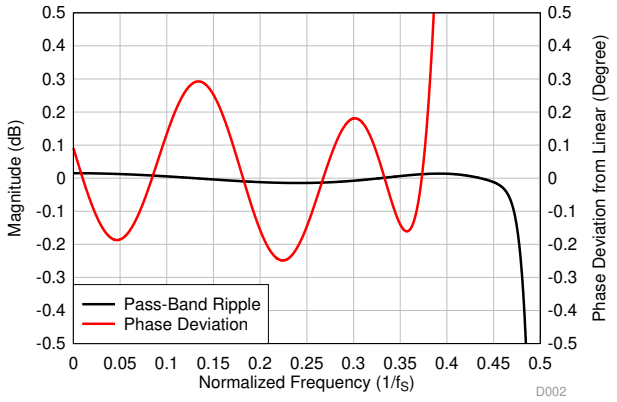


Figure 8-44. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-35. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

8.3.6.7.2.5 Sampling Rate: 88.2 kHz to 96 kHz

Figure 8-45 shows the magnitude response and Figure 8-46 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 8-36 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

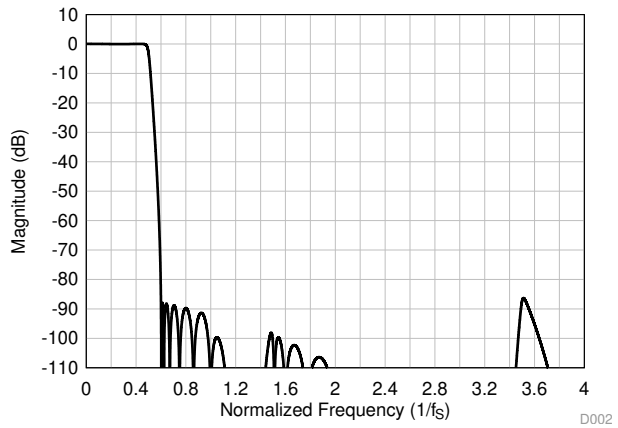


Figure 8-45. Low-Latency Decimation Filter Magnitude Response

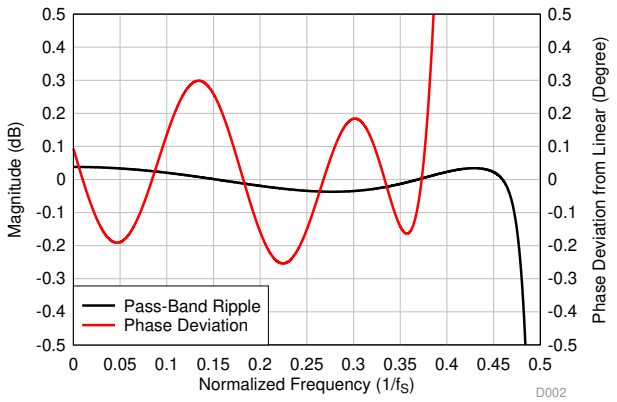


Figure 8-46. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-36. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.6.7.2.6 Sampling Rate: 176.4 kHz to 192 kHz

Figure 8-47 shows the magnitude response and Figure 8-48 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 8-37 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

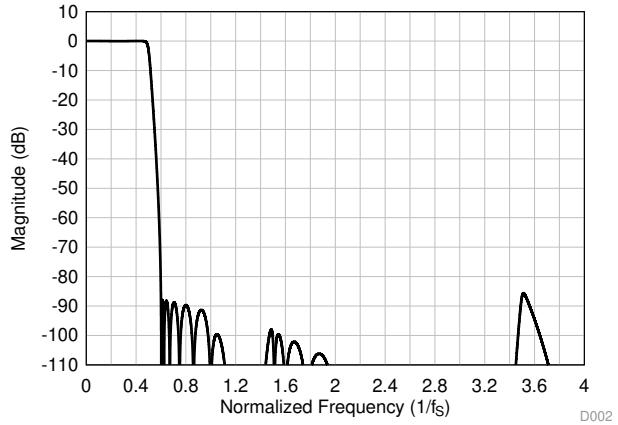


Figure 8-47. Low-Latency Decimation Filter Magnitude Response

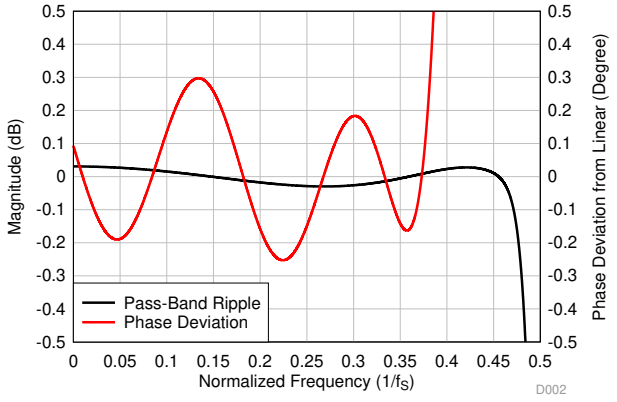


Figure 8-48. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-37. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		1/f_S
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	1/f_S
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.6.7.3 Ultra-Low Latency Filters

For applications where ultra-low latency (within the audio band) is critical, the ultra-low latency decimation filters on the PCM6120-Q1 can be used. The device supports these filters with a group delay of approximately four samples with an almost linear phase response within the 0.325 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the ultra-low latency filters.

8.3.6.7.3.1 Sampling Rate: 14.7 kHz to 16 kHz

Figure 8-49 shows the magnitude response and Figure 8-50 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 14.7 kHz to 16 kHz. Table 8-38 lists the specifications for a decimation filter with a 14.7-kHz to 16-kHz sampling rate.

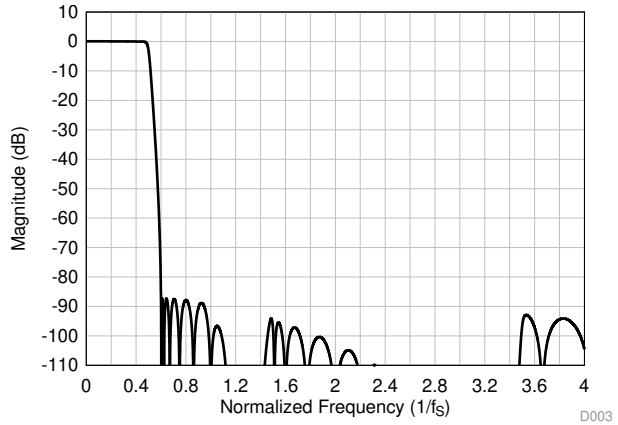


Figure 8-49. Ultra-Low-Latency Decimation Filter Magnitude Response

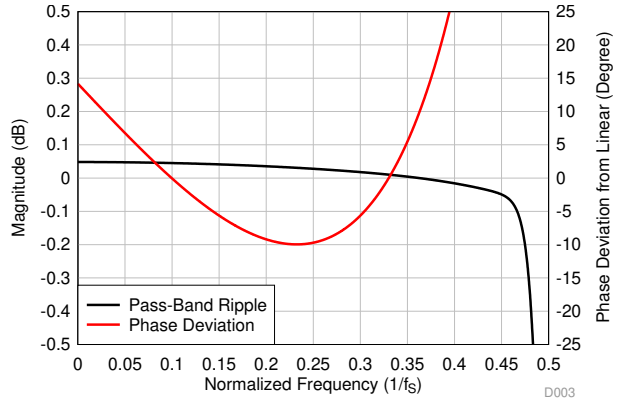


Figure 8-50. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-38. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.45 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.3		1/f_S
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.512		0.512	1/f_S
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.2	Degrees

8.3.6.7.3.2 Sampling Rate: 22.05 kHz to 24 kHz

Figure 8-51 shows the magnitude response and Figure 8-52 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 22.05 kHz to 24 kHz. Table 8-39 lists the specifications for a decimation filter with a 22.05-kHz to 24-kHz sampling rate.

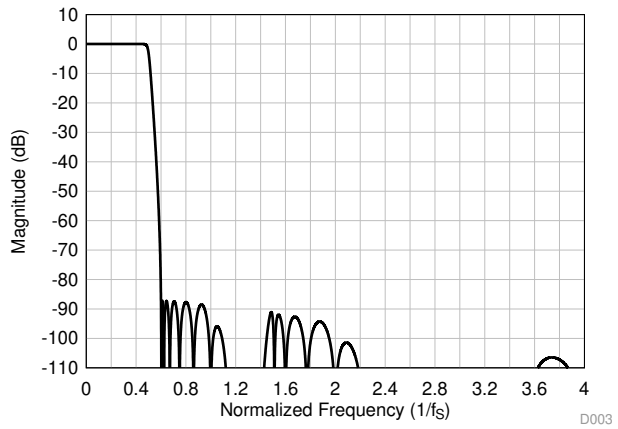


Figure 8-51. Ultra-Low-Latency Decimation Filter Magnitude Response

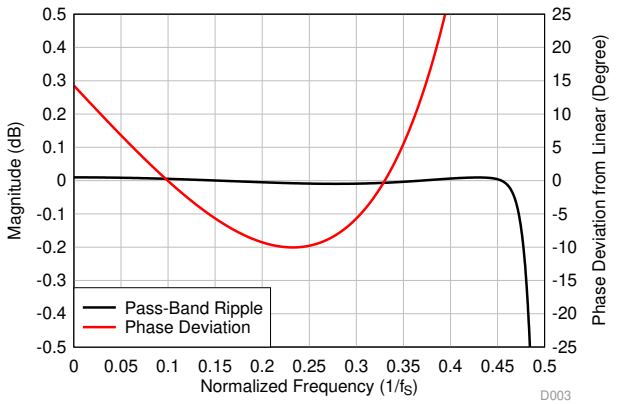


Figure 8-52. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-39. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.46 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.1			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.514		0.514	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.0		14.3	Degrees

8.3.6.7.3.3 Sampling Rate: 29.4 kHz to 32 kHz

Figure 8-53 shows the magnitude response and Figure 8-54 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 29.4 kHz to 32 kHz. Table 8-40 lists the specifications for a decimation filter with a 29.4-kHz to 32-kHz sampling rate.

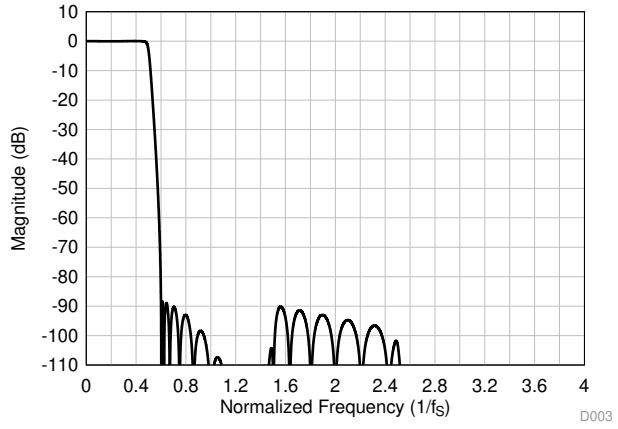


Figure 8-53. Ultra-Low-Latency Decimation Filter Magnitude Response

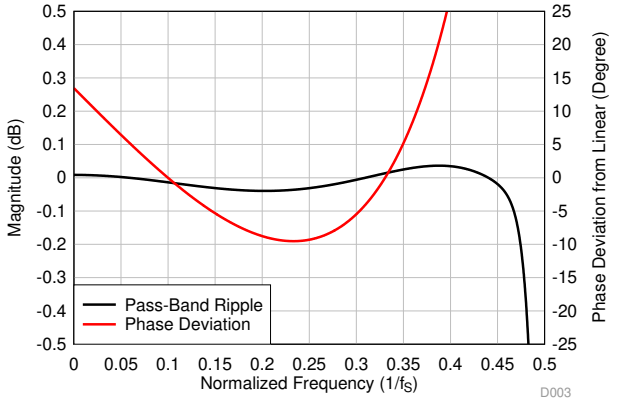


Figure 8-54. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-40. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		5.2		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.492		0.492	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–9.5		13.5	Degrees

8.3.6.7.3.4 Sampling Rate: 44.1 kHz to 48 kHz

Figure 8-55 shows the magnitude response and Figure 8-56 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 44.1 kHz to 48 kHz. Table 8-41 lists the specifications for a decimation filter with a 44.1-kHz to 48-kHz sampling rate.

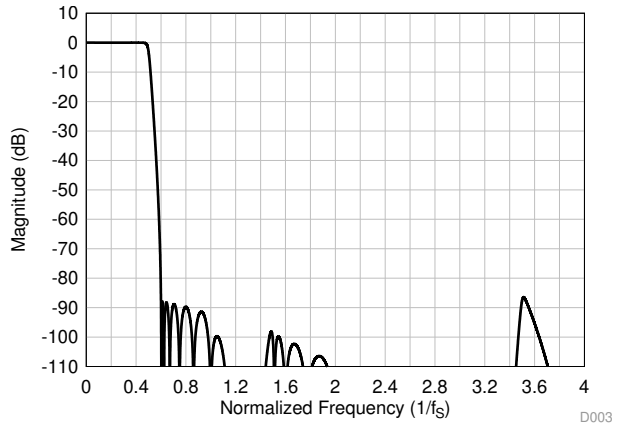


Figure 8-55. Ultra-Low-Latency Decimation Filter Magnitude Response

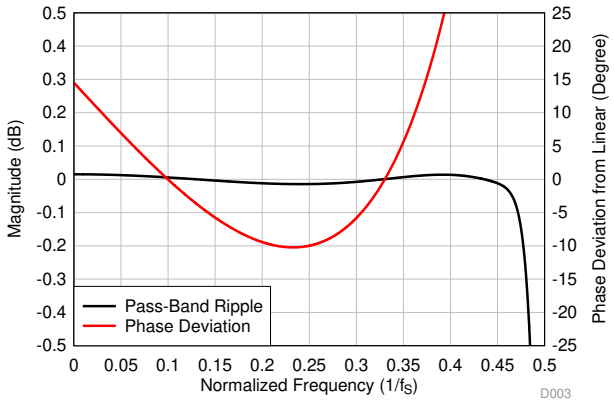


Figure 8-56. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-41. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.325 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.325 × f_S	–0.525		0.525	$1/f_S$
Phase deviation	Frequency range is 0 to 0.325 × f_S	–10.3		14.5	Degrees

8.3.6.7.3.5 Sampling Rate: 88.2 kHz to 96 kHz

Figure 8-57 shows the magnitude response and Figure 8-58 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 88.2 kHz to 96 kHz. Table 8-42 lists the specifications for a decimation filter with an 88.2-kHz to 96-kHz sampling rate.

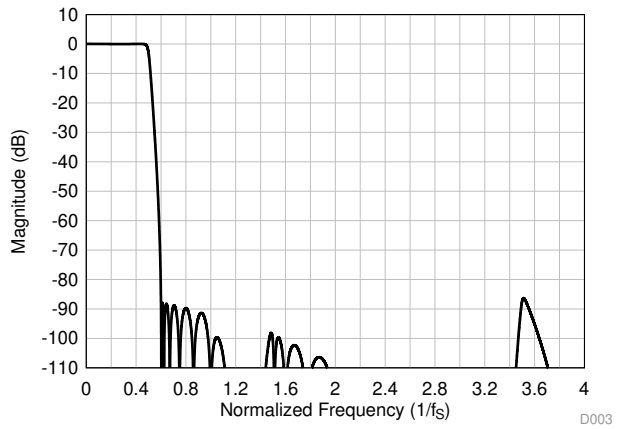


Figure 8-57. Ultra-Low-Latency Decimation Filter Magnitude Response

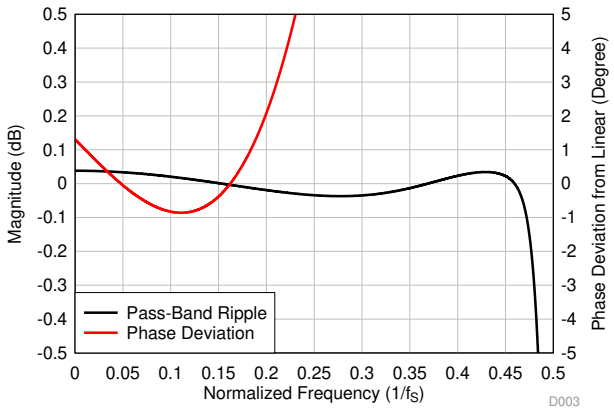


Figure 8-58. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-42. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.1625 × f_S		3.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.1625 × f_S	–0.091		0.091	$1/f_S$
Phase deviation	Frequency range is 0 to 0.1625 × f_S	–0.86		1.30	Degrees

8.3.6.7.3.6 Sampling Rate: 176.4 kHz to 192 kHz

Figure 8-59 shows the magnitude response and Figure 8-60 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 176.4 kHz to 192 kHz. Table 8-43 lists the specifications for a decimation filter with a 176.4-kHz to 192-kHz sampling rate.

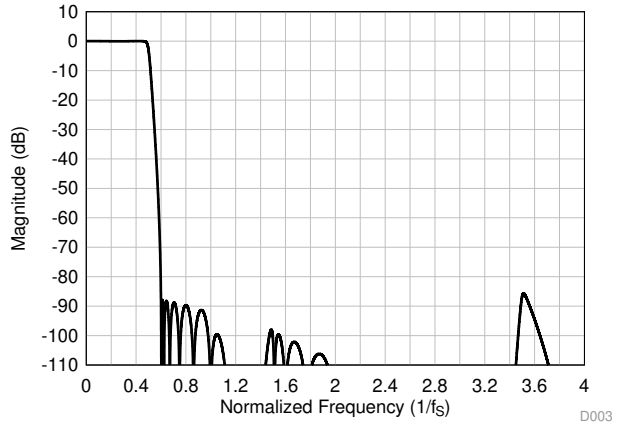


Figure 8-59. Ultra-Low-Latency Decimation Filter Magnitude Response

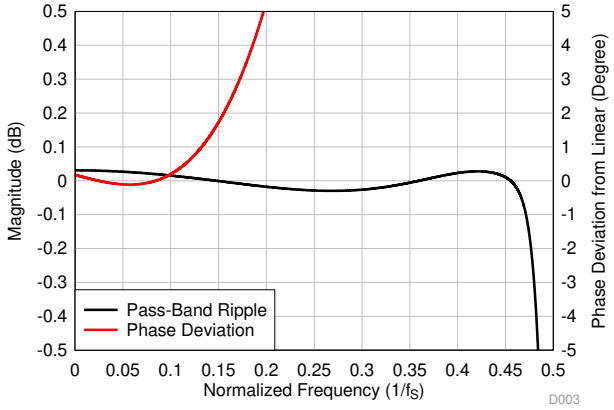


Figure 8-60. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-43. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.463 × f_S	–0.03		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	85.6			dB
Group delay or latency	Frequency range is 0 to 0.085 × f_S		3.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.085 × f_S	–0.024		0.024	$1/f_S$
Phase deviation	Frequency range is 0 to 0.085 × f_S	–0.12		0.18	Degrees

8.3.6.7.3.7 Sampling Rate: 352.8 kHz to 384 kHz

Figure 8-61 shows the magnitude response and Figure 8-62 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 352.8 kHz to 384 kHz. Table 8-44 lists the specifications for a decimation filter with a 352.8-kHz to 384-kHz sampling rate.

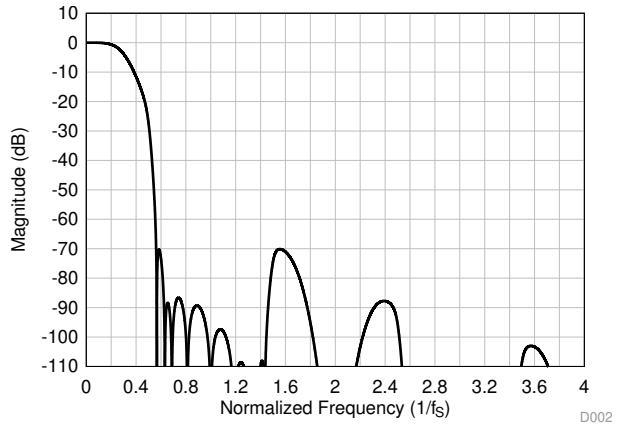


Figure 8-61. Ultra-Low-Latency Decimation Filter Magnitude Response

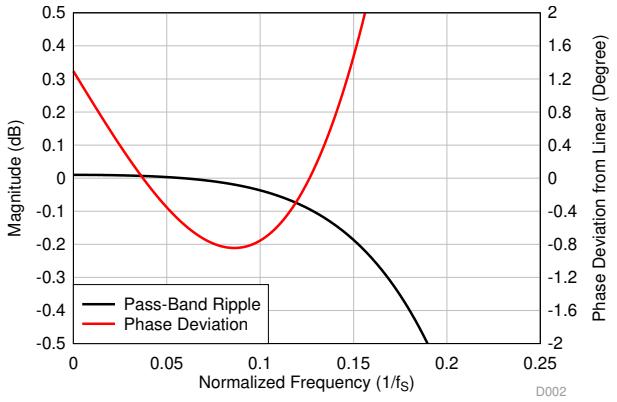


Figure 8-62. Ultra-Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-44. Ultra-Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.1 × f_S	–0.04		0.01	dB
Stop-band attenuation	Frequency range is 0.56 × f_S onwards	70.1			dB
Group delay or latency	Frequency range is 0 to 0.157 × f_S		4.1		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.157 × f_S	–0.18		0.18	$1/f_S$
Phase deviation	Frequency range is 0 to 0.157 × f_S	–0.85		2.07	Degrees

8.3.7 Dynamic Range Enhancer (DRE)

The device integrates an ultra-low noise front-end PGA with 123-dB dynamic range performance with a low-noise, low-distortion, multibit delta-sigma (ΔΣ) ADC with a 113-dB dynamic range. The dynamic range enhancer (DRE) is a digitally assisted algorithm to boost the overall channel performance. The DRE monitors the incoming signal amplitude and accordingly adjusts the internal PGA gain automatically. The DRE achieves a complete-channel dynamic range as high as 123 dB. At a system level, the DRE scheme enables far-field, high-fidelity recording of audio signals in very quiet environments and low-distortion recording in loud environments.

This algorithm is implemented with very low latency and all signal chain blocks are designed to minimize any audible artifacts that may occur resulting from dynamic gain modulation. Additionally, the host can configure the target signal threshold level at which the DRE is triggered by setting the appropriate value for the DRE_LVL[3:0] (P0_R109[7:4]) register bits. The DRE_LVL default level is set to –54 dB and TI recommends setting the DRE_LVL value lower than –30 dB to maximize the benefit of the DRE in real-world applications and to minimize any audible artifacts. Table 8-45 lists the DRE_LVL configuration settings.

Table 8-45. DRE Trigger Threshold Level Programmable Settings

P0_R109_D[7:4] : DRE_LVL[3:0]	DRE TRIGGER THRESHOLD LEVEL
0000	The DRE trigger threshold is the –12-dB input signal level
0001	The DRE trigger threshold is the –18-dB input signal level
0010	The DRE trigger threshold is the –24-dB input signal level
…	…
0111 (default)	The DRE trigger threshold is the –54-dB input signal level
…	…
1001	The DRE trigger threshold is the –66-dB input signal level
1010 to 1111	Reserved (do not use these settings)

The DRE gain range can be dynamically modulated by using the DRE_MAXGAIN[3:0] (P0_R109[3:0]) register bits. The DRE_MAXGAIN default value is set to 24 dB, and the DRE_MAXGAIN value is recommended to be set lower than 24 dB to maximize the benefit of the DRE in real-world applications and to minimize any audible artifacts. Table 8-46 lists the DRE_MAXGAIN configuration settings.

Table 8-46. DRE Maximum Gain Programmable Settings

P0_R109_D[3:0] : DRE_MAXGAIN[3:0]	DRE MAXIMUM GAIN ALLOWED
0000	The DRE maximum gain allowed is 2 dB
0001	The DRE maximum gain allowed is 4 dB
0010	The DRE maximum gain allowed is 6 dB
…	…
1011 (default)	The DRE maximum gain allowed is 24 dB
…	…
1110	The DRE maximum gain allowed is 30 dB
1111	Reserved (do not use this setting)

The DRE scheme is only supported for analog microphone recording channels with an AC-coupled input for best dynamic range performance. The DRE scheme can be independently enabled or disabled for each channel using the CH1_DREEN (P0_R60_D0) and CH2_DREEN (P0_R65_D0) register bits. For a DC-coupled input, the DRE scheme can be used with limited DRE_MAXGAIN depending on the DC differential input common-mode offset.

The DRE configuration registers should be changed only before Power Up of the device. Enabling the DRE for processing increases the power consumption of the device because of increased signal processing. Therefore, disable the DRE for low-power critical applications. Furthermore, the DRE is not supported for output sample rates greater than 192 kHz.

8.3.8 Dynamic Range Compressor (DRC)

The device integrates a dynamic range compressor (DRC) to amplify low-level signals and limits the maximum signal amplitude at the output. This algorithm is implemented with very low latency and all signal chain blocks are designed to minimize any audible artifacts that may occur resulting from dynamic gain modulation. The host can configure the target signal threshold level at which the DRC is triggered by setting the appropriate value for the DRE_LVL[3:0] (P0_R109[7:4]) register bits. Table 8-47 lists the DRE_LVL configuration settings.

Table 8-47. DRC Trigger Threshold Level Programmable Settings

P0_R109_D[7:4] : DRE_LVL[3:0]	DRC TRIGGER THRESHOLD LEVEL
0000	The DRC trigger threshold is the –12-dB input signal level
0001	The DRC trigger threshold is the –18-dB input signal level
0010	The DRC trigger threshold is the –24-dB input signal level
…	…
0111 (default)	The DRC trigger threshold is the –54-dB input signal level
…	…
1001	The DRC trigger threshold is the –66-dB input signal level
1010 to 1111	Reserved (do not use these settings)

The DRC gain range can be dynamically modulated by using the DRE_MAXGAIN[3:0] (P0_R109[3:0]) register bits. Table 8-48 lists the DRE_MAXGAIN configuration settings.

Table 8-48. DRC Maximum Gain Programmable Settings

P0_R109_D[3:0] : DRE_MAXGAIN[3:0]	DRC MAXIMUM GAIN ALLOWED
0000	The DRC maximum gain allowed is 2 dB
0001	The DRC maximum gain allowed is 4 dB
0010	The DRC maximum gain allowed is 6 dB
…	…
1011 (default)	The DRC maximum gain allowed is 24 dB
…	…
1110	The DRC maximum gain allowed is 30 dB
1111	Reserved (do not use this setting)

The DRC scheme is only supported for analog microphone recording channels with an AC-coupled input for best performance. Only one of the AGC, DRC, or DRE features can be enabled at a time. The device can be configured in DRC mode by setting DRC_EN (P0_R108_D1) to 1'b1. The DRC scheme can be independently enabled or disabled for each channel using the CH1_DREEN (P0_R60_D0) and CH2_DREEN (P0_R65_D0) register bits. For a DC-coupled input, the DRC scheme can be used with limited DRE_MAXGAIN depending on the DC differential input common-mode offset.

Only change the DRC configuration registers before powering up the device. Enabling the DRC for processing increases the power consumption of the device because of increased signal processing. Therefore, disable the DRC for low-power critical applications. Furthermore, the DRC is not supported for output sample rates greater than 192 kHz.

8.3.9 Automatic Gain Controller (AGC)

The device includes an automatic gain controller (AGC) for ADC recording. As shown in Figure 8-63, the AGC can be used to maintain a nominally constant output level when recording speech. Instead of manually setting the channel gain in AGC mode, the circuitry automatically adjusts the channel gain when the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters, including target level, maximum gain allowed, attack and release (or decay) time constants, and noise thresholds that allow the algorithm to be fine-tuned for any particular application.

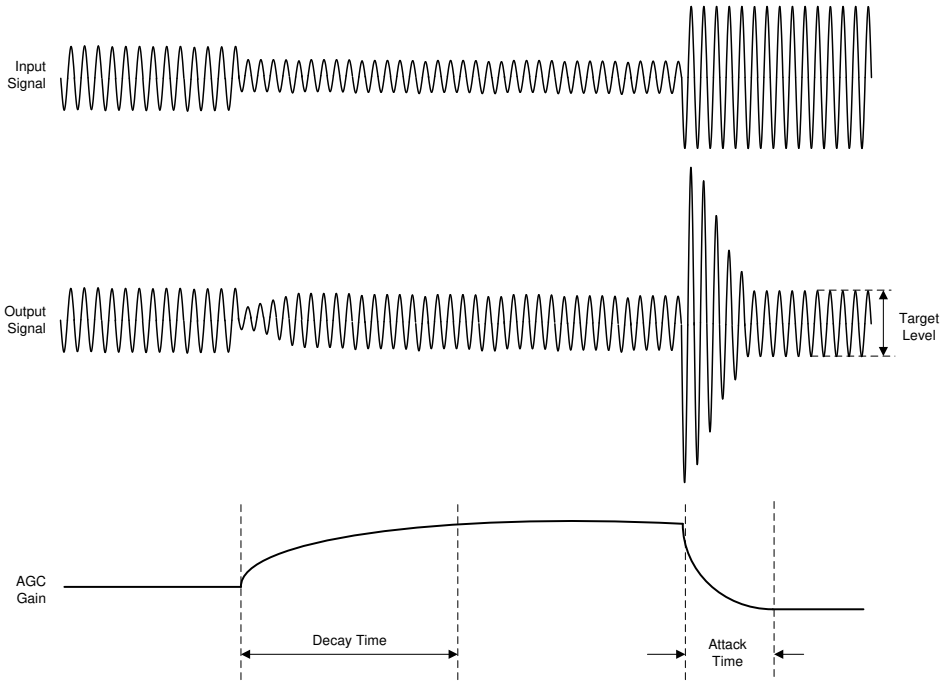


Figure 8-63. AGC Characteristics

The target level (AGC_LVL) represents the nominal approximate output level at which the AGC attempts to hold the ADC output signal level. The PCM6120-Q1 allows programming of different target levels, which can be programmed from –6 dB to –36 dB relative to a full-scale signal, and the AGC_LVL default value is set to –34 dB. The target level is recommended to be set with enough margin to prevent clipping when loud sounds occur. Table 8-49 lists the AGC target level configuration settings.

Table 8-49. AGC Target Level Programmable Settings

P0_R112_D[7:4] : AGC_LVL[3:0]	AGC TARGET LEVEL FOR OUTPUT
0000	The AGC target level is the –6-dB output signal level
0001	The AGC target level is the –8-dB output signal level
0010	The AGC target level is the –10-dB output signal level
…	…
1110 (default)	The AGC target level is the –34-dB output signal level
1111	The AGC target level is the –36-dB output signal level

The maximum gain allowed (AGC_MAXGAIN) gives flexibility to the designer to restrict the maximum gain applied by the AGC. This feature limits the channel gain in situations where environmental noise is greater than the programmed noise threshold. The AGC_MAXGAIN can be programmed from 3 dB to 42 dB with steps of 3 dB and the default value is set to 24 dB. Table 8-50 lists the AGC_MAXGAIN configuration settings.

Table 8-50. AGC Maximum Gain Programmable Settings

P0_R112_D[3:0] : AGC_MAXGAIN[3:0]	AGC MAXIMUM GAIN ALLOWED
0000	The AGC maximum gain allowed is 3 dB
0001	The AGC maximum gain allowed is 6 dB
0010	The AGC maximum gain allowed is 9 dB
…	…
0111 (default)	The AGC maximum gain allowed is 24 dB
…	…
1110	The AGC maximum gain allowed is 39 dB
1111	The AGC maximum gain allowed is 42 dB

For further details on the AGC various configurable parameter and application use, see the *Using the Automatic Gain Controller (AGC) in TLV320ADCx120 Family* application report.

8.3.10 Voice Activity Detection (VAD)

The PCM6120-Q1 supports voice activity detection (VAD) mode. In this mode, the PCM6120-Q1 continuously monitors one of the input channels for voice detection. The device consumes low quiescent current from the AVDD supply in this mode. This feature can be enabled by setting VAD_EN (P0_R117_D0) to 1'b1. On detecting voice activity, the PCM6120-Q1 can alert the host through an interrupt or auto wake up and start recording based on the I^2C programmed configuration. This alert can be configured through the VAD_MODE (P1_R30_D[7:6]) register bits.

This feature is supported on both the analog and digital microphone interfaces. For lowest power VAD, the digital microphone interface is recommended. The input channel for the VAD can be selected by setting the VAD_CH_SEL (P1_R30_D[5:4]) register bits to an appropriate value. See the *Using the Voice Activity Detector (VAD) in the TLV320ADC5120 and TLV320ADC6120* application report for further details.

8.3.11 Digital PDM Microphone Record Channel

In addition to supporting analog microphones, the device also interfaces to digital pulse-density-modulation (PDM) microphones and uses high-order and high-performance decimation filters to generate pulse code modulation (PCM) output data that can be transmitted on the audio serial interface to the host. The device supports up to four digital microphone recording channels. If the second channel analog microphone is not used in the system, then the analog input pins (IN2P and IN2M) can be repurposed as the GPI1 and GPO1 pins, respectively, and can be configured for the PDMDIN1 and PDMCLK clocks for digital PDM microphone recording. GPIO1 or GPI2 (multiplexed with MICBIAS) can be used as PDMDIN2 to enable four-channel PDM microphone recording. If two-channel analog input recording is needed, MICBIAS (configured as GPI2) and GPIO1 can be used as PDMDIN and PDMCLK, respectively, to enable two-channel DMIC recording along with two-channel AIN recording. The device can support a total of four channels at the input (analog and digital).

The device internally generates PDMCLK with a programmable frequency of either 6.144 MHz, 3.072 MHz, 1.536 MHz, or 768 kHz (for output data sample rates in multiples or submultiples of 48 kHz) or 5.6448 MHz, 2.8224 MHz, 1.4112 MHz, or 705.6 kHz (for output data sample rates in multiples or submultiples of 44.1 kHz) using the PDMCLK_DIV[1:0] (P0_R31_D[1:0]) register bits. PDMCLK can be routed on the GPO1 and GPIO1 pins. This clock can be connected to the external digital microphone device. Figure 8-64 shows a connection diagram of the digital PDM microphones.

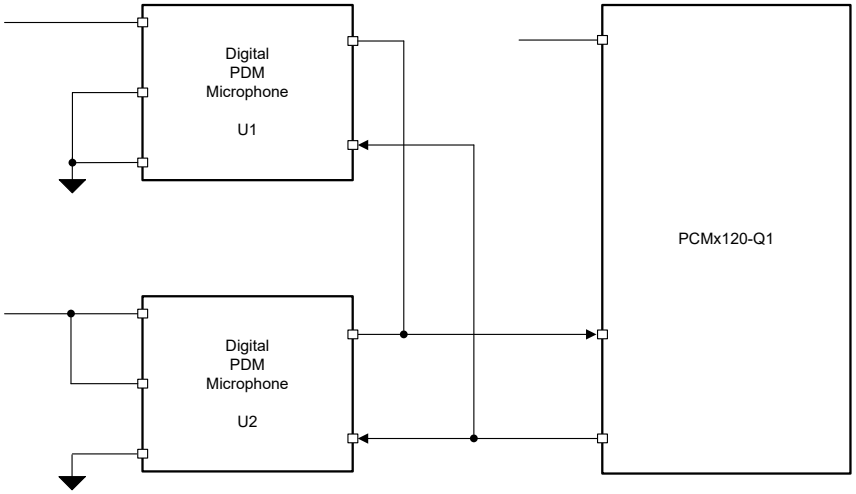


Figure 8-64. Digital PDM Microphones Connection Diagram for the PCM6120-Q1

The single-bit output of the external digital microphone device can be connected to the GPIx pin. This single data line can be shared by two digital microphones to place their data on the opposite edge of PDMCLK. Internally, the device latches the steady value of the data on either the rising or falling edge of PDMCLK based on the configuration register bits set in P0_R32_D[7:4]. Figure 8-65 shows the digital PDM microphone interface timing diagram.

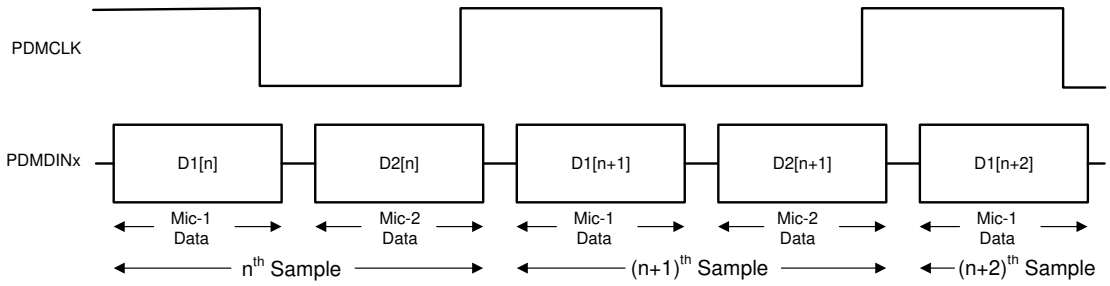


Figure 8-65. Digital PDM Microphone Protocol Timing Diagram

When the digital microphone is used for recording, the analog blocks of the respective ADC channel are powered down and bypassed for power efficiency. Use the CH1_INSRC[1:0] (P0_R60_D[6:5]) and

CH2_INSRC[1:0] (P0_R65_D[6:5]) register bits to select the analog microphone or digital microphone for channel 1 to channel 2. Channel 3 and channel 4 support only the digital microphone interface.

8.3.12 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down the record channel as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the record channel. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7] (P0_R51_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT_LTCH0 (P0_R54), which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIO1 or GPOx pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT_POL (P0_R50_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0] (P0_R50_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV_STS0 (P0_R118) and DEV_STS1 (P0_R119) register bits.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. Additionally, if the channel is not used for analog input recording, then the analog input pins for that channel (INxP and INxM) can be repurposed as multifunction pins (GPIx and GPOx) by configuring the CHx_INSRC[1:0] register bits located in the CHx_CFG0 register. The maximum number of GPO pins supported by the device is four and the maximum number of GPI pins are four. Table 8-51 lists all possible allocations of these multifunctional pins for the various features.

Table 8-51. Multifunction Pin Assignments

ROW	PIN FUNCTION(3)	GPIO1	GPO1	GPI1	GPI2
—	—	GPIO1_CFG	GPO1_CFG	GPI1_CFG	GPI2_CFG
—	—	P0_R33[7:4]	P0_R34[7:4]	P0_R43[6:4]	P0_R43[2:0]
A	Pin disabled	S(1)	S (default)	S (default)	S (default)
B	General-purpose output (GPO)	S	S	NS(2)	NS
C	Interrupt output (IRQ)	S (default)	S	NS	NS
D	Power down for all ADC channels	S	NS	S	S
E	PDM clock output (PDMCLK)	S	S	NS	NS
F	MiCBIAS on/off input (BIASEN)	S	NS	NS	NS
G	General-purpose input (GPI)	S	NS	S	S
H	Master clock input (MCLK)	S	NS	S	S
I	ASI daisy-chain input (SDIN)	S	NS	S	S
J	PDM data input 1 (PDMDIN1)	S	NS	S	S
K	PDM data input 2 (PDMDIN2)	S	NS	S	S

(1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.
(2) NS means the feature mentioned in this row is *not supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.
(3) Only the GPIO1 pin is with reference to the IOVDD supply, the other GPOx and GPIx pins are with reference to the AVDD supply and their primary pin functions are for the PDMCLK or PDMDIN function.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPOx_DRV[3:0] or GPIO1_DRV[3:0] register bits. Table 8-52 lists the drive configuration settings.

Table 8-52. GPIO or GPOx Pins Drive Configuration Settings

P0_R33_D[3:0] : GPIO1_DRV[3:0]	GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1
000	The GPIO1 pin is set to high impedance (floated)
001	The GPIO1 pin is set to be driven active low or active high
010 (default)	The GPIO1 pin is set to be driven active low or weak high (on-chip pullup)
011	The GPIO1 pin is set to be driven active low or Hi-Z (floated)
100	The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high
101	The GPIO1 pin is set to be driven Hi-Z (floated) or active high
110 and 111	Reserved (do not use these settings)

Similarly, the GPO1 pin can be configured using the GPO1_DRV(P0_R34) register bits.

When configured as a general-purpose output (GPO), the GPIO1 or GPOx pin values can be driven by writing the GPIO_VAL or GPOx_VAL (P0_R41) registers. The GPIO_MON (P0_R42) register can be used to readback the status of the GPIO1 pin when configured as a general-purpose input (GPI). Similarly, the GPI_MON (P0_R47) register can be used to readback the status of the GPIx pins when configured as a general-purpose input (GPI).

8.4 Device Functional Modes

8.4.1 Sleep Mode or Software Shutdown

In sleep mode or software shutdown mode, the device consumes very low quiescent current from the AVDD supply and, at the same time, allows the I^2C communication to wake the device for active operation.

The device enters sleep mode when the host device sets the SLEEP_ENZ (P0_R2_D0) bit to 1'b0. If the SLEEP_ENZ bit is asserted low when the device is in active mode, the device ramps down the volume on the record data, powers down the analog and digital blocks, and enters sleep mode. However, the device still continues to retain the last programmed value of the device configuration registers and programmable coefficients.

In sleep mode, do not perform any I^2C transactions, except for exiting sleep mode in order to enter active mode. After entering sleep mode, wait at least 10 ms before starting I^2C transactions to exit sleep mode.

When exiting sleep mode, the host device must configure the PCM6120-Q1 to use either an external 1.8-V AREG supply (default setting) or an on-chip-regulator-generated AREG supply. To configure the AREG supply, write to AREG_SELECT, bit D7 in the same P0_R2 register.

8.4.2 Active Mode

If the host device exits sleep mode by setting the SLEEP_ENZ bit to 1'b1, the device enters active mode. In active mode, I^2C transactions can be done to configure and power-up the device for active operation. After entering active mode, wait at least 1 ms before starting any I^2C transactions in order to allow the device to complete the internal wake-up sequence.

Read and write operations to the programmable coefficient registers in page 2, page 3, and page 4, and to the channel configuration registers (CHx_CFG[1:4]), DRE_CFG0, and AGC_CFG0 in page 0 must be done 10 ms after exiting sleep mode.

After configuring all other registers for the target application and system settings, configure the input and output channel enable registers, IN_CH_EN (P0_R115) and ASI_OUT_CH_EN (P0_R116), respectively. Lastly, configure the device power-up register, PWR_CFG (P0_R117). All programmable coefficient values must be written before powering up the respective channel.

In active mode, the power-up and power-down status of various blocks is monitored by reading the read-only device status bits located in the DEV_STS0 (P0_R117) and DEV_STS1 (P0_R118) registers.

8.4.3 Software Reset

A software reset can be done any time by asserting the SW_RESET (P0_R1_D0) register bit, which is a self-clearing bit. This software reset immediately shuts down the device, and restores all device configuration registers and programmable coefficients to their default values.

8.5 Programming

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. These registers are called *device control registers* and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3, and page 4. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

8.5.1 Control Serial Interfaces

The device control registers can be accessed using I^2C communication to the device. The device operates with a fixed I^2C address and can be configured using this address.

8.5.1.1 I^2C Control Interface

The device supports the I^2C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. The I^2C control protocol requires a 7-bit target address. The 7-bit target address is fixed at 1001110 and cannot be changed. If the I2C_BRDCAST_EN (P0_R2_D2) bit is set to 1'b1, then the I^2C target address is fixed to 1001100 in order to allow simultaneous I^2C broadcast communication to multiple devices in the system, including the PCMx140-Q1, PCMD3140-Q1, and PCMD3180-Q1 devices. Table 8-53 lists the possible device addresses resulting from this configuration.

Table 8-53. I^2C Target Address Settings

I2C_BRDCAST_EN (P0_R2_D2)	I^2C TARGET ADDRESS
0 (default)	1001 110
1	1001 100

8.5.1.1.1 General I^2C Operation

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 8-66 shows a generic data transfer sequence.

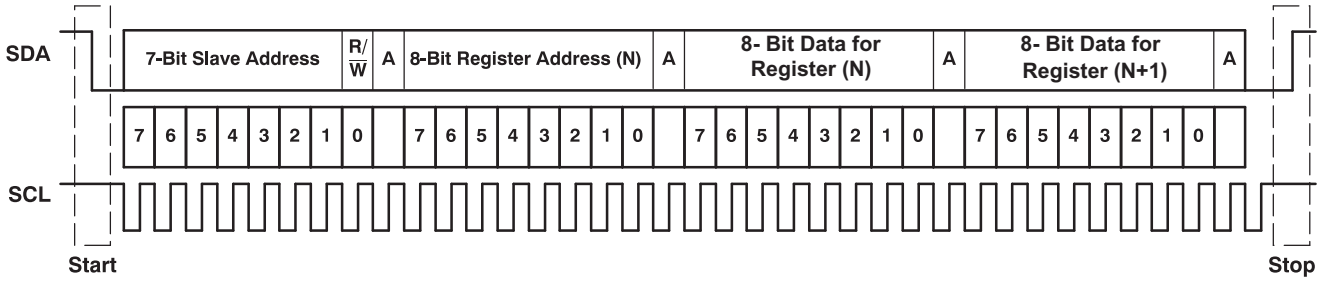


Figure 8-66. Typical I²C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

8.5.1.1.1.1 I²C Single-Byte and Multiple-Byte Transfers

The device I²C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction takes place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

8.5.1.1.1.1.1 I²C Single-Byte Write

As shown in Figure 8-67, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.

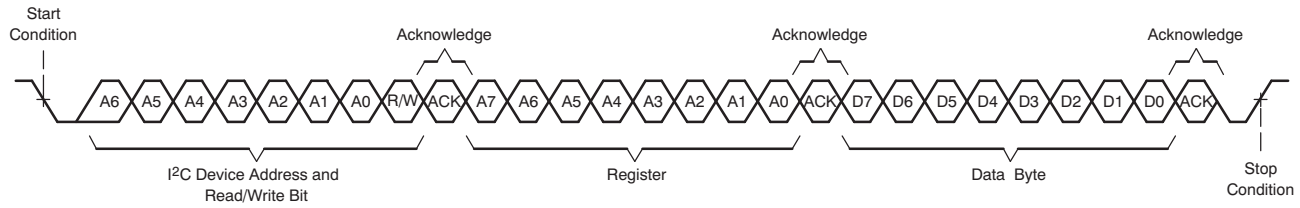


Figure 8-67. I²C Single-Byte Write Transfer

8.5.1.1.1.2 I²C Multiple-Byte Write

As shown in Figure 8-68, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

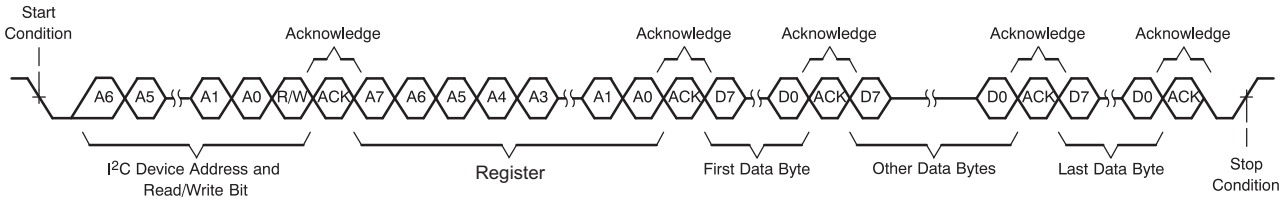


Figure 8-68. I²C Multiple-Byte Write Transfer

8.5.1.1.1.3 I²C Single-Byte Read

As shown in Figure 8-69, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I²C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.

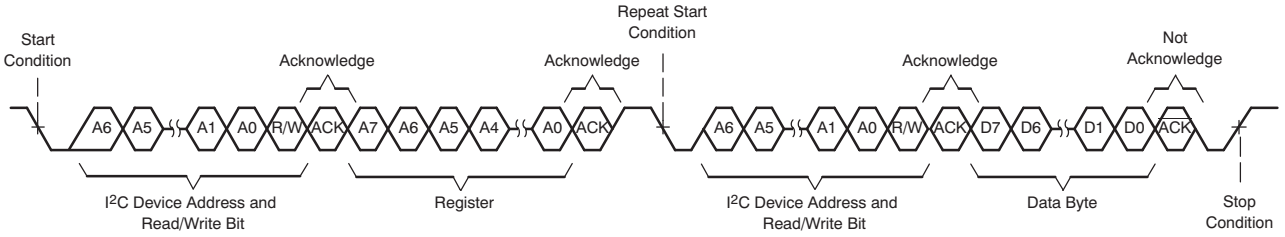


Figure 8-69. I²C Single-Byte Read Transfer

8.5.1.1.1.4 I²C Multiple-Byte Read

As shown in Figure 8-70, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.

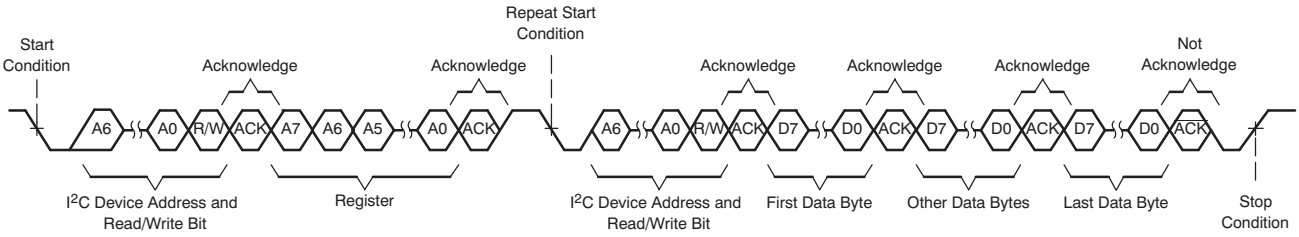


Figure 8-70. I²C Multiple-Byte Read Transfer

8.6 Register Maps

This section describes the control registers for the device in detail. All registers are eight bits in width and are allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using I^2C communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, which is the default page setting at power up (and after a software reset). All programmable coefficient registers are located in page 2, page 3, and page 4. The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

8.6.1 Device Configuration Registers

This section describes the device configuration registers for page 0 and page 1.

8.6.1.1 PCM6120-Q1 Access Codes

Section 8.6.1.1 lists the access codes used for the PCM6120-Q1 registers.

Table 8-54. PCMx120-Q1 Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.6.2 Page 0 Registers

Table 8-55 lists the memory-mapped registers for the Page 0 registers. All register offset addresses not listed in Table 8-55 should be considered as reserved locations and the register contents should not be modified.

Table 8-55. PAGE 0 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 8.6.2.1
0x1	SW_RESET	Software reset register	0x00	Section 8.6.2.2
0x2	SLEEP_CFG	Sleep mode register	0x00	Section 8.6.2.3
0x5	SHDN_CFG	Shutdown configuration register	0x05	Section 8.6.2.4
0x7	ASI_CFG0	ASI configuration register 0	0x30	Section 8.6.2.5
0x8	ASI_CFG1	ASI configuration register 1	0x00	Section 8.6.2.6
0x9	ASI_CFG2	ASI configuration register 2	0x00	Section 8.6.2.7
0xA	ASI_MIX_CFG	ASI input mixing configuration register	0x00	Section 8.6.2.8
0xB	ASI_CH1	Channel 1 ASI slot configuration register	0x00	Section 8.6.2.9
0xC	ASI_CH2	Channel 2 ASI slot configuration register	0x01	Section 8.6.2.10
0xD	ASI_CH3	Channel 3 ASI slot configuration register	0x02	Section 8.6.2.11
0xE	ASI_CH4	Channel 4 ASI slot configuration register	0x03	Section 8.6.2.12
0x13	MST_CFG0	ASI master mode configuration register 0	0x02	Section 8.6.2.13
0x14	MST_CFG1	ASI master mode configuration register 1	0x48	Section 8.6.2.14
0x15	ASI_STS	ASI bus clock monitor status register	0xFF	Section 8.6.2.15
0x16	CLK_SRC	Clock source configuration register 0	0x10	Section 8.6.2.16
0x1F	PDMCLK_CFG	PDM clock generation configuration register	0x40	Section 8.6.2.17
0x20	PDMIN_CFG	PDM DINx sampling edge register	0x00	Section 8.6.2.18
0x21	GPIO_CFG0	GPIO configuration register 0	0x22	Section 8.6.2.19
0x22	GPO_CFG0	GPO configuration register 0	0x00	Section 8.6.2.20
0x29	GPO_VAL	GPIO, GPO output value register	0x00	Section 8.6.2.21
0x2A	GPIO_MON	GPIO monitor value register	0x00	Section 8.6.2.22
0x2B	GPI_CFG0	GPI configuration register 0	0x00	Section 8.6.2.23
0x2F	GPI_MON	GPI monitor value register	0x00	Section 8.6.2.24
0x32	INT_CFG	Interrupt configuration register	0x00	Section 8.6.2.25
0x33	INT_MASK0	Interrupt mask register 0	0xFF	Section 8.6.2.26
0x36	INT_LTCH0	Latched interrupt readback register 0	0x00	Section 8.6.2.27
0x3A	CM_TOL_CFG	ADC common mode configuration register	0x00	Section 8.6.2.28
0x3B	BIAS_CFG	Bias and ADC configuration register	0x00	Section 8.6.2.29
0x3C	CH1_CFG0	Channel 1 configuration register 0	0x00	Section 8.6.2.30
0x3D	CH1_CFG1	Channel 1 configuration register 1	0x00	Section 8.6.2.31
0x3E	CH1_CFG2	Channel 1 configuration register 2	0xC9	Section 8.6.2.32
0x3F	CH1_CFG3	Channel 1 configuration register 3	0x80	Section 8.6.2.33
0x40	CH1_CFG4	Channel 1 configuration register 4	0x00	Section 8.6.2.34
0x41	CH2_CFG0	Channel 2 configuration register 0	0x00	Section 8.6.2.35
0x42	CH2_CFG1	Channel 2 configuration register 1	0x00	Section 8.6.2.36
0x43	CH2_CFG2	Channel 2 configuration register 2	0xC9	Section 8.6.2.37
0x44	CH2_CFG3	Channel 2 configuration register 3	0x80	Section 8.6.2.38
0x45	CH2_CFG4	Channel 2 configuration register 4	0x00	Section 8.6.2.39
0x48	CH3_CFG2	Channel 3 configuration register 2	0xC9	Section 8.6.2.40
0x49	CH3_CFG3	Channel 3 configuration register 3	0x80	Section 8.6.2.41
0x4A	CH3_CFG4	Channel 3 configuration register 4	0x00	Section 8.6.2.42

Table 8-55. PAGE 0 Registers (continued)

Address	Acronym	Register Name	Reset Value	Section
0x4D	CH4_CFG2	Channel 4 configuration register 2	0xC9	Section 8.6.2.43
0x4E	CH4_CFG3	Channel 4 configuration register 3	0x80	Section 8.6.2.44
0x4F	CH4_CFG4	Channel 4 configuration register 4	0x00	Section 8.6.2.45
0x6B	DSP_CFG0	DSP configuration register 0	0x01	Section 8.6.2.46
0x6C	DSP_CFG1	DSP configuration register 1	0x40	Section 8.6.2.47
0x6D	DRE_CFG0	DRE configuration register 0	0x7B	Section 8.6.2.48
0x70	AGC_CFG0	AGC configuration register 0	0xE7	Section 8.6.2.49
0x71	GAIN_CFG	Gain change Configuration	0x00	Section 8.6.2.50
0x73	IN_CH_EN	Input channel enable configuration register	0xC0	Section 8.6.2.51
0x74	ASI_OUT_CH_EN	ASI output channel enable configuration register	0x00	Section 8.6.2.52
0x75	PWR_CFG	Power up configuration register	0x00	Section 8.6.2.53
0x76	DEV_STS0	Device status value register 0	0x00	Section 8.6.2.54
0x77	DEV_STS1	Device status value register 1	0x80	Section 8.6.2.55
0x7E	I2C_CKSUM	I^2C checksum register	0x00	Section 8.6.2.56

8.6.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in Table 8-56.

Return to the Table 8-55.

The device memory map is divided into pages. This register sets the page.

Table 8-56. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

8.6.2.2 SW_RESET Register (Address = 0x1) [Reset = 0x00]

SW_RESET is shown in Table 8-57.

Return to the Table 8-55.

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

Table 8-57. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits; Write only reset value
0	SW_RESET	R/W	0b	Software reset. This bit is self clearing. 0d = Do not reset 1d = Reset all registers to their reset values

8.6.2.3 SLEEP_CFG Register (Address = 0x2) [Reset = 0x00]

SLEEP_CFG is shown in Table 8-58.

Return to the Table 8-55.

This register configures the regulator, VREF quick charge, I2C broadcast and sleep mode.

Table 8-58. SLEEP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AREG_SELECT	R/W	0b	The analog supply selection from either the internal regulator supply or the external AREG supply. 0d = External 1.8-V AREG supply (use this setting when AVDD is 1.8 V and short AREG with AVDD) 1d = Internally generated 1.8-V AREG supply using an on-chip regulator (use this setting when AVDD is 3.3 V)
6-5	RESERVED	R/W	00b	Reserved bits; Write only reset values
4-3	VREF_QCHG[1:0]	R/W	00b	The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)
2	I2C_BRDCAST_EN	R/W	0b	I2C broadcast addressing setting. 0d = I2C broadcast mode disabled 1d = I2C broadcast mode enabled; the I2C target address is fixed at 1001 100
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	SLEEP_ENZ	R/W	0b	Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode

8.6.2.4 SHDN_CFG Register (Address = 0x5) [Reset = 0x05]

SHDN_CFG is shown in Table 8-59.

Return to the Table 8-55.

This register configures the device shutdown

Table 8-59. SHDN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-4	INCAP_QCHG[1:0]	R/W	00b	The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω. 0d = INxP, INxM quick-charge duration of 2.5 ms (typical) 1d = INxP, INxM quick-charge duration of 12.5 ms (typical) 2d = INxP, INxM quick-charge duration of 25 ms (typical) 3d = INxP, INxM quick-charge duration of 50 ms (typical)
3-2	RESERVED	R/W	01b	Reserved bits; Write only reset values
1-0	RESERVED	R/W	01b	Reserved bits; Write only reset values

8.6.2.5 ASI_CFG0 Register (Address = 0x7) [Reset = 0x30]

ASI_CFG0 is shown in Table 8-60.

Return to the Table 8-55.

This register is the ASI configuration register 0.

Table 8-60. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_FORMAT[1:0]	R/W	00b	ASI protocol format. 0d = TDM mode 1d = I^2S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use
5-4	ASI_WLEN[1:0]	R/W	11b	ASI word or slot length. 0d = 16 bits (Recommended this setting to be used with 10-kΩ or 20-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	FSYNC_POL	R/W	0b	ASI FSYNC polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	BCLK_POL	R/W	0b	ASI BCLK polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	TX_EDGE	R/W	0b	ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
0	TX_FILL	R/W	0b	ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles

8.6.2.6 ASI_CFG1 Register (Address = 0x8) [Reset = 0x00]

ASI_CFG1 is shown in Table 8-61.

Return to the Table 8-55.

This register is the ASI configuration register 1.

Table 8-61. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_LSB	R/W	0b	ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
6-5	TX_KEEPER[1:0]	R/W	00b	ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles

Table 8-61. ASI_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TX_OFFSET[4:0]	R/W	00000b	ASI data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

8.6.2.7 ASI_CFG2 Register (Address = 0x9) [Reset = 0x00]

ASI_CFG2 is shown in Table 8-62.

Return to the Table 8-55.

This register is the ASI configuration register 2.

Table 8-62. ASI_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_DAISY	R/W	0b	ASI daisy chain connection. 0d = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus. This is supported only if ASI input mixing is disabled, refer register 10 for details on ASI input mixing feature.
6	RESERVED	R	0b	Reserved bit; Write only reset value
5	ASI_ERR	R/W	0b	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
4	ASI_ERR_RCOV	R/W	0b	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2-0	RESERVED	R	000b	Reserved bits; Write only reset value

8.6.2.8 ASI_MIX_CFG Register (Address = 0xA) [Reset = 0x00]

ASI_MIX_CFG is shown in Table 8-63.

Return to the Table 8-55.

This register is the ASI input mixing configuration register.

Table 8-63. ASI_MIX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_MIX_SEL[1:0]	R/W	00b	ASI input (from GPIx or GPIO) mixing selection with channel data. 0d = No mixing 1d = Channel 1 and channel 2 output data mixed with ASI input data on channel 1 (slot 0) 2d = Channel 1 and channel 2 output data mixed with ASI input data on channel 2 (slot 1) 3d = Mixed both channel data with ASI input data independently. Mixed asi_in_ch_1 with channel 1 output data and similarly mix asi_in_ch_2 with channel 2 output data
5-4	ASI_GAIN_SEL[1:0]	R/W	00b	ASI input data gain selection before mixing to channel data. 0d = No gain 1d = Gain asi input data by -6dB 2d = Gain asi input data by -12dB 3d = Gain asi input data by -18dB
3	ASI_IN_INVERSE	R/W	0b	Invert ASI input data before mixing to channel data. 0d = No inversion done for ASI input data 1d = ASI input data inverted before mixing with channel data
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.2.9 ASI_CH1 Register (Address = 0xB) [Reset = 0x00]

ASI_CH1 is shown in Table 8-64.

Return to the Table 8-55.

This register is the ASI slot configuration register for channel 1.

Table 8-64. ASI_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH1_SLOT[5:0]	R/W	000000b	Channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

8.6.2.10 ASI_CH2 Register (Address = 0xC) [Reset = 0x01]

ASI_CH2 is shown in Table 8-65.

Return to the Table 8-55.

This register is the ASI slot configuration register for channel 2.

Table 8-65. ASI_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value

Table 8-65. ASI_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CH2_SLOT[5:0]	R/W	000001b	Channel 2 slot assignment. 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is left slot 31 32d = TDM is slot 32 or I²S, LJ is right slot 0 33d = TDM is slot 33 or I²S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I²S, LJ is right slot 31

8.6.2.11 ASI_CH3 Register (Address = 0xD) [Reset = 0x02]

ASI_CH3 is shown in Table 8-66.

Return to the Table 8-55.

This register is the ASI slot configuration register for channel 3.

Table 8-66. ASI_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH3_SLOT[5:0]	R/W	000010b	Channel 3 slot assignment. 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is left slot 31 32d = TDM is slot 32 or I²S, LJ is right slot 0 33d = TDM is slot 33 or I²S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I²S, LJ is right slot 31

8.6.2.12 ASI_CH4 Register (Address = 0xE) [Reset = 0x03]

ASI_CH4 is shown in Table 8-67.

Return to the Table 8-55.

This register is the ASI slot configuration register for channel 4.

Table 8-67. ASI_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits; Write only reset value
5-0	CH4_SLOT[5:0]	R/W	000011b	Channel 4 slot assignment. 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is left slot 31 32d = TDM is slot 32 or I²S, LJ is right slot 0 33d = TDM is slot 33 or I²S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I²S, LJ is right slot 31

8.6.2.13 MST_CFG0 Register (Address = 0x13) [Reset = 0x02]

MST_CFG0 is shown in Table 8-68.

Return to the Table 8-55.

This register is the ASI master mode configuration register 0.

Table 8-68. MST_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MST_SLV_CFG	R/W	0b	ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device) 1d = Device is in master mode (both BCLK and FSYNC are generated from the device)
6	AUTO_CLK_CFG	R/W	0b	Automatic clock configuration setting. 0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived) 1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings)
5	AUTO_MODE_PLL_DIS	R/W	0b	Automatic mode PLL setting. 0d = PLL is enabled in auto clock configuration 1d = PLL is disabled in auto clock configuration
4	BCLK_FSYNC_GATE	R/W	0b	BCLK and FSYNC clock gate (valid when the device is in master mode). 0d = Do not gate BCLK and FSYNC 1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode
3	FS_MODE	R/W	0b	Sample rate setting (valid when the device is in master mode). 0d = f_S is a multiple (or submultiple) of 48 kHz 1d = f_S is a multiple (or submultiple) of 44.1 kHz
2-0	MCLK_FREQ_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz

8.6.2.14 MST_CFG1 Register (Address = 0x14) [Reset = 0x48]

MST_CFG1 is shown in Table 8-69.

Return to the Table 8-55.

This register is the ASI master mode configuration register 1.

Table 8-69. MST_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE[3:0]	R/W	0100b	Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 15d = Reserved; Don't use

Table 8-69. MST_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	FS_BCLK_RATIO[3:0]	R/W	1000b	Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d to 15d = Reserved; Don't use

8.6.2.15 ASI_STS Register (Address = 0x15) [Reset = 0xFF]

ASI_STS is shown in Table 8-70.

Return to the Table 8-55.

This register s the ASI bus clock monitor status register

Table 8-70. ASI_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FS_RATE_STS[3:0]	R	1111b	Detected sample rate of the ASI bus. 0d = 7.35 kHz or 8 kHz 1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz 9d to 14d = Reserved status 15d = Invalid sample rate
3-0	FS_RATIO_STS[3:0]	R	1111b	Detected BCLK to FSYNC frequency ratio of the ASI bus. 0d = Ratio of 16 1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048 13d to 14d = Reserved status 15d = Invalid ratio

8.6.2.16 CLK_SRC Register (Address = 0x16) [Reset = 0x10]

CLK_SRC is shown in Table 8-71.

Return to the Table 8-55.

This register is the clock source configuration register.

Table 8-71. CLK_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_PLL_SLV_CLK_SRC	R/W	0b	Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1). 0d = BCLK is used as the audio root clock source 1d = MCLK (GPIO or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting)
6	MCLK_FREQ_SEL_MODE	R/W	0b	Master mode MCLK (GPIO or GPIx) frequency selection mode (valid when the device is in auto clock configuration). 0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R19) configuration 1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R22) configuration
5-3	MCLK_RATIO_SEL[2:0]	R/W	010b	These bits select the MCLK (GPIO or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode. 0d = Ratio of 64 1d = Ratio of 256 2d = Ratio of 384 3d = Ratio of 512 4d = Ratio of 768 5d = Ratio of 1024 6d = Ratio of 1536 7d = Ratio of 2304
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	INV_BCLK_FOR_FSYNC	R/W	0b	Invert BCLK polarity only for FSYNC generation in master mode configuration. 0d = Do not invert BCLK polarity for FSYNC generation 1d = Invert BCLK polarity for FSYNC generation
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

8.6.2.17 PDMCLK_CFG Register (Address = 0x1F) [Reset = 0x40]

PDMCLK_CFG is shown in Table 8-72.

Return to the Table 8-55.

This register is the PDM clock generation configuration register.

Table 8-72. PDMCLK_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6-2	RESERVED	R/W	10000b	Reserved bits; Write only reset values
1-0	PDMCLK_DIV[1:0]	R/W	00b	PDMCLK divider value. 0d = PDMCLK is 2.8224 MHz or 3.072 MHz 1d = PDMCLK is 1.4112 MHz or 1.536 MHz 2d = PDMCLK is 705.6 kHz or 768 kHz 3d = PDMCLK is 5.6448 MHz or 6.144 MHz (applicable only for PDM channel 1 and 2)

8.6.2.18 PDMIN_CFG Register (Address = 0x20) [Reset = 0x00]

PDMIN_CFG is shown in Table 8-73.

Return to the Table 8-55.

This register is the PDM DINx sampling edge configuration register.

Table 8-73. PDMIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDMDIN1_EDGE	R/W	0b	PDMCLK latching edge used for channel 1 and channel 2 data. 0d = Channel 1 data are latched on the negative edge, channel 2 data are latched on the positive edge 1d = Channel 1 data are latched on the positive edge, channel 2 data are latched on the negative edge
6	RESERVED	R/W	0b	Reserved bit; Write only reset value
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

8.6.2.19 GPIO_CFG0 Register (Address = 0x21) [Reset = 0x22]

GPIO_CFG0 is shown in Table 8-74.

Return to the Table 8-55.

This register is the GPIO configuration register 0.

Table 8-74. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	R/W	0010b	GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = Reserved; Don't use 4d = GPIO1 is configured as a PDM clock output (PDMCLK) 5d = Reserved; Don't use 6d = Reserved; Don't use 7d = PD all ADC channels 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 12d = GPIO1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 13d = GPIO1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 14d to 15d = Reserved; Don't use
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPIO1_DRV[2:0]	R/W	010b	GPIO1 output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

8.6.2.20 GPO_CFG0 Register (Address = 0x22) [Reset = 0x00]

GPO_CFG0 is shown in Table 8-75.

Return to the Table 8-55.

This registeris the GPO configuration register 0.

Table 8-75. GPO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_CFG[3:0]	R/W	0000b	IN2M_GPO1 (GPO1) configuration. 0d = GPO1 is disabled 1d = GPO1 is configured as a general-purpose output (GPO) 2d = GPO1 is configured as a device interrupt output (IRQ) 3d = Reserved; Don't use 4d = GPO1 is configured as a PDM clock output (PDMCLK) 5d to 15d = Reserved; Don't use
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPO1_DRV[2:0]	R/W	000b	IN2M_GPO1 (GPO1) output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Reserved; Don't use 3d = Drive active low and Hi-Z 4d = Reserved; Don't use 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

8.6.2.21 GPO_VAL Register (Address = 0x29) [Reset = 0x00]

GPO_VAL is shown in Table 8-76.

Return to the Table 8-55.

This register is the GPIO and GPO output value register.

Table 8-76. GPO_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_VAL	R/W	0b	GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
6	GPO1_VAL	R/W	0b	GPO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

8.6.2.22 GPIO_MON Register (Address = 0x2A) [Reset = 0x00]

GPIO_MON is shown in Table 8-77.

Return to the Table 8-55.

This register is the GPIO monitor value register.

Table 8-77. GPIO_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_MON	R	0b	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6-0	RESERVED	R	0000000b	Reserved bits; Write only reset value

8.6.2.23 GPI_CFG0 Register (Address = 0x2B) [Reset = 0x00]

GPI_CFG0 is shown in Table 8-78.

Return to the Table 8-55.

This register is the GPI configuration register 0.

Table 8-78. GPI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6-4	GPI1_CFG[2:0]	R/W	000b	IN2P_GPI1 (GPI1) configuration. 0d = GPI1 is disabled 1d = GPI1 is configured as a general-purpose input (GPI) 2d = GPI1 is configured as a master clock input (MCLK) 3d = GPI1 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 4d = GPI1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 5d = GPI1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 6d = Reserved; Don't use 7d = PD all ADC channels
3	RESERVED	R	0b	Reserved bit; Write only reset value
2-0	GPI2_CFG[2:0]	R/W	000b	MICBIAS as GPI2 configuration. 0d = GPI2 is disabled 1d = GPI2 is configured as a general-purpose input (GPI) 2d = GPI2 is configured as a master clock input (MCLK) 3d = GPI2 is configured as an ASI input for daisy-chain or ASI input for mixing (SDIN) 4d = GPI2 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 5d = GPI2 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 6d = Reserved; Don't use 7d = PD all ADC channels

8.6.2.24 GPI_MON Register (Address = 0x2F) [Reset = 0x00]

GPI_MON is shown in Table 8-79.

Return to the Table 8-55.

This regiser is the GPI monitor value register.

Table 8-79. GPI_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPI1_MON	R	0b	GPI1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
6	GPI2_MON	R	0b	GPI2 monitor value when MICBIAS is configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

8.6.2.25 INT_CFG Register (Address = 0x32) [Reset = 0x00]

INT_CFG is shown in Table 8-80.

Return to the Table 8-55.

This regiser is the interrupt configuration register.

Table 8-80. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	R/W	0b	Interrupt polarity. 0d = Active low (IRQZ) 1d = Active high (IRQ)

Table 8-80. INT_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	INT_EVENT[1:0]	R/W	00b	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event Dont use 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	RESERVED	R	00b	Reserved bits; Write only reset value
2	LTCH_READ_CFG	R/W	0b	Interrupt latch registers readback configuration. 0d = All interrupts can be read through the LTCH registers 1d = Only unmasked interrupts can be read through the LTCH registers
1-0	RESERVED	R	00b	Reserved bits; Write only reset value

8.6.2.26 INT_MASK0 Register (Address = 0x33) [Reset = 0xFF]

INT_MASK0 is shown in Table 8-81.

Return to the Table 8-55.

This register is the interrupt masks register 0.

Table 8-81. INT_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0	R/W	1b	ASI clock error mask. 0d = Do not mask 1d = Mask
6	INT_MASK0	R/W	1b	PLL Lock interrupt mask. 0d = Do not mask 1d = Mask
5	INT_MASK0	R/W	1b	ASI input mixing saturation alert mask. 0d = Do not mask 1d = Mask
4	INT_MASK0	R/W	1b	VAD Power up detect interrupt mask. 0d = Do not mask 1d = Mask
3	INT_MASK0	R/W	1b	VAD Power down detect interrupt mask. 0d = Do not mask 1d = Mask
2	RESERVED	R/W	1b	Reserved bit; Write only reset value
1	RESERVED	R/W	1b	Reserved bit; Write only reset value
0	RESERVED	R/W	1b	Reserved bit; Write only reset value

8.6.2.27 INT_LTCH0 Register (Address = 0x36) [Reset = 0x00]

INT_LTCH0 is shown in Table 8-82.

Return to the Table 8-55.

This register is the latched Interrupt readback register 0.

Table 8-82. INT_LTCH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0	R	0b	Interrupt caused by an ASI bus clock error (self-clearing bit). 0d = No interrupt 1d = Interrupt

Table 8-82. INT_LTCH0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_LTCH0	R	0b	Interrupt caused by PLL LOCK (self-clearing bit). 0d = No interrupt 1d = Interrupt
5	INT_LTCH0	R	0b	Interrupt caused by ASI input mixing channel saturation alert (self clearing bit). 0d = No interrupt 1d = Interrupt
4	INT_LTCH0	R	0b	Interrupt caused by VAD power up detect (self clearing bit). 0d = No interrupt 1d = Interrupt
3	INT_LTCH0	R	0b	Interrupt caused by VAD power down detect (self clearing bit). 0d = No interrupt 1d = Interrupt
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

8.6.2.28 CM_TOL_CFG Register (Address = 0x3A) [Reset = 0x00]

CM_TOL_CFG is shown in Table 8-83.

Return to the Table 8-55.

This register is the ADC common mode configuration register

Table 8-83. CM_TOL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH1_INP_CM_TOL_CFG[1:0]	R/W	00b	Channel 1 input common mode variance tolerance configuration. 0d = Common mode variance tolerance for AC coupled = 100 mVpp and DC coupled = 2.82 Vpp 1d = Common Mode Tolerance of: AC/DC Coupled Input=1V peak to peak 2d = Common Mode Tolerance of: AC/DC Coupled Input=0-AVDD(Supported only with Input Impendance of 10 kΩ/20 kΩ). For input impedance of 2.5 kΩ, input common mode tolerance= 0.4V to 2.6V. 3d = Reserved; Don't use
5-4	CH2_INP_CM_TOL_CFG[1:0]	R/W	00b	Channel 2 input common mode variance tolerance configuration. 0d = Common mode variance tolerance for AC coupled = 100 mVpp and DC coupled = 2.82 Vpp 1d = Common Mode Tolerance of: AC/DC Coupled Input=1V peak to peak 2d = Common Mode Tolerance of: AC/DC Coupled Input=0-AVDD(Supported only with Input Impendance of 10 kΩ/20 kΩ). For input impedance of 2.5 kΩ, input common mode tolerance= 0.4V to 2.6V. 3d = Reserved; Don't use
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.29 BIAS_CFG Register (Address = 0x3B) [Reset = 0x00]

BIAS_CFG is shown in Table 8-84.

Return to the Table 8-55.

This register is the bias and ADC configuration register

Table 8-84. BIAS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bit; Write only reset value
6-4	MBIAS_VAL[2:0]	R/W	000b	MICBIAS value. 0d = Microphone bias is set to VREF (2.750 V, 2.500 V, or 1.375 V) 1d = Microphone bias is set to VREF x 1.096 (3.014 V, 2.740 V, or 1.507 V) 2d = Microphone bias is set to VCM = IN1M, for ADC single-ended configuration 3d = Microphone bias is set to VCM = IN2M, for ADC single-ended configuration 4d = Microphone bias is set to VCM = average of IN1M and IN2M, for ADC single-ended configuration 5d = Microphone bias is set to VCM = internal crude common mode 6d = Microphone bias is set to AVDD 7d = MICBIAS configured as GPI2
3-2	RESERVED	R	00b	Reserved bits; Write only reset value
1-0	ADC_FSCALE[1:0]	R/W	00b	ADC full-scale setting (configure this setting based on the AVDD supply minimum voltage used). 0d = VREF is set to 2.75 V to support 2 V_{RMS} for the differential input or 1 V_{RMS} for the single-ended input 1d = VREF is set to 2.5 V to support 1.818 V_{RMS} for the differential input or 0.909 V_{RMS} for the single-ended input 2d = VREF is set to 1.375 V to support 1 V_{RMS} for the differential input or 0.5 V_{RMS} for the single-ended input 3d = Reserved; Don't use

8.6.2.30 CH1_CFG0 Register (Address = 0x3C) [Reset = 0x00]

CH1_CFG0 is shown in Table 8-85.

Return to the Table 8-55.

This register is configuration register 0 for channel 1.

Table 8-85. CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_INTYP	R/W	0b	Channel 1 input type. 0d = Microphone input 1d = Line input
6-5	CH1_INSRC[1:0]	R/W	00b	Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK) 3d = Reserved; Don't use
4	CH1_DC	R/W	0b	Channel 1 input coupling (applicable for the analog input). 0d = AC-coupled input 1d = DC-coupled input
3-2	CH1_IMP[1:0]	R/W	00b	Channel 1 input impedance (applicable for the analog input). 0d = Typical 2.5-kΩ input impedance 1d = Typical 10-kΩ input impedance 2d = Typical 20-kΩ input impedance 3d = Reserved; Don't use
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	CH1_DREEN	R/W	0b	Channel 1 dynamic range enhancer (DRE) and automatic gain controller (AGC) setting. 0d = DRE / AGC / DRC disabled 1d = DRE or AGC or DRC enabled based on the configuration of bit 3 in register 108 (P0_R108)

8.6.2.31 CH1_CFG1 Register (Address = 0x3D) [Reset = 0x00]

CH1_CFG1 is shown in Table 8-86.

Return to the Table 8-55.

This register is configuration register 1 for channel 1.

Table 8-86. CH1_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CH1_GAIN[6:0]	R/W	0000000b	Channel 1 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 0.5 dB 2d = Channel gain is set to 1 dB 3d to 83d = Channel gain is set as per configuration 84d = Channel gain is set to 42 dB 85d to 127d = Reserved; Don't use
0	CH1_GAIN_SIGN_BIT	R/W	0b	Channel-1 gain sign configuration. 0d = Positive channel gain 1d = Negative channel gain (minimum channel gain supported till -11 dB; supported only for channel input impedance of 10-kΩ and 20-kΩ)

8.6.2.32 CH1_CFG2 Register (Address = 0x3E) [Reset = 0xC9]

CH1_CFG2 is shown in Table 8-87.

Return to the Table 8-55.

This register is configuration register 2 for channel 1.

Table 8-87. CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_DVOL[7:0]	R/W	11001001b	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.2.33 CH1_CFG3 Register (Address = 0x3F) [Reset = 0x80]

CH1_CFG3 is shown in Table 8-88.

Return to the Table 8-55.

This register is configuration register 3 for channel 1.

Table 8-88. CH1_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH1_GCAL[3:0]	R/W	1000b	Channel 1 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB

Table 8-88. CH1_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.34 CH1_CFG4 Register (Address = 0x40) [Reset = 0x00]

CH1_CFG4 is shown in Table 8-89.

Return to the Table 8-55.

This register is configuration register 4 for channel 1.

Table 8-89. CH1_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PCAL[7:0]	R/W	00000000b	Channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.2.35 CH2_CFG0 Register (Address = 0x41) [Reset = 0x00]

CH2_CFG0 is shown in Table 8-90.

Return to the Table 8-55.

This register is configuration register 0 for channel 2.

Table 8-90. CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH2_INTYP	R/W	0b	Channel 2 input type. 0d = Microphone input 1d = Line input
6-5	CH2_INSRC[1:0]	R/W	00b	Channel 2 input configuration. 0d = Analog differential input (the GPI1 and GPO1 pin functions must be disabled) 1d = Analog single-ended input (the GPI1 and GPO1 pin functions must be disabled) 2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK) 3d = Reserved; Don't use
4	CH2_DC	R/W	0b	Channel 2 input coupling (applicable for the analog input). 0d = AC-coupled input 1d = DC-coupled input
3-2	CH2_IMP[1:0]	R/W	00b	Channel 2 input impedance (applicable for the analog input). 0d = Typical 2.5-kΩ input impedance 1d = Typical 10-kΩ input impedance 2d = Typical 20-kΩ input impedance 3d = Reserved; Don't use
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	CH2_DREEN	R/W	0b	Channel 2 dynamic range enhancer (DRE) and automatic gain controller (AGC) setting. 0d = DRE / AGC / DRC disabled 1d = DRE or AGC or DRC enabled based on the configuration of bit 3 in register 108 (P0_R108)

8.6.2.36 CH2_CFG1 Register (Address = 0x42) [Reset = 0x00]

CH2_CFG1 is shown in Table 8-91.

Return to the Table 8-55.

This register is configuration register 1 for channel 2.

Table 8-91. CH2_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CH2_GAIN[6:0]	R/W	0000000b	Channel 2 gain. 0d = Channel gain is set to 0 dB 1d = Channel gain is set to 0.5 dB 2d = Channel gain is set to 1 dB 3d to 83d = Channel gain is set as per configuration 84d = Channel gain is set to 42 dB 85d to 127d = Reserved; Don't use
0	CH2_GAIN_SIGN_BIT	R/W	0b	Channel-2 gain sign configuration. 0d = Positive channel gain 1d = Negative channel gain (minimum channel gain supported till -11 dB; supported only for channel input impedance of 10-kΩ and 20-kΩ)

8.6.2.37 CH2_CFG2 Register (Address = 0x43) [Reset = 0xC9]

CH2_CFG2 is shown in Table 8-92.

Return to the Table 8-55.

This register is configuration register 2 for channel 2.

Table 8-92. CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_DVOL[7:0]	R/W	11001001b	Channel 2 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.2.38 CH2_CFG3 Register (Address = 0x44) [Reset = 0x80]

CH2_CFG3 is shown in Table 8-93.

Return to the Table 8-55.

This register is configuration register 3 for channel 2.

Table 8-93. CH2_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH2_GCAL[3:0]	R/W	1000b	Channel 2 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB

Table 8-93. CH2_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.39 CH2_CFG4 Register (Address = 0x45) [Reset = 0x00]

CH2_CFG4 is shown in Table 8-94.

Return to the Table 8-55.

This register is configuration register 4 for channel 2.

Table 8-94. CH2_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PCAL[7:0]	R/W	00000000b	Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.2.40 CH3_CFG2 Register (Address = 0x48) [Reset = 0xC9]

CH3_CFG2 is shown in Table 8-95.

Return to the Table 8-55.

This register is configuration register 2 for channel 3.

Table 8-95. CH3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_DVOL[7:0]	R/W	11001001b	Channel 3 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.2.41 CH3_CFG3 Register (Address = 0x49) [Reset = 0x80]

CH3_CFG3 is shown in Table 8-96.

Return to the Table 8-55.

This register is configuration register 3 for channel 3.

Table 8-96. CH3_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH3_GCAL[3:0]	R/W	1000b	Channel 3 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.42 CH3_CFG4 Register (Address = 0x4A) [Reset = 0x00]

CH3_CFG4 is shown in Table 8-97.

Return to the Table 8-55.

This register is configuration register 4 for channel 3.

Table 8-97. CH3_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3_PCAL[7:0]	R/W	00000000b	Channel 3 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.2.43 CH4_CFG2 Register (Address = 0x4D) [Reset = 0xC9]

CH4_CFG2 is shown in Table 8-98.

Return to the Table 8-55.

This register is configuration register 2 for channel 4.

Table 8-98. CH4_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_DVOL[7:0]	R/W	11001001b	Channel 4 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB 255d = Digital volume control is set to 27 dB

8.6.2.44 CH4_CFG3 Register (Address = 0x4E) [Reset = 0x80]

CH4_CFG3 is shown in Table 8-99.

Return to the Table 8-55.

This register is configuration register 3 for channel 4.

Table 8-99. CH4_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH4_GCAL[3:0]	R/W	1000b	Channel 4 gain calibration. 0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.45 CH4_CFG4 Register (Address = 0x4F) [Reset = 0x00]

CH4_CFG4 is shown in Table 8-100.

Return to the Table 8-55.

This register is configuration register 4 for channel 4.

Table 8-100. CH4_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4_PCAL[7:0]	R/W	00000000b	Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock

8.6.2.46 DSP_CFG0 Register (Address = 0x6B) [Reset = 0x01]

DSP_CFG0 is shown in Table 8-101.

Return to the Table 8-55.

This register is the digital signal processor (DSP) configuration register 0.

Table 8-101. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_DVOL_OTF_CHG	R/W	0b	Disable run-time changes to DVOL settings. 0d = Digital volume control changes supported while ADC is powered-on 1d = Digital volume control changes not supported while ADC is powered-on. This is useful for 384 kHz and higher sample rate if more than one channel processing is required.
6	ENH_DRE_AGC_DRC	R/W	0b	Enhanced DRE/AGC/DRC mode. 0d = Standard DRE/AGC/DRC algorithms 1d = Enhanced DRE/AGC/DRC algorithms
5-4	DECI_FILT[1:0]	R/W	00b	Decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use

Table 8-101. DSP_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CH_SUM[1:0]	R/W	00b	Channel summation mode for higher SNR 0d = Channel summation mode is disabled 1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 output 2d = Reserved; Don't use 3d = Reserved; Don't use
1-0	HPF_SEL[1:0]	R/W	01b	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 x f_S (384 Hz at f_S = 48 kHz) is selected

8.6.2.47 DSP_CFG1 Register (Address = 0x6C) [Reset = 0x40]

DSP_CFG1 is shown in Table 8-102.

Return to the Table 8-55.

This register is the digital signal processor (DSP) configuration register 1.

Table 8-102. DSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DVOL_GANG	R/W	0b	DVOL control ganged across channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH1_DVOL) irrespective of whether channel 1 is turned on or not
6-5	BIQUAD_CFG[1:0]	R/W	10b	Number of biquads per channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
4	DISABLE_SOFT_STEP	R/W	0b	Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
3	DRE_AGC_SEL	R/W	0b	DRE or AGC selection when is enabled for any channel if DRC_EN is 0 and CH_DRE_EN is enabled for a channel 0d = DRE is selected 1d = AGC is selected
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	DRC_EN	R/W	0b	Dynamic range compression (DRC) same as DRE without gain compesnation in digital 0d = DRC disabled. Device can be in DRE or AGC mode depending on DRE_AGC_SEL bit 1d = DRC enabled. Device cannot be in DRE or AGC mode.
0	EN_AVOID_CLIP	R/W	0b	Anti clippler when channel gain > 0 dB and either of DRE, DRC or AGC mode enabled. 0d = Channel gain is maintained as per user programmed value 1d = Signal level is compressed to avoid clipping when channel gain > 0 dB amd signal level crosses programmed threshold setting set in page-4.

8.6.2.48 DRE_CFG0 Register (Address = 0x6D) [Reset = 0x7B]

DRE_CFG0 is shown in Table 8-103.

Return to the Table 8-55.

This register is the dynamic range enhancer (DRE) configuration register 0.

Table 8-103. DRE_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DRE_LVL[3:0]	R/W	0111b	DRE trigger signal level threshold. 0d = Input signal level threshold is -12 dB 1d = Input signal level threshold is -18 dB 2d = Input signal level threshold is -24 dB 3d to 6d = Input signal level threshold is as per configuration 7d = Input signal level threshold is -54 dB 8d = Input signal level threshold is -60 dB 9d = Input signal level threshold is -66 dB 10d to 15d = Reserved; Don't use
3-0	DRE_MAXGAIN[3:0]	R/W	1011b	DRE maximum gain allowed. 0d = Maximum gain allowed is 2 dB 1d = Maximum gain allowed is 4 dB 2d = Maximum gain allowed is 6 dB 3d to 10d = Maximum gain allowed is as per configuration 11d = Maximum gain allowed is 24 dB 12d = Maximum gain allowed is 26 dB 13d to 15d = Reserved; Don't use

8.6.2.49 AGC_CFG0 Register (Address = 0x70) [Reset = 0xE7]

AGC_CFG0 is shown in Table 8-104.

Return to the Table 8-55.

This register is the automatic gain controller (AGC) configuration register 0.

Table 8-104. AGC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	AGC_LVL[3:0]	R/W	1110b	AGC output signal target level. 0d = Output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is as per configuration 14d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB
3-0	AGC_MAXGAIN[3:0]	R/W	0111b	AGC maximum gain allowed. 0d = Maximum gain allowed is 3 dB 1d = Maximum gain allowed is 6 dB 2d = Maximum gain allowed is 9 dB 3d to 11d = Maximum gain allowed is as per configuration 12d = Maximum gain allowed is 39 dB 13d = Maximum gain allowed is 42 dB 14d to 15d = Reserved; Don't use

8.6.2.50 GAIN_CFG Register (Address = 0x71) [Reset = 0x00]

GAIN_CFG is shown in Table 8-105.

Return to the Table 8-55.

This register is the channel gain change configuration register.

Table 8-105. GAIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OTF_GAIN_CHANGE_CFG[1:0]	R/W	00b	On the fly channel gain change configuration 0d = On-the-fly gain change with some artifacts due to applying gain change immediately 1d = On-the-fly gain change enabled with reduced artifacts but without soft-stepping 2d = On-the-fly gain change enabled with soft-stepping of 0.5 dB per ~20 µs, supported channel gain up to 30 dB for 10-kΩ input impedance mode and 24 dB for 20-kΩ input impedance mode 3d = On-the-fly gain change enabled with soft-stepping of 0.5 dB per ~40 µs, supported channel gain up to 30 dB for 10-kΩ input impedance mode and 24 dB for 20-kΩ input impedance mode
5	RESERVED	R/W	0b	Reserved bit; Write only reset value
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.2.51 IN_CH_EN Register (Address = 0x73) [Reset = 0xC0]

IN_CH_EN is shown in Table 8-106.

Return to the Table 8-55.

This register is the input channel enable configuration register.

Table 8-106. IN_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_EN	R/W	1b	Input channel 1 enable setting. 0d = Channel 1 is disabled 1d = Channel 1 is enabled
6	IN_CH2_EN	R/W	1b	Input channel 2 enable setting. 0d = Channel 2 is disabled 1d = Channel 2 is enabled
5	IN_CH3_EN	R/W	0b	Input channel 3 (PDM only) enable setting. 0d = Channel 3 is disabled 1d = Channel 3 is enabled
4	IN_CH4_EN	R/W	0b	Input channel 4 (PDM only) enable setting. 0d = Channel 4 is disabled 1d = Channel 4 is enabled
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.52 ASI_OUT_CH_EN Register (Address = 0x74) [Reset = 0x00]

ASI_OUT_CH_EN is shown in Table 8-107.

Return to the Table 8-55.

This register is the ASI output channel enable configuration register.

Table 8-107. ASI_OUT_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_OUT_CH1_EN	R/W	0b	ASI output channel 1 enable setting. 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled
6	ASI_OUT_CH2_EN	R/W	0b	ASI output channel 2 enable setting. 0d = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled
5	ASI_OUT_CH3_EN	R/W	0b	ASI output channel 3 enable setting. 0d = Channel 3 output slot is in a tri-state condition 1d = Channel 3 output slot is enabled

Table 8-107. ASI_OUT_CH_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ASI_OUT_CH4_EN	R/W	0b	ASI output channel 4 enable setting. 0d = Channel 4 output slot is in a tri-state condition 1d = Channel 4 output slot is enabled
3-0	RESERVED	R	0000b	Reserved bits; Write only reset value

8.6.2.53 PWR_CFG Register (Address = 0x75) [Reset = 0x00]

PWR_CFG is shown in Table 8-108.

Return to the Table 8-55.

This register is the power-up configuration register.

Table 8-108. PWR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MICBIAS_PDZ	R/W	0b	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS
6	ADC_PDZ	R/W	0b	Power control for ADC and PDM channels. 0d = Power down all ADC and PDM channels 1d = Power up all enabled ADC and PDM channels
5	PLL_PDZ	R/W	0b	Power control for the PLL. 0d = Power down the PLL 1d = Power up the PLL
4	DYN_CH_PUPD_EN	R/W	0b	Dynamic channel power-up, power-down enable. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on
3-2	DYN_MAXCH_SEL[1:0]	R/W	00b	Dynamic mode maximum channel select configuration. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled 2d = Reserved; Don't use 3d = Reserved; Don't use
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	VAD_EN	R/W	0b	Enable voice activity detection (VAD) algorithm. 0d = VAD is disabled 1d = VAD is enabled

8.6.2.54 DEV_STS0 Register (Address = 0x76) [Reset = 0x00]

DEV_STS0 is shown in Table 8-109.

Return to the Table 8-55.

This register is the device status value register 0.

Table 8-109. DEV_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_STATUS	R	0b	ADC or PDM channel 1 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up
6	CH2_STATUS	R	0b	ADC or PDM channel 2 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up

Table 8-109. DEV_STS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	RESERVED	R	000000b	Reserved bits; Write only reset value

8.6.2.55 DEV_STS1 Register (Address = 0x77) [Reset = 0x80]

DEV_STS1 is shown in Table 8-110.

Return to the Table 8-55.

This register is the device status value register 1.

Table 8-110. DEV_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MODE_STS[2:0]	R	100b	Device mode status. 4d = Device is in sleep mode or software shutdown mode 6d = Device is in active mode with all ADC or PDM channels turned off 7d = Device is in active mode with at least one ADC or PDM channel turned on
4-0	RESERVED	R	00000b	Reserved bits; Write only reset value

8.6.2.56 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C_CKSUM is shown in Table 8-111.

Return to the Table 8-55.

This register returns the I^2C transactions checksum value.

Table 8-111. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	00000000b	These bits return the I^2C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages.

8.6.3 Page 1 Registers

Table 8-112 lists the memory-mapped registers for the Page 1 registers. All register offset addresses not listed in Table 8-112 should be considered as reserved locations and the register contents should not be modified.

Table 8-112. PAGE 1 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	Section 8.6.3.1
0x1E	VAD_CFG1	Voice activity detection configuration register 1	0x20	Section 8.6.3.2
0x1F	VAD_CFG2	Voice activity detection configuration register 2	0x08	Section 8.6.3.3

8.6.3.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x0]

PAGE_CFG is shown in Figure 8-71 and described in Table 8-113.

Return to the Table 8-112.

The device memory map is divided into pages. This register sets the page.

Figure 8-71. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

Table 8-113. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	00000000b	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

8.6.3.2 VAD_CFG1 Register (Address = 0x1E) [Reset = 0x20]

VAD_CFG1 is shown in Figure 8-72 and described in Table 8-114.

Return to the Table 8-112.

This register is configuration register 1 for voice activity detection.

Figure 8-72. VAD_CFG1 Register

7	6	5	4	3	2	1	0
VAD_MODE[1:0]		VAD_CH_SEL[1:0]		VAD_CLK_CFG[1:0]		VAD_EXT_CLK_CFG[1:0]	
R/W-00b		R/W-10b		R/W-00b		R/W-00b	

Table 8-114. VAD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VAD_MODE[1:0]	R/W	00b	Auto ADC power up / power down configuration selection. 0d = User initiated ADC power-up and ADC power-down 1d = VAD interrupt based ADC power up and ADC power down 2d = VAD interrupt based ADC power up but user initiated ADC power down 3d = User initiated ADC power-up but VAD interrupt based ADC power down

Table 8-114. VAD_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VAD_CH_SEL[1:0]	R/W	10b	VAD channel select. 0d = Channel 1 is monitored for VAD activity 1d = Channel 2 is monitored for VAD activity 2d = Channel 3 is monitored for VAD activity 3d = Channel 4 is monitored for VAD activity
3-2	VAD_CLK_CFG[1:0]	R/W	00b	Clock select for VAD 0d = VAD processing using internal oscillator clock 1d = VAD processing using external clock on BCLK input 2d = VAD processing using external clock on MCLK input 3d = Custom clock configuration based on MST_CFG, CLK_SRC and CLKGEN_CFG registers in page 0
1-0	VAD_EXT_CLK_CFG[1:0]	R/W	00b	Clock configuration using external clock for VAD. 0d = External clock is 3.072 MHz 1d = External clock is 6.144 MHz 2d = External clock is 12.288 MHz 3d = External clock is 18.432 MHz

8.6.3.3 VAD_CFG2 Register (Address = 0x1F) [Reset = 0x8]

VAD_CFG2 is shown in Figure 8-73 and described in Table 8-115.

Return to the Table 8-112.

This register is configuration register 2 for voice activity detection.

Figure 8-73. VAD_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED	SDOUT_INT_CFG	RESERVED	RESERVED	VAD_PD_DET_EN	RESERVED		
R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-1b	R-000b		

Table 8-115. VAD_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	Reserved bit; Write only reset value
6	SDOUT_INT_CFG	R/W	0b	SDOUT interrupt configuration. 0d = SDOUT pin is not enabled for interrupt function 1d = SDOUT pin is enabled to support interrupt output when channel data in not being recorded
5	RESERVED	R	0b	Reserved bit; Write only reset value
4	RESERVED	R/W	0b	Reserved bit; Write only reset value
3	VAD_PD_DET_EN	R/W	1b	Enable ASI output data during VAD activity. 0d = VAD processing is not enabled during ADC recording 1d = VAD processing is enabled during ADC recording and VAD interrupts are generated as configured
2-0	RESERVED	R	000b	Reserved bits; Write only reset values

8.6.4 Programmable Coefficient Registers

8.6.4.1 Programmable Coefficient Registers: Page 2

This register page (shown in Table 8-116) consists of the programmable coefficients for the biquad 1 to biquad 6 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

Table 8-116. Page 2 Programmable Coefficient Registers

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x00	PAGE[7:0]	Device page register	0x00
0x08	BQ1_N0_BYT1[7:0]	Programmable biquad 1, N0 coefficient byte[31:24]	0x7F
0x09	BQ1_N0_BYT2[7:0]	Programmable biquad 1, N0 coefficient byte[23:16]	0xFF
0x0A	BQ1_N0_BYT3[7:0]	Programmable biquad 1, N0 coefficient byte[15:8]	0xFF
0x0B	BQ1_N0_BYT4[7:0]	Programmable biquad 1, N0 coefficient byte[7:0]	0xFF
0x0C	BQ1_N1_BYT1[7:0]	Programmable biquad 1, N1 coefficient byte[31:24]	0x00
0x0D	BQ1_N1_BYT2[7:0]	Programmable biquad 1, N1 coefficient byte[23:16]	0x00
0x0E	BQ1_N1_BYT3[7:0]	Programmable biquad 1, N1 coefficient byte[15:8]	0x00
0x0F	BQ1_N1_BYT4[7:0]	Programmable biquad 1, N1 coefficient byte[7:0]	0x00
0x10	BQ1_N2_BYT1[7:0]	Programmable biquad 1, N2 coefficient byte[31:24]	0x00
0x11	BQ1_N2_BYT2[7:0]	Programmable biquad 1, N2 coefficient byte[23:16]	0x00
0x12	BQ1_N2_BYT3[7:0]	Programmable biquad 1, N2 coefficient byte[15:8]	0x00
0x13	BQ1_N2_BYT4[7:0]	Programmable biquad 1, N2 coefficient byte[7:0]	0x00
0x14	BQ1_D1_BYT1[7:0]	Programmable biquad 1, D1 coefficient byte[31:24]	0x00
0x15	BQ1_D1_BYT2[7:0]	Programmable biquad 1, D1 coefficient byte[23:16]	0x00
0x16	BQ1_D1_BYT3[7:0]	Programmable biquad 1, D1 coefficient byte[15:8]	0x00
0x17	BQ1_D1_BYT4[7:0]	Programmable biquad 1, D1 coefficient byte[7:0]	0x00
0x18	BQ1_D2_BYT1[7:0]	Programmable biquad 1, D2 coefficient byte[31:24]	0x00
0x19	BQ1_D2_BYT2[7:0]	Programmable biquad 1, D2 coefficient byte[23:16]	0x00
0x1A	BQ1_D2_BYT3[7:0]	Programmable biquad 1, D2 coefficient byte[15:8]	0x00
0x1B	BQ1_D2_BYT4[7:0]	Programmable biquad 1, D2 coefficient byte[7:0]	0x00
0x1C	BQ2_N0_BYT1[7:0]	Programmable biquad 2, N0 coefficient byte[31:24]	0x7F
0x1D	BQ2_N0_BYT2[7:0]	Programmable biquad 2, N0 coefficient byte[23:16]	0xFF
0x1E	BQ2_N0_BYT3[7:0]	Programmable biquad 2, N0 coefficient byte[15:8]	0xFF
0x1F	BQ2_N0_BYT4[7:0]	Programmable biquad 2, N0 coefficient byte[7:0]	0xFF
0x20	BQ2_N1_BYT1[7:0]	Programmable biquad 2, N1 coefficient byte[31:24]	0x00
0x21	BQ2_N1_BYT2[7:0]	Programmable biquad 2, N1 coefficient byte[23:16]	0x00
0x22	BQ2_N1_BYT3[7:0]	Programmable biquad 2, N1 coefficient byte[15:8]	0x00
0x23	BQ2_N1_BYT4[7:0]	Programmable biquad 2, N1 coefficient byte[7:0]	0x00
0x24	BQ2_N2_BYT1[7:0]	Programmable biquad 2, N2 coefficient byte[31:24]	0x00
0x25	BQ2_N2_BYT2[7:0]	Programmable biquad 2, N2 coefficient byte[23:16]	0x00
0x26	BQ2_N2_BYT3[7:0]	Programmable biquad 2, N2 coefficient byte[15:8]	0x00
0x27	BQ2_N2_BYT4[7:0]	Programmable biquad 2, N2 coefficient byte[7:0]	0x00
0x28	BQ2_D1_BYT1[7:0]	Programmable biquad 2, D1 coefficient byte[31:24]	0x00
0x29	BQ2_D1_BYT2[7:0]	Programmable biquad 2, D1 coefficient byte[23:16]	0x00
0x2A	BQ2_D1_BYT3[7:0]	Programmable biquad 2, D1 coefficient byte[15:8]	0x00
0x2B	BQ2_D1_BYT4[7:0]	Programmable biquad 2, D1 coefficient byte[7:0]	0x00
0x2C	BQ2_D2_BYT1[7:0]	Programmable biquad 2, D2 coefficient byte[31:24]	0x00
0x2D	BQ2_D2_BYT2[7:0]	Programmable biquad 2, D2 coefficient byte[23:16]	0x00
0x2E	BQ2_D2_BYT3[7:0]	Programmable biquad 2, D2 coefficient byte[15:8]	0x00
0x2F	BQ2_D2_BYT4[7:0]	Programmable biquad 2, D2 coefficient byte[7:0]	0x00
0x30	BQ3_N0_BYT1[7:0]	Programmable biquad 3, N0 coefficient byte[31:24]	0x7F
0x31	BQ3_N0_BYT2[7:0]	Programmable biquad 3, N0 coefficient byte[23:16]	0xFF

Table 8-116. Page 2 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x32	BQ3_N0_BYT3[7:0]	Programmable biquad 3, N0 coefficient byte[15:8]	0xFF
0x33	BQ3_N0_BYT4[7:0]	Programmable biquad 3, N0 coefficient byte[7:0]	0xFF
0x34	BQ3_N1_BYT1[7:0]	Programmable biquad 3, N1 coefficient byte[31:24]	0x00
0x35	BQ3_N1_BYT2[7:0]	Programmable biquad 3, N1 coefficient byte[23:16]	0x00
0x36	BQ3_N1_BYT3[7:0]	Programmable biquad 3, N1 coefficient byte[15:8]	0x00
0x37	BQ3_N1_BYT4[7:0]	Programmable biquad 3, N1 coefficient byte[7:0]	0x00
0x38	BQ3_N2_BYT1[7:0]	Programmable biquad 3, N2 coefficient byte[31:24]	0x00
0x39	BQ3_N2_BYT2[7:0]	Programmable biquad 3, N2 coefficient byte[23:16]	0x00
0x3A	BQ3_N2_BYT3[7:0]	Programmable biquad 3, N2 coefficient byte[15:8]	0x00
0x3B	BQ3_N2_BYT4[7:0]	Programmable biquad 3, N2 coefficient byte[7:0]	0x00
0x3C	BQ3_D1_BYT1[7:0]	Programmable biquad 3, D1 coefficient byte[31:24]	0x00
0x3D	BQ3_D1_BYT2[7:0]	Programmable biquad 3, D1 coefficient byte[23:16]	0x00
0x3E	BQ3_D1_BYT3[7:0]	Programmable biquad 3, D1 coefficient byte[15:8]	0x00
0x3F	BQ3_D1_BYT4[7:0]	Programmable biquad 3, D1 coefficient byte[7:0]	0x00
0x40	BQ3_D2_BYT1[7:0]	Programmable biquad 3, D2 coefficient byte[31:24]	0x00
0x41	BQ3_D2_BYT2[7:0]	Programmable biquad 3, D2 coefficient byte[23:16]	0x00
0x42	BQ3_D2_BYT3[7:0]	Programmable biquad 3, D2 coefficient byte[15:8]	0x00
0x43	BQ3_D2_BYT4[7:0]	Programmable biquad 3, D2 coefficient byte[7:0]	0x00
0x44	BQ4_N0_BYT1[7:0]	Programmable biquad 4, N0 coefficient byte[31:24]	0x7F
0x45	BQ4_N0_BYT2[7:0]	Programmable biquad 4, N0 coefficient byte[23:16]	0xFF
0x46	BQ4_N0_BYT3[7:0]	Programmable biquad 4, N0 coefficient byte[15:8]	0xFF
0x47	BQ4_N0_BYT4[7:0]	Programmable biquad 4, N0 coefficient byte[7:0]	0xFF
0x48	BQ4_N1_BYT1[7:0]	Programmable biquad 4, N1 coefficient byte[31:24]	0x00
0x49	BQ4_N1_BYT2[7:0]	Programmable biquad 4, N1 coefficient byte[23:16]	0x00
0x4A	BQ4_N1_BYT3[7:0]	Programmable biquad 4, N1 coefficient byte[15:8]	0x00
0x4B	BQ4_N1_BYT4[7:0]	Programmable biquad 4, N1 coefficient byte[7:0]	0x00
0x4C	BQ4_N2_BYT1[7:0]	Programmable biquad 4, N2 coefficient byte[31:24]	0x00
0x4D	BQ4_N2_BYT2[7:0]	Programmable biquad 4, N2 coefficient byte[23:16]	0x00
0x4E	BQ4_N2_BYT3[7:0]	Programmable biquad 4, N2 coefficient byte[15:8]	0x00
0x4F	BQ4_N2_BYT4[7:0]	Programmable biquad 4, N2 coefficient byte[7:0]	0x00
0x50	BQ4_D1_BYT1[7:0]	Programmable biquad 4, D1 coefficient byte[31:24]	0x00
0x51	BQ4_D1_BYT2[7:0]	Programmable biquad 4, D1 coefficient byte[23:16]	0x00
0x52	BQ4_D1_BYT3[7:0]	Programmable biquad 4, D1 coefficient byte[15:8]	0x00
0x53	BQ4_D1_BYT4[7:0]	Programmable biquad 4, D1 coefficient byte[7:0]	0x00
0x54	BQ4_D2_BYT1[7:0]	Programmable biquad 4, D2 coefficient byte[31:24]	0x00
0x55	BQ4_D2_BYT2[7:0]	Programmable biquad 4, D2 coefficient byte[23:16]	0x00
0x56	BQ4_D2_BYT3[7:0]	Programmable biquad 4, D2 coefficient byte[15:8]	0x00
0x57	BQ4_D2_BYT4[7:0]	Programmable biquad 4, D2 coefficient byte[7:0]	0x00
0x58	BQ5_N0_BYT1[7:0]	Programmable biquad 5, N0 coefficient byte[31:24]	0x7F
0x59	BQ5_N0_BYT2[7:0]	Programmable biquad 5, N0 coefficient byte[23:16]	0xFF
0x5A	BQ5_N0_BYT3[7:0]	Programmable biquad 5, N0 coefficient byte[15:8]	0xFF
0x5B	BQ5_N0_BYT4[7:0]	Programmable biquad 5, N0 coefficient byte[7:0]	0xFF
0x5C	BQ5_N1_BYT1[7:0]	Programmable biquad 5, N1 coefficient byte[31:24]	0x00
0x5D	BQ5_N1_BYT2[7:0]	Programmable biquad 5, N1 coefficient byte[23:16]	0x00
0x5E	BQ5_N1_BYT3[7:0]	Programmable biquad 5, N1 coefficient byte[15:8]	0x00
0x5F	BQ5_N1_BYT4[7:0]	Programmable biquad 5, N1 coefficient byte[7:0]	0x00
0x60	BQ5_N2_BYT1[7:0]	Programmable biquad 5, N2 coefficient byte[31:24]	0x00
0x61	BQ5_N2_BYT2[7:0]	Programmable biquad 5, N2 coefficient byte[23:16]	0x00
0x62	BQ5_N2_BYT3[7:0]	Programmable biquad 5, N2 coefficient byte[15:8]	0x00
0x63	BQ5_N2_BYT4[7:0]	Programmable biquad 5, N2 coefficient byte[7:0]	0x00

Table 8-116. Page 2 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x64	BQ5_D1_BYT1[7:0]	Programmable biquad 5, D1 coefficient byte[31:24]	0x00
0x65	BQ5_D1_BYT2[7:0]	Programmable biquad 5, D1 coefficient byte[23:16]	0x00
0x66	BQ5_D1_BYT3[7:0]	Programmable biquad 5, D1 coefficient byte[15:8]	0x00
0x67	BQ5_D1_BYT4[7:0]	Programmable biquad 5, D1 coefficient byte[7:0]	0x00
0x68	BQ5_D2_BYT1[7:0]	Programmable biquad 5, D2 coefficient byte[31:24]	0x00
0x69	BQ5_D2_BYT2[7:0]	Programmable biquad 5, D2 coefficient byte[23:16]	0x00
0x6A	BQ5_D2_BYT3[7:0]	Programmable biquad 5, D2 coefficient byte[15:8]	0x00
0x6B	BQ5_D2_BYT4[7:0]	Programmable biquad 5, D2 coefficient byte[7:0]	0x00
0x6C	BQ6_N0_BYT1[7:0]	Programmable biquad 6, N0 coefficient byte[31:24]	0x7F
0x6D	BQ6_N0_BYT2[7:0]	Programmable biquad 6, N0 coefficient byte[23:16]	0xFF
0x6E	BQ6_N0_BYT3[7:0]	Programmable biquad 6, N0 coefficient byte[15:8]	0xFF
0x6F	BQ6_N0_BYT4[7:0]	Programmable biquad 6, N0 coefficient byte[7:0]	0xFF
0x70	BQ6_N1_BYT1[7:0]	Programmable biquad 6, N1 coefficient byte[31:24]	0x00
0x71	BQ6_N1_BYT2[7:0]	Programmable biquad 6, N1 coefficient byte[23:16]	0x00
0x72	BQ6_N1_BYT3[7:0]	Programmable biquad 6, N1 coefficient byte[15:8]	0x00
0x73	BQ6_N1_BYT4[7:0]	Programmable biquad 6, N1 coefficient byte[7:0]	0x00
0x74	BQ6_N2_BYT1[7:0]	Programmable biquad 6, N2 coefficient byte[31:24]	0x00
0x75	BQ6_N2_BYT2[7:0]	Programmable biquad 6, N2 coefficient byte[23:16]	0x00
0x76	BQ6_N2_BYT3[7:0]	Programmable biquad 6, N2 coefficient byte[15:8]	0x00
0x77	BQ6_N2_BYT4[7:0]	Programmable biquad 6, N2 coefficient byte[7:0]	0x00
0x78	BQ6_D1_BYT1[7:0]	Programmable biquad 6, D1 coefficient byte[31:24]	0x00
0x79	BQ6_D1_BYT2[7:0]	Programmable biquad 6, D1 coefficient byte[23:16]	0x00
0x7A	BQ6_D1_BYT3[7:0]	Programmable biquad 6, D1 coefficient byte[15:8]	0x00
0x7B	BQ6_D1_BYT4[7:0]	Programmable biquad 6, D1 coefficient byte[7:0]	0x00
0x7C	BQ6_D2_BYT1[7:0]	Programmable biquad 6, D2 coefficient byte[31:24]	0x00
0x7D	BQ6_D2_BYT2[7:0]	Programmable biquad 6, D2 coefficient byte[23:16]	0x00
0x7E	BQ6_D2_BYT3[7:0]	Programmable biquad 6, D2 coefficient byte[15:8]	0x00
0x7F	BQ6_D2_BYT4[7:0]	Programmable biquad 6, D2 coefficient byte[7:0]	0x00

8.6.4.2 Programmable Coefficient Registers: Page 3

This register page (shown in Table 8-117) consists of the programmable coefficients for the biquad 7 to biquad 12 filters. To optimize the coefficients register transaction time for page 2, page 3, and page 4, the device also supports (by default) auto-incremented pages for the I^2C writes and reads. After a transaction of register address 0x7F, the device auto increments to the next page at register 0x08 to transact the next coefficient value.

Table 8-117. Page 3 Programmable Coefficient Registers

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x00	PAGE[7:0]	Device page register	0x00
0x08	BQ7_N0_BYT1[7:0]	Programmable biquad 7, N0 coefficient byte[31:24]	0x7F
0x09	BQ7_N0_BYT2[7:0]	Programmable biquad 7, N0 coefficient byte[23:16]	0xFF
0x0A	BQ7_N0_BYT3[7:0]	Programmable biquad 7, N0 coefficient byte[15:8]	0xFF
0x0B	BQ7_N0_BYT4[7:0]	Programmable biquad 7, N0 coefficient byte[7:0]	0xFF
0x0C	BQ7_N1_BYT1[7:0]	Programmable biquad 7, N1 coefficient byte[31:24]	0x00
0x0D	BQ7_N1_BYT2[7:0]	Programmable biquad 7, N1 coefficient byte[23:16]	0x00
0x0E	BQ7_N1_BYT3[7:0]	Programmable biquad 7, N1 coefficient byte[15:8]	0x00
0x0F	BQ7_N1_BYT4[7:0]	Programmable biquad 7, N1 coefficient byte[7:0]	0x00
0x10	BQ7_N2_BYT1[7:0]	Programmable biquad 7, N2 coefficient byte[31:24]	0x00
0x11	BQ7_N2_BYT2[7:0]	Programmable biquad 7, N2 coefficient byte[23:16]	0x00
0x12	BQ7_N2_BYT3[7:0]	Programmable biquad 7, N2 coefficient byte[15:8]	0x00
0x13	BQ7_N2_BYT4[7:0]	Programmable biquad 7, N2 coefficient byte[7:0]	0x00
0x14	BQ7_D1_BYT1[7:0]	Programmable biquad 7, D1 coefficient byte[31:24]	0x00
0x15	BQ7_D1_BYT2[7:0]	Programmable biquad 7, D1 coefficient byte[23:16]	0x00
0x16	BQ7_D1_BYT3[7:0]	Programmable biquad 7, D1 coefficient byte[15:8]	0x00
0x17	BQ7_D1_BYT4[7:0]	Programmable biquad 7, D1 coefficient byte[7:0]	0x00
0x18	BQ7_D2_BYT1[7:0]	Programmable biquad 7, D2 coefficient byte[31:24]	0x00
0x19	BQ7_D2_BYT2[7:0]	Programmable biquad 7, D2 coefficient byte[23:16]	0x00
0x1A	BQ7_D2_BYT3[7:0]	Programmable biquad 7, D2 coefficient byte[15:8]	0x00
0x1B	BQ7_D2_BYT4[7:0]	Programmable biquad 7, D2 coefficient byte[7:0]	0x00
0x1C	BQ8_N0_BYT1[7:0]	Programmable biquad 8, N0 coefficient byte[31:24]	0x7F
0x1D	BQ8_N0_BYT2[7:0]	Programmable biquad 8, N0 coefficient byte[23:16]	0xFF
0x1E	BQ8_N0_BYT3[7:0]	Programmable biquad 8, N0 coefficient byte[15:8]	0xFF
0x1F	BQ8_N0_BYT4[7:0]	Programmable biquad 8, N0 coefficient byte[7:0]	0xFF
0x20	BQ8_N1_BYT1[7:0]	Programmable biquad 8, N1 coefficient byte[31:24]	0x00
0x21	BQ8_N1_BYT2[7:0]	Programmable biquad 8, N1 coefficient byte[23:16]	0x00
0x22	BQ8_N1_BYT3[7:0]	Programmable biquad 8, N1 coefficient byte[15:8]	0x00
0x23	BQ8_N1_BYT4[7:0]	Programmable biquad 8, N1 coefficient byte[7:0]	0x00
0x24	BQ8_N2_BYT1[7:0]	Programmable biquad 8, N2 coefficient byte[31:24]	0x00
0x25	BQ8_N2_BYT2[7:0]	Programmable biquad 8, N2 coefficient byte[23:16]	0x00
0x26	BQ8_N2_BYT3[7:0]	Programmable biquad 8, N2 coefficient byte[15:8]	0x00
0x27	BQ8_N2_BYT4[7:0]	Programmable biquad 8, N2 coefficient byte[7:0]	0x00
0x28	BQ8_D1_BYT1[7:0]	Programmable biquad 8, D1 coefficient byte[31:24]	0x00
0x29	BQ8_D1_BYT2[7:0]	Programmable biquad 8, D1 coefficient byte[23:16]	0x00
0x2A	BQ8_D1_BYT3[7:0]	Programmable biquad 8, D1 coefficient byte[15:8]	0x00
0x2B	BQ8_D1_BYT4[7:0]	Programmable biquad 8, D1 coefficient byte[7:0]	0x00
0x2C	BQ8_D2_BYT1[7:0]	Programmable biquad 8, D2 coefficient byte[31:24]	0x00
0x2D	BQ8_D2_BYT2[7:0]	Programmable biquad 8, D2 coefficient byte[23:16]	0x00
0x2E	BQ8_D2_BYT3[7:0]	Programmable biquad 8, D2 coefficient byte[15:8]	0x00
0x2F	BQ8_D2_BYT4[7:0]	Programmable biquad 8, D2 coefficient byte[7:0]	0x00
0x30	BQ9_N0_BYT1[7:0]	Programmable biquad 9, N0 coefficient byte[31:24]	0x7F
0x31	BQ9_N0_BYT2[7:0]	Programmable biquad 9, N0 coefficient byte[23:16]	0xFF
0x32	BQ9_N0_BYT3[7:0]	Programmable biquad 9, N0 coefficient byte[15:8]	0xFF

Table 8-117. Page 3 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x33	BQ9_N0_BYT4[7:0]	Programmable biquad 9, N0 coefficient byte[7:0]	0xFF
0x34	BQ9_N1_BYT1[7:0]	Programmable biquad 9, N1 coefficient byte[31:24]	0x00
0x35	BQ9_N1_BYT2[7:0]	Programmable biquad 9, N1 coefficient byte[23:16]	0x00
0x36	BQ9_N1_BYT3[7:0]	Programmable biquad 9, N1 coefficient byte[15:8]	0x00
0x37	BQ9_N1_BYT4[7:0]	Programmable biquad 9, N1 coefficient byte[7:0]	0x00
0x38	BQ9_N2_BYT1[7:0]	Programmable biquad 9, N2 coefficient byte[31:24]	0x00
0x39	BQ9_N2_BYT2[7:0]	Programmable biquad 9, N2 coefficient byte[23:16]	0x00
0x3A	BQ9_N2_BYT3[7:0]	Programmable biquad 9, N2 coefficient byte[15:8]	0x00
0x3B	BQ9_N2_BYT4[7:0]	Programmable biquad 9, N2 coefficient byte[7:0]	0x00
0x3C	BQ9_D1_BYT1[7:0]	Programmable biquad 9, D1 coefficient byte[31:24]	0x00
0x3D	BQ9_D1_BYT2[7:0]	Programmable biquad 9, D1 coefficient byte[23:16]	0x00
0x3E	BQ9_D1_BYT3[7:0]	Programmable biquad 9, D1 coefficient byte[15:8]	0x00
0x3F	BQ9_D1_BYT4[7:0]	Programmable biquad 9, D1 coefficient byte[7:0]	0x00
0x40	BQ9_D2_BYT1[7:0]	Programmable biquad 9, D2 coefficient byte[31:24]	0x00
0x41	BQ9_D2_BYT2[7:0]	Programmable biquad 9, D2 coefficient byte[23:16]	0x00
0x42	BQ9_D2_BYT3[7:0]	Programmable biquad 9, D2 coefficient byte[15:8]	0x00
0x43	BQ9_D2_BYT4[7:0]	Programmable biquad 9, D2 coefficient byte[7:0]	0x00
0x44	BQ10_N0_BYT1[7:0]	Programmable biquad 10, N0 coefficient byte[31:24]	0x7F
0x45	BQ10_N0_BYT2[7:0]	Programmable biquad 10, N0 coefficient byte[23:16]	0xFF
0x46	BQ10_N0_BYT3[7:0]	Programmable biquad 10, N0 coefficient byte[15:8]	0xFF
0x47	BQ10_N0_BYT4[7:0]	Programmable biquad 10, N0 coefficient byte[7:0]	0xFF
0x48	BQ10_N1_BYT1[7:0]	Programmable biquad 10, N1 coefficient byte[31:24]	0x00
0x49	BQ10_N1_BYT2[7:0]	Programmable biquad 10, N1 coefficient byte[23:16]	0x00
0x4A	BQ10_N1_BYT3[7:0]	Programmable biquad 10, N1 coefficient byte[15:8]	0x00
0x4B	BQ10_N1_BYT4[7:0]	Programmable biquad 10, N1 coefficient byte[7:0]	0x00
0x4C	BQ10_N2_BYT1[7:0]	Programmable biquad 10, N2 coefficient byte[31:24]	0x00
0x4D	BQ10_N2_BYT2[7:0]	Programmable biquad 10, N2 coefficient byte[23:16]	0x00
0x4E	BQ10_N2_BYT3[7:0]	Programmable biquad 10, N2 coefficient byte[15:8]	0x00
0x4F	BQ10_N2_BYT4[7:0]	Programmable biquad 10, N2 coefficient byte[7:0]	0x00
0x50	BQ10_D1_BYT1[7:0]	Programmable biquad 10, D1 coefficient byte[31:24]	0x00
0x51	BQ10_D1_BYT2[7:0]	Programmable biquad 10, D1 coefficient byte[23:16]	0x00
0x52	BQ10_D1_BYT3[7:0]	Programmable biquad 10, D1 coefficient byte[15:8]	0x00
0x53	BQ10_D1_BYT4[7:0]	Programmable biquad 10, D1 coefficient byte[7:0]	0x00
0x54	BQ10_D2_BYT1[7:0]	Programmable biquad 10, D2 coefficient byte[31:24]	0x00
0x55	BQ10_D2_BYT2[7:0]	Programmable biquad 10, D2 coefficient byte[23:16]	0x00
0x56	BQ10_D2_BYT3[7:0]	Programmable biquad 10, D2 coefficient byte[15:8]	0x00
0x57	BQ10_D2_BYT4[7:0]	Programmable biquad 10, D2 coefficient byte[7:0]	0x00
0x58	BQ11_N0_BYT1[7:0]	Programmable biquad 11, N0 coefficient byte[31:24]	0x7F
0x59	BQ11_N0_BYT2[7:0]	Programmable biquad 11, N0 coefficient byte[23:16]	0xFF
0x5A	BQ11_N0_BYT3[7:0]	Programmable biquad 11, N0 coefficient byte[15:8]	0xFF
0x5B	BQ11_N0_BYT4[7:0]	Programmable biquad 11, N0 coefficient byte[7:0]	0xFF
0x5C	BQ11_N1_BYT1[7:0]	Programmable biquad 11, N1 coefficient byte[31:24]	0x00
0x5D	BQ11_N1_BYT2[7:0]	Programmable biquad 11, N1 coefficient byte[23:16]	0x00
0x5E	BQ11_N1_BYT3[7:0]	Programmable biquad 11, N1 coefficient byte[15:8]	0x00
0x5F	BQ11_N1_BYT4[7:0]	Programmable biquad 11, N1 coefficient byte[7:0]	0x00
0x60	BQ11_N2_BYT1[7:0]	Programmable biquad 11, N2 coefficient byte[31:24]	0x00
0x61	BQ11_N2_BYT2[7:0]	Programmable biquad 11, N2 coefficient byte[23:16]	0x00
0x62	BQ11_N2_BYT3[7:0]	Programmable biquad 11, N2 coefficient byte[15:8]	0x00
0x63	BQ11_N2_BYT4[7:0]	Programmable biquad 11, N2 coefficient byte[7:0]	0x00
0x64	BQ11_D1_BYT1[7:0]	Programmable biquad 11, D1 coefficient byte[31:24]	0x00

Table 8-117. Page 3 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x65	BQ11_D1_BYT2[7:0]	Programmable biquad 11, D1 coefficient byte[23:16]	0x00
0x66	BQ11_D1_BYT3[7:0]	Programmable biquad 11, D1 coefficient byte[15:8]	0x00
0x67	BQ11_D1_BYT4[7:0]	Programmable biquad 11, D1 coefficient byte[7:0]	0x00
0x68	BQ11_D2_BYT1[7:0]	Programmable biquad 11, D2 coefficient byte[31:24]	0x00
0x69	BQ11_D2_BYT2[7:0]	Programmable biquad 11, D2 coefficient byte[23:16]	0x00
0x6A	BQ11_D2_BYT3[7:0]	Programmable biquad 11, D2 coefficient byte[15:8]	0x00
0x6B	BQ11_D2_BYT4[7:0]	Programmable biquad 11, D2 coefficient byte[7:0]	0x00
0x6C	BQ12_N0_BYT1[7:0]	Programmable biquad 12, N0 coefficient byte[31:24]	0x7F
0x6D	BQ12_N0_BYT2[7:0]	Programmable biquad 12, N0 coefficient byte[23:16]	0xFF
0x6E	BQ12_N0_BYT3[7:0]	Programmable biquad 12, N0 coefficient byte[15:8]	0xFF
0x6F	BQ12_N0_BYT4[7:0]	Programmable biquad 12, N0 coefficient byte[7:0]	0xFF
0x70	BQ12_N1_BYT1[7:0]	Programmable biquad 12, N1 coefficient byte[31:24]	0x00
0x71	BQ12_N1_BYT2[7:0]	Programmable biquad 12, N1 coefficient byte[23:16]	0x00
0x72	BQ12_N1_BYT3[7:0]	Programmable biquad 12, N1 coefficient byte[15:8]	0x00
0x73	BQ12_N1_BYT4[7:0]	Programmable biquad 12, N1 coefficient byte[7:0]	0x00
0x74	BQ12_N2_BYT1[7:0]	Programmable biquad 12, N2 coefficient byte[31:24]	0x00
0x75	BQ12_N2_BYT2[7:0]	Programmable biquad 12, N2 coefficient byte[23:16]	0x00
0x76	BQ12_N2_BYT3[7:0]	Programmable biquad 12, N2 coefficient byte[15:8]	0x00
0x77	BQ12_N2_BYT4[7:0]	Programmable biquad 12, N2 coefficient byte[7:0]	0x00
0x78	BQ12_D1_BYT1[7:0]	Programmable biquad 12, D1 coefficient byte[31:24]	0x00
0x79	BQ12_D1_BYT2[7:0]	Programmable biquad 12, D1 coefficient byte[23:16]	0x00
0x7A	BQ12_D1_BYT3[7:0]	Programmable biquad 12, D1 coefficient byte[15:8]	0x00
0x7B	BQ12_D1_BYT4[7:0]	Programmable biquad 12, D1 coefficient byte[7:0]	0x00
0x7C	BQ12_D2_BYT1[7:0]	Programmable biquad 12, D2 coefficient byte[31:24]	0x00
0x7D	BQ12_D2_BYT2[7:0]	Programmable biquad 12, D2 coefficient byte[23:16]	0x00
0x7E	BQ12_D2_BYT3[7:0]	Programmable biquad 12, D2 coefficient byte[15:8]	0x00
0x7F	BQ12_D2_BYT4[7:0]	Programmable biquad 12, D2 coefficient byte[7:0]	0x00

8.6.4.3 Programmable Coefficient Registers: Page 4

This register page (shown in Table 8-118) consists of the programmable coefficients for mixer 1 to mixer 4 and the first-order IIR filter.

Table 8-118. Page 4 Programmable Coefficient Registers

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x00	PAGE[7:0]	Device page register	0x00
0x08	MIX1_CH1_BYT1[7:0]	Digital mixer 1, channel 1 coefficient byte[31:24]	0x7F
0x09	MIX1_CH1_BYT2[7:0]	Digital mixer 1, channel 1 coefficient byte[23:16]	0xFF
0x0A	MIX1_CH1_BYT3[7:0]	Digital mixer 1, channel 1 coefficient byte[15:8]	0xFF
0x0B	MIX1_CH1_BYT4[7:0]	Digital mixer 1, channel 1 coefficient byte[7:0]	0xFF
0x0C	MIX1_CH2_BYT1[7:0]	Digital mixer 1, channel 2 coefficient byte[31:24]	0x00
0x0D	MIX1_CH2_BYT2[7:0]	Digital mixer 1, channel 2 coefficient byte[23:16]	0x00
0x0E	MIX1_CH2_BYT3[7:0]	Digital mixer 1, channel 2 coefficient byte[15:8]	0x00
0x0F	MIX1_CH2_BYT4[7:0]	Digital mixer 1, channel 2 coefficient byte[7:0]	0x00
0x10	MIX1_CH3_BYT1[7:0]	Digital mixer 1, channel 3 coefficient byte[31:24]	0x00
0x11	MIX1_CH3_BYT2[7:0]	Digital mixer 1, channel 3 coefficient byte[23:16]	0x00
0x12	MIX1_CH3_BYT3[7:0]	Digital mixer 1, channel 3 coefficient byte[15:8]	0x00
0x13	MIX1_CH3_BYT4[7:0]	Digital mixer 1, channel 3 coefficient byte[7:0]	0x00
0x14	MIX1_CH4_BYT1[7:0]	Digital mixer 1, channel 4 coefficient byte[31:24]	0x00
0x15	MIX1_CH4_BYT2[7:0]	Digital mixer 1, channel 4 coefficient byte[23:16]	0x00
0x16	MIX1_CH4_BYT3[7:0]	Digital mixer 1, channel 4 coefficient byte[15:8]	0x00
0x17	MIX1_CH4_BYT4[7:0]	Digital mixer 1, channel 4 coefficient byte[7:0]	0x00
0x18	MIX2_CH1_BYT1[7:0]	Digital mixer 2, channel 1 coefficient byte[31:24]	0x00
0x19	MIX2_CH1_BYT2[7:0]	Digital mixer 2, channel 1 coefficient byte[23:16]	0x00
0x1A	MIX2_CH1_BYT3[7:0]	Digital mixer 2, channel 1 coefficient byte[15:8]	0x00
0x1B	MIX2_CH1_BYT4[7:0]	Digital mixer 2, channel 1 coefficient byte[7:0]	0x00
0x1C	MIX2_CH2_BYT1[7:0]	Digital mixer 2, channel 2 coefficient byte[31:24]	0x7F
0x1D	MIX2_CH2_BYT2[7:0]	Digital mixer 2, channel 2 coefficient byte[23:16]	0xFF
0x1E	MIX2_CH2_BYT3[7:0]	Digital mixer 2, channel 2 coefficient byte[15:8]	0xFF
0x1F	MIX2_CH2_BYT4[7:0]	Digital mixer 2, channel 2 coefficient byte[7:0]	0xFF
0x20	MIX2_CH3_BYT1[7:0]	Digital mixer 2, channel 3 coefficient byte[31:24]	0x00
0x21	MIX2_CH3_BYT2[7:0]	Digital mixer 2, channel 3 coefficient byte[23:16]	0x00
0x22	MIX2_CH3_BYT3[7:0]	Digital mixer 2, channel 3 coefficient byte[15:8]	0x00
0x23	MIX2_CH3_BYT4[7:0]	Digital mixer 2, channel 3 coefficient byte[7:0]	0x00
0x24	MIX2_CH4_BYT1[7:0]	Digital mixer 2, channel 4 coefficient byte[31:24]	0x00
0x25	MIX2_CH4_BYT2[7:0]	Digital mixer 2, channel 4 coefficient byte[23:16]	0x00
0x26	MIX2_CH4_BYT3[7:0]	Digital mixer 2, channel 4 coefficient byte[15:8]	0x00
0x27	MIX2_CH4_BYT4[7:0]	Digital mixer 2, channel 4 coefficient byte[7:0]	0x00
0x28	MIX3_CH1_BYT1[7:0]	Digital mixer 3, channel 1 coefficient byte[31:24]	0x00
0x29	MIX3_CH1_BYT2[7:0]	Digital mixer 3, channel 1 coefficient byte[23:16]	0x00
0x2A	MIX3_CH1_BYT3[7:0]	Digital mixer 3, channel 1 coefficient byte[15:8]	0x00
0x2B	MIX3_CH1_BYT4[7:0]	Digital mixer 3, channel 1 coefficient byte[7:0]	0x00
0x2C	MIX3_CH2_BYT1[7:0]	Digital mixer 3, channel 2 coefficient byte[31:24]	0x00
0x2D	MIX3_CH2_BYT2[7:0]	Digital mixer 3, channel 2 coefficient byte[23:16]	0x00
0x2E	MIX3_CH2_BYT3[7:0]	Digital mixer 3, channel 2 coefficient byte[15:8]	0x00
0x2F	MIX3_CH2_BYT4[7:0]	Digital mixer 3, channel 2 coefficient byte[7:0]	0x00
0x30	MIX3_CH3_BYT1[7:0]	Digital mixer 3, channel 3 coefficient byte[31:24]	0x7F
0x31	MIX3_CH3_BYT2[7:0]	Digital mixer 3, channel 3 coefficient byte[23:16]	0xFF
0x32	MIX3_CH3_BYT3[7:0]	Digital mixer 3, channel 3 coefficient byte[15:8]	0xFF
0x33	MIX3_CH3_BYT4[7:0]	Digital mixer 3, channel 3 coefficient byte[7:0]	0xFF
0x34	MIX3_CH4_BYT1[7:0]	Digital mixer 3, channel 4 coefficient byte[31:24]	0x00

Table 8-118. Page 4 Programmable Coefficient Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	RESET VALUE
0x35	MIX3_CH4_BYT2[7:0]	Digital mixer 3, channel 4 coefficient byte[23:16]	0x00
0x36	MIX3_CH4_BYT3[7:0]	Digital mixer 3, channel 4 coefficient byte[15:8]	0x00
0x37	MIX3_CH4_BYT4[7:0]	Digital mixer 3, channel 4 coefficient byte[7:0]	0x00
0x38	MIX4_CH1_BYT1[7:0]	Digital mixer 4, channel 1 coefficient byte[31:24]	0x00
0x39	MIX4_CH1_BYT2[7:0]	Digital mixer 4, channel 1 coefficient byte[23:16]	0x00
0x3A	MIX4_CH1_BYT3[7:0]	Digital mixer 4, channel 1 coefficient byte[15:8]	0x00
0x3B	MIX4_CH1_BYT4[7:0]	Digital mixer 4, channel 1 coefficient byte[7:0]	0x00
0x3C	MIX4_CH2_BYT1[7:0]	Digital mixer 4, channel 2 coefficient byte[31:24]	0x00
0x3D	MIX4_CH2_BYT2[7:0]	Digital mixer 4, channel 2 coefficient byte[23:16]	0x00
0x3E	MIX4_CH2_BYT3[7:0]	Digital mixer 4, channel 2 coefficient byte[15:8]	0x00
0x3F	MIX4_CH2_BYT4[7:0]	Digital mixer 4, channel 2 coefficient byte[7:0]	0x00
0x40	MIX4_CH3_BYT1[7:0]	Digital mixer 4, channel 3 coefficient byte[31:24]	0x00
0x41	MIX4_CH3_BYT2[7:0]	Digital mixer 4, channel 3 coefficient byte[23:16]	0x00
0x42	MIX4_CH3_BYT3[7:0]	Digital mixer 4, channel 3 coefficient byte[15:8]	0x00
0x43	MIX4_CH3_BYT4[7:0]	Digital mixer 4, channel 3 coefficient byte[7:0]	0x00
0x44	MIX4_CH4_BYT1[7:0]	Digital mixer 4, channel 4 coefficient byte[31:24]	0x7F
0x45	MIX4_CH4_BYT2[7:0]	Digital mixer 4, channel 4 coefficient byte[23:16]	0xFF
0x46	MIX4_CH4_BYT3[7:0]	Digital mixer 4, channel 4 coefficient byte[15:8]	0xFF
0x47	MIX4_CH4_BYT4[7:0]	Digital mixer 4, channel 4 coefficient byte[7:0]	0xFF
0x48	IIR_N0_BYT1[7:0]	Programmable first-order IIR, N0 coefficient byte[31:24]	0x7F
0x49	IIR_N0_BYT2[7:0]	Programmable first-order IIR, N0 coefficient byte[23:16]	0xFF
0x4A	IIR_N0_BYT3[7:0]	Programmable first-order IIR, N0 coefficient byte[15:8]	0xFF
0x4B	IIR_N0_BYT4[7:0]	Programmable first-order IIR, N0 coefficient byte[7:0]	0xFF
0x4C	IIR_N1_BYT1[7:0]	Programmable first-order IIR, N1 coefficient byte[31:24]	0x00
0x4D	IIR_N1_BYT2[7:0]	Programmable first-order IIR, N1 coefficient byte[23:16]	0x00
0x4E	IIR_N1_BYT3[7:0]	Programmable first-order IIR, N1 coefficient byte[15:8]	0x00
0x4F	IIR_N1_BYT4[7:0]	Programmable first-order IIR, N1 coefficient byte[7:0]	0x00
0x50	IIR_D1_BYT1[7:0]	Programmable first-order IIR, D1 coefficient byte[31:24]	0x00
0x51	IIR_D1_BYT2[7:0]	Programmable first-order IIR, D1 coefficient byte[23:16]	0x00
0x52	IIR_D1_BYT3[7:0]	Programmable first-order IIR, D1 coefficient byte[15:8]	0x00
0x53	IIR_D1_BYT4[7:0]	Programmable first-order IIR, D1 coefficient byte[7:0]	0x00

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The PCM6120-Q1 is a multichannel, high-performance audio analog-to-digital converter (ADC) that supports output sample rates of up to 768 kHz. The device supports either up to two analog microphones or up to four digital pulse density modulation (PDM) microphones for simultaneous recording applications.

Communication to the PCM6120-Q1 for configuration of the control registers is supported using an I^2C interface. The device supports a highly flexible, audio serial interface (TDM, I^2S, and LJ) to transmit audio data seamlessly in the system across devices.

9.2 Typical Applications

9.2.1 Two-Channel Analog Microphone Recording

Figure 9-1 shows a typical configuration of the PCM6120-Q1 for an application using two analog microelectrical-mechanical system (MEMS) microphones for simultaneous recording operation with an I^2C control interface and a time-division multiplexing (TDM) audio data slave interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

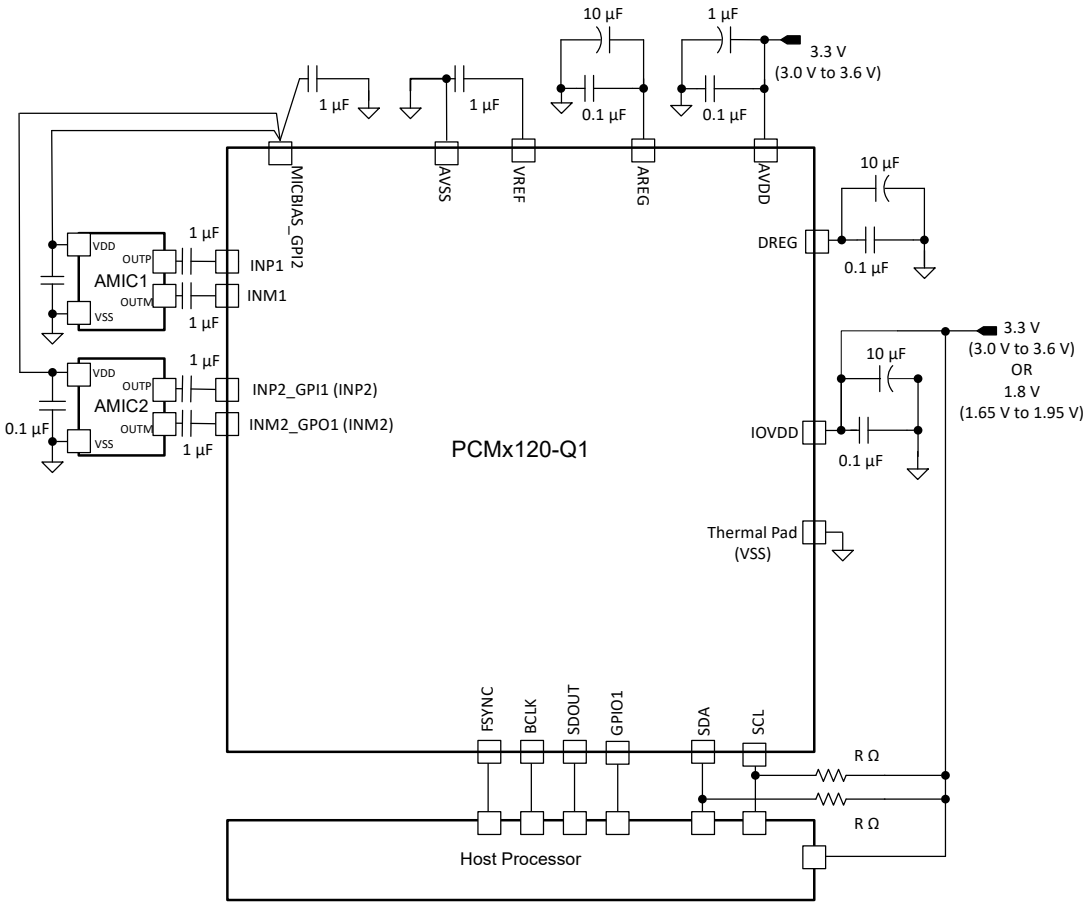


Figure 9-1. Two-Channel Analog Microphone Recording Diagram

9.2.1.1 Design Requirements

Table 9-1 lists the design parameters for this application.

Table 9-1. Design Parameters

KEY PARAMETER	SPECIFICATION
AVDD	3.3 V
AVDD supply current consumption	>14 mA (PLL on, two-channel recording, f_S = 48 kHz)
IOVDD	1.8 V or 3.3 V
Maximum MICBIAS current	5 mA (MICBIAS voltage is the same as AVDD)

9.2.1.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM6120-Q1 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power-up the IOVDD and AVDD power supplies
   b. Wait for at least 1 ms to allow the device to initialize the internal registers initialization
   c. The device now goes into sleep mode (low-power mode < 10 µA)
2. Transition from sleep mode to active mode whenever required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence

c. Override default configuration registers or programmable coefficients value as required (this step is optional)
d. Enable all desired input channels by writing to P0_R115
e. Enable all desired audio serial interface output channels by writing to P0_R116
f. Power-up the ADC, MICBIAS, and PLL by writing to P0_R117
g. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

   This specific step can be done at any point in the sequence after step a.

   See the *Section 8.3.2* section for supported sample rates and the BCLK to FSYNC ratio.
h. The device recording data are now sent to the host processor via the TDM audio serial data bus

3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
   a. Enter sleep mode by writing to P0_R2 to enable sleep mode
   b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
   c. Read P0_R119 to check the device shutdown and sleep mode status
   d. If the device P0_R119_D7 status bit is 1'b1 then stop FSYNC and BCLK in the system
   e. The device now goes into sleep mode (low-power mode < 10 µA) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
   d. The device recording data are now sent to the host processor via the TDM audio serial data bus
5. Repeat step 2 to step 4 as required for configuration changes or step 3 to step 4 for mode transitions

9.2.1.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I²C register control script that shows how to set up the PCM6120-Q1 in a two-channel analog microphone recording mode with differential inputs.

```
# Key: w 9C XX YY ==> write to I2C address 0x9C, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. There are
# other valid sequences depending on which features are used.
#
# See the PCM6120-Q1EVM user guide for jumper settings and audio connections.
#
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 44.1 kHz (output data sample rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power-up the IOVDD and AVDD power supplies
# Wait for the IOVDD and AVDD power supplies to settle to a steady-state operating voltage range.
# Wait for 1 ms.
#
# Wake-up the device with an I2C write into P0_R2 using an internal AREG
w 9C 02 81
#
# Enable input Ch-1 and Ch-2 by an I2C write into P0_R115
w 9C 73 C0
#
# Enable ASI output Ch-1 and Ch-2 slots by an I2C write into P0_R116
w 9C 74 C0
#
# Power-up the ADC, MICBIAS, and PLL by an I2C write into P0_R117
w 9C 75 E0
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data via the host on the ASI bus with a TDM protocol 32-bits channel wordlength
```

9.2.1.3 Application Curves

Measurements are done on the EVM by feeding the device analog input signal using audio precision.

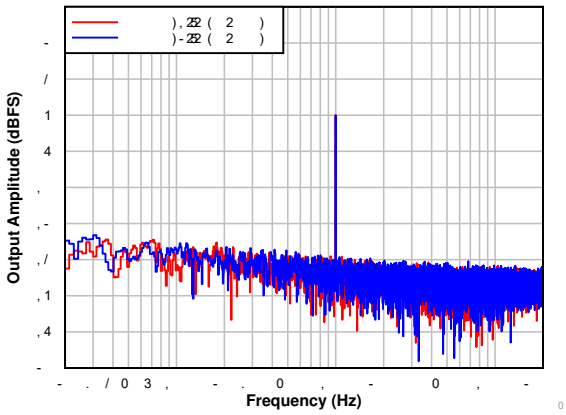


Figure 9-2. FFT With a –60-dBr Input With DRE Enabled

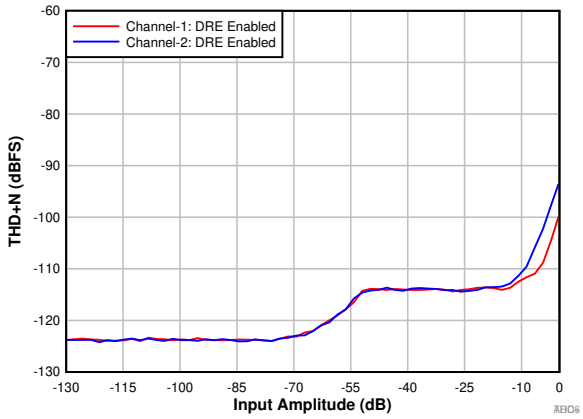


Figure 9-3. THD+N vs Input Amplitude With DRE Enabled

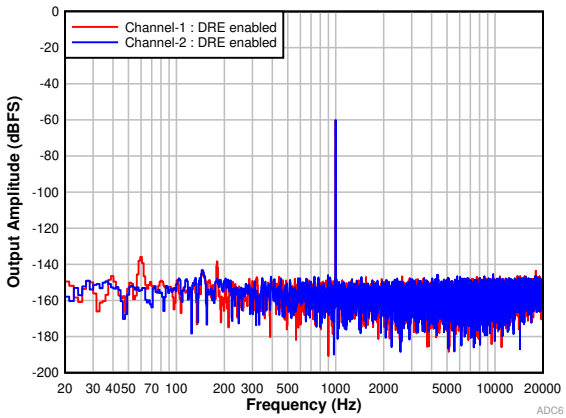


Figure 9-4. FFT With a –60-dBr Input With DRE Disabled

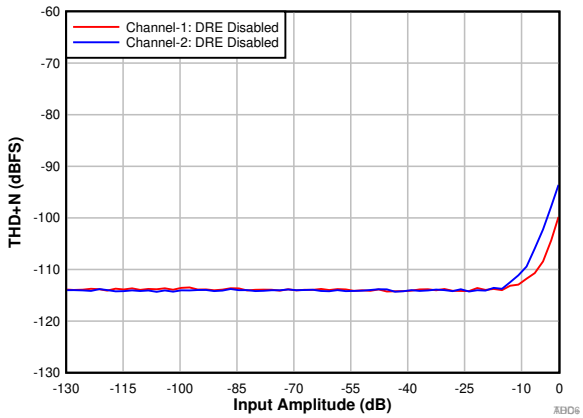


Figure 9-5. THD+N vs Input Amplitude With DRE Disabled

9.2.2 Four-Channel Digital PDM Microphone Recording

Figure 9-6 shows a typical configuration of the PCM6120-Q1 for an application using four digital PDM MEMS microphones with simultaneous recording operation using an I^2C control interface and the TDM audio data slave interface. If the MICBIAS output is not used in the system then the 1 µF capacitor for the MICBIAS pin is not must.

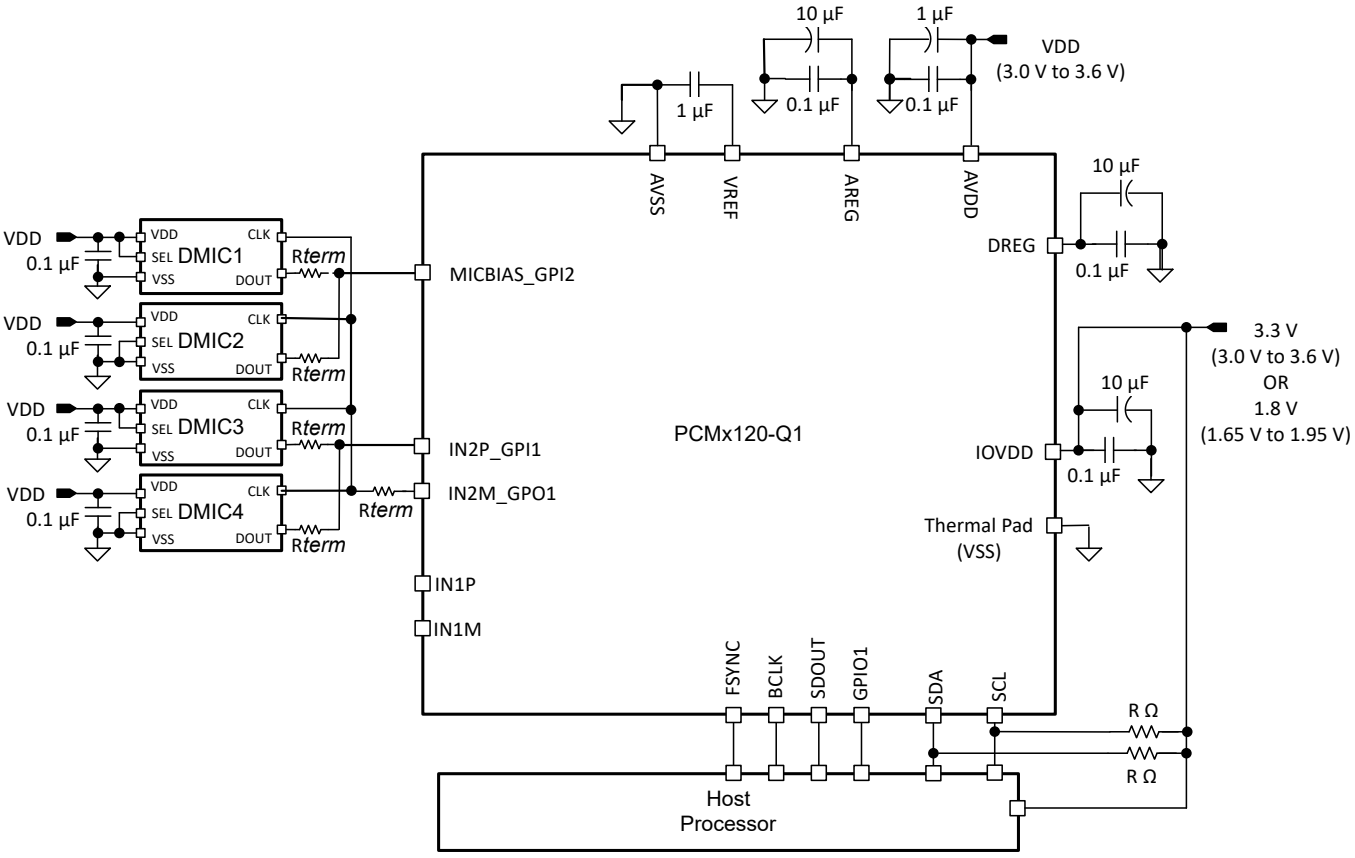


Figure 9-6. Four-Channel Digital PDM Microphone Recording Diagram

9.2.2.1 Design Requirements

Table 9-2 lists the design parameters for this application.

Table 9-2. Design Parameters

KEY PARAMETER	SPECIFICATION
AVDD	3.3 V
AVDD supply current consumption	>8 mA (PLL on, four-channel recording, f_S = 48 kHz)
IOVDD	1.8 V or 3.3 V

9.2.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM6120-Q1 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies
   b. Wait for at least 1 ms to allow the device to initialize the internal registers initialization
   c. The device now goes into sleep mode (low-power mode < 10 µA)
2. Transition from sleep mode to active mode whenever required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
   d. Configure channel 1 to channel 2 (CHx_INSRC) for the digital microphone as the input source for recording
   e. Configure GPO1 (GPO1_CFG) and GPIO1 (GPIO1_CFG) as the PDMCLK output
   f. Configure GPIx (GPI1x_CFG) as PDMDINx
   g. Enable all desired input channels by writing to P0_R115
   h. Enable all desired audio serial interface output channels by writing to P0_R116
   i. Power-up the ADC and PLL by writing to P0_R117
   j. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a.

      See the *Section 8.3.2* section for supported sample rates and the BCLK to FSYNC ratio.
   k. The device recording data is now sent to the host processor using the TDM audio serial data bus
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
   a. Enter sleep mode by writing to P0_R2 to enable sleep mode
   b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
   c. Read P0_R119 to check the device shutdown and sleep mode status
   d. If the device P0_R119_D7 status bit is 1'b1 then stop FSYNC and BCLK in the system
   e. The device now goes into sleep mode (low-power mode < 10 µA) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
   d. The device recording data are now sent to the host processor using the TDM audio serial data bus
5. Repeat step 3 and step 4 as required for mode transitions and step 2 to step 4 for configuration changes

9.2.2.2.1 Example Device Register Configuration Script for EVM Setup

This section provides a typical EVM I²C register control script that shows how to set up the PCM6120-Q1 in a four-channel digital PDM microphone recording mode.

```
# Key: w 9C XX YY ==> write to I2C address 0x9C, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. There are
# other valid sequences depending on which features are used.
#
# See the PCM6120-Q1EVM user guide for jumper settings and audio connections.
#
# PDM 4-channel : PDMDIN1 - Ch1 and Ch2, PDMDIN2 - Ch3 and Ch4
#
# FSYNC = 44.1 kHz (output data sample rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power-up the IOVDD and AVDD power supplies
# Wait for the IOVDD and AVDD power supplies to settle to a steady state operating voltage range.
# Wait for 1 ms.
#
# Wake-up the device by an I2C write into P0_R2 using an internal AREG
w 9C 02  81
#
# Configure CH2_INSRC as a digital PDM input by an I2C write into P0_R65
w 9C 41 40
#
# Configure MICBIAS_GPI2 as a digital PDM input by an I2C write into P0_R59
w 9C 3B 70
#
# Configure GPO1 as PDMCLK by an I2C write into P0_R34
w 9C 22 41
#
# Configure GPI1 and GPI2 as PDMDIN1 and PDMDIN2 by an I2C write into P0_R43
w 9C 2B 45
#
# Enable input Ch-1 to Ch-4 by an I2C write into P0_R115
w 9C 73 F0
#
# Enable ASI output Ch-1 to Ch-4 slots by an I2C write into P0_R116
w 9C 74 F0
#
# Power-up the ADC and PLL by an I2C write into P0_R117
w 9C 75 60
#
# Apply FSYNC = 44.1 kHz and BCLK = 11.2896 MHz and
# Start recording data via the host on the ASI bus with a TDM protocol 32-bits channel wordlength
```

9.3 What to Do and What Not to Do

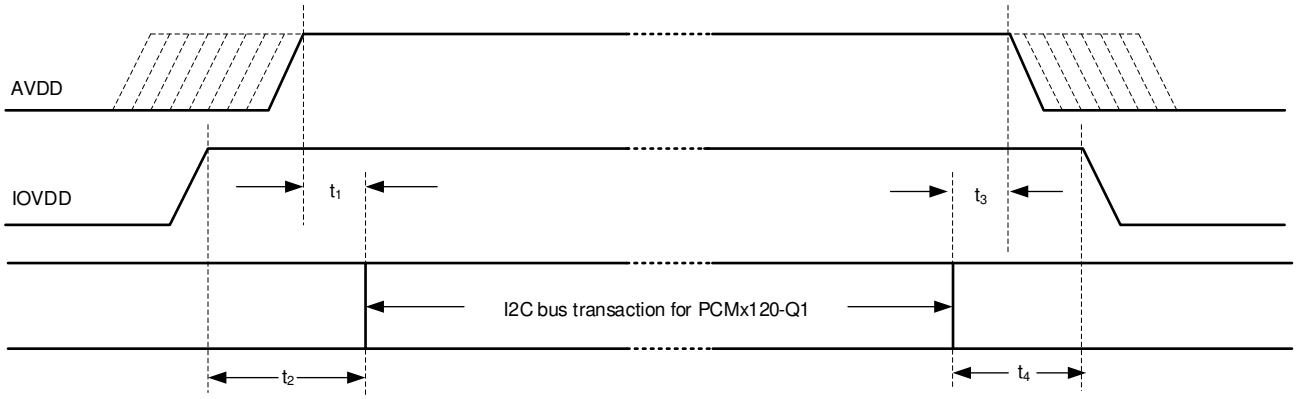
In the VAD mode of operation, there are some limitations on interrupt generation when auto wake up is enabled. For details about these limitations, see the *Using the Voice Activity Detector (VAD) in the TLV320ADC5120 and TLV320ADC6120* application report.

The automatic gain controller (AGC) feature has some limitation when using sampling rates lower than 44.1 kHz. For further details about this limitation, see the *Using the Automatic Gain Controller (AGC) in TLV320ADCx120 Family* application report.

10 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all supplies are stable, then only initiate the I^2C transactions to initialize the device.

For the supply power-up requirement, t_1 and t_2 must be at least 2 ms to allow the device to initialize the internal registers. See the *Section 8.4* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_3 and t_4 must be at least 10 ms. This timing (as shown in Figure 10-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.



Make sure that the supply ramp rate is slower than 1 V/µs and that the wait time between a power-down and a power-up event is at least 100 ms. For supply ramp rate slower than 0.1 V/ms, host device must apply a software reset as first transaction before doing any device configuration. Make sure all digital input pins are at valid input levels and not toggling during supply sequencing.

The PCM6120-Q1 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG. However, if the AVDD voltage is less than 1.98 V in the system, then short the AREG and AVDD pins onboard and do not enable the internal AREG by keeping the AREG_SELECT bit to 1b'0 (default value) of P0_R2. If the AVDD supply used in the system is higher than 2.7 V, then the host device can set AREG_SELECT to 1'b1 while exiting sleep mode to allow the device internal regulator to generate the AREG supply.

11 Layout

11.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- The supply decoupling capacitors must be used ceramic type with low ESR.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

11.2 Layout Example

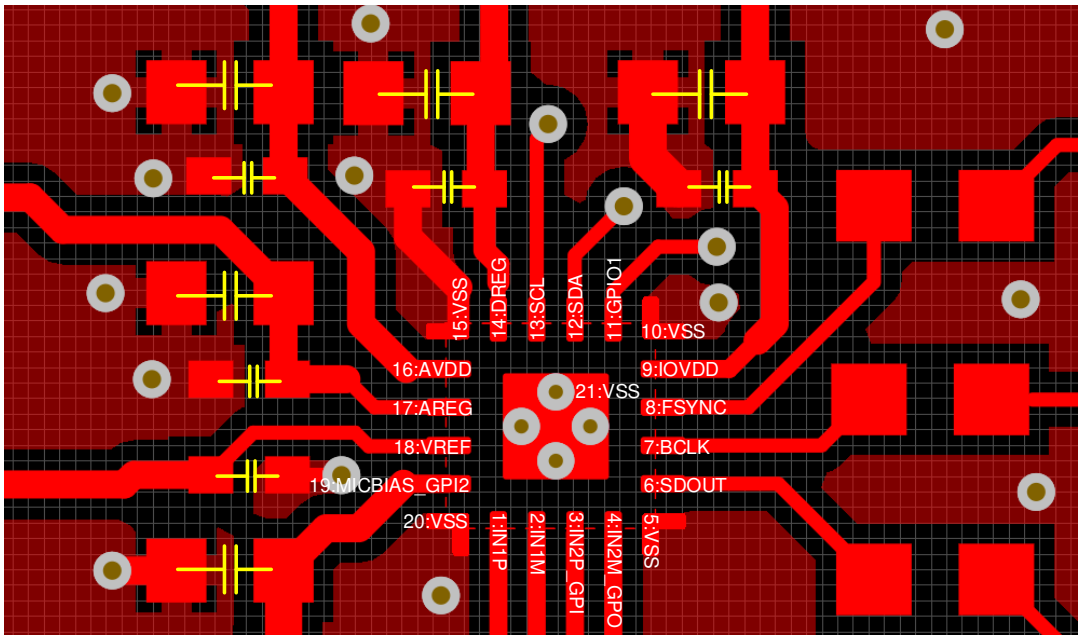


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Multiple TLV320ADCx140 & TLV320ADCx120 Multiple TLV320ADCx140 Devices With Shared TDM and I²C Bus* application report
- Texas Instruments, *Configuring and Operating TLV320ADCx120 as an Audio Bus Master* application report
- Texas Instruments, *TLV320ADCx120 Sampling Rates and Programmable Processing Blocks Supported* application report
- Texas Instruments, *TLV320ADCx140 & TLV320ADCx120 Programmable Biquad Filter Configuration and Applications* application report
- Texas Instruments, *TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios* application report
- Texas Instruments, *TLV320ADCx140 & TLV320ADCx120 Integrated Analog Anti-Aliasing Filter and Flexible Digital Filter* application report
- Texas Instruments, *Using the Automatic Gain Controller (AGC) in TLV320ADCx120 Family* application report
- Texas Instruments, *Using the Voice Activity Detector (VAD) in the TLV320ADCx120 and PCMD3140 devices* application report
- Texas Instruments, *Input Common Mode Tolerance and High CMRR modes for TLV320ADCx120 devices* application report
- Texas Instruments, *Using the Dynamic Range Enhancer (DRE) and Dynamic Range Compressor (DRC) in TLV320ADC5120/6120* application report
- Texas Instruments, *ADCx120EVM-PDK Evaluation module* user's guide
- Texas Instruments, PurePath™ Console Graphical Development Suite for Audio System Design and Development

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

Burr-Brown™, PurePath™, and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

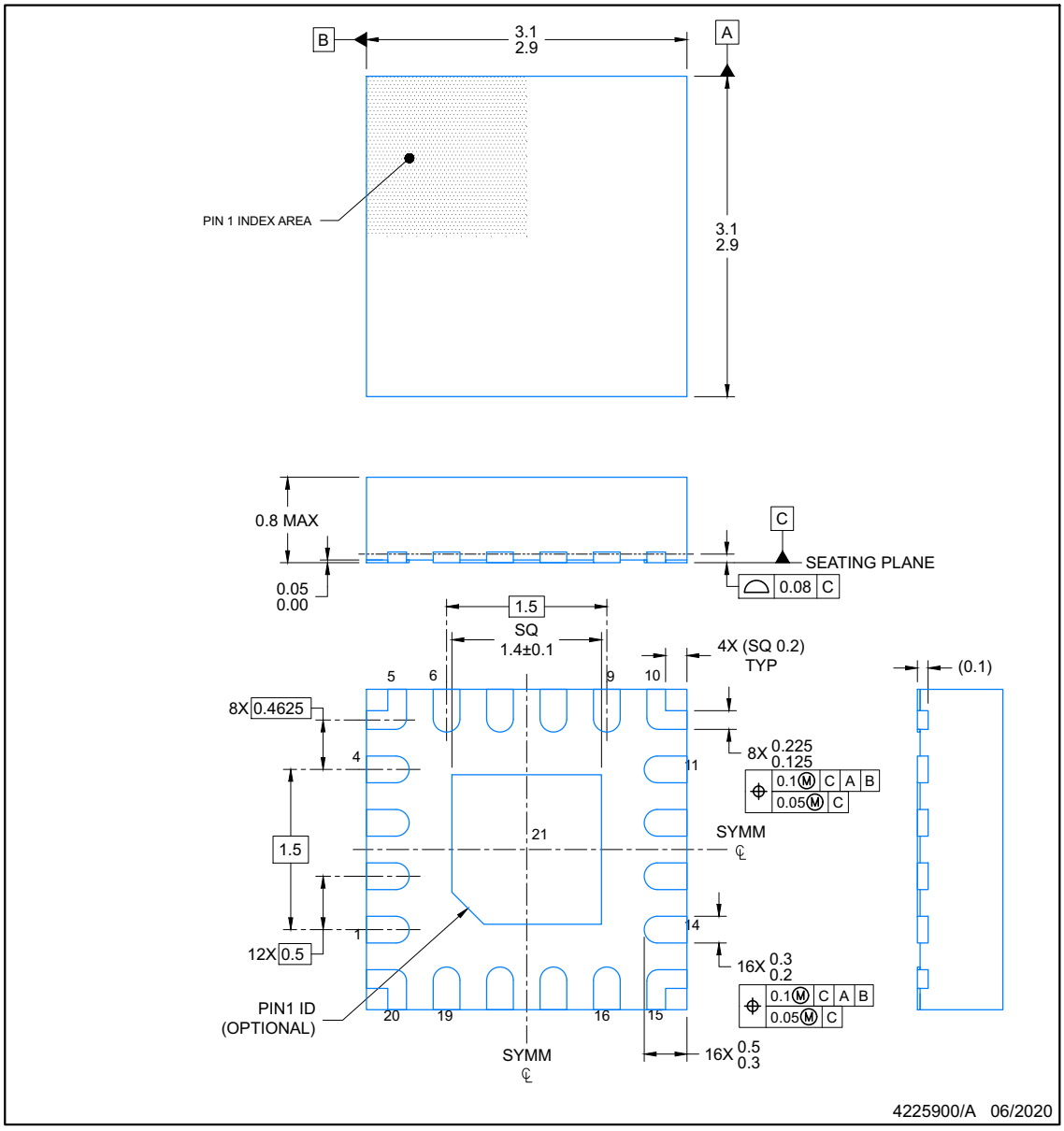
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

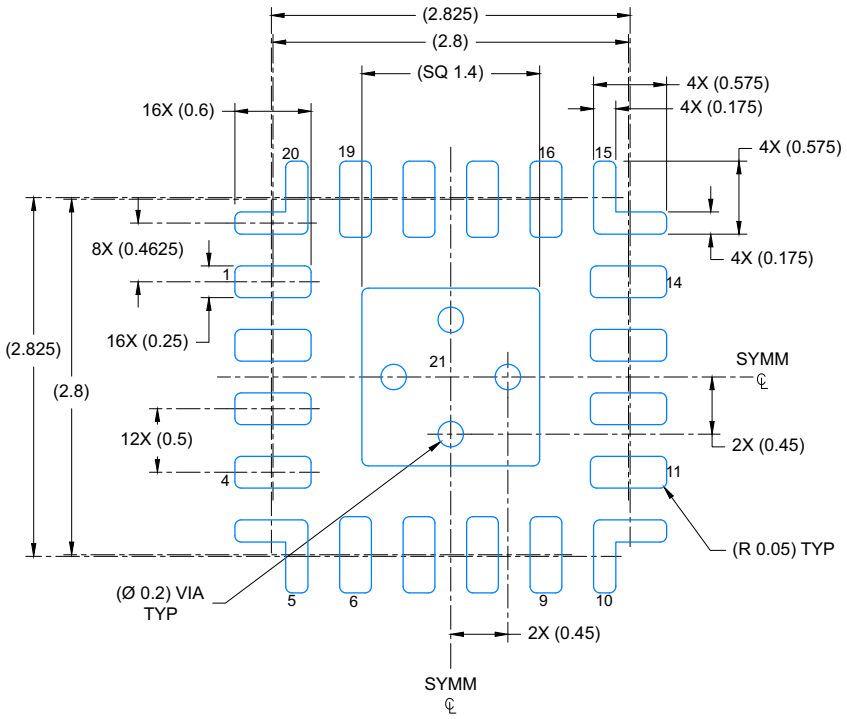
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

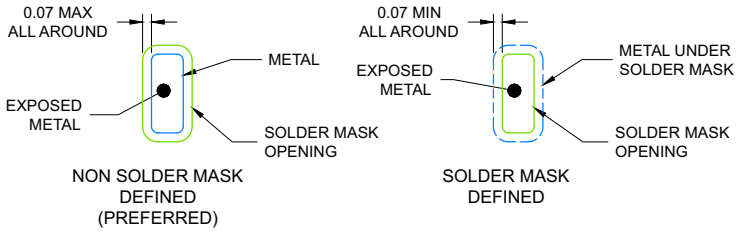
RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225900/A 06/2020

NOTES: (continued)

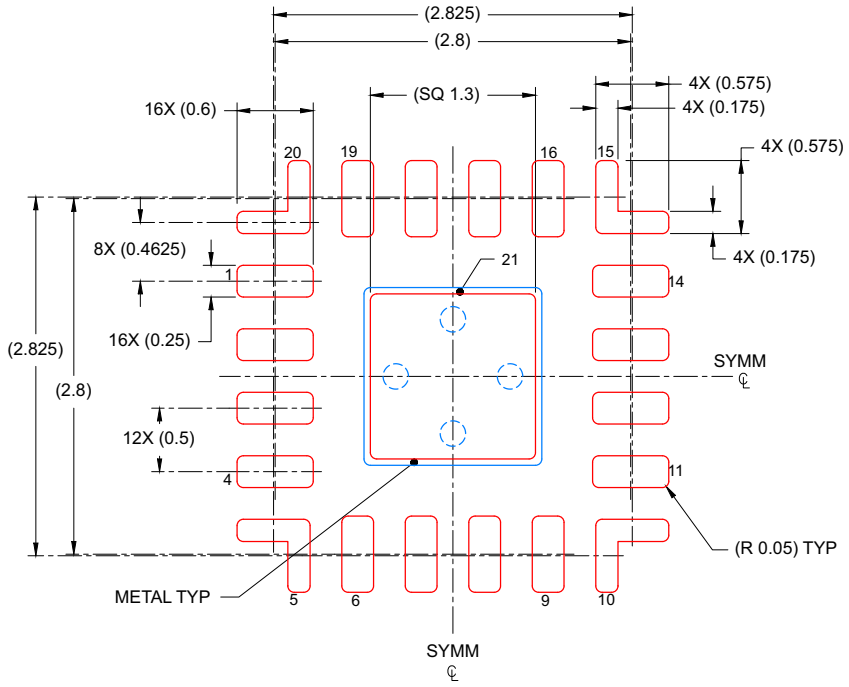
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0020A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 20X

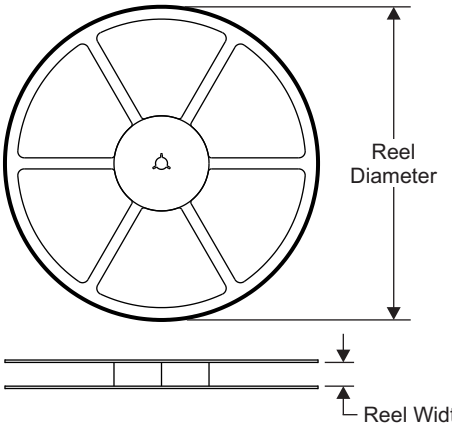
4225900/A 06/2020

NOTES: (continued)

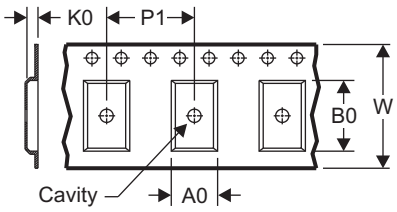
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

13.1 Tape and Reel Information

REEL DIMENSIONS

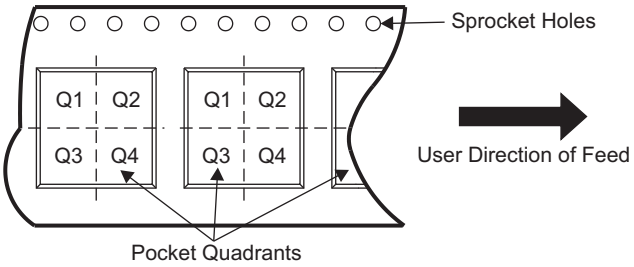


TAPE DIMENSIONS



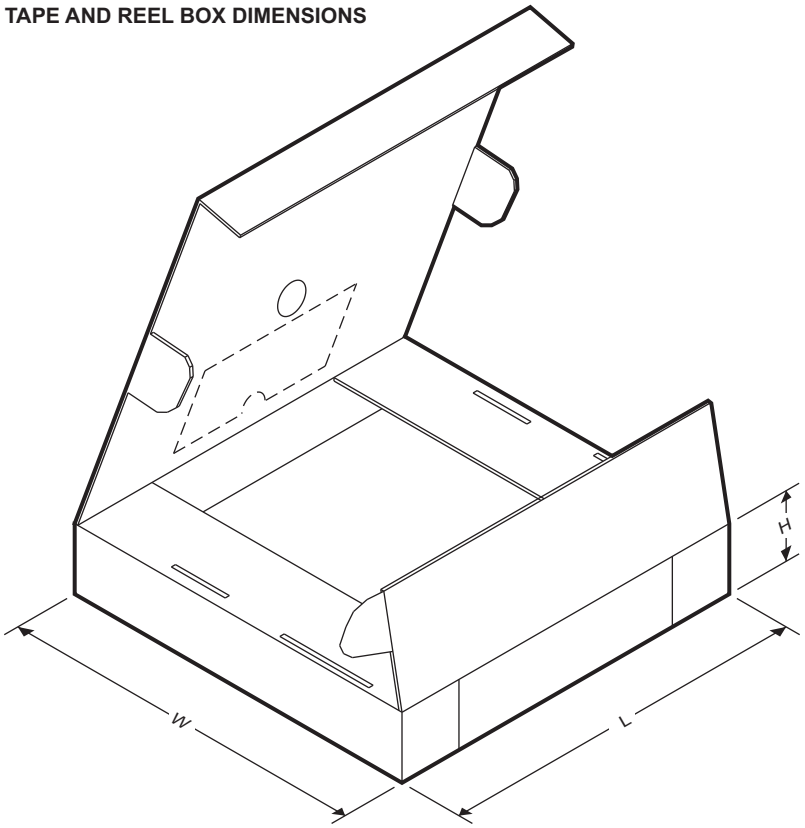
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XCM6120QRTERQ1	WQFN	RTE	20	3000	330	12.4	3.3	3.3	1.1	8	12	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XCM6120QRTERQ1	WQFN	RTE	20	3000	367	367	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM6120QRTERQ1	ACTIVE	WQFN	RTE	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6120Q	Samples
XCM6120QRTERQ1	ACTIVE	WQFN	RTE	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

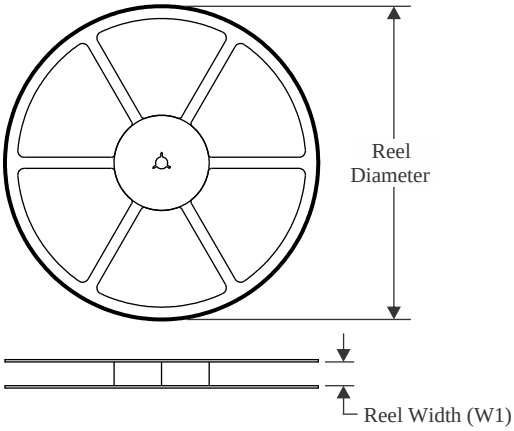
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

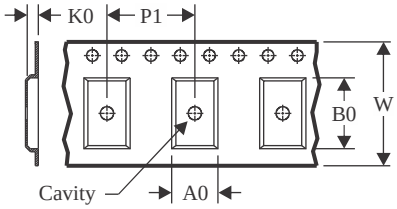
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

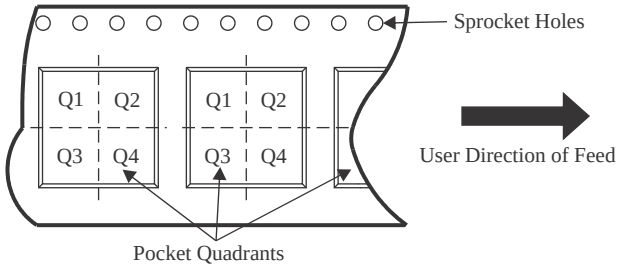


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

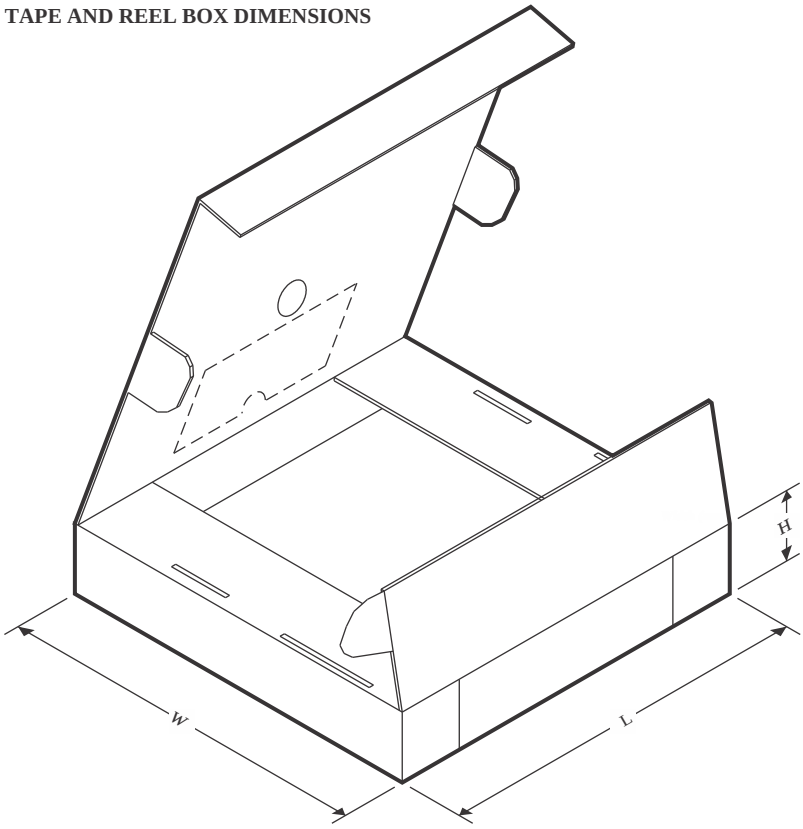
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM6120QRTERQ1	WQFN	RTE	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

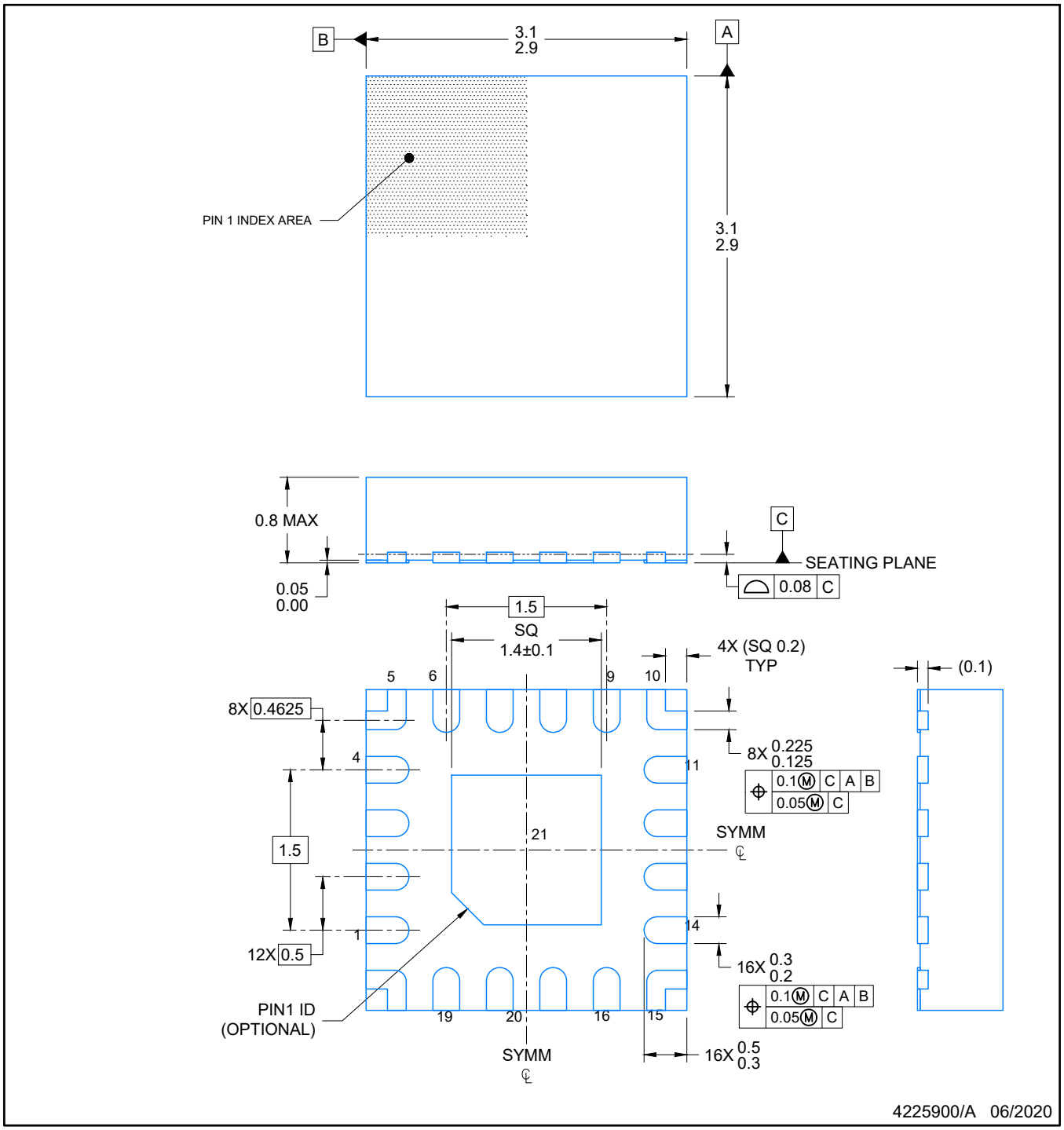
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM6120QRTERQ1	WQFN	RTE	20	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RTE0020A

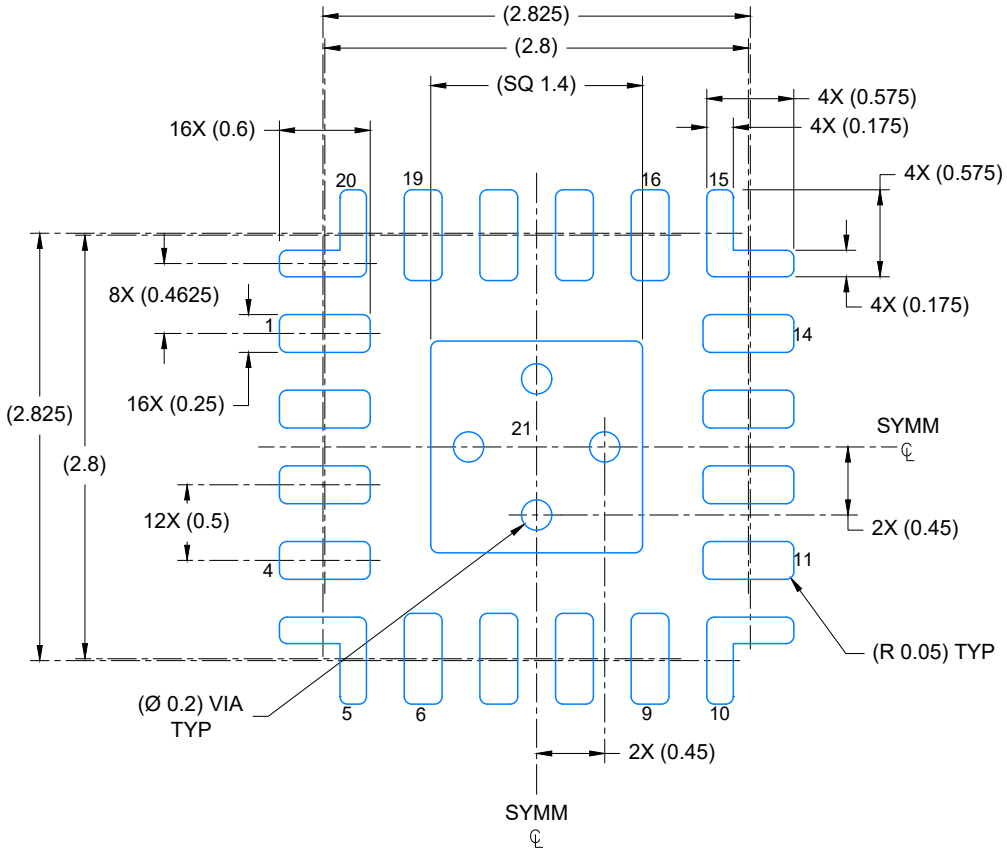
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

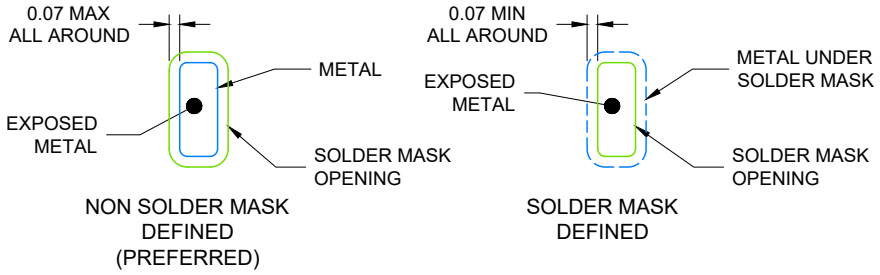


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

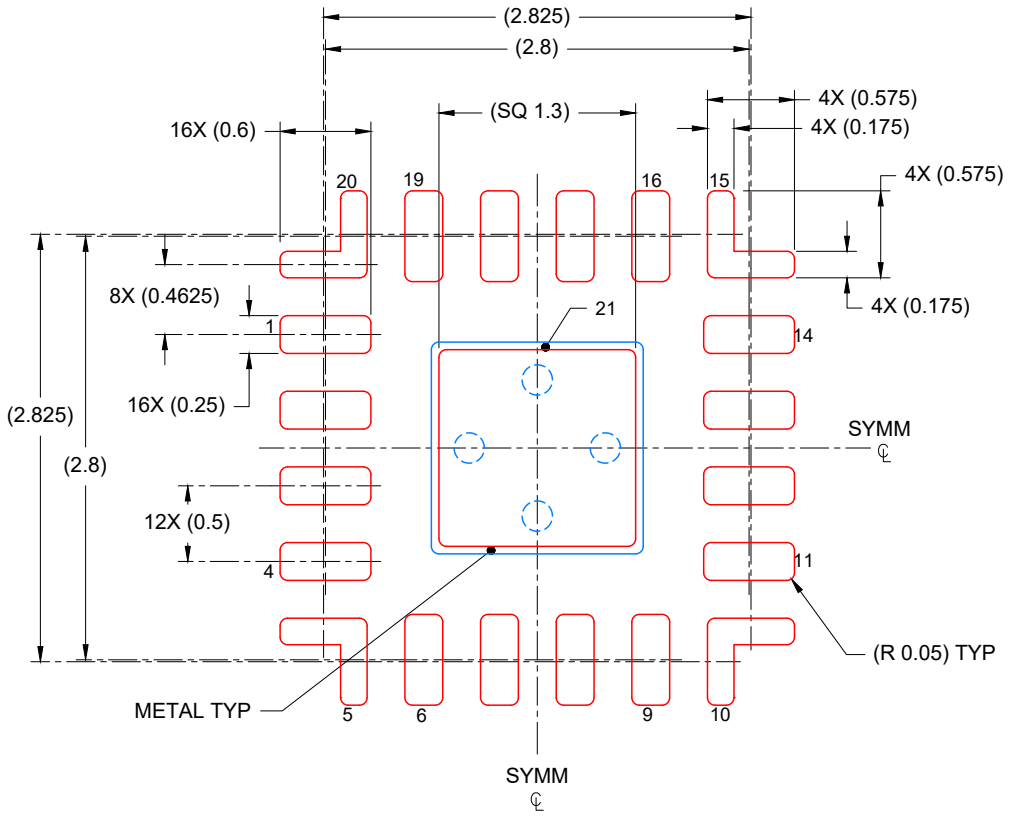


SOLDER MASK DETAILS

4225900/A 06/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 20X

4225900/A 06/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PGA460 Ultrasonic Signal Processor and Transducer Driver

1 Features

- Fully Integrated Solution for Ultrasonic Sensing
- Complimentary Low-Side Drivers With Configurable Current Limit Supporting Both Transformer Based and Direct Drive Topology for Transducer Excitation
- Single Transducer for Both Burst/Listen or a Transducer Pair, One for Burst and the Other for Listen Operation
- Low-Noise Receiver With Programmable 6-Point Time-Varying Gain (32 to 90 dB) With DSP (BPF, Demodulation) for Echo Envelope Detection
- Two Presets of 12-Point Time-Varying Threshold for Object Detection
- Timers to Measure Multiple Echo Distance and Duration
- Integrated Temperature Sensor
- Record Time for Object Detection up to 11 m
- 128 Bytes of RAM for Echo Recording
- 42 Bytes of User EEPROM to Store Configuration for Fast Initialization
- One-Wire High-Voltage Time-Command Interface or USART Asynchronous Interface
- CMOS Level USART Interface
- Sensor Diagnostics (Decay Frequency and Time, Excitation Voltage), Supply, and Transceiver Diagnostics.

2 Applications

- Ultrasonic Radar
- Object distance and Position Sensing
- Presence and Proximity Detection
- Drone and Robotics Landing Assist and Obstacle Detection
- Occupancy and Motion Sensors

3 Description

The PGA460 device is a highly-integrated system on-chip ultrasonic transducer driver and signal conditioner with an advanced DSP core. The device has a complimentary low-side driver pair that can drive a transducer either in a transformer based topology using a step-up transformer or in a direct-drive topology using external high-side FETs. The device can receive and condition the reflected echo signal for reliable object detection. This feature is accomplished using an analog front-end (AFE) consisting of a low-noise amplifier followed by a programmable time-varying gain stage feeding into an ADC. The digitized signal is processed in the DSP core for both near-field and far-field object detection using time-varying thresholds.

The main communication with an external controller is achieved by either a time-command interface (TCI) or a one-wire USART asynchronous interface on the IO pin, or a CMOS-level USART interface on the RXD and TXD pins. The PGA460 can be put in ultra-low quiescent current low-power mode to reduce power consumption when not in use and can be woken up by commands on the communication interfaces.

The PGA460 also includes on-chip system diagnostics which monitor transducer voltage during burst, frequency and decay time of transducer to provide information about the integrity of the excitation as well as supply-side and transceiver-side diagnostics for overvoltage, undervoltage, overcurrent and short-circuit scenarios.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA460	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram (Transformer Drive)

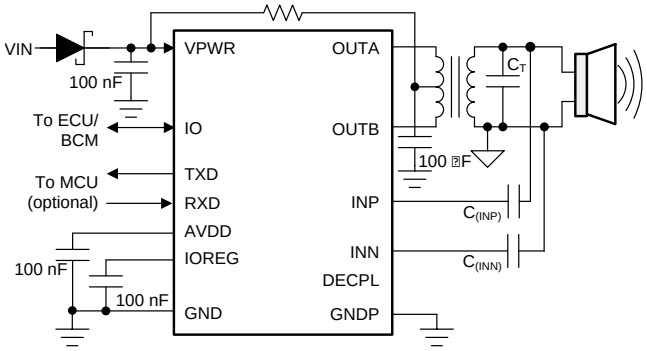


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2017) to Revision B **Page**

- Changed Functional Block Diagram's GND and GNDP pin designators for correct grounding of the Output Driver. ... 11
- Updated tablenotes of Table 3 ... 38
- Added sentence: USART Synchronous Mode is identical to a Serial Peripheral Interface (SPI) without a chip-select because the addressing is handled by the three-bit UART_ADDR value to enable up to eight devices on a single bus. ... 43
- Added sentence: The temperature measurement's sample and conversion time requires at least 100 us after the temperature measurement command is issued. Do not send other commands during this time to allow the temperature value to properly update ... 51

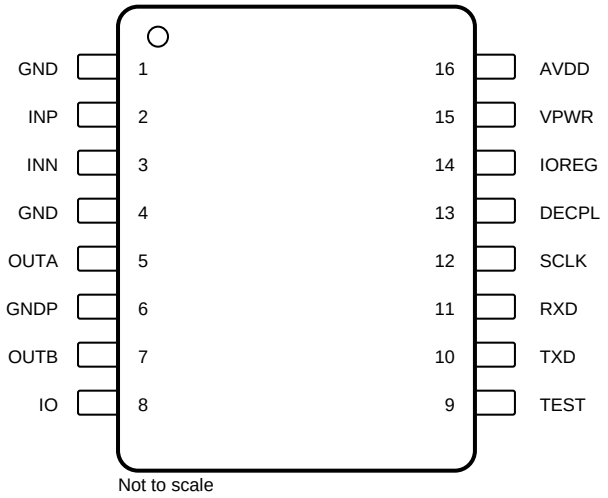
Changes from Original (April 2017) to Revision A **Page**

- Added zero padding information to the *CONFIGURATION/STATUS Command* section ... 32
- Changed UART interface parameter text from: 1 stop bit to: 2 stop bit ... 34
- Changed interfield wait time text from: optional to: required for 1 stop bit ... 34
- Added sentence: The sync field (0x55) is not included as part of the checksum calculation. ... 37
- Updated content and added tablenotes to Table 3 ... 38
- Added sentence: The diagnostic field is included in the slave generated checksum calculation. ... 41
- Added subsection *Direct Data Burst Through USART Synchronous Mode* ... 47
- Added Equation 8 ... 52
- Added sentence: This includes all threshold timing and level values. ... 54
- Updated *UART and USART Communication Examples* content ... 57
- Updated content in Table 101 ... 107
- Added content to *Application Curves* ... 109

- Added content to *Direct-Driven (Transformer-Less) Method* and changed Figure 141 such that a GND node is present at $XDCR_{Negative}$ and C_{INN} 110
- Changed text from: TDK EPCOS B78416A2232A03 Transformer, muRata MA40H1S-R transducer to: Fairchild FDC6506P p-channel MOSFET, muRata MA40H1S-R transducer 111

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	P	Ground
2	INP	I	Positive transducer receive
3	INN	I	Negative transducer receive
4	GND	P	Ground
5	OUTA	O	Transducer driver output A
6	GNDP	P	Power ground
7	OUTB	O	Transducer driver output B
8	IO	I/O	Time-command interface data input and output
9	TEST	I/O	Test output pin
10	TXD	O	USART interface transmit
11	RXD	I	USART interface receive
12	SCLK	I	USART synchronous-mode clock input
13	DECPL	O	Decoupling transistor gate drive
14	IOREG	P	I/O buffer voltage regulator capacitor
15	VPWR	P	Power-supply voltage
16	AVDD	P	Analog voltage-regulator capacitor

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VPWR	–0.3	30	V
	IO	–0.3	30	
	INP, INN	–0.3	2	V
	TEST, SCLK, RXD	–0.3	5.5	V
Output voltage	AVDD	–0.3	2	V
	IOREG, DECPL, TEST, TXD	–0.3	5.5	
	OUTA, OUTB	–0.3	30	
Ground voltage	GNDP, GND	–0.3	0.3	V
Sink current	OUTA, OUTB		500	mA
Operating junction temperature		–40	125	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	Corner Pins (1, 8, 9, 16)	±750	
			All Other Pins	±500	
		IEC 61000-4-2 contact discharge	IO pin	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

			MIN	MAX	UNIT
V_{VPWR_XF}	Supply input for transformer topology		6	15	V
V_{VPWR_DD}	Supply input for direct drive topology		6	28	V
V_{IO}	IO pin	IO	–0.1	V_{PWR}	V
V_{INx}	Transducer receive input	INP, INN	–0.1	0.9	V
V_{DIG_IO}	Digital I/O pins	RXD, TEST, SCLK	–0.1	V_{IOREG}	V
V_{GND}	Ground pins	GNDP, GND	–0.1	0.1	V
I_{LPM}	V_{PWR} Input current	Low Power Mode Enabled		500	µA
I_{BURST}		During Ultrasonic Burst		500	mA
T_A	Operating free-air temperature		–40	105	°C
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PGA460 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Internal Supply Regulators Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD}	Internal analog supply voltage	I_{AVDD} = 5 mA	1.74	1.8	1.9	V
$I_{VPWR\_RX\_ONLY}$	Supply current from VPWR pin during listen only mode.	V_{VPWR} = 14 V; no bursting; Listen only active		12		mA
V_{IOREG_33}	Digital IO supply voltage	V_{TEST} = 0 V during power-up ; I_{IOREG} = 2 mA	2.95	3.3	3.65	V
V_{IOREG_50}		V_{TEST} ≥ 2 V during power-up ; I_{IOREG} = 2 mA; V_{VPWR} > 7.5 V	4.45	5	5.65	
I_{LIM_AVDD}	AVDD current limit	AVDD short to GND	40		150	mA
I_{LIM_IOREG}	IOREG current limit	IOREG short to GND	10		50	mA
V_{OV_AVDD}	AVDD overvoltage threshold		1.95		2.3	V
V_{UV_AVDD}	AVDD undervoltage threshold		1.29		1.53	V
$V_{OV\_IOREG\_33}$	IOREG overvoltage threshold	V_{TEST} = 0 V during power-up	3.6		4.6	V
$V_{UV\_IOREG\_33}$	IOREG undervoltage threshold	V_{TEST} = 0 V during power-up	2.57		2.9	V
$V_{UV\_IOREG\_50}$		V_{TEST} ≥ 2 V during power-up	3.8		4.5	
V_{OV_VPWR}	VPWR overvoltage threshold	VPWR_OV_TH = 0x0	11	12.3	15	V
		VPWR_OV_TH = 0x1	16	17.7	21	
		VPWR_OV_TH = 0x2	21.5	22.8	27	
		VPWR_OV_TH = 0x3	27	28.3	31	
V_{UV_VPWR}	VPWR undervoltage threshold		5.25		6	V
t_{ON_REG}	AVDD and IOREG power-up time	V_{VPWR} = 6 V			10	ms

6.6 Transducer Driver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLAMP_DRV}	Driver clamping voltage	Driver switched off	30			V
$I_{PULSE\_MAX\_DRV}$	Maximum driver pulse current	V_{OUTA},V_{OUTB} = 6 V: F_{SW} = 30 kHz; T_A = 105°C			500	mA
$RDSON_{DRV}$	MOSFET on resistance	I_{DRAIN} = 500 mA: T_A = 105°C; DIS_CL=1		4.8	8	Ω
E_{DIS_BURST}	Energy dissipated during burst				6.4	mJ
I_{LEAK_DRV}	Leakage current	V_{OUTA},V_{OUTB}=14 V	–1		1	µA
$I_{CLAMP\_DRV\_0}$	Current clamping range for minimum code setting	V_{VPWR}>7 V;CURR_LIM1 = CURR_LIM2= 0	15	50	75	mA
$I_{CLAMP\_DRV\_63}$	Current clamping range from maximum code setting	V_{VPWR}>7 V;CURR_LIM1 = CURR_LIM2= 63	450	500	570	mA
$I_{STEP\_SIZE\_CLAMP\_DRV}$	Step size (change in current from value at previous step)		5.2	7.2	9.2	mA

Transducer Driver Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW_LOW}	Configurable switching frequency	FREQ_SHIFT = 0	30		80	kHz
f_{SW_HIGH}		FREQ_SHIFT = 1	180		480	

6.7 Transducer Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$GAIN_{RNG\_TOT\_RCV}$	Total receiver amplification gain range	$F_{SW} = F_{SW\_LOW}, F_{SW\_HIGH}$; T_A = –40°C to +105°C	32		90	dB
$GAIN_{RNG\_RCV}$	Receiver amplification gain	AFE_GAIN_RNG = 0x03	32		64	
		AFE_GAIN_RNG = 0x02	46		78	
		AFE_GAIN_RNG = 0x01	52		84	
		AFE_GAIN_RNG = 0x00	58		90	
$GAIN_{NSTEP\_RCV}$	Gain adjustment steps			64		
$GAIN_{STEP\_SIZE\_RCV}$	Gain adjustment step size		0.2	0.5	0.8	dB
$GAIN_{THRM\_DRFT\_RCV}$	Gain thermal drift	F_{SW} = 30 kHz; T_A = –40°C to +105°C; Gain = 58.5 dB	–3.5%		3.5%	
Z_{INP_RCV}	Input impedance	F_{SW} < 80 kHz	300			kΩ
N_{RCV}	Noise floor	F_{SW} = 58 kHz; T_A = 105°C; BW = 4 kHz		7		nV/sqrt(Hz)

6.8 Analog to Digital Converter Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INP_ADC}	Input voltage range		0		V_{AVDD}	V
V_{REF_ADC}	Voltage reference			V_{AVDD}		
N_{ADC}	Resolution			12		Bits
t_{CONV}	Conversion time			1		µs

6.9 Digital Signal Processing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$FREQ_{CENTER\_BPF}$	Band-pass filter center frequency	Normalized to driver frequency		1		
BW_{BPF}	Band-pass filter band width		2		8	kHz
N_{BPF}	Band-pass filter adjustable steps			4		
$FREQ_{STEP\_SIZE\_BPF}$	Band-pass filter step size			2		kHz
$FREQ_{CUTOFF\_LPF}$	Low-pass filter cutoff frequency		1		4	kHz
N_{LPF}	Low-pass filter adjustable steps			4		
$FREQ_{STEP\_SIZE\_LPF}$	Low-pass filter step size			1		kHz

6.10 Temperature Sensor Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{RANGE_SENSE}	Temperature sensor range		–40		125	°C
T_{ACC_SENSE}	Range accuracy	VPWR=12 V;TEMP_GAIN = 0; TEMP_OFF = 0		5		°C

6.11 High-Voltage I/O Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_IO}	High-voltage IO input high level	IO pin	0.6 × V_{VPWR}			V

High-Voltage I/O Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_IO}	High-voltage IO input low level	IO pin			0.4 × V_{VPWR}	V
V_{HYS_IO}	High-voltage input hysteresis	IO pin	0.05 × VPWR		0.175 × VPWR	V
V_{OL_IO}	High-voltage IO output low level	IO pin ; I_{IO} = 10 mA			2	V
R_{PU_IO}	High-voltage IO pullup resistance	IO pin	4	10	16	kΩ
I_{LIM_IO}	Current limit on high-voltage IO	Short to VPWR	40		250	mA

6.12 Digital I/O Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_DIGIO}	Digital input high level	RX and SCLK pin; V_{IOREG}=V_{IOREG_33}/V_{IOREG_50}	0.7*$V_{IO\ REG}$			V
V_{IL_DIGIO}	Digital input low level	RX and SCLK pin; V_{IOREG}=V_{IOREG_33}/V_{IOREG_50}			0.3*$V_{IO\ REG}$	V
V_{HYS_DIGIO}	Digital input hysteresis	RX and SCLK pin	100			mV
V_{OH_DIGIO}	Digital output high level	DECPL and TX pin; I_{DECPL}/I_{TX} = –2 mA; V_{IOREG}=V_{IOREG_33}/V_{IOREG_50}	V_{IOREG} – 0.2			V
V_{OL_DIGIO}	Digital output low level	DECPL and TX pin; I_{DECPL}/I_{TX} = 2mA			0.2	V
$R_{PU\_DIGIO\_RX}$	Digital input pull-up resistance to IOREG	RX pin	90	100	160	kΩ
$R_{PU\_DIGIO\_SCLK}$	Digital input pull-down resistance	SCLK pin	80	100	130	kΩ

6.13 EEPROM Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Bytes_{EE}$	EEPROM memory size	Application and Device Internal		64		Bytes
t_{RET_EE}	EEPROM data retention time	T_A = 105°C			10	Years
$Cycl_{BURN\_EE}$	EEPROM burn cycles				1000	Cycles
t_{PROG_EE}	EEPROM programming time			600		ms

6.14 Timing Requirements

		MIN	NOM	MAX	UNIT
TIME COMMAND INTERFACE					
t_{BIT_TCI}	Bit period	225	300	375	µs
t_{BIT0_TCI}	Logical 0 bit length	150	200	250	µs
t_{BIT1_TCI}	Logical 1 bit length	75	100	125	µs
t_{BLP1_TCI}	BURST/LISTEN (Preset1) command period	328	400	472	µs
t_{BLP2_TCI}	BURST/LISTEN (Preset2) command period	920	1010	1100	µs
t_{LP1_TCI}	LISTEN only (Preset1) command period	697	780	863	µs
t_{LP2_TCI}	LISTEN only (Preset2) command period	503	580	657	µs
t_{CFG_TCI}	Device configuration command period	1170	1270	1370	µs
t_{TEMP_TCI}	Temperature measurement command period	1440	1550	1660	µs
t_{NOISE_TCI}	Noise level measurement command period	2070	2200	2340	µs
t_{DT_TCI}	Command processing dead-time	75	100	125	µs
USART ASYNCHRONOUS INTERFACE					
t_{BIT_UART}	Logical bit length at 19.2 kbps	45.5	52.08	58.6	µs
t_{BITF_UART}	Logical bit length at 115.2 kbps	7.6	8.68	9.76	µs
USART SYNCHRONOUS INTERFACE					
t_{BIT_USART}	Logical bit length at 8 Mbps	55	125		ns

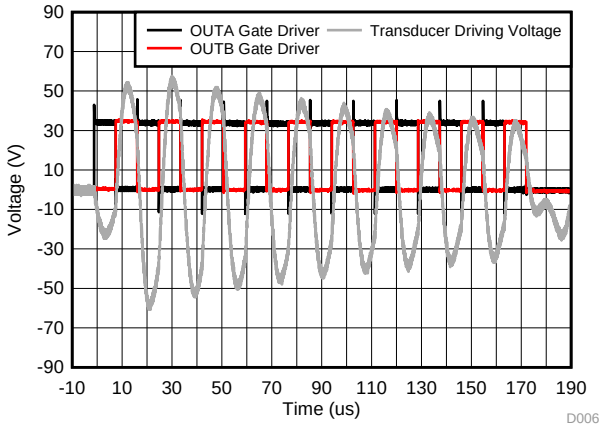
6.15 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CORE_CLK}	Core frequency(1)		15.5	16	16.5	MHz
ACC_{CORE_CLK}	Core frequency accuracy(2)		–4%		4%	
$Baud_{UART}$	USART asynchronous interface baud rate		2.4	19.2	131.5	kbps
$Baud_{USART}$	USART interface synchronous mode baud rate				8	Mbps

(1) At Room Temperature (25°C)
(2) Across Operating Temperature Range (-40°C to 105°C)

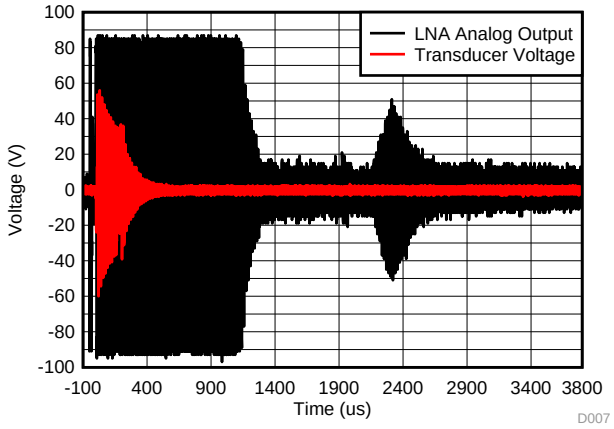
6.16 Typical Characteristics

10 pulses, 400-mA current limit, 58.6-kHz driving frequency



TDK EPCOS B78416A2232A003 transformer
muRata MA58MF14-7N transducer
OUTA/B Gate Driver is scaled up by 10 times

Figure 1. Driver Stage and Resulting Transducer Behavior



TDK EPCOS B78416A2232A003 transformer
muRata MA58MF14-7N transducer
LNA analog output is scaled and shifted. Actual signal is 100 times smaller and common mode is shifted up by 0.9 V

Figure 2. Receiver AFE Output Post-LNA Object at 35 cm

7 Detailed Description

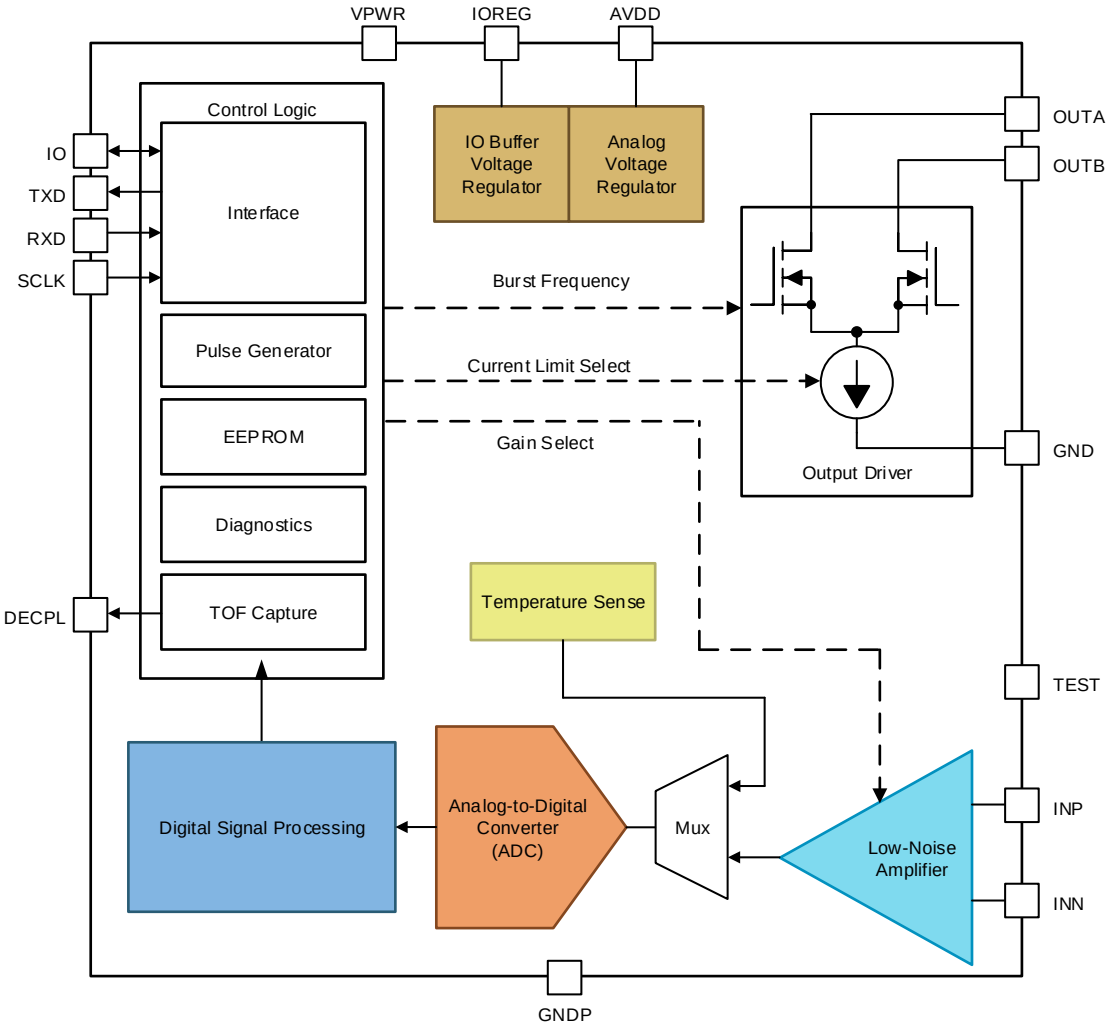
7.1 Overview

The PGA460 device is a signal-conditioning and transducer-driver device for ultrasonic sensing for object or distance sensing. The output driver consists of complimentary low-side drivers capable of driving a center-tap transformer to generate large excitation voltages across an ultrasonic transducer and as a result create the desired sound pressure level (SPL). The output driver can also be configured to be used in direct-drive mode without a transformer using external FETs. The output driver implements configurable current limit for efficient driving of the transformer and configurable bursting frequencies and burst length to be compatible with a large number of transducers.

The analog front-end (AFE) can sense the received echo from the transducer and amplify it for correct object detection. The AFE implements a low-noise amplifier followed by a time-varying gain amplifier that allows signals from objects at a variable distance to be amplified correspondingly. This implementation allows for the maximum dynamic range of the ADC to be used for both near-field and far-field objects in the same recording. An embedded temperature sensor can be used to calibrate the signal conditioner for changes in temperature. The digital signal processing path further filters the received echo and uses time-varying thresholds for accurate detection of objects. Two presets for both bursting and thresholds are available which allow faster detection cycles by saving time required to configure the device between multiple bursts. Most configuration parameters are stored in nonvolatile memory for quick power up, which reduces initialization time.

The PGA460 device provides multiple IO protocols to communicate with the master controller. The device provides a time-command interface and one-wire UART on the VPWR reference IO pin. It also provides both synchronous and asynchronous USART on the TXD, RXD, and SCLK pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-Supply Block

The PGA460 device uses multiple internal regulators as supplies for the internal circuits. The analog voltage regulator (AVDD) requires an external capacitor of 100 nF. The power-supply block generates precision voltage references, current bias, and an internal clock. An additional regulator (IOREG) generates the supply voltage for the USART pins (RXD, TXD, and SCLK), DECPL pin, and TEST pin for their digital functionality. The AVDD and IOREG regulators are not intended to support any external load. The external capacitors are recommended to be placed as close as possible to the related pins (AVDD and IOREG). The PGA460 device starts to power up when a voltage is applied to the VPWR pin. The internal power-on reset (POR) is released when all regulator supplies are in regulation and the internal clock is running. During low-power mode, the IOREG regulator is powered up while the other regulators shut down to conserve power.

Feature Description (continued)

7.3.2 Burst Generation

The PGA460 device has a programmable frequency for the burst and number of pulse by configuring the FREQ and P1_PULSE/P2_PULSE registers.

Use Equation 1 to calculate the frequency of burst for a range of 30 kHz to 80 kHz (FREQ_SHIFT bit set to 0).

$$f_{(DRV)} = 0.2\ \text{kHz} \times f + 30\ \text{kHz} \quad (1)$$

where

- f is the frequency which can be from 0 to 200 as defined in the FREQUENCY register.

The actual driving frequency of the output stage is derived from the core clock frequency using Equation 1 and Equation 2

$$n = \frac{f_{(CORE\_CLK)}}{f_{(DRV)}} \quad (2)$$

where

- n is the ratio by which the main oscillator $f_{(CORE\_CLK)}$ is divided.

The PULSE_P1 and PULSE_P2 registers can range from 0 to 31. When set to a value of M that is greater than 0, the M pulse pairs are generated on the OUTA and OUTB outputs.

7.3.2.1 Using Center-Tap Transformer

The PGA460 device provides efficient burst generation by exciting the primary side of a center-tap transformer connected on the OUTA and OUTB pins through the complementary low-side FETs operating in a current limiting mode. The frequency of the burst is from 30 kHz to 80 kHz with the current limit from 50 mA to 500 mA. The frequency of the burst, the current limit for transformer primary current, and the number of burst pulses can be controlled by using the FREQUENCY, CURR_LIM_P1, CURR_LIM_P12, PULSE_P1, and PULSE_P2 parameters, respectively.

Figure 3 shows the functional block diagram for echo generation.

Feature Description (continued)

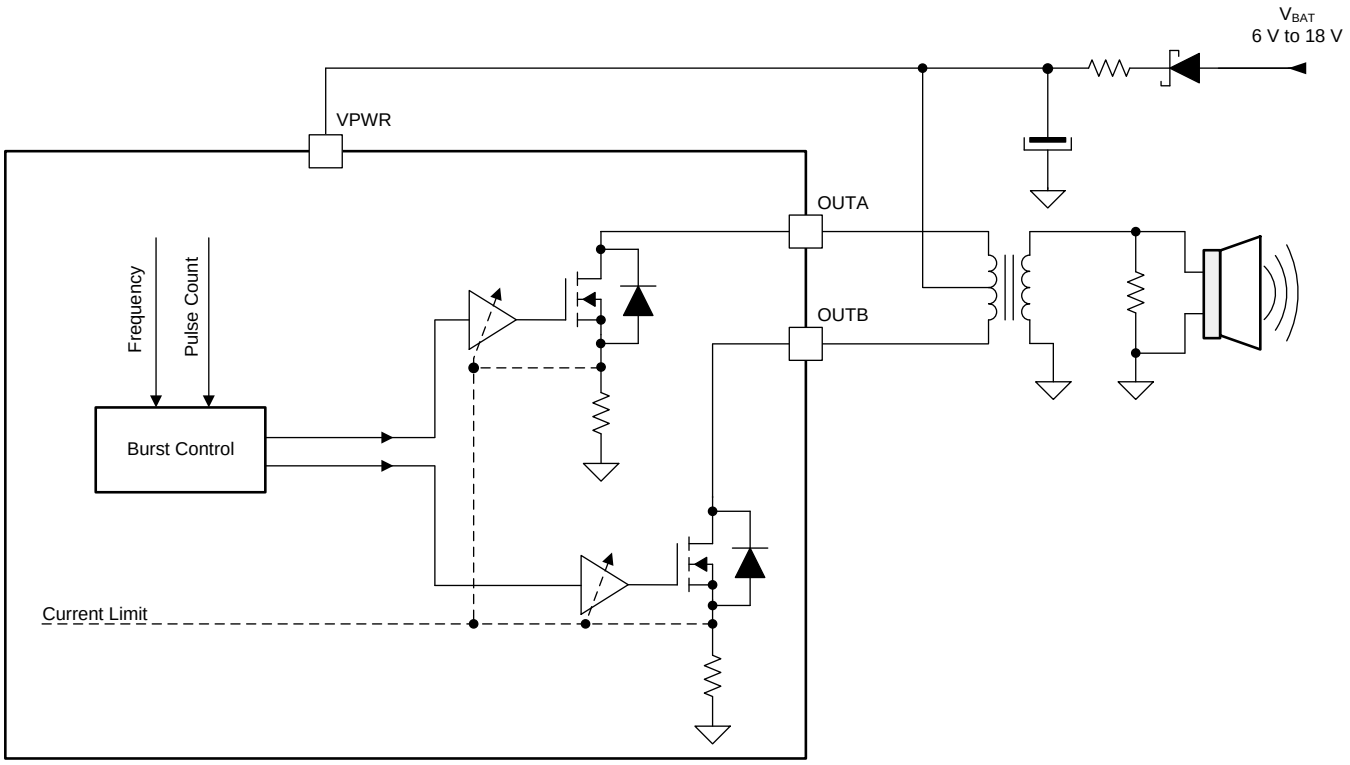


Figure 3. Echo Generation Block Diagram

7.3.2.2 Direct Drive

The complementary low-side drivers can be used in conjunction with an external PMOS FET to provide single-ended direct excitation to the transducer. In this configuration, the internal FETs can be used in a RDSON mode by disabling current limiting feature by setting the DIS_CL bit in the CURR_LIM_P1 register.

An additional dead-time feature can be used in this mode to eliminate the shoot-through currents between the external PMOS FET and internal low-side FETs by configuring the PULSE_DT bit. The burst cycle period of the low-side FETs remains unchanged; however, the deactivation time is reduced by the dead-time programmed value. Figure 4 shows this case.

Feature Description (continued)

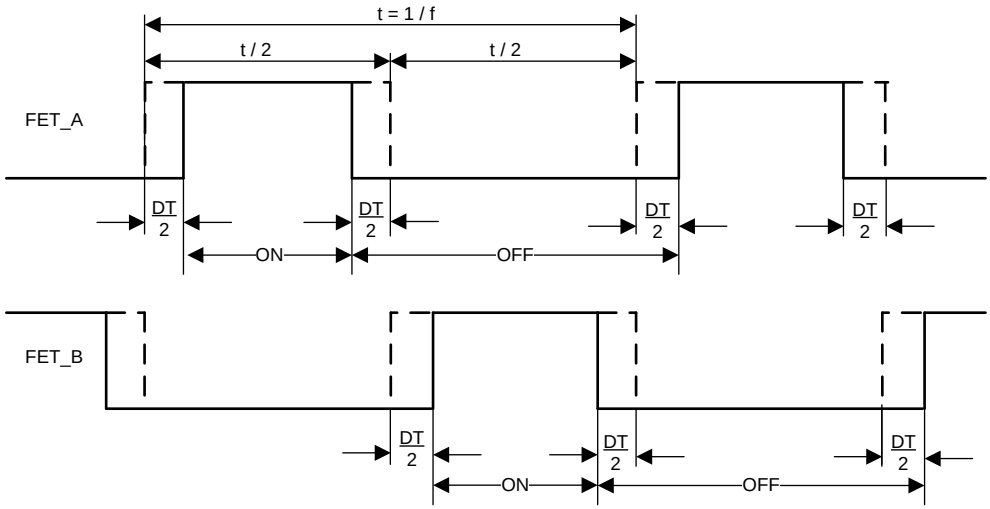


Figure 4. Echo Generation Dead-Time Adjustment

7.3.2.3 Other Configurations

When any of the P1_PULSE or P2_PULSE bits are set to 0, only the OUTA output generates a pulse, while the OUTB output remains in the high-impedance (High-Z) state during this period. This configuration is used to reduce the output voltage when only short distances are required to be detected.

NOTE

- For higher frequency support, the device has an option to shift up the burst frequency range which occurs by setting the FREQ_SHIFT bit in the CURR_LIM_P1 register. When this bit is set, the burst frequency is 6 times higher of the burst frequency selected by the FREQUENCY register. With this bit set, the range of burst frequencies is from 180 kHz to 480 kHz with a step of approximately 1.2 kHz.
- The maximum dead time setting should be less than or equal to t / 8 where t is burst period.

7.3.3 Analog Front-End

The analog front-end (AFE) in the PGA460 device, shown in Figure 5, receives the reflected echo from the object, amplifies it, and feeds it into a digital signal processing (DSP) data path for echo detection. Because the received echo signal can vary amplitude (in millivolts for near objects and in microvolts for far objects), the first AFE stage is a very low-noise balanced amplifier with a predetermined fixed gain followed by a variable gain-stage amplifier with configurable gain from 32 dB to 90 dB. The amplified echo signal is converted into a digital signal by a 12-bit analog-to-digital converter (ADC) and fed to a DSP processing block for further evaluation and time-of-flight measurement.

The PGA460 AFE implements system diagnostics for sensing element (transducer) monitoring during the burst and decay stage of the echo recording process in a way of measuring the maximum achieved voltage at the transducer node and the frequency of oscillation at the transducer node. For more information on these diagnostics, see the *System Diagnostics* section.

Feature Description (continued)

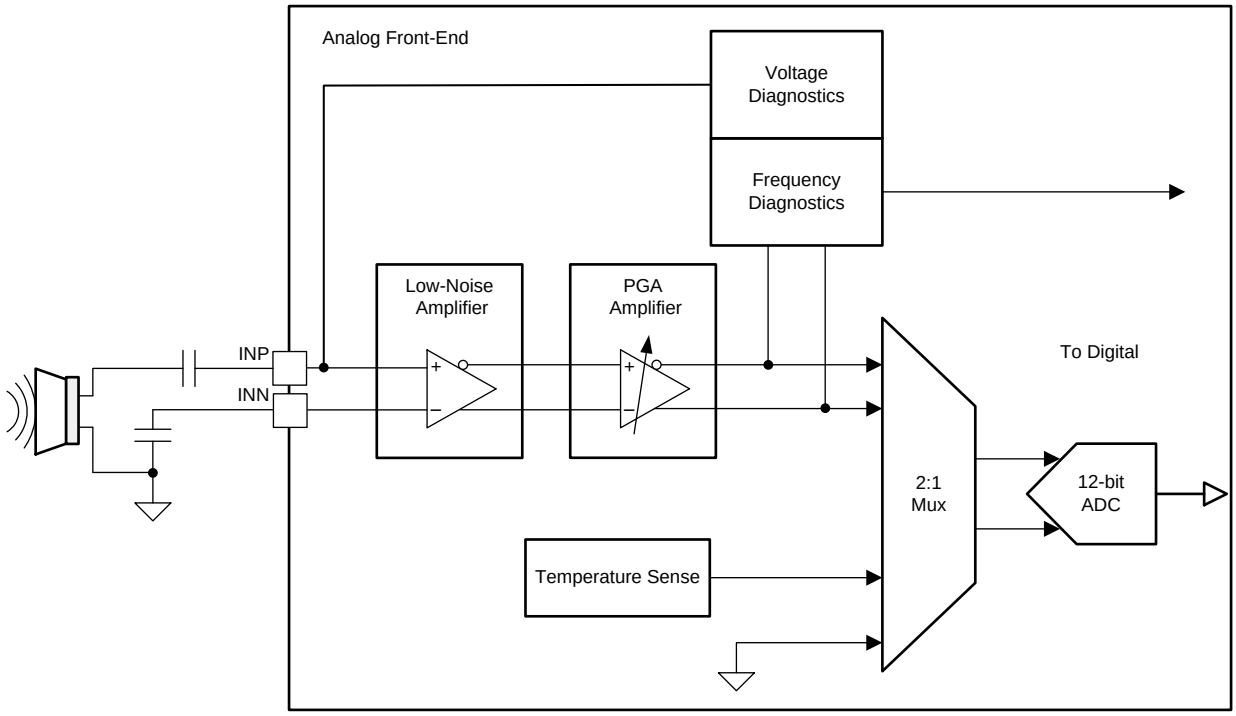


Figure 5. Analog Front-End

The variable gain amplifier in the AFE implements a time-varying gain feature which allows the user to set different static gains and also specify a gain profile for the echo listening process (echo record time). This feature allows for a uniform amplification of echo signals from objects at different distances without saturating the ADC. As an example, for closer objects, gain can be programmed lower initially in time and then increased during the recording time to detect farther objects which have a very small echo signal. This feature helps in attaining sufficient SNR after ADC conversion for all distances for accurate time of flight measurement.

The time-varying gain parameters are stored in the EEPROM memory and characterized by:

- The initial fixed-gain parameter, GAIN_INIT.
- A time-varying gain start-time value stored in the TVGAIN0 register.
- An array of 5 gain-varying cross points placed in the TVGAIN0 to TVGAIN6 registers.

Figure 6 shows an example plot of the time-varying gain.

Feature Description (continued)

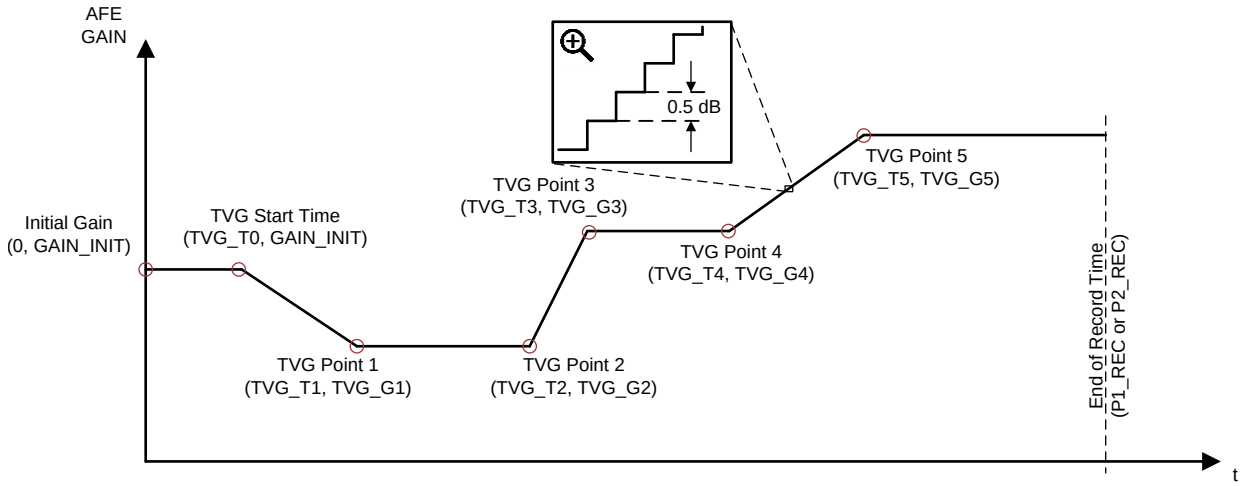


Figure 6. Time-Varying Gain Assignment Example

The time value, TVG start time, is expressed in terms of absolute time, and all following TVG point times (TVG_Tx parameters) are expressed as a delta time between the current and previous point. All gain values are expressed in an absolute gain value in dB and are unrelated from each other. The final gain setting of TVG Point 5 (TVG_G5) will be kept constant until the end of the echo record time. The time-varying gain assignment is the same for both presets. A linear interpolation scheme is used to calculate gain between two TVG points. The AFE gain resolution is 0.5 dB typical.

NOTE

The time-varying gain changes during the recording are applied only on the record cycle that follows. If the TVGAIN[0:6] registers programmed to 0x00, the time-varying gain function of the PGA460 device is disabled and a fixed gain defined by the INIT_GAIN register is applied. In this case, changing the INIT_GAIN register changes the gain of AFE during the recording.

The offset on the time-varying gain is controlled through the two AFE_GAIN_RNG bits in DECPL_TEMP register. For each of the four settings as defined in the *Register Maps* section, the gain can be varied from 0 to 32 dB added on top of the offset.

7.3.4 Digital Signal Processing

The DSP block of the PGA460 device processes the digital data from the ADC to extract the peak profile of the echo after which the output of the DSP is compared against the programmed threshold to measure the time of flight for object distance calculation.

Figure 7 shows the data path of the DSP. Also, the output of the comparator can be deglitched by the THR_CMP_DEGLTCH[7:4] bits in the DEADTIME register.

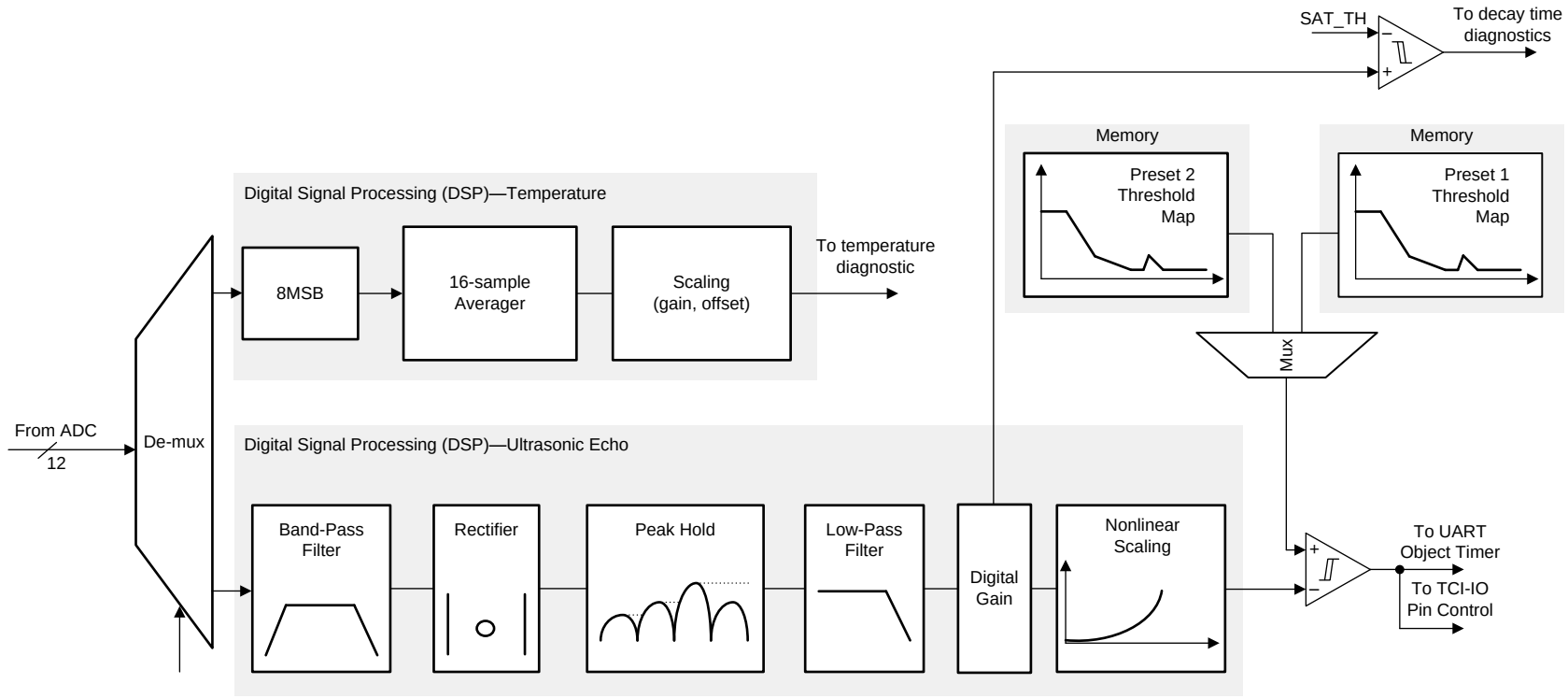


Figure 7. DSP Data-Path

7.3.4.1 Ultrasonic Echo—Band-Pass Filter

The ultrasonic echo signal is an amplitude-modulated signal with an underlying carrier frequency equal to the drive frequency of the ultrasonic transducer. The DSP band-pass filter block allows the frequencies outside of the observed frequency band to be filtered out and therefore reducing the amount of noise influencing the ultrasonic echo signal.

The center frequency of the filter is automatically adjusted based on the driving frequency set by the FREQ bit while the bandwidth of the filter can be adjusted from 2 kHz to 8 kHz in steps of 2 kHz by setting the BPF_BW bit in the INIT_GAIN EEPROM register.

The band-pass filter is a second-order Butterworth IIR type filter. On power up, the PGA460 device calculates the coefficients and places them in the BPF_A2_xSB, BPF_A3_xSB, and BPF_B1_xSB registers. These registers can be overwritten by the user to reconfigure the filter. However, if the FREQ or BPF_BW bit is changed, the coefficient calculation sequence is rerun and the device rewrites these registers. In case the FREQ_SHIFT bit is set to 1 (80- to 480-kHz driving frequency range), the band-pass filter coefficients are not calculated automatically by the PGA460 device. In this case the MCU is required to write these values through the UART or USART interface.

7.3.4.2 Ultrasonic Echo–Rectifier, Peak Hold, Low-Pass Filter, and Data Selection

The rectifier, peak extractor, and low-pass filter DSP blocks demodulate the echo signal while outputting a base-band representation to be compared against the programmed thresholds. These blocks are defined as:

Rectifier This block outputs the absolute value of the input signal since the input signal can be positive and negative in amplitude.

Peak hold This block holds the peak value of the rectified signal for a specific amount of time required for the low-pass filter to detect the peak amplitude of the signal.

Low-pass filter (LPF) This block removes any noise artifacts from the echo signal. The LPF is realized as a first-order IIR type filter. The user can set the cutoff frequency by setting the LPF_CO bit in CURR_LIM_P2 register from 1 kHz to 4 kHz with a step of 1 kHz.

On power up the PGA460 device calculates the values of the filter coefficients and places them in the LPF_A2_xSB and LPF_B1_xSB registers, respectively. The user can overwrite the values in these registers and reconfigure the filter. In this case, the PGA460 device does not take any action. However, if the LPF_CO bit is changed, the coefficient calculation sequence must be rerun and the device repopulates these registers.

7.3.4.3 Ultrasonic Echo—Nonlinear Scaling

The nonlinear scaling block in the DSP data path provides exponential scaling (digital nonlinear amplification) for the echo signal to achieve a higher SNR. This feature is useful for detecting long distance object where the amplitude of the echo signal is very attenuated and close to the noise floor.

The nonlinear scaling block performs the following algorithm:

if $(t < \text{Time\_Offset})$

$$\text{Output} = \text{Input};$$

else

$$\text{Output} = (\text{Input} - \text{Noise\_Level})^{\text{Scale\_Exponent}};$$

where

- t is the current record time.
- Time_Offset is set by the SCALE_N parameter and is used to select one of the time points corresponding to threshold points, TH9, TH10, TH11, or TH12 defined in the *Ultrasonic Echo—Threshold Data Assignment* section.
- Scale_Exponent is the nonlinear exponent (1.5 or 2) and defined by the SCALE_K bit.
- Noise_Level is the user-set noise level between 0 and 31 in 1 LSB step and defined by the NOISE_LVL bit. (3)

The SCALE_N, SCALE_K, and NOISE_LVL bits are EEPROM parameters in the DSP_SCALE register.

NOTE

The nonlinear scaling block can be applied to Preset1 and Preset2.

7.3.4.4 Ultrasonic Echo—Threshold Data Assignment

The PGA460 threshold assignments are organized in two presets: Preset1 and Preset2. Both of these presets have an independent memory map for threshold segment allocation. The PGA460 device supports up to 12 threshold segments for each preset defined by the threshold segment points (TSP) in the P1_THR_[0:15] registers for Preset1 and P2_THR_[0:15]registers for Preset2.

Figure 8 shows an example of a threshold assignment.

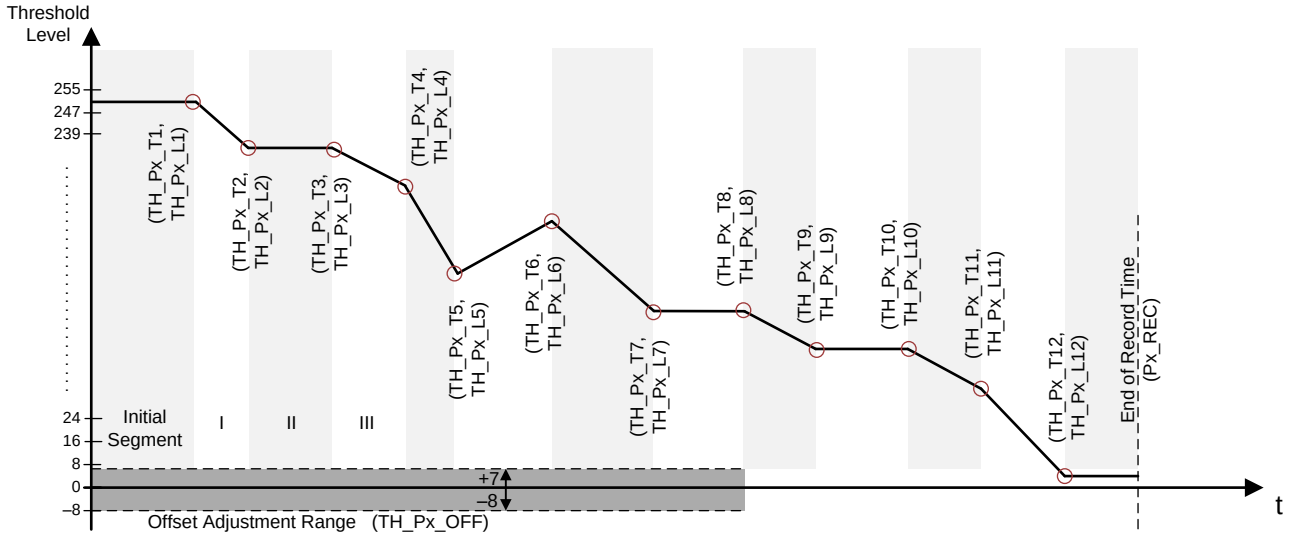


Figure 8. Threshold Assignment Example

As shown in Figure 8, each TSP is described in the (time, level) format while *Px* is the preset number (P1 for Preset1, P2 for Preset2). Additionally, only the initial segment time parameter (TH_Px_T1) value is expressed in terms of absolute time, while all following TSP times (TH_Px_Tx parameters) are expressed as a delta time between the absolute time value of the previous TSP and the absolute time value of the current TSP. The level values of each TSP (TH_Px_Lx parameters) are all expressed in an absolute LSB-level value and are unrelated from each other. The TSP level threshold value at any given time moment is determined by the PGA460 device as a linear interpolation function between the two neighboring threshold segment points

As shown in Figure 8, the initial segment has a constant threshold value determined by the TH_Px_L1 parameter until reaching the start of the first segment and also the 12th segment will have a constant threshold value determined by the TH_Px_L12 parameter until reaching the end of record time defined by the Px_REC parameter.

The TH_Px_L1 through TH_Px_L8 threshold parameters are 5-bits wide and the TH_Px_L9 through TH_Px_L12 parameters are 8-bits wide. These sizes help save memory space and at the same time allow higher resolution for long-range detection of weak echo signals in presence of noise while keeping the range constant across all TSPs. Because the TH_Px_L1 through TH_Px_L8 resolution is an 8 LSB, a threshold offset is defined to allow finer adjustment of the threshold map for short-range detection.

NOTE

- All calculated values of TSP after adding offset, if negative, are clamped to 0 before linear interpolation which causes the slope of threshold curve to deviate from expected value.
- Both Preset1 and Preset2 threshold map parameters are protected by a CRC calculation algorithm (Equation 6).
- At power up or wakeup from low power mode, all threshold registers (Px_THR_XX) and threshold CRC register (THR_CRC) are not initialized to the default value which causes a CRC error and sets THR_CRC_ERR bit to 1. This occurrence indicates to the MCU that the configuration is not loaded properly. Writing to threshold registers reruns CRC calculation and updates the error bit.

7.3.4.5 Digital Gain

A digital gain feature after the low-pass filtering is implemented to improve the SNR of the received echo without lowering the threshold values. Because this gain is applied after the band-pass and low-pass filtering, the digital gain does not amplify the out of band noise. This gain feature can help in suppressing false detection such as ground reflection and detecting farther objects with more accuracy.

Two sets of digital gain ranges are available: short range (SR) and long range (LR). The SR and LR gain levels are set using the Px_DIG_GAIN_SR and Px_DIG_GAIN_LR parameters, respectively, in the Px_GAIN_CTRL register independently for Preset1 and Preset2. The LR gain is applied starting from the threshold level point set by Px_DIG_GAIN_LR_ST parameter to the end of the record period. The SR gain is applied from time zero to the start of the selected LR-threshold level point.

To prevent false detection of an echo at the point in time where the digital gain is applied, the defined thresholds are also changed as shown in the example plot in Figure 9. Here, the LR gain is applied starting from the threshold level point 9. If the LR gain is different than the SR gain at threshold level point 8, the threshold level 8 is multiplied by the ratio between the LR gain and SR gain (DIG_GAIN_LR/DIG_GAIN_SR) 1 µs after the end of the SR threshold level 9 point. Although this creates a discontinuity in the threshold level, the object detection is not affected (a false threshold crossing is prevented) because the echo signal is also scaled by the same gain ratio. After this point, the threshold level is changed to the next set threshold level (point 9 in example below) using a linear interpolation scheme. The threshold levels should be adjusted by taking the digital gain and the ratio between the LR and SR gains into account.

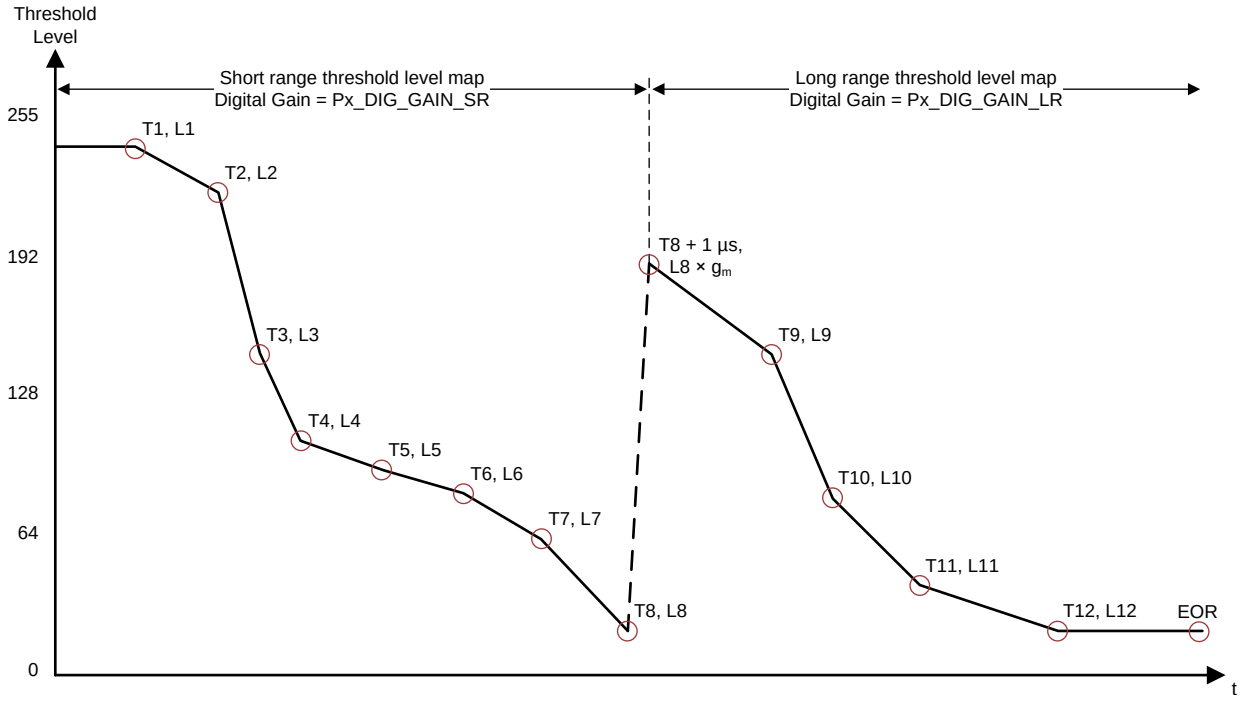


Figure 9. Example of DIG_GAIN_LR_ST = [00] TH9

7.3.5 System Diagnostics

The system diagnostics in the PGA460 device help characterize the transducer element during the burst itself and determine the status of the overall system. By using the provided information the system should be able to detect transducer failure, driver-circuit failure (transformer failure if used), environmental effects on the system (such as ice, dirt, snow), objects compromising the transducer operation (such as pressure applied to the transducer), and others.

Three implemented system diagnostics are available in the PGA460 device that provide information which can be used in detecting system flaws. These diagnostics are described as follows:

Voltage diagnostic measurement The voltage diagnostic feature is obtained by monitoring the current flowing through the INP pin only when a BURST/LISTEN run command is executed. The transducer excitation voltage at the particular burst frequency results in a current at INP pin that is compared to a reference current with a current comparator as shown in Figure 10. If the excitation current exceeds the threshold level set using the FVOLT_ERR_TH in FVOLT_DEC register, the current comparator output goes high which implies a normal burst with the desired level of excitation voltage. The measurement starts approximately 50 µs after the burst stage is started and ends at the end of the burst stage. The result of this diagnostic measurement is reported in the status frames of the IO time-command or the UART interface as described in the *Interface Description* section.

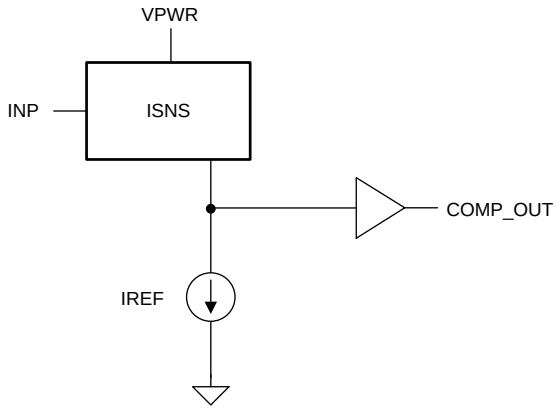


Figure 10. Block Diagram for Voltage Diagnostic

$$V_{(diag)} \cong 3.25E^{-03} \times FVOLT\_ERR\_TH[2:0] \times \left(R_{(INP)} + \frac{1}{6.28 \times f_{(burst)} \times C_{(INP)}} \right) \quad (4)$$

where

- FVOLT_ERR_TH[2:0] corresponds to 1 for 000b to 8 for 111b.
- f_{burst} is the burst frequency in kilohertz.
- C_{INP} is the input capacitance on the INP pin.
- $R_{INP}$is an optional resistor (See Figure 136) used for EMI and ESD robustness.

NOTE

Prior to bursting, the comparator output is expected to be low. In the event that the output is stuck high, the condition is detected and the diagnostic fail flag is set

Transducer frequency measurement During the decay stage of the record interval a frequency measurement on the transducer node is performed to validate the performance and proper tuning of the transformer and transducer matching.

To measure the transducer frequency, a start parameter, FDIAG_START, and a window length parameter, FDIAG_LEN, are defined in EEPROM memory. The start parameter, FDIAG_START, defines the time when the frequency measurement starts relative to the end of the burst time. The diagnostic window length parameter, FDIAG_LEN, sets the time width of the diagnostic window in terms of signal periods captured. A brief example of parameter configuration can be explained:

1. Assume FDIAG_START = 2 and FDIAG_LEN = 1. Referring to the *Register Maps* section, the start time of these EEPROM parameters is determined to be 200 µs after the burst is completed and window length of 3 signal periods. Assuming an operating frequency of 58 kHz, the signal period is 17.24 µs and therefore the diagnostic ends at 200 µs + 3 × 17.24 µs = 251.72 µs after the burst is complete.
2. The frequency information captured in the measurement window is averaged and expressed as a 500-ns time based counter value. The signal frequency can be calculated using Equation 5.

   f = 1 / (FDIAG_VAL × 500e–09)

   where

   - FDIAG_VAL is a value that can be extracted using any of the device interfaces. (5)
3. If the specified number of objects are detected before a frequency diagnostic measurement completes, no frequency measurement results are saved. This can be managed by setting the previously defined diagnostic parameters and threshold settings for near-object detection.

An additional frequency error feature is implemented in the PGA460 device to signify that the

measured transducer frequency is outside of the limits set by the FDIAG_ERR_TH threshold parameter. The result of this feature is reported in the status frames of the IO time-command or the UART interface. For more information on reporting the transducer frequency error, see the *Interface Description* section.

Decay-period time capture During the decay stage of the record interval a transducer decay time measurement is performed to verify correct operation of the transducer. This diagnostic in combination with the transducer frequency measurement are commonly used in ultrasonic systems to detect external blockage of the ultrasonic transducer.

The decay period time is measured at the output of the digital data path. The measurement starts at the same time when the burst stage is completed and the decay period is measured as long as the echo level is higher than a saturation threshold level defined in the EEPROM by the SAT_TH parameter. The provided result can be extracted by using any of the PGA460 interfaces, while the value is expressed in 16-µs time increments. If the decay time measured greater than 4 ms, the value extracted will read 0xFF.

Noise level measurement An additional system diagnostic implemented in the PGA460 device is the noise-level measurement diagnostic. The purpose of this function is to evaluate the surrounding noise generated by other ultrasonic systems nearby to determine disturbances and also evaluate the noise floor level when far distance objects are being detected.

During the noise-level measurement, the PGA460 device executes the LISTEN ONLY (Preset2) command (see the *Interface Description* section for details of the command) where no burst is performed but only a record interval is started and lasts 8.192 ms. During this record interval, the data collected at the output of the digital data path is averaged into two groups each containing 4096 samples. The final noise level is measured by performing the noise-level measurement function is the higher averaged value of the two groups. This value is reported as the final noise-level measurement.

NOTE

The nonlinear scaling block is always disabled (scale factor EEPROM by setting the SCALE_K bit 0 and the NOISE_LVL bit to 0) during the noise-level measurement process.

Figure 11 shows the system diagnostics implemented in the PGA460 device as a full object-detection record cycle example. The numbers 1, 2, and 3 in Figure 11 show voltage diagnostic, transducer frequency, and decay-period measurement, respectively.

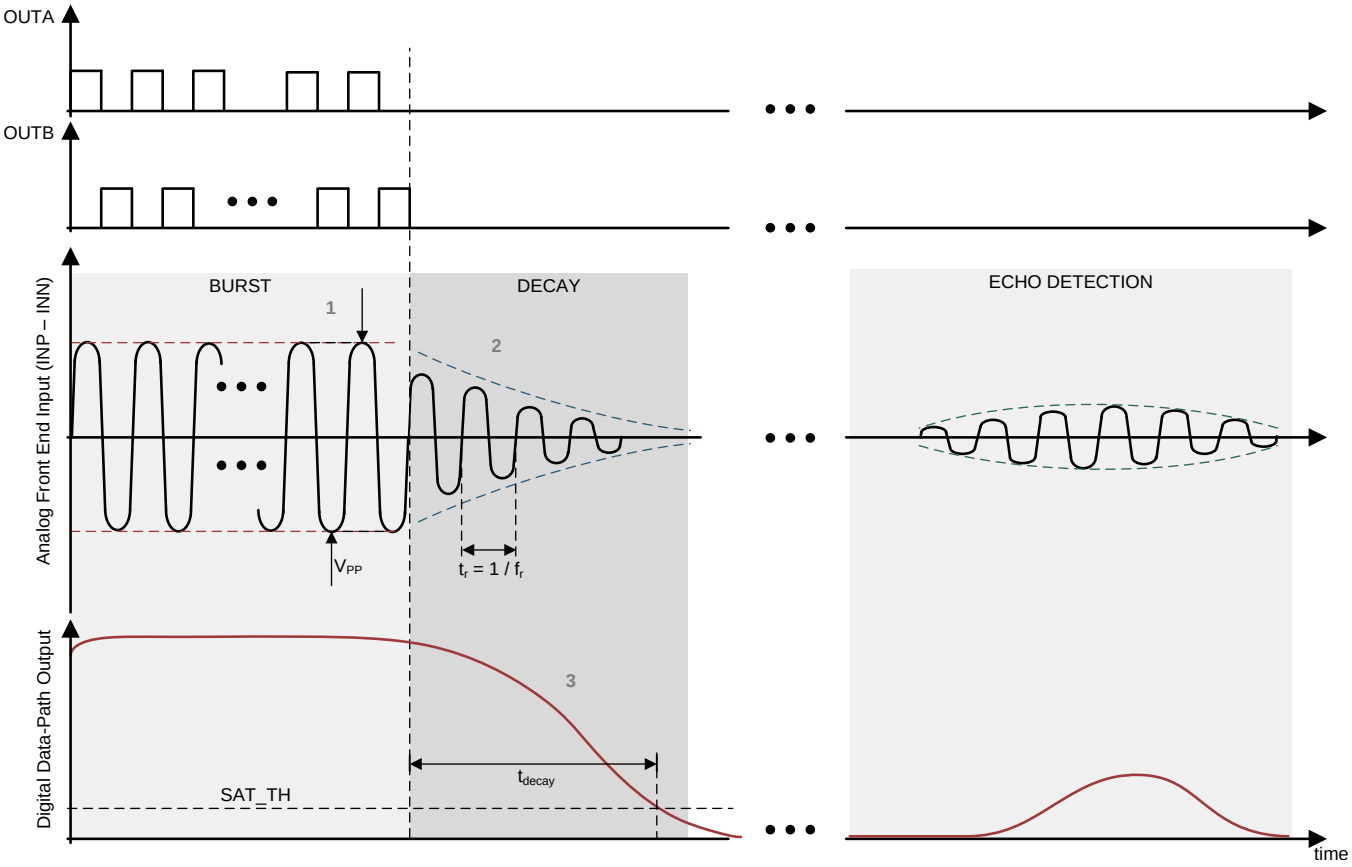


Figure 11. Systems Diagnostics Example

7.3.5.1 Device Internal Diagnostics

The PGA460 device also offers Internal diagnostics against overvoltage (OV), undervoltage (UV), overcurrent (OC), and thermal shutdown.

The OV, UV, and thermal shutdown conditions are reported through the status bits in the DEV_STAT1 register. The OC protection is implemented on the device integrated regulators; however, the effect of this protection is not reported. For proper operation and to avoid false triggering, all electrical diagnostics are passed through a 25-µs deglitch while the thermal shutdown diagnostic is passed through a 50-µs deglitch before being reported.

The OV and UV protection thresholds for the internal regulators are listed in the *Specifications* section. When a fault is detected, the corresponding status bit is set and it is cleared upon interface read (clear-on-read type).The input device supply on the VPWR pin defines a fixed UV-threshold level and adjustable OV-threshold level (VPWR_OV_TH) that keeps the device active while disabling the output driver. This feature allows control of power dissipation at high voltage inputs without damaging the driver. When a VPWR_UV flag is detected, any presently running TCI command finish and no new TCI commands are executed until the undervoltage condition is removed. This feature is not applicable to USART communication irrespective of the pins (RXD, TXD, or IO)

The thermal shutdown protection diagnostic monitors the temperature of the FETs of the low-side driver. In case of a thermal shutdown event, the PGA460 device disables the output drivers and re-enables them when the thermal shutdown condition is removed. After thermal shutdown recovery, the thermal shutdown status bit is set to notify the user of the action taken.

NOTE

If the voltage on the VPWR pin is less than 5 V, the performance of the device is not ensured as the digital core might reset. Any settings stored in the volatile memory section of the register map will be cleared.

7.3.6 Interface Description

The PGA460 device is equipped with two communication interfaces, each with a designated pin. The time-command interface is connected to the IO pin which is an open-drain output structure with an internal 10-kΩ pullup resistor capable of communicating at battery level voltage. The asynchronous UART interface can communicate on the IO pin and is also connected to the RXD and TXD pins. A third Interface option is to use the synchronous USART interface which is available only at the RXD and TXD pins. This communication uses SCLK pin for a serial clock input and is the fastest data-rate mode. USART communication on RXD and TXD pins is available at a 3.3-V or 5-V CMOS level depending on the configured IOREG voltage as described in the *TEST Pin Functionality* section.

NOTE

Because the system is unlikely to simultaneously use both the time-command interface and the UART interface, the PGA460 device can disable the IO pin transceiver to preserve power. To do so, the IO_IF_SEL bit must be 0, and the IO_DIS bit must be 1 which immediately disables the IO pin transceiver upon which communication is only possible through the RXD and TXD pins. Setting the IO_DIS bit back to 0 does not re-enable the IO interface. If the IO_DIS bit was set unintentionally, the device can recover the IO interface (reset the IO_DIS bit to 0) upon power-cycle; however, when the value of this bit is programmed in the EEPROM, the PGA460 device always follows the EEPROM-programmed value on power up.

7.3.6.1 Time-Command Interface

The time-command interface is the communication interface connected on the IO pin. The default state for the IO pin when the interface is idle is HIGH (pulled up to VPWR). The pin communication is bi-directional, where upon receiving a command, the PGA460 device is actively driving the IO pin and providing a response by changing the state of the IO pin. If the time-command interface remains stuck while transmitting a command or data for a particular command that is either LOW or HIGH for more than 15 ms, then the PGA460 communication resets and is expected to receive a new command transmission from the master device.

The time-command interface is specified by five time commands, where four are classified as run commands and one CONFIGURATION/STATUS command. Logic 0 is transmitted by pulling the IO pin low for a time duration of t_{BIT0_TCI} and logic 1 is transmitted by pulling the IO pin low for time duration of t_{BIT1_TCI} as defined in the *Specifications* section. Figure 12 and Figure 13 receptively show the general timing diagram for device time commands and for logic bit timing. The $t_{(DT\_TCI)}$ dead-time is defined for the PGA460 device to process the received command and change the IO pin state from input to output.

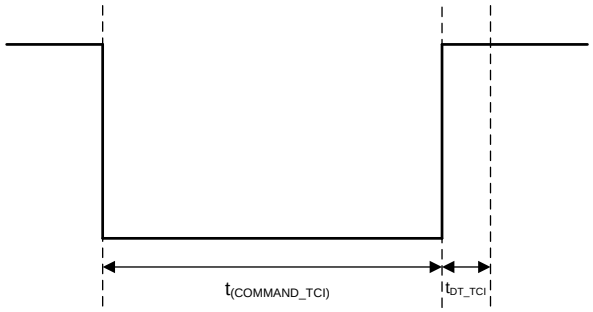


Figure 12. Time-Command Interface Command Timing

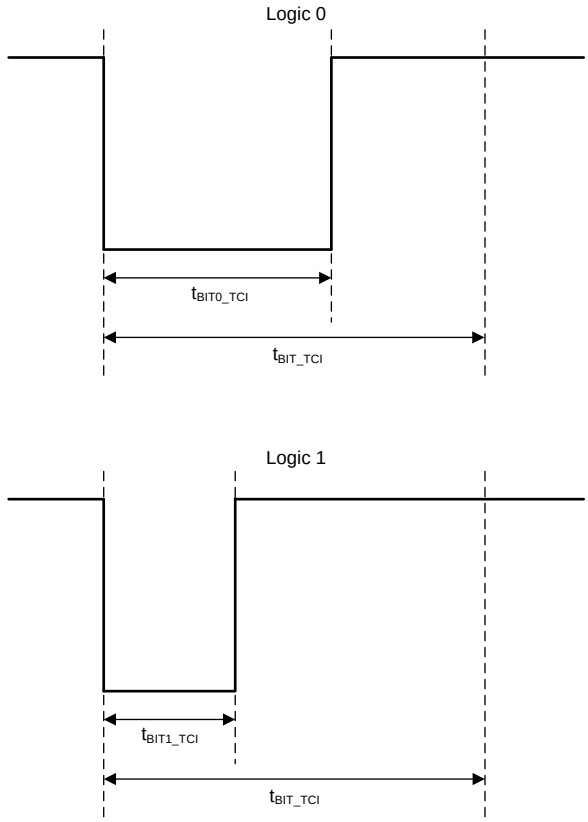


Figure 13. Time-Command Interface Bit Timing

7.3.6.1.1 RUN Commands

The run commands are used for device run-time operation and are most commonly used during the normal operation cycle of the PGA460 device. These device commands are specified by pulling the IO pull low for a specified period of time as defined in the *Specifications* section. The following are classified as run commands:

Burst/Listen (Preset1) The device sends an ultrasonic burst using the P1_PULSE number of pulses while using the CURR_LIM1 current-limit setting and runs an object-detection record interval defined by the value of the P1_REC time length. During the process of object detection, the P1_THR_xx threshold map is used for signal comparison. The nonlinear scaling DSP function is available for use with this command.

Burst/Listen (Preset2) The device sends an ultrasonic burst using the P2_PULSE number of pulses while using the CURR_LIM2 current-limit setting and runs an object-detection record interval defined by the value of the P2_REC time length. During the process of object detection, the P2_THR_xx threshold map is used for signal comparison. The nonlinear scaling DSP function is available for use with this command.

Listen Only (Preset1) The device does not send an ultrasonic burst, however, and only runs an object-detection record interval defined by the value of the P1_REC time length. During the process of object detection, the P1_THR_xx threshold map is used for signal comparison. The nonlinear scaling DSP function is available for use with this command.

Listen Only (Preset2) The device does not send an ultrasonic burst, however, but only runs an object-detection record interval defined by the value of the P2_REC time length. During the process of object detection, the P2_THR_xx threshold map is used for signal comparison. The nonlinear scaling DSP function is available for use with this command.

Figure 14 shows the process of the communication of the IO pin run command.

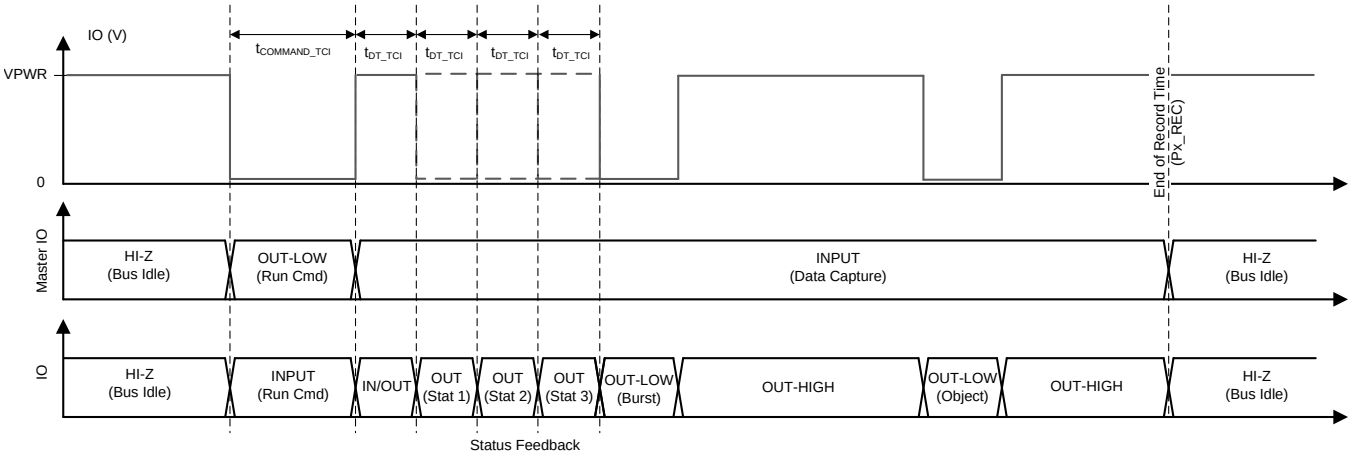


Figure 14. Time-Command Interface RUN Command Execution

The status field of the PGA460 device is embedded in the run command and provided back to the master controller by extending the dead-time on the IO bus. The dead-time can be further extended for up to 3 × $t_{(DT\_TCI)}$ which signifies three status bits, STAT[1:3]. Each status bit has an assigned diagnostic and a priority as listed in Table 1.

Table 1. Time-Command Interface Status Bits Description

STATUS BIT	PRIORITY	DESCRIPTION
STAT 1	1, low	Threshold settings uninitialized error
STAT 2	2	Frequency diagnostics error
		Voltage diagnostic error
STAT 3	3, high	Power-up auto EEPROM CRC error
		User triggered EEPROM download CRC error

As listed in Table 1, the STAT3 bit has the highest priority. When a STAT3 error condition is present, then the dead-time is further extended by 3 × $t_{(DT\_TCI)}$. In this case, if any STAT2 or STAT1 error conditions are also present, these conditions are overruled by the higher priority of STAT3 error conditions. In a similar way, a STAT1 condition is overruled by a STAT2 error condition in which case the dead-time is further extended by 2 × $t_{(DT\_TCI)}$. When all STAT3 and STAT2 error conditions have cleared, a STAT1 condition further extends the dead-time by an additional $t_{(DT\_TCI)}$.

The functions of the status bits can be explained as follows:

STAT 1 This status bit is set to 1 when both preset threshold register groups are uninitialized. Any run command received over the TCI communications channel is not executed until either preset threshold register group is programmed.

STAT 2 This status bit is set to 1 when any of the following occurs:

- If the measured frequency value as described in the *System Diagnostics* section for frequency diagnostics is higher or lower than the delta value defined by the FDIAG_ERR_TH parameter in the EEPROM memory (this is consider to be a frequency diagnostic error).
- If the measured voltage value as described in the *System Diagnostics* section for transducer voltage measurement is lower than the level provided by the FVOLT_ERR_TH parameter in EEPROM memory.

STAT 3 Any run command received over the TCI communications channel is not executed until the EE CRC error is fixed.

The user can write to any EEPROM-mapped register to clear the error.

The user must reprogram the EEPROM to prevent the error upon another automatically or manually triggered EEPROM download operation.

When the device receives a run command, the IO pin is actively driven by the PGA460 device depending on the final DSP output to indicate object detection. If, at any time, the processed echo signal exceeds the threshold at that time, the IO pin is pulled low (GND, strong pulldown) otherwise the IO pin is pulled up by the internal 10-kΩ (weak pullup) resistor. When the record time reaches the end of the record defined by the Px_REC parameters, the IO pin is released (pulled up as an input) and the device is ready for a next command. Figure 15 shows the object detection functionality of the IO pin. The device pulls the IO pin low during the burst and then releases it to provide a reference for the recording time-frame for the MCU. Knowing the time of reference, the duration of the programmed burst and following falling edges for each object detected, the master controller or MCU can calculate the object distance.

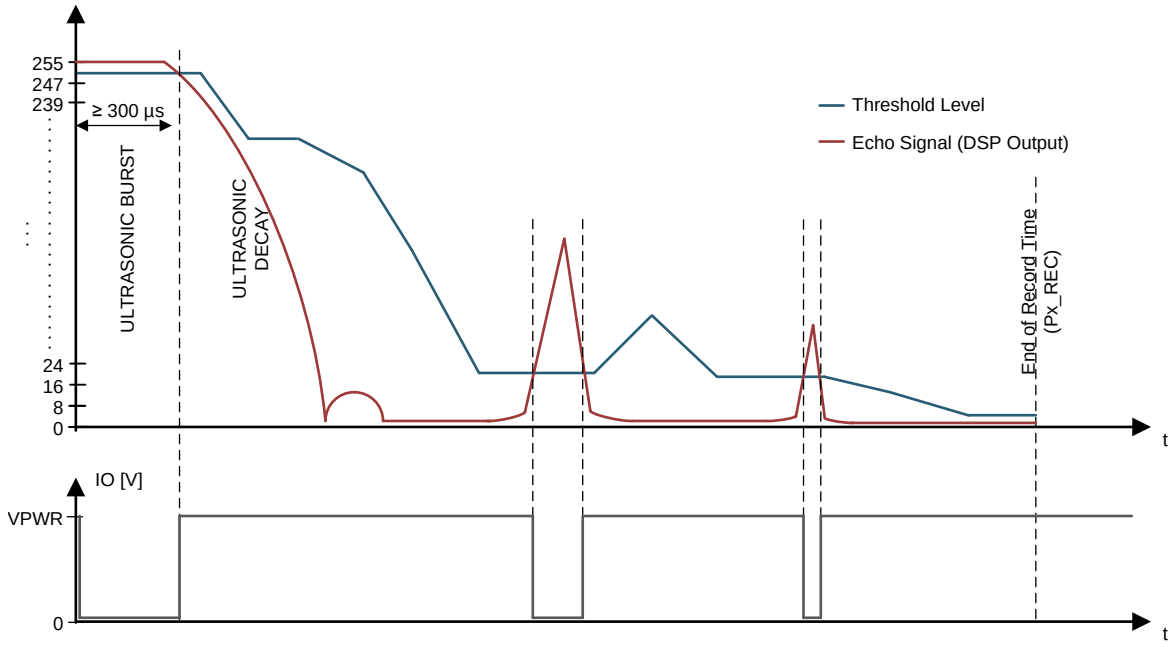


Figure 15. IO-Pin Object-Detection Signaling With Burst/Listen Time Command

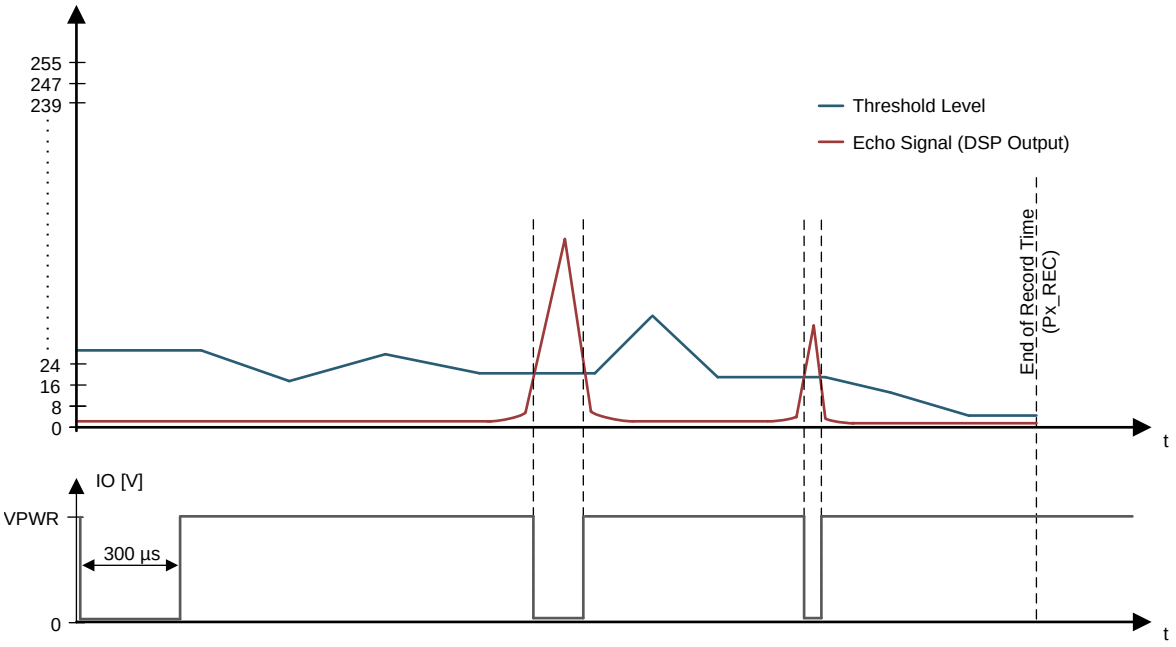


Figure 16. IO-Pin Object-Detection Signaling With Listen-Only Time Command

The PGA460 device forces IO pin to go low after the $t_{(DT\_TCI)}$ time passes after receiving a run command for a minimum of 300 µs which indicates start of the record period. This process occurs to provide the master controller a reference edge to start the time of flight measurement and also for PGA460 device to separate the response of the status (STAT) bits from the record cycle information. In general, the duration of burst for lower frequency range followed by ringing causes the AFE to saturate and pull the IO pin low for more than 300 µs. For higher frequency burst or for listen-only command, or in situations where the saturation caused by the ultrasonic burst might not be a higher value than the assigned threshold, as shown in Figure 16, the minimum pulse width is 300 µs. With a certain filter and deglitch setting, a fake object can be detected directly after this 300-µs period.

7.3.6.1.2 CONFIGURATION/STATUS Command

The CONFIGURATION/STATUS command is used for the following:

- PGA460 internal parameter configuration
- Time-varying gain and threshold setup
- EEPROM programing
- Diagnostics and temperature measurements
- Echo data-dump function

When the CONFIGURATION/STATUS command is issued, the remaining data is transferred by using bit-like communication where a logical 1 and logical 0 are encoded as shown in Figure 13. Figure 17 and Figure 18 show a full-length CONFIGURATION/STATUS command.

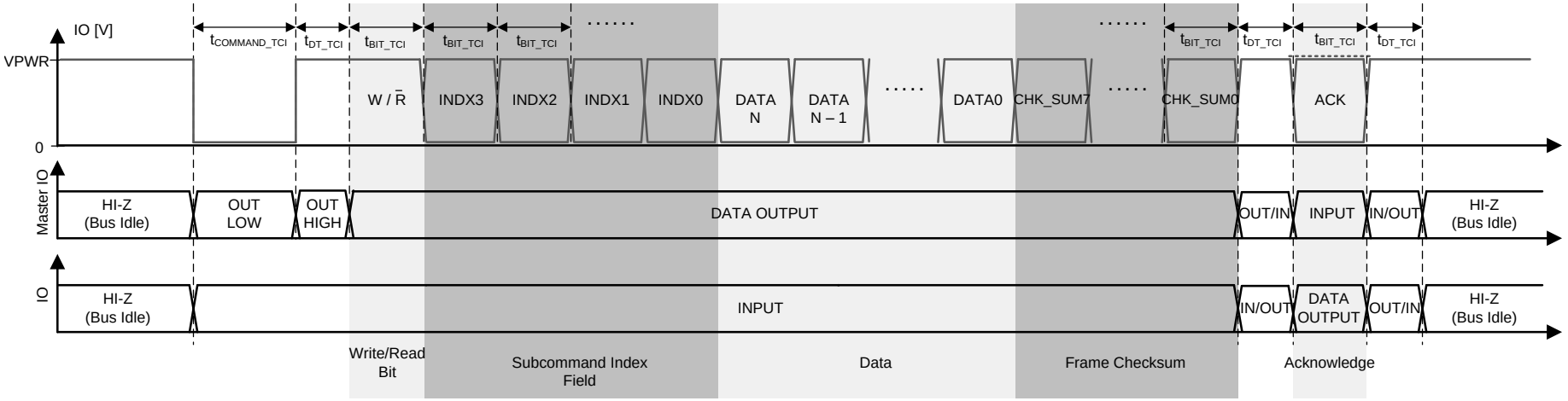


Figure 17. Time-Command Interface CONFIGURATION/STATUS Command—Write

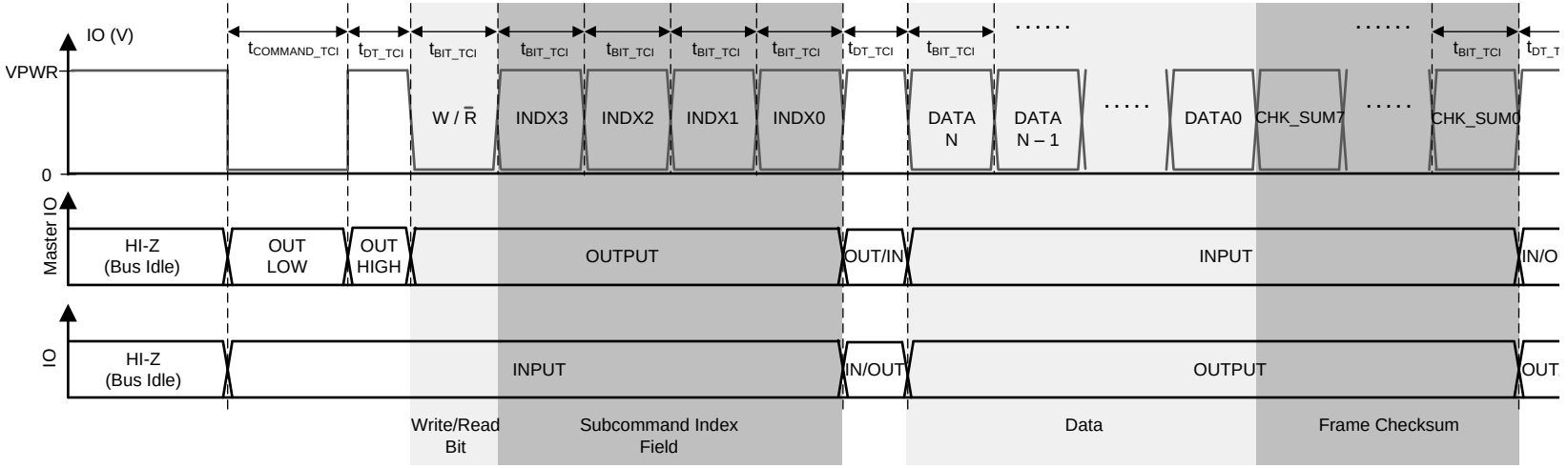


Figure 18. Time-Command Interface CONFIGURATION/STATUS Command—Read

As indicated, each CONFIGURATION/STATUS command frame consists of three data segments: subcommand field, data field, and frame checksum. The subcommands are defined and ordered by a 4-bit index field, where each subcommand can have a different data length in the data segment of the frame. Table 2 lists all PGA460 subcommands ordered according to their respective index.

Table 2. Time-Command Interface Subcommand Description(1)

INDEX	DESCRIPTION	DATA LENGTH (BITS)		ACCESS	EE
0	Temperature value	8		R	N
1	Transducer frequency diagnostic value	8	24	R	N
	Decay period time diagnostic value	8			
	Noise level diagnostic value	8			
2	Driver frequency (FREQ)	8		R/W	Y
3	Number of burst pulses for Preset1 (P1_PULSE)	5	18	R/W	Y
	Number of burst pulses for Preset2 (P2_PULSE)	5			
	Threshold comparator Deglitch (THR_CMP_DEG)	4			
	Burst pulses dead-time (PULSE_DT)	4			
4	Record time length for Preset1 (P1_REC)	4	8	R/W	Y
	Record time length for Preset2 (P2_REC)	4			
5	Threshold assignment for Preset1 (P1_THR_0 to P1_THR_15)(2)	124		R/W	N
6	Threshold assignment for Preset2 (P2_THR_0 to P2_THR_15)(2)	124		R/W	N
7	Band-pass filter bandwidth (BPF_BW)	2	42	R/W	Y
	Initial AFE gain (GAIN_INIT)	6			
	Low-pass filter cutoff frequency (LPF_CO)	2			
	Noninear scaling noise level (NOISE_LVL)	5			
	Nonlinear scaling exponent (SCALE_K)	1			
	Nonlinear scaling time offset (SCALE_N)	2			
	Temperature-scale gain (TEMP_GAIN)	4			
	Temperature-scale offset (TEMP_OFF)	4			
	P1 digital gain start threshold (P1_DIG_GAIN_LR_ST)	2			
	P1 digital long-range gain (P1_DIG_GAIN_LR)	3			
	P1 digital short-range gain (P1_DIG_GAIN_SR)	3			
	P2 digital gain start threshold (P2_DIG_GAIN_LR_ST)	2			
	P2 digital long-range gain (P2_DIG_GAIN_LR)	3			
	P2 digital short-range gain (P2_DIG_GAIN_SR)	3			
8	Time-varying gain Assignment (TV_GAIN0 to TV_GAIN6)	56		R/W	Y
9	User-data memory (USER_1 to USER_20)	160		R/W	Y

(1) The acronyms used in this table (for example, CURR_LIM1) are the same as those used in the *Register Maps* section.
(2) Including the threshold level offset parameter (TH_Px_OFF).

Table 2. Time-Command Interface Subcommand Description(1) (continued)

INDEX	DESCRIPTION	DATA LENGTH (BITS)		ACCESS	EE
10	Frequency diagnostic window length (FDIAG_LEN)	4	46	R/W	Y
	Frequency diagnostic start time (FDIAG_START)	4			
	Frequency diagnostic error time threshold (FDIAG_ERR_TH)	3			
	Saturation diagnostic level (SAT_TH)	4			
	P1 nonlinear scaling (P1_NLS_EN)	1			
	P2 nonlinear scaling (P2_NLS_EN)	1			
	Supply overvoltage shutdown threshold (VPWR_OV_TH)	2			
	Sleep mode timer (LPM_TMR)	2			
	Voltage diagnostic threshold (FVOLT_ERR_TH)	3			
	AFE gain range (AFE_GAIN_RNG)	2			
	Low-power mode enable (LPM_EN)	1			
	Decouple time and temperature select (DECPL_TEMP_SEL)	1			
	Decouple time and temperature value (DECPL_T)	4			
	Disable current limit (DIS_CL)	1			
	Reserved	1			
	Driver current limit for Preset1 (CURR_LIM1)	6			
	Driver current limit for Preset2 (CURR_LIM2)	6			
11	Echo data-dump enable (DATADUMP_EN)	1	8	R/W	N
	EEPROM programming password (0xD)	4			
	EEPROM programming successful (EE_PRGM_OK)	1			
	Reload EEPROM (EE_RLOAD)	1			
	Program EEPROM (EE_PRGM)	1			
12	Echo data-dump values(3)	1024		R	N
13	EEPROM user-bulk command (0x00 to 0x2B)(4)	352		R/W	Y
14	Reserved				
15	EEPROM CRC value (EE_CRC) THR_CRC value (THR_CC)	16		R	Y

(3) Echo dump memory is an array of 128 samples, 8 bits/sample.
(4) For index 13, byte 0x2B is read-only, when an index-13 write command is sent, the byte-2B data field will have no effect on the EE_CRC value.

The frame checksum value is generated by both the master and slave devices, and is added after the data field, while calculated as the inverted eight bit sum with carry-over on all bits in the frame. The checksum calculation occurs byte-wise starting from the most-significant bit (MSB) which is the read-write (R/W) bit in the PGA460 write operation while for PGA460 read operation, this is the MSB of the data field. In cases where the number of bits on which the checksum field is calculated is not a multiple of eight, then the checksum operation pads trailing zeros until the closest multiple eight is achieved. Zero padding is only required for the checksum calculation. The zero-padded bits should not actually be transmitted over the IO-TCI interface.

The following example, is one example of a frame checksum calculation showing the PGA460 write operation of for subcommand Index 7 (42 data bits):

- Total number of bits for checksum generation: 1 R/W bit, 4 bits index value, 42 bits data values. The total number of bits is 47.
- Because the checksum is calculated byte-wise, 1 trailing zero is added to achieve 6 full bytes.
- Figure 19 shows additional checksum calculation.

The following example, is a second example of a frame checksum calculation showing the PGA460 read operation of for subcommand index 8:

- Total number of bits for checksum generation by the PGA460 device: 56 bits data values + 8 command bits. The total number of bits is 64.
- The 8 command bits are equal to 4-zero bits + Index[3:0] = 8 command bits which is the first byte used in the checksum calculation.

- No trailing zeros added because the number of bits is already 56 or 7 bytes.
- Figure 19 shows additional checksum calculation.

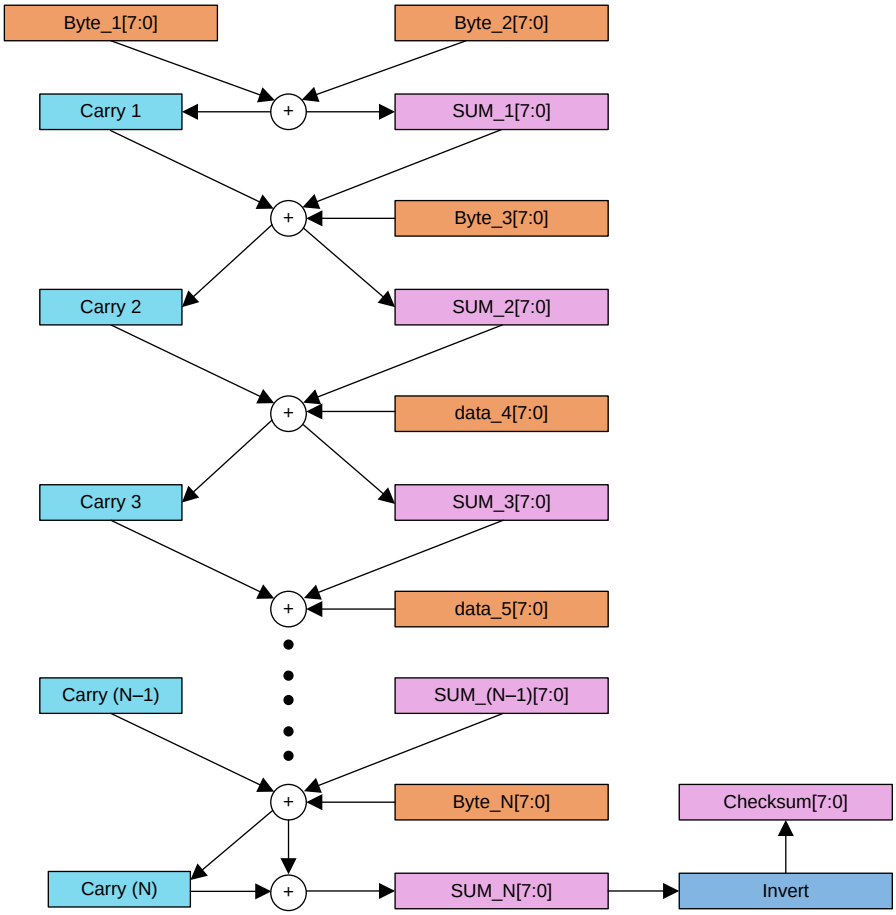


Figure 19. Checksum Calculation

In addition, when a PGA460 write operation is issued, the PGA460 device implements an acknowledgment bit response to signify a correct data transfer occurred. In this case, if the CONFIGURATION/STATUS command time period is not detected properly, the PGA460 device does issue an acknowledgment bit. If the CONFIGURATION/STATUS command-time period is detected properly but the checksum of the transferred frame is not correct, then the PGA460 device transmits a logical 0 acknowledgment. If the CONFIGURATION/STATUS command-time period is detected properly and the checksum value matches the correct checksum, then the PGA460 device transmits a logical 1 acknowledgment.

In the case of a bit-like communication (PGA460 actively serving CONFIGURATION/STATUS command) when the bit stream is interrupted with another time command (either RUN or CONFIGURATION), the PGA460 device decodes this event as a bit-timed event in which case the execution of the initial CONFIGURATION/STATUS command continues until either a time-out error event is reached or, in the case of a continuous data transfer, the PGA460 frame checksum invalidates the incorrectly transferred frame. In the case where the bit-stream is valid but is longer than expected, the PGA460 executes on the correctly transferred frame but ignores the rest of the bit-stream.

If, during PGA460 IDLE state, the time-command interface receives a time command with pulse duration outside the limits of any of the commands, this condition is ignored and the PGA460 device remains in the IDLE state until a valid time command is received. In this case, the PGA460 does not respond with a negative acknowledgment.

7.3.6.2 USART Interface

7.3.6.2.1 USART Asynchronous Mode

The PGA460 device includes a USART digital communication interface. The main function of the USART is to enable writes to and reads from all addresses available for USART access. This function include access to most EEPROM-register and RAM-register memory locations on the PGA460 device. The USART asynchronous-mode (UART) digital communication is a master-slave communication link in which the PGA460 is a slave device only. The master device controls when the data transmission begins and ends. The slave device does not transmit data back to the master device until it is commanded to do so by the master device. A logic 1 value on the UART interface is defined as a recessive value (weak pullup on the RXD pin). A logic 0 value on the UART interface is defined as a dominant value (strong pulldown on the RXD pin).

The UART asynchronous-mode interface in PGA460 is designed for data-rates from 2400-bps to 115200-bps operation, where the data rate is automatically detected based on the sync field produced by the master controller. Other parameters related to the operation of the UART interface include:

- Baud rate from 2400 bps to 115 200 bps, auto-detected (as previously described)
- 8 data bits
- 1 start bit
- 2 stop bit
- No parity bit
- No flow control
- Interfield wait time (required for 1 stop bit)

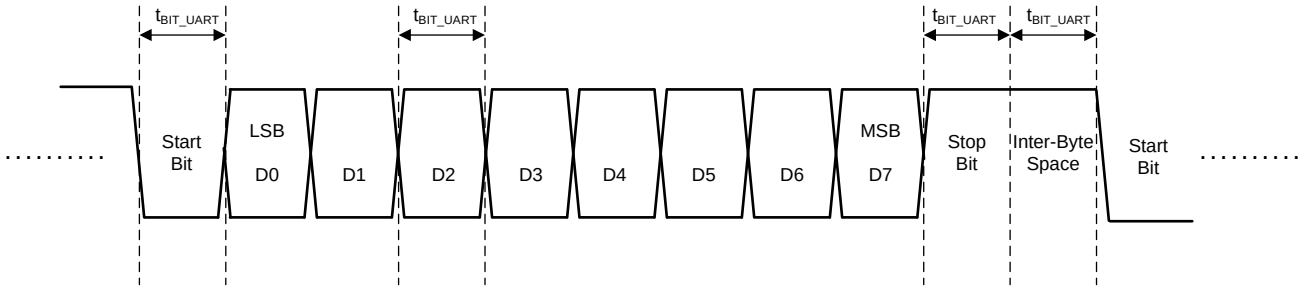


Figure 20. USART Asynchronous Interface Bit Timing

Figure 20 shows the bit timing for USART asynchronous mode. Both data and control are in little endian format. Data is transmitted through the UART interface in byte-sized packets. The first bit of the packet field is the start bit (dominant). The next 8 bits of the field are data bits to be processed by the UART receiver. The final bit in the field is the stop bit (recessive). The combined byte of information, and the start and stop bits make up an UART field. Figure 21 shows the standard field structure for a UART interface field.

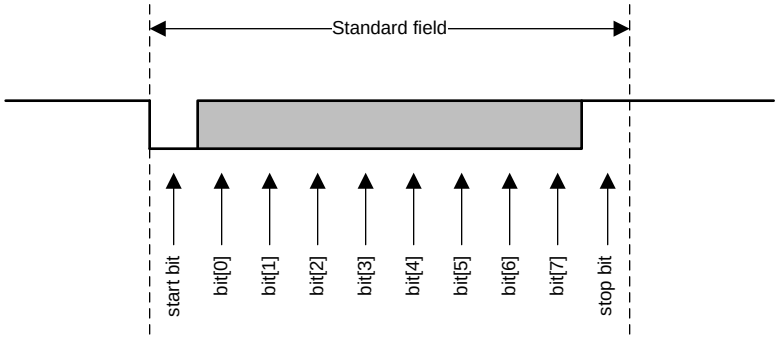


Figure 21. UART Interface Packet Field

A group of fields makes up a transmission frame. A transmission frame is composed of the fields required to complete one transmission operation on the UART interface. Figure 22 shows the structure of a data transmission operation in a transmission frame.

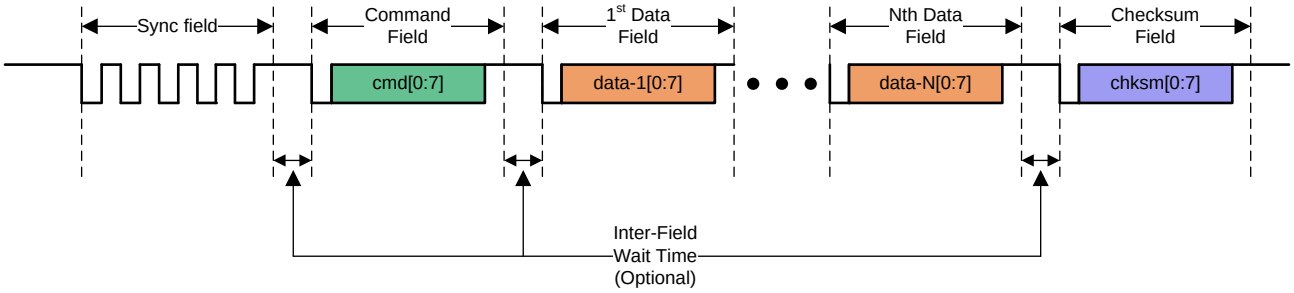


Figure 22. UART Interface Transmission Frame

Each transmission frame must have a synchronization field and command field followed by a number of data fields. The sync field and command fields are always transmitted by the master device. The data fields can be transmitted either by the master or the slave depending on the command given in the command field. The command field determines the direction of travel of the data fields (master-to-slave or slave-to-master). The number of data fields transmitted is also determined by the command in the command field. The interfield wait time is 1-bit long and is required for the slave or the master to process data that has been received, or when data must change direction after the command field is sent and the slave device must transmit data back to the master device. Time must be allowed for the master and slave signal drivers to change direction. If the UART interface remains idle in either the logic 0 or logic 1 state for more than 15 ms, then the PGA460 communication resets and expects to receive a sync field as the next data transmission from the master device.

7.3.6.2.1.1 Sync Field

The sync field is the first field in every frame that is transmitted by the master. The sync field is used by the PGA460 device to confirm the correct baud rate of the frame that is send by the master device. This bit width is used to accurately receive all subsequent fields transmitted by the master. The bit width is defined as the number of internal oscillator clock periods that make up an entire bit of data transmitted by the master. This bit width is measured by counting the number of slave oscillator clocks in the entire length of the sync field data, and then dividing by 8. Figure 23 shows the format of the sync field.

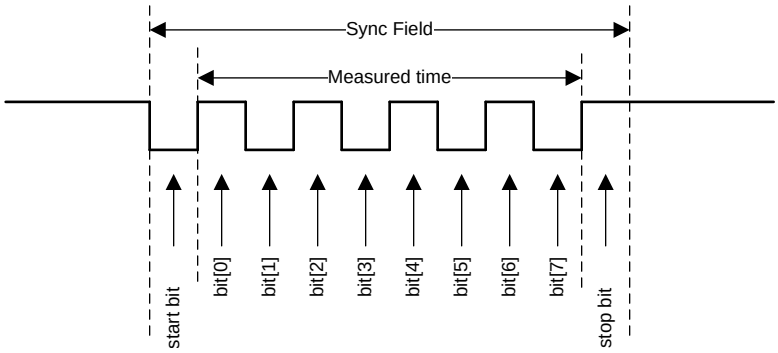


Figure 23. UART Sync Field

Consecutive sync-field bits are measured, including the start and stop bits, and compared to determine if a valid sync field is being transmitted to the PGA460 device is valid. If the difference in bit widths of any two consecutive sync field bits is greater than ±25%, then the PGA460 device ignores the rest of the UART frame; essentially, the PGA460 device does not respond to the UART message.

7.3.6.2.1.2 Command Field

The command field is the second field in every frame sent by the master device. The command field contains instructions about what to do with and where to send the data that is transmitted to a particular PGA460 device. The command field can also instruct the PGA460 device to send data back to the master device during a read operation. The number of data fields to be transmitted is also determined by the command in the command field. Figure 24 shows the format of the command field.

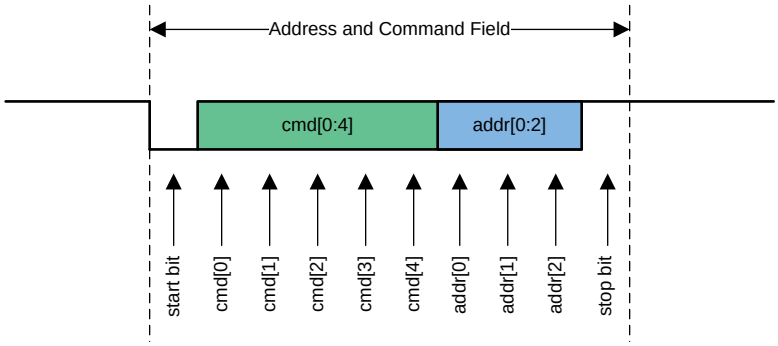


Figure 24. UART Command Field

In the PGA460 device, the last 3-bits of the command field are reserved for UART address information. The address information in the command field is compared to the UART_ADDR parameter in the EEPROM memory where the UART address is programmed. Upon receiving the command field, the PGA460 device checks if the self-address matches the received address and if it matches, the device executes on the received command. If the address does not match, the device disregards the received frame. For improved communication efficiency, common broadcast commands are defined where the PGA460 device executes regardless of the address in the command field. For these commands and all UART commands, see Table 3.

NOTE

The factory preprogrammed address for the PGA460 device is 0.

7.3.6.2.1.3 Data Fields

After the master device has transmitted the command field in the transmission frame, zero or more data fields are transmitted to the PGA460 device (write operation) or to the master (read operation). The data fields can be raw memory data or a command related parameters. The format of the data is determined by the command in the command field. Figure 25 shows the typical format of a data field.

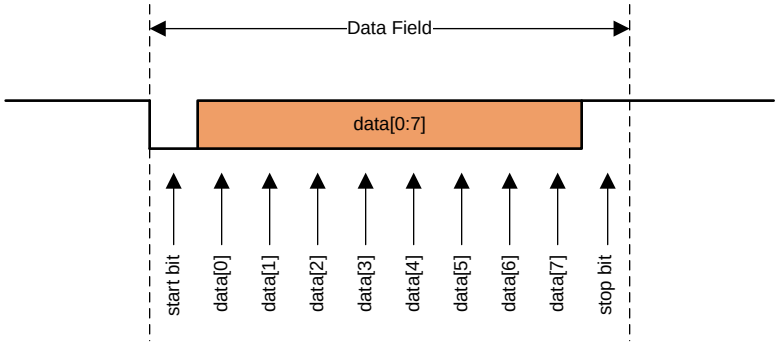


Figure 25. UART Data Field

7.3.6.2.1.4 Checksum Field

A checksum field is transmitted as the last field of every UART frame. The checksum contains the value of the *inverted byte sum with carry* operation over all data fields and the command field (command field for master only). On a master-to-PGA460 transmission, the checksum field is calculated by the master device and checked by the PGA460 device. On a PGA460-to-master transmission, the PGA460 device generates the checksum and the master validates the integrity. The format of the checksum is identical to the data field and the procedure for calculating the checksum is explained in the *Time-Command Interface* section. Because the UART interface is a byte-based interface, no zero padding occurs in the process of calculating the checksum.

When the master device calculates the checksum field, the calculation occurs on the UART command field followed by all UART data fields that are transmitted as a part of the current communication frame. When the PGA460 device is calculating the checksum field, the calculation includes the diagnostic data field (see the *Diagnostic Field* section) followed by all UART data fields in the current frame. The sync field (0x55) is not included as part of the checksum calculation.

7.3.6.2.1.5 PGA460 UART Commands

Table 3 lists the PGA460 UART commands.

NOTE

In the case where any command is improperly received by the PGA460 device, for example a wrong command, wrong number of bytes, or wrong data byte values, then the PGA460 device does not execute on the received command or set the Error_Status[4] bit described in the *Diagnostic Field* section.

Table 3. UART Interface Command List

CMD[4:0]	COMMAND NAME	PGA460 RESPONSE	M-TO-S DATA BYTES	MASTER-TO-SLAVE DATA BYTES DESCRIPTION	S-TO-M DATA BYTES	SLAVE-TO-MASTER DATA BYTES DESCRIPTION
SINGLE ADDRESS						
0	Burst and listen (Preset1)	No	1	Byte1: N - Number of objects to be detected (valid range is from 1 to 8)	0	
1	Burst and listen (Preset2)	No	1		0	
2	Listen only (Preset1)	No	1		0	
3	Listen only (Preset2)	No	1		0	
4	Temperature and noise-level measurement	No	1	Byte1: 0 - Temperature measurement 1 - Noise Measurement 2–255 - Not used	0	
5	Ultrasonic measurement result(1)(2)	Yes	0		4 × N	Byte1–Byte2: Object 1 time-of-flight (µs) (MSB, LSB) Byte3: Object 1 width Byte4: Object 1 peak amplitude . . Byte(3 × N – 3) – Byte(3 × N – 2): Object N time-of-flight (µs) (MSB, LSB) Byte(4 × N – 1): Object N width Byte(4 × N): Object N peak amplitude
6	Temperature and noise level result	Yes	0		2	Byte1: Temperature value Byte2: Noise level value
7	Transducer echo data dump	Yes	0		128	Byte1–Byte128: Echo data dump (array of 128 samples)
8	System diagnostics(3)	Yes	0		2	Byte1: Transducer frequency Byte2: Decay period time
9	Register read	Yes	1	Byte1: Register address	1	Byte1: Register data
10	Register write(4)	No	2	Byte1: Register address Byte2: Register data	0	
11	EEPROM bulk read	Yes	0		43	Byte1: USER_DATA1 data . . Byte43: P2_GAIN_CTRL data

(1) If command 5 is executed while the echo data dump bit is enabled, the read out data will either be invalid or out-of-date. Only the echo data dump memory can be filled, or the threshold comparator be utilized per burst-and-listen or listen-only command.
(2) To convert the object's time-of-flight in microseconds to distance in meters: $\boldsymbol{distance\ (m) = [v_{sound} \times (MSB<<8 + LSB) \div 2 \times 1\mu s]}$. For improved burst-and-listen accuracy, add the additional burst offset to the originally calculated distance: $\boldsymbol{distance_{burst\_offset}\ (m) = [v_{sound} \times (Pulses\ /\ Frequency) \div 2\ ]}$. The speed of sound is typically assumed to be 343m/s at room temperature. Adjust the speed of sound as a function of ambient temperature: $\boldsymbol{v_{sound} = 331m/s + (0.6m/s/°C \times Temperature(°C))}$.
(3) If command 8 is executed before a run command, read out data is invalid.
(4) For commands 10 and 22: Wait 60 µs if INIT_GAIN, TVG, THR or P1_GAIN_CTRL or P2_GAIN_CTRL is written to before a read, otherwise wait 3.3 µs for other functions.

Table 3. UART Interface Command List (continued)

CMD[4:0]	COMMAND NAME	PGA460 RESPONSE	M-TO-S DATA BYTES	MASTER-TO-SLAVE DATA BYTES DESCRIPTION	S-TO-M DATA BYTES	SLAVE-TO-MASTER DATA BYTES DESCRIPTION
12	EEPROM bulk write(5)	No	43	Byte1: USER_DATA1 data . . Byte43: P2_GAIN_CTRL data	0	
13	Time-varying-gain bulk read	Yes	0		7	Byte1–Byte6 : TVGAIN0 - TVGAIN6 data
14	Time-varying-gain bulk write(5)	No	7	Byte1–Byte6: TVGAIN0 - TVGAIN6 data	0	
15	Threshold bulk read	Yes	0		32	Byte1–Byte32: P1_THR_0 - P2_THR_15 data
16	Threshold bulk write(5)	No	32	Byte1–Byte28: 1_THR_0 - 2_THR_15 data	0	
BROADCAST						
17	Burst and listen (Preset1)	No	1	Byte1: N - Number of objects to be detected (valid range is from 1 to 8)	0	
18	Burst and listen (Preset2)	No	1		0	
19	Listen only (Preset1)	No	1		0	
20	Listen only (Preset2)	No	1		0	
21	Temperature and noise-level measurement	No	1	Byte1: 0 - Temperature measurement 1 - Noise measurement 2–255 - Not used	0	
22	Register write(4)	No	2	Byte1: Register address Byte2: Register data	0	
23	EEPROM bulk write(5)	No	43	Byte1: USER_DATA1 data . . Byte43: P2_GAIN_CTRL data	0	
24	Time-varying-gain bulk write(5)	No	7	Byte1–Byte6: TVGAIN0 - TVGAIN6 data	0	
25	Threshold bulk write	No	32	Byte1–Byte32: 1_THR_0 - 2_THR_15	0	
26–31	RESERVED	No				

(5) For commands 12, 14 16, 23, 24, and 25: Wait 50 µs before issuing a read command.

7.3.6.2.1.6 UART Operations

7.3.6.2.1.6.1 No-Response Operation

The no-response operation on the UART interface is fairly straightforward. The command field specifies the address and command for the operation, where the subsequent data bytes, if any, are to be stored in the PGA460 device. The number of data bytes to be sent is predetermined by the UART command. The last field in the frame is the checksum field which is generated by the master. Figure 26 shows an example of memory register write operation (command 10).

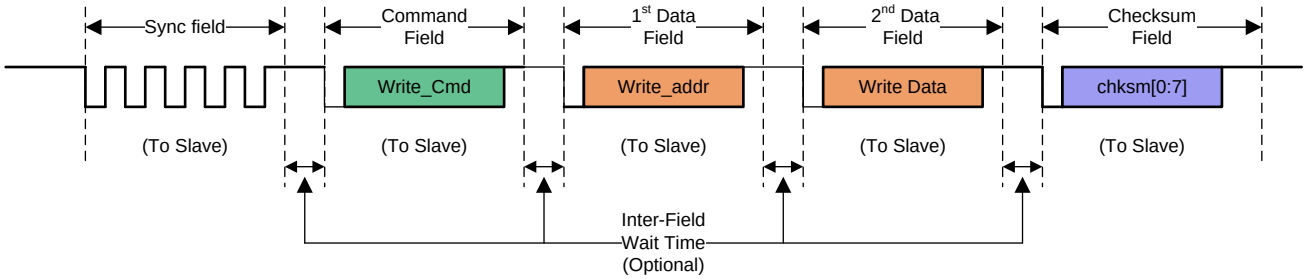


Figure 26. UART No-Response Example

NOTE

If a NO-RESPONSE command arrives on the UART interface while another NO-RESPONSE command is also served or if the PGA460 device is busy performing functions, then the previous command is aborted and the new command is served immediately. This process is particularly important when the PGA460 device is running a record interval because of any of the Command0 through Command4 or Command17 through Command21 being previously received while another command is received on the UART. In this case, the PGA460 device aborts the previous command and terminates the current record interval after which it initiates a new command serving cycle.

7.3.6.2.1.6.2 Response Operation (All Except Register Read)

The response operation of the PGA460 UART interface is initiated with the master sending a response request. After the response request is received by the PGA460 device, the UART responds with the proper data of the command being requested. In a response operation, the master does not generate a checksum Field, rather it is generated by the PGA460.

NOTE

Because the data direction changes (master device to PGA460 followed by PGA460 to master device) and because of the amount of processing time required by the PGA460 device to respond, a response delay time of 1-bit period occurs between the response request and the PGA460 response on the UART.

Figure 27 shows an example of the PGA460 response operation.

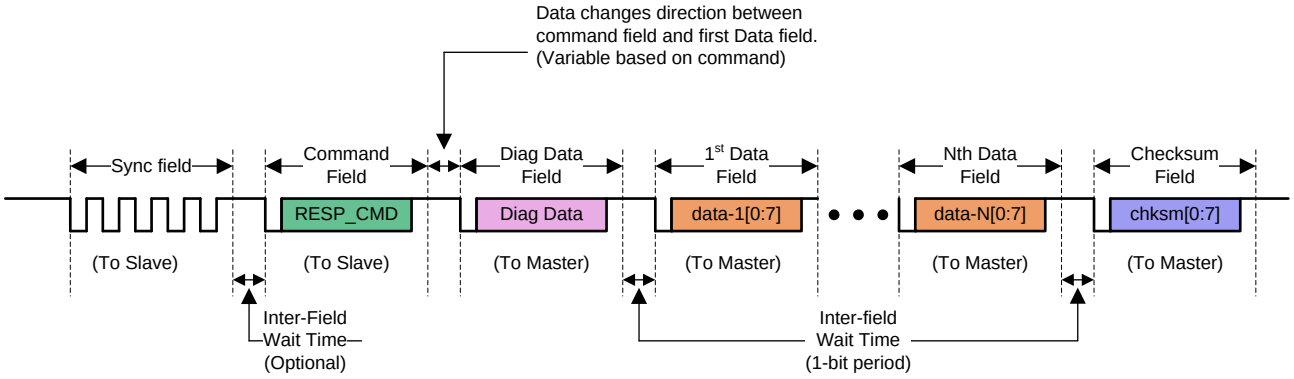


Figure 27. UART Response Example

7.3.6.2.1.6.3 Response Operation (Register Read)

Because the REGISTER READ command requires the master device to specify a register address in the PGA460 memory, an additional frame type is defined where the master issues the sync and command fields followed by the memory register address as the only byte field in the master frame and a master checksum as the last field. Following the master-to-slave transmission, the PGA460 device responds with a standard *PGA460 Response Operation* frame. Figure 28 shows this operation.

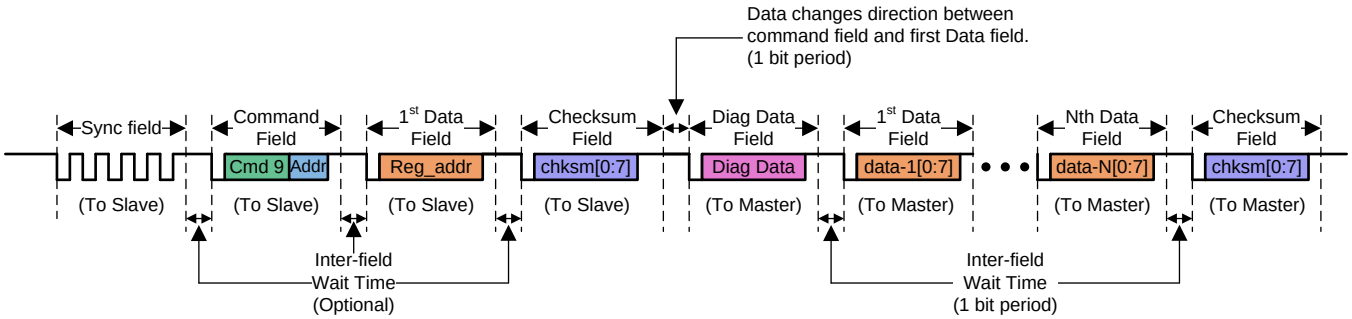


Figure 28. UART Register Read Response Example

NOTE

If a RESPONSE command arrives on the UART interface while another NO-RESPONSE command is also served or if the PGA460 device is busy performing functions, then the PGA460 device responds with a diagnostic field (see the *Diagnostic Field* section) having an error status of 0 which denotes that the device is busy serving functions. If the PGA460 is currently serving a RESPONSE command while another RESPONSE command arrives, then the PGA460 device ignores the new RESPONSE command until it is done serving the previous RESPONSE command.

7.3.6.2.1.7 Diagnostic Field

As described in the *Response Operation (Register Read)* section, the PGA460 device begins the response transmission with a diagnostic data field. This field contains UART communication error bits. If a particular bit is set to 1 then the associated communication error has occurred sometime between the last response operation and the current response operation. After a response operation is performed, the communication error bits are cleared. The diagnostic field is included in the slave generated checksum calculation. Figure 29 shows the diagnostic data field.

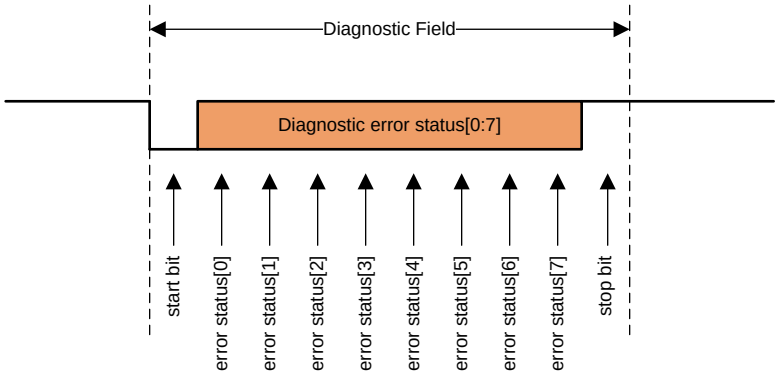


Figure 29. UART Diagnostic Data Field

Table 4 lists the diagnostic data error status bits.

The error status[7:6] bits in the diagnostic field are set to 01b so that the bit time transmitted by the slave can be easily measured. If more error status is required, these bit locations can be used to transmit the additional error status.

Table 4. UART Diagnostic Data Description

BIT	UART_DIAG = 0	UART_DIAG = 1
Error status [0]	PGA460 Device Busy	
Error status [1]	Sync field bit rate too high (>115200 bps) Sync field bit rate too low (>115200 bps)	Threshold settings CRC error
Error status [2]	Consecutive sync field bit widths do not match	Frequency diagnostics error
Error status [3]	Invalid checksum received from master (essentially a calculated slave checksum does not match the checksum transmitted by the master)	Voltage diagnostics error
Error status [4]	Invalid command sent from master	Logic 0
Error status [5]	General communication error: • SYNC filed stop bit too short • Command filed incorrect stop bit (dominant when should be recessive) • Command filed stop bit too short • Data field incorrect stop bit (dominant when should be recessive) • Data field stop bit too short • Data field PGA460 transmit value overdriven to dominant value during stop bit transmission • Data contention during PGA460 UART transmit	EEPROM CRC error or TRM CRC error
Error status [6]	Logic 1	
Error status [7]	Logic 0	

7.3.6.2.1.8 USART Synchronous Mode

For fast (8 Mbps) communication between the master MCU and the PGA460 device, a fast USART synchronous mode is implemented. This mode uses and is only available on the RXD and TXD pins and is also using the SCLK pin as a clock input for communication to the device. In this mode the USART interface acts as a serial-shift register with data set on the rising edge of the clock and sampled on the falling edge of the clock. Differently than the USART asynchronous mode, the synchronous mode communication frame does not include a start,

stop, nor interfield wait bit which means that as soon as the data in one frame has completed, the next communication data frame follows immediately. USART Synchronous Mode is identical to a Serial Peripheral Interface (SPI) without a chip-select because the addressing is handled by the three-bit UART_ADDR value to enable up to eight devices on a single bus. Figure 30 shows the bit timing in synchronous mode and Figure 31 shows the data flow for USART synchronous mode.

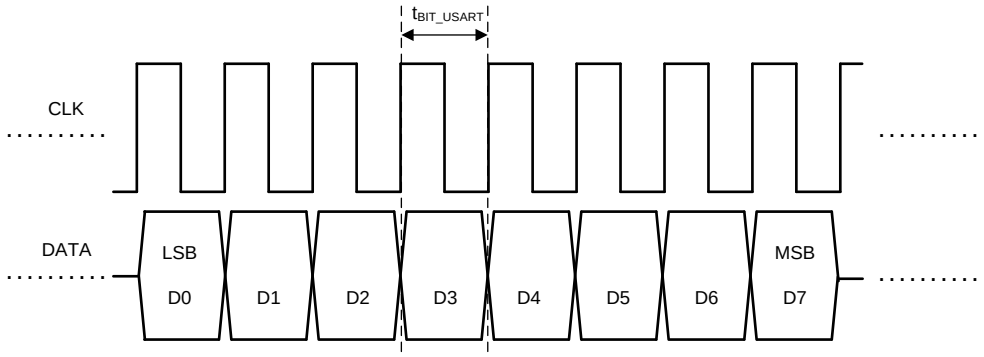


Figure 30. USART Synchronous Interface Bit Timing

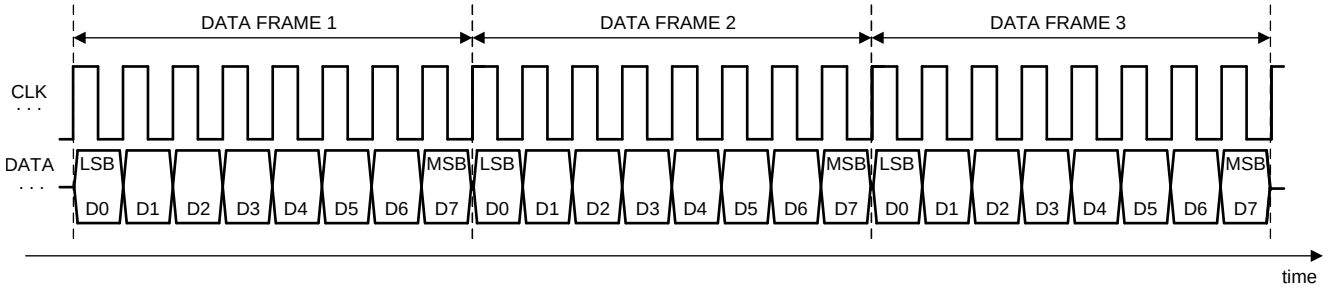


Figure 31. USART Synchronous Mode Data Flow

As shown in Figure 31, each data frame is 8-bits long with little endian format (least significant bit [LSB] first). All other functionality of the USART synchronous mode aligns with the USART asynchronous mode. Muxing of the IO pin of the USART synchronous mode is not possible and the IO pin transceiver is disabled when the device is communicating through USART in the case when the IO_IF_SEL bit is set to 1.

The PGA460 device can communicate in USART synchronous mode immediately when a rising clock on the SCLK pin is detected. No activation or deactivation of this mode is available.

If this communication mode is not used, the SCLK pin should be connected to GND to prevent noise triggering the clock input.

7.3.6.2.2 One-Wire UART Interface

The PGA460 device implements an option to connect the UART interface on the IO pin. In this case, the UART interface becomes a battery-voltage one-wire interface (OWI) because the IO pin is an open-drain type and implements a 10-kΩ pullup to the VPWR pin. This feature is possible because the communication on the UART interface is unidirectional at all times.

To enable the one-wire UART interface the IO_IF_SEL bit must be set to 1, in which case the internal communication multiplexers connect the digital logic of the UART interface to the IO-pin transceiver. The RXD and TXD pins are not changed and their operation is preserved.

Although UART communication through the IO pin, RXD pin, and TXD pin is allowed simultaneously, a possibility can occur for data collision in the case when the master controller is communicating to the IO pin while another master-controlled is trying to communicate through the UART transceiver on the RXD and TXD pins. Therefore, in an application where the IO pin is used, the RXD pin must be connected to the Hi-Z state which would cause the UART transceiver to disable when the PGA460 device has been enabled. For a detailed explanation, see the *Interface Description* section.

NOTE

When UART sync mode is selected while the IO_IF_SEL bit is set to 1 (IO pin to UART interface) the IO transceiver is disabled.

7.3.6.2.3 Ultrasonic Object Detection Through UART Operations

The PGA460 UART interface has the capability to record up to 8 objects that would cut the assigned threshold. The result is expressed as a 1-µs interval time value from the time when the burst stage is complete and the echo signal drops below the assigned threshold to the moment when any of the detected objects cut the assigned threshold again. Additionally, the width of the echo signal that cuts the threshold and the peak amplitude of the object is also measured and reported. If the object is detected at the end of record time, then object width is reported as 0xFF.The width of the echo that cuts the threshold is expressed as 4-µs interval-time values. When a LISTEN ONLY command is used, the object detection starting point is at the start time of the record interval. Figure 32 and Figure 33 show an example of two objects being detected with BURST/LISTEN and LISTEN ONLY commands, respectively. Object detection cannot occur when the DATADUMP_EN bit is set to 1.

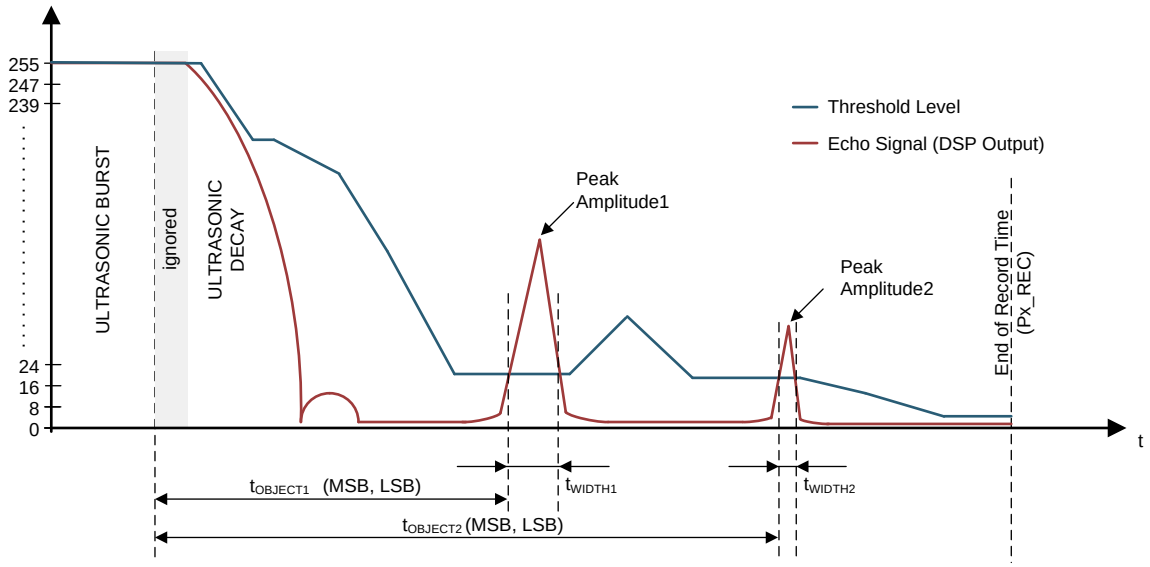


Figure 32. UART Object Detection Signaling With Burst and Listen Command

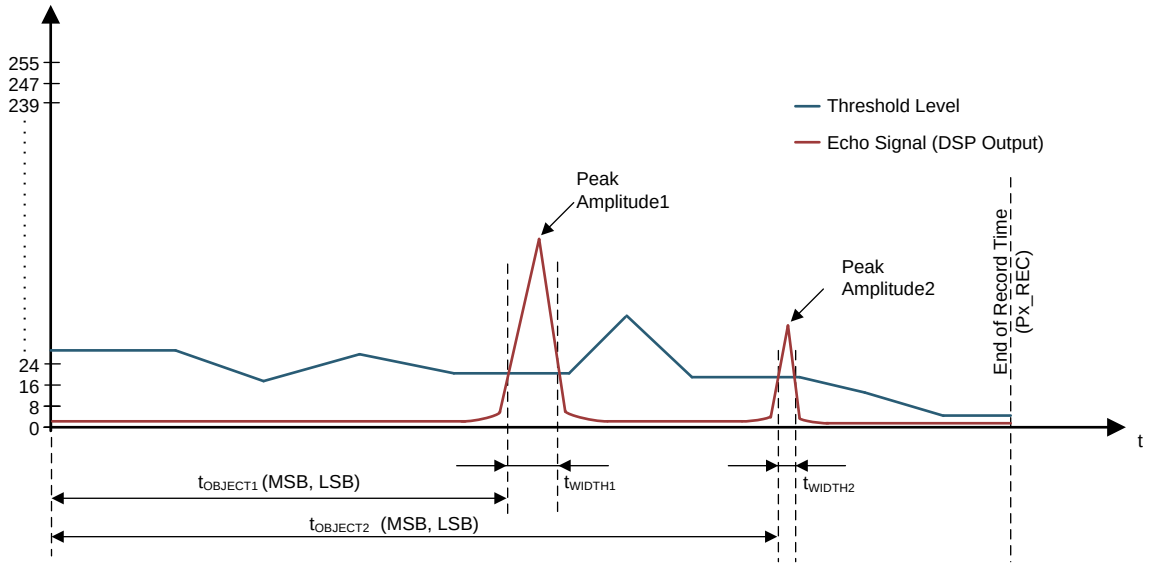


Figure 33. UART Object Detection Signaling With LISTEN ONLY Command

The comparison is done between the assigned threshold and the amplitude of the signal at the output of the DSP data path. If the threshold level is higher in value than the signal amplitude then no object is being detected. If the signal amplitude is higher in value than the threshold level denoting an echo reflection then an object is detected and the time-mark is captured. When the record time reaches the end of the record defined by the Px_REC parameters and the number of objects to be detected is still not achieved, the record interval is complete and the undetected object locations are assigned a value of 0xFF. At this point the device is ready for the next command which should be USART command 5. In case the number of objects to be detected is fulfilled before the end of record interval, the device interrupts the record cycle because the number of objects has already been detected and the device is ready for command 5. Issuing command 5 before issuing command 0 to 4 provides unpredictable data.

The following example shows how to use the PGA460 UART commands for object detection:

1. On PGA460 power up, the master configures the following:
   - EEPROM by using the EEPROM bulk write command
   - Time-varying gain by using the time-varying gain bulk write command
   - Threshold parameters by using the threshold bulk write command or by independently writing to a particular parameter by using the register write command
2. When the PGA460 device has been configured, the master device issues a run command with any of the following commands:
   - BURST/LISTEN (Preset1)
   - BURST/LISTEN (Preset2)
   - LISTEN ONLY (Preset1)
   - LISTEN ONLY (Preset2)

   Following a successful receive of any of the these run commands the PGA460 device immediately runs the requested action.
3. When the record interval has expired, the master device can issue the ultrasonic measurement result command to collect the data from the PGA460 device.

7.3.6.3 In-System IO-Pin Interface Selection

The PGA460 device is factory programmed with the time-command interface enabled on the IO-pin. In a system where the end user uses the IO-pin in a one-wire UART mode, two possible options of enabling the one-wire UART interface on the IO-pin are available as follows:

- If access to the UART RXD and TXD pins is possible then the user can set the IO_IF_SEL bit to 1 in the EEPROM memory space and then execute an EEPROM program command to store the configuration for

future use.

- If access to the RXD and TXD pins is not possible (assuming the end product has already been assembled) then the device can be toggled between interfaces by using the pattern on the IO-pin shown in Figure 34.

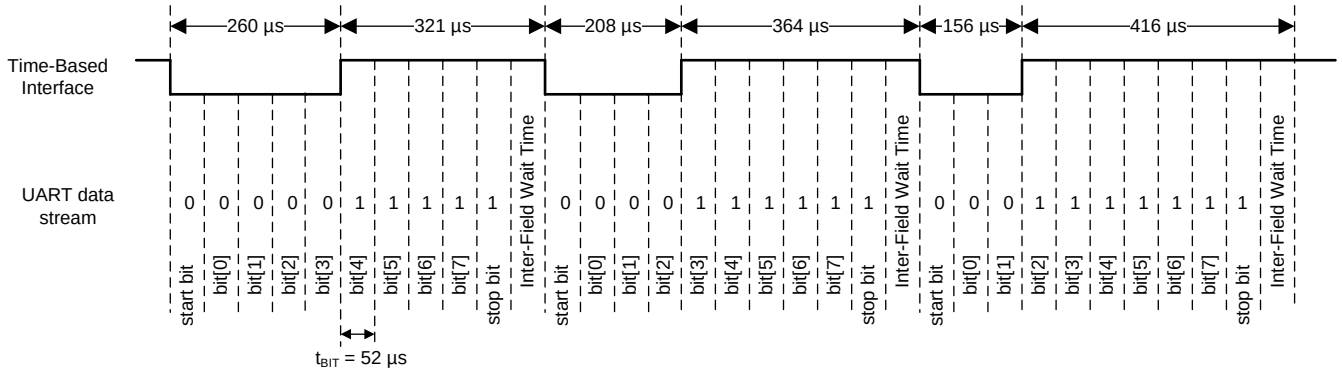


Figure 34. IO-Pin Interface Toggle Pattern

As show in Figure 34, the data format is selected in a specific way so that a time-command interface and a UART interface can easily reproduce the pattern. The following two scenarios are possible:

IO-Pin in time-command interface while the master device is in UART interface In this case the master device can send a UART frame with the following data: 0xF0 followed by 0xF8 followed by 0xFC while the UART baud-rate is 19200 bps.

NOTE

In this case the master device does not generate a sync field.

IO-Pin in UART interface while the master deivce is in time-command interface In this case the master device generates three time-command pulses with time durations as shown in Figure 34.

As soon as the data is received by the PGA460 device, the interface on the IO-pin is toggled. The pattern in Figure 34 toggles the value of the IO_IF_SEL bit in the EEPROM memory; however, it does not program the EEPROM. Therefore, as soon as the PGA460 Interface is set to the target interface, the master controller must issue a command to program the EEPROM with the desired configuration.

NOTE

In case of toggling the selection pattern for the IO interface option, a STAT2 bit is triggered to 1. Upon reading, the STAT2 bit is cleared.

7.3.7 Echo Data Dump

7.3.7.1 On-Board Memory Data Store

The PGA460 device offers a data-dump function where the data at the output of the digital data path can be extracted in a raw digital format. This function is usually required for the ultrasonic system to be properly tuned and to make correct time-varying gain and threshold adjustments. Additional uses can include system evaluation and testing.

The echo data-dump function can be enabled for any of the four BURST/LISTEN or LISTEN ONLY commands and is enabled by the DATADUMP_EN bit in the EE_CNTRL register. When enabled, and upon receiving a BURST/LISTEN or a LISTEN ONLY command, the PGA460 device holds the IO pin low for the entire record interval thus signaling the master MCU that data-dump cycle is in progress. When the data-dump cycle is complete the data can be extracted by the data dump read command. For more information on the PGA460 device commands, see Table 2.

The data-dump memory is composed of a 128-byte data memory array. Echo data is down sampled to allow capturing of the complete recording interval. The down sampling amount depends on the record time-length parameter for the preset of interest set by the P1_REC and P2_REC bits in the REC_LENGTH EEPROM register. During the process of down-sampling, a peak hold function is performed and therefore only the highest level values after down-sampling are stored in the data-dump memory. When the DATADUMP_EN bit is 1, object detection and measurement is disabled.

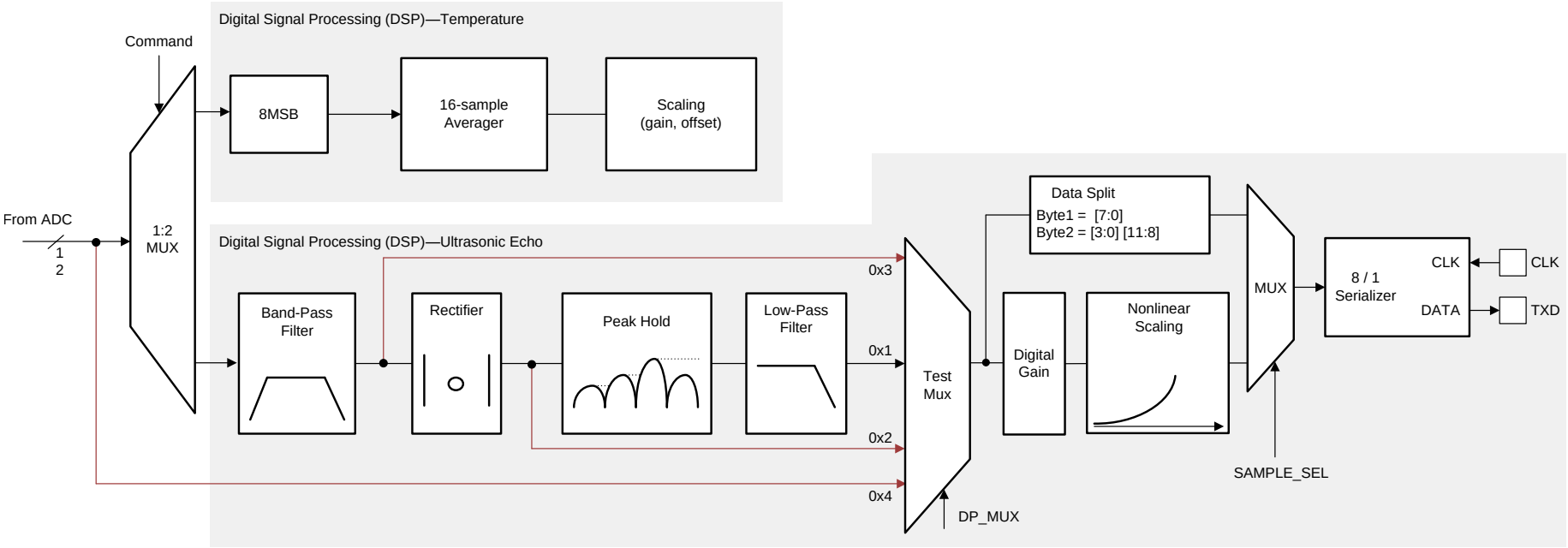
The following is a brief example to present the data dump implementation:

1. The DATADUMP_EN bit is set to 1.
2. The P1_REC bit is set to 0x01, which selects a record time-length interval of 8192 µs. Because the output rate of the digital data dath is 1 µs/sample, the total record interval has 8192 samples.
3. When any of BURST/LISTEN (Preset1) or LISTEN ONLY (Preset1) commands is executed, one sample location in the data-dump memory is written with the highest (peak) value of 8192 / 128 = 64 samples.

   Therefore the first data-dump value is the highest value of the 0–63 sample range while the last data-dump value is the highest value 8127–8191 sample range.

7.3.7.2 Direct Data Burst Through USART Synchronous Mode

In the case where each 1-µs Data-Path sample is needed to be extracted for further analysis, the PGA460 device offers a Test Mode where the Raw Digital data can be extracted at different points in the Digital data path as shown in Figure 35. Data burst is enabled when DP_MUX value is greater than 0 and less than 5, then the object detection and measurement is disabled.



This feature is only possible in USART Synchronous Mode.

Figure 35. Direct Data Burst

To enable this mode, the Digital Data-Path Mux can select the source signal to be burst out of the device by setting the DP_MUX parameter in the device memory. Once the DP_MUX parameter is enabled (set to a value other than 0x00), and if any of the SEND/RECEIVE, Receive Only or TEMPERATURE READ commands are issued using the standard UART command method, the selected source signal is passed through the Digital Multiplexer and Serialized by the 8/1 Serializer block. This signal is immediately outputted on the UART TXD pin that now acts as a data output pin, while the master sends clock pulses to the CLK pin.

It is important that after issuing any of these commands the master does not stop sending clock pulses on the CLK pin until the Bus is idle. Once a Checksum received is verified and the bus is idle, that is considered the end of the Burst data. This is needed for proper data synchronization in the PGA460 device. For further explanation on the USART Synchronous communication mode, see the *USART Synchronous Mode* section.

Figure 36 shows the format of the order of the data stream coming out of the PGA460 device.

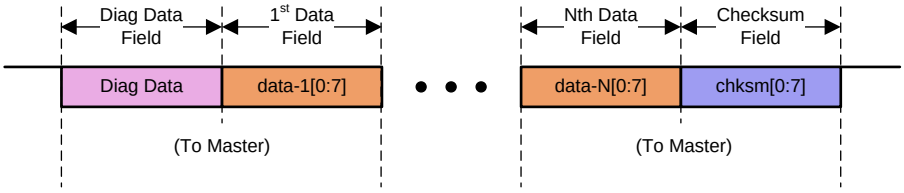


Figure 36. Direct Data Burst Data Format

As shown in Figure 36, the output data-stream starts with a PGA460 diagnostic data field, followed by number of data bytes and ends with a checksum field calculated on the diagnostic data byte and all data bytes. The number of data bytes depends on the number of samples extracted from the PGA460 device, which depends on the Recording Time Interval of the current command. The recording time Interval is determined by the P1_REC and P2_REC parameters in the EEPROM memory while the sampling rate of the ADC and digital signal path is 1 µs / Sample. From here it can be calculated that the number of samples is equivalent to the recording time when expressed in microseconds.

The digital output offers two modes of operation based on the SAMPLE_SEL parameter:

When SAMPLE_SEL = 0 The output of the data path is selected by the Digital Data-Path Test Mux and the data length is 8 bits/sample long. For the LPF output , we now use the active digital gain select to determine which 8 bits are sent out. For all the others, if the active digital gain select = 0 then we get the 8 MSB bits, else the PGA460 sends the 8 LSB bits. In this case, the sample rate is 1us, meaning every sample that the ADC outputs will also be sent out of the PGA460 device.

When SAMPLE_SEL = 1 The output of the data path is selected by the digital data path test mux. However, the full 12bits/sample data length is sent out of the PGA460 device. In this case, the sample rate is 2 µs, meaning every 2nd sample produced by the ADC will be sent out. The 12 bit data is split into two bytes and sent in the order LS Byte followed by the MS Byte. The MS Byte is padded with a 4 bit sample counter so that the master controller can track the order of samples from the PGA460 device.

NOTE

For both of the previously listed options, the nonlinear scaling block is only enabled if the data is extracted from the Low-Pass filter (DP_MUX = 0x1). In all other cases, the nonlinear scaling block is disabled.

7.3.8 Low-Power Mode

The PGA460 device implements a low-power mode where the current consumption is significantly reduced to preserve system power. The low-power mode feature is enabled by setting the LPM_EN bit in the EEPROM. If this bit is set, the PGA460 device goes into low-power mode after a certain period of inactivity as defined by the LPM_TMR bits in the FVOLT_DEC EEPROM register. Inactivity is defined when no activity occurs on the communication interfaces such as commands to BURST/LISTEN, LISTEN ONLY, or to configure the device. Any command causes a reset of the timer. During the programming of the EEPROM, the timer remains in reset.

In low-power mode the PGA460 device can wake up in two different ways based on the interface used for communication: time-command interface and USART interface. These ways are described in the following sections.

7.3.8.1 Time-Command Interface

The device wakes up immediately after a deglitched falling edge on the IO pin is detected. The master controller must generate a wake-up signal defined as a dominant pulse (logic 0) on the time command interface with a length of at least 300 µs. After the wake-up pulse is complete, at least one command processing dead-time must be allowed before starting a time-command pulse which is shown in Figure 37.

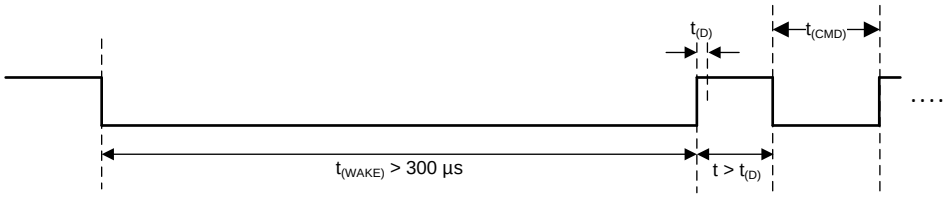


Figure 37. Time Command Interface Wake-Up Pulse

7.3.8.2 UART Interface

The master device must generate a wake-up signal defined as a dominant pulse (logic 0) on the UART interface with a length of at least 300 µs. After the wake-up pulse is complete, at least one inter-byte space must be allowed before starting a UART transmission. Figure 38 shows an example of a UART wakeup.

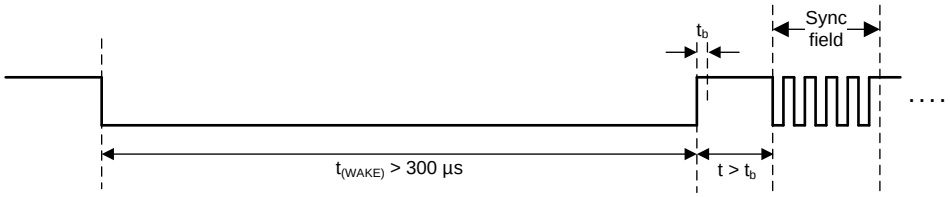


Figure 38. UART Wake-Up Pulse

7.3.9 Transducer Time and Temperature Decoupling

7.3.9.1 Time Decoupling

The PGA460 device has the option to decouple the transducer from the transformer and the rest of the driving circuitry during the echo detection stage of the record interval. The transducer is less exposed to noise generated by the driving circuit during this process and is less loaded, meaning the detected echo is capable of producing a higher voltage swing to be detected by the PGA460 device. For this function, the DECPL pin on the PGA460 device is used that drives the gate (or base) of an external transistor, Q_{DECPL}. During the burst and decay stages of the record interval the DECPL pin is high (3.3 V or 5 V depending on the IOREG level) and enables the external transistor which then connects the transformer driving circuit to GND and couples it to the transducer. The time-decoupling function is selected when the DECPL_TEMP_SEL bit in the EEPROM is set to 0.

When the burst stage is complete, a timer is started which times to the value defined by the DECPL_T bit in the EEPROM. When this time has elapsed, the state of the DECPL pin becomes low (GND) which means that the external transistor, Q_{DECPL}, is disabled which disconnects the transformer secondary coil from the transducer. Figure 39 shows the circuit implementation.

7.3.9.2 Temperature Decoupling

Similarly to time decoupling, a temperature-decoupling function has been implemented in the PGA460 device that can connect and disconnect a temperature-compensation capacitor at a certain temperature point to compensate for the temperature nonlinearity of the transducer. By using this function, the transducer frequency is assumed to remain within limits across temperature. To enable this function, the DECPL_TEMP_SEL bit must be set to 1.

Upon receiving a run command, the PGA460 device executes the TEMPERATURE MEASUREMENT command first and compares the result with the temperature setting defined by the DECPL_T bit in the EEPROM. If the temperature measured is higher than the value based on the DECPL_T bit, then the DECPL pin is low (GND) causing the Q_{DECPL} transistor to be disabled and the temperature compensation capacitor to disconnect. If the measured temperature is less than the value based on the DECPL_T bit, the DECPL pin is high (3.3 V or 5 V depending on the IOREG level), the Q_{DECPL} transistor is enabled and the temperature compensation capacitor is connected to the circuit. Figure 40 shows the circuit implementation.

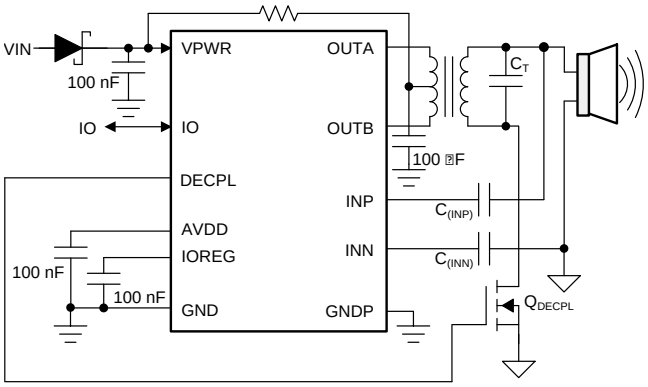


Figure 39. Transducer Time Decoupling

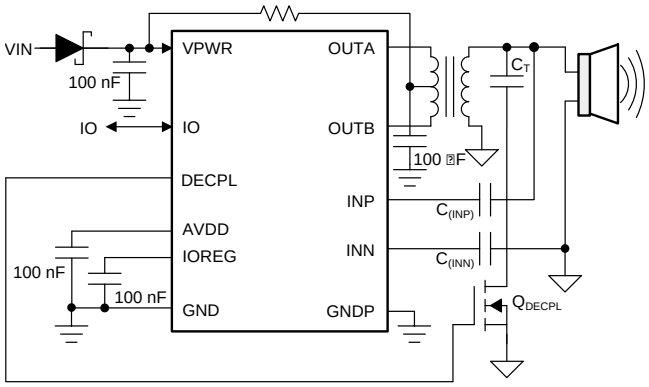


Figure 40. Transducer Temperature Decoupling

7.3.10 Memory CRC Calculation

The PGA460 implements a cyclic redundancy check (CRC) that is a self-contained algorithm to verify the integrity of the EEPROM stored data and threshold settings. When an EEPROM program or EEPROM-reload operation is executed, or when a threshold register is written, the CRC controller calculates the correct CRC value and writes it to the corresponding registers: For EEPROM memory, this value is written to the EE_CRC register. For threshold settings, this value is written to the THR_CRC register.

A CRC is performed at power-up when an EEPROM reload command is issued. The CRC algorithm for all memory blocks is the same and is shown in Equation 6 with an initial seed value of 0xFF and uses MSB ordering. This calculation is performed byte wise starting from the MSB to the LSB. The data is concatenated as follows:

- For EEPROM memory: Concatenation starts with MSB USER_DATA1 (0x00) to LSB P2_GAIN_CTRL (0x2A) and calculated CRC is stored in the EE_CRC register (0x2B)
- For threshold settings: Concatenation starts with MSB P1_THR_0 (0x5F) to LSB P2_THR_15 (0x7E) and calculated CRC is stored in the THR_CRC register (0x7F)

$$X^8 + X^2 + X + 1 \text{ (ATM HEC)} \quad (6)$$

The results of the CRC check are stored in the DEV_STAT0 register and can be directly read through the UART interface, while the time-command interface reports these in *Status Bit3* and *Status Bit1*. For more information on the time-command interface status bits, see the *Time-Command Interface* section. For the default values, see the *Register Maps* section.

7.3.11 Temperature Sensor and Temperature Data-Path

The PGA460 device has an on-chip temperature sensor and a dedicated temperature data path for accurate temperature measurement. The output value is provided as an unsigned 8-bit number from –40°C to +125°C. The temperature sensor measurement can be used to adjust the variation of the transducer performance as the ambient temperature changes. The temperature measurement's sample and conversion time requires at least 100 us after the temperature measurement command is issued. Do not send other commands during this time to allow the temperature value to properly update.

The output of the temperature digital data path can be read by using the time-command interface of the UART interface. The value provided is related to the measured temperature as shown in Equation 7.

$$T = \frac{T_{(VAL)} - 64}{1.5}$$

$$T_{(VAL)} = ADC_{UNCOMP} \times \left(1 + \frac{TEMP\_GAIN}{128}\right) + TEMP\_OFF$$

where

- $T_{(VAL)}$is value read from the device using TCI or UART commands.
- T is the temperature.
- TEMP_GAIN and TEMP_OFF are signed values in the limits from –8 to +7. (7)

Because the output value of $T_{(VAL)}$ after the calculation can result in a decimal number, the value is rounded-up to the closest integer value.

The temperature digital data path consists of a 16-sample averager and a scaling block as shown in Figure 41. The 16-sample averaging block averages 16 temperature measurements arriving at a rate of 1 sample/µs into one result to remove temperature measurement variations. The scaling block is used to adjust the Gain and the offset parameter to better calibrate the temperature sensor. These two parameters are programmed using TEMP_GAIN and TEMP_OFF bits in the TEMP_TRIM EEPROM register.

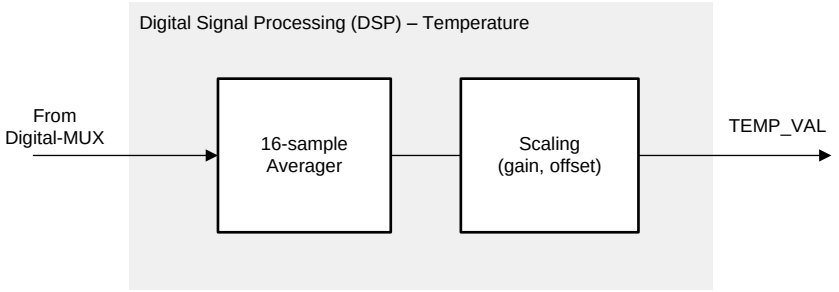


Figure 41. Temperature-Sensor Signal Path

Before compensation (TEMP_GAIN bit set to 0, TEMP_OFF bit set to 0), $T_{(VAL)}$ is same the value converted by the ADC. As previously above, the user can compensate for variations in operating conditions (VPWR), board design, and configuration of the device by performing a two-temperature measurement and trim. After compensation, $T_{(VAL)}$ can be converted to an absolute temperature using Equation 7. As the VPWR is increased, power dissipation increases and the internal die temperature can be different from the ambient temperature. The temperature sensor always indicates the die temperature.

Without calibrating TEMP_GAIN and TEMP_OFF, the ambient temperature can be approximated from the die temperature reading using Equation 8

$$T_{Ambient}\ (°C) = T_{Die} - [R_{\theta JA} \times (VPWR \times I_{VPWR\_RX\_ONLY})]$$

where

- $R_{\theta JA}$(°C/W) is the Junction-to-ambient thermal resistance of 96.1°C/W.
- VPWR (V) is the input voltage.
- $I_{VPWR\_RX\_ONLY}$(mA) is the supply current from VPWR pin during listen only mode of 12mA. (8)

7.3.12 TEST Pin Functionality

The PGA460 TEST pin serves multiple purposes including:

- Allows the user to extract internal signals from the PGA460 device.
- Selects the output voltage of the digital pins which enables a 3.3-V MCU or a 5-V MCU to be connected to the device without using any external voltage translators. The RXD, TXD, SCLK, DECPL, and TEST pins are affected by this selection.

Internal signals on the TEST pin can be extracted by selecting a predefined signal through the internal test mux. The TEST_MUX register parameter is used to select this signal. Table 5 lists the possible PGA460 internal signals that are output at the TEST pin.

Table 5. Internal Signals that can be Muxed out on the TEST Pin

TEST_MUX VALUE	SIGNAL NAME	TYPE	DESCRIPTION
0x00	Hi-Z (disabled)	Analog	The TEST pin is in the high impedance state
0x01	ASC Output		SAR ADC input after the ADC buffer
0x02	Reserved		
0x03	Reserved		
0x04	8MHz Clock	Digital	8-MHz clock output from PGA460
0x05	ADC Sample Clock		1-µs ADC sample Clock
0x06	Reserved		
0x07	Reserved		

When used as an analog test-mux output, the TEST pin output voltage can change from 0 V to 1.8 V while the common mode voltage is set to 0.9 V.

The digital voltage-level selection performed by the TEST pin is executed at device power up. On power-up, the device checks the level of the TEST pin. If the level is low, the digital output pins operate at 3.3 V. If the TEST pin is tied high (3.3 V or 5 V are both considered high state), the digital output pins operate at a 5 V. This condition is latched in the PGA460 device so that the test mux can further use the TEST pin as previously described. If the application requires that a 5-V digital output is used and a test mux output must be extracted from the PGA460 device, then a weak pullup resistor on the TEST pin can be connected as shown in Figure 42.

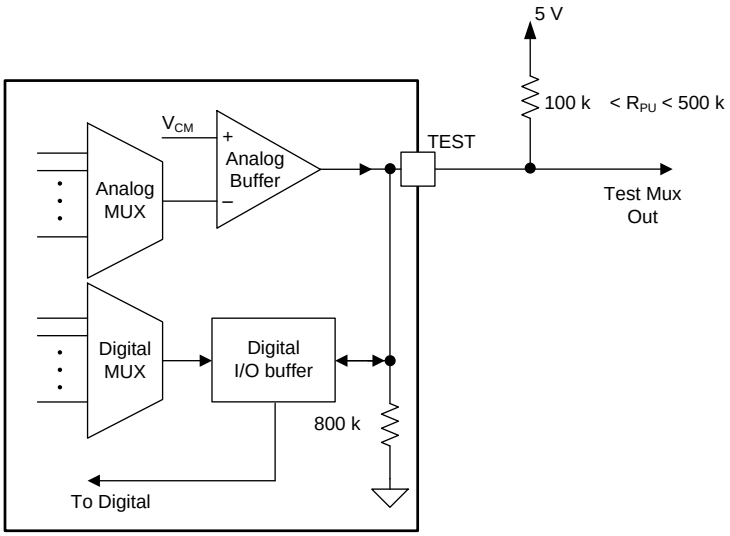


Figure 42. Test Pin Test Mux Output Application

As shown in Figure 42, the resistor (R_{PU}) is connected to a permanent power supply and a current path to ground is generated through the R_{PU} resistor and the 800-kΩ internal resistance. This configuration is no problem for the system; however, it might cause a small quiescent-current increase in applications that require the use of the PGA460 low-power mode to preserve energy. In this case, the TEST pin can be connected to a GPIO pin on the external MCU that can output a logic low or high state on the TEST pin to select the voltage level at device start-up and later disable the GPIO output to preserve energy or reconfigure the GPIO as an input in case the MCU uses any of the PGA460 test output signals. The external pullup resistor is only required for CMOS 5-V UART communication and is not required for 3-V communication.

7.4 Device Functional Modes

The PGA460 device functional modes as defined as:

Active mode After the power-up sequence is complete, the device waits for a BURST/LISTEN or LISTEN ONLY command to drive the transducer, and amplify and condition the received echo. In this mode, the device can also be configured with various parameters, and data about the detected object can be queried from the device. All these functions are achieved using commands defined in *Interface Description* section.

Low-power mode The device can be configured to go to this mode after a defined period of inactivity as defined in *Low-Power Mode* section. In this mode most of the blocks are turned off to dramatically reduce current consumption. The device can come out of this mode with commands on the interface as described in the *Time-Command Interface* and *UART Interface* section. In this mode, the device cannot burst or listen for an echo. All configuration stored in volatile memory is also lost. This includes all threshold timing and level values.

7.5 Programming

Figure 43 and Figure 44 are flow charts showing how the PGA460 device can be configured using the USART or the TCI interfaces respectively.

Programming (continued)

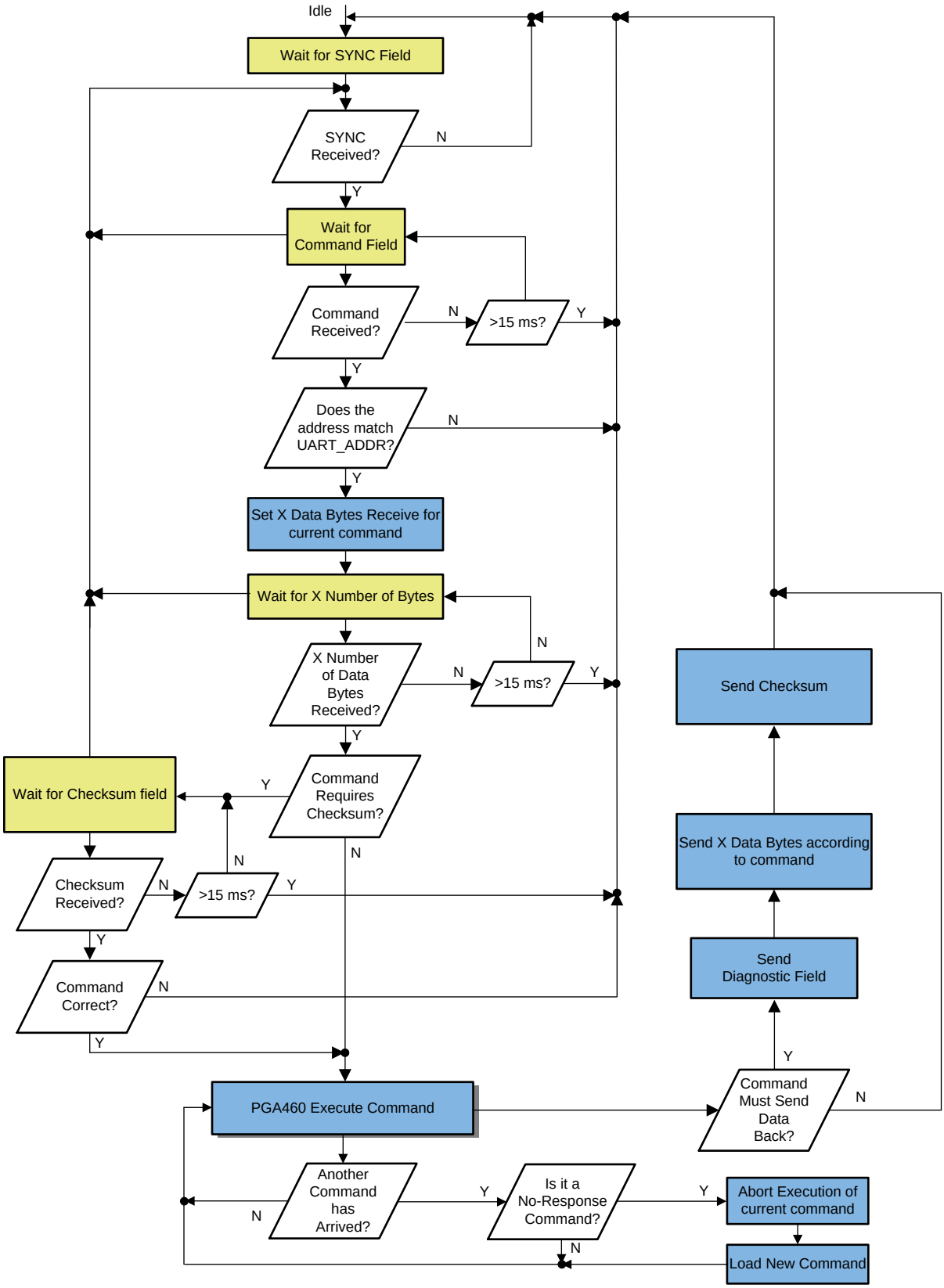


Figure 43. UART Communication Flow Chart

Programming (continued)

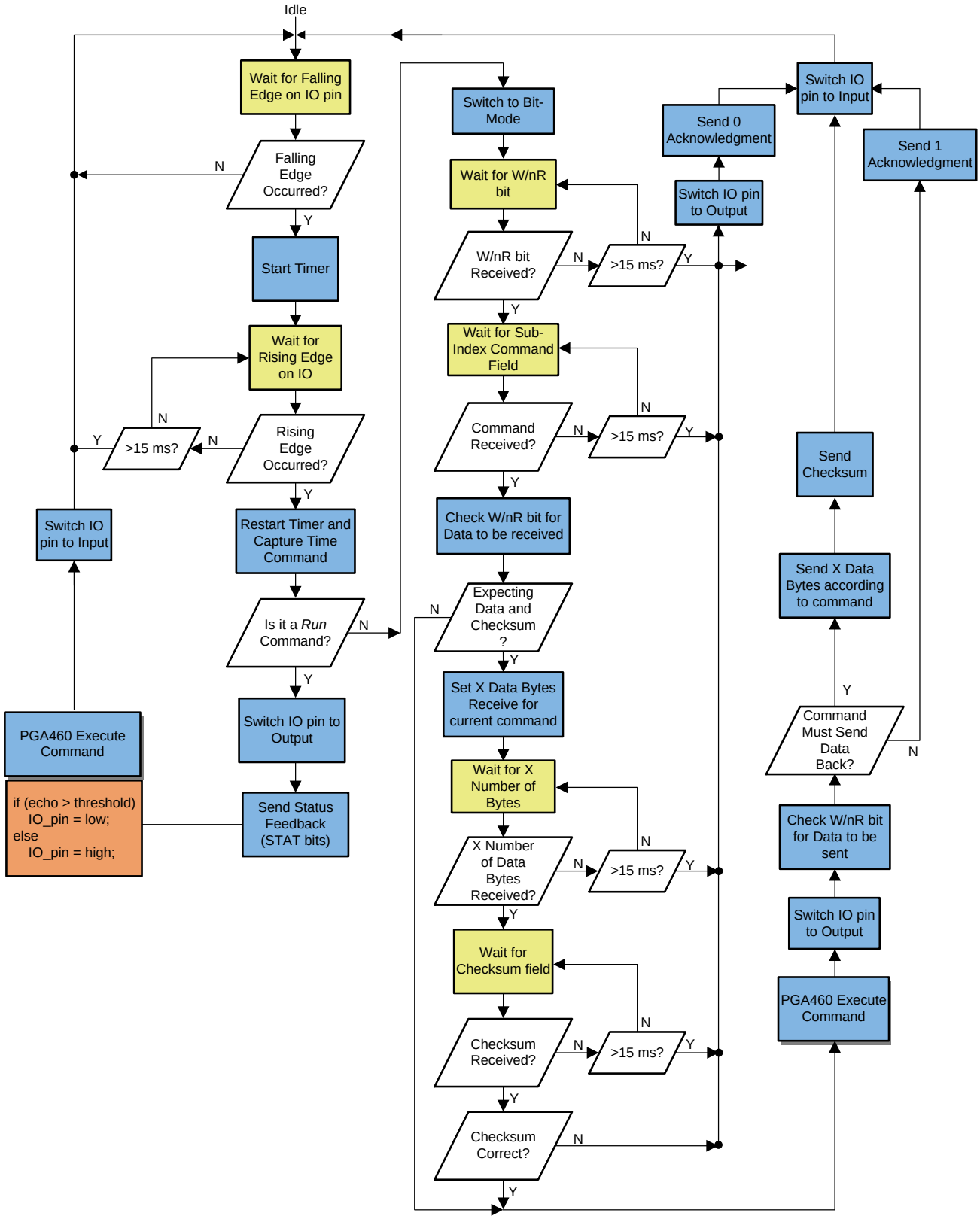


Figure 44. Time-Command Interface Communication Flow Chart

Programming (continued)

7.5.1 UART and USART Communication Examples

The following are some examples of UART and USART communication:

Example1 – Read register 0x1B, where PGA460 address is 0x0:

Master to PGA460: 0x55, 0x09, 0x1B, 0xDB …

PGA460 to master: … 0xdiag, 0xdata, 0xchecksum

Example2 – Write register 0x40, data 0x80, where PGA460 address is 0x0:

Master to PGA460: 0x55, 0x0A, 0x40, 0x80, 0x35

PGA460 to master:No response, idle (0xFF)

Example3 – Execute command 0 (Burst/Listen Preset1) to detect 1 object, where PGA460 address is 0x0:

Master to PGA460: 0x55, 0x00, 0x01, 0xFE

PGA460 to master: No response, idle (0xFF)

Example4 – Execute command 5 (ultrasonic measurement result), where PGA460 address is 0x0, assuming previous execution of Example3 where the master has commanded PGA460 to search for one object:

Master to PGA460: 0x55, 0x05, 0xFA …

PGA460 to master: … 0xdiag , 0xtime_of_flight_in_us_[MSB], 0xtime_of_flight_in_us_[LSB], 0xtime_object_width_in_us, 0xpeak_amplidute_in_LSB, 0xchecksum

NOTE

A repeatable sequence of 0xFF signifies the idle bus state.

7.6 Register Maps

7.6.1 EEPROM Programming

To program the EEPROM, follow these steps:

1. Send an EEPROM program command using UART or TCI with a unique *unlock* pattern on 4-bits. The program bit is set to 0 in register 0x40. The unlock passcode is 0x Dh.
2. Immediately send the same UART or TCI command with the program bit set to 1.

If any other command is issued after the unlock code (Step 1), the EEPROM program is initiated. Also, if the unlock command in Step 1 is not correct, the EEPROM is not programmed. The EEPROM is locked again automatically after each program command

NOTE

This EEPROM passcode is applicable by communication in the UART mode and for TCI mode done through Config command 11.

7.6.2 Register Map Partitioning and Default Values

The register map in the *Register Maps* section is organized as follows:

- Address 0h-2Bh: EEPROM nonvolatile memory. Content in these registers is preserved during power cycle and low-power mode.
- Address 40h-4Dh and address 5Fh-7Fh: Register-based volatile memory. Content in these registers is lost during power cycle and low-power mode.
- Address 2Ch-3Fh and address 4Eh-5Eh are reserved for Texas Instruments internal use and are not accessible to the user.

All registers are reset to the default values as shown in the *Register Maps* section. However, the PGA460 EEPROM is programmed to values as described in Table 6. These values are loaded into registers at power up, overwriting the default reset values.

Register Maps (continued)

Table 6. EEPROM Factory Default Values

EEPROM REGISTER	REGISTER ADDRESS	Default Value
USER_DATA1-USER_DATA-20	0h-13h	00h
TVGAIN0	14h	AFh
TVGAIN1	15h	FFh
TVGAIN2	16h	FFh
TVGAIN3	17h	2Dh
TVGAIN4	18h	68h
TVGAIN5	19h	36h
TVGAIN6	1Ah	FCh
INIT_GAIN	1Bh	C0h
FREQUENCY	1Ch	8Ch
DEADTIME	1Dh	00h
PULSE_P1	1Eh	01h
PULSE_P2	1Fh	12h
CURR_LIM_P1	20h	47h
CURR_LIM_P2	21h	FFh
REC_LENGTH	22h	1Ch
FREQ_DIAG	23h	00h
SAT_FDIAG_TH	24h	EEh
FVOLT_DEC	25h	7Ch
DECPL_TEMP	26h	0A
DSP_SCALE	27h	00h
TEMP_TRIM	28h	00h
P1_GAIN_CTRL	29h	00h
P2_GAIN_CTRL	2Ah	00h
EE_CRC	2Bh	Auto calculated on EEPROM burn

7.6.3 REGMAP Registers

Table 7 lists the memory-mapped registers for the REGMAP. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. REGMAP Registers

Offset	Acronym	Register Name	Section
0h	USER_DATA1	User general purpose data register 1	Go
1h	USER_DATA2	User general purpose data register 2	Go
2h	USER_DATA3	User general purpose data register 3	Go
3h	USER_DATA4	User general purpose data register 4	Go
4h	USER_DATA5	User general purpose data register 5	Go
5h	USER_DATA6	User general purpose data register 6	Go
6h	USER_DATA7	User general purpose data register 7	Go
7h	USER_DATA8	User general purpose data register 8	Go
8h	USER_DATA9	User general purpose data register 9	Go
9h	USER_DATA10	User general purpose data register 10	Go
Ah	USER_DATA11	User general purpose data register 11	Go
Bh	USER_DATA12	User general purpose data register 12	Go
Ch	USER_DATA13	User general purpose data register 13	Go

Table 7. REGMAP Registers (continued)

Offset	Acronym	Register Name	Section
Dh	USER_DATA14	User general purpose data register 14	Go
Eh	USER_DATA15	User general purpose data register 15	Go
Fh	USER_DATA16	User general purpose data register 16	Go
10h	USER_DATA17	User general purpose data register 17	Go
11h	USER_DATA18	User general purpose data register 18	Go
12h	USER_DATA19	User general purpose data register 19	Go
13h	USER_DATA20	User general purpose data register 20	Go
14h	TVGAIN0	Time-varying gain map segment configuration register 0	Go
15h	TVGAIN1	Time-varying gain map segment configuration register 1	Go
16h	TVGAIN2	Time-varying gain map segment configuration register 2	Go
17h	TVGAIN3	Time-varying gain map segment configuration register 3	Go
18h	TVGAIN4	Time-varying gain map segment configuration register 4	Go
19h	TVGAIN5	Time-varying gain map segment configuration register 5	Go
1Ah	TVGAIN6	Time-varying gain map segment configuration register 6	Go
1Bh	INIT_GAIN	AFE initial gain configuration register	Go
1Ch	FREQUENCY	Burst frequency configuration register	Go
1Dh	DEADTIME	Deadtime and threshold deglitch configuration	Go
1Eh	PULSE_P1	Preset1 pulse burst, IO control and UART diagnostic configuration	Go
1Fh	PULSE_P2	Preset2 pulse burst, IO control and UART diagnostic configuration	Go
20h	CURR_LIM_P1	Preset1 driver current limit configuration	Go
21h	CURR_LIM_P2	Preset2 current limit and low pass filter configuration	Go
22h	REC_LENGTH	Echo data record period configuration register	Go
23h	FREQ_DIAG	Frequency diagnostic configuration register	Go
24h	SAT_FDIAG_TH	Decay saturation, frequency diag error and Preset1 non-linear control configuration	Go
25h	FVOLT_DEC	Voltage thresholds and Preset2 non-linear scaling configuration	Go
26h	DECPL_TEMP	De-couple temp and AFE gain range configuration	Go
27h	DSP_SCALE	DSP path non-linear scaling and noise level configuration	Go
28h	TEMP_TRIM	Temperature compensation values register	Go
29h	P1_GAIN_CTRL	Preset1 digital gain configuration register	Go
2Ah	P2_GAIN_CTRL	Preset2 digital gain confiuration register	Go
2Bh	EE_CRC	User EEPROM space CRC value register	Go
40h	EE_CNTRL	User EEPROM control register	Go
41h	BPF_A2_MSB	BPF A2 coefficient most-signifcant byte configuration	Go
42h	BPF_A2_LSB	BPF A2 coefficient least-signifcant byte configuration	Go
43h	BPF_A3_MSB	BPF A3 coefficient most-signifcant byte configuration	Go
44h	BPF_A3_LSB	BPF A3 coefficient least-signifcant byte configuration	Go
45h	BPF_B1_MSB	BPF B1 coefficient most-signifcant byte configuration	Go
46h	BPF_B1_LSB	BPF B1 coefficient least-signifcant byte configuration	Go
47h	LPF_A2_MSB	LPF A2 coefficient most-signifcant byte configuration	Go
48h	LPF_A2_LSB	LPF A2 coefficient least-signifcant byte configuration	Go
49h	LPF_B1_MSB	LPF B1 coefficient most-signifcant byte configuration	Go
4Ah	LPF_B1_LSB	LPF B1 coefficient least-signifcant byte configuration	Go
4Bh	TEST_MUX	Test multiplexer configuration register	Go
4Ch	DEV_STAT0	Device Status register 0	Go

Table 7. REGMAP Registers (continued)

Offset	Acronym	Register Name	Section
4Dh	DEV_STAT1	Device status register 1	Go
5Fh	P1_THR_0	Preset1 threshold map segment configuration register 0	Go
60h	P1_THR_1	Preset1 threshold map segment configuration register 1	Go
61h	P1_THR_2	Preset1 threshold map segment configuration register 2	Go
62h	P1_THR_3	Preset1 threshold map segment configuration register 3	Go
63h	P1_THR_4	Preset1 threshold map segment configuration register 4	Go
64h	P1_THR_5	Preset1 threshold map segment configuration register 5	Go
65h	P1_THR_6	Preset1 threshold map segment configuration register 6	Go
66h	P1_THR_7	Preset1 threshold map segment configuration register 7	Go
67h	P1_THR_8	Preset1 threshold map segment configuration register 8	Go
68h	P1_THR_9	Preset1 threshold map segment configuration register 9	Go
69h	P1_THR_10	Preset1 threshold map segment configuration register 10	Go
6Ah	P1_THR_11	Preset1 threshold map segment configuration register 11	Go
6Bh	P1_THR_12	Preset1 threshold map segment configuration register 12	Go
6Ch	P1_THR_13	Preset1 threshold map segment configuration register 13	Go
6Dh	P1_THR_14	Preset1 threshold map segment configuration register 14	Go
6Eh	P1_THR_15	Preset1 threshold map segment configuration register 15	Go
6Fh	P2_THR_0	Preset2 threshold map segment configuration register 0	Go
70h	P2_THR_1	Preset2 threshold map segment configuration register 1	Go
71h	P2_THR_2	Preset2 threshold map segment configuration register 2	Go
72h	P2_THR_3	Preset2 threshold map segment configuration register 3	Go
73h	P2_THR_4	Preset2 threshold map segment configuration register 4	Go
74h	P2_THR_5	Preset2 threshold map segment configuration register 5	Go
75h	P2_THR_6	Preset2 threshold map segment configuration register 6	Go
76h	P2_THR_7	Preset2 threshold map segment configuration register 7	Go
77h	P2_THR_8	Preset2 threshold map segment configuration register 8	Go
78h	P2_THR_9	Preset2 threshold map segment configuration register 9	Go
79h	P2_THR_10	Preset2 threshold map segment configuration register 10	Go
7Ah	P2_THR_11	Preset2 threshold map segment configuration register 11	Go
7Bh	P2_THR_12	Preset2 threshold map segment configuration register 12	Go
7Ch	P2_THR_13	Preset2 threshold map segment configuration register 13	Go
7Dh	P2_THR_14	Preset2 threshold map segment configuration register 14	Go
7Eh	P2_THR_15	Preset2 threshold map segment configuration register 15	Go
7Fh	THR_CRC	Threshold map configuration registers data CRC register	Go

Complex bit access types are encoded to fit into small table cells. Table 8 shows the codes that are used for access types in this section.

Table 8. REGMAP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	C R	to Clear Read
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write

Table 8. REGMAP Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.6.3.1 USER_DATA1 Register (Address = 0h) [reset = 0h]

USER_DATA1 is shown in Figure 45 and described in Table 9.

Return to Summary Table.

User general purpose data register 1

Figure 45. USER_DATA1 Register

7	6	5	4	3	2	1	0
USER_1							
R/W-0h							

Table 9. USER_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_1	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.2 USER_DATA2 Register (Address = 1h) [reset = 0h]

USER_DATA2 is shown in Figure 46 and described in Table 10.

Return to Summary Table.

User general purpose data register 2

Figure 46. USER_DATA2 Register

7	6	5	4	3	2	1	0
USER_2							
R/W-0h							

Table 10. USER_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_2	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.3 USER_DATA3 Register (Address = 2h) [reset = 0h]

USER_DATA3 is shown in Figure 47 and described in Table 11.

Return to Summary Table.

User general purpose data register 3

Figure 47. USER_DATA3 Register

7	6	5	4	3	2	1	0
USER_3							
R/W-0h							

Table 11. USER_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_3	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.4 USER_DATA4 Register (Address = 3h) [reset = 0h]

USER_DATA4 is shown in Figure 48 and described in Table 12.

Return to Summary Table.

User general purpose data register 4

Figure 48. USER_DATA4 Register

7	6	5	4	3	2	1	0
USER_4							
R/W-0h							

Table 12. USER_DATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_4	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.5 USER_DATA5 Register (Address = 4h) [reset = 0h]

USER_DATA5 is shown in Figure 49 and described in Table 13.

Return to Summary Table.

User general purpose data register 5

Figure 49. USER_DATA5 Register

7	6	5	4	3	2	1	0
USER_5							
R/W-0h							

Table 13. USER_DATA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_5	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.6 USER_DATA6 Register (Address = 5h) [reset = 0h]

USER_DATA6 is shown in Figure 50 and described in Table 14.

Return to Summary Table.

User general purpose data register 6

Figure 50. USER_DATA6 Register

7	6	5	4	3	2	1	0
USER_6							
R/W-0h							

Table 14. USER_DATA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_6	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.7 USER_DATA7 Register (Address = 6h) [reset = 0h]

USER_DATA7 is shown in Figure 51 and described in Table 15.

Return to Summary Table.

User general purpose data register 7

Figure 51. USER_DATA7 Register

7	6	5	4	3	2	1	0
USER_7							
R/W-0h							

Table 15. USER_DATA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_7	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.8 USER_DATA8 Register (Address = 7h) [reset = 0h]

USER_DATA8 is shown in Figure 52 and described in Table 16.

Return to Summary Table.

User general purpose data register 8

Figure 52. USER_DATA8 Register

7	6	5	4	3	2	1	0
USER_8							
R/W-0h							

Table 16. USER_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_8	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.9 USER_DATA9 Register (Address = 8h) [reset = 0h]

USER_DATA9 is shown in Figure 53 and described in Table 17.

Return to Summary Table.

User general purpose data register 9

Figure 53. USER_DATA9 Register

7	6	5	4	3	2	1	0
USER_9							
R/W-0h							

Table 17. USER_DATA9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_9	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.10 USER_DATA10 Register (Address = 9h) [reset = 0h]

USER_DATA10 is shown in Figure 54 and described in Table 18.

Return to Summary Table.

User general purpose data register 10

Figure 54. USER_DATA10 Register

7	6	5	4	3	2	1	0
USER_10							
R/W-0h							

Table 18. USER_DATA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_10	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.11 USER_DATA11 Register (Address = Ah) [reset = 0h]

USER_DATA11 is shown in Figure 55 and described in Table 19.

Return to Summary Table.

User general purpose data register 11

Figure 55. USER_DATA11 Register

7	6	5	4	3	2	1	0
USER_11							
R/W-0h							

Table 19. USER_DATA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_11	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.12 USER_DATA12 Register (Address = Bh) [reset = 0h]

USER_DATA12 is shown in Figure 56 and described in Table 20.

Return to Summary Table.

User general purpose data register 12

Figure 56. USER_DATA12 Register

7	6	5	4	3	2	1	0
USER_12							
R/W-0h							

Table 20. USER_DATA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_12	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.13 USER_DATA13 Register (Address = Ch) [reset = 0h]

USER_DATA13 is shown in Figure 57 and described in Table 21.

Return to Summary Table.

User general purpose data register 13

Figure 57. USER_DATA13 Register

7	6	5	4	3	2	1	0
USER_13							
R/W-0h							

Table 21. USER_DATA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_13	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.14 USER_DATA14 Register (Address = Dh) [reset = 0h]

USER_DATA14 is shown in Figure 58 and described in Table 22.

Return to Summary Table.

User general purpose data register 14

Figure 58. USER_DATA14 Register

7	6	5	4	3	2	1	0
USER_14							
R/W-0h							

Table 22. USER_DATA14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_14	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.15 USER_DATA15 Register (Address = Eh) [reset = 0h]

USER_DATA15 is shown in Figure 59 and described in Table 23.

Return to Summary Table.

User general purpose data register 15

Figure 59. USER_DATA15 Register

7	6	5	4	3	2	1	0
USER_15							
R/W-0h							

Table 23. USER_DATA15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_15	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.16 USER_DATA16 Register (Address = Fh) [reset = 0h]

USER_DATA16 is shown in Figure 60 and described in Table 24.

Return to Summary Table.

User general purpose data register 16

Figure 60. USER_DATA16 Register

7	6	5	4	3	2	1	0
USER_16							
R/W-0h							

Table 24. USER_DATA16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_16	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.17 USER_DATA17 Register (Address = 10h) [reset = 0h]

USER_DATA17 is shown in Figure 61 and described in Table 25.

Return to Summary Table.

User general purpose data register 17

Figure 61. USER_DATA17 Register

7	6	5	4	3	2	1	0
USER_17							
R/W-0h							

Table 25. USER_DATA17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_17	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.18 USER_DATA18 Register (Address = 11h) [reset = 0h]

USER_DATA18 is shown in Figure 62 and described in Table 26.

Return to Summary Table.

User general purpose data register 18

Figure 62. USER_DATA18 Register

7	6	5	4	3	2	1	0
USER_18							
R/W-0h							

Table 26. USER_DATA18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_18	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.19 USER_DATA19 Register (Address = 12h) [reset = 0h]

USER_DATA19 is shown in Figure 63 and described in Table 27.

Return to Summary Table.

User general purpose data register 19

Figure 63. USER_DATA19 Register

7	6	5	4	3	2	1	0
USER_19							
R/W-0h							

Table 27. USER_DATA19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_19	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.20 USER_DATA20 Register (Address = 13h) [reset = 0h]

USER_DATA20 is shown in Figure 64 and described in Table 28.

Return to Summary Table.

User general purpose data register 20

Figure 64. USER_DATA20 Register

7	6	5	4	3	2	1	0
USER_20							
R/W-0h							

Table 28. USER_DATA20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	USER_20	R/W	0h	This register has no internal functional use. Register content is User defined solely for external use .

7.6.3.21 TVGAIN0 Register (Address = 14h) [reset = 0h]

TVGAIN0 is shown in Figure 65 and described in Table 29.

Return to Summary Table.

Time-varying gain map segment configuration register 0

Figure 65. TVGAIN0 Register

7	6	5	4	3	2	1	0
TVG_T0				TVG_T1			
R/W-0h				R/W-0h			

Table 29. TVGAIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TVG_T0	R/W	0h	Time varying gain Start time parameter: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs
3:0	TVG_T1	R/W	0h	Time Varying Gain T0/T1 Delta Time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs

7.6.3.22 TVGAIN1 Register (Address = 15h) [reset = 0h]

TVGAIN1 is shown in Figure 66 and described in Table 30.

Return to Summary Table.

Time-varying gain map segment configuration register 1

Figure 66. TVGAIN1 Register

7	6	5	4	3	2	1	0
TVG_T2				TVG_T3			
R/W-0h				R/W-0h			

Table 30. TVGAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TVG_T2	R/W	0h	Time Varying Gain T1/T2 Delta Time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs
3:0	TVG_T3	R/W	0h	Time Varying Gain T2/T3 Delta Time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs

7.6.3.23 TVGAIN2 Register (Address = 16h) [reset = 0h]

TVGAIN2 is shown in Figure 67 and described in Table 31.

Return to Summary Table.

Time-varying gain map segment configuration register 2

Figure 67. TVGAIN2 Register

7	6	5	4	3	2	1	0
TVG_T4				TVG_T5			
R/W-0h				R/W-0h			

Table 31. TVGAIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TVG_T4	R/W	0h	Time Varying Gain T3/T4 Delta Time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs
3:0	TVG_T5	R/W	0h	Time Varying Gain T4/T5 Delta Time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs

7.6.3.24 TVGAIN3 Register (Address = 17h) [reset = 0h]

TVGAIN3 is shown in Figure 68 and described in Table 32.

Return to Summary Table.

Time-varying gain map segment configuration register 3

Figure 68. TVGAIN3 Register

7	6	5	4	3	2	1	0
TVG_G1						TVG_G2	
R/W-0h						R/W-0h	

Table 32. TVGAIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	TVG_G1	R/W	0h	TVG Point 1 Gain Value: Gain = 0.5 * (TVG_G1 +1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register
1:0	TVG_G2	R/W	0h	TVG Point 2 Gain Value: Gain = 0.5 * (TVG_G2 + 1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register

7.6.3.25 TVGAIN4 Register (Address = 18h) [reset = 0h]

TVGAIN4 is shown in Figure 69 and described in Table 33.

Return to Summary Table.

Time-varying gain map segment configuration register 4

Figure 69. TVGAIN4 Register

7	6	5	4	3	2	1	0
TVG_G2				TVG_G3			
R/W-0h				R/W-0h			

Table 33. TVGAIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TVG_G2	R/W	0h	TVG Point 2 Gain Value: Gain = 0.5 * (TVG_G2 +1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register
3:0	TVG_G3	R/W	0h	TVG Point 3 Gain Value: Gain = 0.5 * (TVG_G3 + 1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register

7.6.3.26 TVGAIN5 Register (Address = 19h) [reset = 0h]

TVGAIN5 is shown in Figure 70 and described in Table 34.

Return to Summary Table.

Time-varying gain map segment configuration register 5

Figure 70. TVGAIN5 Register

7	6	5	4	3	2	1	0
TVG_G3				TVG_G4			
R/W-0h				R/W-0h			

Table 34. TVGAIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TVG_G3	R/W	0h	TVG Point 3 Gain Value: Gain = 0.5 * (TVG_G3 +1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register
5:0	TVG_G4	R/W	0h	TVG Point 4 Gain Value: Gain = 0.5 * (TVG_G4 + 1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register

7.6.3.27 TVGAIN6 Register (Address = 1Ah) [reset = 0h]

TVGAIN6 is shown in Figure 71 and described in Table 35.

Return to Summary Table.

Time-varying gain map segment configuration register 6

Figure 71. TVGAIN6 Register

7	6	5	4	3	2	1	0
TVG_G5						RESERVED	FREQ_SHIFT
R/W-0h						R/W-0h	R/W-0h

Table 35. TVGAIN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	TVG_G5	R/W	0h	TVG Point 5 Gain Value: Gain = 0.5 * (TVG_G5 +1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register
1	RESERVED	R/W	0h	Reserved
0	FREQ_SHIFT	R/W	0h	Burst Frequency Range Shift: 0b = Disabled 1b = Enabled, active freqency = 6 * frequency result from calculation using equation given in the FREQUENCY register

7.6.3.28 INIT_GAIN Register (Address = 1Bh) [reset = 0h]

INIT_GAIN is shown in Figure 72 and described in Table 36.

Return to Summary Table.

AFE initial gain configuration register

Figure 72. INIT_GAIN Register

7	6	5	4	3	2	1	0
BPF_BW		GAIN_INIT					
R/W-0h		R/W-0h					

Table 36. INIT_GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	BPF_BW	R/W	0h	Digital banpass filter bandwidth: BandWidth = 2 * (BPF_BW + 1) [kHz]
5:0	GAIN_INIT	R/W	0h	Initial AFE Gain: Init_Gain = 0.5 * (GAIN_INIT+1) + value(AFE_GAIN_RNG) [dB] Where value(AFE_GAIN_RNG) is the corresponding value in dB for bits set for AFE_GAIN_RNG in DECPL_TEMP register

7.6.3.29 FREQUENCY Register (Address = 1Ch) [reset = 0h]

FREQUENCY is shown in Figure 73 and described in Table 37.

Return to Summary Table.

Burst frequency configuration register

Figure 73. FREQUENCY Register

7	6	5	4	3	2	1	0
FREQ							
R/W-0h							

Table 37. FREQUENCY Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FREQ	R/W	0h	Burst frequency equation parameter: Frequency = 0.2 * FREQ + 30 [kHz] The valid FREQ parameter value range is from 0 to 250 (00h to FAh)

7.6.3.30 DEADTIME Register (Address = 1Dh) [reset = 0h]

DEADTIME is shown in Figure 74 and described in Table 38.

Return to Summary Table.

Pulse deadtime and threshold deglitch configuration register

Figure 74. DEADTIME Register

7	6	5	4	3	2	1	0
THR_CMP_DEGLTCH				PULSE_DT			
R/W-0h				R/W-0h			

Table 38. DEADTIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	THR_CMP_DEGLTCH	R/W	0h	Threshold level comparator deglitch period: deglitch period = (THR_CMP_DEGLITCH * 8) [µs]
3:0	PULSE_DT	R/W	0h	Burst Pulse Dead-Time: DeadTime = 0.0625 * PULSE_DT[µs]

7.6.3.31 PULSE_P1 Register (Address = 1Eh) [reset = 0h]

PULSE_P1 is shown in Figure 75 and described in Table 39.

Return to Summary Table.

Preset1 pulse burst number, IO pin control, and UART diagnostic configuration register

Figure 75. PULSE_P1 Register

7	6	5	4	3	2	1	0
IO_IF_SEL	UART_DIAG	IO_DIS	P1_PULSE				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

Table 39. PULSE_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IO_IF_SEL	R/W	0h	Interface Selection on IO pin: 0b = Time-Based Interface 1b = One-Wire UART Interface
6	UART_DIAG	R/W	0h	UART Diagnostic Page Selection: 0b = Diagnostic bits related to UART interface 1b = Diagnostic bits related to System Diagnostics
5	IO_DIS	R/W	0h	Disable IO pin transceiver: 0b = IO transceiver enabled 1b = IO transceiver disabled Note: Available only if IO_IF_SEL = 0
4:0	P1_PULSE	R/W	0h	Number of burst pulses for Preset1 Note: 0h means one pulse is generated on OUTA only

7.6.3.32 PULSE_P2 Register (Address = 1Fh) [reset = 0h]

PULSE_P2 is shown in Figure 76 and described in Table 40.

Return to Summary Table.

Preset2 pulse burst number and UART address configuration register

Figure 76. PULSE_P2 Register

7	6	5	4	3	2	1	0
UART_ADDR			P2_PULSE				
R/W-0h			R/W-0h				

Table 40. PULSE_P2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	UART_ADDR	R/W	0h	UART interface address
4:0	P2_PULSE	R/W	0h	Number of burst pulses for Preset2 Note: 0h means one pulse is generated on OUTA only

7.6.3.33 CURR_LIM_P1 Register (Address = 20h) [reset = 0h]

CURR_LIM_P1 is shown in Figure 77 and described in Table 41.

Return to Summary Table.

Preset1 driver current limit configuration register

Figure 77. CURR_LIM_P1 Register

7	6	5	4	3	2	1	0
DIS_CL		CURR_LIM1					
R/W-0h		R/W-0h					

Table 41. CURR_LIM_P1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_CL	R/W	0h	Disable Current Limit for Preset1 and Preset2 0b = current limit enabled 1b = current limit disabled
5:0	CURR_LIM1	R/W	0h	Driver Current Limit for Preset1 Current_Limit = 7 * CURR_LIM1 + 50 [mA]

7.6.3.34 CURR_LIM_P2 Register (Address = 21h) [reset = 0h]

CURR_LIM_P2 is shown in Figure 78 and described in Table 42.

Return to Summary Table.

Preset2 current limit and low pass filter configuration register

Figure 78. CURR_LIM_P2 Register

7	6	5	4	3	2	1	0
LPF_CO		CURR_LIM2					
R/W-0h		R/W-0h					

Table 42. CURR_LIM_P2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	LPF_CO	R/W	0h	Lowpass filter cutoff frequency: Cut off frequency = LPF_CO + 1 [kHz]
5:0	CURR_LIM2	R/W	0h	Driver current limit for Preset2 Current limit = 7 * CURR_LIM2 + 50 [mA]

7.6.3.35 REC_LENGTH Register (Address = 22h) [reset = 0h]

REC_LENGTH is shown in Figure 79 and described in Table 43.

Return to Summary Table.

Echo data record period configuration register

Figure 79. REC_LENGTH Register

7	6	5	4	3	2	1	0
P1_REC				P2_REC			
R/W-0h				R/W-0h			

Table 43. REC_LENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	P1_REC	R/W	0h	Preset1 record time length: Record time = 4.096 * (P1_REC + 1) [ms]
3:0	P2_REC	R/W	0h	Preset2 record time length: Record time = 4.096 * (P2_REC + 1) [ms]

7.6.3.36 FREQ_DIAG Register (Address = 23h) [reset = 0h]

FREQ_DIAG is shown in Figure 80 and described in Table 44.

Return to Summary Table.

Frequency diagnostic configuration register

Figure 80. FREQ_DIAG Register

7	6	5	4	3	2	1	0
FDIAG_LEN				FDIAG_START			
R/W-0h				R/W-0h			

Table 44. FREQ_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	FDIAG_LEN	R/W	0h	Frequency diagnostic window length: For value 0h, the diagnostic is disabled. For values 0 to Fh, the window length is given by 3 * FDIAG_LEN [Signal Periods]
3:0	FDIAG_START	R/W	0h	Frequency diagnostic start time: Start time = 100 * FDIAG_START [µs] Note: this time is relative to the end-of-burst time

7.6.3.37 SAT_FDIAG_TH Register (Address = 24h) [reset = 0h]

SAT_FDIAG_TH is shown in Figure 81 and described in Table 45.

Return to Summary Table.

Decay saturation threshold, frequency diagnostic error threshold, and Preset1 non-linear enable control configuration register

Figure 81. SAT_FDIAG_TH Register

7	6	5	4	3	2	1	0
FDIAG_ERR_TH			SAT_TH				P1_NLS_EN
R/W-0h			R/W-0h				R/W-0h

Table 45. SAT_FDIAG_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	FDIAG_ERR_TH	R/W	0h	Frequency diagnostic asbolute error time threshold: threshold = (FDIAG_ERR_TH + 1) [µs]
4:1	SAT_TH	R/W	0h	Saturation diagnostic threshold level.
0	P1_NLS_EN	R/W	0h	Set high to enable Preset1 non-linear scaling

7.6.3.38 FVOLT_DEC Register (Address = 25h) [reset = 0h]

FVOLT_DEC is shown in Figure 82 and described in Table 46.

Return to Summary Table.

Voltage thresholds and Preset2 non-linear scaling enable configuration register

Figure 82. FVOLT_DEC Register

7	6	5	4	3	2	1	0
P2_NLS_EN	VPWR_OV_TH		LPM_TMR		FVOLT_ERR_TH		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		

Table 46. FVOLT_DEC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P2_NLS_EN	R/W	0h	Set high to enable Preset2 non-linear scaling
6:5	VPWR_OV_TH	R/W	0h	VPWR over voltage threshold select: 00b = 12.3 V 01b = 17.7 V 10b = 22.8 V 11b = 28.3 V
4:3	LPM_TMR	R/W	0h	Low power mode enter time: 00b = 250 ms 01b = 500 ms 10b = 1 s 11b = 4s
2:0	FVOLT_ERR_TH	R/W	0h	See section on System Diagnostics for Voltage diagnostic measurement: 000b = 1 001b = 2 010b = 3 011b = 4 100b = 5 101b = 6 110b = 7 111b = 8

7.6.3.39 DECPL_TEMP Register (Address = 26h) [reset = 0h]

DECPL_TEMP is shown in Figure 83 and described in Table 47.

Return to Summary Table.

De-couple temperature and AFE gain range configuration register

Figure 83. DECPL_TEMP Register

7	6	5	4	3	2	1	0
AFE_GAIN_RNG		LPM_EN	DECPL_TEMP_SEL	DECPL_T			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			

Table 47. DECPL_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	AFE_GAIN_RNG	R/W	0h	AFE gain range selection codes: 00b = 58 to 90 dB 01b = 52 to 84 dB 10b = 46 to 78 dB 11b = 32 to 64 dB

Table 47. DECPL_TEMP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	LPM_EN	R/W	0h	PGA460 Low Power Mode Enable: 0b = Low power mode is disabled 1b = Low power mode is enabled
4	DECPL_TEMP_SEL	R/W	0h	Decouple Time / Temperature Select: 0b = Time Decouple 1b = Temperature Decouple
3:0	DECPL_T	R/W	0h	Secondary decouple time / temperature decouple If DECPL_TEMP_SEL = 0 (Time Decouple) Time = 4096 * (DECPL_T + 1) [µs] If DECPL_TEMP_SEL = 1 (Temperature Decouple) Temperature = 10 * DECPL_T - 40 [degC]

7.6.3.40 DSP_SCALE Register (Address = 27h) [reset = 0h]

DSP_SCALE is shown in Figure 84 and described in Table 48.

Return to Summary Table.

DSP non-linear scaling and noise level configuration register

Figure 84. DSP_SCALE Register

7	6	5	4	3	2	1	0
NOISE_LVL					SCALE_K	SCALE_N	
R/W-0h					R/W-0h	R/W-0h	

Table 48. DSP_SCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	NOISE_LVL	R/W	0h	Value ranges from 0 to 31 with 1 LSB steps for digital gain values (Px_DIG_GAIN_LR) less than 8 If digital gain (Px_DIG_GAIN_LR) is larger than 8, then multiply the NOISE_LVL by Px_DIG_GAIN_LR/8
2	SCALE_K	R/W	0h	Non-Linear scaling exponent selection: 0b = 1.50 1b = 2.00
1:0	SCALE_N	R/W	0h	Selects the starting threshold level point from which the non-linear gain (if enabled) is applied: 00b = TH9 01b = TH10 10b = TH11 11b = TH12

7.6.3.41 TEMP_TRIM Register (Address = 28h) [reset = 0h]

TEMP_TRIM is shown in Figure 85 and described in Table 49.

Return to Summary Table.

Temperature sensor compensation values register

Figure 85. TEMP_TRIM Register

7	6	5	4	3	2	1	0
TEMP_GAIN				TEMP_OFF			
R/W-0h				R/W-0h			

Table 49. TEMP_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TEMP_GAIN	R/W	0h	Temperature scaling gain: signed value can range from -8 (1000b) to 7 (0111b) used for measured temperature value compensation
3:0	TEMP_OFF	R/W	0h	Temperature Scaling Offset: signed value can range from -8 (1000b) to 7 (0111b) used for measured temperature value compensation

7.6.3.42 P1_GAIN_CTRL Register (Address = 29h) [reset = 0h]

P1_GAIN_CTRL is shown in Figure 86 and described in Table 50.

Return to Summary Table.

Preset1 digital gain configuration register

Figure 86. P1_GAIN_CTRL Register

7	6	5	4	3	2	1	0
P1_DIG_GAIN_LR_ST		P1_DIG_GAIN_LR			P1_DIG_GAIN_SR		
R/W-0h		R/W-0h			R/W-0h		

Table 50. P1_GAIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	P1_DIG_GAIN_LR_ST	R/W	0h	Selects the starting Preset1 threshold level point from which the long range (LR) digital gain, P1_DIG_GAIN_LR, is applied 00b = TH9 01b = TH10 10b = TH11 11b = TH12
5:3	P1_DIG_GAIN_LR	R/W	0h	Preset1 Digital long range (LR) gain applied from the selected long range threshold level point to the end of the record period Applied to the thresholds set by P1_DIG_GAIN_LR_ST: 000b = multiplied by 1 001b = multiplied by 2 010b = multiplied by 4 011b = multiplied by 8 100b = multiplied by 16 101b = multiplied by 32 110b = invalid 111b = invalid
2:0	P1_DIG_GAIN_SR	R/W	0h	Preset1 Digital short range (SR) gain applied from time zero to the start of the selected long range (LR) threshold level point: 000b = multiplied by 1 001b = multiplied by 2 010b = multiplied by 4 011b = multiplied by 8 100b = multiplied by 16 101b = multiplied by 32 110b = invalid 111b = invalid

7.6.3.43 P2_GAIN_CTRL Register (Address = 2Ah) [reset = 0h]

P2_GAIN_CTRL is shown in Figure 87 and described in Table 51.

Return to Summary Table.

Preset2 digital gain confiuration register

Figure 87. P2_GAIN_CTRL Register

7	6	5	4	3	2	1	0
P2_DIG_GAIN_LR_ST		P2_DIG_GAIN_LR			P2_DIG_GAIN_SR		
R/W-0h		R/W-0h			R/W-0h		

Table 51. P2_GAIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	P2_DIG_GAIN_LR_ST	R/W	0h	Selects the starting Preset2 threshold level point from which the long range (LR) digital gain, P2_DIG_GAIN_LR, is applied 00b = TH9 01b = TH10 10b = TH11 11b = TH12
5:3	P2_DIG_GAIN_LR	R/W	0h	Preset2 Digital long range (LR) gain applied from the selected long range threshold level point to the end of the record period Applied to the thresholds set by P2_DIG_GAIN_LR_ST: 000b = multiplied by 1 001b = multiplied by 2 010b = multiplied by 4 011b = multiplied by 8 100b = multiplied by 16 101b = multiplied by 32 110b = invalid 111b = invalid
2:0	P2_DIG_GAIN_SR	R/W	0h	Preset2 Digital short range (SR) gain applied from time zero to the start of the selected long range (LR) threshold level point: 000b = multiplied by 1 001b = multiplied by 2 010b = multiplied by 4 011b = multiplied by 8 100b = multiplied by 16 101b = multiplied by 32 110b = invalid 111b = invalid

7.6.3.44 EE_CRC Register (Address = 2Bh) [reset = 0h]

EE_CRC is shown in Figure 88 and described in Table 52.

Return to Summary Table.

User EEPROM space data CRC register

Figure 88. EE_CRC Register

7	6	5	4	3	2	1	0
EE_CRC							
R/W-0h							

Table 52. EE_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EE_CRC	R/W	0h	User EEPROM space data CRC value

7.6.3.45 EE_CNTRL Register (Address = 40h) [reset = 00h]

EE_CNTRL is shown in Figure 89 and described in Table 53.

Return to Summary Table.

User EEPROM control register

Figure 89. EE_CNTRL Register

7	6	5	4	3	2	1	0
DATADUMP_EN	EE_UNLCK				EE_PRGM_OK	EE_RLOAD	EE_PRGM
RH/W-0h	R/W-0h				R-0h	R/W-0h	R/W-0h

Table 53. EE_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DATADUMP_EN	RH/W	0h	Data Dump Enable bit: 0b = Disabled 1b = Enabled
6:3	EE_UNLCK	R/W	0h	EEPROM program enable unlock passcode register: The valid passcode for enabling EEPROM programming is 0xD.
2	EE_PRGM_OK	R	0h	EEPROM programming status: 0b = EEPROM was not programmed successfully 1b = EEPROM was programmed successfully
1	EE_RLOAD	R/W	0h	EEPROM Reload Trigger: 0b = Disabled 1b = Reload Data from EEPROM
0	EE_PRGM	R/W	0h	EEPROM Program Trigger: 0b = Disabled 1b = Program Data to EEPROM

7.6.3.46 BPF_A2_MSB Register (Address = 41h) [reset = 00h]

BPF_A2_MSB is shown in Figure 90 and described in Table 54.

Return to Summary Table.

BPF A2 coefficient most-signifcant byte configuration

Figure 90. BPF_A2_MSB Register

7	6	5	4	3	2	1	0
BPF_A2_MSB							
R/W-0h							

Table 54. BPF_A2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_A2_MSB	R/W	0h	Bandpass filter A2 coefficient most-significant byte value

7.6.3.47 BPF_A2_LSB Register (Address = 42h) [reset = 00h]

BPF_A2_LSB is shown in Figure 91 and described in Table 55.

Return to Summary Table.

BPF A2 coefficient least-signifcant byte configuration

Figure 91. BPF_A2_LSB Register

7	6	5	4	3	2	1	0
BPF_A2_LSB							
R/W-0h							

Table 55. BPF_A2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_A2_LSB	R/W	0h	Bandpass filter A2 coefficient least-signifcant byte value

7.6.3.48 BPF_A3_MSB Register (Address = 43h) [reset = 00h]

BPF_A3_MSB is shown in Figure 92 and described in Table 56.

Return to Summary Table.

BPF A3 coefficient most-signifcant byte configuration

Figure 92. BPF_A3_MSB Register

7	6	5	4	3	2	1	0
BPF_A3_MSB							
R/W-0h							

Table 56. BPF_A3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_A3_MSB	R/W	0h	Bandpass filter A3 coefficient most-signifcant byte value

7.6.3.49 BPF_A3_LSB Register (Address = 44h) [reset = 00h]

BPF_A3_LSB is shown in Figure 93 and described in Table 57.

Return to Summary Table.

BPF A3 coefficient least-signifcant byte configuration

Figure 93. BPF_A3_LSB Register

7	6	5	4	3	2	1	0
BPF_A3_LSB							
R/W-0h							

Table 57. BPF_A3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_A3_LSB	R/W	0h	Bandpass filter A3 coefficient least-signifcant byte value

7.6.3.50 BPF_B1_MSB Register (Address = 45h) [reset = 00h]

BPF_B1_MSB is shown in Figure 94 and described in Table 58.

Return to Summary Table.

BPF B1 coefficient most-signifcant byte configuration

Figure 94. BPF_B1_MSB Register

7	6	5	4	3	2	1	0
BPF_B1_MSB							
R/W-0h							

Table 58. BPF_B1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_B1_MSB	R/W	0h	Bandpass filter B1 coefficient most-signifcant byte value

7.6.3.51 BPF_B1_LSB Register (Address = 46h) [reset = 00h]

BPF_B1_LSB is shown in Figure 95 and described in Table 59.

Return to Summary Table.

BPF B1 coefficient least-signifcant byte configuration

Figure 95. BPF_B1_LSB Register

7	6	5	4	3	2	1	0
BPF_B1_LSB							
R/W-0h							

Table 59. BPF_B1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BPF_B1_LSB	R/W	0h	Bandpass filter B1 coefficient least-signifcant byte value

7.6.3.52 LPF_A2_MSB Register (Address = 47h) [reset = 00h]

LPF_A2_MSB is shown in Figure 96 and described in Table 60.

Return to Summary Table.

LPF A2 coefficient most-signifcant byte configuration

Figure 96. LPF_A2_MSB Register

7	6	5	4	3	2	1	0
RESERVED	LPF_A2_MSB						
R-0h	R/W-0h						

Table 60. LPF_A2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LPF_A2_MSB	R/W	0h	Lowpass filter A2 coefficient most-signifcant byte value

7.6.3.53 LPF_A2_LSB Register (Address = 48h) [reset = 00h]

LPF_A2_LSB is shown in Figure 97 and described in Table 61.

Return to Summary Table.

LPF A2 coefficient least-signifcant byte configuration

Figure 97. LPF_A2_LSB Register

7	6	5	4	3	2	1	0
LPF_A2_LSB							
R/W-0h							

Table 61. LPF_A2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LPF_A2_LSB	R/W	0h	Lowpass filter A2 coefficient least-signifcant byte value

7.6.3.54 LPF_B1_MSB Register (Address = 49h) [reset = 00h]

LPF_B1_MSB is shown in Figure 98 and described in Table 62.

Return to Summary Table.

LPF B1 coefficient most-signifcant byte configuration

Figure 98. LPF_B1_MSB Register

7	6	5	4	3	2	1	0
RESERVED	LPF_B1_MSB						
R-0h	R/W-0h						

Table 62. LPF_B1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:0	LPF_B1_MSB	R/W	0h	Lowpass filter B1 coefficient most-signifcant byte value

7.6.3.55 LPF_B1_LSB Register (Address = 4Ah) [reset = 00h]

LPF_B1_LSB is shown in Figure 99 and described in Table 63.

Return to Summary Table.

LPF B1 coefficient least-signifcant byte configuration

Figure 99. LPF_B1_LSB Register

7	6	5	4	3	2	1	0
LPF_B1_LSB							
R/W-0h							

Table 63. LPF_B1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LPF_B1_LSB	R/W	0h	Lowpass filter B1 coefficient least-signifcant byte value

7.6.3.56 TEST_MUX Register (Address = 4Bh) [reset = 00h]

TEST_MUX is shown in Figure 100 and described in Table 64.

Return to Summary Table.

Test multiplexers configuration register

Figure 100. TEST_MUX Register

7	6	5	4	3	2	1	0
TEST_MUX			RESERVED	SAMPLE_SEL	DP_MUX		
R/W-0h			R-0h	R/W-0h	R/W-0h		

Table 64. TEST_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TEST_MUX	R/W	0h	Multiplexer output on the TEST Pin: 000b = GND ("Mux Off") 001b = Analog Front End output 010b = Reserved 011b = Reserved 100b = 8MHz clock 101b = ADC sample output clock 110b = Reserved 111b = Reserved Note 1 000b through 011b are analog output signals Note 2 100b through 111b are digital output signals
4	RESERVED	R	0h	Reserved
3	SAMPLE_SEL	R/W	0h	Data path sample select: 0b = 8 bit sample output at 1 µs per sample 1b = 12 bit sample output at 2 µs per sample Note: For use with DP_MUX parameter values 001b to 100b

Table 64. TEST_MUX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DP_MUX	R/W	0h	Data path multiplexer source select codes: 000b = Disabled 001b = LPF output 010b = Rectifier output 011b = BPF output 100b = ADC output 101b = Not used 110b = Not used 111b = Not used

7.6.3.57 DEV_STAT0 Register (Address = 4Ch) [reset = 84h]

DEV_STAT0 is shown in Figure 101 and described in Table 65.

Return to Summary Table.

Device Status register 0

Figure 101. DEV_STAT0 Register

7	6	5	4	3	2	1	0
REV_ID		OPT_ID		CMW_WU_ERR	THR_CRC_ERR	EE_CRC_ERR	TRIM_CRC_ERR
R-2h		R-0h		R-0h	R-1h	R-0h	R-0h

Table 65. DEV_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	REV_ID	R	2h	Device Revision Identification
5:4	OPT_ID	R	0h	Device Option Identification
3	CMW_WU_ERR	R	0h	Wakeup Error indicator: 0 = no error 1 = user tried to send a command before the wake up sequence is done
2	THR_CRC_ERR	R	1h	Threshold map configuration register data CRC error status: 0 = No error 1 = CRC error detected This flag is asserted upon device power-up to indicate the un-initialized state of the threshold map configuration registers.
1	EE_CRC_ERR	R	0h	User EEPROM space data CRC error status: 0 = No error 1 = CRC error detected
0	TRIM_CRC_ERR	R	0h	Trim EEPROM space data CRC error status: 0 = No error 1 = CRC error detected

7.6.3.58 DEV_STAT1 Register (Address = 4Dh) [reset = 00h]

DEV_STAT1 is shown in Figure 102 and described in Table 66.

Return to Summary Table.

Device status register 1

Figure 102. DEV_STAT1 Register

7	6	5	4	3	2	1	0
RESERVED	TSD_PROT	IOREG_OV	IOREG_UV	AVDD_OV	AVDD_UV	VPWR_OV	VPWR_UV
R-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 66. DEV_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	TSD_PROT	RC	0h	Thermal shut-down protection status: 0 = No thermal shutdown has occured 1 = Thermal shutdown has occured
5	IOREG_OV	RC	0h	IOREG pin over voltage status: 0 = No error 1 = IOREG over voltage error
4	IOREG_UV	RC	0h	IOREG pin under voltage status: 0 = No error 1 = IOREG under voltage error
3	AVDD_OV	RC	0h	AVDD pin over voltage status: 0 = No error 1 = AVDD over voltage error
2	AVDD_UV	RC	0h	AVDD pin under voltage status: 0 = No Error 1 = AVDD Uuder voltage error
1	VPWR_OV	RC	0h	VPWR pin over voltage status: 0 = No error 1 = VPWR over voltage error
0	VPWR_UV	RC	0h	VPWR pin under voltage status: 0 = No error 1 = VPWR under voltage Error

7.6.3.59 P1_THR_0 Register (Address = 5Fh) [reset = X]

P1_THR_0 is shown in Figure 103 and described in Table 67.

Return to Summary Table.

Preset1 threshold map segment configuration register 0

Figure 103. P1_THR_0 Register

7	6	5	4	3	2	1	0
TH_P1_T1				TH_P1_T2			
R/W-X				R/W-X			

Table 67. P1_THR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T1	R/W	X	Preset1 Threshold T1 absolute time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 67. P1_THR_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T2	R/W	X	Preset1 Threshold T2 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.60 P1_THR_1 Register (Address = 60h) [reset = X]

P1_THR_1 is shown in Figure 104 and described in Table 68.

Return to Summary Table.

Preset1 threshold map segment configuration register 1

Figure 104. P1_THR_1 Register

7	6	5	4	3	2	1	0
TH_P1_T3				TH_P1_T4			
R/W-X				R/W-X			

Table 68. P1_THR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T3	R/W	X	Preset1 Threshold T3 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 68. P1_THR_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T4	R/W	X	Preset1 Threshold T4 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.61 P1_THR_2 Register (Address = 61h) [reset = X]

P1_THR_2 is shown in Figure 105 and described in Table 69.

Return to Summary Table.

Preset1 threshold map segment configuration register 2

Figure 105. P1_THR_2 Register

7	6	5	4	3	2	1	0
TH_P1_T5				TH_P1_T6			
R/W-X				R/W-X			

Table 69. P1_THR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T5	R/W	X	Preset1 Threshold T5 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 69. P1_THR_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T6	R/W	X	Preset1 Threshold T6 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.62 P1_THR_3 Register (Address = 62h) [reset = X]

P1_THR_3 is shown in Figure 106 and described in Table 70.

Return to Summary Table.

Preset1 threshold map segment configuration register 3

Figure 106. P1_THR_3 Register

7	6	5	4	3	2	1	0
TH_P1_T7				TH_P1_T8			
R/W-X				R/W-X			

Table 70. P1_THR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T7	R/W	X	Preset1 Threshold T7 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 70. P1_THR_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T8	R/W	X	Preset1 Threshold T8 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.63 P1_THR_4 Register (Address = 63h) [reset = X]

P1_THR_4 is shown in Figure 107 and described in Table 71.

Return to Summary Table.

Preset1 threshold map segment configuration register 4

Figure 107. P1_THR_4 Register

7	6	5	4	3	2	1	0
TH_P1_T9				TH_P1_T10			
R/W-X				R/W-X			

Table 71. P1_THR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T9	R/W	X	Preset1 Threshold T9 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 71. P1_THR_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T10	R/W	X	Preset1 Threshold T10 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.64 P1_THR_5 Register (Address = 64h) [reset = X]

P1_THR_5 is shown in Figure 108 and described in Table 72.

Return to Summary Table.

Preset1 threshold map segment configuration register 5

Figure 108. P1_THR_5 Register

7	6	5	4	3	2	1	0
TH_P1_T11				TH_P1_T12			
R/W-X				R/W-X			

Table 72. P1_THR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_T11	R/W	X	Preset1 Threshold T11 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

Table 72. P1_THR_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	TH_P1_T12	R/W	X	Preset1 Threshold T12 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.65 P1_THR_6 Register (Address = 65h) [reset = X]

P1_THR_6 is shown in Figure 109 and described in Table 73.

Return to Summary Table.

Preset1 threshold map segment configuration register 6

Figure 109. P1_THR_6 Register

7	6	5	4	3	2	1	0
TH_P1_L1					TH_P1_L2		
R/W-X					R/W-X		

Table 73. P1_THR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	TH_P1_L1	R/W	X	Preset1 Threshold L1 level This bit-field powers-up un-initialized.
2:0	TH_P1_L2	R/W	X	Preset1 Threshold L2 level bits (Bit4 to Bit2) This bit-field powers-up un-initialized.

7.6.3.66 P1_THR_7 Register (Address = 66h) [reset = X]

P1_THR_7 is shown in Figure 110 and described in Table 74.

Return to Summary Table.

Preset1 threshold map segment configuration register 7

Figure 110. P1_THR_7 Register

7	6	5	4	3	2	1	0
TH_P1_L2				TH_P1_L3			TH_P1_L4
R/W-X				R/W-X			R/W-X

Table 74. P1_THR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TH_P1_L2	R/W	X	Preset1 Threshold L2 level (Bit1 to Bit0) This bit-field powers-up un-initialized.

Table 74. P1_THR_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:1	TH_P1_L3	R/W	X	Preset1 Threshold L3 level This bit-field powers-up un-initialized.
0	TH_P1_L4	R/W	X	Preset1 Threshold L4 level (Bit4) This bit-field powers-up un-initialized.

7.6.3.67 P1_THR_8 Register (Address = 67h) [reset = X]

P1_THR_8 is shown in Figure 111 and described in Table 75.

Return to Summary Table.

Preset1 threshold map segment configuration register 8

Figure 111. P1_THR_8 Register

7	6	5	4	3	2	1	0
TH_P1_L4				TH_P1_L5			
R/W-X				R/W-X			

Table 75. P1_THR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P1_L4	R/W	X	Preset1 Threshold L4 level (Bits3 to Bit0) This bit-field powers-up un-initialized.
3:0	TH_P1_L5	R/W	X	Preset1 Threshold L5 level (Bit4 to Bit1) This bit-field powers-up un-initialized.

7.6.3.68 P1_THR_9 Register (Address = 68h) [reset = X]

P1_THR_9 is shown in Figure 112 and described in Table 76.

Return to Summary Table.

Preset1 threshold map segment configuration register 9

Figure 112. P1_THR_9 Register

7	6	5	4	3	2	1	0
TH_P1_L5	TH_P1_L6					TH_P1_L7	
R/W-X	R/W-X					R/W-X	

Table 76. P1_THR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TH_P1_L5	R/W	X	Preset1 Threshold L5 level (Bit0) This bit-field powers-up un-initialized.
6:2	TH_P1_L6	R/W	X	Preset1 Threshold L6 level This bit-field powers-up un-initialized.
1:0	TH_P1_L7	R/W	X	Preset1 Threshold L7 level (Bits4 to Bit3) This bit-field powers-up un-initialized.

7.6.3.69 P1_THR_10 Register (Address = 69h) [reset = X]

P1_THR_10 is shown in Figure 113 and described in Table 77.

Return to Summary Table.

Preset1 threshold map segment configuration register 10

Figure 113. P1_THR_10 Register

7	6	5	4	3	2	1	0
TH_P1_L7				TH_P1_L8			
R/W-X				R/W-X			

Table 77. P1_THR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TH_P1_L7	R/W	X	Preset1 Threshold L7 Level (Bit2 to Bit0) This bit-field powers-up un-initialized.
4:0	TH_P1_L8	R/W	X	Preset1 Threshold L8 level This bit-field powers-up un-initialized.

7.6.3.70 P1_THR_11 Register (Address = 6Ah) [reset = X]

P1_THR_11 is shown in Figure 114 and described in Table 78.

Return to Summary Table.

Preset1 threshold map segment configuration register 11

Figure 114. P1_THR_11 Register

7	6	5	4	3	2	1	0
TH_P1_L9							
R/W-X							

Table 78. P1_THR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P1_L9	R/W	X	Threshold L9 level This bit-field powers-up un-initialized.

7.6.3.71 P1_THR_12 Register (Address = 6Bh) [reset = X]

P1_THR_12 is shown in Figure 115 and described in Table 79.

Return to Summary Table.

Preset1 threshold map segment configuration register 12

Figure 115. P1_THR_12 Register

7	6	5	4	3	2	1	0
TH_P1_L10							
R/W-X							

Table 79. P1_THR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P1_L10	R/W	X	Preset1 Threshold L10 Level This bit-field powers-up un-initialized.

7.6.3.72 P1_THR_13 Register (Address = 6Ch) [reset = X]

P1_THR_13 is shown in Figure 116 and described in Table 80.

Return to Summary Table.

Preset1 threshold map segment configuration register 13

Figure 116. P1_THR_13 Register

7	6	5	4	3	2	1	0
TH_P1_L11							
R/W-X							

Table 80. P1_THR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P1_L11	R/W	X	Preset1 Threshold L11 Level This bit-field powers-up un-initialized.

7.6.3.73 P1_THR_14 Register (Address = 6Dh) [reset = X]

P1_THR_14 is shown in Figure 117 and described in Table 81.

Return to Summary Table.

Preset1 threshold map segment configuration register 14

Figure 117. P1_THR_14 Register

7	6	5	4	3	2	1	0
TH_P1_L12							
R/W-X							

Table 81. P1_THR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P1_L12	R/W	X	Preset1 Threshold L12 Level. This bit-field powers-up un-initialized.

7.6.3.74 P1_THR_15 Register (Address = 6Eh) [reset = X]

P1_THR_15 is shown in Figure 118 and described in Table 82.

Return to Summary Table.

Preset1 threshold map segment configuration register 15

Figure 118. P1_THR_15 Register

7	6	5	4	3	2	1	0
RESERVED				TH_P1_OFF			
R-X				R/W-X			

Table 82. P1_THR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	X	Reserved
3:0	TH_P1_OFF	R/W	X	Preset1 Threshold level Offset with values from 7 to -8 using signed magnitude representation with MSB as the sign bit This bit-field powers-up un-initialized.

7.6.3.75 P2_THR_0 Register (Address = 6Fh) [reset = X]

P2_THR_0 is shown in Figure 119 and described in Table 83.

Return to Summary Table.

Preset2 threshold map segment configuration register 0

Figure 119. P2_THR_0 Register

7	6	5	4	3	2	1	0
TH_P2_T1				TH_P2_T2			
R/W-X				R/W-X			

Table 83. P2_THR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T1	R/W	X	Preset2 Threshold T1 absolute time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T2	R/W	X	Preset2 Threshold T2 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.76 P2_THR_1 Register (Address = 70h) [reset = X]

P2_THR_1 is shown in Figure 120 and described in Table 84.

Return to Summary Table.

Preset2 threshold map segment configuration register 1

Figure 120. P2_THR_1 Register

7	6	5	4	3	2	1	0
TH_P2_T3				TH_P2_T4			
R/W-X				R/W-X			

Table 84. P2_THR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T3	R/W	X	Preset2 Threshold T3 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T4	R/W	X	Preset2 Threshold T4 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.77 P2_THR_2 Register (Address = 71h) [reset = X]

P2_THR_2 is shown in Figure 121 and described in Table 85.

Return to Summary Table.

Preset2 threshold map segment configuration register 2

Figure 121. P2_THR_2 Register

7	6	5	4	3	2	1	0
TH_P2_T5				TH_P2_T6			
R/W-X				R/W-X			

Table 85. P2_THR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T5	R/W	X	Preset2 Threshold T5 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T6	R/W	X	Preset2 Threshold T6 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.78 P2_THR_3 Register (Address = 72h) [reset = X]

P2_THR_3 is shown in Figure 122 and described in Table 86.

Return to Summary Table.

Preset2 threshold map segment configuration register 3

Figure 122. P2_THR_3 Register

7	6	5	4	3	2	1	0
TH_P2_T7				TH_P2_T8			
R/W-X				R/W-X			

Table 86. P2_THR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T7	R/W	X	Preset2 Threshold T7 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T8	R/W	X	Preset2 Threshold T8 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.79 P2_THR_4 Register (Address = 73h) [reset = X]

P2_THR_4 is shown in Figure 123 and described in Table 87.

Return to Summary Table.

Preset2 threshold map segment configuration register 4

Figure 123. P2_THR_4 Register

7	6	5	4	3	2	1	0
TH_P2_T9				TH_P2_T10			
R/W-X				R/W-X			

Table 87. P2_THR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T9	R/W	X	Preset2 Threshold T9 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T10	R/W	X	Preset2 Threshold T10 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.80 P2_THR_5 Register (Address = 74h) [reset = X]

P2_THR_5 is shown in Figure 124 and described in Table 88.

Return to Summary Table.

Preset2 threshold map segment configuration register 5

Figure 124. P2_THR_5 Register

7	6	5	4	3	2	1	0
TH_P2_T11				TH_P2_T12			
R/W-X				R/W-X			

Table 88. P2_THR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_T11	R/W	X	Preset2 Threshold T11 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.
3:0	TH_P2_T12	R/W	X	Preset2 Threshold T12 delta time: 0000b = 100 µs 0001b = 200 µs 0010b = 300 µs 0011b = 400 µs 0100b = 600 µs 0101b = 800 µs 0110b = 1000 µs 0111b = 1200 µs 1000b = 1400 µs 1001b = 2000 µs 1010b = 2400 µs 1011b = 3200 µs 1100b = 4000 µs 1101b = 5200 µs 1110b = 6400 µs 1111b = 8000 µs This bit-field powers-up un-initialized.

7.6.3.81 P2_THR_6 Register (Address = 75h) [reset = X]

P2_THR_6 is shown in Figure 125 and described in Table 89.

Return to Summary Table.

Preset2 threshold map segment configuration register 6

Figure 125. P2_THR_6 Register

7	6	5	4	3	2	1	0
TH_P2_L1					TH_P2_L2		
R/W-X					R/W-X		

Table 89. P2_THR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	TH_P2_L1	R/W	X	Preset2 Threshold L1 level This bit-field powers-up un-initialized.
2:0	TH_P2_L2	R/W	X	Preset2 Threshold L2 level (Bit4 to Bit2) This bit-field powers-up un-initialized.

7.6.3.82 P2_THR_7 Register (Address = 76h) [reset = X]

P2_THR_7 is shown in Figure 126 and described in Table 90.

Return to Summary Table.

Preset2 threshold map segment configuration register 7

Figure 126. P2_THR_7 Register

7	6	5	4	3	2	1	0
TH_P2_L2				TH_P2_L3			TH_P2_L4
R/W-X				R/W-X			R/W-X

Table 90. P2_THR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	TH_P2_L2	R/W	X	Preset2 Threshold L2 level (Bit1 to Bit0) This bit-field powers-up un-initialized.
5:1	TH_P2_L3	R/W	X	Preset2 Threshold L3 level This bit-field powers-up un-initialized.
0	TH_P2_L4	R/W	X	Preset2 Threshold L4 level (Bit4) This bit-field powers-up un-initialized.

7.6.3.83 P2_THR_8 Register (Address = 77h) [reset = X]

P2_THR_8 is shown in Figure 127 and described in Table 91.

Return to Summary Table.

Preset2 threshold map segment configuration register 8

Figure 127. P2_THR_8 Register

7	6	5	4	3	2	1	0
TH_P2_L4				TH_P2_L5			
R/W-X				R/W-X			

Table 91. P2_THR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	TH_P2_L4	R/W	X	Preset2 Threshold L4 level (Bit3 to Bit0) This bit-field powers-up un-initialized.
3:0	TH_P2_L5	R/W	X	Preset2 Threshold L5 level (Bit4 to Bit1) This bit-field powers-up un-initialized.

7.6.3.84 P2_THR_9 Register (Address = 78h) [reset = X]

P2_THR_9 is shown in Figure 128 and described in Table 92.

Return to Summary Table.

Preset2 threshold map segment configuration register 9

Figure 128. P2_THR_9 Register

7	6	5	4	3	2	1	0
TH_P2_L5				TH_P2_L6			TH_P2_L7
R/W-X				R/W-X			R/W-X

Table 92. P2_THR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TH_P2_L5	R/W	X	Preset2 Threshold L5 level (Bit0) This bit-field powers-up un-initialized.
6:2	TH_P2_L6	R/W	X	Preset2 Threshold L6 level This bit-field powers-up un-initialized.
1:0	TH_P2_L7	R/W	X	Preset2 Threshold L7 level (Bit4 to Bit3) This bit-field powers-up un-initialized.

7.6.3.85 P2_THR_10 Register (Address = 79h) [reset = X]

P2_THR_10 is shown in Figure 129 and described in Table 93.

Return to Summary Table.

Preset2 threshold map segment configuration register 10

Figure 129. P2_THR_10 Register

7	6	5	4	3	2	1	0
TH_P2_L7			TH_P2_L8				
R/W-X			R/W-X				

Table 93. P2_THR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TH_P2_L7	R/W	X	Preset2 Threshold L7 level (Bit2 to Bit0) This bit-field powers-up un-initialized.
4:0	TH_P2_L8	R/W	X	Preset2 Threshold L8 level This bit-field powers-up un-initialized.

7.6.3.86 P2_THR_11 Register (Address = 7Ah) [reset = X]

P2_THR_11 is shown in Figure 130 and described in Table 94.

Return to Summary Table.

Preset2 threshold map segment configuration register 11

Figure 130. P2_THR_11 Register

7	6	5	4	3	2	1	0
TH_P2_L9							
R/W-X							

Table 94. P2_THR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P2_L9	R/W	X	Preset2 Threshold L9 level This bit-field powers-up un-initialized.

7.6.3.87 P2_THR_12 Register (Address = 7Bh) [reset = X]

P2_THR_12 is shown in Figure 131 and described in Table 95.

Return to Summary Table.

Preset2 threshold map segment configuration register 12

Figure 131. P2_THR_12 Register

7	6	5	4	3	2	1	0
TH_P2_L10							
R/W-X							

Table 95. P2_THR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P2_L10	R/W	X	Preset2 Threshold L10 Level This bit-field powers-up un-initialized.

7.6.3.88 P2_THR_13 Register (Address = 7Ch) [reset = X]

P2_THR_13 is shown in Figure 132 and described in Table 96.

Return to Summary Table.

Preset2 threshold map segment configuration register 13

Figure 132. P2_THR_13 Register

7	6	5	4	3	2	1	0
TH_P2_L11							
R/W-X							

Table 96. P2_THR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P2_L11	R/W	X	Preset2 Threshold L11 Level This bit-field powers-up un-initialized.

7.6.3.89 P2_THR_14 Register (Address = 7Dh) [reset = X]

P2_THR_14 is shown in Figure 133 and described in Table 97.

Return to Summary Table.

Preset2 threshold map segment configuration register 14

Figure 133. P2_THR_14 Register

7	6	5	4	3	2	1	0
TH_P2_L12							
R/W-X							

Table 97. P2_THR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TH_P2_L12	R/W	X	Preset2 Threshold L12 Level This bit-field powers-up un-initialized.

7.6.3.90 P2_THR_15 Register (Address = 7Eh) [reset = X]

P2_THR_15 is shown in Figure 134 and described in Table 98.

Return to Summary Table.

Preset2 threshold map segment configuration register 15

Figure 134. P2_THR_15 Register

7	6	5	4	3	2	1	0
RESERVED				TH_P2_OFF			
R-X				R/W-X			

Table 98. P2_THR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	X	Reserved
3:0	TH_P2_OFF	R/W	X	Preset2 Threshold level Offset with values from 7 to -8 using signed magnitude representation with MSB as the sign bit This bit-field powers-up un-initialized.

7.6.3.91 THR_CRC Register (Address = 7Fh) [reset = X]

THR_CRC is shown in Figure 135 and described in Table 99.

Return to Summary Table.

Threshold map configuration registers data CRC register

Figure 135. THR_CRC Register

7	6	5	4	3	2	1	0
THR_CRC							
R/W-X							

Table 99. THR_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THR_CRC	R/W	X	Threshold map configuration registers data CRC value: This read-only register is updated whenever a threshold map configuration register gets updated This bit-field powers-up un-initialized.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PGA460 device must be paired with an external transducer. The PGA460 device drives the transducer, and then filters and processes the returned echo signal sensed by the transducer. The transducer should be chosen based on the resonant frequency, input voltage requirements, sensitivity, beam pattern, and decay time. The PGA460 device meets most transducer requirements by adjusting the driving frequency, driving current limit, band-pass filtering coefficients, and low-pass filtering coefficients. The external transformer or p-channel MOSFET should be chosen to meet the input voltage requirements of the transducer and have a saturation current rated equal to or greater than the configured driving current limit of the PGA460 device. The interface options include USART, TCI, and one-wire UART. After the burst-and-listen cycle is complete, the PGA460 device can be called to return the distance, amplitude, and width of the echo through a communication interface.

8.1.1 Transducer Types

The driver mode is dependant on the transducer type. Two types of transducers are available for open-air ultrasonic measurements. Closed-top transducers are transducers which hermetically seal the piezoelectric membrane from exposure to air or destructive particles. Closed-top transducer are favorable in applications that are subject to harsh environmental conditions, such as exposure to outdoor elements, extreme temperature changes, and debris. As a result of the additional protection offered by closed-top transducers, a transformer-driven method is typically required to maximize distance performance.

Open-top transducers are transducers with vents or slots that expose the piezoelectric membrane to the air. Open-top transducers are favorable for controlled indoor applications to minimize the risk of the transducer becoming damaged. Open-top transducers do not require as much driving voltage as closed-top transducers to achieve maximum distance performance; therefore, a transformer is not necessary. For low-voltage driven transducers, such as open-tops, a direct-drive (or bridge-drive) method can be used as an alternative to a transformer. The direct-driven method can work on certain closed-top transducers, but the maximum achievable distance will be reduced.

8.2 Typical Applications

In all typical applications, the PGA460 must be paired with at least one external transducer for generating an ultrasonic echo to transmit through air and to detect the reflected echo returning from an object. The tasks of transmitting and receiving the echo can be separated into independent transducers for improved performance. In this case, the application must only detect ultrasonic echoes, no external driver components (transformer or p-channel MOSFET) are required.

Typical Applications (continued)

8.2.1 Transformer-Driven Method

Figure 136 shows the transformer-driven method schematic for a single transducer.

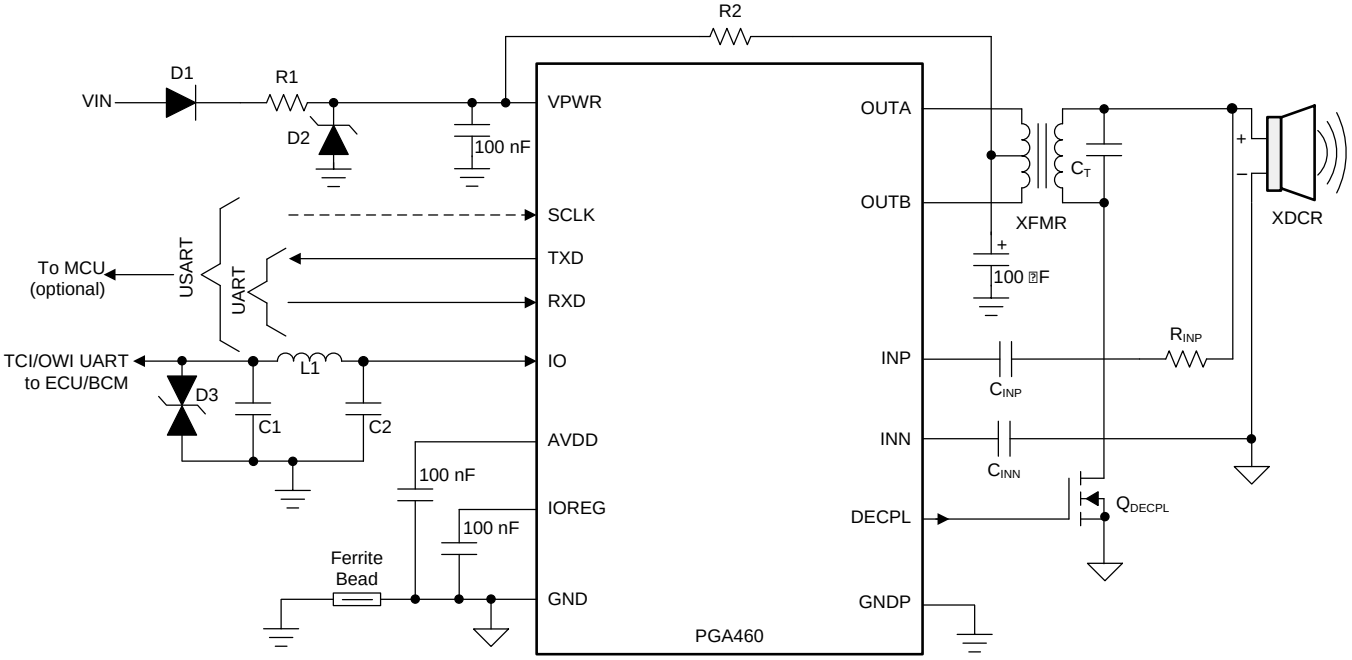


Figure 136. Transformer-Driven Method Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 100 as the input parameters.

Table 100. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 to 18 V
Input voltage recommended	7.4 V
Transformer turns ratio	(1-2) : (2-3) : (4-6) = 1:1:8.42
Transformer driving current rating	500 mA
Transformer main voltage (4-6) rating	200 V_{AC}
Transducer driving voltage	120 V_{PP}
Transducer frequency	58.5 kHz
Transducer pulse count	20

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Transducer
  - Transducer driving voltage
  - Transducer resonant frequency
  - Transducer pulse count
- Driver
  - Transformer turns ratio
  - Transformer saturation current
  - Transformer main voltage (4-6) rating

Table 101 lists the recommended component values for typical applications.

Table 101. Recommended Component Values for Typical Applications

DESIGNATOR	VALUE	COMMENT
R1	10 Ω (1/2 Watt)	Optional (noise reduction)
R2	100 Ω(1/2 Watt)	Optional (limit in-rush current)
$R_{(INP)}$	3 kΩ (1/4 Watt)	Optional (transformer drive only. For EMI/ESD robustness)
L1	100 nH	Optional (transient suppression)
C1	100 nF	Optional (Transient suppression)
C2	100 nF	Optional (transient suppression)
$C_{(INP)}$	$C_{(INP)} = \frac{21.22 \times 10^{-6}}{f_{(TRANSDUCER)}}$	
$C_{(INN)}$	$C_{(INN)} = \frac{0.0024}{f_{(TRANSDUCER)}}$	
C_T		Value depends on transducer and transformer used
D1	1N4007 or equivalent	Schottky diode recommended
D2	V_Z < 30 V	Optional (transient suppression)
D3	V_{BR} < 30 V	Optional (transient suppression)
XDCR		Example devices for low-frequency range: Closed top for transformer driven: muRata MA58MF14-7N, SensComp 40KPT25 Open top for direct driven: muRata MA40H1S-R, SensComp 40LPT16, Kobitone 255-400PT160-ROX
XFMR		Example devices: TDK EPCOS B78416A2232A003, muRata-Toko N1342DEA-0008BQE=P3, Mitsumi K5-R4
Q_{DECPL}		Optional (time or temperature decoupling FET) If no decoupling FET is used, ground the XFMR and CT
Q1		Can be FETs or BJTs as discrete implementation or transistor-array package. Example devices: Example devices: FDN358P Single FET, MUN5114 single BJT
Ferrite bead	BK215HS102-T or equivalent	Optional (noise reduction)). Can be substituted with 0-Ω short.

8.2.1.2.1 Transducer Driving Voltage

When a voltage is applied to piezoelectric ceramics, mechanical distortion is generated according to the voltage and frequency. The mechanical distortion is measured in units of sound pressure level (SPL) to indicate the volume of sound, and can be derived from a free-field microphone voltage measurement using Equation 9.

$$\text{SPL (db)} = 20 \times \log \frac{\left(\frac{V_{(MIC)}}{3.4\ \text{mV}} \right)}{P_O} \quad (9)$$

where

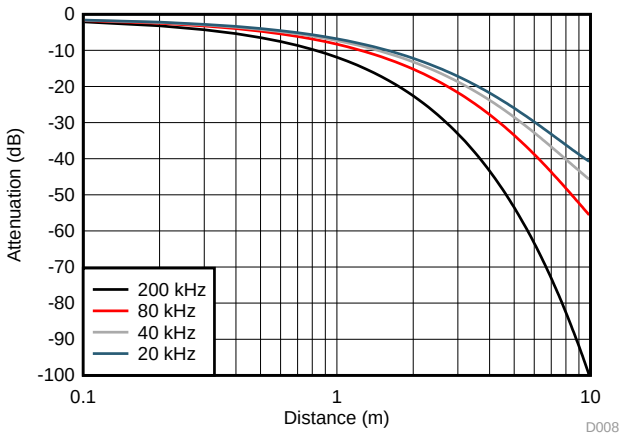
- $V_{(MIC)}$ is the measured sensor sound pressure (mV_{RMS}).
- P_O is a referenced sound pressure of 20 μPa.

The SPL does not increase indefinitely with the driving voltage. After a particular driving voltage, the amount of SPL that a transducer can generate becomes saturated. A transducer is given a maximum driving voltage specification to indicate when the maximum SPL is generated. Driving the transducer beyond the maximum driving voltage makes the ultrasonic module less power-efficient and can damage or decrease the life expectancy of the transducer.

For the detailed procedure on measuring the SPL of a transducer, refer to *PGA460 Ultrasonic Module Hardware and Software Optimization*.

8.2.1.2.2 Transducer Driving Frequency

The strength of ultrasonic waves propagated into the air attenuate proportionally with distance. This attenuation is caused by diffusion, diffraction, and absorption loss as the ultrasonic energy transmits through the medium of air. As shown in Figure 137, the higher the frequency of the ultrasonic wave, the larger the attenuation rate and the shorter the distance the wave reaches.



t = 20 °C

Figure 137. Attenuation Characteristics of Sound Pressure by Distance

An ultrasonic transducer has a fixed resonant center frequency with a typical tolerance of ±2%. The lower frequency range of 30 to 80 kHz is the default operating range for common automotive and consumer applications for a step resolution of 1 cm and typical range of 30 cm to 5m. The upper frequency range of 180 to 480 kHz is reserved for high-precision industrial applications with a step resolution of 1 mm and a typical range of 5 cm to 1 m.

8.2.1.2.3 Transducer Pulse Count

The pulse count determines how many alternating periods are applied to the transducer by the complementary low-side drivers and determines the total width of the ultrasonic ping that was transmitted. The larger the width of the transmitted ping, the larger the width of the returned echo signature of the reflected surface and the more resolution available to set a stable threshold. A disadvantage of a large pulse count is a large ringing-decay period, which limits how detectable objects are at short distances.

Select a pulse count based on the minimum object distance requirement. If short-distance object detection is not a priority, a high pulse count is not a concern. Certain transducers can be driven continuously while others have a limit to the maximum driving-pulse count. Refer to the specification for the selected transducer to determine if the pulse count must be limited.

8.2.1.2.4 Transformer Turns Ratio

A center-tap transformer is typically paired with the transducer to convert a DC voltage to a high-sinusoidal AC voltage. The center tap is a contact made to a point halfway along the primary winding of the transformer. The center tap is supplied with the DC voltage that is then multiplied on the secondary side based on the turns ratio of the transformer. Figure 138 shows the typical pinout of a center-tap transformer where pin 2 is the center tap, pins 1 and 3 are connected to OUTB and OUTA, pin 4 is connected to the positive terminal of the transducer, and pin 6 is connected to ground.

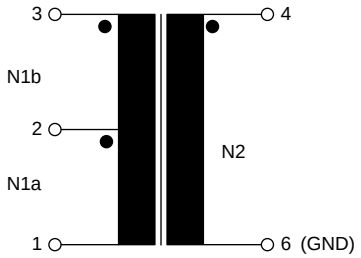


Figure 138. Typical Pinout of Center-Tap Transformer for Ultrasonic Transducers

Two modes to generate the transducer voltage using the center tap transformer are available. These modes are defined as follows:

Push-pull In this mode, the two internal low-side switches of the PGA460 device are used to turn current on and off in two primary coils of the center-tap transformer.

The primary coils have the same number of turns. The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The direction of current in the primary coils generates voltages of opposite polarity in the secondary coils which effectively doubles the peak-to-peak voltage in the secondary coil.

Single-ended In this mode, one low-side switch is used to turn current on and off in the primary of the transformer.

The rate of change of current in the primary coil generates a voltage in the secondary coil of the transformer, which is connected to the transducer. The center tap of the transformer is not required for this mode, and can be left floating. Instead, the reference voltage is connected to an outermost primary-side terminal (pin 3) and either OUTA or OUTB is connected to the other primary-side terminal (pin1).

8.2.1.2.5 Transformer Saturation Current and Main Voltage Rating

Leakage inductance is caused when magnetic flux is not completely coupled between windings in a transformer. Magnetic saturation of a transformer core can be caused by excessive primary voltage, operation at too low of a frequency, by the presence of a DC current in any of the windings, or a combination of these causes. The PGA460 device can limit the primary-side driver current of the transformer internally from 50 to 500 mA. The center-tap voltage is typically referenced to the VPWR voltage. However, if the VPWR voltage is too high of a voltage on the center tap of the primary side, then the voltage must be down-regulated. If the VPWR is too low, then the voltage must be up-regulated.

8.2.1.3 Application Curves

Components used: TDK EPCOS B78416A2232A003 Transformer, muRata MA58MF14-7N transducer. To minimize the ranging of the TDK EPCOS B78416A2232A003 transformer and muRata MA58MF14-7N transducer combination, place a 680pF tuning capacitor (C_T) and 10kΩ damping resistor (R_{Damp}) in parallel to the transducer. This will enable sub-15cm ranging depending on the pulse count, center-tap voltage, and driver current limit.

Data shown in Figure 139 and Figure 140 was recorded using the echo dump feature of the PGA460 device (see the *Echo Data Dump* section)

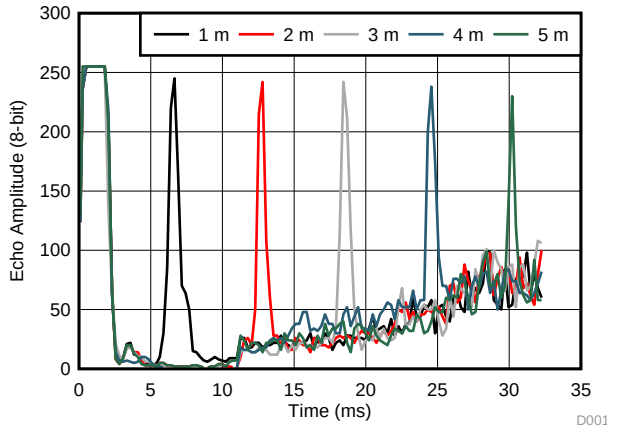


Figure 139. Long Range ISO-Pole Measurements Using Transformer Drive

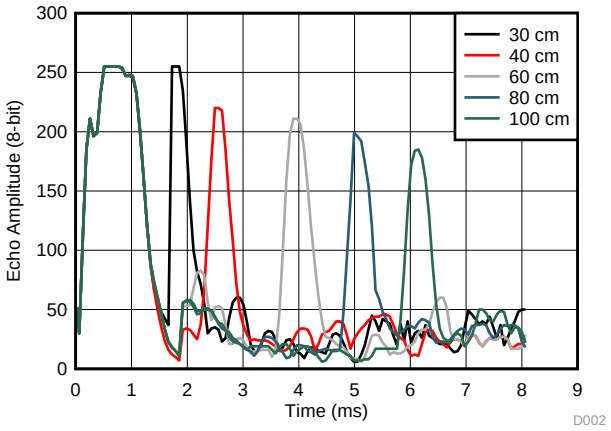


Figure 140. Short Range ISO-Pole Measurements Using Transformer Drive

8.2.2 Direct-Driven (Transformer-Less) Method

The direct-driven method substitutes the traditional center-tap transformer with a bridge driver, and is suitable for plastic-shelled open-top transducers. Any open or closed top transducer can be driven directly, but the maximum amount of SPL may not be generated during transmission. The direct-driven configuration uses either a half-bridge or full-bridge gate driver to generate an alternating square wave to drive the transducer. By default, the half-bridge driver configuration is enabled to allow the use of a single transducer to transmit and receive. The PGA460 device cannot drive a single transducer in the full-bridge configuration without the addition of external components (beyond the scope of this document).. Because the low-side drivers are integrated into the PGA460 device, only one external high-side p-channel MOSFET is required. In the half-bridge configuration, one OUTx channel is used to drive the p-channel MOSFET, while the other is used to directly excite the transducer.. Figure 141 shows the direct-driven method schematic for a single transducer.

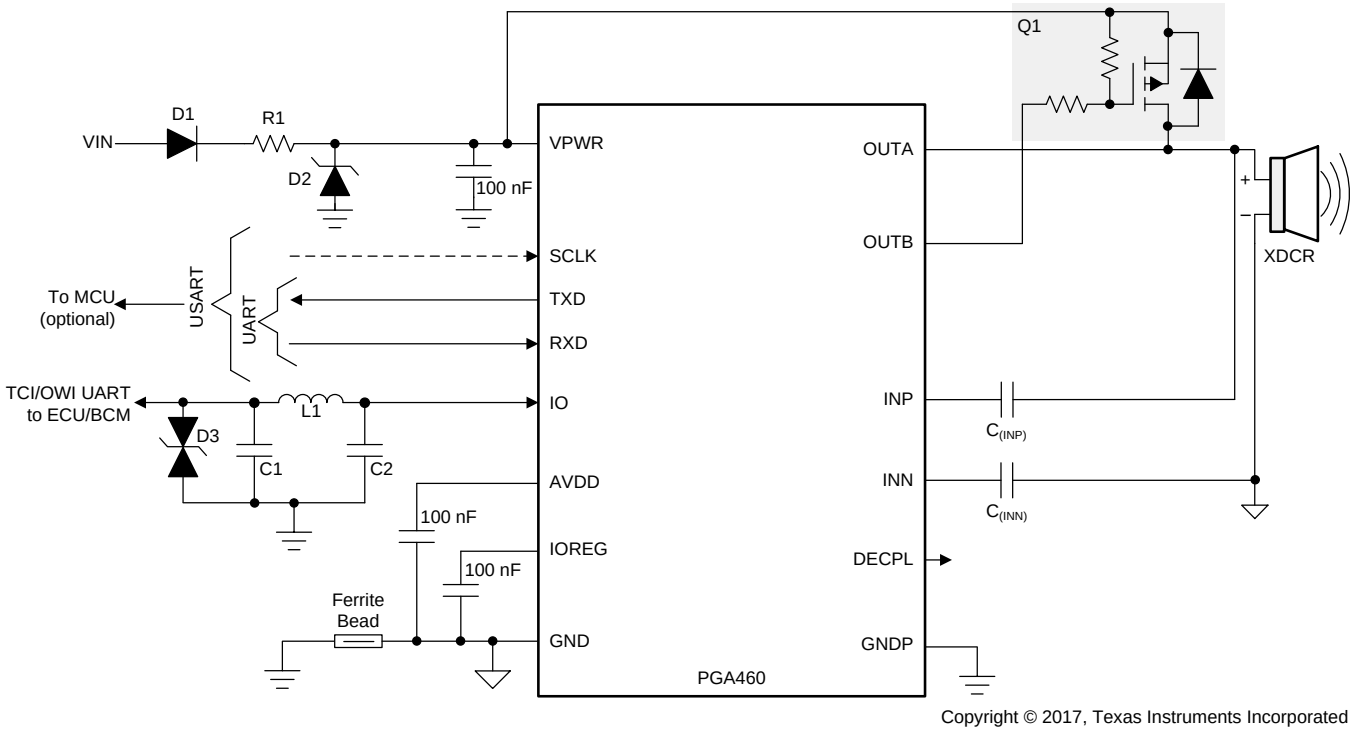


Figure 141. Direct-Driven Method Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 102 as the input parameters.

Table 102. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 to 7.2 V
Input voltage recommended	7.2 V
Transducer driving voltage	7.2 V_{PP}
Transducer frequency	40 kHz
Transducer pulse count	20

8.2.2.2 Detailed Design Procedure

For recommended component values in typical applications, see Table 101.

8.2.2.3 Application Curves

Components used: Fairchild FDC6506P p-channel MOSFET, muRata MA40H1S-R transducer

Data shown in Figure 139 and Figure 140 was recorded using the echo dump feature of the PGA460 device (see the *Echo Data Dump* section)

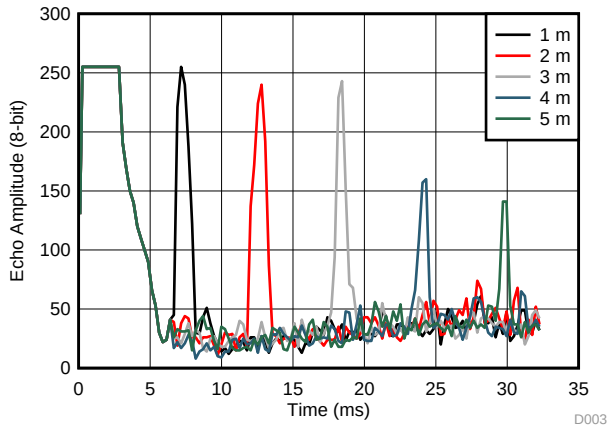


Figure 142. Long Range ISO-Pole Measurements Using Direct Drive

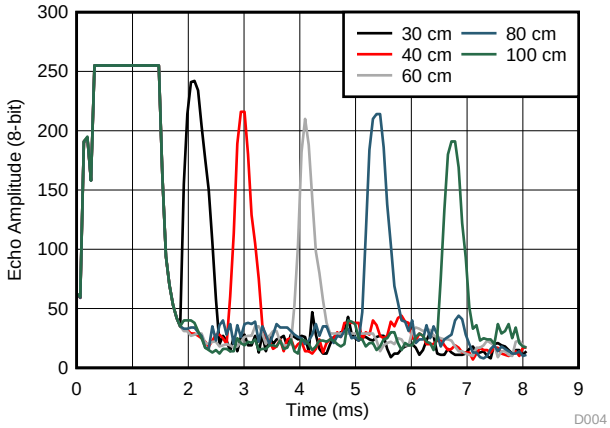


Figure 143. Short Range ISO-Pole Measurements Using Direct Drive

9 Power Supply Recommendations

The PGA460 device is designed to operate from an input voltage supply range from 6 V to 28 V. If the input supply is located more than a few inches from the PGA460 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

The electrolytic capacitor at the VPWR pin is intended to act as a fast discharge capacitor during the bursting stage of the PGA460 device. The center-tap transformer can be supplied with a center-tap voltage that is different than what is supplied to the VPWR pin, but must remain within specified maximum voltage rating of the OUTA and OUTB outputs. No electrolytic capacitor is required for the direct-driven method, although it is recommended for reference voltage stability, and can be less than 100 µF.

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to a accomplish a small-form factor ultrasonic module design. The layers should be separated by analog and digital signals. The pin map of the device is routed such that the power and digital signals are on the opposing side of the analog driver and receiver pins. Consider the following best practices for PGA460 device layout in order of descending priority:

- Separating the grounding types is important to reduce noise at the AFE input of the PGA460. In particular, the transducer sensor ground, supporting driver, and return-path circuitry should have a separate ground before being connected to the main ground. Separating the sensor and main grounds through a ferrite bead is best practice, but not required; a copper-trace or 0-Ω short is also acceptable when bridging grounds.
- The analog return path pins, INP and INN, are most susceptible to noise and therefore should be routed as short and directly to the transducer as possible. Ensure the INN capacitor is close to the pin to reduce the length of the ground wire.
- In applications where protection from an ESD strike on the case of the transducer is important, ground routing of the capacitor on the INN pin should be separate from the device ground and connected directly with the shortest possible trace to the connector ground.
- The analog drive pins can be high-current, high-voltage, or both and therefore the design limitation of the OUTA and OUTB pins is based on the copper trace profile. The driver pins are recommended to be as short and direct as possible when using a transformer, and driving the primary windings with a high-current limit
- The decoupling capacitors for the AVDD, IOREG, and VPWR pins should be placed as close to the pins as possible
- Any digital communication should be routed away from the analog receiver pins. The IO, TXD, RXD, and SCLK pins should be routed on the opposite side of the PCB, away from of the analog signals. When the IO pin is referenced to a high-voltage VPWR, and operating at a high-speed baud rate, the trace to the connector or master should be as direct as possible

10.2 Layout Example

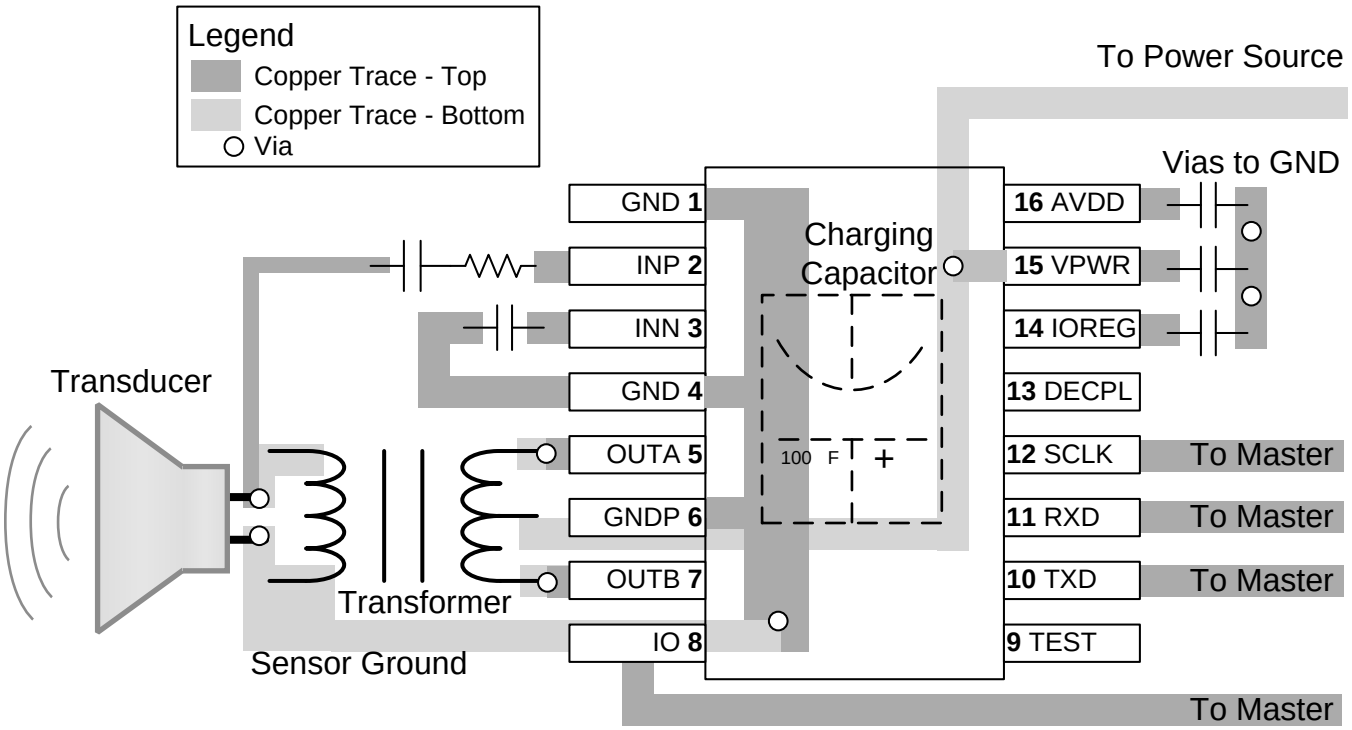


Figure 144. PGA460 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PGA460 Frequently Asked Questions (FAQ) and EVM Troubleshooting Guide* (SLAA733)
- *PGA460 Software Development Guide* (SLAA730)
- *PGA460 Ultrasonic Module Hardware and Software Optimization* (SLAA732)
- *PGA460-Q1 EVM Quick Start Guide* (SLVUB17)
- *PGA460-Q1 EVM User's Guide* (SLAU659)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA460TPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PGA460	Samples
PGA460TPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PGA460	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF PGA460 :

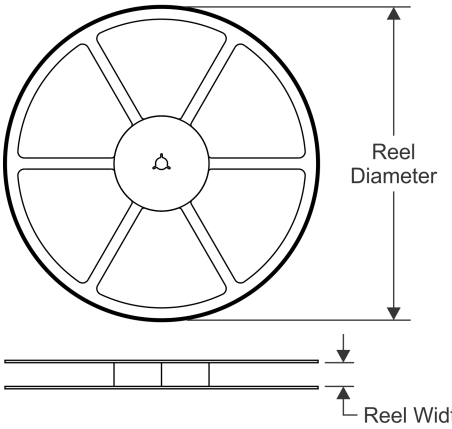
- Automotive: PGA460-Q1

NOTE: Qualified Version Definitions:

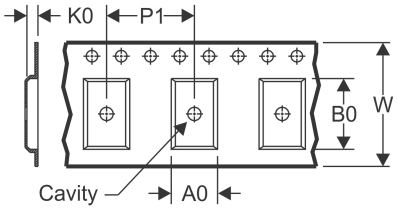
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

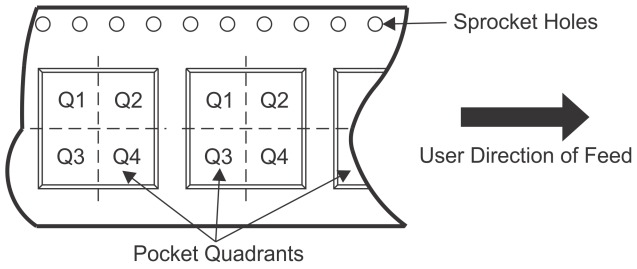


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

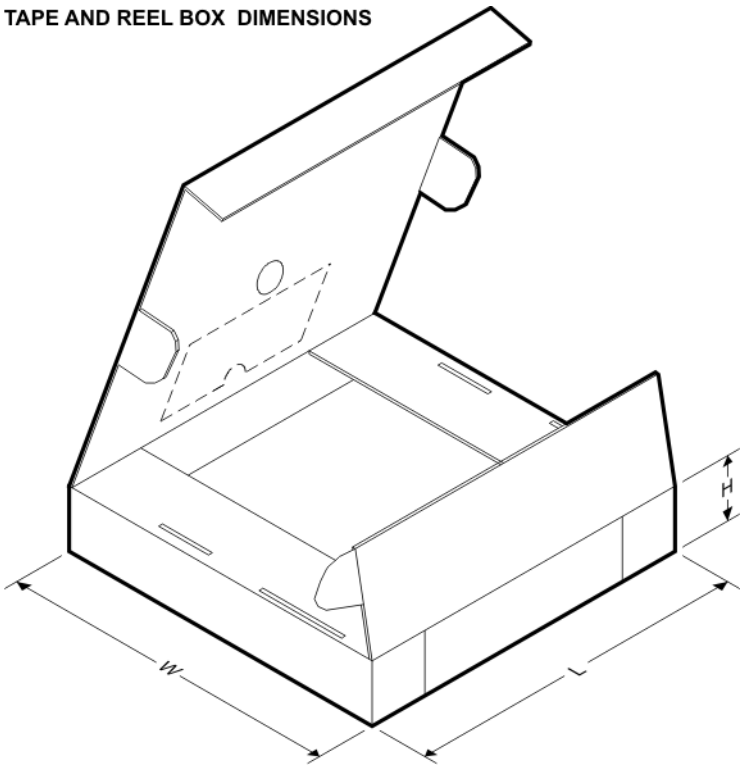
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA460TPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

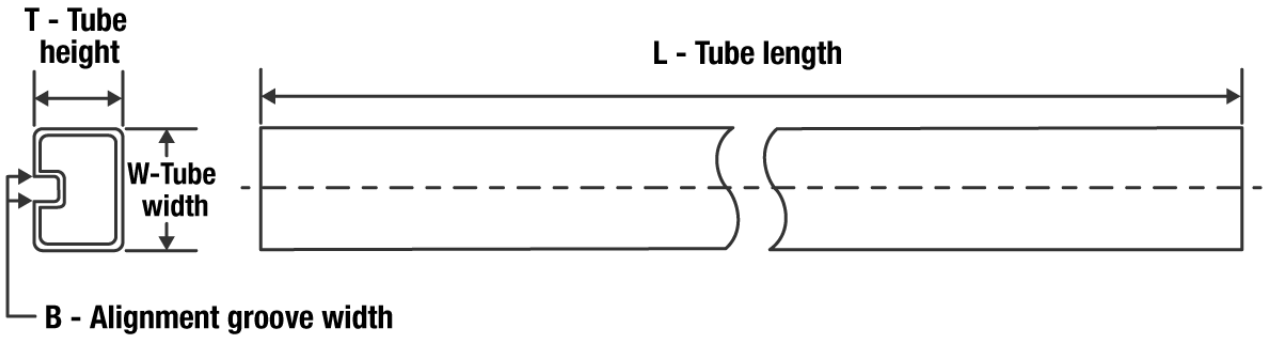
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA460TPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

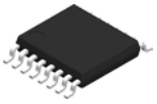
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA460TPW	PW	TSSOP	16	90	530	10.2	3600	3.5

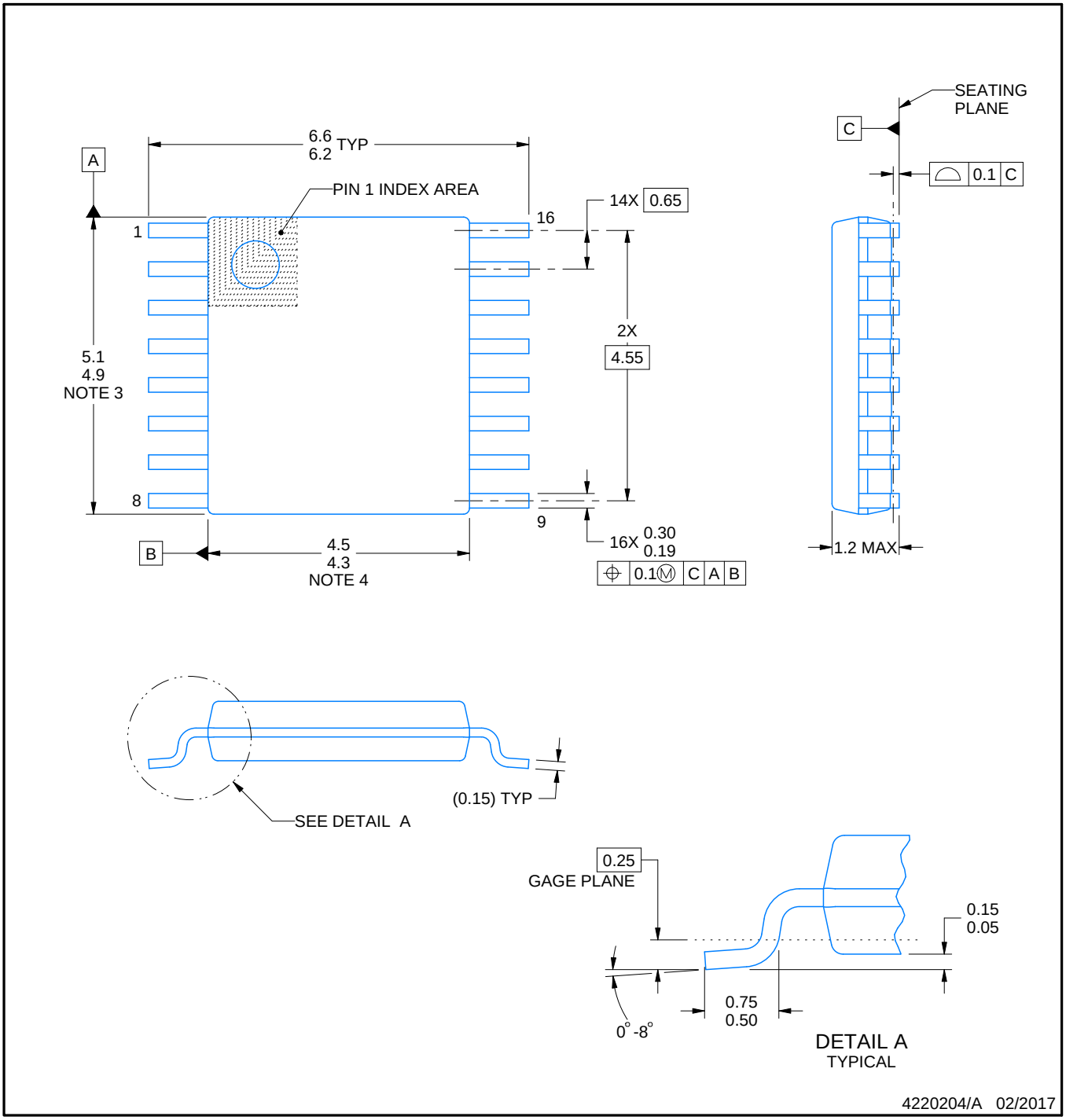
PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

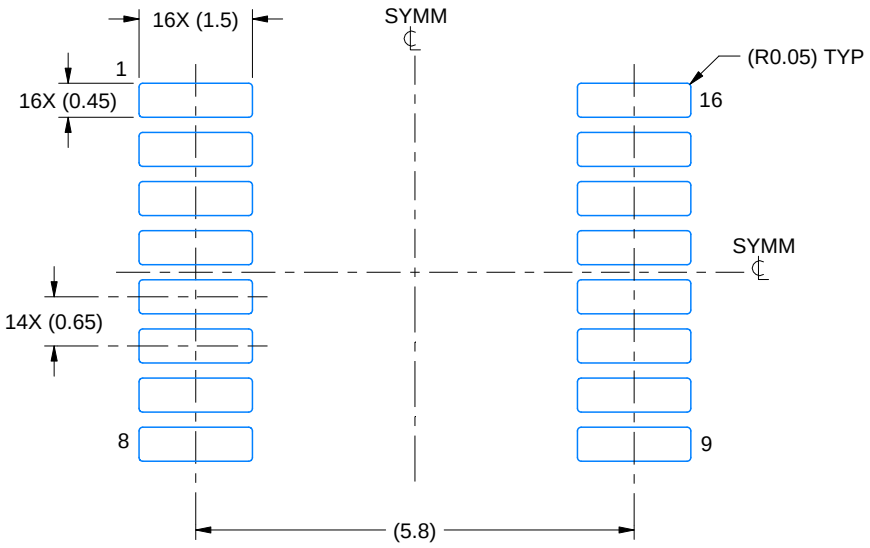
SMALL OUTLINE PACKAGE





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



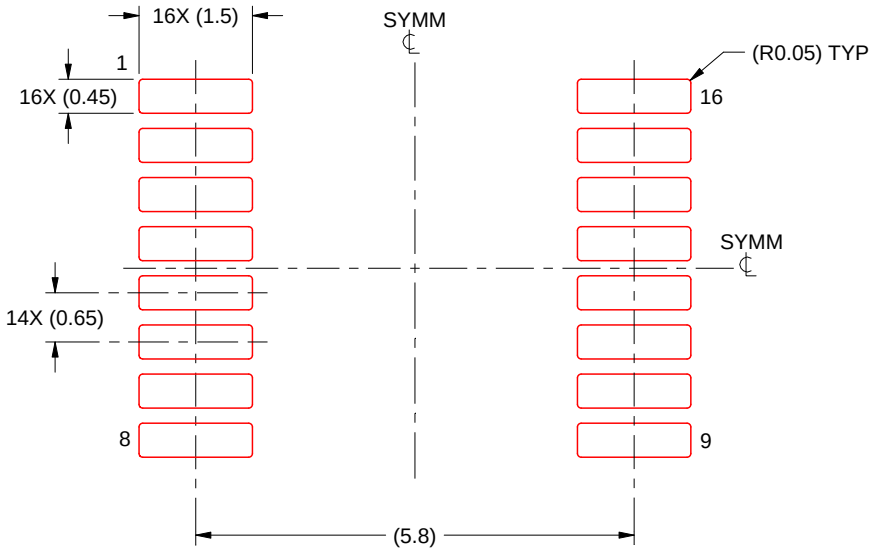
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SN65HVD64 AISG® On and Off Keying Coax Modem Transceiver

1 Features

- 3-V to 5.5-V Supply Range
- 1.6-V to 5.5-V Independent Logic Supply
- –15-dBm to +5-dBm Wide-Input Dynamic Range for Receiver
- 0-dBm to 6-dBm Adjustable Power Delivered by the Driver to the Coax
- Supports AISG® V2.0 and V3.0
- Low-Power Standby Mode
- Direction Control Output for RS-485 Bus Arbitration
- Up to 115 kbps of Signaling Support
- 2.176-MHz Center Frequency for Integrated Active Bandpass Filter
- Supports -40 °C to 120 °C Ambient Temperatures
- 3-mm × 3-mm 16-Pin VQFN Package

2 Applications

- AISG – Interface for Antenna Line Devices
- Tower-Mounted Amplifiers (TMA)
- General Modem Interfaces

3 Description

The SN65HVD64 transceiver modulates and demodulates signals between a logic (baseband) interface and a frequency suitable for long coaxial media, to facilitate wired data transfer among radio equipment.

The SN65HVD64 device is an integrated AISG transceiver designed to meet the requirements of the Antenna Interface Standards Group v2.0 and v3.0 specification.

The SN65HVD64 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176-MHz center frequency.

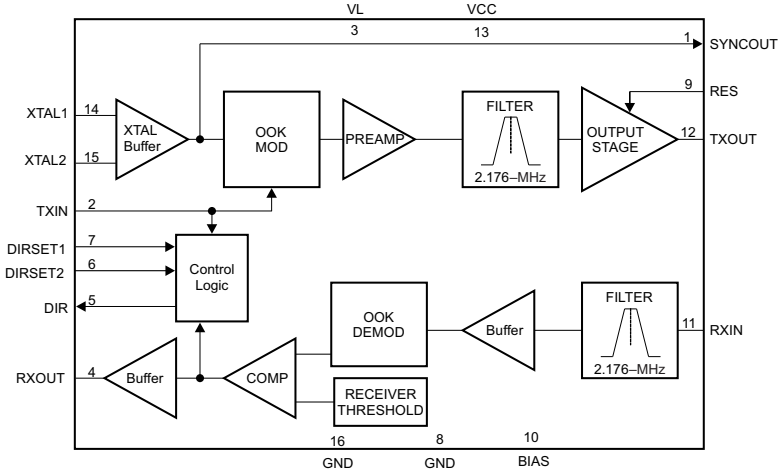
The transmitter supports adjustable output power levels from 0 dBm to 6 dBm delivered to the 50-Ω coax cable. The SN65HVD64 transmitter is compliant with the spectrum emission requirement provided by the AISG standard.

A direction control output facilitates bus arbitration for an RS-485 interface. This device integrates an oscillator input for a crystal, and also accepts standard clock inputs to the oscillator.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65HVD64	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram

Table of Contents

4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release.

5 Pin Configuration and Functions

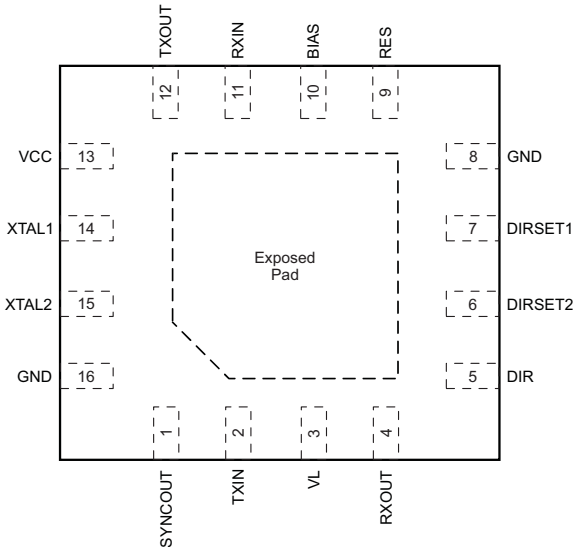


Figure 5-1. RGT Package, 16-Pin VQFN, Top View

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
BIAS	10	O	Bias voltage output for setting driver output power by external resistors
DIR	5	O	Direction control output signal for bus arbitration
DIRSET1	7	—	DIRSET1 and DIRSET2: Bits to set the duration of DIR DIRSET[2:1]: [L:L] = 9.6 kbps; [L:H] = 38.4 kbps; [H:L] = 115 kbps; [H:H] = standby mode
DIRSET2	6	—	
GND	8	—	Ground
	16		
RES	9	P	Input voltage to adjust driver output power that is set by external resistors from BIAS pin to GND
RXIN	11	I	Modulated input signal to the receiver
RXOUT	4	O	Digital data bit stream from receiver
SYNCOUT	1	O	Open-drain output to synchronize other devices to the 4x-carrier oscillator at XTAL1 and XTAL2
TXIN	2	I	Digital data bit stream to driver
TXOUT	12	O	Modulated output signal from the driver
V_{CC}	13	P	Analog supply voltage for the device
VL	3	P	Logic supply voltage for the device
XTAL1	14	I/O	I/O pins of the crystal oscillator. Connect a 4 × f_C crystal between these pins or connect XTAL1 to an 8.704-MHz clock and connect XTAL2 to GND.
XTAL2	15		
EP	—	—	Exposed pad. Connection to ground plane is recommended for best thermal conduction.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} and VL	–0.5	6	V
Voltage at coax pins	–0.5	6	V
Voltage at logic pins	–0.3	V_{VL} + 0.3	V
Logic output current	–20	20	mA
TXOUT output current	Internally limited		
SYNCOUT output current	Internally limited		
Junction temperature, T_J		170	°C
Continuous total power dissipation	See the *Thermal Information*		°C
Storage temperature, T_{stg} (2)	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Applicable before the device is installed in the final product.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		3		5.5	V
V_L	Logic supply voltage		1.6		5.5	V
$V_{I(pp)}$	Input signal amplitude at RXIN				1.12	Vpp
V_{IH}	High-level input voltage	TXIN, DIRSET1, DIRSET2	70%V_L		V_L	V
		XTAL1, XTAL2	70%V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage	TXIN, DIRSET1, DIRSET2	0		30%V_L	V
		XTAL1, XTAL2	0		30%V_{CC}	
$1/t_{UI}$	Data signaling rate		9.6		115	kbps
F_{OSC}	Oscillator frequency		–30 ppm	8.704	30 ppm	MHz
Z_{LOAD}	Load impedance between TXOUT to RXIN			50		Ω
	Load impedance between RXIN and GND at f_C (channel)			50		Ω
R1	Bias resistor between BIAS and RES			4.1		kΩ
R2	Bias resistor between RES and GND			10		kΩ
R_{SYNC}	Pullup resistor between SYNCOUT and V_{CC}			1		kΩ
V_{RES}	Voltage at RES pin		0.7		1.5	V
C_C	Coupling capacitance between RXIN and coax (channel)			220		nF
C_{BIAS}	Capacitance between BIAS and GND			1		µF
T_A	Operating free-air temperature		–40		120	°C
T_J	Junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		VQFN RGT 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	64.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.9	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	25	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{CC}	Supply current	DIRSET1 = L DIRSET2 = H	TXIN = L (active)		28	33	mA
			TXIN = H (quiescent)		25	31	
			TXIN = 115 kbps, 50% duty cycle		27	33	
		DIRSET1 = H, DIRSET2 = H (standby)			12	17	
I_{VL}	Logic supply current	TXIN = H, RXIN = DC input				50	µA
PSRR	Receiver power supply rejection ratio	$V_{TXIN} = V_L$		45	60		dB
T_{SD_RISE}	Thermal shutdown rising			143	156	170	°C
T_{SD_FALL}	Thermal shutdown falling			123	136	147	°C
T_{SD_HYS}	Thermal shutdown hysteresis			18	20	23	°C
LOGIC PINS							
V_{OH}	High-level logic output voltage (RXOUT, DIR)	I_{OH} = –4 mA for V_L > 2.4 V, I_{OH} = –2 mA for V_L < 2.4 V		90%V_{VL}			V
V_{OL}	Low-level logic output voltage (RXOUT, DIR)	I_{OL} = 4 mA for V_L > 2.4 V, I_{OL} = 2 mA for V_L < 2.4 V				10%V_{VL}	V
COAX DRIVER							
$V_{O(PP)}$	Peak-to-peak output voltage at device pin TXOUT (see Figure 7-1)	V_{RES} = 1.5 V (Maximum setting)		2.24	2.5		V_{PP}
		V_{RES} = 0.7 V (Minimum setting)			1.17	1.3	
$V_{O(PP)}$	Peak-to-peak voltage at coax out (see Figure 7-1)	V_{RES} = 1.5 V		5	6		dBm
		V_{RES} = 0.7 V			–0.6	0.3	
$V_{O(OFF)}$	Off-state output voltage	At TXOUT				1	mVpp
		At coax out				–60	dBm
	Output emissions	Coupled to coaxial cable with characteristic impedance of 50 Ω, as shown in Figure 6-1 (1) (2)					N/A
f_O	Output frequency				2.176		MHz
Δf	Output frequency variation			–100		100	ppm
Z_O	Output impedance	At 100 kHz			0.03		Ω
		At 10 MHz			3.5		
$\lvert I_{OS} \rvert$	Short-circuit output current	TXOUT is also protected by a thermal shutdown circuit during short-circuit faults			300	450	mA
COAX RECEIVER							
V_{IT}	Input threshold	f_{IN} = 2.176 MHz		79	112	158	mVPP
				–18	–15	–12	dBm
Z_{IN}	Input impedance	$f = f_O$		11	21		kΩ
RECEIVER FILTER							
f_{PB}	Passband	VRXIN = 1.12VP_P		1.1		4.17	MHz
f_{REJ}	Receiver rejection range	2.176-MHz carrier amplitude of 112.4 mV_{PP}, frequency band of spurious components with 800 mVPP allowed.		1.1		4.17	MHz
$t_{noise\ filter}$	Receiver noise filter time (slow bit rate)	DIRSET for 9.6 kbps			4		µs
	Receiver noise filter time (fast bit rate)	DIRSET for > 9.6 kbps			2		µs
XTAL AND SYNC							
I_I	Input leakage current	XTAL1, XTAL2, 0V < V_{IN} < V_{CC}		–15		15	µA
V_{OL}	Output low voltage	SYNCOUT, with 1-kΩ resistor from SYNCOUT to V_{CC}				0.4	V

(1) Specified by design with a recommended 470-pF capacitor between RXIN and GND. Measurements above 150 MHz are determined by setup.

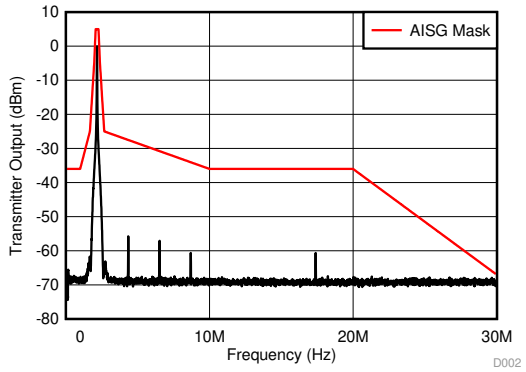
(2) Conforms to AISG spectrum emissions mask, 3GPP TS 25.461, see Figure 7-3.

6.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

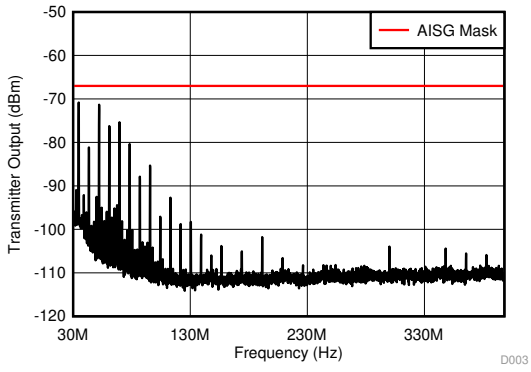
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pAQ}, t_{pQA}	Coax driver propagation delay	See Figure 7-1			5	µs
t_r, t_f	Coax receiver output rise/fall time	C_L = 15 pF, R_L = 1 kΩ; see Figure 7-1			20	ns
t_{PHL}, t_{PLH}	Receiver propagation delay	See Figure 7-2		5.5	11	µs
	Coax receiver output duty cycle	$V_{RXIN(ON)}$ = 630 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
		$V_{RXIN(ON)}$ = 200 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
t_{DIR}	Direction control active duration	DIRSET2 = GND or OPEN, DIRSET1 = GND or OPEN		1667		µs
		DIRSET2 = GND, DIRSET1 = VL		417		
		DIRSET2 = VL, DIRSET1 = VL		137		
$t_{DIRSKEW}$	Direction control skew (DIR to RXOUT)		270			ns
t_{dis}	Standby disable delay	300 mV_{PP} at 2.176 MHz on RXIN		2		ms
t_{en}	Standby enable delay	300 mV_{PP} at 2.176 MHz on RXIN		2		ms

6.7 Typical Characteristics



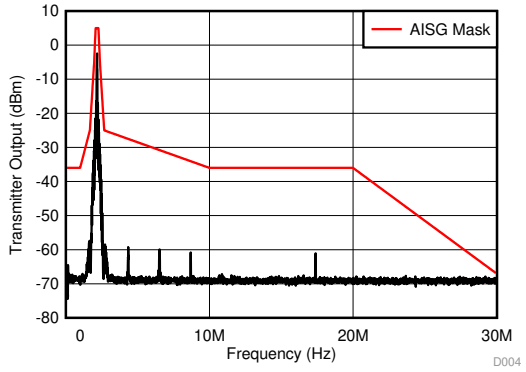
50% Duty Cycle C_F = 470 pF

Figure 6-1. Low-Frequency Emissions Spectrum With 9.6-kbps Signaling Rate



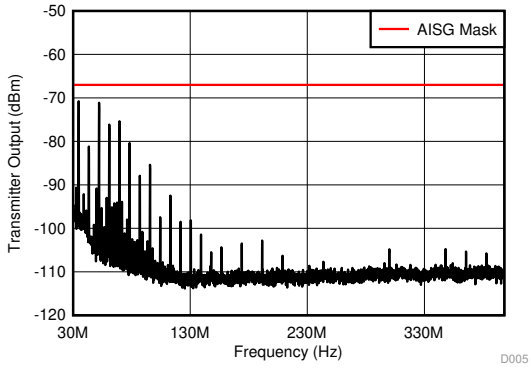
50% Duty Cycle C_F = 470 pF

Figure 6-2. High-Frequency Emissions Spectrum With 9.6-kbps Signaling Rate



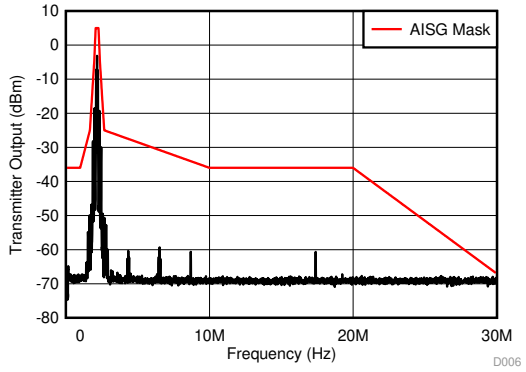
50% Duty Cycle C_F = 470 pF

Figure 6-3. Low-Frequency Emissions Spectrum With 38.4-kbps Signaling Rate



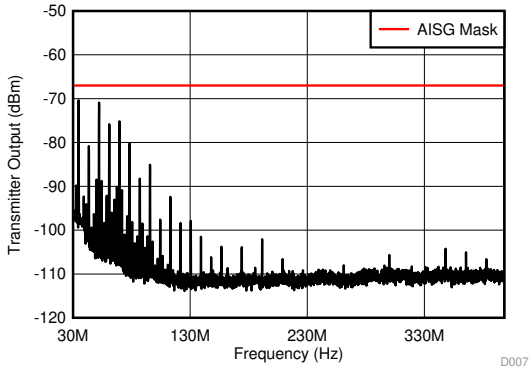
50% Duty Cycle C_F = 470 pF

Figure 6-4. High-Frequency Emissions Spectrum With 38.4-kbps Signaling Rate



50% Duty Cycle C_F = 470 pF

Figure 6-5. Low-Frequency Emissions Spectrum With 115.2-kbps Signaling Rate



50% Duty Cycle C_F = 470 pF

Figure 6-6. High-Frequency Emissions Spectrum With 115.2-kbps Signaling Rate

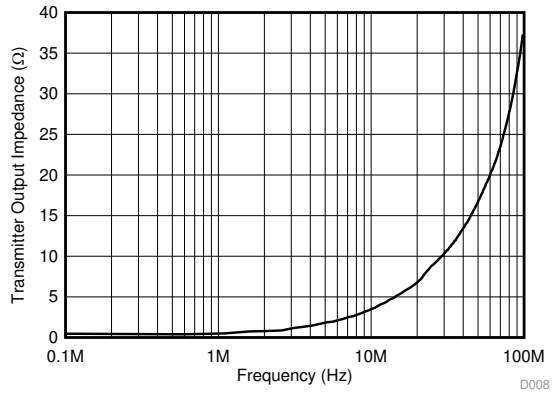


Figure 6-7. Transmitter Output Impedance

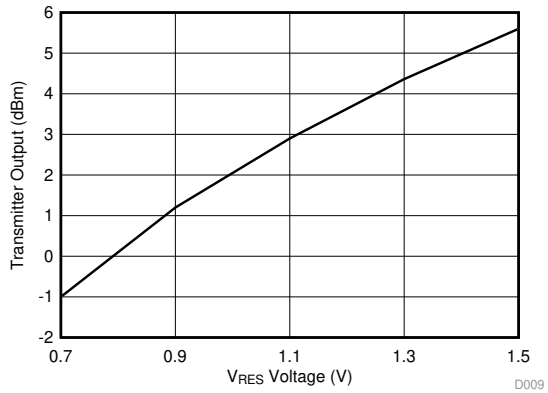
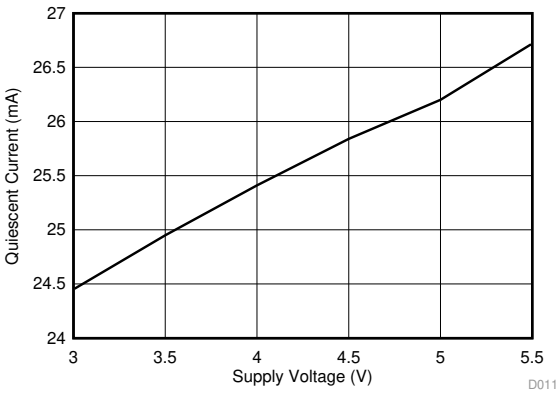
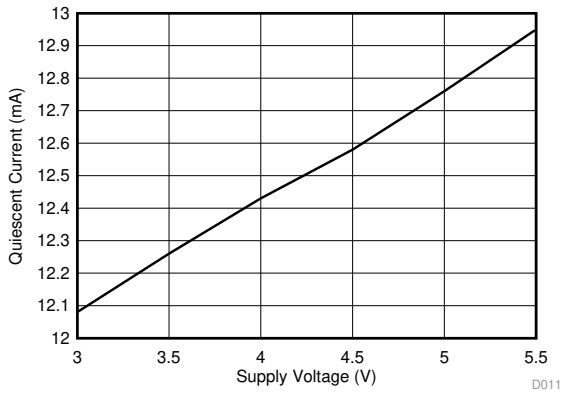


Figure 6-8. Transmit Power Adjustment



TXIN = VL

Figure 6-9. Supply Current vs Supply Voltage While Transmitting



TXIN = VL

Figure 6-10. Supply Current vs Supply Voltage in Standby Mode

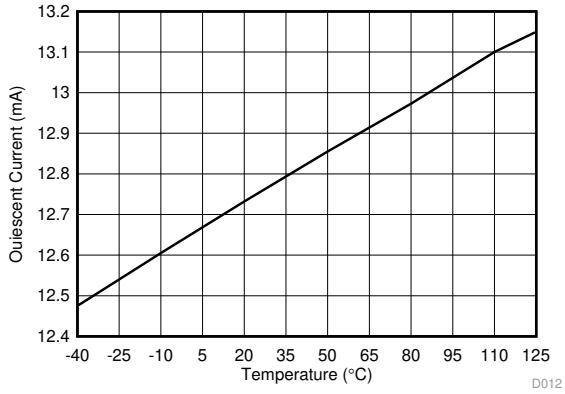


Figure 6-11. Supply Current vs Temperature in Standby Mode

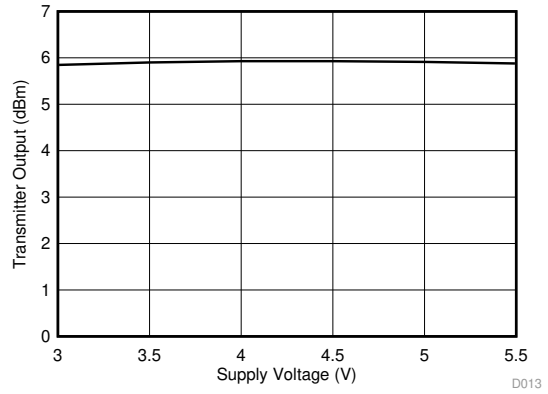


Figure 6-12. Transmitter Output Power vs Supply Voltage

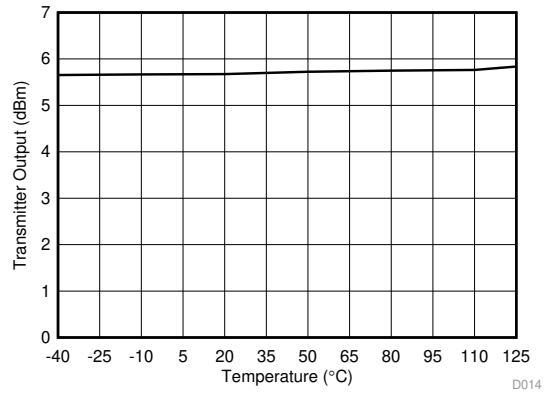


Figure 6-13. Transmitter Output Power vs Temperature

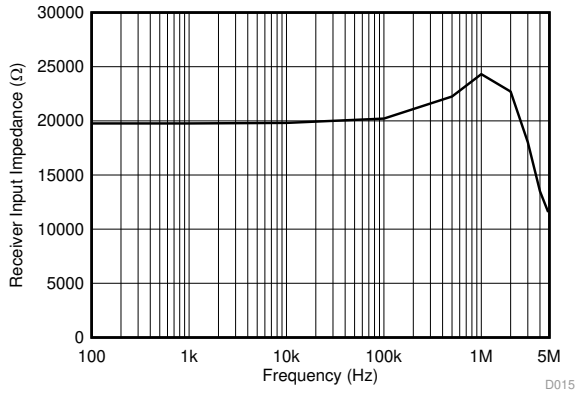


Figure 6-14. Receiver Input Impedance vs Frequency

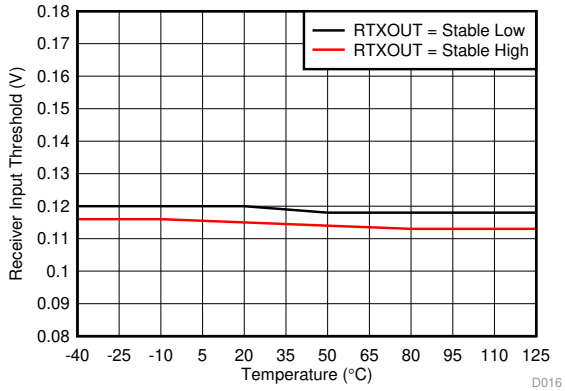


Figure 6-15. Receiver Input Threshold vs Temperature

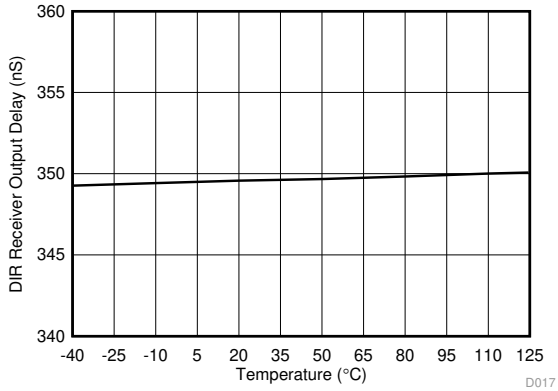


Figure 6-16. DIR Output Delay vs Temperature

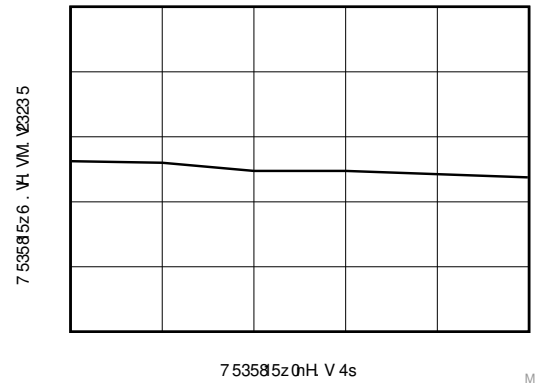


Figure 6-17. Receiver Duty Cycle With 9.6 kbps Signaling Rate

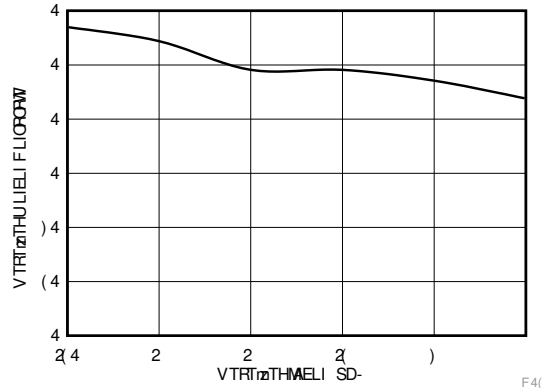


Figure 6-18. Receiver Duty Cycle With 115.2 kbps Signaling Rate

7 Parameter Measurement Information

Signal generator rate is 115 kbps, 50% duty cycle. Rise and fall times are less than 6 ns, and nominal output levels are 0 V and 3 V. Coupling capacitor, C_C, is 220 nF.

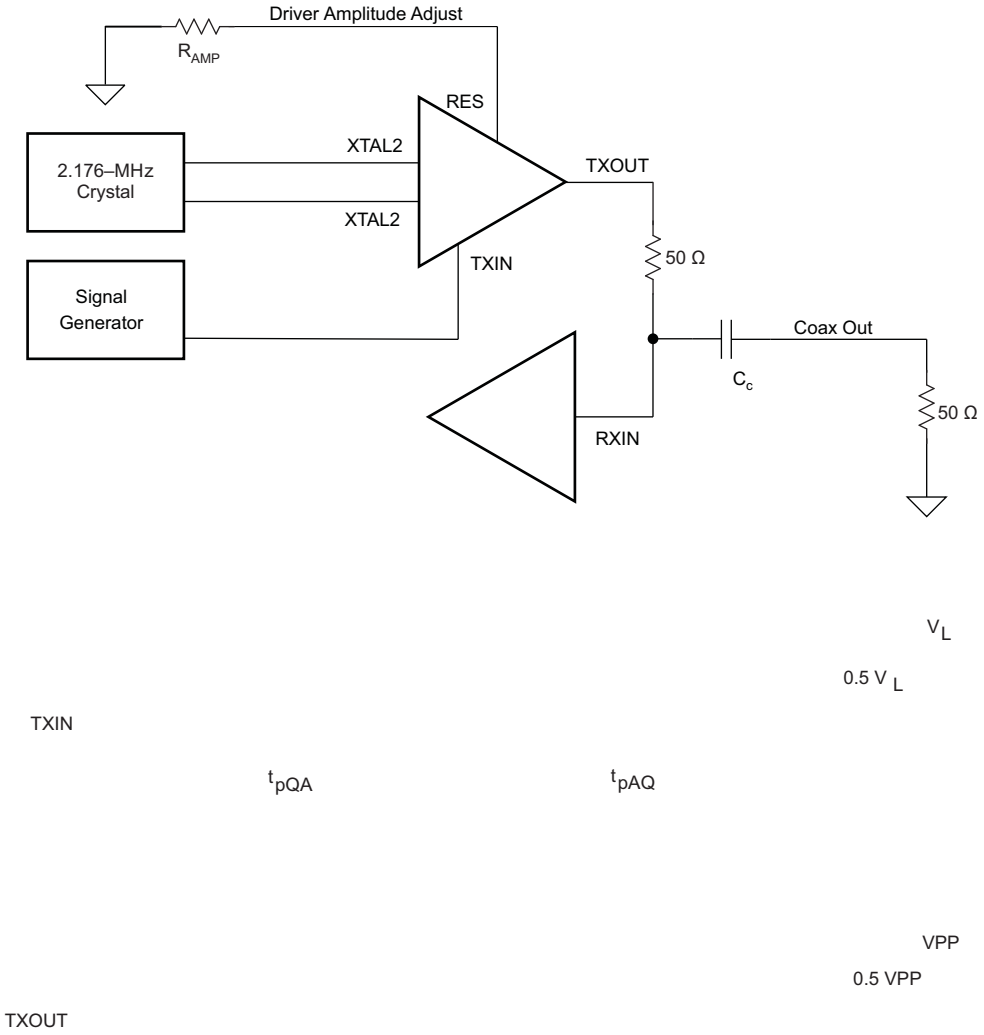


Figure 7-1. Measurement of Modem Driver Output Voltage With 50-Ω Loads

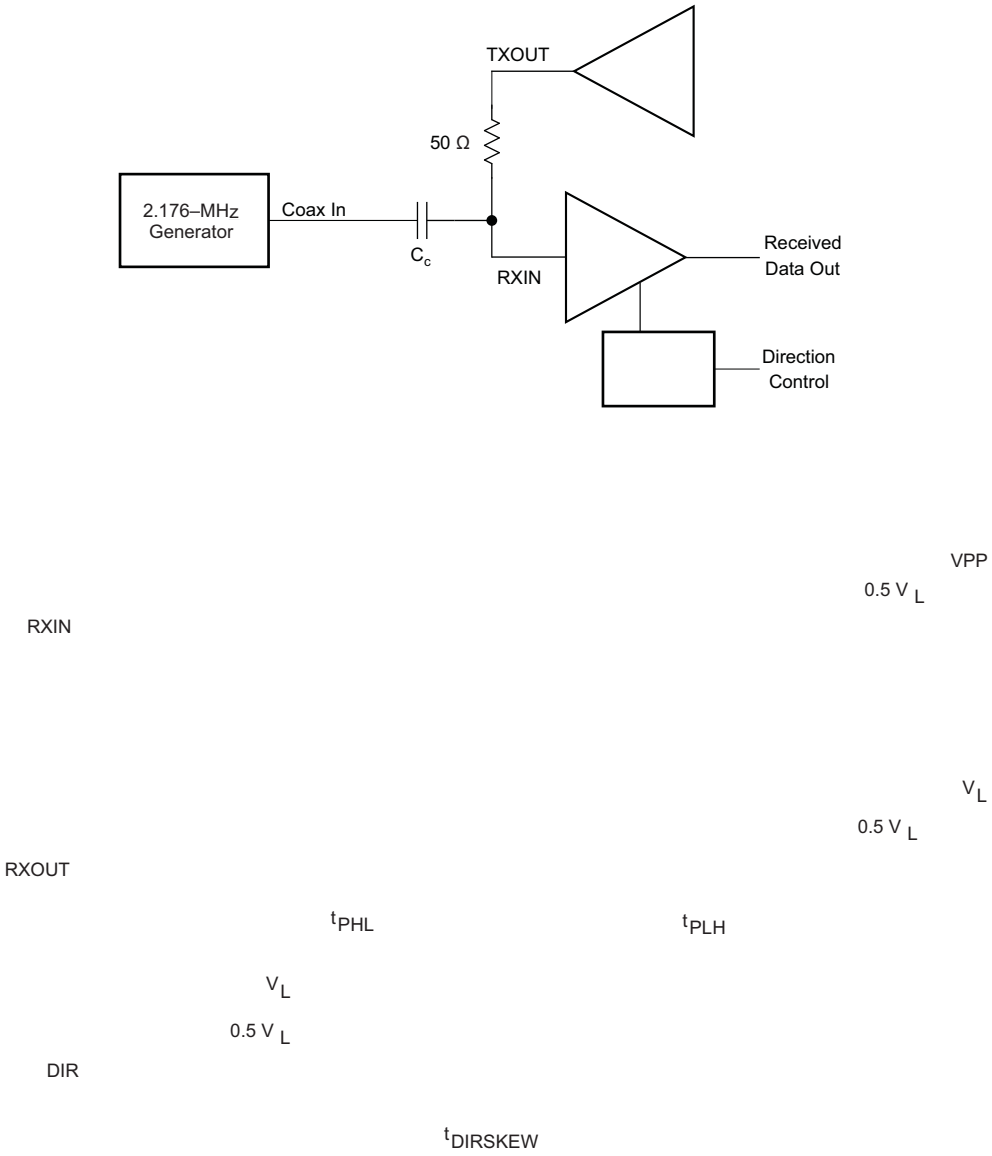


Figure 7-2. Measurement of Modem Receiver Propagation Delays

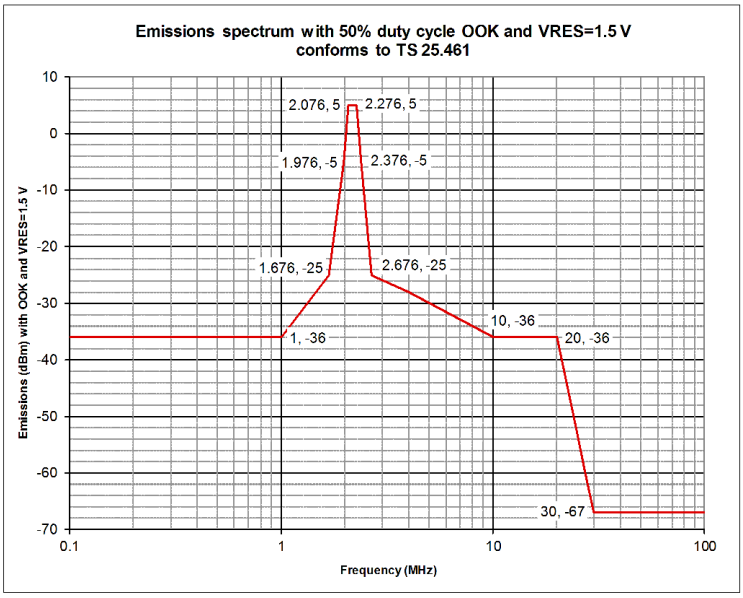


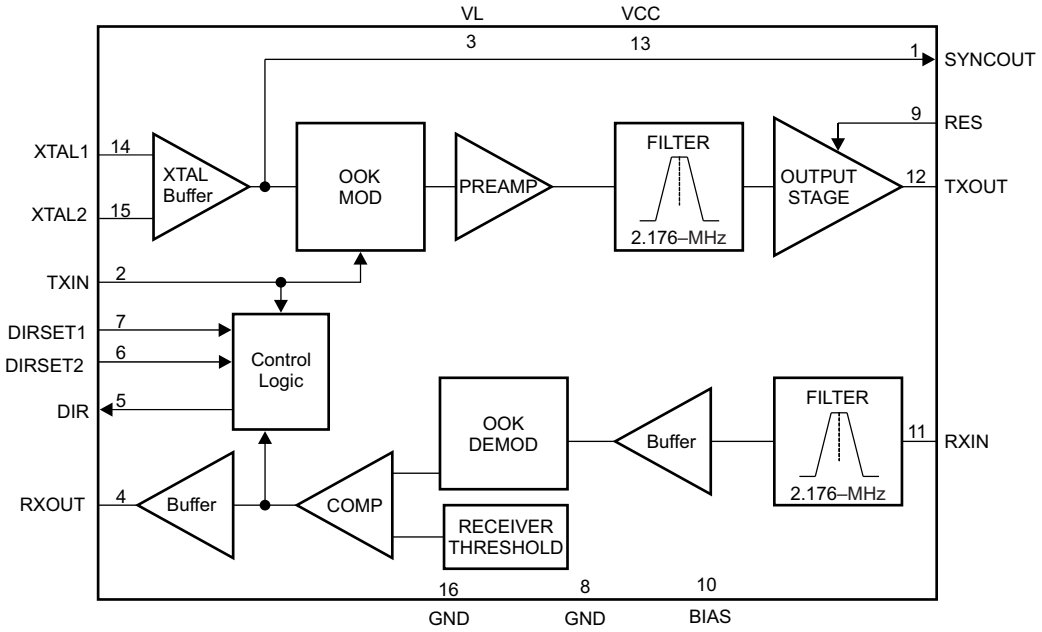
Figure 7-3. AISG Emissions Template

8 Detailed Description

8.1 Overview

The SN65HVD64 transceiver modulates and demodulates signals between the logic (baseband) and a frequency suitable for long coaxial media. The SN65HVD64 device is an integrated AISG transceiver designed to meet the requirements of the Antenna Interface Standards Group v2.0 and v3.0 specification. The SN65HVD64 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176-MHz center frequency. The transmitter supports adjustable output power levels from 0 dBm to 6 dBm delivered to the 50-Ω coax cable. The SN65HVD64 transmitter is compliant with the spectrum emission requirement provided by the AISG standard. A direction control output facilitates bus arbitration for an RS-485 interface. This device integrates an oscillator input for a crystal, and also accepts standard clock inputs to the oscillator.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Coaxial Interface

The SN65HVD64 transceiver enables the transfer of data between radio equipment by modulating baseband data to a carrier frequency of 2.176 MHz (per the AISG standard). The transmitter output amplitude can be configured from 0 dBm to 6 dBm in order to communicate over a variety of different links, and the output emissions spectrum is designed to be compliant to AISG limits. The receiver features an active bandpass filter circuit that helps to separate the carrier frequency data from other spurious frequency components.

8.3.2 Reference Input

The 2.176-MHz modulation frequency is derived from an input reference that is nominally 8.704 MHz. The input reference can come either from a crystal or from an oscillator circuit with a tolerance of up to 30 ppm.

8.3.3 RS-485 Direction Control

To facilitate bus arbitration of an RS-485 interface, the SN65HVD64 provides a direction control output that can be used to control the enable/disable controls of an RS-485 transceiver. The direction control output automatically toggles based on activity present on the coaxial input interface, and has an adjustable time constant (controlled by the DIRSET1 and DIRSET2 pins) in order to accommodate various signaling rates.

8.4 Device Functional Modes

If DIRSET1 and DIRSET2 are in a logic high state, the device will be in standby mode. While in standby mode, the receiver functions normally, detecting carrier frequency activity on the RXIN pin and setting the RXOUT state. The transmitter circuits are not active in standby mode, thus the TXOUT pin is idle regardless of the logic state of TXIN. The supply current in standby mode is significantly reduced, allowing power savings when the node is not transmitting.

When not in standby mode, the default power-on state is idle. When in idle mode, RXOUT is high, and TXOUT is quiet. The device transitions to receive mode when a valid modulated signal is detected on the RXIN line or the device transitions to transmit mode when TXIN goes low. The device stays in either receive or transmit mode until DIR time-out (nominal 16 bit times) after the last activity on RXOUT or TXIN.

When in receive mode:

- RXOUT responds to all valid modulated signals on RXIN, whether from the local transmitter, a remote transmitter, or long noise burst.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high. (In normal operation, TXIN is expected to remain high when the device is in receive mode.)
- The device stays in receive mode until 16 bit times after the last rising edge on RXOUT, caused by valid modulated signal on the RXIN line.

When in transmit mode:

- RXOUT stays high, regardless of the input signal on RXIN.
- TXOUT responds to TXIN, generating 2.176-MHz signals on TXOUT when TXIN is low, and TXOUT is quiet when TXIN is high.
- The device stays in transmit mode until 16 bit times after TXIN goes high.

Table 8-1 shows the driver functions. Table 8-2 shows the receiver functions. Figure 8-1 shows the transitions between each state.

Table 8-1. Driver Function Table

TXIN(1)	[DIRSET1, DIRSET2]	TXOUT	COMMENT
H	[L,L], [L,H] or [H,L]	< 1 mV_{PP} at 2.176 MHz	Driver not active
L		V_{OPP} at 2.176 MHz	Driver active
X	[H,H]	< 1 mV_{PP} at 2.176 MHz	Standby mode

(1) H = High, L = Low, X = Indeterminate

Table 8-2. Receiver and DIR Function Table

RXIN(1)	RXOUT	DIR	COMMENT (see Figure 8-1)
IDLE mode (not transmitting or receiving)			
< V_{IT} at 2.176 MHz for longer than DIR time-out	H	L	No outgoing or incoming signal
RECEIVE mode (not already transmitting)			
< V_{IT} at 2.176 MHz for less than $t_{DIR\ time\text{-}out}$	H	H	Incoming 1 bit, DIR stays HIGH for DIR time-out
> V_{IT} at 2.176 MHz for longer than $t_{noise\ filter}$	L	H	Incoming 0 bit, DIR output is HIGH
TRANSMIT mode (not already receiving)			
X	H	L	Outgoing message, DIR stays LOW for DIR time-out

(1) H = High, L = Low, X = Indeterminate

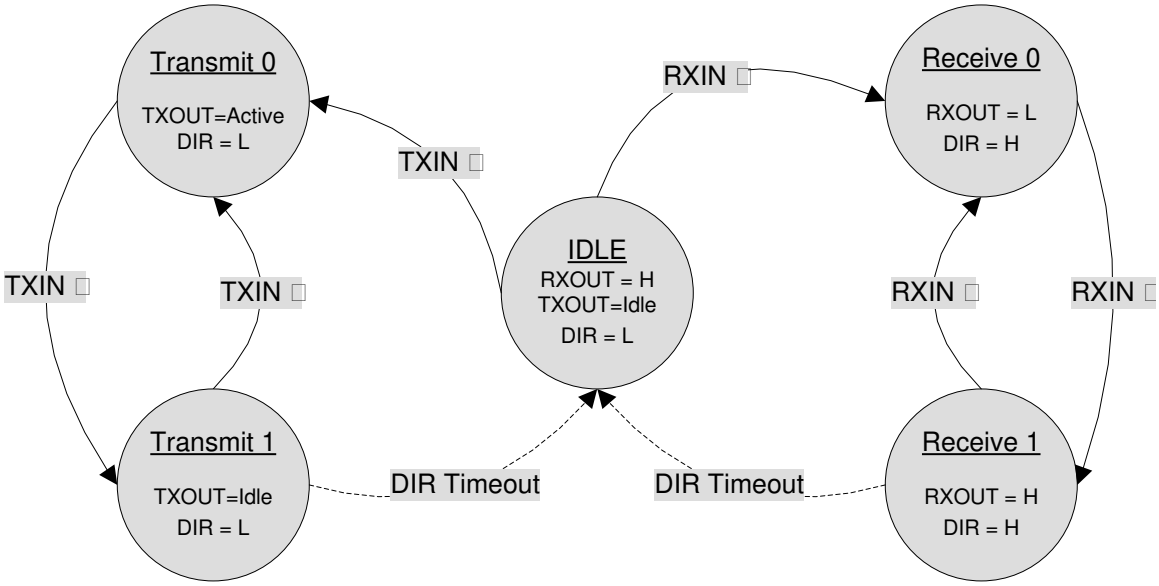


Figure 8-1. State Transition Diagram

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Driver Amplitude Adjust

The SN65HVD64 device can provide up to 2.5 V of peak-to-peak output signal at the TXOUT pin to compensate for potential loss within the external filter, cable, connections, and termination. External resistors are used to set the amplitude of the modulated driver output signal. Resistors connected across RES and BIAS set the output amplitude. The maximum peak-to-peak voltage at TXOUT is 2.5 V, corresponding to 6 dBm on the coaxial cable. The TXOUT voltage level can be adjusted by choice of resistors to set the voltage at the RES pin according to Equation 1:

$$\text{VTXOUT } (V_{PP}) = (2.5\ V_{PP} \times V_{RES}\ (V)) / 1.5\ V\ V_{RES}\ (V) = 1.5\ V \times R2 / (R1 + R2)\ V_{TXOUT}\ (V_{PP}) = 2.5\ V_{PP} \times R2 / (R1 + R2) \quad (1)$$

The voltage at the RES pin should be from 0.7 V to 1.5 V. Connect RES directly to the BIAS (R1 = 0 Ω) for maximum output level of 2.5 VPP. This gives a minimum voltage level at TXOUT of 1.2 VPP, corresponding to about 0 dBm at the coaxial cable. A 1-µF capacitor should be connected between the BIAS pin and GND. To obtain a nominal power level of 3 dBm at the feeder cable as the AISG standard requires, use R1 = 4.1 kΩ and R2 = 10 kΩ that provide 1.78 V_{PP} at TXOUT.

9.1.2 Direction Control

In many applications the mast-top modem that receives data from the base distributes the received data through an RS-485 network to several mast-top devices. When the mast-top modem receives the first logic 0 bit (active modulated signal) it takes control of the mast-top RS-485 network by asserting the direction control signal. The duration of the direction control assertion should be optimized to pass a complete message of length B bits at the known signaling rate ($1/t_{BIT}$) before relinquishing control of the mast-top RS-485 network. For example, if the messages are 10 bits in length (B=10) and the signaling rate is 9600 bits per second (t_{BIT} = 0.104 ms) then a positive pulse of duration 1.7 ms is sufficient (with margin to allow for network propagation delays) to enable the mast-top RS-485 drivers to distribute each received message. Figure 9-1 shows the assertion of direction control.

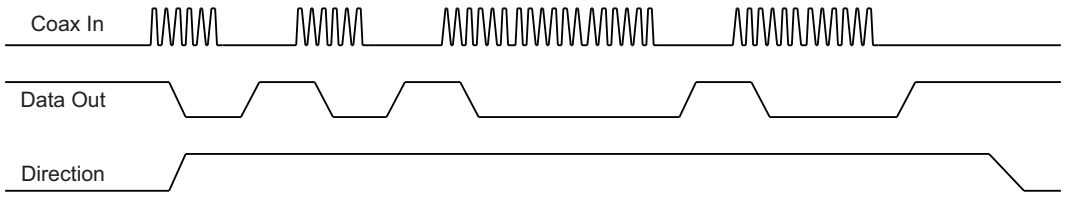


Figure 9-1. Assertion of Direction Control

9.1.3 Direction Control Time Constant

The time constant for the direction control function can be set by the control mode pins, DIRSET1 and DIRSET2. These pins should be set to correspond to the desired data rate. With no external connections to the control mode pins, the internal time constant is set to the maximum value, corresponding to the minimum data rate.

9.1.4 Conversion Between dBm and Peak-to-Peak Voltage

$$dBm = 20 \times LOG10\ [Volts\text{-}pp / SQRT(0.008 \times Z_o)] = 20 \times LOG10\ [VPP / 0.63] \text{ for } Z_o = 50\ \Omega \quad (2)$$

$$VPP = SQRT(0.008 \times Z_o) \times 10^{(dBm/20)} = 0.63 \times 10^{(dBm/20)} \text{ for } Z_o = 50\ \Omega \quad (3)$$

Table 9-1 shows conversions between dBm and peak-to-peak voltage with a 50-Ω load, for various levels of interest including reference levels from the *3GPP TS 25.461 Technical Specification*.

Table 9-1. Conversions Between dBM and Peak-to-Peak Voltage

SIGNAL ON COAX	dBm	V_{PP}
Maximum Driver ON Signal	5	1.12
Nominal Driver ON Signal	3	0.89
Minimum Driver ON Signal	1	0.71
AISG Maximum Receiver Threshold	–12	0.16
Nominal Receiver Threshold	–15	0.11
Minimum Receiver Threshold	–18	0.08
Maximum Driver OFF Signal	–40	0.006

9.2 Typical Application

The AISG On-Off Keying (OOK) interface allows for command, control, and diagnostic information to be communicated between a base station and the corresponding tower-mounted antennae. Figure 9-2 shows a typical application.

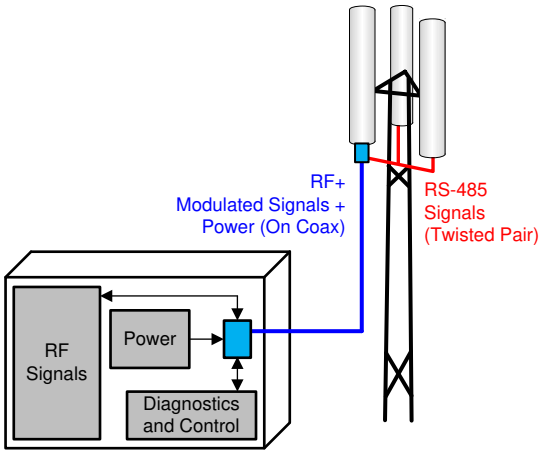


Figure 9-2. Typical AISG Application

9.2.1 Design Requirements

An AISG transceiver is used to convert between digital logic-level signals and RF signals. The AISG standard requires an RF carrier frequency of 2.176 MHz with 100-ppm accuracy. The output signal of the driver, when active, should be from 1 dBm to 5 dBm. The receiver must be designed such that the input threshold is from –18 dBm to –12 dBm.

9.2.2 Detailed Design Procedure

To ensure accuracy of the carrier frequency, an input reference frequency equal to four times the carrier (that is, 8.704 MHz) should be connected to the XTAL1 or XTAL2 inputs. This signal can come from a crystal (connected between XTAL1 and XTAL2) or from a PLL/clock generator circuit (connected to XTAL1 with XTAL2 grounded). The frequency accuracy must be within 100 ppm.

The driver output power level of the SN65HVD64 device can be adjusted through use of the RES pin. To align with AISG requirements, a nominal power level of 3 dBm should be configured by connecting a 4.1-kΩ resistor between RES and BIAS and a 10-kΩ resistor between RES and GND. Figure 9-3 shows an example schematic.

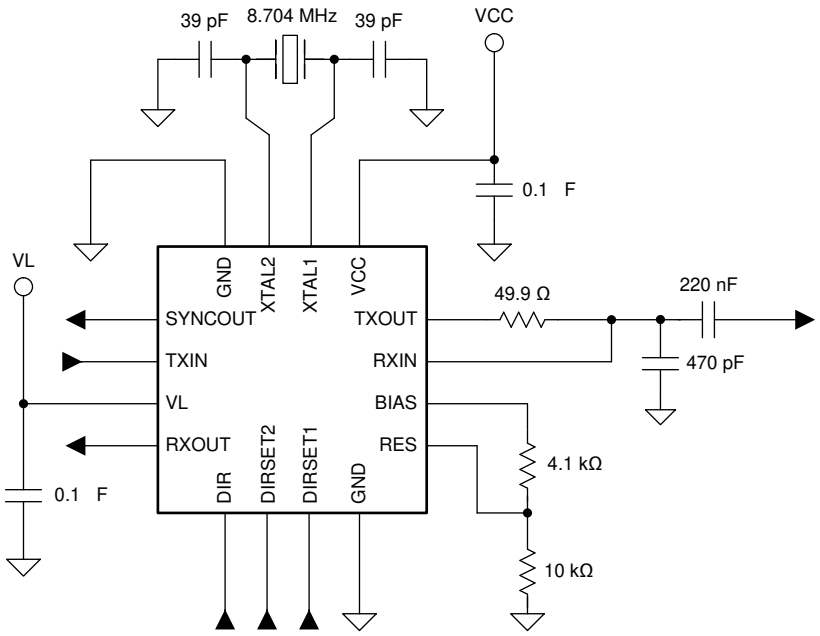


Figure 9-3. SN65HVD64 Schematic

9.2.3 Application Curve

Figure 9-4 shows the application curve for the SN65HVD64 device.

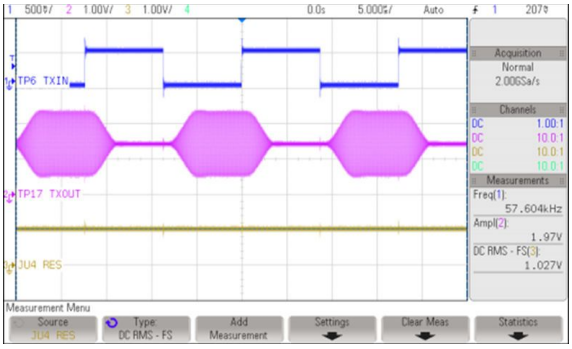


Figure 9-4. SN65HVD64 Application Curve

10 Power Supply Recommendations

The SN65HVD64 device has two power supply pins: V_{CC}, which provides power to the analog circuitry, and VL, which is a logic supply. V_{CC} should be operated from 3 V to 5.5 V, while VL can range from 1.6 V to 5.5 V to interface to different logic levels. Power supply decoupling capacitances of at least 0.1 µF should be placed as close as possible to each power supply pin.

11 Layout

11.1 Layout Guidelines

Best practices for high-speed PCB design should be observed because the coax interface to the SN65HVD64 device operates at RF. The RF signaling traces should have a controlled characteristic impedance that is well-matched to the coaxial line. A continuous reference plane should be used to avoid impedance discontinuities. Power and ground distribution should be done through planes rather than traces to decrease series resistance and increase the effective decoupling capacitance on the power rails.

11.2 Layout Example

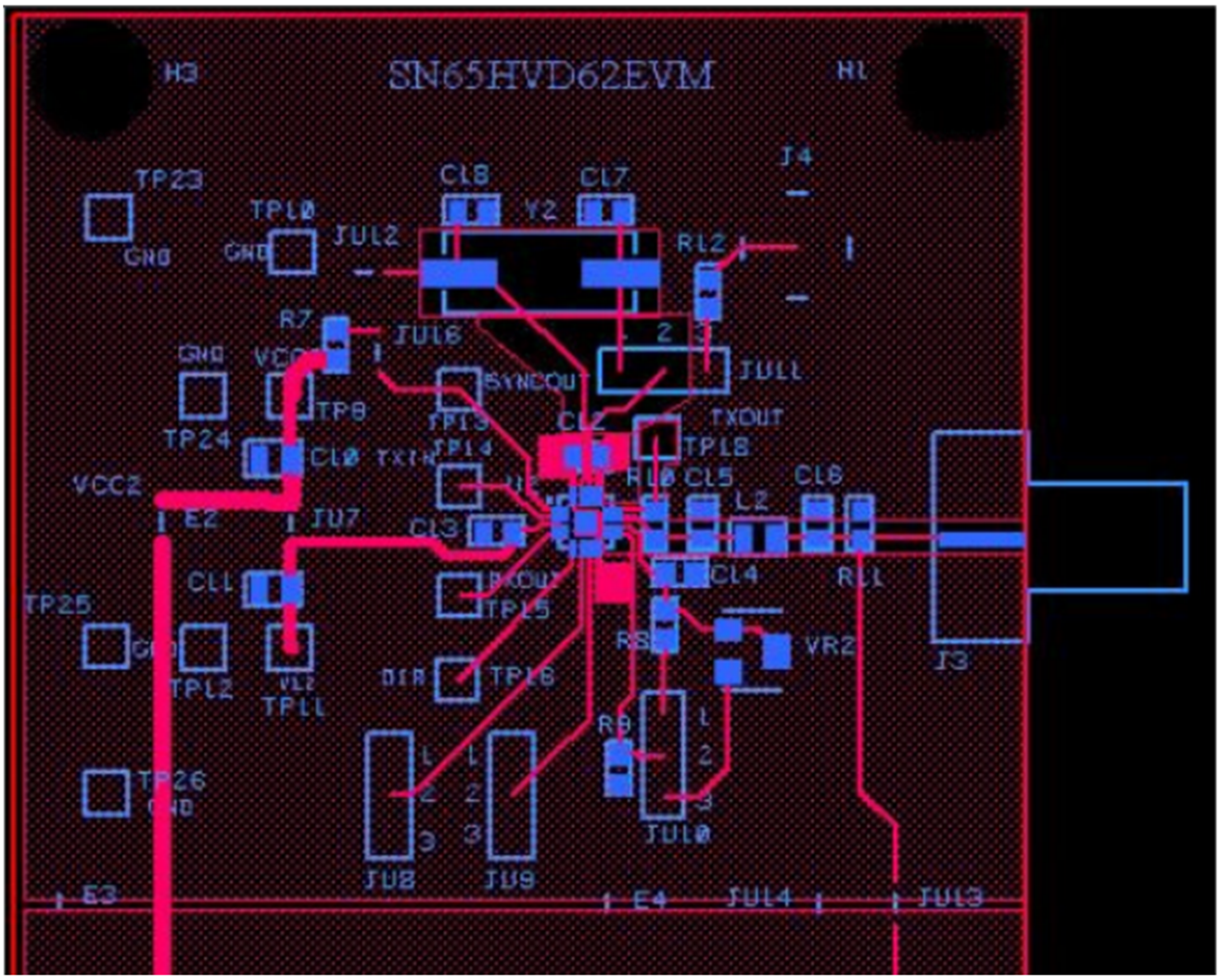


Figure 11-1. SN65HVD64 Layout

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
AISG® is a registered trademark of Antenna Interface Standards Group, Ltd.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD64RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 120	HVD64	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

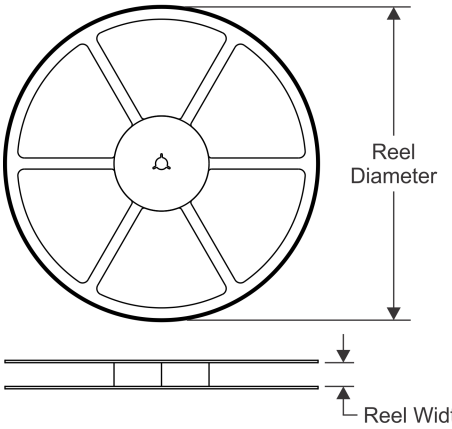
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

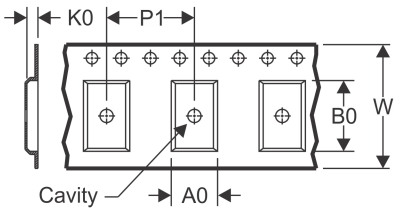
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

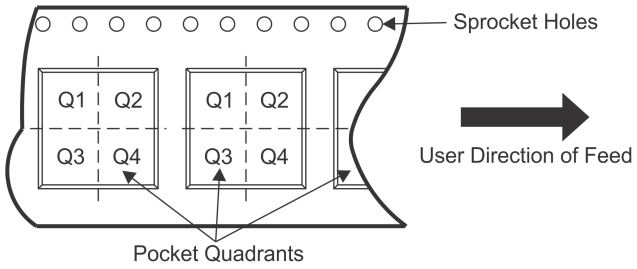


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

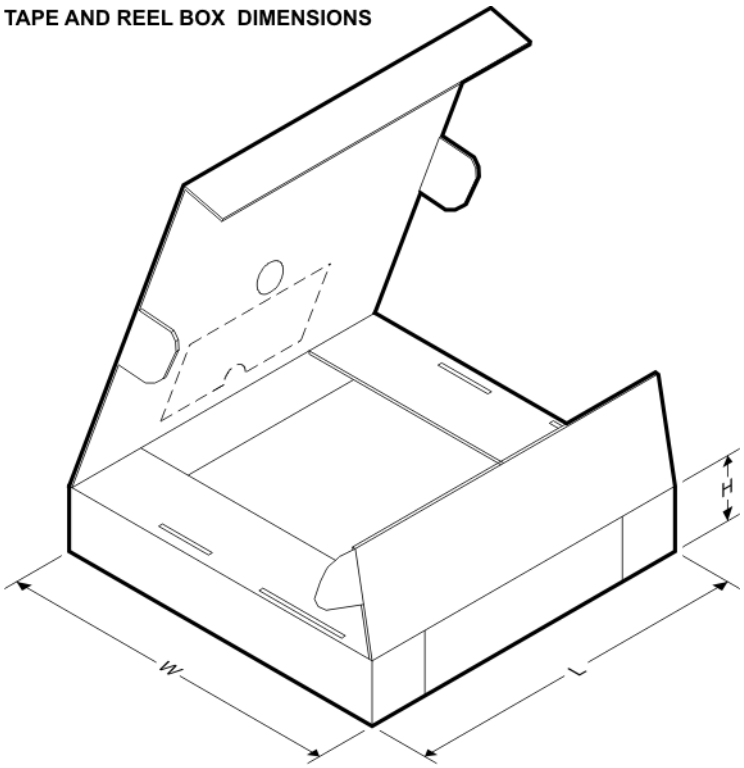
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD64RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

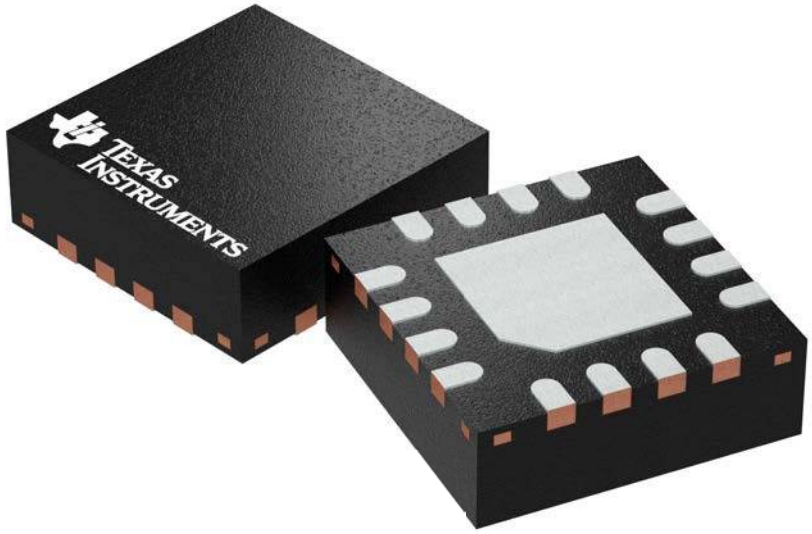


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD64RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



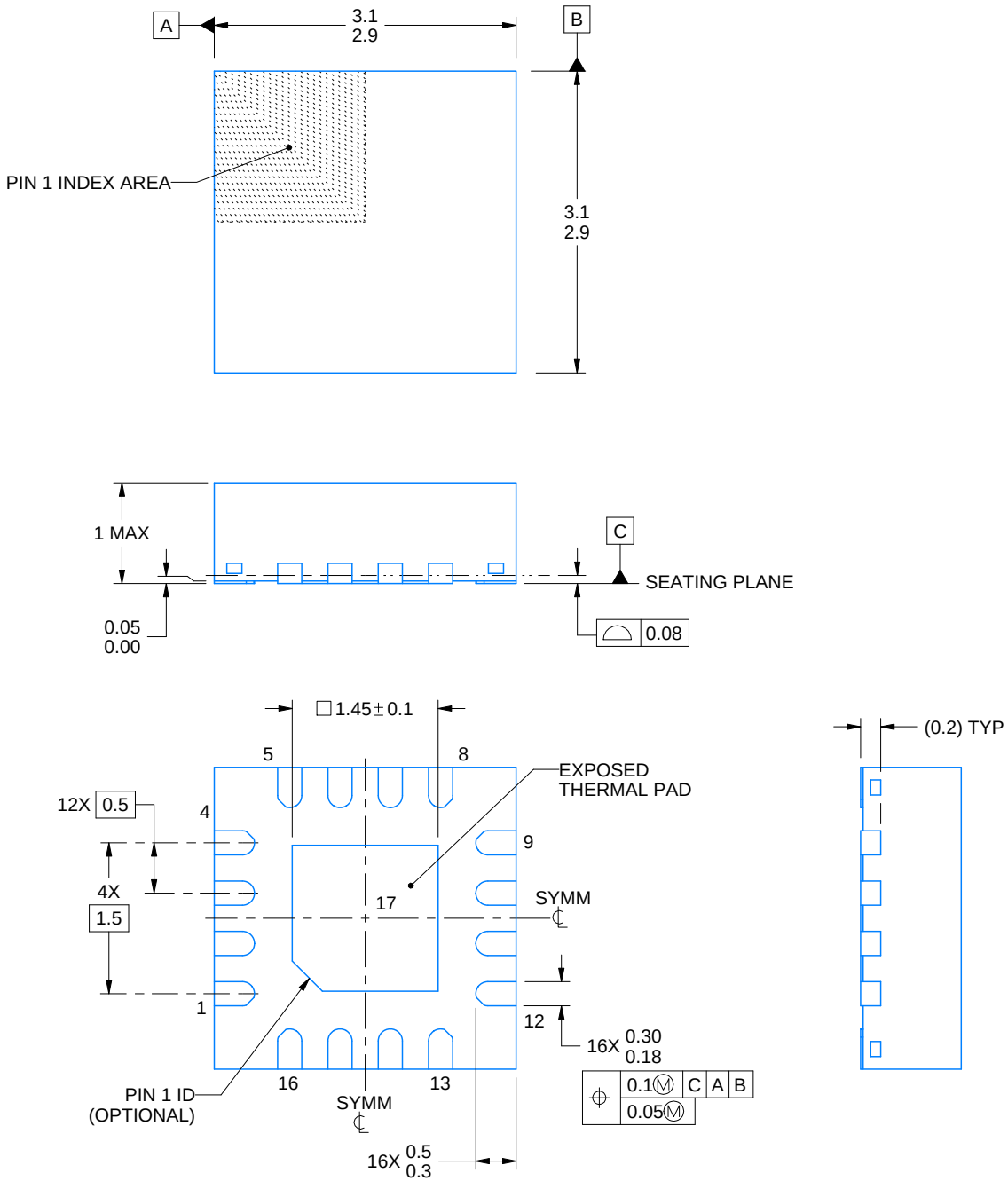
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016A

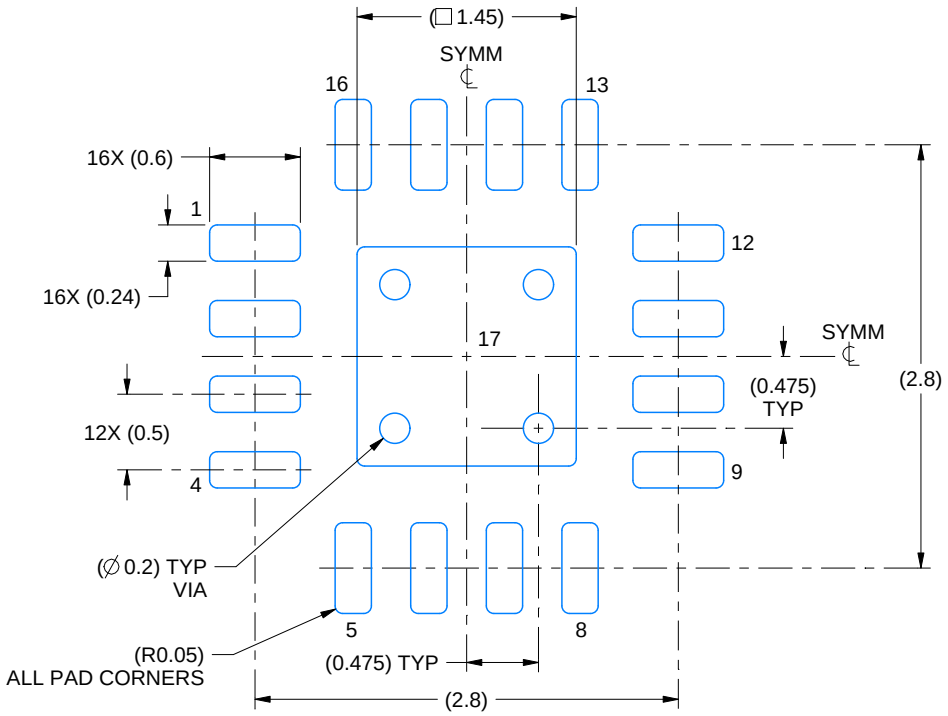
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

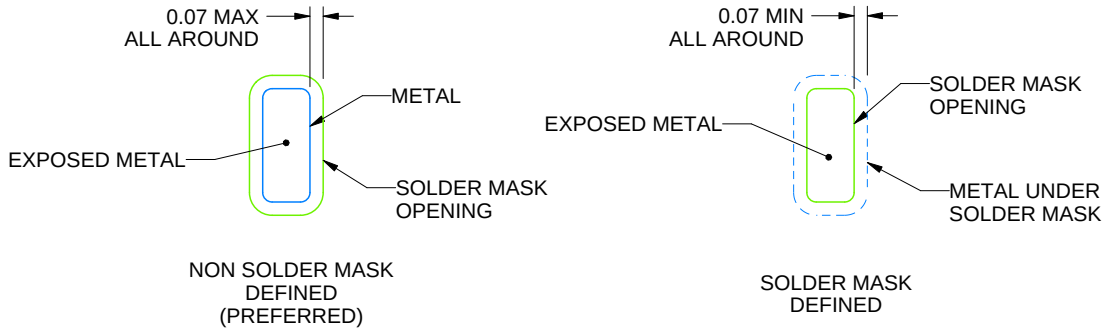


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

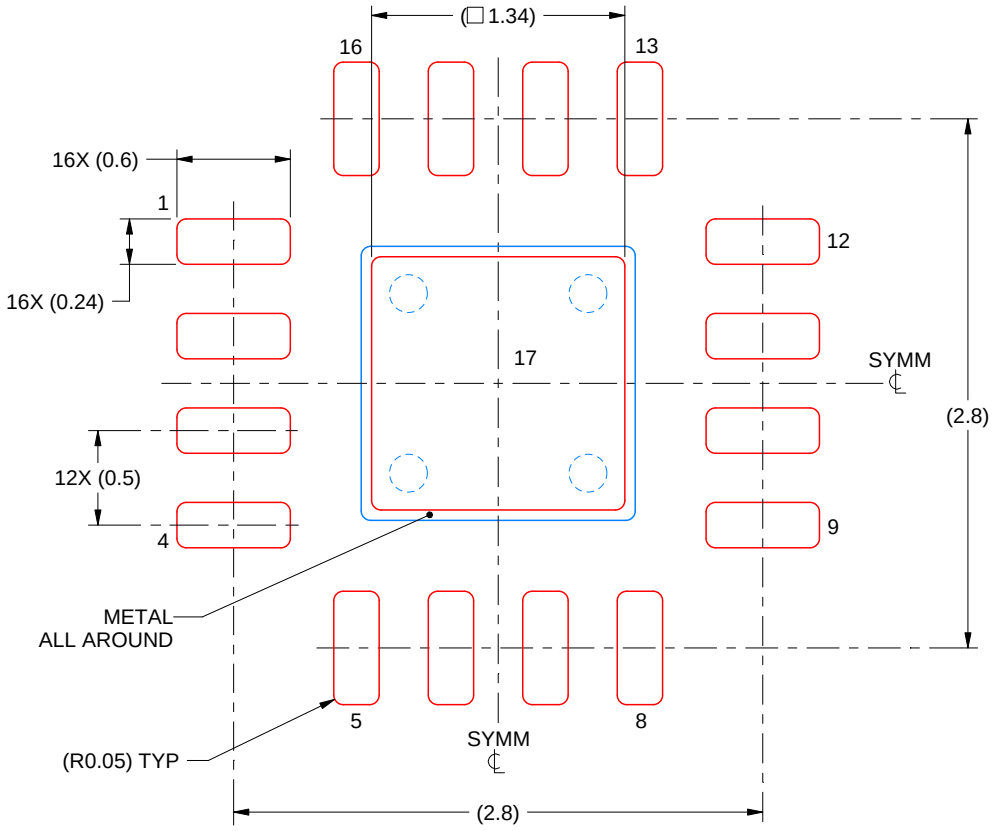


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SN74LV273A-Q1 Automotive Octal D-Type Flip-Flops With Clear

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1:
    - 40°C to + 125°C, T_A
  - Device HBM ESD Classifiaction Level 2
  - Device CDM ESD Classifcation Level C6
- Available in wettable flank QFN (WRKS) package
- 2 V to 5.5 V V_{CC} operation
- Maximum t_{pd} of 10.5 ns at 5 V
- Supports mixed-mode voltage operation on all ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Synchronize data to clock
- Simple memory - 8 bits

3 Description

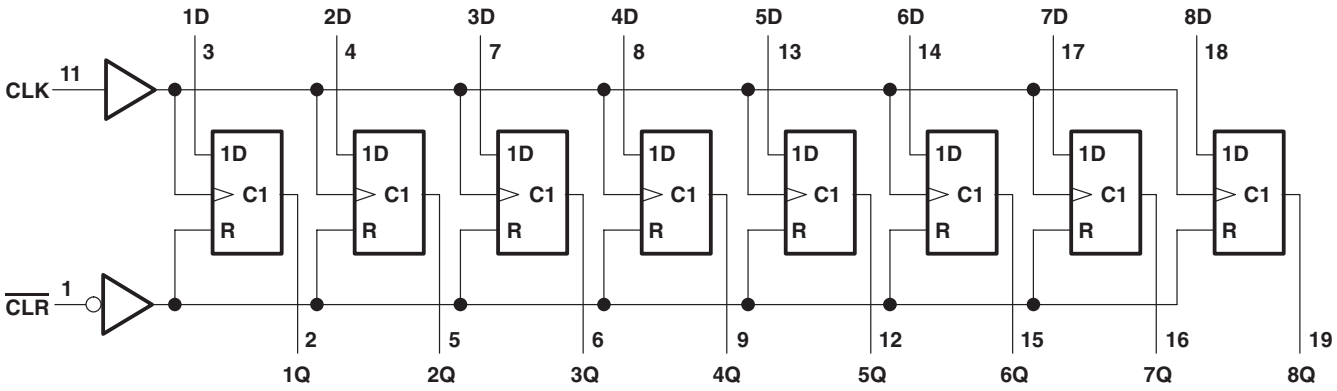
The SN74LV273A-Q1 device is an octal positive-edge triggered D-type flip-flop with shared direct active low clear ($\overline{CLR}$) input and clock (CLK).

Information at the data (D) inputs meeting the setup time requirements is transferred to the (Q) outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level or transitioning from a high level to a low level, the D input has no effect at the output. Information at the data (Q) outputs can be asynchronously cleared with a low level input through the clear ($\overline{CLR}$) pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV273A-Q1	WRKS (WQFN, 20)	4.50 × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
August 2022	*	Initial Release

5 Pin Configuration and Functions

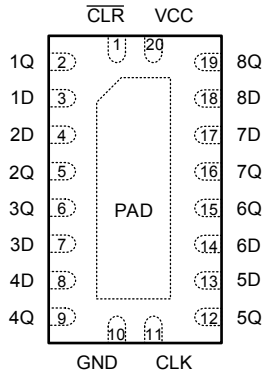


Figure 5-1. SN74LV273A-Q1: WRKS Package, 20-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	1	I	Clear for all channels, active low
1Q	2	O	Output for channel 1
1D	3	I	Input for channel 1
2D	4	I	Input for channel 2
2Q	5	O	Output for channel 2
3Q	6	O	Output for channel 3
3D	7	I	Input for channel 3
4D	8	I	Input for channel 4
4Q	9	O	Output for channel 4
GND	10	G	Ground
CLK	11	I	Clock for all channels, rising edge triggered
5Q	12	O	Output for channel 5
5D	13	I	Input for channel 5
6D	14	I	Input for channel 6
6Q	15	O	Output for channel 6
7Q	16	O	Output for channel 7
7D	17	I	Input for channel 7
8D	18	I	Input for channel 8
8Q	19	O	Output for channel 8
V_{CC}	20	P	Positive supply
Thermal pad		—	Thermal Pad[2]

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) WRKS Package Only

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage (2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV273A-Q1 WRKS (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

ADVANCE INFORMATION

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = –50 mA	2 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			
		I_{OH} = –6 mA	3 V	2.48			
		I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	Low level output voltage	I_{OL} = 50 mA	2 V to 5.5 V			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I	Input leakage current	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{off}	Input/Output Power-Off Leakage Current	V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i	Input Capacitance	V_I = V_{CC} or GND	3.3 V		2		pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER		TEST CONDITION	25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	6.5		7.5		ns
		CLK high or low	7		9		
t_{su}	Setup time	Data before CLK↑	8.5		12		ns
		$\overline{CLR}$ inactive before CLK↑	4		4.5		
t_h	Hold time	Data after CLK↑	0.5		2.5		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER		TEST CONDITION	25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		6.5		ns
		CLK high or low	5		7		
t_{su}	Setup time	Data before CLK↑	5.5		8		ns
		$\overline{CLR}$ inactive before CLK↑2.5	2.5		3		
t_h	Hold time	Data after CLK↑	1		2.5		ns

6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER		TEST CONDITION	25°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5.5		ns
		CLK high or low	5		5.5		
t_{su}	Setup time	Data before CLK↑	4.5		6		ns
		$\overline{CLR}$ inactive before CLK↑	2		2.5		
t_h	Hold time	Data after CLK↑	1		2		ns

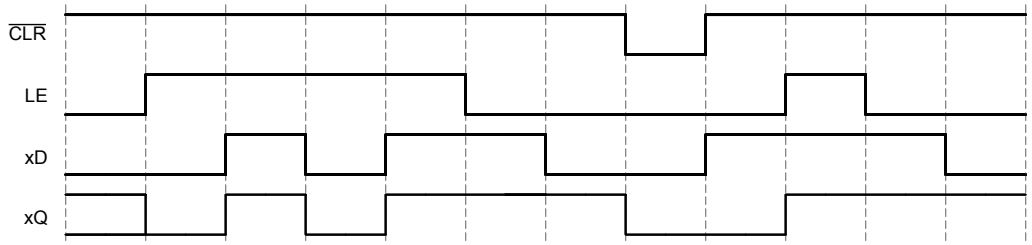


Figure 6-1. Typical Clock, Load, and Clear Sequences

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted), (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF	55	95		45			MHz
			C_L = 50 pF	45	75		40			
t_{pd}	CLK	Q	C_L = 15 pF		10.4	18.3	1		22.5	ns
	$\overline{CLR}$				10.3	19	1		23	
t_{pd}	CLK	Q	C_L = 50 pF		12.9	22.1	1		27	ns
	$\overline{CLR}$				13.1	22.8	1		27.5	
$t_{sk(o)}$						2			2	

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted), (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF	75	140		65			MHz
			C_L = 50 pF	50	110		45			
t_{pd}	CLK	Q	C_L = 15 pF		7.1	13.6	1		17.5	ns
	$\overline{CLR}$				6.9	13.6	1		17.5	
t_{pd}	CLK	Q	C_L = 50 pF		9.1	17.1	1		21	ns
	$\overline{CLR}$				8.7	17.1	1		21	
$t_{sk(o)}$						1.5			1.5	

6.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted), (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF	120	205		100			MHz
			C_L = 50 pF	80	160		70			
t_{pd}	CLK	Q	C_L = 15 pF		4.8	9	1		11.5	ns
	$\overline{CLR}$				4.7	8.5	1		11	
t_{pd}	CLK	Q	C_L = 50 pF		6.2	11	1		14	ns
	$\overline{CLR}$				6	10.5	1		13.5	
$t_{sk(o)}$						1			1	

ADVANCE INFORMATION

ADVANCE INFORMATION

6.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF f = 10 MHz	3.3 V	15.9	pF
			5 V	17.1	

6.13 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[1]		SN74LV273A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics for surface-mount packages only.

6.14 Typical Characteristics

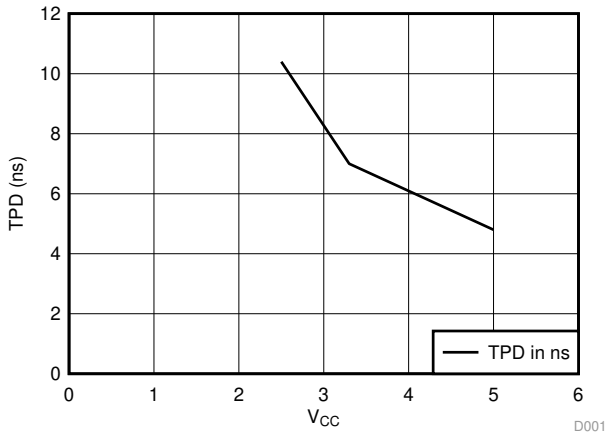


Figure 6-2. T_{PD} vs V_{cc} at 25°C

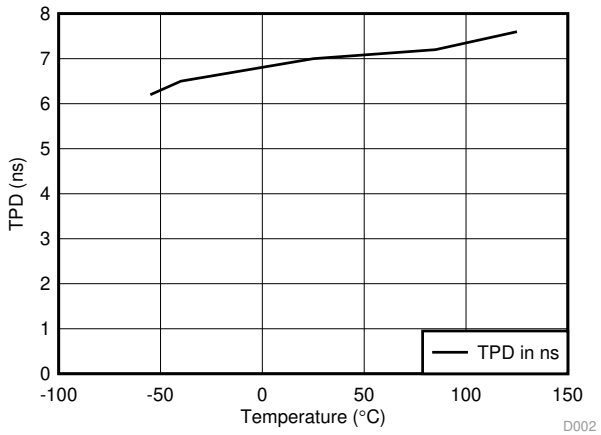
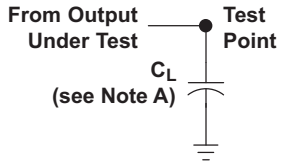
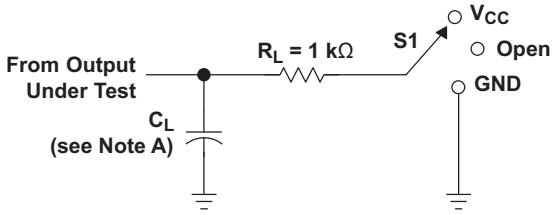


Figure 6-3. T_{PD} vs Temperature

7 Parameter Measurement Information

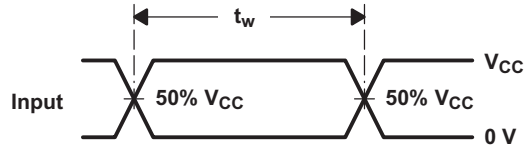


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

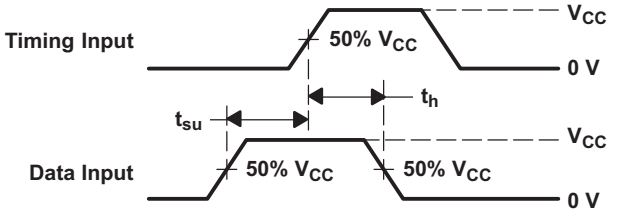


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

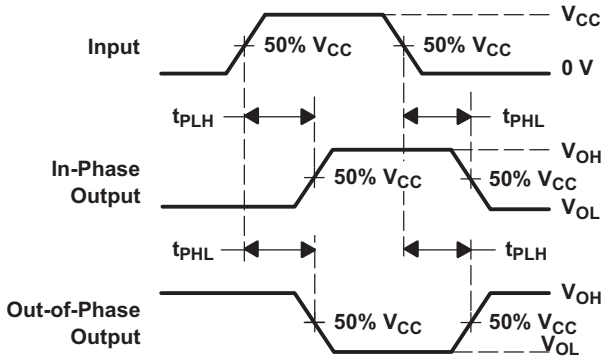
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



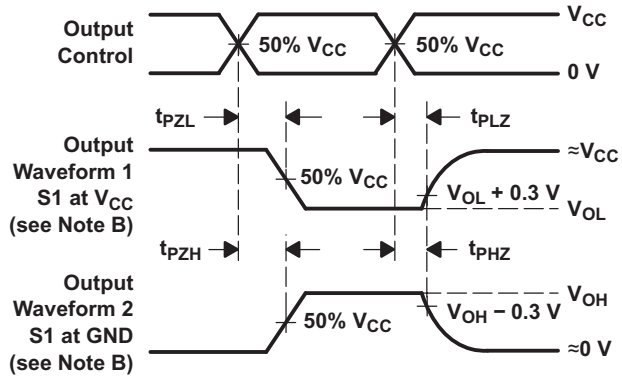
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The SN74LV273A-Q1 device is an octal positive-edge triggered D-type flip-flop with shared direct active low clear ($\overline{CLR}$) input and clock (CLK).

Information at the data (D) inputs meeting the setup time requirements is transferred to the (Q) outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level or transitioning from a high level to a low level, the D input has no effect at the output. Information at the data (Q) outputs can be asynchronously cleared with a low level input through the clear ($\overline{CLR}$) pin.

The SN74LV273A-Q1 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

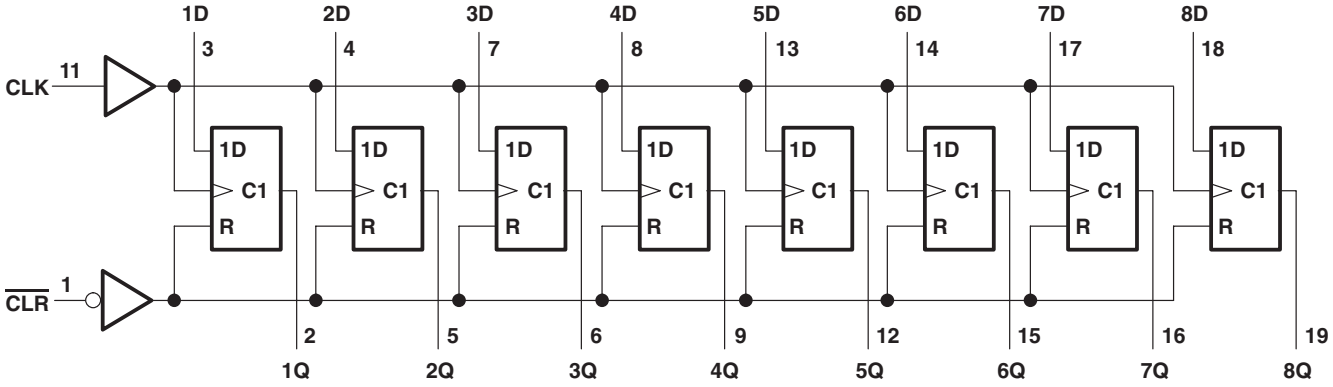


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

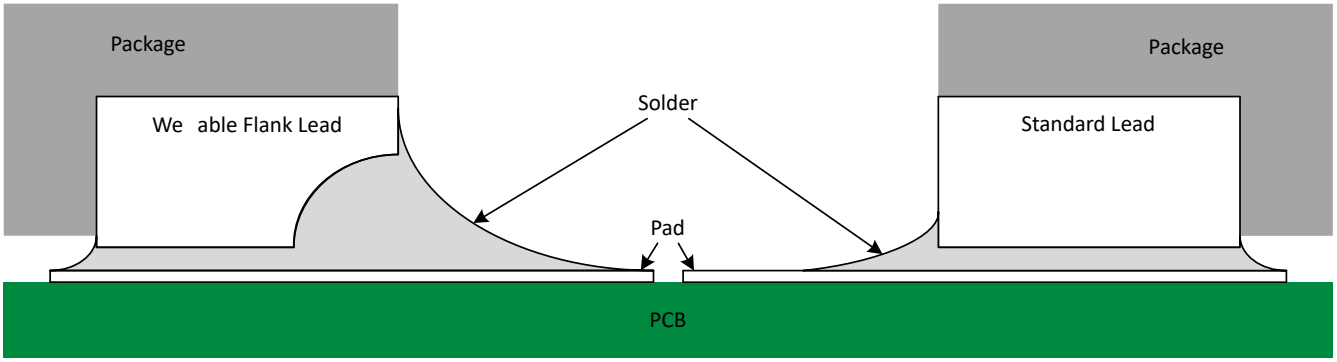


Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 8-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. Please see the mechanical drawing for additional details.

8.3.5 Clamp Diode Structure

Figure 8-3 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

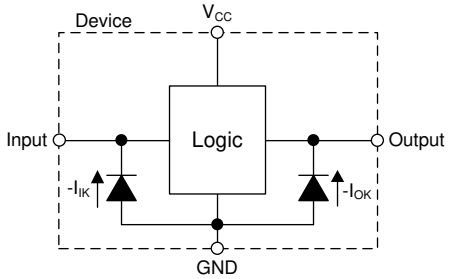


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

ADVANCE INFORMATION

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	L, H, ↓	X	Q_0
H	↑	L	L
H	↑	H	H

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2) L = output low, H = output high, Q_0 = previous state

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74LV273A-Q1 is used to synchronize incoming data to the system clock on an 8-bit bus.

9.2 Typical Application

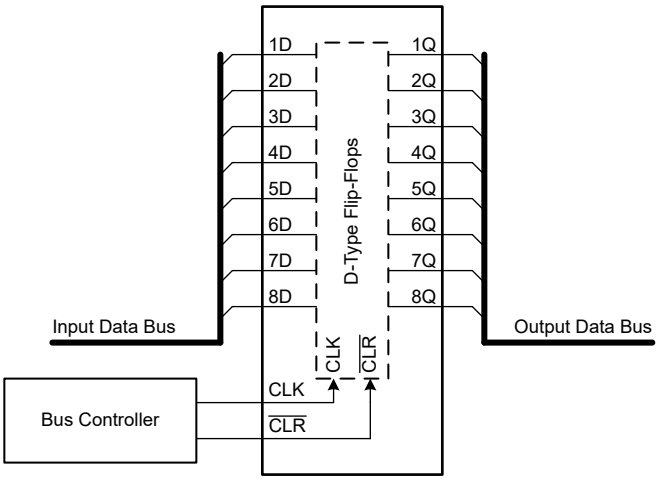


Figure 9-1. Typical Application Diagram

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV273A-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV273A-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV273A-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV273A-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

ADVANCE INFORMATION

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV273A-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV273A-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

ADVANCE INFORMATION

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV273A-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

9.2.5 Application Curves

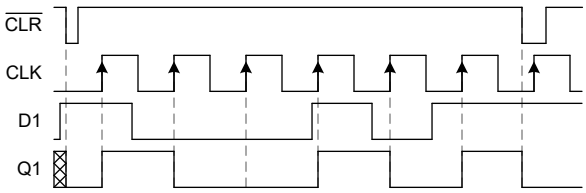


Figure 9-2. Application Timing Diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

ADVANCE INFORMATION

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

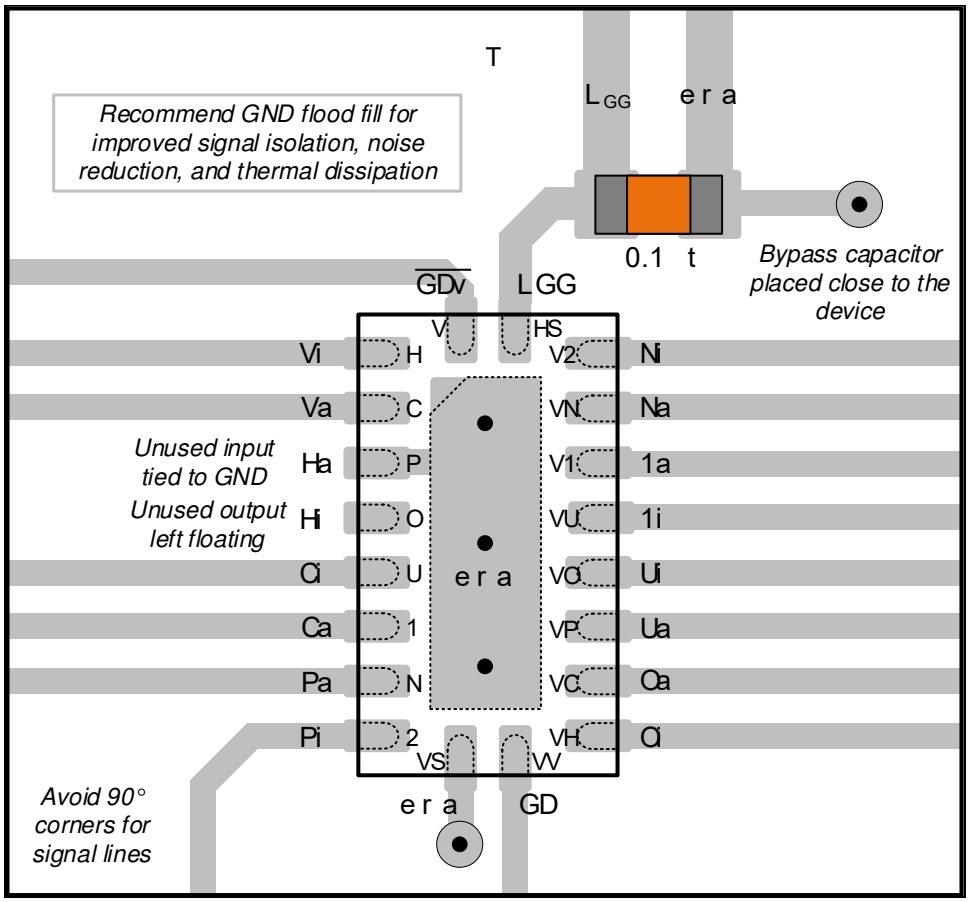


Figure 11-1. Layout Example for the SN74LV273A-Q1 in the WRKS Package

12 Device and Documentation Support

12.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Power-Up Behavior of Clocked Devices*
- Texas Instruments, *Introduction to Logic*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

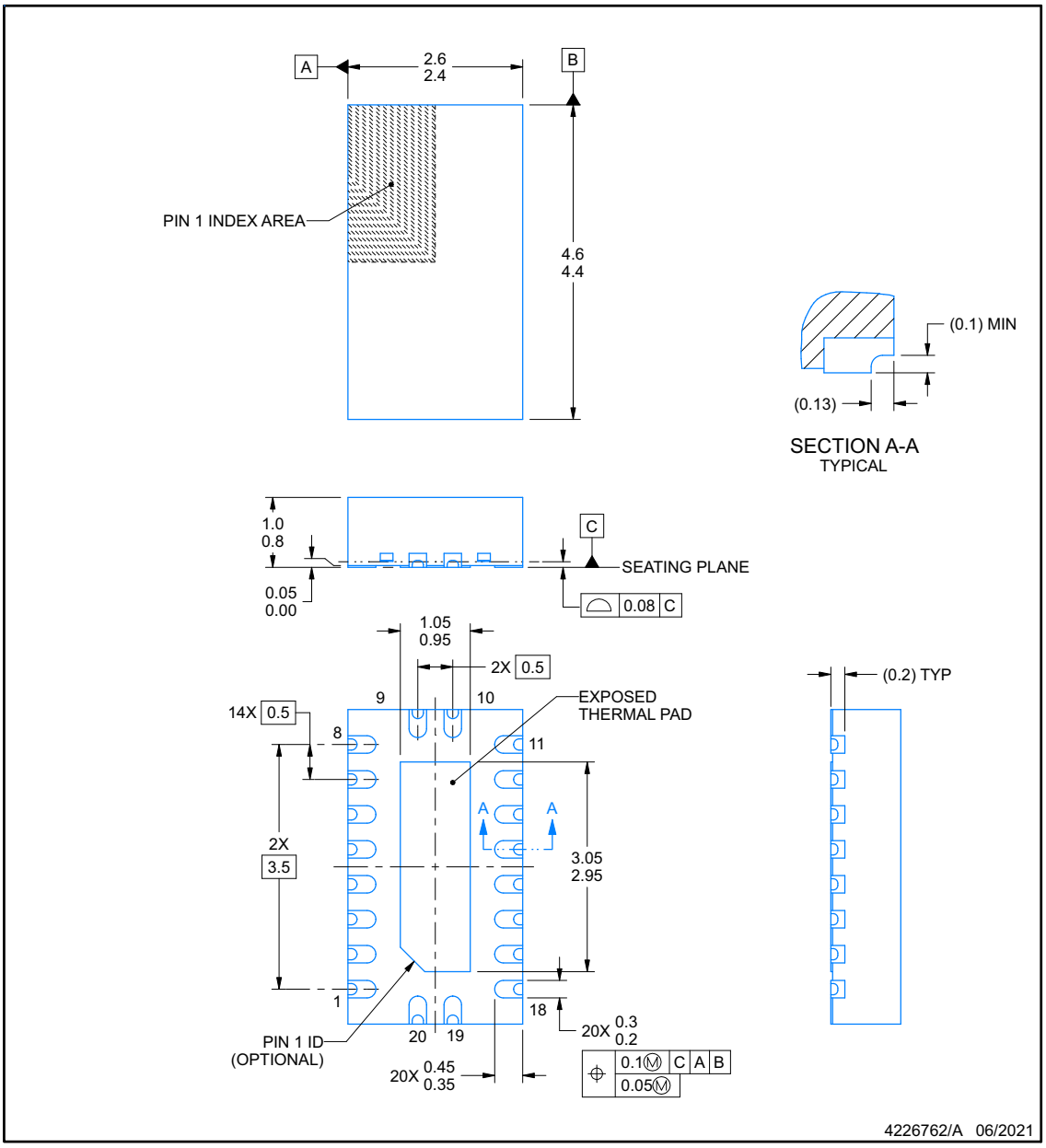
ADVANCE INFORMATION

PACKAGE OUTLINE

RKS0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

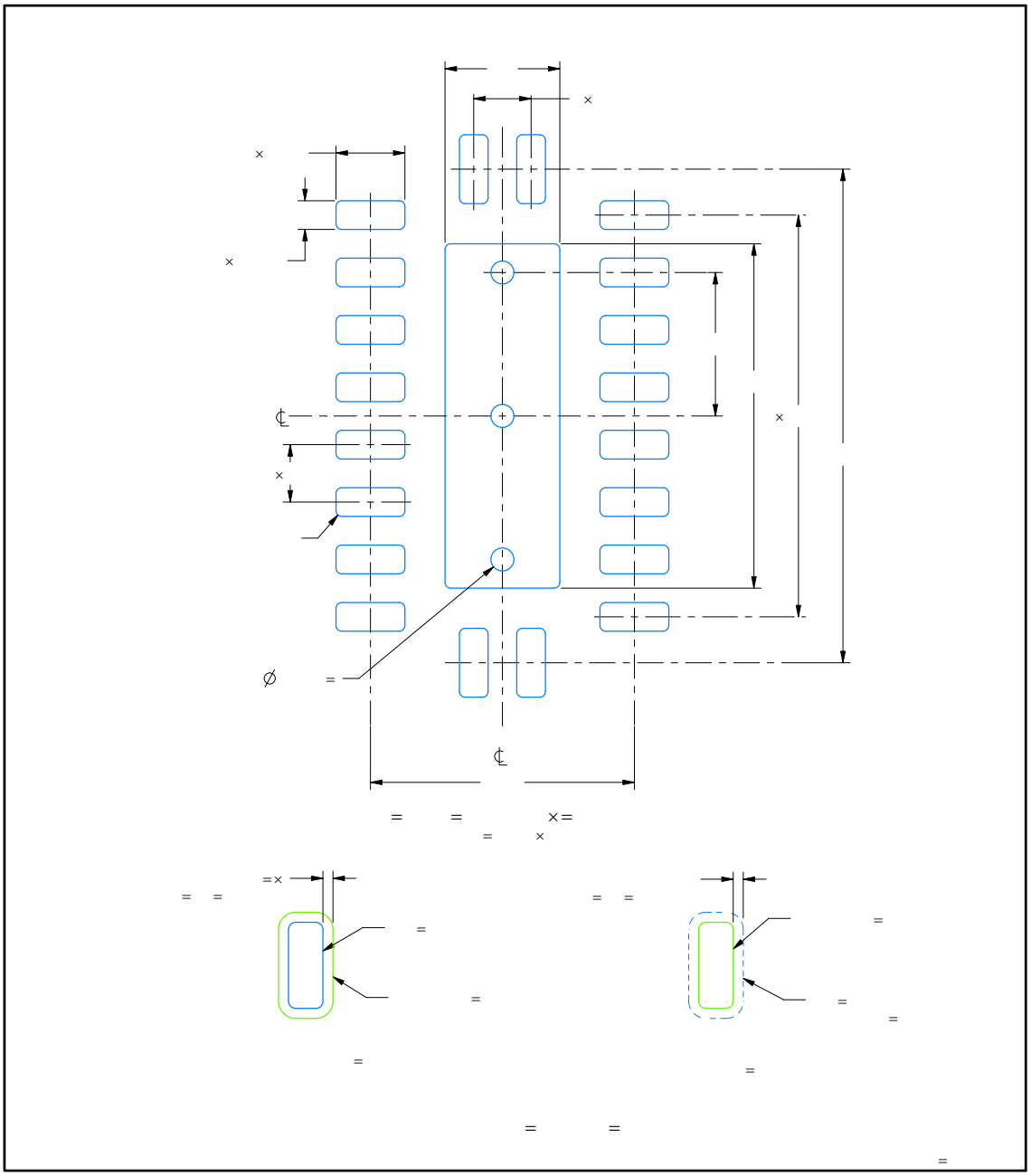


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RKS0020B — **VQFN - 1 mm max height**

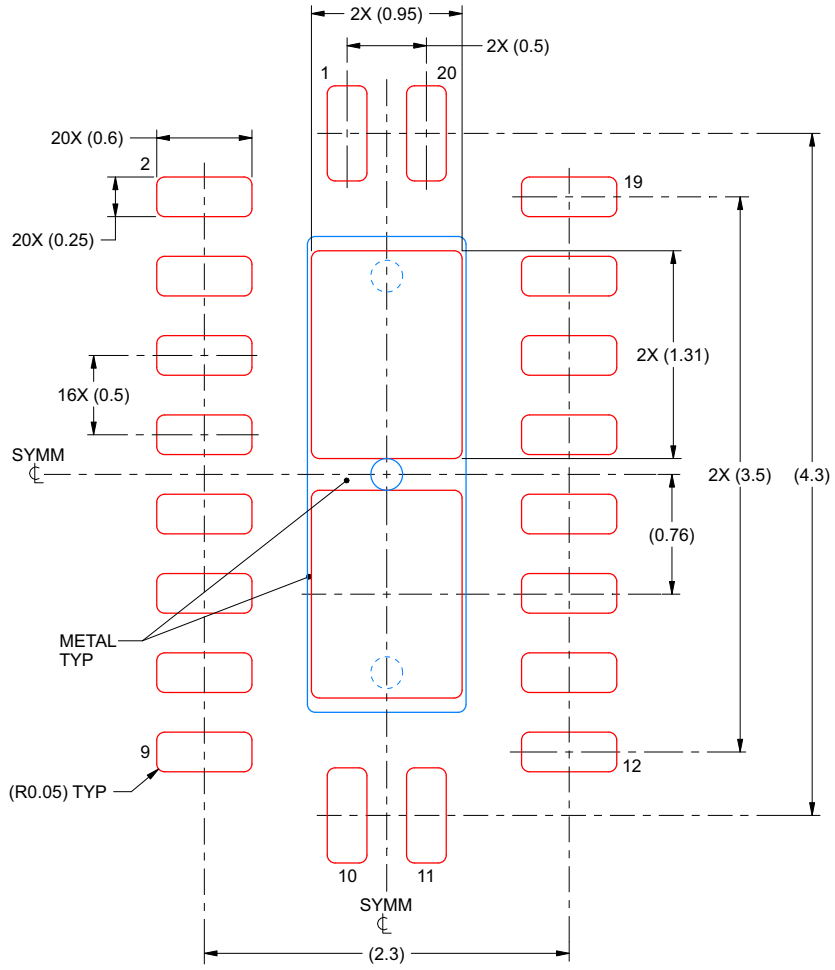


ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RKS0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

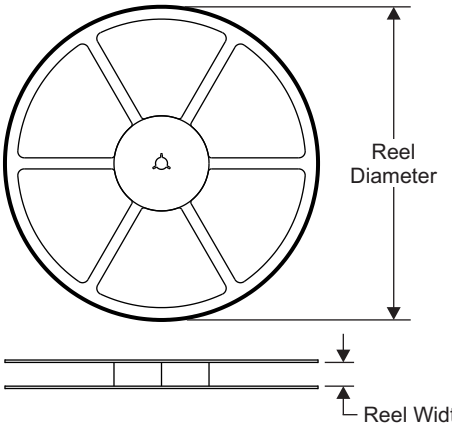
4226762/A 06/2021

NOTES: (continued)

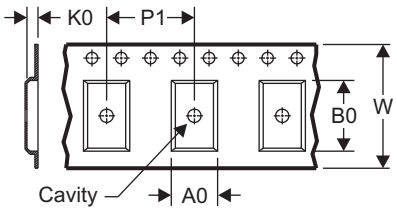
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

13.1 Tape and Reel Information

REEL DIMENSIONS

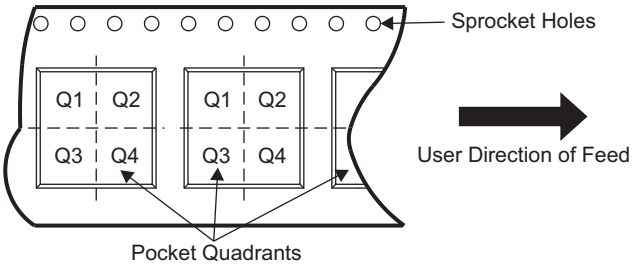


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

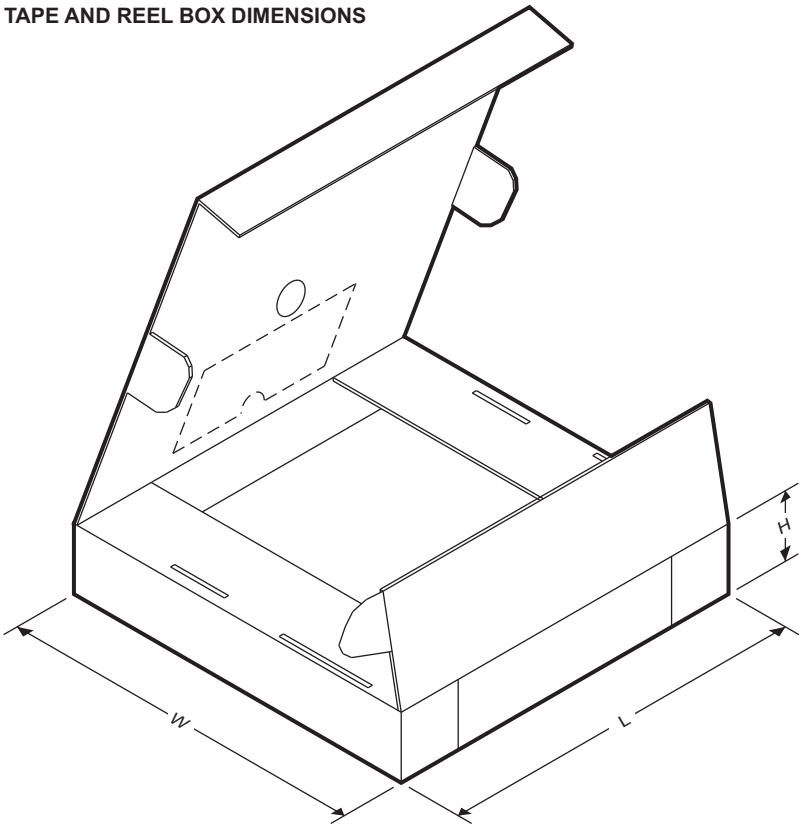


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV273AQWRKSRQ1	WQFN	RKS	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV273AQWRKSRQ1	WQFN	RKS	20	3000	210.0	185.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCLV273AQWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV273A-Q1 :

- Catalog : SN74LV273A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

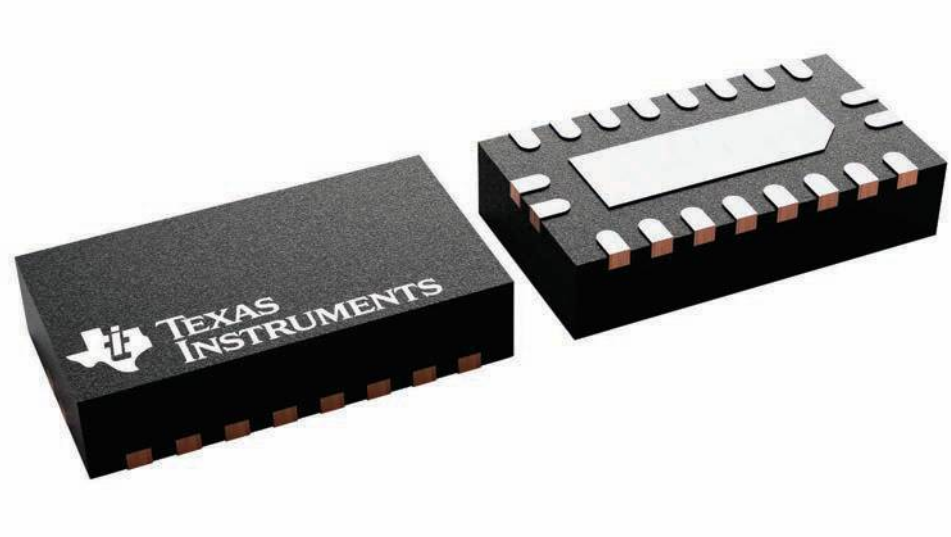
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226872/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

SN74LV541A-Q1 Automotive Octal Buffers/Drivers With 3-State Outputs

1 Features

8 100

1

40 + 1257 T

2

6

N 4 5

2 V 595 V V

6 5 V

8

I 88

8 250

17

2 Applications

3 Description

T N74 V541 8 1 +

2 V 595 V V 9 T

4O 1 O 25

7

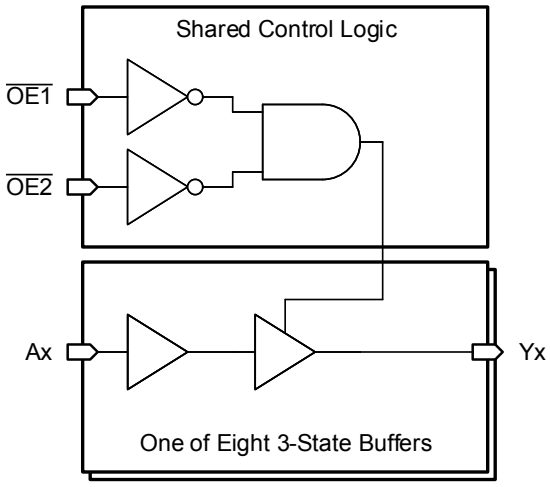
9

Package Information[415]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
N74 V541 8 1	4 N7205	4950 2950
	4 OT7205	5910 3900

415 7

9



Logic Diagram (Positive Logic)

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

DATE	REVISION	NOTES
2022	6	I

5 Pin Configuration and Functions

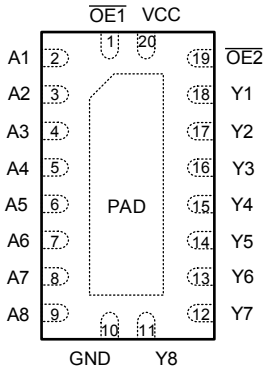


Figure 5-1. WRKS Package, 20-Pin WQFN (Top View)

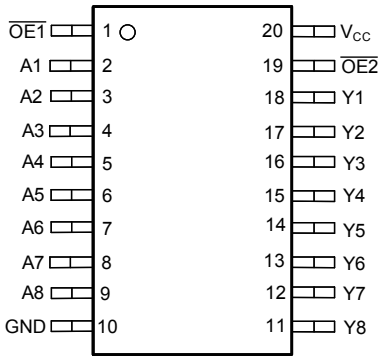


Figure 5-2. DGS Package, 20-Pin SOT (Top View)

Table 5-1. Pin Functions

PIN		TYPE[415]	DESCRIPTION
NAME	NO.		
O 1	1	I	O 17
1	2	I	I 1
2	3	I	I 2
3	4	I	I 3
4	5	I	I 4
5	6	I	I 5
6	7	I	I 6
7	8	I	I 7
8	9	I	I 8
N	10		
8	11	O	O 8
7	12	O	O 7
6	13	O	O 6
5	14	O	O 5
4	15	O	O 4
3	16	O	O 3
2	17	O	O 2
1	18	O	O 1
O 2	19	I	O 27
V	20		
T [425]			T N 9 9

[415] I I 7O O 7I+O I O 7 7 9
[425]

6 Specifications

6.1 Absolute Maximum Ratings

O 8 4 5 415

			MIN	MAX	UNIT
V			095	7	V
V_I	I 425		095	7	V
V_O	V 8 8 425		095	7	V
V_O	O 425 435		095	V + 095	V
I_I	I	V_I 0		20	
I_O	O	V_O 0		50	
I_O		V_O 0 V		25	
	V N			50	
T			65	150	

415 O *Absolute Maximum Ratings* 9 *Absolute Maximum Ratings* *Recommended Operating Conditions*9
I *Recommended Operating Conditions* *Absolute Maximum Ratings*7
7 7 7 7 9
425 T 8 9
435 T 595 V 9

6.2 ESD Ratings

			VALUE	UNIT
V_{45}		457 1008002 2415	4000	V
		4 57 1008011 4	2000	

415 1008002 N I++ 8 001 9

6.3 Recommended Operating Conditions

8 4 5 415

			MIN	MAX	UNIT
V			2	595	V
V_I	8	V 2 V	195		V
		V 298 V 595 V	V 097		
V_I	8	V 2 V		095	V
		V 298 V 595 V	V	093	
V_I	I		0	595	V
V_O	O		0 V		V
		38	0	595	
I_O	8	V 2 V		50	
		V 298 V 297 V		2	
		V 3 V 396 V		8	
		V 495 V 595 V		16	
I_O	8	V 2 V		50	
		V 298 V 297 V		2	
		V 3 V 396 V		8	
		V 495 V 595 V		16	
+	I	V 298 V 297 V		200	+ V
		V 3 V 396 V		100	
		V 495 V 595 V		20	
T	O 8		40	125	

415 V N 9 *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC415		SN74LV541A-Q1		UNIT
		WRKS (WQFN)	DGS (SOT)	
		20 PINS	20 PINS	
	88	86	12595	+
45	88 45	8296	8090	+
	88	5499	6398	+
T	88	995	894	+
	88	5499	7999	+
45	88 45	3295	N+	+

415 7 *Semiconductor and IC Package Thermal Metrics.*

ADVANCE INFORMATION

ADVANCE INFORMATION

6.5 Electrical Characteristics

8 4 59

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
V_O		I_O 50	2 V 595 V	V 091			V
		I_O 2	293 V	2			
		I_O 8	3 V	2948			
		I_O 16	495 V	398			
V_O		I_O 50	2 V 595 V			091	V
		I_O 2	293 V			094	
		I_O 8	3 V			0944	
		I_O 16	495 V			0955	
I_I	I	V_I 595 V N	0 V 595 V			1	
I_O	O 8 4 8 5	V_O V N	595 V			5	
I		V_I V N7 I_O 0	595 V			20	
I	I +O 8O	V_I V_O 0 595 V	0 V			5	
	I	V_I V N	393 V		2		

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

8 4 57 4 7815

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
			15		697		1		1395	
	O				895		1		1995	
	O				894		1		15	
			50		897		1		1895	
	O				1095		1		24	
	O				1293		1		20	
45						2			2	

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

8 4 57 4 7815

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
			15		498	7	1		895	
	O				691	1095	1		1295	
	O				598	11	1		12	
			50		691	1095	1		12	
	O				794	14	1		16	
	O				898	1594	1		1795	
45						195			195	

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

8 4 57 4 7815

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			–40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
			15		395	5	1		6	
	$\overline{O}$		15		493	792	1		895	
	$\overline{O}$		15		399	795	1		8	
			50		493	7	1		8	
	$\overline{O}$		50		593	992	1		1095	
	$\overline{O}$		50		596	898	1		10	
45			50			1			1	

6.9 Noise Characteristics415

V 393 V7 50 7T 25

PARAMETER			SN74LV541A-Q1			UNIT
			MIN	TYP	MAX	
V_{O45}	7	V_O		095	093	V
$V_{O4\ V5}$	7	V_O		094	093	V
$V_{O4\ V5}$	7	V_O		299		V
V_{I45}	8		2931			V
V_{I45}	8				0999	V

415 8 9

6.10 Operating Characteristics

T 25

PARAMETER	TEST CONDITIONS		V_{CC}	TYP	UNIT
	50	10	393 V	1693	
			5 V	1793	

6.11 Typical Characteristics

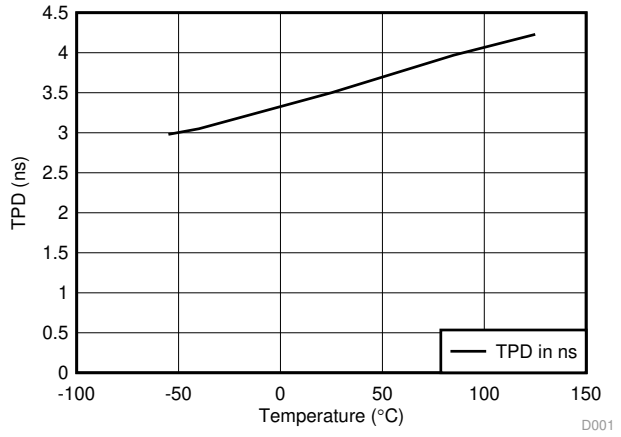


Figure 6-1. TPD vs Temperature

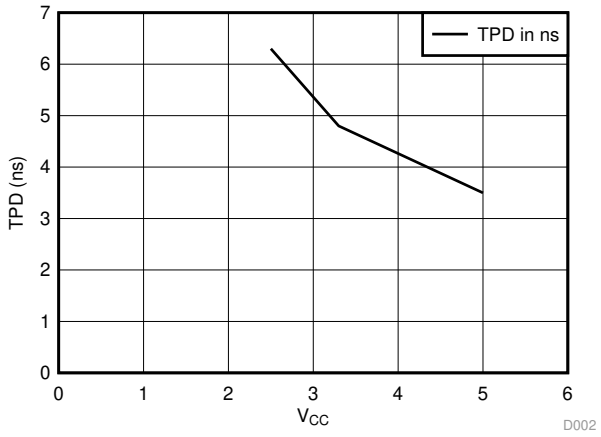
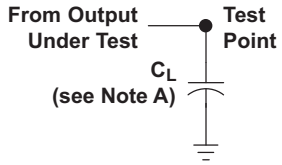


Figure 6-2. TPD vs V_{CC} at 25°C

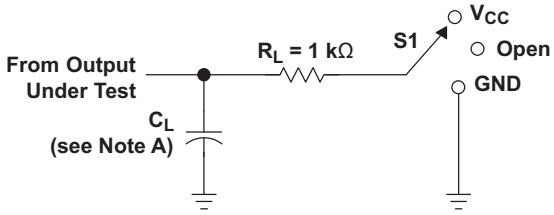
ADVANCE INFORMATION

ADVANCE INFORMATION

7 Parameter Measurement Information

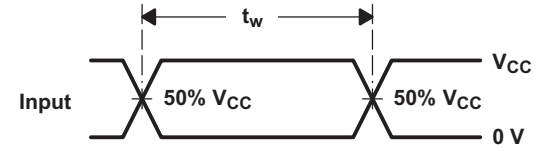


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

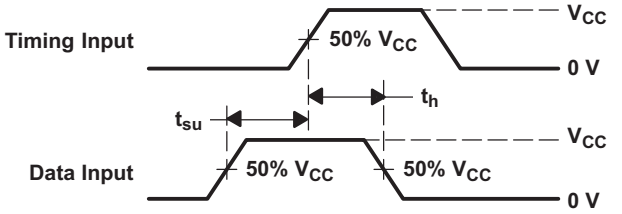


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

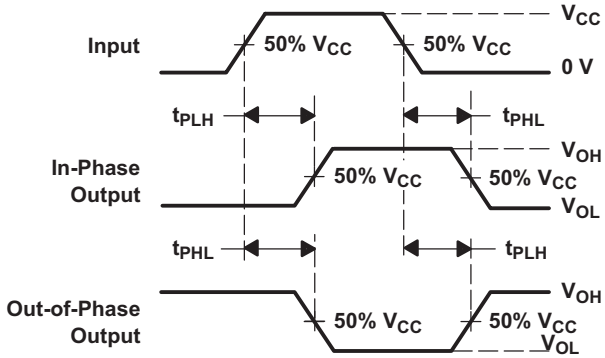
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



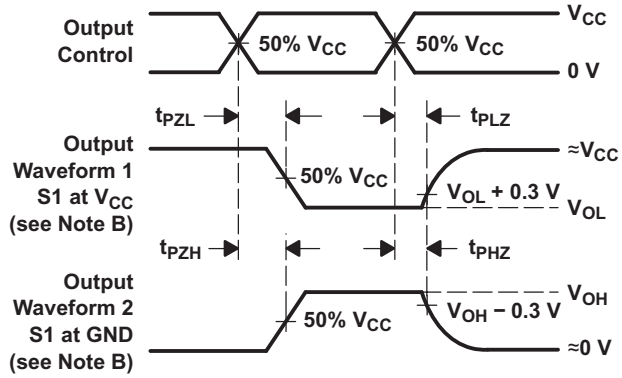
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

9 9
9 1
2
9
3 9
9 T 7 9
9 9
9 9
9 9
9 9

7 9
7 9
1 7 o 50 7 3 7

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

T N74 V541 8 1 + 2 V 595 V V 9

T 4O 1 O 25 7
9 7
9 7 8 9

T 8 8 I 9T I 7
9

8.2 Functional Block Diagram

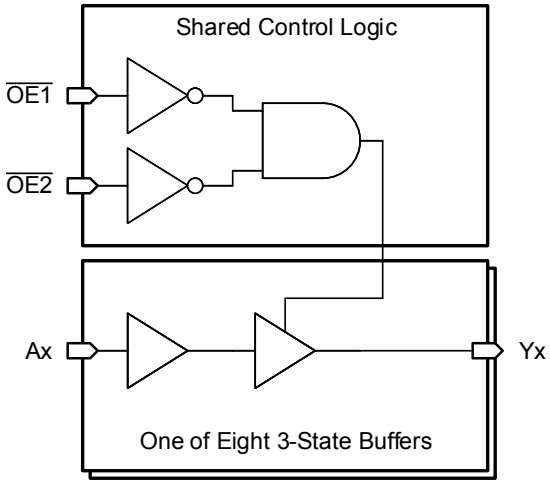


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

T O 38 9 7 7
9T *balanced*
9T 7
9 7
9I
9T *Absolute*
Maximum Ratings 9
8 7 7
Electrical Characteristics 9I 8 7
9I
7 9 8 8
8 9
T 7
9T 7 108 9
U 38 O 9

8.3.2 Partial Power Down (I_{off})

T 0 V9 7
7 9T
I *Electrical Characteristics* 9

ADVANCE INFORMATION

8.3.3 Wettable Flanks

T 9 *Features*
9

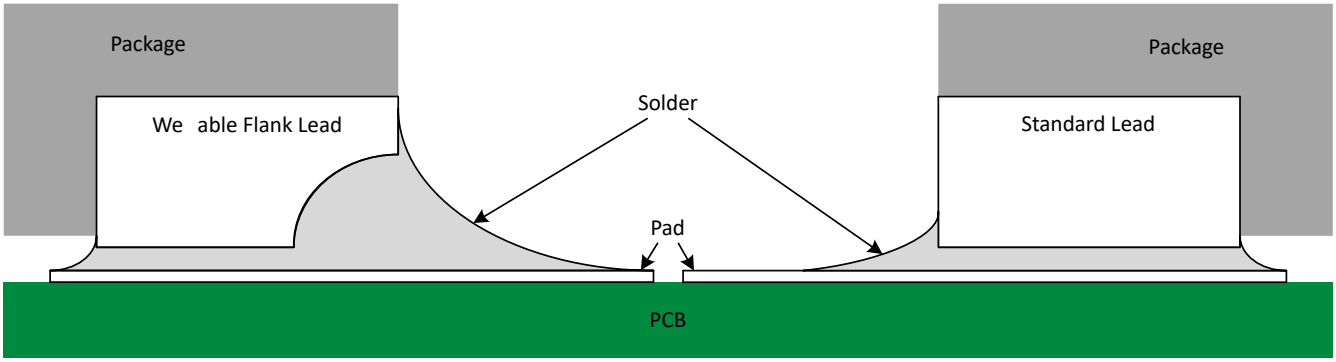


Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

7 N
4 OI59 8827 8
9
9

8.3.4 Clamp Diode Structure

883 9

CAUTION

V *Absolute Maximum Ratings* 8
9T
9

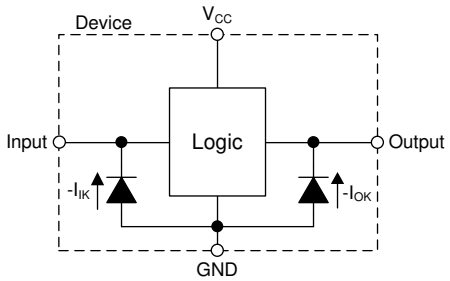


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS[415]			OUTPUT[425]
$\overline{OE1}$	$\overline{OE2}$	A	Y

415 7 7
425 7 7

9 Application and Implementation

Note

I TI 7
TI 9 TI
7
9

9.1 Application Information

T N74 V541 8 1 9I
7 7 7
9T *Application Curve*
9
9

9.2 Typical Application

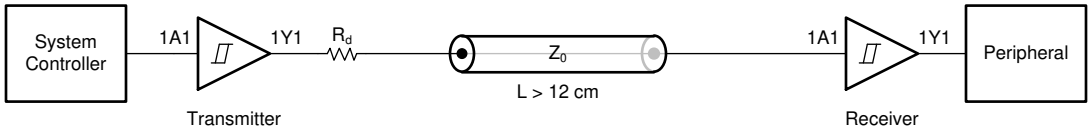


Figure 9-1. Input Expansion with Shift Registers

9.2.1 Power Considerations

*Recommended Operating Conditions*9T
3 *Electrical Characteristics* 9

T
N74 V541 8 1 7 I 7 *Electrical Characteristics*7
9 T
9
V *Absolute Maximum Ratings*9

T
N74 V541 8 1 7I 7 *Electrical Characteristics*7
9T
9 N *Absolute Maximum Ratings*9

T N74 V541 8 1 50
9 7
50 9

T N74 V541 8 1 V_O +I_O7
Electrical Characteristics V_O V_O 9 I 7
V 9

T O
9

T T
4 5 9

ADVANCE INFORMATION

CAUTION

T 7T45 *Absolute Maximum Ratings*7
9 *Absolute Maximum*
*Ratings*9T 9

9.2.2 Input Considerations

I VI45 O 7 VI45 I 9
*Absolute Maximum Ratings*9

U V 9T
7 8 8
7 9 8 I 7 8
O 9T 7 N74 V541 8 1 4
*Electrical Characteristics*57
9 108
9

T N74 V541 8 1 O 7
Recommended Operating Conditions 9 7
7 9

Feature Description 9

9.2.3 Output Considerations

T I 9
VO *Electrical Characteristics*9T
O 9
VO *Electrical Characteristics*9

8 7 7
9T 9

T
9

U 9 V 9

Feature Description 9

ADVANCE INFORMATION

9.2.4 Detailed Design Procedure

19 V N9 T
V N 9 *Layout*
9
29 50 9T 7 7
9 T 7
N74 V541 8 1 9
39 4V $+I_{O45}$ 59 T
Absolute Maximum Ratings 9 O
9
49 T 7 7
7 O
9

9.2.5 Application Curves

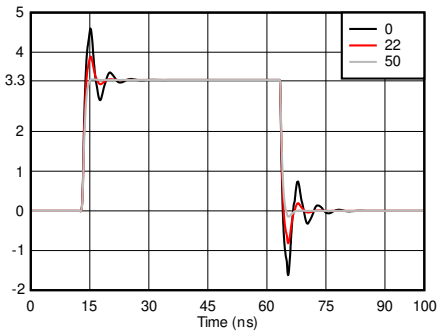


Figure 9-2. Simulated Signal Integrity at the Reciever With Different Damping Resistor (Rd) Values

10 Power Supply Recommendations

T
Absolute Maximum Ratings 9 V
9 7 TI 0918
V 7 TI 0918 0922 8 9
9 091 1
9T
9

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

7 9 I 7
9 8 N 7
3 48 9
9
7
7 9 T
9 7 N V 7
9

11.2 Layout Example

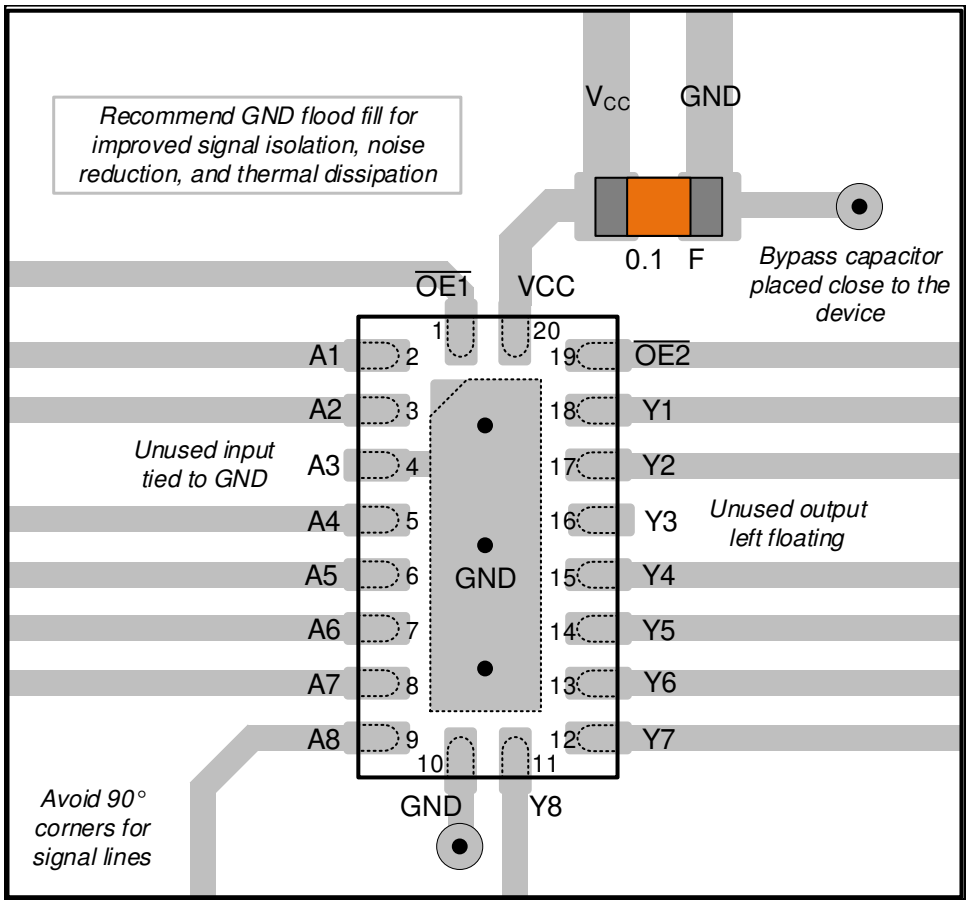


Figure 11-1. Layout Example for the SN74LV541A-Q1 in the WRKS Package

12 Device and Documentation Support

12.1 Related Documentation

7

T I 7*Power-Up Behavior of Clocked Devices*
T I 7*Introduction to Logic*

12.2 Receiving Notification of Documentation Updates

T
9 9I 8 7 *Alert me* 9T
4 59 7
9

12.3 Support Resources

TI 2 3 8 7
9 9
U I U 9T TI
TI3 TI3 T U 9

12.4 Trademarks

TI 2 T I 9
9

12.5 Electrostatic Discharge Caution

T 9T I
9 9
9
9

12.6 Glossary

TI T 7 7 9

13 Mechanical, Packaging, and Orderable Information

T 7 7 9T
9T
9 8 7 8 9

ADVANCE INFORMATION

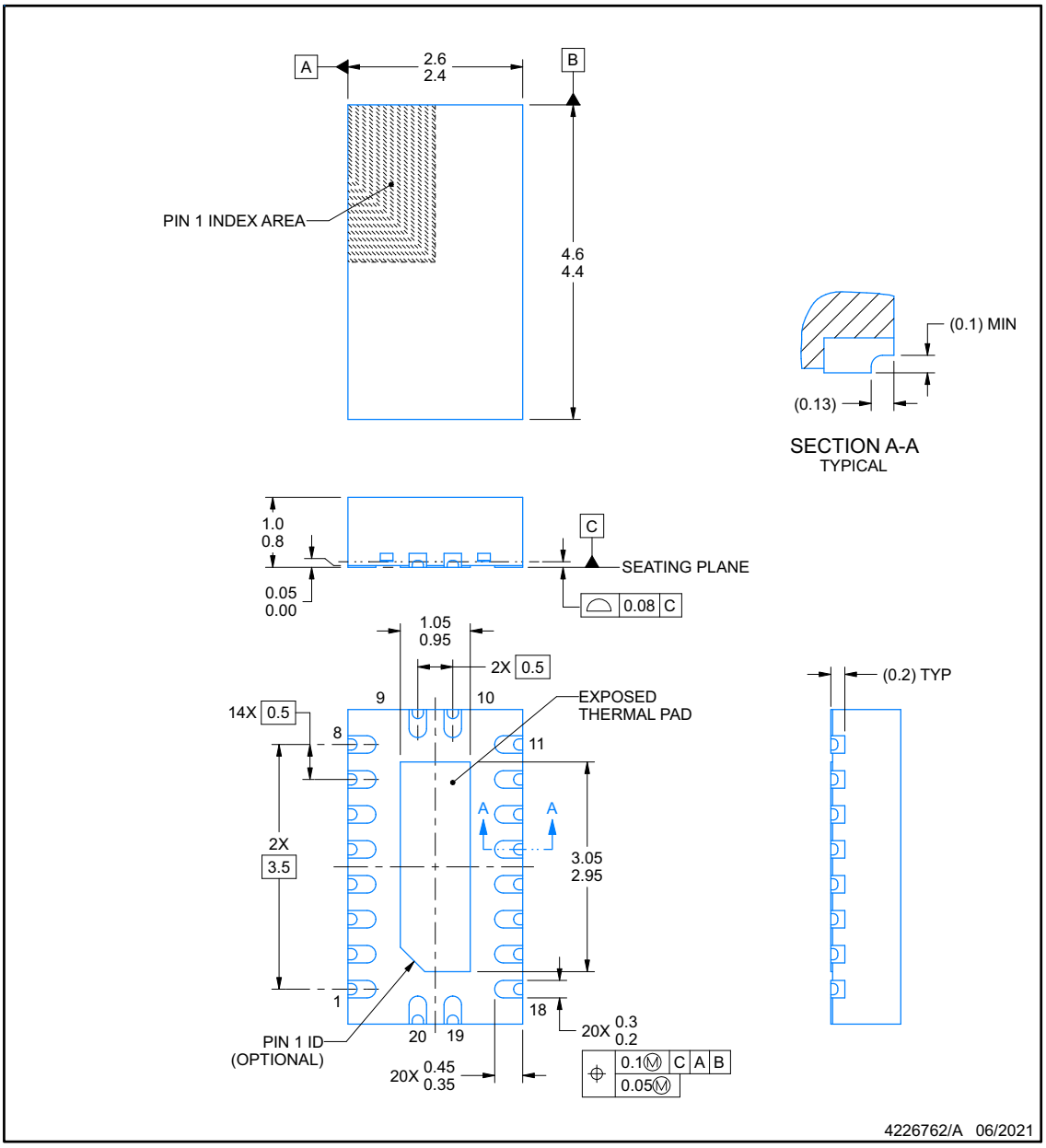
ADVANCE INFORMATION

PACKAGE OUTLINE

RKS0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

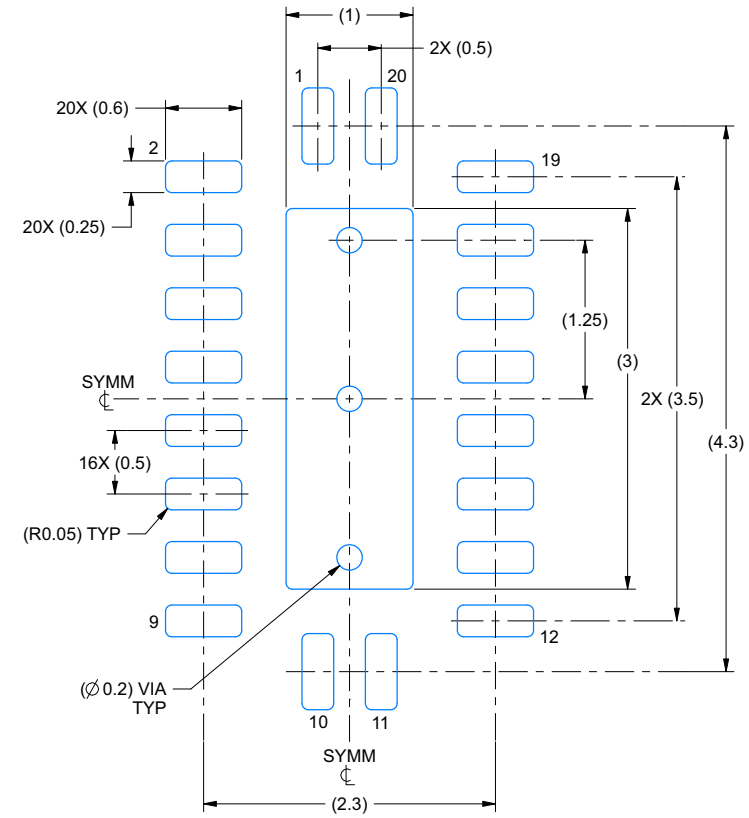
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

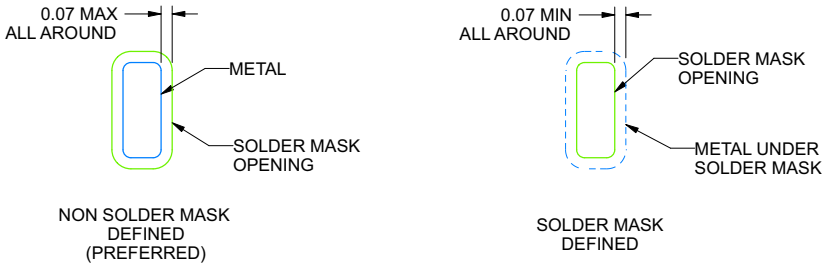
RKS0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4226762/A 06/2021

NOTES: (continued)

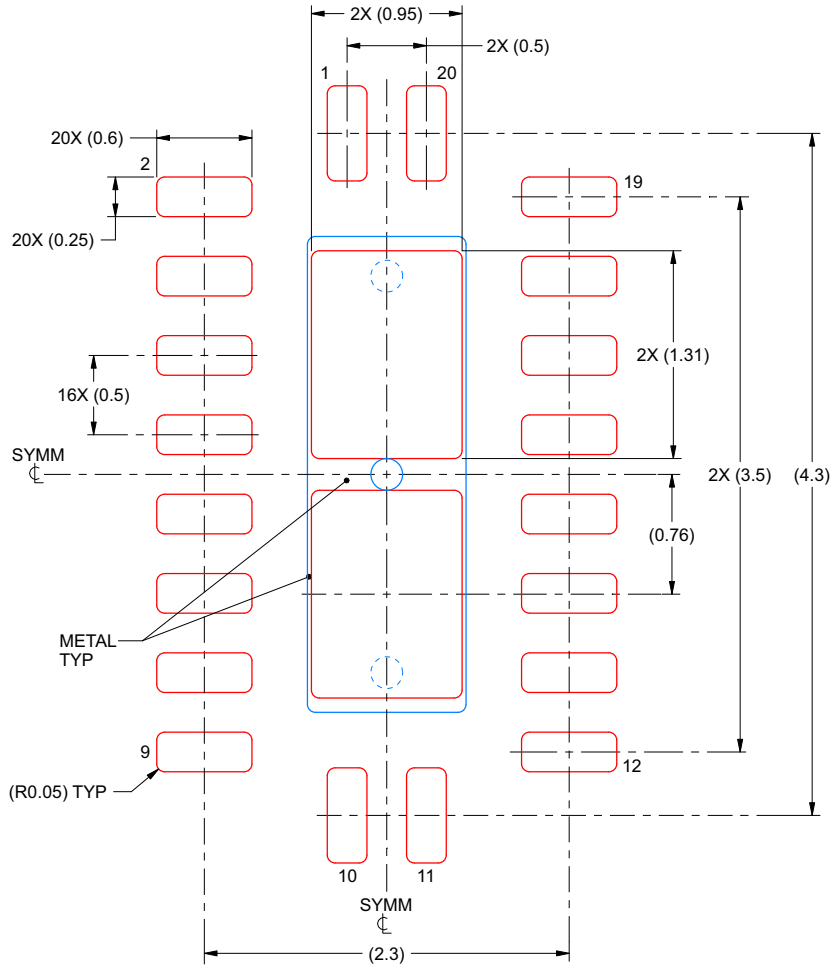
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RKS0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226762/A 06/2021

NOTES: (continued)

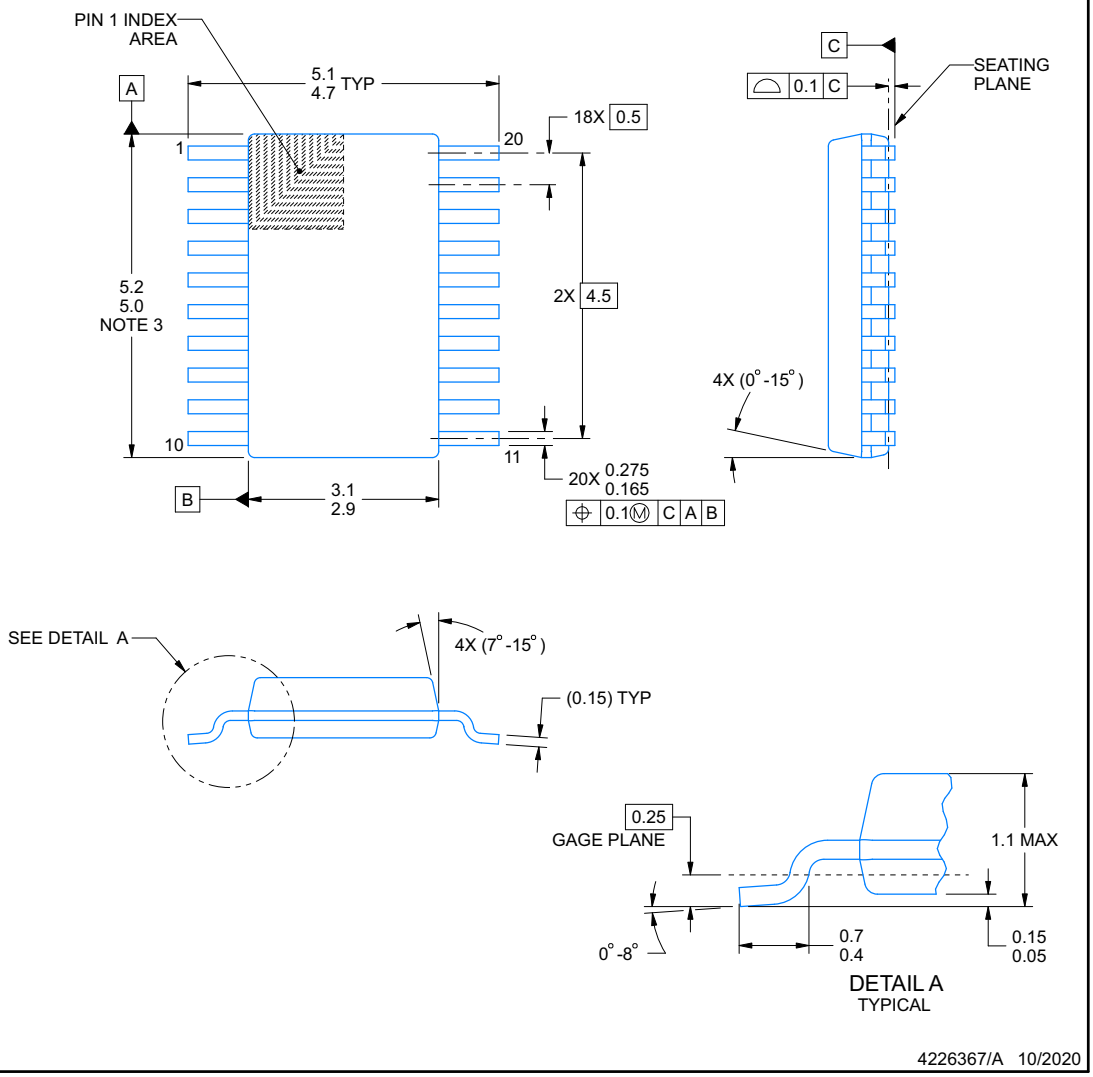
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

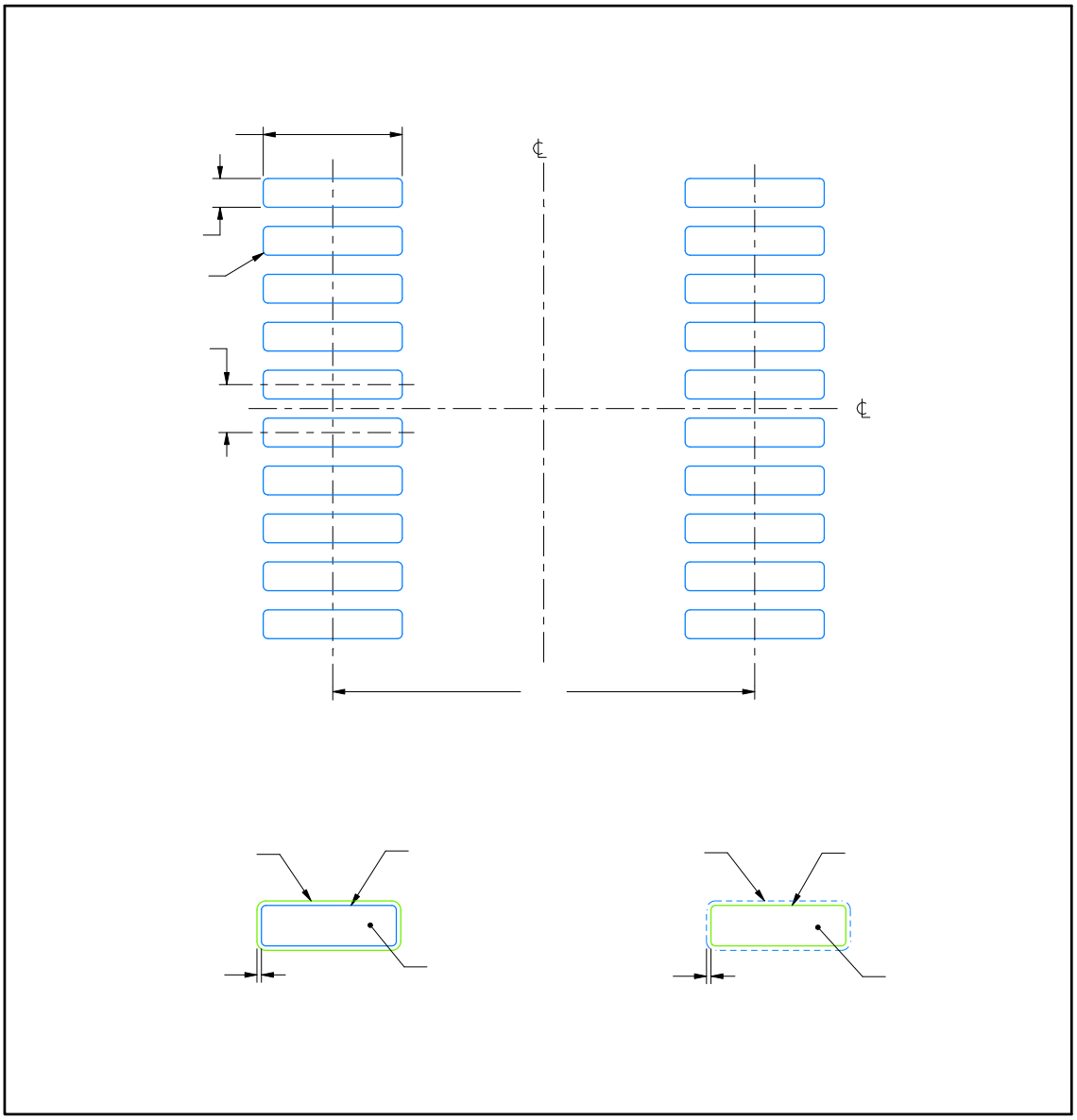
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DGS0020A

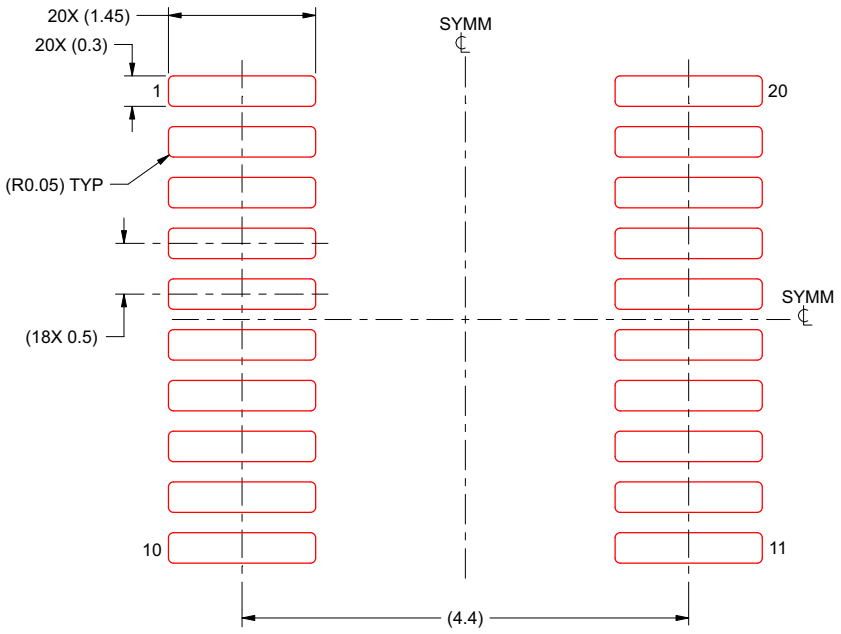
VSSOP - 1.1 mm max height



EXAMPLE STENCIL DESIGN

DGS0020A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

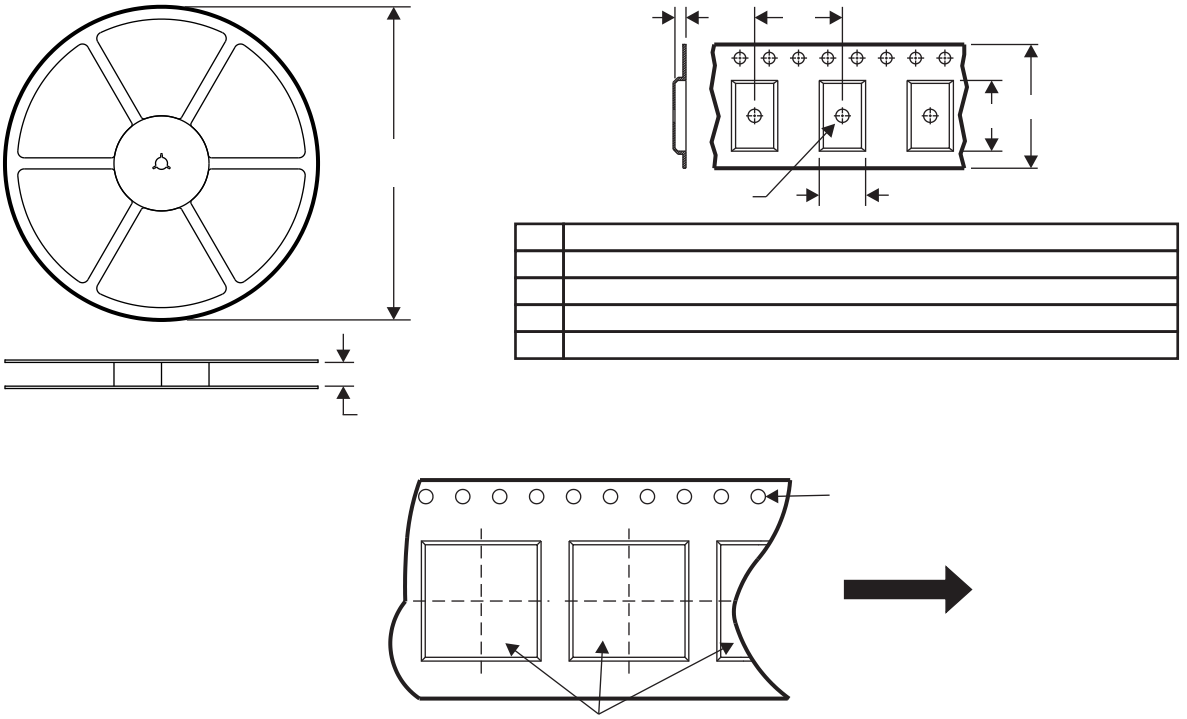
4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

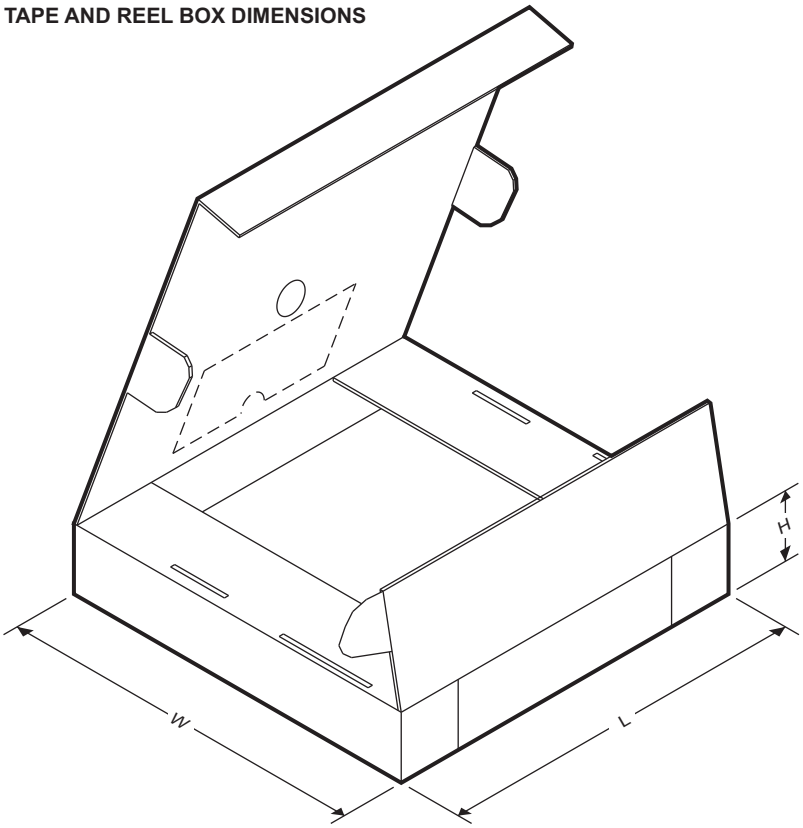
13.1 Tape and Reel Information



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
N74 V541 1	N		20	3000	3309 0	169 4	69 95	79 0	19 4	89 0	169 0	1
N74 V541 1	OT		20	2000	330	169 4	594 0	594 0	194 5	8	16	1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device		Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
N74 V541	1	N		20	3000	2109	185	35
N74 V541	1	OT		20	2000	356	356	35

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCLV541AQWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LV541A-Q1 :

- Catalog : SN74LV541A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

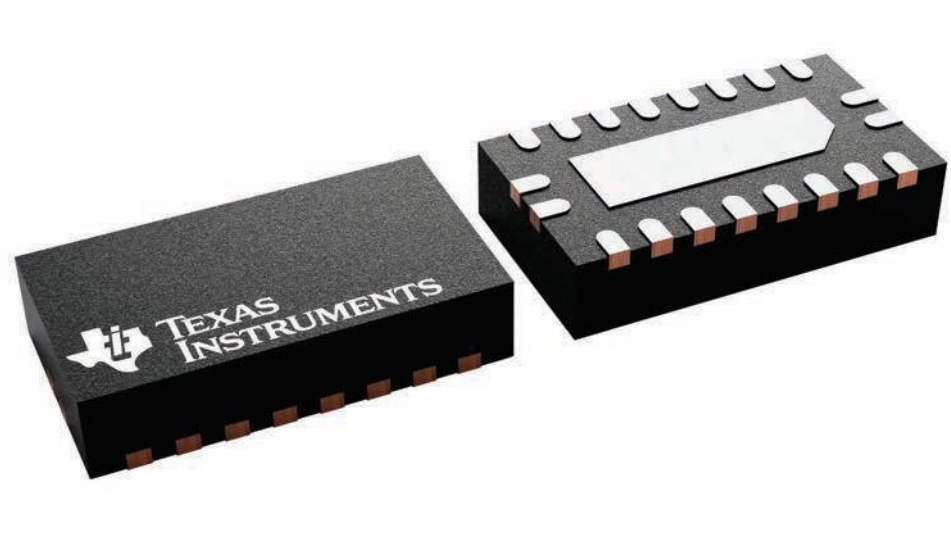
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226872/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265