INA238 85-V, 16-Bit, High-Precision Power Monitor With I²C Interface

1 Features

- High-resolution, 16-bit delta-sigma ADC
- Current monitoring accuracy:
  - Offset voltage: ±5 µV (maximum)
  - Offset drift: ±0.02 µV/°C (maximum)
  - Gain error: ±0.1% (maximum)
  - Gain error drift: ±25 ppm/°C (maximum)
  - Common mode rejection: 140 dB (minimum)
- Power monitoring accuracy:
  - 0.7% full scale, –40°C to +125°C (maximum)
- Fast alert response: 75 µs
- Wide common-mode range: –0.3 V to +85 V
- Bus voltage sense input: 0 V to 85 V
- Shunt full-scale differential range: ±163.84 mV / ±40.96 mV
- Input bias current: 2.5 nA (maximum)
- Temperature sensor: ±1°C (maximum at 25°C)
- Programmable conversion time and averaging
- 2.94-MHz high-speed I²C interface with 16 pin-selectable addresses
- Operates from a 2.7-V to 5.5-V supply:
  - Operational current: 640 µA (typical)
  - Shutdown current: 5 µA (maximum)

2 Applications

- DC/DC converters and power inverters
- Industrial battery packs
- Power-over-ethernet (PoE)
- Telecom equipment
- Enterprise servers

3 Description

The INA238 is an ultra-precise digital power monitor with a 16-bit delta-sigma ADC specifically designed for current-sensing applications. The device can measure a full-scale differential input of ±163.84 mV or ±40.96 mV across a resistive shunt sense element with common-mode voltage support from –0.3 V to +85 V.

The INA238 reports current, bus voltage, temperature, and power, all while performing the needed calculations in the background. The integrated temperature sensor is ±1°C accurate for die temperature measurement and is useful in monitoring the system ambient temperature.

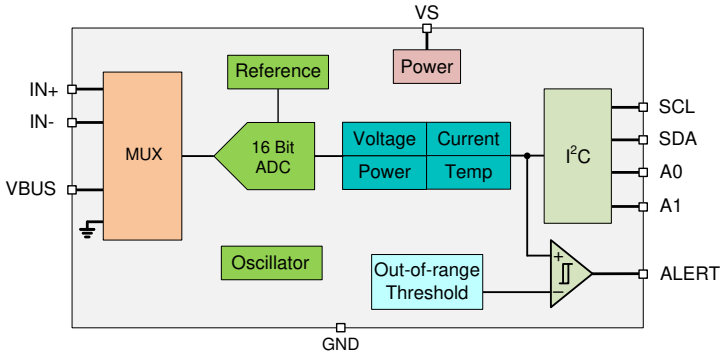
The low offset and gain drift design of the INA238 allows the device to be used in precise systems that do not undergo multi-temperature calibration during manufacturing. Further, the very low offset voltage and noise allow for use in A to kA sensing applications and provide a wide dynamic range without significant power dissipation losses on the sensing shunt element. The low input bias current of the device permits the use of larger current-sense resistors, thus providing accurate current measurements in the micro-amp range.

The device allows for selectable ADC conversion times from 50 µs to 4.12 ms as well as sample averaging from 1x to 1024x, which further helps reduce the noise of the measured data.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA238	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2021) to Revision A (May 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the figures and equations throughput the document to align with the commercial data sheet	1
• Changed Power-supply rejection ratio parameter name to Shunt offset voltage vs power supply in the *Electrical Characteristics* table	5
• Added V_{BUS} offset voltage vs power supply typical values to the *Electrical Characteristics* table	5
• Added register field settings for the typical ADC conversion times.	5
• Changed the Shunt Calibration (SHUNT_CAL) register 14-0 bit name from CURRLSB to SHUNT_CAL	20
• Changed the Device ID (DEVICE_ID) register reset value	20
• Changed the TOL 15-4 bit reset value from 7FF0h to 7FFh	20
• Changed the equation definition list in Equation 1	28

5 Pin Configuration and Functions

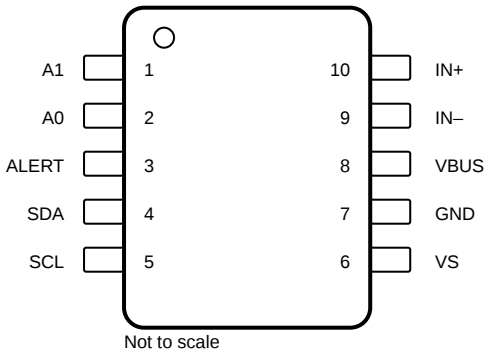


Figure 5-1. DGS Package 10-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	A1	Digital input	I²C address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Digital input	I²C address pin. Connect to GND, SCL, SDA, or VS.
3	ALERT	Digital output	Open-drain alert output, default state is active low.
4	SDA	Digital input/output	Open-drain bidirectional I²C data.
5	SCL	Digital input	I²C clock input.
6	VS	Power supply	Power supply, 2.7 V to 5.5 V.
7	GND	Ground	Ground.
8	VBUS	Analog input	Bus voltage input.
9	IN–	Analog input	Negative input to the device. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
10	IN+	Analog input	Positive input to the device. For high-side applications, connect to power supply side of sense resistor. For low-side applications, connect to load side of sense resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		6	V
V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–40	40	V
	Common-mode	–0.3	85	V
V_{VBUS}		–0.3	85	V
V_{ALERT}	ALERT	–0.3	V_S + 0.3	V
V_{IO}	SDA, SCL	–0.3	6	V
I_{IN}	Input current into any pin		5	mA
I_{OUT}	Digital output current		10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) VIN+ and VIN– are the voltages at the IN+ and IN– pins, respectively.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	–0.3		85	V
V_S	Operating supply range	2.7		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA238 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	97.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = 25 °C, V_S = 3.3 V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0 V, V_{CM} = $V_{IN–}$ = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	T_A = –40°C to +125°C	–0.3		85	V
V_{VBUS}	Bus voltage input range		0		85	V
CMRR	Common-mode rejection	–0.3 V < V_{CM} < 85 V, T_A = –40°C to +125°C	140	160		dB
V_{DIFF}	Shunt voltage input range	T_A = –40°C to +125°C, ADCRANGE = 0	–163.84		163.84	mV
		T_A = –40°C to +125°C, ADCRANGE = 1	–40.96		40.96	mV
V_{os}	Shunt offset voltage	V_{CM} = 48 V		±1.5	±5	µV
		V_{CM} = 0 V		±1.5	±5	µV
dV_{os}/dT	Shunt offset voltage drift	T_A = –40°C to +125°C		±2	±20	nV/°C
PSRR	Shunt offset voltage vs power supply	V_S = 2.7 V to 5.5 V, T_A = –40°C to +125°C		±0.1	±1	µV/V
V_{os_bus}	V_{BUS} offset voltage	V_{BUS} = 20 mV		±1	±5	mV
dV_{os}/dT	V_{BUS} offset voltage drift	T_A = –40°C to +125°C		±4	±40	µV/°C
PSRR	V_{BUS} offset voltage vs power supply	V_S = 2.7 V to 5.5 V		±1.1		mV/V
I_B	Input bias current	Either input, IN+ or IN–, V_{CM} = 85 V		0.1	2.5	nA
Z_{VBUS}	VBUS pin input impedance	Active mode	0.8	1	1.2	MΩ
I_{VBUS}	VBUS pin leakage current	Shutdown mode, V_{BUS} = 85 V		10		nA
R_{DIFF}	Input differential impedance	Active mode, V_{IN+} – $V_{IN–}$ < 164 mV		92		kΩ
DC ACCURACY						
G_{SERR}	Shunt voltage gain error			±0.01	±0.1	%
G_{S_DRFT}	Shunt voltage gain error drift				±25	ppm/°C
G_{BERR}	V_{BUS} voltage gain error			±0.01	±0.1	%
G_{B_DRFT}	V_{BUS} voltage gain error drift				±25	ppm/°C
P_{TME}	Power total measurement error (TME)	T_A = –40°C to +125°C, at full scale			±0.7	%
	ADC resolution			16		Bits
	1 LSB step size	Shunt voltage, ADCRANGE = 0		5		µV
		Shunt voltage, ADCRANGE = 1		1.25		µV
		Bus voltage		3.125		mV
		Temperature		125		m°C
T_{CT}	ADC conversion-time[1]	Conversion time field = 0h		50		µs
		Conversion time field = 1h		84		
		Conversion time field = 2h		150		
		Conversion time field = 3h		280		
		Conversion time field = 4h		540		
		Conversion time field = 5h		1052		
		Conversion time field = 6h		2074		
		Conversion time field = 7h		4120		
INL	Integral Non-Linearity			±2		m%
DNL	Differential Non-Linearity			0.2		LSB
CLOCK SOURCE						
F_{OSC}	Internal oscillator frequency			1		MHz
F_{OSC_TOL}	Internal oscillator frequency tolerance	T_A = 25°C			±0.5	%
		T_A = –40°C to +125°C			±1	%

6.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = 3.3 V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0 V, V_{CM} = $V_{IN–}$ = 48 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR						
	Measurement range		–40		+125	°C
	Temperature accuracy	T_A = 25°C		±0.15	±1	°C
		T_A = –40°C to +125°C		±0.2	±2	°C
POWER SUPPLY						
V_S	Supply voltage		2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 0 V		640	750	µA
		V_{SENSE} = 0 V, T_A = –40°C to +125°C			1.1	mA
I_{QSD}	Quiescent current, shutdown	Shutdown mode		2.8	5	µA
T_{POR}	Device start-up time	Power-up (NPOR)		300		µs
		From shutdown mode		60		
DIGITAL INPUT / OUTPUT						
V_{IH}	Logic input level, high	SDA, SCL	1.2		5.5	V
V_{IL}	Logic input level, low		GND		0.4	V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	GND		0.4	V
I_{IO_LEAK}	Digital leakage input current	0 ≤ V_{IN} ≤ V_S	–1		1	µA

(1) Subject to oscillator accuracy and drift

6.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

6.7 Timing Diagram

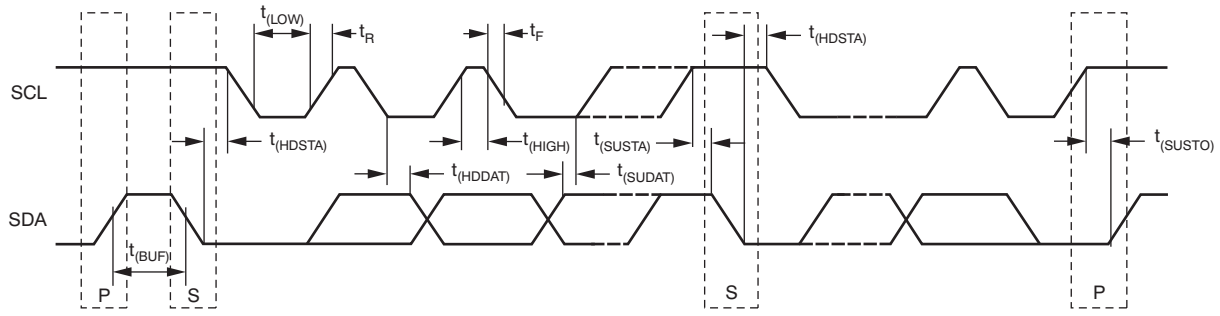
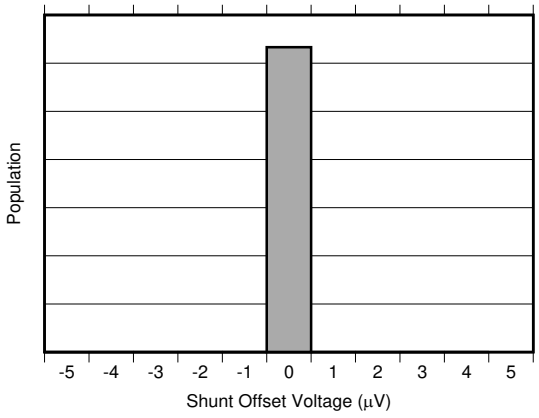


Figure 6-1. I^2C Timing Diagram

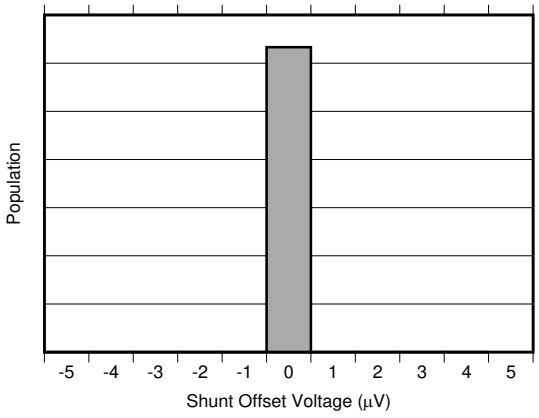
6.8 Typical Characteristics

at T_A = 25 °C, V_{VS} = 3.3 V, V_{CM} = 48 V, V_{SENSE} = 0, and V_{VBUS} = 48 V (unless otherwise noted)



V_{CM} = 48 V

Figure 6-2. Shunt Input Offset Voltage Production Distribution



V_{CM} = 0 V

Figure 6-3. Shunt Input Offset Voltage Production Distribution

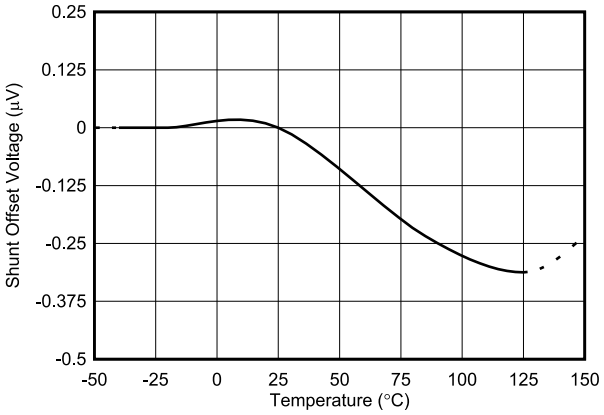


Figure 6-4. Shunt Input Offset Voltage vs. Temperature

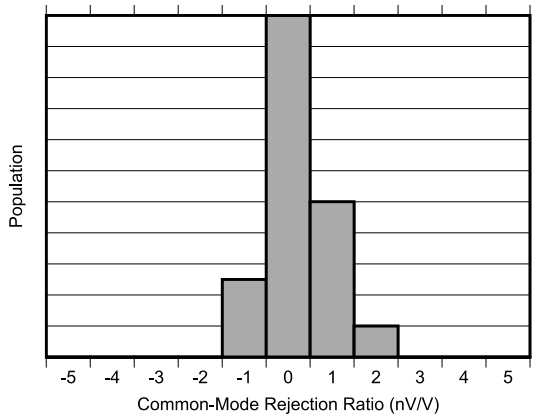


Figure 6-5. Common-Mode Rejection Ratio Production Distribution

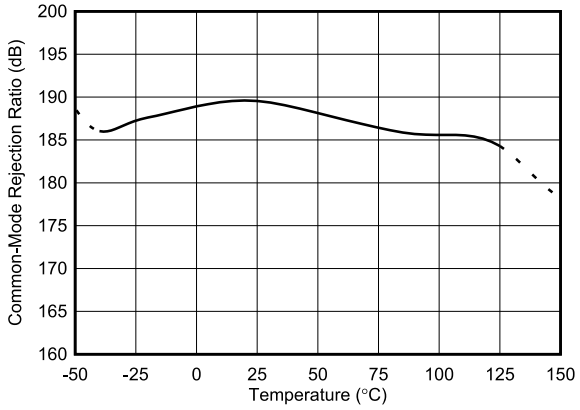
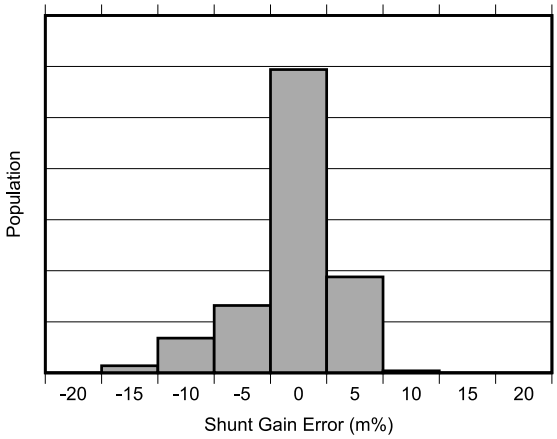


Figure 6-6. Shunt Input Common-Mode Rejection Ratio vs. Temperature

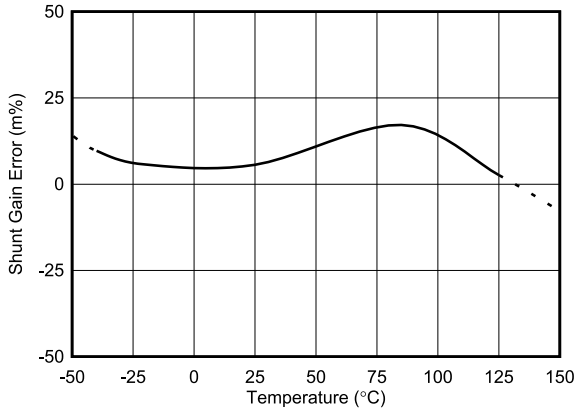


V_{CM} = 24 V

Figure 6-7. Shunt Input Gain Error Production Distribution

6.8 Typical Characteristics (continued)

at T_A = 25 °C, V_{VS} = 3.3 V, V_{CM} = 48 V, V_{SENSE} = 0, and V_{VBUS} = 48 V (unless otherwise noted)



V_{CM} = 24 V

Figure 6-8. Shunt Input Gain Error vs. Temperature

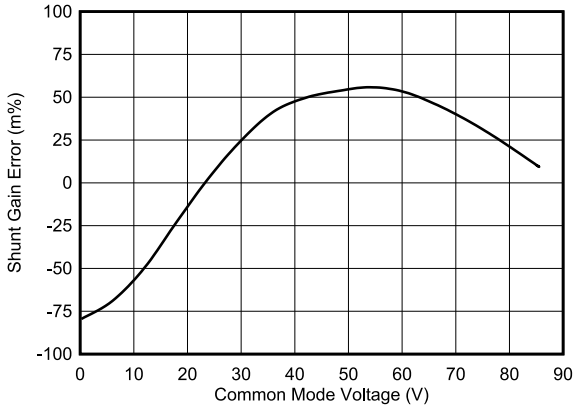
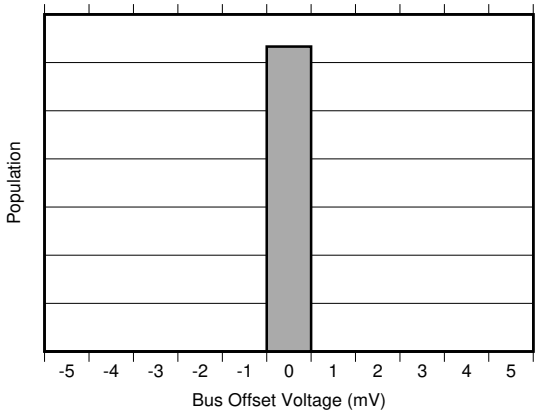
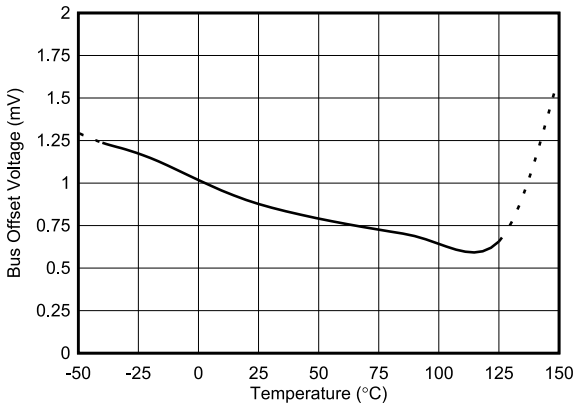


Figure 6-9. Shunt Input Gain Error vs. Common-Mode Voltage



V_{VBUS} = 20 mV

Figure 6-10. Bus Input Offset Voltage Production Distribution



V_{VBUS} = 20 mV

Figure 6-11. Bus Input Offset Voltage vs. Temperature

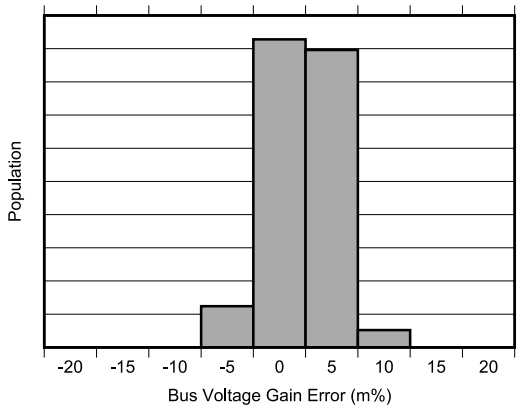


Figure 6-12. Bus Input Gain Error Production Distribution

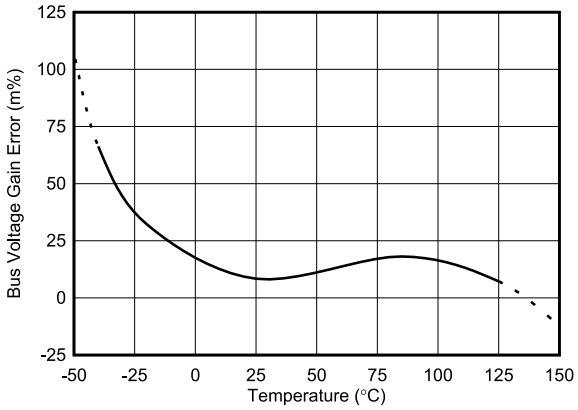


Figure 6-13. Bus Input Gain Error vs. Temperature

6.8 Typical Characteristics (continued)

at T_A = 25 °C, V_{VS} = 3.3 V, V_{CM} = 48 V, V_{SENSE} = 0, and V_{VBUS} = 48 V (unless otherwise noted)

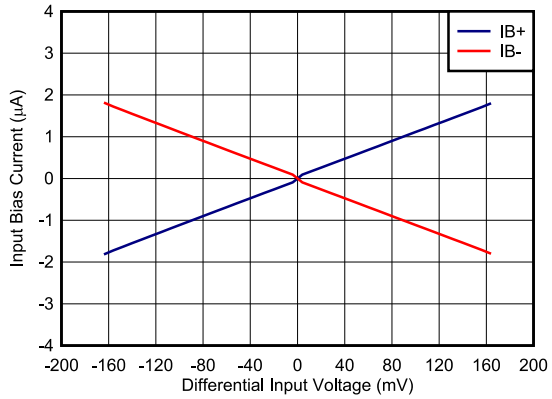


Figure 6-14. Input Bias Current vs. Differential Input Voltage

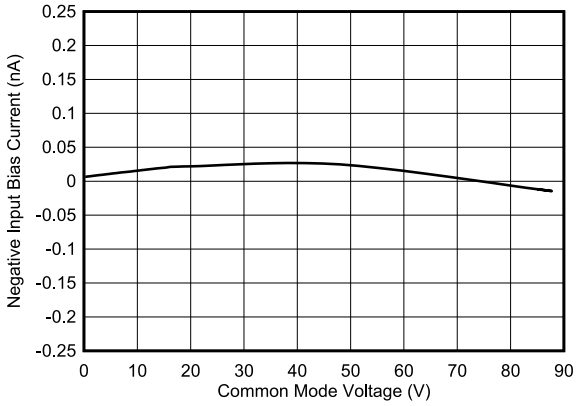


Figure 6-15. Input Bias Current (IB+ or IB–) vs. Common-Mode Voltage

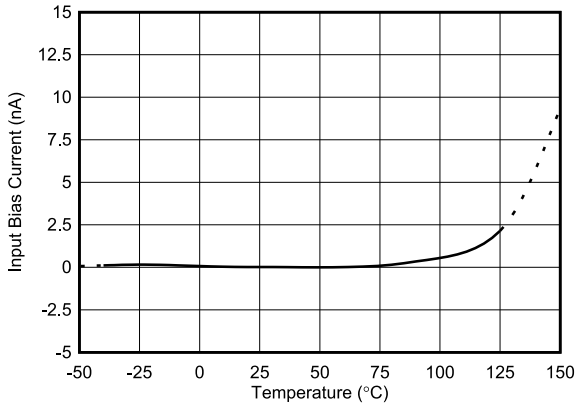


Figure 6-16. Input Bias Current vs. Temperature

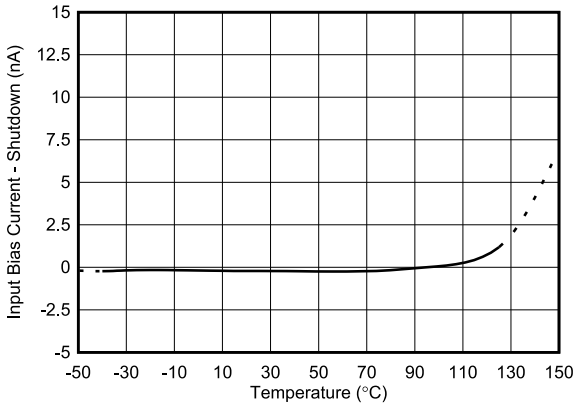


Figure 6-17. Input Bias Current vs. Temperature, Shutdown

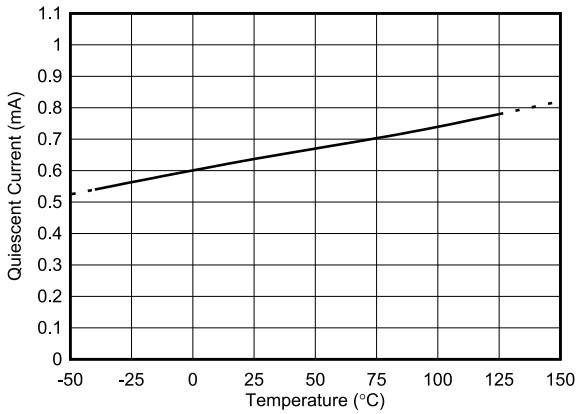


Figure 6-18. Active I_Q vs. Temperature

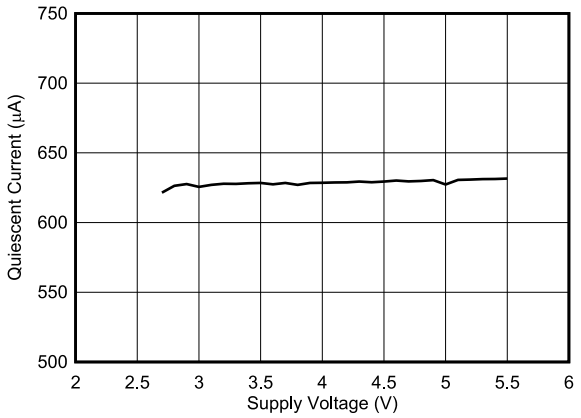


Figure 6-19. Active I_Q vs. Supply Voltage

6.8 Typical Characteristics (continued)

at T_A = 25 °C, V_{VS} = 3.3 V, V_{CM} = 48 V, V_{SENSE} = 0, and V_{VBUS} = 48 V (unless otherwise noted)

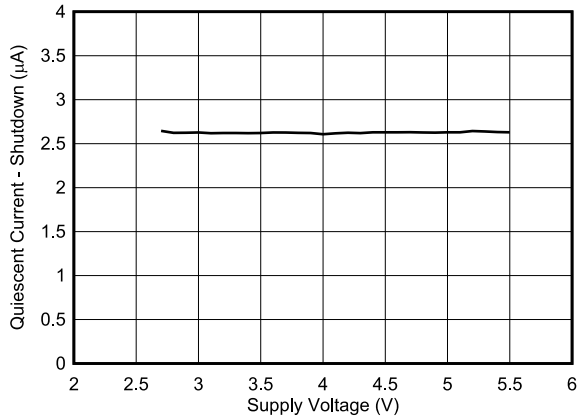


Figure 6-20. Shutdown I_Q vs. Supply Voltage

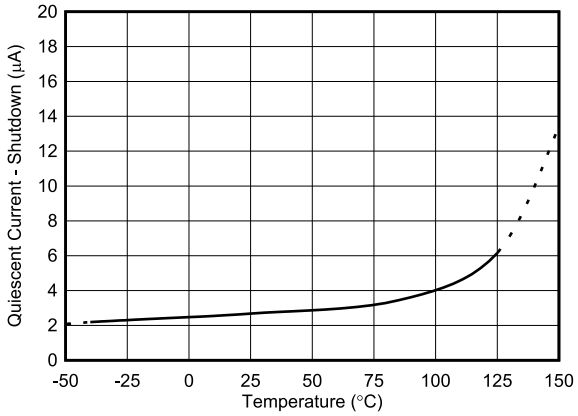


Figure 6-21. Shutdown I_Q vs. Temperature

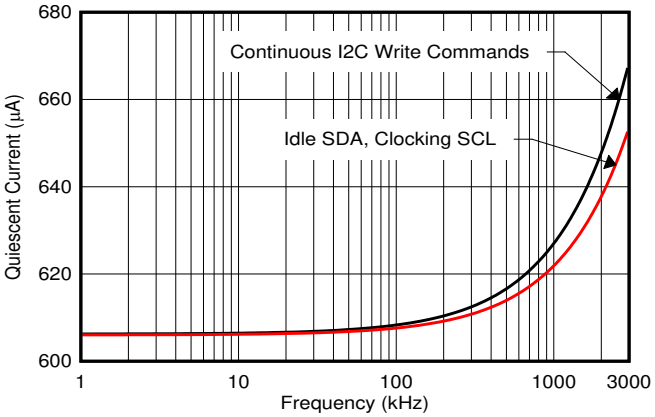


Figure 6-22. Active I_Q vs. Clock Frequency

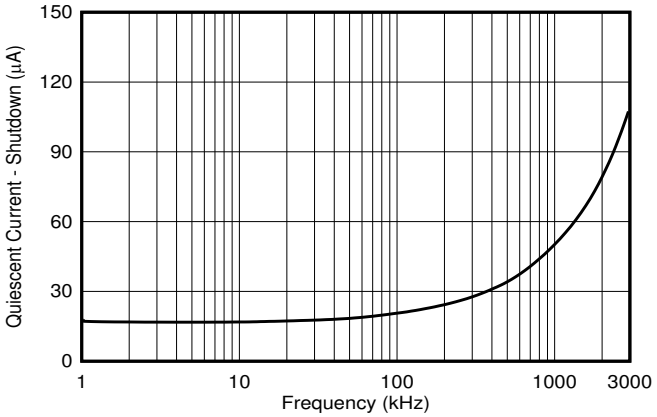


Figure 6-23. Shutdown I_Q vs. Clock Frequency

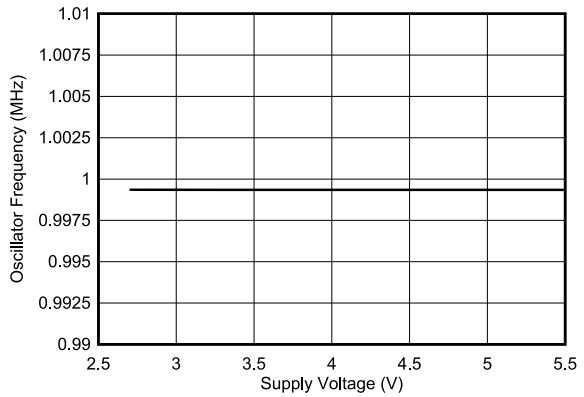


Figure 6-24. Internal Clock Frequency vs. Power Supply

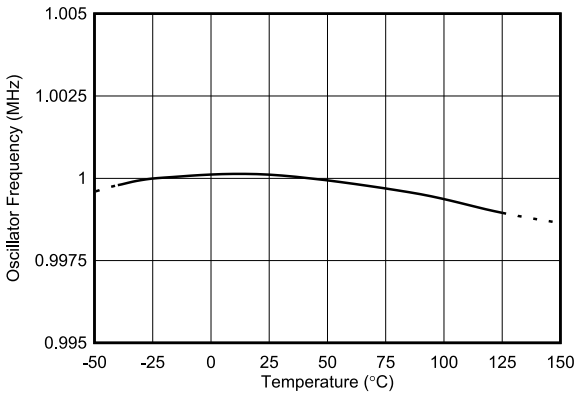


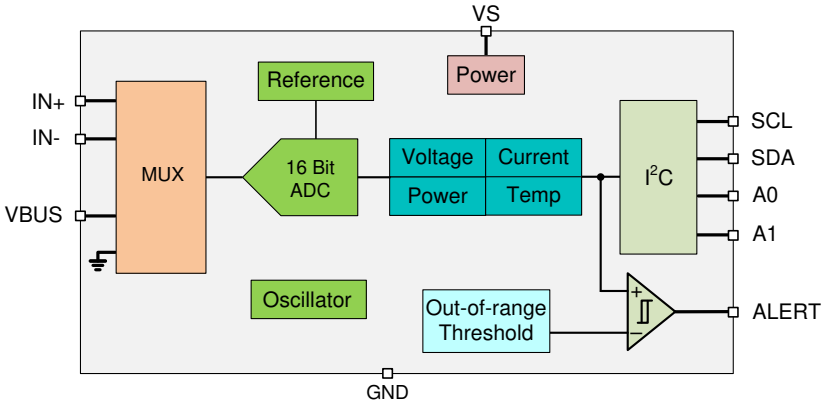
Figure 6-25. Internal Clock Frequency vs. Temperature

7 Detailed Description

7.1 Overview

The INA238 device is a digital current sense amplifier with an I²C digital interface. It measures shunt voltage, bus voltage and internal temperature while calculating current, power necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation. Detailed register information is found in Section 7.6.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Versatile High Voltage Measurement Capability

The INA238 operates off a 2.7 V to 5.5 V supply but can measure voltage and current on rails as high as 85 V. The current is measured by sensing the voltage drop across a external shunt resistor at the IN+ and IN– pins. The input stage of the INA238 is designed such that the input common-mode voltage can be higher than the device supply voltage, V_S. The supported common-mode voltage range at the input pins is –0.3 V to +85 V, which makes the device well suited for both high-side and low-side current measurements. There are no special considerations for power-supply sequencing because the common-mode input range and device supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa without damaging the device.

The device also measures the bus supply voltage through the V_{BUS} pin and temperature through the integrated temperature sensor. The differential shunt voltage is measured between the IN+ and IN– pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0 V to 85 V, while monitored temperatures can range from -40 ºC to +125 ºC.

Shunt voltage, bus voltage, and temperature measurements are multiplexed internally to a single ADC as shown in Figure 7-1.

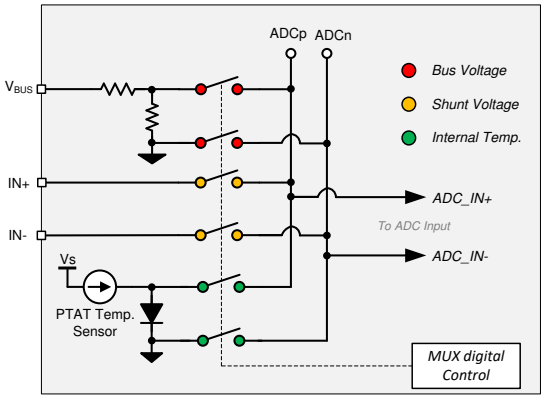


Figure 7-1. High-Voltage Input Multiplexer

7.3.2 Power Calculation

The current and power are calculated after a shunt voltage and bus voltage measurement as shown in Figure 7-2. Power is calculated based on the previous current calculation and the latest bus voltage measurement. If the value loaded into the SHUNT_CAL register is zero, the power value reported is also zero. The current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers where they can then be read. These calculations are performed in the background and do not add to the overall conversion time.

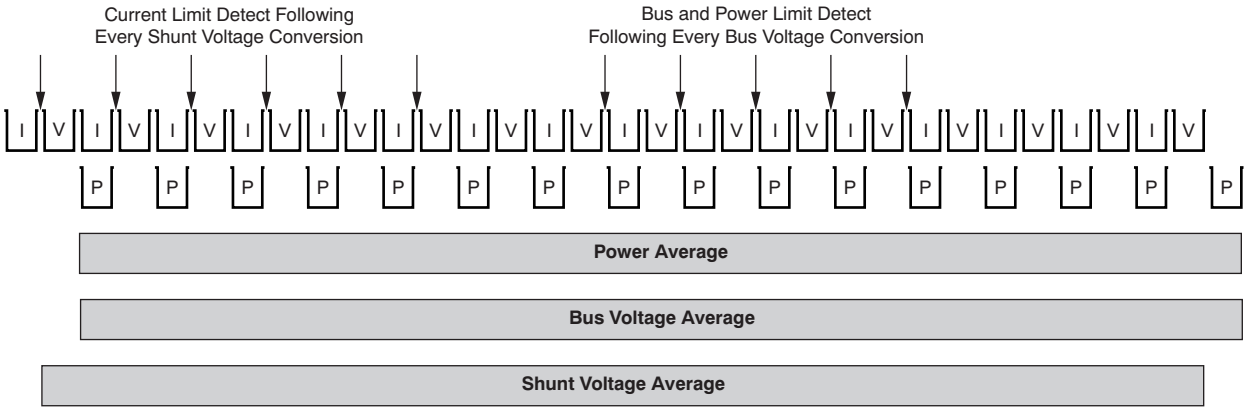


Figure 7-2. Power Calculation Scheme

7.3.3 Low Bias Current

The INA238 features very low input bias current which provides several benefits. The low input bias current of the INA238 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that it allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense amplifiers, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

The bias current in the INA238 is the smallest when the sensed current is zero. As the current starts to increase, the differential voltage drop across the shunt resistor increases which results in an increase in the bias current as shown in Figure 6-14.

7.3.4 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current flow at the shunt voltage measurement channel. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs as shown in Figure 7-1. The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across the common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0-V offset voltage that maximizes the useful dynamic range of the system.

The INA238 can measure the shunt voltage, bus voltage, and die temperature, or a combination of any based on the selected MODE bits setting in the ADC_CONFIG register. This permits selecting modes to convert only the shunt voltage or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. When no averaging is selected, once an ADC conversion is completed, the converted values are independently updated in their corresponding registers where they can be read through the digital interface at the time of conversion end. The conversion time for shunt voltage, bus voltage, and

temperature inputs are set independently from 50 µs to 4.12ms depending on the values programmed in the ADC_CONFIG register. Enabled measurement inputs are converted sequentially so the total time to convert all inputs depends on the conversion time for each input and the number of inputs enabled. When averaging is used, the intermediate values are subsequently stored in an averaging accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging has been completed, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—continuous and triggered—set by the MODE bits in ADC_CONFIG register. In continuous-conversion mode, the ADC will continuously convert the input measurements and update the output registers as described above in an indefinite loop. In triggered-conversion mode, the ADC will convert the input measurements as described above, after which the ADC will go into shutdown mode until another single-shot trigger is generated by writing to the MODE bits. Writing the MODE bits will interrupt and restart triggered or continuous conversions that are in progress. Although the device can be read at any time, and the data from the last conversion remains available, the Conversion Ready flag (CNVRF bit in DIAG_ALRT register) is provided to help coordinate triggered conversions. This bit is set after all conversions and averaging is completed.

The Conversion Ready flag (CNVRF) clears under these conditions:

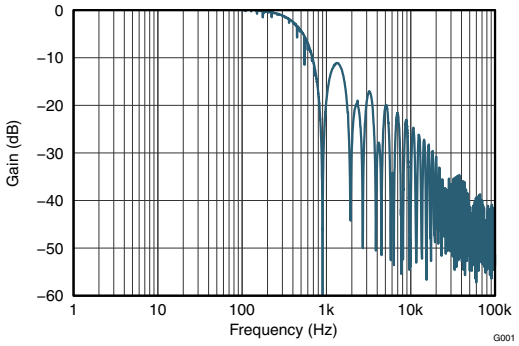
- Writing to the ADC_CONFIG register (except for selecting shutdown mode); or
- Reading the DIAG_ALRT Register

While the INA238 device is used in either one of the conversion modes, a dedicated digital engine is calculating the current and power values in the background as described in Section 7.3.2. All of the calculations are performed in the background and do not contribute to conversion time.

For applications that must synchronize with other components in the system, the INA238 conversion can be delayed by programming the CONVDLY bits in CONFIG register in the range between 0 (no delay) and 510 ms. The resolution in programming the conversion delay is 2 ms. The conversion delay is set to 0 by default. Conversion delay can assist in measurement synchronization when multiple external devices are used for voltage or current monitoring purposes. In applications where an time aligned voltage and current measurements are needed, two devices can be used with the current measurement delayed such that the external voltage and current measurements will occur at approximately the same time. Keep in mind that even though the internal time base for the ADC is precise, synchronization will be lost over time due to internal and external time base mismatch.

7.3.4.1 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods T_{CT} from 50 µs to 4.12 ms. With this configuration the first amplitude notch appears at the Nyquist frequency of the output signal which is determined by the selected conversion time period and defined as f_{NOTCH}= 1 / (2 x T_{CT}). This means that the filter cut-off frequency will scale proportionally with the data output rate as described. Figure 7-3 shows the filter response when the 1.052 ms conversion time period is selected.



Conversion time = 1.052 ms, single conversion only

Figure 7-3. ADC Frequency Response

7.3.4.2 Flexible Conversion Times and Averaging

ADC conversion times for shunt voltage, bus voltage and temperature can be set independently from 50 µs to 4.12 ms. The flexibility in conversion time allows for robust operation in a variety of noisy environments. The device also allows for programmable averaging times from a single conversion all the way to an average of 1024 conversions. The amount of averaging selected applies uniformly to all active measurement inputs. The ADC_CONFIG register shown in Table 7-6 provides additional details on the supported conversion times and averaging modes. The INA238 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages. Figure 7-4 and Figure 7-5 shown below illustrate the effect of conversion time and averaging on a constant input signal.

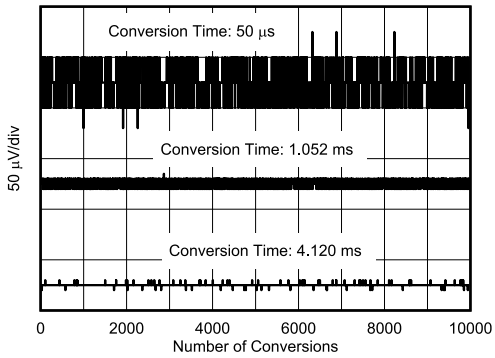


Figure 7-4. Noise vs. Conversion Time (Averaging = 1)

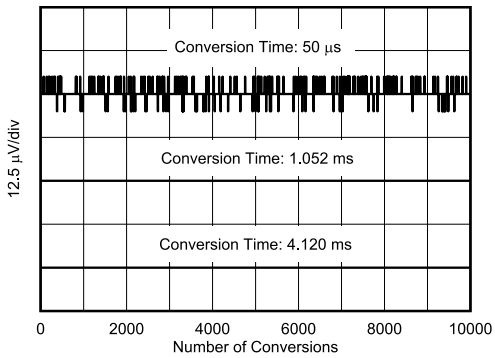


Figure 7-5. Noise vs. Conversion Time (Averaging = 128)

Settings for the conversion time and number of conversions averaged impact the effective measurement resolution. For more detailed information on how averaging reduces noise and increases the effective number of bits (ENOB) see Section 8.1.3.

7.3.5 Integrated Precision Oscillator

The internal timebase of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions. The digital filter response varies with conversion time; therefore, the precise clock ensures filter response and notch frequency consistency across temperature. On power up, the internal oscillator and ADC take roughly 300 µs to reach <1% error stability. Once the clock stabilizes, the ADC data output will be accurate to the electrical specifications provided in Section 6.

7.3.6 Multi-Alert Monitoring and Fault Detection

The INA238 includes a multipurpose, open-drain ALERT output pin that can be used to report multiple diagnostics or as an indicator that the ADC conversion is complete when the device is operating in both triggered and continuous conversion mode. The diagnostics listed in Table 7-1 are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses its associated out-of-range threshold.

Table 7-1. ALERT Diagnostics Description

INA238 DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Shunt Under Voltage Limit	SHNTUL	SUVL	0x8000 h (two's complement)
Shunt Over Voltage Limit	SHNTOL	SOVL	0x7FFF h (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (two's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

A read of the DIAG_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register, shown in Table 7-13, is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert latch enable — In case the ALERT pin is triggered, this function will hold the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG_ALRT register will reset the status of the ALERT pin. This function is enabled by setting the ALATCH bit.
- Conversion ready enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise. However, the diagnostic will be delayed due to the time needed for averaging. This function is enabled by setting the SLOWALERT bit.
- Alert polarity — Allows the device to invert the active state of the ALERT pin. Note that the ALERT pin is an open-drain output that must be pulled-up by a resistor. The ALERT pin is active-low by default and can be configured for active high function using the APOL control bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG_ALRT register:

- Math overflow — Indicated by the MATHOF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit should always read '1' when the device is operating properly.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. Figure 7-6 shows an example where the device reports ADC conversion complete events while the INA238 device is subject to shunt over voltage (over current) event, bus under voltage event, over temperature event and over power-limit event.

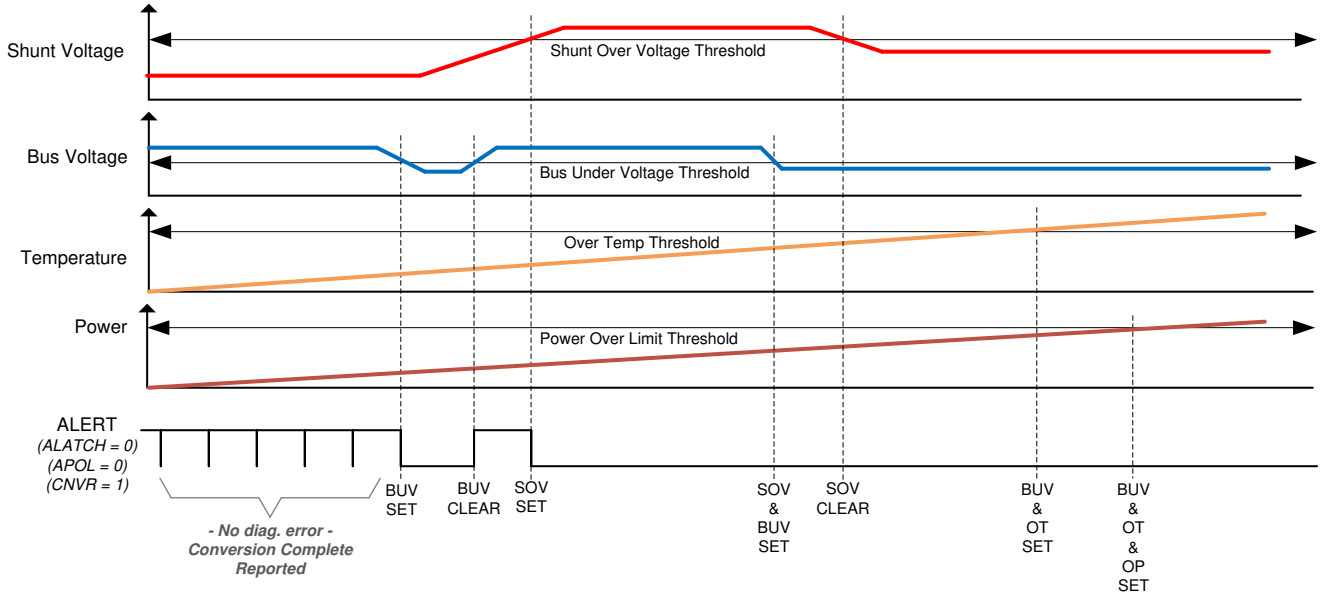


Figure 7-6. Multi-Alert Configuration

7.4 Device Functional Modes

7.4.1 Shutdown Mode

In addition to the two conversion modes (continuous and triggered), the device also has a shutdown mode (selected by the MODE bits in ADC_CONFIG register) that reduces the quiescent current to less than 5 µA and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. The registers of the device can be written to and read from while the device is in shutdown mode. The device remains in shutdown mode until another triggered conversion command or continuous conversion command is received.

The device can be triggered to perform conversions while in shutdown mode. When a conversion is triggered, the ADC will start conversion; once conversion completes the device will return to the shutdown state.

Note that the shutdown current is specified with an inactive communications bus. Active clock and data activity will increase the current consumption as a function of the bus frequency as shown in Figure 6-23.

7.4.2 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 1.26V (typical) at which all of the registers are reset to their default values. A manual device reset can be initiated by setting the RST bit in the CONFIG register. The default power-up register values are shown in the reset column for each register description. Links to the register descriptions are shown in Section 7.6.

7.5 Programming

7.5.1 I²C Serial Interface

The INA238 operates only as a secondary device on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitive coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed-circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA238 supports the transmission protocol for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94 MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA238, the main device must first address secondary devices through a secondary device address byte. The secondary device address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 7-2 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs. When connecting the SDA pin to either A0 or A1 to set the device address, additional hold time of 100 ns is needed on the MSB of the I2C address to insure correct device addressing.

Table 7-2. Address Pins and Secondary Device Addresses

A1	A0	Secondary Device Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

7.5.1.1 Writing to and Reading Through the I²C Serial Interface

Accessing a specific register on the INA238 is accomplished by writing the appropriate value to the register pointer. Refer to Section 7.6 for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 7-9) is the first byte transferred after the secondary device address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

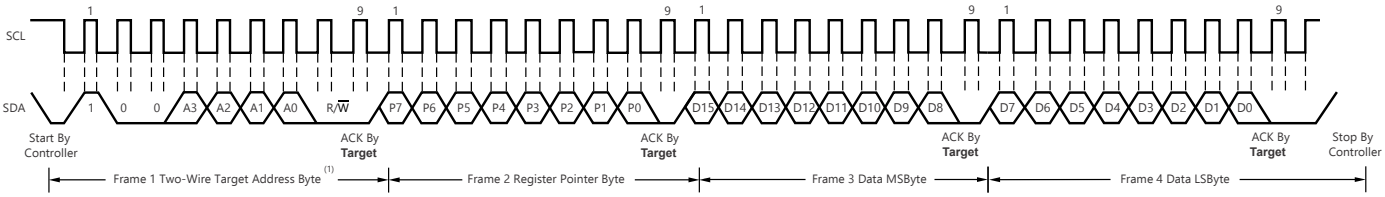
Writing to a register begins with the first byte transmitted by the main device. This byte is the secondary device address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next

byte transmitted by the main device is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The main device may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a secondary device address byte with the R/ $\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The main device then generates a start condition and sends the address byte for the secondary device with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the secondary device and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the main device; then the secondary device transmits the least significant byte. The main device may or may not acknowledge receipt of the second data byte. The main device may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

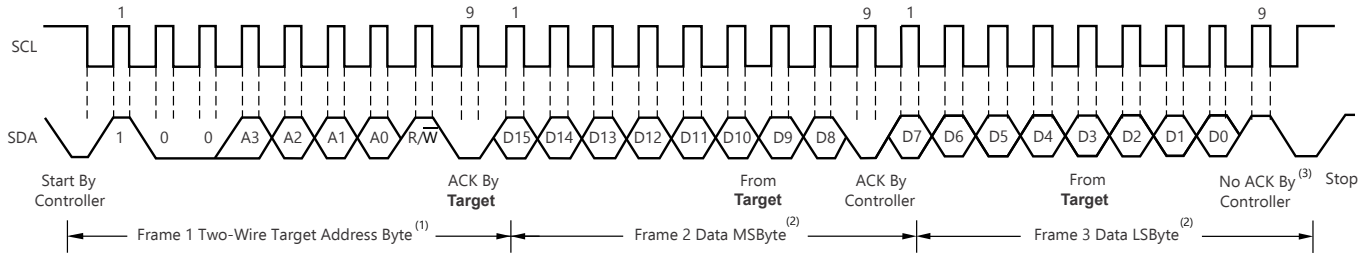
Figure 7-7 shows the write operation timing diagram. Figure 7-8 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers.

Register bytes are sent most-significant byte first, followed by the least significant byte.



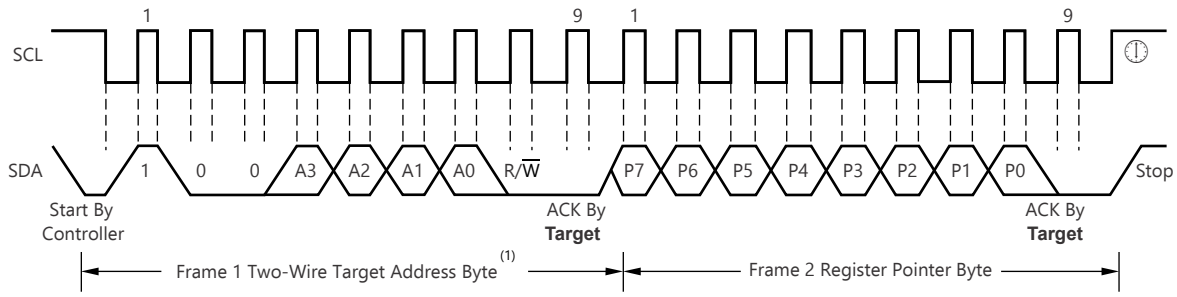
A. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 7-2.
B. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 7-7. Timing Diagram for Write Word Format



A. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 7-2.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 7-9.
C. ACK by the main device can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 7-8. Timing Diagram for Read Word Format



A. The value of the Secondary Device Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 7-2.

Figure 7-9. Typical Register Pointer Set

7.5.1.2 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The main device generates a start condition followed by a valid serial byte containing high-speed (HS) main device code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The device does not acknowledge the HS main device code, but does recognize it and switches its internal filters to support 2.94-MHz operation.

The main device then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

7.5.1.3 SMBus Alert Response

The INA238 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple secondary devices. When an Alert occurs, the main device can broadcast the Alert Response secondary device address (0001 100) with the Read/Write bit set high. Following this Alert Response, any secondary device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until that device wins arbitration.

7.6 Register Maps

7.6.1 INA238 Registers

Table 7-3 lists the INA238 registers. All register locations not listed in Table 7-3 should be considered as reserved locations and the register contents should not be modified.

Table 7-3. INA238 Registers

Address	Acronym	Register Name	Register Size (bits)	Section
0h	CONFIG	Configuration	16	Go
1h	ADC_CONFIG	ADC Configuration	16	Go
2h	SHUNT_CAL	Shunt Calibration	16	Go
4h	VSHUNT	Shunt Voltage Measurement	16	Go
5h	VBUS	Bus Voltage Measurement	16	Go
6h	DIETEMP	Temperature Measurement	16	Go
7h	CURRENT	Current Result	16	Go
8h	POWER	Power Result	24	Go
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16	Go
Ch	SOVL	Shunt Overvoltage Threshold	16	Go

Table 7-3. INA238 Registers (continued)

Address	Acronym	Register Name	Register Size (bits)	Section
Dh	SUVL	Shunt Undervoltage Threshold	16	Go
Eh	BOVL	Bus Overvoltage Threshold	16	Go
Fh	BUVL	Bus Undervoltage Threshold	16	Go
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	Go
11h	PWR_LIMIT	Power Over-Limit Threshold	16	Go
3Eh	MANUFACTURER_ID	Manufacturer ID	16	Go
3Fh	DEVICE_ID	Device ID	16	Go

Complex bit access types are encoded to fit into small table cells. Table 7-4 shows the codes that are used for access types in this section.

Table 7-4. INA238 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 Configuration (CONFIG) Register (Address = 0h) [reset = 0h]

The CONFIG register is shown in Table 7-5.

Return to the Summary Table.

Table 7-5. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RESERVED	R/W	0h	Reserved. Always reads 0.
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2 ms. 0h = 0 s 1h = 2 ms FFh = 510 ms
5	RESERVED	R/W	0h	Reserved. Always reads 0.
4	ADCRANGE	R/W	0h	Shunt full scale range selection across IN+ and IN–. 0h = ±163.84 mV 1h = ± 40.96 mV
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.2 ADC Configuration (ADC_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC_CONFIG register is shown in Table 7-6.

Return to the Summary Table.

Table 7-6. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The user can set the MODE bits for continuous or triggered mode on bus voltage, shunt voltage or temperature measurement. 0h = Shutdown 1h = Triggered bus voltage, single shot 2h = Triggered shunt voltage, single shot 3h = Triggered shunt voltage and bus voltage, single shot 4h = Triggered temperature, single shot 5h = Triggered temperature and bus voltage, single shot 6h = Triggered temperature and shunt voltage, single shot 7h = Triggered bus voltage, shunt voltage and temperature, single shot 8h = Shutdown 9h = Continuous bus voltage only Ah = Continuous shunt voltage only Bh = Continuous shunt and bus voltage Ch = Continuous temperature only Dh = Continuous bus voltage and temperature Eh = Continuous temperature and shunt voltage Fh = Continuous bus voltage, shunt voltage and temperature
11-9	VBUSCT	R/W	5h	Sets the conversion time of the bus voltage measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
8-6	VSHCT	R/W	5h	Sets the conversion time of the shunt voltage measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs
5-3	VTCT	R/W	5h	Sets the conversion time of the temperature measurement: 0h = 50 µs 1h = 84 µs 2h = 150 µs 3h = 280 µs 4h = 540 µs 5h = 1052 µs 6h = 2074 µs 7h = 4120 µs

Table 7-6. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

7.6.1.3 Shunt Calibration (SHUNT_CAL) Register (Address = 2h) [reset = 1000h]

The SHUNT_CAL register is shown in Table 7-7.

Return to the Summary Table.

Table 7-7. SHUNT_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved. Always reads 0.
14-0	SHUNT_CAL	R/W	1000h	The register provides the device with a conversion constant value that represents shunt resistance used to calculate current value in Amperes. This also sets the resolution for the CURRENT register. Value calculation under Section 8.1.2.

7.6.1.4 Shunt Voltage Measurement (VSHUNT) Register (Address = 4h) [reset = 0h]

The VSHUNT register is shown in Table 7-8.

Return to the Summary Table.

Table 7-8. VSHUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0h	Differential voltage measured across the shunt output. Two's complement value. Conversion factor: 5 µV/LSB when ADCRANGE = 0 1.25 µV/LSB when ADCRANGE = 1

7.6.1.5 Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]

The VBUS register is shown in Table 7-9.

Return to the Summary Table.

Table 7-9. VBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 3.125 mV/LSB

7.6.1.6 Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in Table 7-10.

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Table 7-10. DIETEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 125 m°C/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

7.6.1.7 Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in Table 7-11.

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Table 7-11. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Value description under Section 8.1.2.

7.6.1.8 Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in Table 7-12.

Return to the Summary Table.

Table 7-12. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in watts. Unsigned representation. Positive value. Value description under Section 8.1.2.

7.6.1.9 Diagnostic Flags and Alert (DIAG_ALRT) Register (Address = Bh) [reset = 0001h]

The DIAG_ALRT register is shown in Table 7-13.

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Table 7-13. DIAG_ALRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle state when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALRT Register has been read. 0h = Transparent 1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disable conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin

Table 7-13. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SLOWALERT	R/W	0h	When enabled, ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (Active-low, open-drain) 1h = Inverted (active-high, open-drain)
11-10	RESERVED	R	0h	Reserved. Always read 0.
9	MATHOF	R	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. 0h = Normal 1h = Overflow Must be manually cleared by triggering another conversion.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R/W	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Over Temp Event When ALATCH =1 this bit is cleared by reading this register.
6	SHNTOL	R/W	0h	This bit is set to 1 if the shunt voltage measurement exceeds the threshold limit in the shunt over-limit register. 0h = Normal 1h = Over Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
5	SHNTUL	R/W	0h	This bit is set to 1 if the shunt voltage measurement falls below the threshold limit in the shunt under-limit register. 0h = Normal 1h = Under Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
4	BUSOL	R/W	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
3	BUSUL	R/W	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALATCH =1 this bit is cleared by reading this register.
2	POL	R/W	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
1	CNVRF	R/W	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion is complete When ALATCH =1 this bit is cleared by reading this register or starting a new triggered conversion.

Table 7-13. DIAG_ALRT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MEMSTAT	R/W	1h	This bit is set to 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

7.6.1.10 Shunt Overvoltage Threshold (SOVL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered in this register, then a shunt voltage measurement of 0 V will trip this alarm. When using negative values for the shunt under and overvoltage thresholds be aware that the over voltage threshold must be set to the larger (that is, less negative) of the two values. The SOVL register is shown in Table 7-14.

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Table 7-14. SOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Shunt Overvoltage (overcurrent protection). Two's complement value. Conversion Factor: 5 µV/LSB when ADCRANGE = 0 1.25 µV/LSB when ADCRANGE = 1.

7.6.1.11 Shunt Undervoltage Threshold (SUVL) Register (Address = Dh) [reset = 8000h]

The SUVL register is shown in Table 7-15.

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Table 7-15. SUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SUVL	R/W	8000h	Sets the threshold for comparison of the value to detect Shunt Undervoltage (undercurrent protection). Two's complement value. Conversion Factor: 5 µV/LSB when ADCRANGE = 0 1.25 µV/LSB when ADCRANGE = 1.

7.6.1.12 Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in Table 7-16.

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Table 7-16. BOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

7.6.1.13 Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in Table 7-17.

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Table 7-17. BUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.

Table 7-17. BUVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

7.6.1.14 Temperature Over-Limit Threshold (TEMP_LIMIT) Register (Address = 10h) [reset = 7FFFh]

The TEMP_LIMIT register is shown in Table 7-18.

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Table 7-18. TEMP_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	TOL	R/W	7FFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. The value entered in this field compares directly against the value from the DIETEMP register to determine if an over temperature condition exists. Conversion factor: 125 m°C/LSB.
3-0	Reserved	R	0	Reserved, always reads 0

7.6.1.15 Power Over-Limit Threshold (PWR_LIMIT) Register (Address = 11h) [reset = FFFFh]

The PWR_LIMIT register is shown in Table 7-19.

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Table 7-19. PWR_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over power condition exists. Conversion factor: 256 × Power LSB.

7.6.1.16 Manufacturer ID (MANUFACTURER_ID) Register (Address = 3Eh) [reset = 5449h]

The MANUFACTURER_ID register is shown in Table 7-20.

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Table 7-20. MANUFACTURER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5449h	Reads back TI in ASCII.

7.6.1.17 Device ID (DEVICE_ID) Register (Address = 3Fh) [reset = 2381h]

The DEVICE_ID register is shown in Table 7-21.

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Table 7-21. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIEID	R	238h	Stores the device identification bits.
3-0	REV_ID	R	1h	Device revision identification.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Device Measurement Range and Resolution

The INA238 device supports two input ranges for the shunt voltage measurement. The supported full scale differential input across the IN+ and IN– pins can be either ±163.84 mV or ±40.96 mV depending on the ADCRANGE bit in CONFIG register. The range for the bus voltage measurement is from 0 V to 85 V. The internal die temperature sensor range extends from –256 °C to +256 °C but is limited by the package to –40 °C to 125 °C.

Table 8-1 provides a description of full scale voltage on shunt, bus, and temperature measurements, along with their associated step size.

Table 8-1. ADC Full Scale Values

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	±163.84 mV (ADCRANGE = 0)	5 µV/LSB
	±40.96 mV (ADCRANGE = 1)	1.25 µV/LSB
Bus voltage	0 V to 85 V	3.125 mV/LSB
Temperature	–40 °C to +125 °C	125 m°C/LSB

The device shunt voltage measurements, bus voltage, and temperature measurements can be read through the VSHUNT, VBUS, and DIETEMP registers, respectively. The digital output in VSHUNT and VBUS registers is 16-bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in VSHUNT can be positive or negative. The VBUS data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by its respective resolution size. The digital output in the DIETEMP register is 12-bit and can be directly converted to °C by multiplying by the above resolution size. This output value can also be positive or negative.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts as described in Section 8.1.2.

8.1.2 Current and Power Calculations

For the INA238 device to report current values in Ampere units, a constant conversion value must be written in the SHUNT_CAL register that is dependent on the maximum measured current and the shunt resistance used in the application. The SHUNT_CAL register is calculated based on Equation 1. The term CURRENT_LSB is the LSB step size for the CURRENT register where the current in Amperes is stored. The value of CURRENT_LSB is based on the maximum expected current as shown in Equation 2, and it directly defines the resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, it is common to select a higher round-number (no higher than 8x) value for the CURRENT_LSB in order to simplify the conversion of the CURRENT.

The R_{SHUNT} term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use Equation 1 for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT_CAL must be multiplied by 4.

$$SHUNT\_CAL = 819.2 \times 10^6 \times CURRENT\_LSB \times R_{SHUNT} \quad (1)$$

where

- 819.2×10^6 is an internal fixed value used to ensure scaling is maintained properly.
- the value of SHUNT_CAL must be multiplied by 4 for ADCRANGE = 1.

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT_CAL register. If the value loaded into the SHUNT_CAL register is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT_CAL register with the calculated value, the measured current in Amperes can be read from the CURRENT register. The final value is scaled by CURRENT_LSB and calculated in Equation 3:

$$Current\ [A] = CURRENT\_LSB \times CURRENT \quad (3)$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as a 24-bit value and converted to Watts by using Equation 4:

$$Power\ [W] = 0.2 \times CURRENT\_LSB \times POWER \quad (4)$$

where

- POWER is the value read from the POWER register.
- CURRENT_LSB is the lsb size of the current calculation as defined by Equation 2.

For a design example using these equations refer to Section 8.2.2.

8.1.3 ADC Output Data Rate and Noise Performance

The INA238 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The INA238 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

Table 8-2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 50 µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which assures that full noise distribution is taken into consideration.

Table 8-2. INA238 Noise Performance

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	1	0.05	12.5	9.9
84		0.084	12.7	10.5
150		0.15	13.4	11.4
280		0.28	13.7	12.2
540		0.54	14.1	12.4
1052		1.052	14.1	12.7
2074		2.074	15.7	13.1
4120		4.12	15.7	13.4
50	4	0.2	12.7	10.6
84		0.336	13.7	11.4
150		0.6	14.1	12.2
280		1.12	14.7	12.7
540		2.16	15.7	13.4
1052		4.208	15.7	14.1
2074		8.296	15.7	14.7
4120		16.48	15.7	14.7
50	16	0.8	13.7	11.5
84		1.344	15.7	12.7
150		2.4	15.7	13.4
280		4.48	15.7	13.7
540		8.64	15.7	14.1
1052		16.832	15.7	14.7
2074		33.184	15.7	15.7
4120		65.92	16.0	15.7
50	64	3.2	15.7	12.5
84		5.376	15.7	13.7
150		9.6	15.7	14.7
280		17.92	15.7	14.7
540		34.56	16.0	14.7
1052		67.328	16.0	15.7
2074		132.736	16.0	15.7
4120		263.68	16.0	15.7
50	128	6.4	15.7	13.1
84		10.752	15.7	14.1
150		19.2	15.7	14.7
280		35.84	16.0	15.7
540		69.12	16.0	15.7
1052		134.656	16.0	15.7
2074		265.472	16.0	15.7
4120		527.36	16.0	16.0

Table 8-2. INA238 Noise Performance (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	256	12.8	15.7	13.7
84		21.504	15.7	14.7
150		38.4	15.7	15.7
280		71.68	16.0	15.7
540		138.24	16.0	15.7
1052		269.312	16.0	16.0
2074		530.944	16.0	16.0
4120		1054.72	16.0	16.0
50	512	25.6	15.7	14.1
84		43	16.0	15.7
150		76.8	16.0	15.7
280		143.36	16.0	15.7
540		276.48	16.0	15.7
1052		538.624	16.0	16.0
2074		1061.888	16.0	16.0
4120		2109.44	16.0	16.0
50	1024	51.2	15.7	14.7
84		86.016	15.7	15.7
150		153.6	16.0	16.0
280		286.72	16.0	16.0
540		552.96	16.0	16.0
1052		1077.248	16.0	16.0
2074		2123.776	16.0	16.0
4120		4218.88	16.0	16.0

8.1.4 Input Filtering Considerations

As previously discussed, INA238 offers several options for noise filtering by allowing the user to select the conversion times and number of averages independently in the ADC_CONFIG register. The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in monitoring of the power-supply bus.

The internal ADC has good inherent noise rejection; however, the transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating filtering at the input of the device. Filtering high frequency signals enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. For best results, filter using the lowest possible series resistance (typically 100 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 µF and 1 µF. Figure 8-1 shows the device with a filter added at the input.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate ±40 V differential across the IN+ and IN– pins. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 40-V differential or 85-V common-mode absolute maximum rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance. See the *Transient Robustness for Current Shunt Monitors* reference design which describes a high-side current shunt monitor used to measure the voltage developed across a current-sensing resistor when current passes through it.

In applications that do not have large energy storage, electrolytic capacitors on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event. This problem occurs because an excessive dV/dt can activate the ESD protection in the device in systems where large currents are available. Testing demonstrates that the addition of 10-Ω resistors in series with each input of the device sufficiently protects the inputs against this dV/dt failure up to the 40-V maximum differential voltage rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

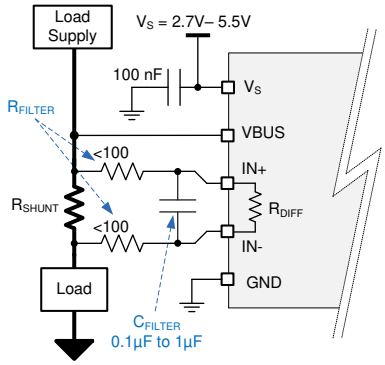


Figure 8-1. Input Filtering

Do not use values greater than 100 ohms for R_{FILTER}. Doing so will degrade gain error and increase non-linearity.

8.2 Typical Application

The low offset voltage and low input bias current of the INA238 allow accurate monitoring of a wide range of currents. To accurately monitor currents with high resolution, select the value of the shunt resistor so that the resulting sense voltage is close to the maximum allowable differential input voltage range (either ±163.84 mV or ±40.96 mV, depending on register settings). The circuit for monitoring currents in a high-side configuration is shown in Figure 8-2.

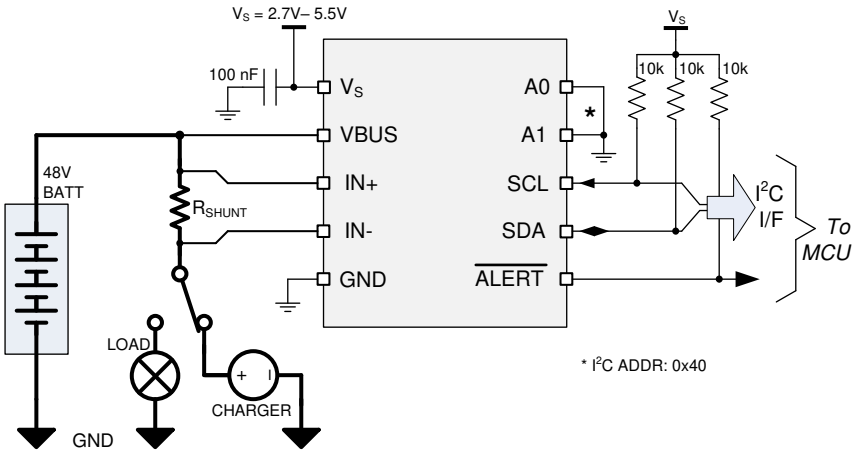


Figure 8-2. INA238 High-Side Sensing Application Diagram

8.2.1 Design Requirements

The INA238 measures the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through it. The device also measures the bus supply voltage and calculates power when calibrated. It also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

The design requirements for the circuit shown in Figure 8-2 are listed in Table 8-3.

Table 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	5 V
Bus supply rail (V_{CM})	48 V
Bus supply rail over voltage fault threshold	52 V
Average Current	6 A
Overcurrent fault threshold (I_{MAX})	10 A
ADC Range Selection (V_{SENSE_MAX})	±163.84 mV
Temperature	25 ºC

8.2.2 Detailed Design Procedure

8.2.2.1 Select the Shunt Resistor

Using values from Table 8-3, the maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed (I_{MAX}) and the maximum allowable sense voltage (V_{SENSE_MAX}) for the chosen ADC range. When operating at the maximum current, the differential input voltage must not exceed the maximum full scale range of the device, V_{SENSE_MAX}. Using Equation 5 for the given design parameters, the maximum value for R_{SHUNT} is calculated to be 16.38 mΩ. The closest standard resistor value that is smaller than the maximum calculated value is 16.2 mΩ. Also keep in mind that R_{SHUNT} must be able to handle the power dissipated across it in the maximum load condition.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \tag{5}$$

8.2.2.2 Configure the Device

The first step to program the INA238 is to properly set the device and ADC configuration registers. On initial power up the CONFIG and ADC_CONFIG registers are set to the reset values as shown in Table 7-5 and Table 7-6. In this default power on state the device is set to measured on the ±163.84 mV range with the ADC continuously converting the shunt voltage, bus voltage, and temperature. If the default power up conditions do not meet the design requirements, these registers will need to be set properly after each V_S power cycle event.

8.2.2.3 Program the Shunt Calibration Register

The shunt calibration register needs to be correctly programmed at each V_S power up in order for the device to properly report any result based on current. The first step in properly setting this register is to calculate the LSB value for the current by using Equation 2. Applying this equation with the maximum expected current of 10 A results in an LSB size of 305.1758 µA. Applying Equation 1 to the CURRENT_LSB and selected value for the shunt resistor results in a shunt calibration register setting of 4050d (FD2h). Failure to set the value of the shunt calibration register will result in a zero value for any result based on current.

8.2.2.4 Set Desired Fault Thresholds

Fault thresholds are set by programming the desired trip threshold into the corresponding fault register. The list of supported fault registers is shown in Table 7-1.

An over current threshold is set by programming the shunt over voltage limit register (SOVL). The voltage that needs to be programmed into this register is calculated by multiplying the over current threshold by the shunt resistor. In this example the over current threshold is 10 A and the value of the current sense resistor is 16.2 mΩ, which give a shunt voltage limit of 162 mV. Once the shunt voltage limit is known, the value for the shunt over voltage limit register is calculated by dividing the shunt voltage limit by the shunt voltage LSB size.

In this example, the calculated value of the shunt over voltage limit register is 162 mV / 5 µV = 32400d (7E90h).

An over voltage fault threshold on the bus voltage is set by programming the bus over voltage limit register (BOVL). In this example the desired over voltage threshold is 52 V. The value that needs to be programmed into this register is calculated by dividing the target threshold voltage by the bus voltage fault limit LSB value of 3.125 mV. For this example, the target value for the BOVL register is 52 V / 3.125 mV = 16640d (4100h).

When setting the power over-limit value, the LSB size used to calculate the value needed in the limit registers will be 256 times greater than the power LSB. This is because the power register is a 24 bits in length while the power fault limit register is 16 bits.

Values stored in the alert limit registers are set to the default values after V_S power cycle events and need to be reprogrammed each time power is applied.

8.2.2.5 Calculate Returned Values

Parametric values are calculated by multiplying the returned value by the LSB value. Table 8-4 below shows the returned values for this application example assuming the design requirements shown in Table 8-3.

Table 8-4. Calculating Returned Values

PARAMETER	Returned Value	LSB Value	Calculated Value
Shunt voltage (V)	19440d	5 µV/LSB	0.0972 V
Current (A)	19660d	10 A/2^{15} = 305.176 µA/LSB	5.9997 A
Bus voltage (V)	15360d	3.125 mV/LSB	48 V
Power (W)	4718604d	Current LSB x 0.2 = 61.035156 µW/LSB	288 W
Temperature (°C)	200d	125 m°C/LSB	25°C

Shunt Voltage, Current, Bus Voltage (positive only), and Temperature return values in two's complement format. In two's complement format a negative value in binary is represented by having a 1 in the most significant bit of the returned value. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value should then be converted to decimal with the negative sign applied. For example, assume a shunt voltage reading returns 1011 0100 0001 0000. This is a negative value due to the MSB having a value of one. Inverting the bits and adding one results in 0100 1011 1111 0000 (19440d) which from the shunt voltage example in Table 8-4 correlates to a voltage of 97.2 mV. Since the returned value was negative the measured shunt voltage value is -97.2 mV.

8.2.3 Application Curves

Figure 8-3 and Figure 8-4 show the ALERT pin response to a bus overvoltage fault with a conversion time of 50 µs, averaging set to 1, and the SLOWALERT bit set to 0 for bus only conversions. For these scope shots, persistence was enabled on the ALERT channel to show the variation in the alert response for many sequential fault events. If the magnitude of the fault is sufficient the ALERT response can be as fast as one quarter of the ADC conversion time as shown in Figure 8-3. For fault conditions that are just exceeding the limit threshold, the response time for the ALERT pin can vary from approximately 0.5 to 1.5 conversion cycles as shown in Figure 8-4. Variation in the alert response exists because the external fault event is not synchronized to the internal ADC conversion start. Also the ADC is constantly sampling to get a result, so the response time for fault events starting from zero will slower than fault events starting from values near the set fault threshold. Since the timing of the alert can be difficult to predict, applications where the alert timing is critical should assume a alert response equal to 1.5 times the ADC conversion time for bus voltage or shunt voltage only conversions.

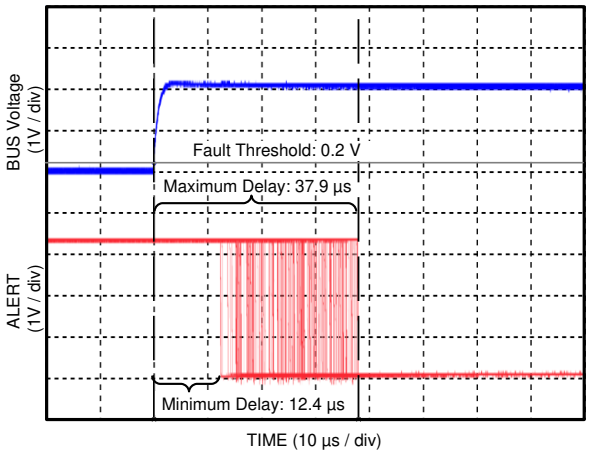


Figure 8-3. Alert Response Time (Sampled Values Significantly Above Threshold)

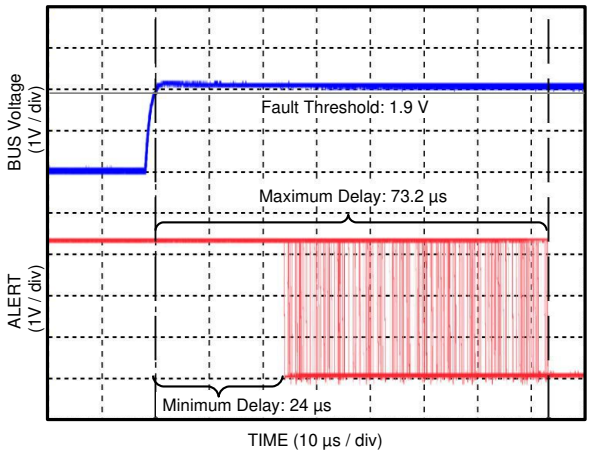


Figure 8-4. Alert Response Time (Sampled Values Slightly Above Threshold)

9 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power-supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 85 V. Note that the device can also withstand the full 0 V to 85 V range at the input terminals, regardless of whether the device has power applied or not. Avoid applications where the GND pin is disconnected while device is actively powered.

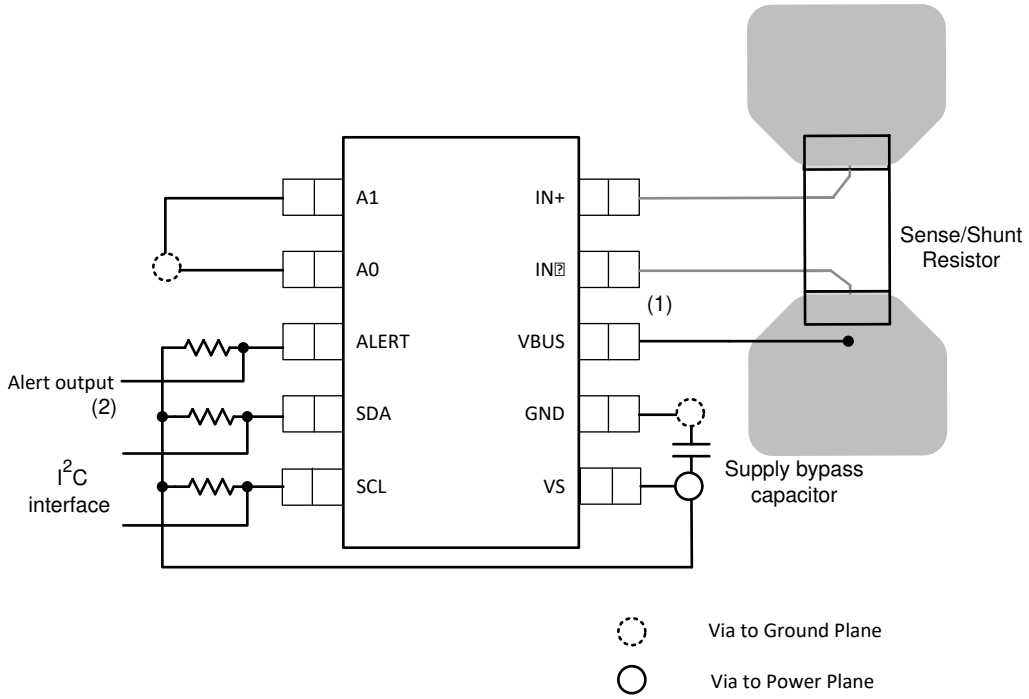
Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is sensed between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

10.2 Layout Example



(1) Connect the VBUS pin to the voltage powering the load for load power calculations..
(2) Can be left floating if unused.

Figure 10-1. INA238 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA238AIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	238I	Samples
INA238AIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	238I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA238 :

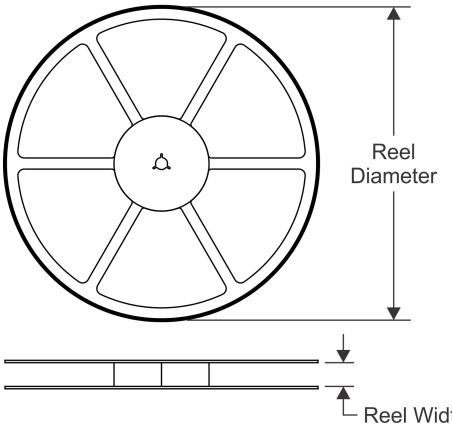
- Automotive : INA238-Q1

NOTE: Qualified Version Definitions:

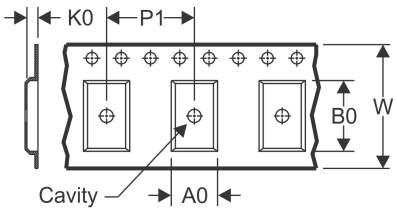
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

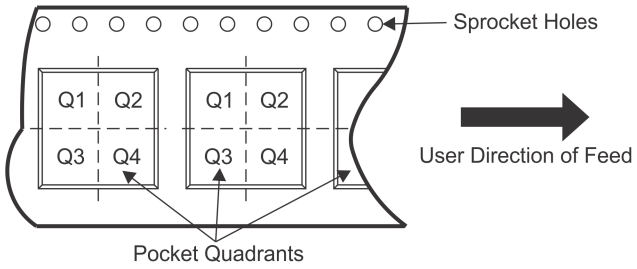


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

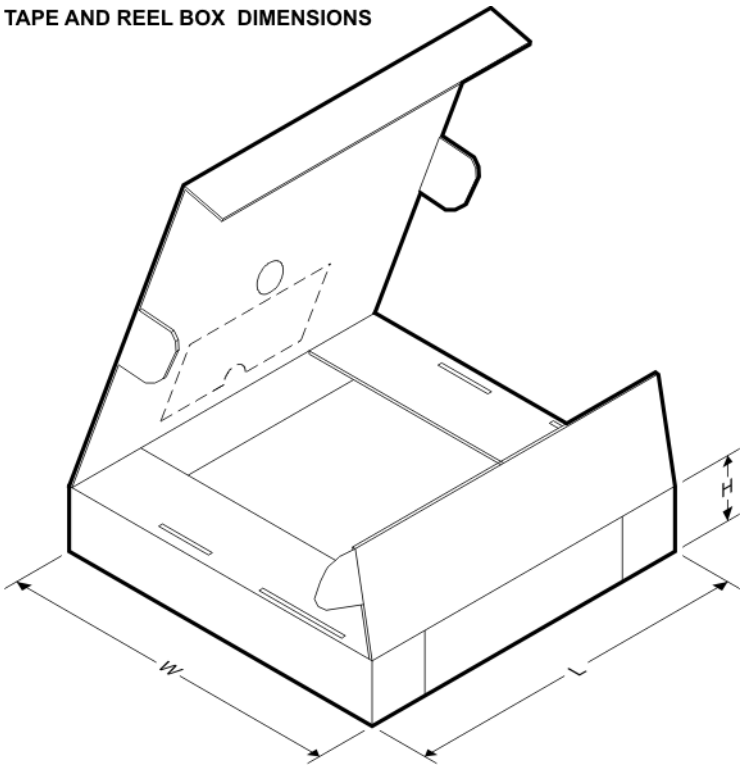
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA238AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA238AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

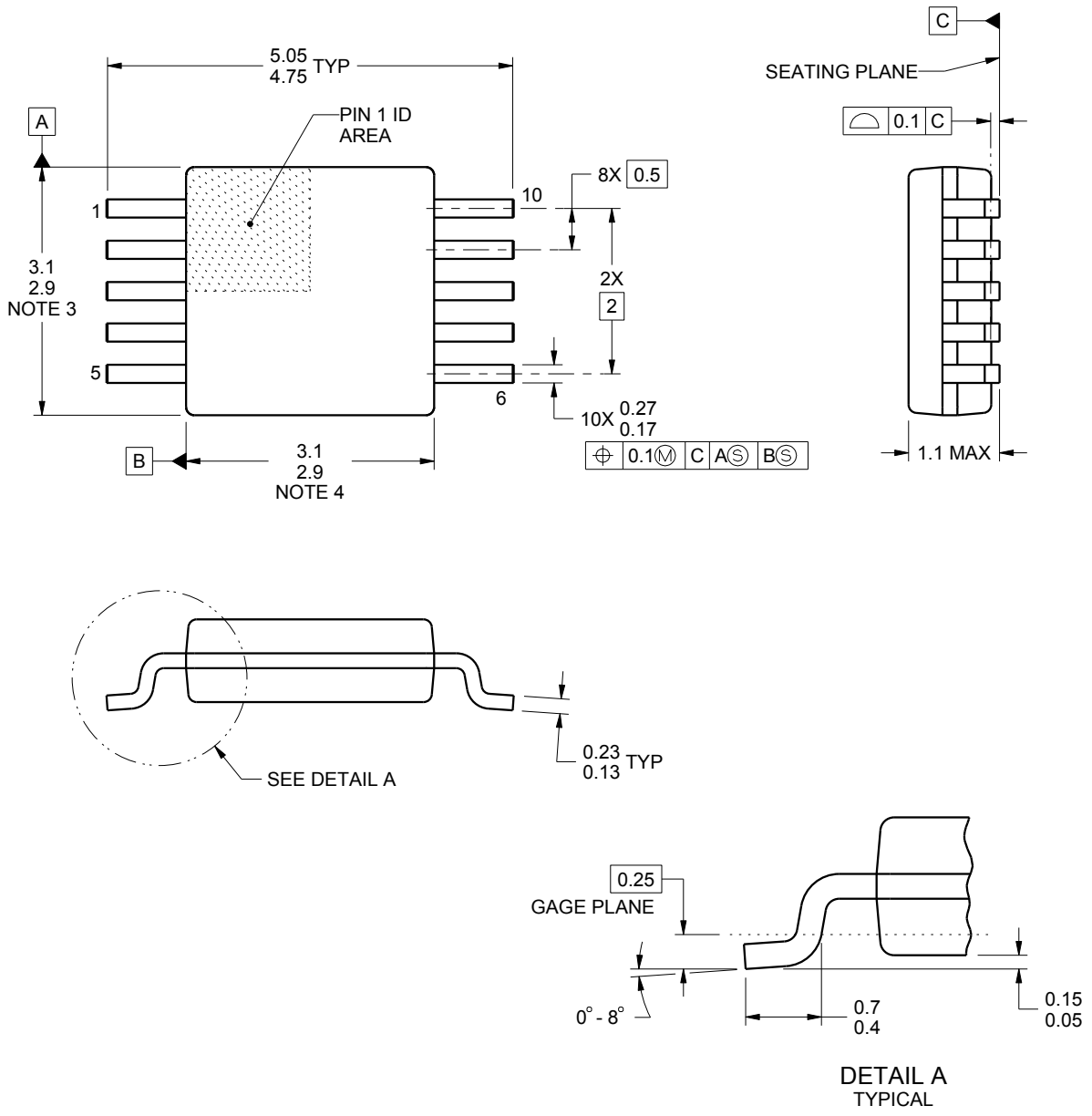
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA238AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA238AIDGST	VSSOP	DGS	10	250	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

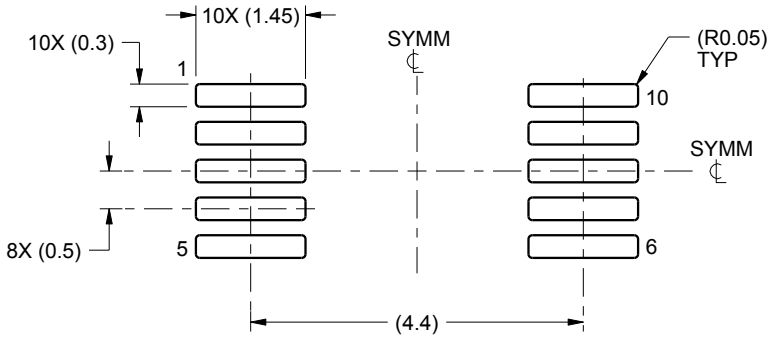
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

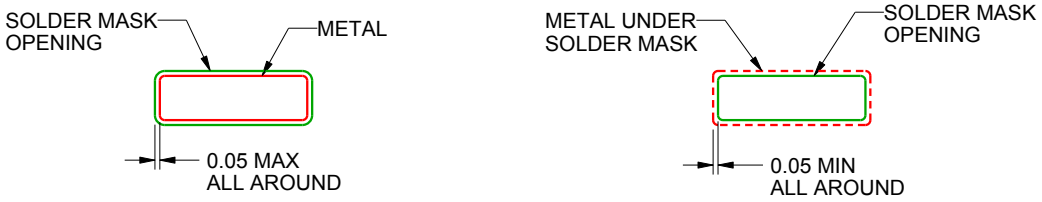


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

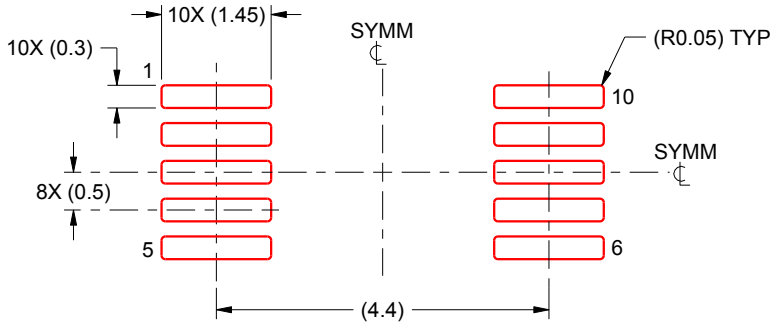


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

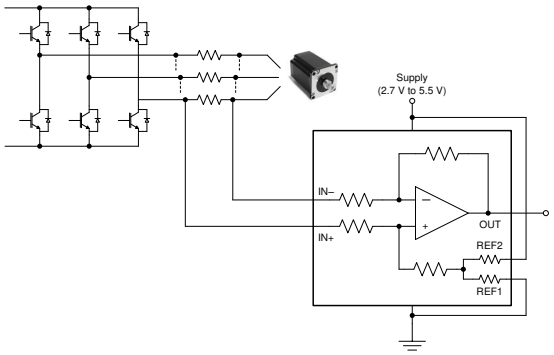
INA240 –4-V to 80-V, Bidirectional, Ultra-Precise Current Sense Amplifier With Enhanced PWM Rejection

1 Features

- Enhanced PWM Rejection
- Excellent CMRR:
  - 132-dB DC CMRR
  - 93-dB AC CMRR at 50 kHz
- Wide Common-Mode Range: –4 V to 80 V
- Accuracy:
  - Gain:
    - Gain Error: 0.20% (Maximum)
    - Gain Drift: 2.5 ppm/°C (Maximum)
  - Offset:
    - Offset Voltage: ±25 µV (Maximum)
    - Offset Drift: 250 nV/°C (Maximum)
- Available Gains:
  - INA240A1: 20 V/V
  - INA240A2: 50 V/V
  - INA240A3: 100 V/V
  - INA240A4: 200 V/V
- Quiescent Current: 2.4 mA (Maximum)

2 Applications

- Motor Controls
- Solenoid and Valve Controls
- Power Management
- Actuator Controls
- Pressure Regulators
- Telecom Equipment



Typical Application

3 Description

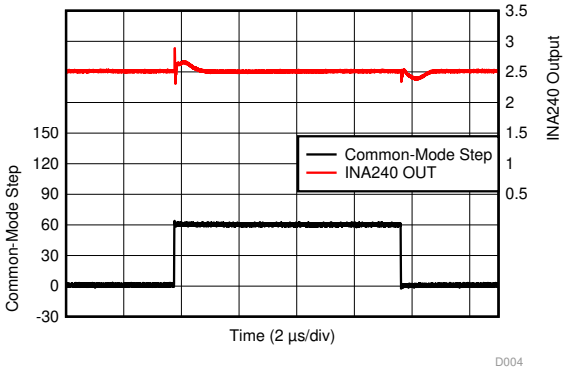
The INA240 device is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating the flyback period of typical solenoid applications. Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use pulse width modulation (PWM) signals (such as motor drives and solenoid control systems). This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage.

This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale. All versions are specified over the extended operating temperature range (–40°C to +125°C), and are offered in an 8-pin TSSOP and 8-pin SOIC packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA240	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Enhanced PWM Rejection

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2017) to Revision C (December 2021)	Page
• Changed D (SOIC) package size from: 4.00 mm × 3.91 mm to: 4.90 mm × 3.91 mm	1
• Added text *or leave unconnected.* to the NC pin description	3

Changes from Revision A (October 2016) to Revision B (October 2017)	Page
• Added D (SOIC) package to *Device Information* table	1
• Added *Description (cont.)* section	1
• Added preview label to 8-pin TSSOP package	1
• Added D (SOIC) pinout diagram and table to *Pin Configuration and Functions* section	3
• Changed y-axis values in Figure 7-15	6
• Added Figure 11-2	24

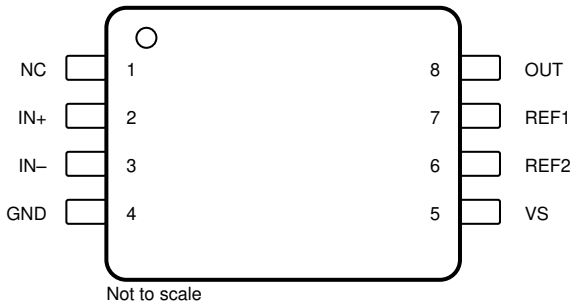
Changes from Revision * (July 2016) to Revision A (October 2016)	Page
• Changed document status from Product Preview to Production Data	1

5 Device Comparison

Table 5-1. Device Comparison

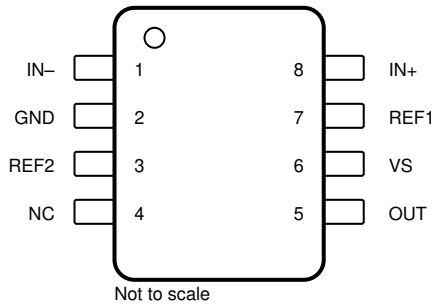
PRODUCT	GAIN (V/V)
INA240A1	20
INA240A2	50
INA240A3	100
INA240A4	200

6 Pin Configuration and Functions



NC- no internal connection

Figure 6-1. INA240 PW Package 8-Pin TSSOP Top View



NC- no internal connection

Figure 6-2. INA240 D Package 8-Pin SOIC Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	PW (TSSOP)	D (SOIC)		
GND	4	2	Analog	Ground
IN–	3	1	Analog input	Connect to load side of shunt resistor
IN+	2	8	Analog input	Connect to supply side of shunt resistor
NC	1	4	—	Reserved. Connect to ground or leave floating
OUT	8	5	Analog output	Output voltage
REF1	7	7	Analog input	Reference 1 voltage. Connect to 0 V to VS; see the *Adjusting the Output Midpoint With the Reference Pins* section for connection options
REF2	6	3	Analog input	Reference 2 voltage. Connect to 0 V to VS; see the *Adjusting the Output Midpoint With the Reference Pins* section for connection options
VS	5	6	—	Power supply, 2.7 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			6	V
Analog inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–80	80	V
	Common-mode	–6	90	
REF1, REF2, NC inputs		GND – 0.3	V_S + 0.3	V
Output		GND – 0.3	V_S + 0.3	V
Operating free-air temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–4		80	V
V_S	Operating supply voltage	2.7		5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA240		UNIT
		PW (TSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.1	113.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.2	51.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.4	57.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.4	56.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25 °C, VS = 5 V, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_{CM} = 12 V, and $V_{REF1} = V_{REF2} = V_S$ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	V_{IN+} = –4 V to 80 V, V_{SENSE} = 0 mV T_A = – 40°C to 125°C	–4		80	V
CMRR	Common-mode rejection ratio	V_{IN+} = –4 V to 80 V, V_{SENSE} = 0 mV T_A = –40°C to 125°C	120	132		dB
		f = 50 kHz		93		
V_{OS}	Offset voltage, input-referred	V_{SENSE} = 0 mV		±5	±25	µV
dV_{OS}/dT	Offset voltage drift	V_{SENSE} = 0 mV, T_A = –40°C to 125°C		±50	±250	nV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{SENSE} = 0 mV T_A = –40°C to 125°C		±1	±10	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$, V_{SENSE} = 0 mV		90		µA
	Reference input range		0		V_S	V
OUTPUT						
G	Gain	INA240A1		20		V/V
		INA240A2		50		
		INA240A3		100		
		INA240A4		200		
	Gain error	GND + 50 mV ≤ V_{OUT} ≤ V_S – 200 mV		±0.05%	±0.20%	
		T_A = –40°C to 125°C		±0.5	±2.5	ppm/°C
	Non-linearity error	GND + 10 mV ≤ V_{OUT} ≤ V_S – 200 mV		±0.01%		
	Reference divider accuracy	$V_{OUT} = \lvert (V_{REF1} – V_{REF2}) \rvert / 2$ at V_{SENSE} = 0 mV, T_A = –40°C to 125°C		0.02%	0.1%	
RVRR	Reference voltage rejection ratio (input-referred)	INA240A1		20		µV/V
		INA240A3		5		
		INA240A2, INA240A4		2		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND T_A = –40°C to 125°C		V_S – 0.05	V_S – 0.2	V
	Swing to GND	R_L = 10 kΩ to GND, V_{SENSE} = 0 mV $V_{REF1} = V_{REF2}$ = 0 V, T_A = –40°C to 125°C		V_{GND} + 1	V_{GND} + 10	mV
FREQUENCY RESPONSE						
BW	Bandwidth	All gains, –3-dB bandwidth		400		kHz
		All gains, 2% THD+N(1)		100		
	Settling time - output settles to 0.5% of final value	INA240A1		9.6		µs
		INA240A4		9.8		
SR	Slew rate			2		V/µs
NOISE (INPUT REFERRED)						
	Voltage noise density			40		nV/√Hz
POWER SUPPLY						
V_S	Operating voltage range	T_A = –40°C to 125°C	2.7		5.5	V
I_Q	Quiescent current	V_{SENSE} = 0 mV		1.8	2.4	mA
		I_Q vs temperature, T_A = –40°C to 125°C			2.6	
TEMPERATURE RANGE						
	Specified range		–40		125	°C

(1) See the *Input Signal Bandwidth* section for more details.
(2) See Figure 7-13.

7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

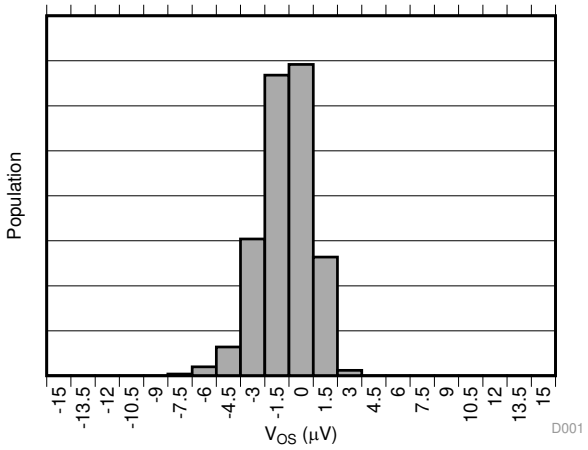


Figure 7-1. Input Offset Voltage Production Distribution

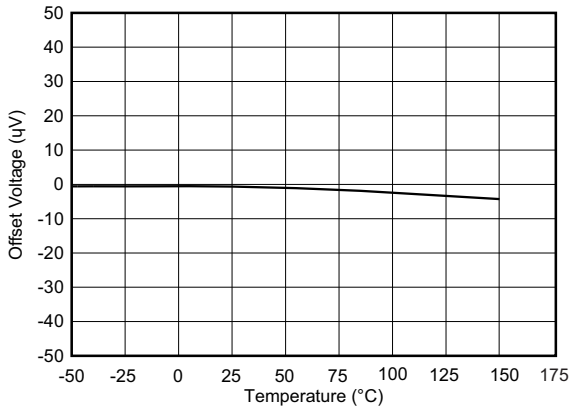


Figure 7-2. Offset Voltage vs Temperature

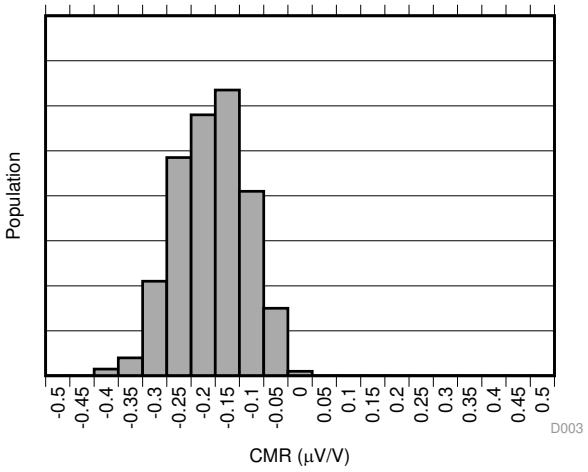


Figure 7-3. Common-Mode Rejection Production Distribution

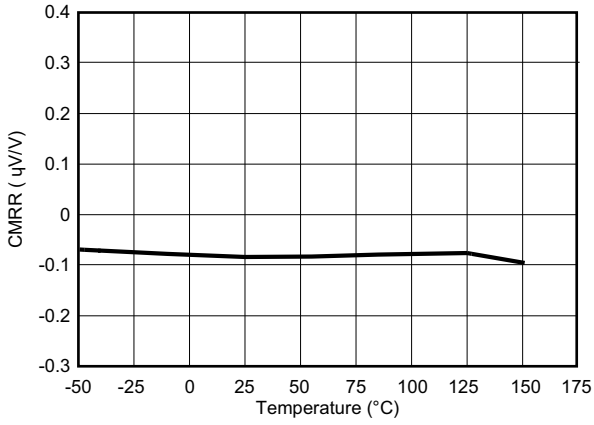


Figure 7-4. Common-Mode Rejection Ratio vs Temperature

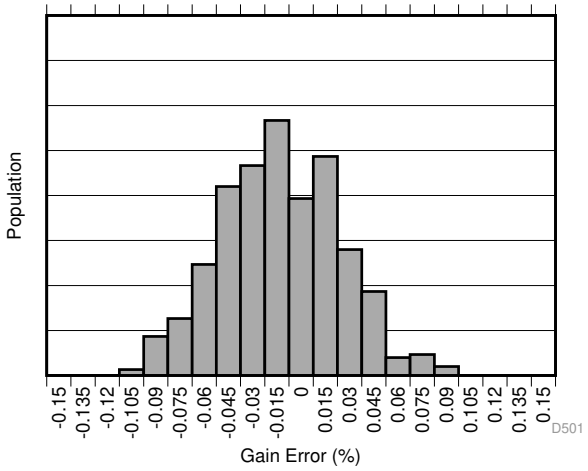


Figure 7-5. Gain Error Production Distribution

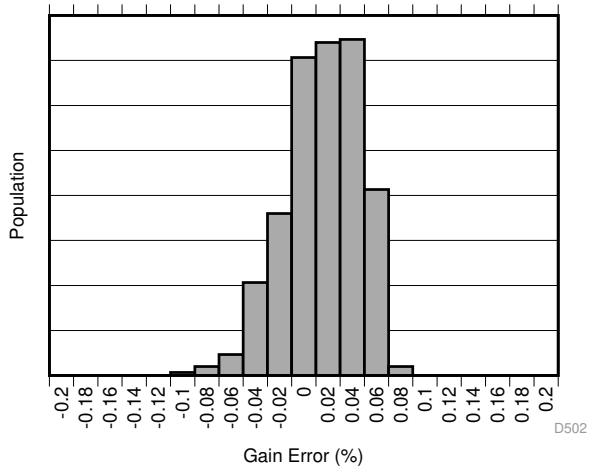


Figure 7-6. Gain Error Production Distribution

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

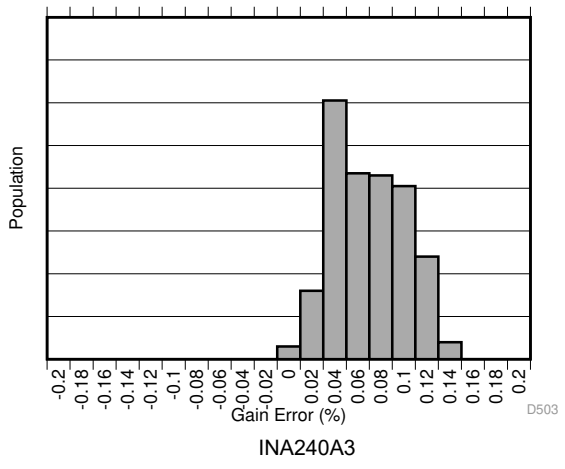


Figure 7-7. Gain Error Production Distribution

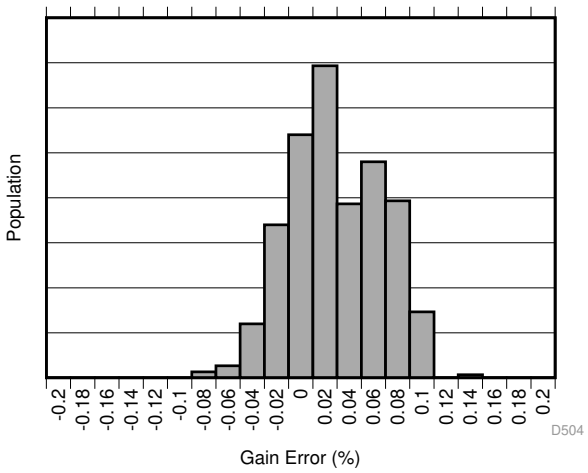


Figure 7-8. Gain Error Production Distribution

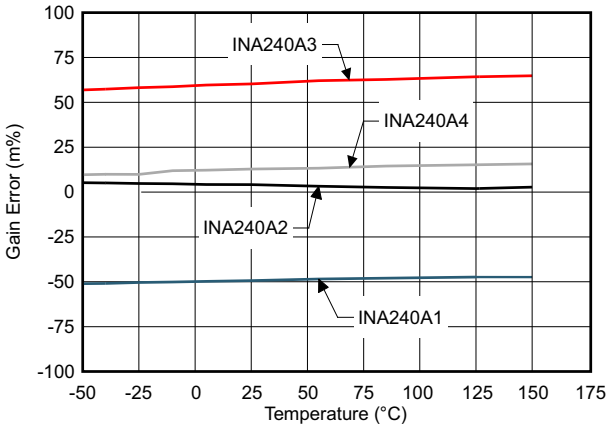


Figure 7-9. Gain Error vs Temperature

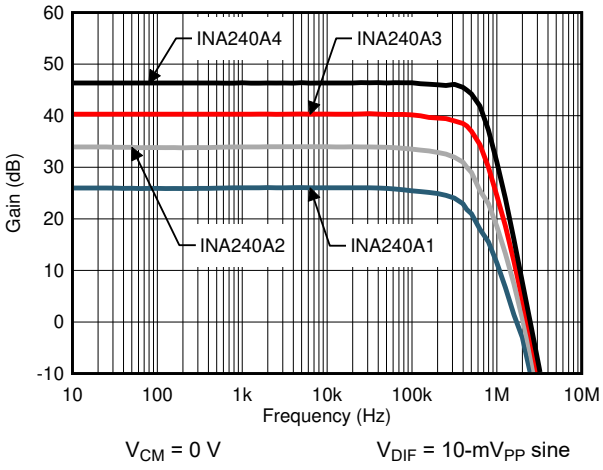


Figure 7-10. Gain vs Frequency

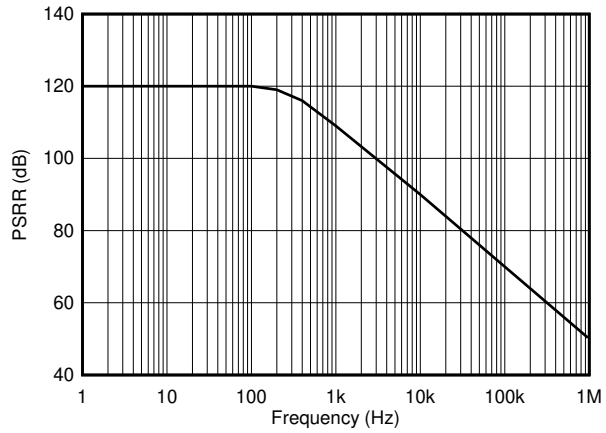


Figure 7-11. Power-Supply Rejection Ratio vs Frequency

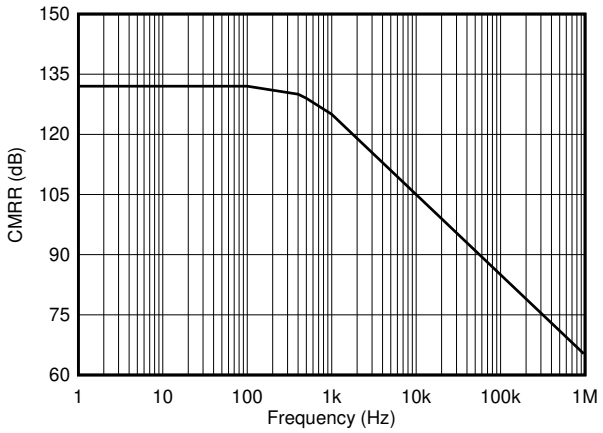


Figure 7-12. Common-Mode Rejection Ratio vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)

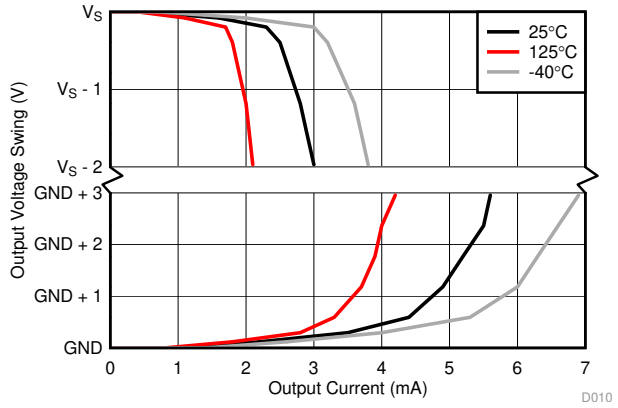
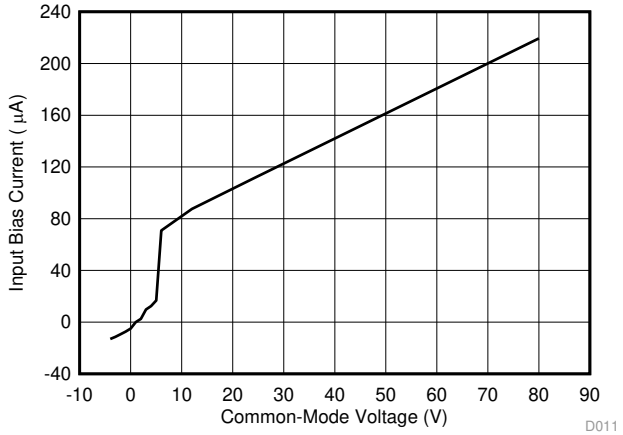
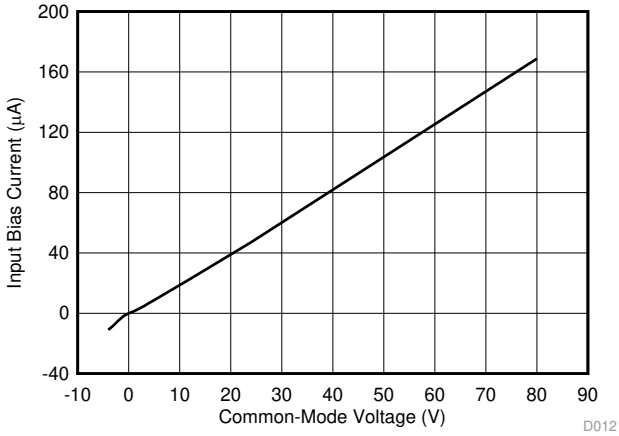


Figure 7-13. Output Voltage Swing vs Output Current



V_S = 5 V

Figure 7-14. Input Bias Current vs Common-Mode Voltage



V_S = 0 V

Figure 7-15. Input Bias Current vs Common-Mode Voltage

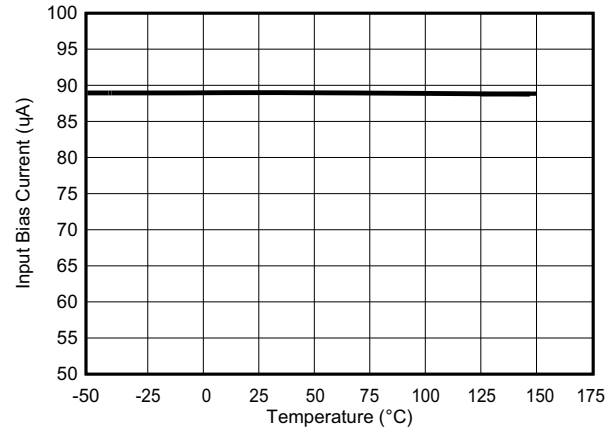


Figure 7-16. Input Bias Current vs Temperature

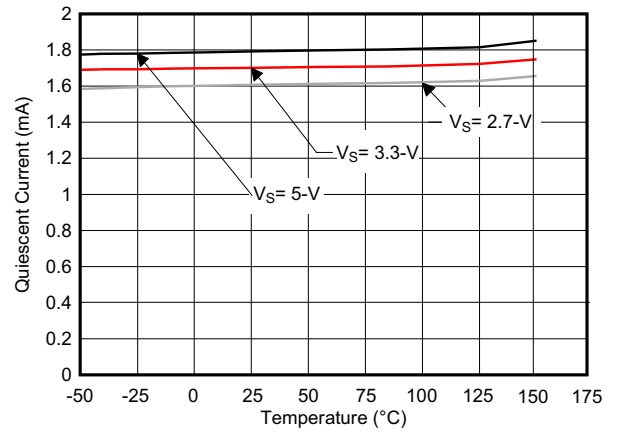


Figure 7-17. Quiescent Current vs Temperature

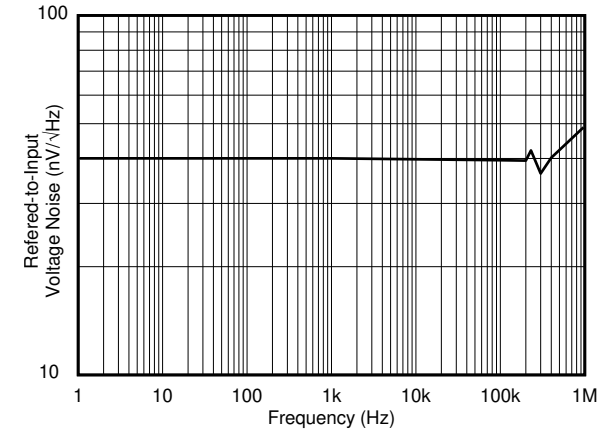
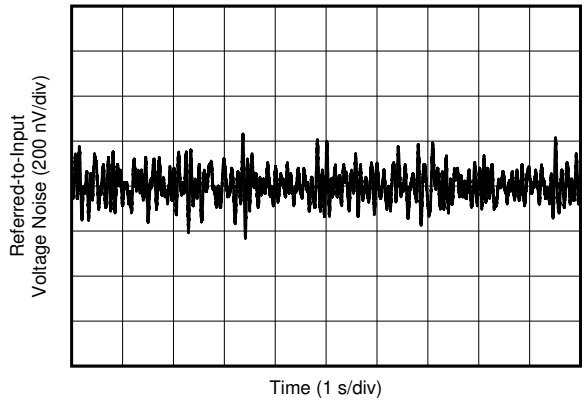


Figure 7-18. Input-Referred Voltage Noise vs Frequency

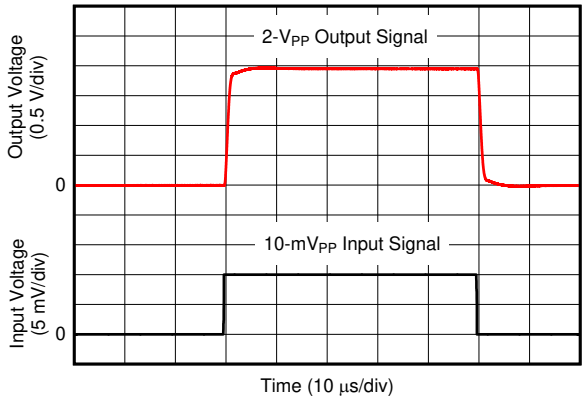
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{CM} = 12 V, and V_{REF} = V_S / 2 (unless otherwise noted)



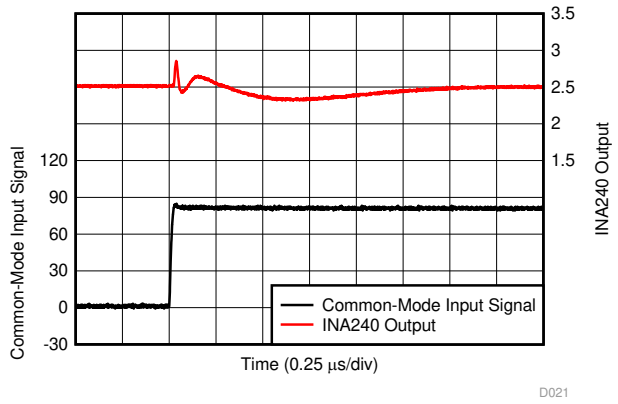
V_S = ±2.5 V V_{CM} = 0 V V_{DIF} = 0 V
V_{REF1} = V_{REF2} = 0 V Input referred

Figure 7-19. 0.1-Hz to 10-Hz Voltage Noise



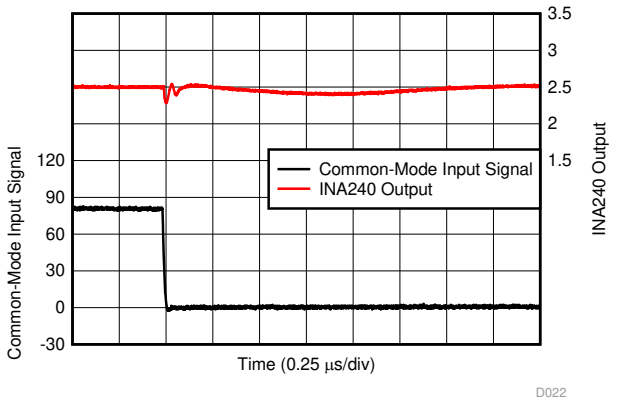
V_{REF1} = V_{REF2} = 0 V 10-mV_{PP} input step

Figure 7-20. Step Response



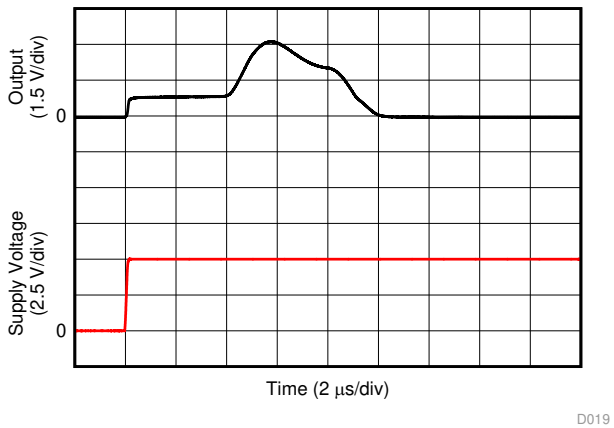
Rising edge

Figure 7-21. Common-Mode Voltage Transient Response



Falling edge

Figure 7-22. Common-Mode Voltage Transient Response



V_{REF1} = V_{REF2} = 0 V

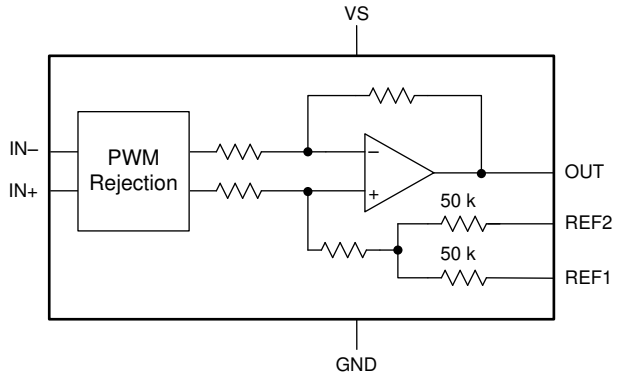
Figure 7-23. Start-Up Response

8 Detailed Description

8.1 Overview

The INA240 is a current-sense amplifier that offers a wide common-mode range, precision, zero-drift topology, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Amplifier Input Signal

The INA240 is designed to handle large common-mode transients over a wide voltage range. Input signals from current measurement applications for linear and PWM applications can be connected to the amplifier to provide a highly accurate output, with minimal common-mode transient artifacts.

8.3.1.1 Enhanced PWM Rejection Operation

The enhanced PWM rejection feature of the INA240 provides increased attenuation of large common-mode ΔV/Δt transients. Large ΔV/Δt common-mode transients associated with PWM signals are employed in applications such as motor or solenoid drive and switching power supplies. Traditionally, large ΔV/Δt common-mode transitions are handled strictly by increasing the amplifier signal bandwidth, which can increase chip size, complexity and ultimately cost. The INA240 is designed with high common-mode rejection techniques to reduce large ΔV/Δt transients before the system is disturbed as a result of these large signals. The high AC CMRR, in conjunction with signal bandwidth, allows the INA240 to provide minimal output transients and ringing compared with standard circuit approaches.

8.3.1.2 Input Signal Bandwidth

The INA240 input signal, which represents the current being measured, is accurately measured with minimal disturbance from large ΔV/Δt common-mode transients as previously described. For PWM signals typically associated with motors, solenoids, and other switching applications, the current being monitored varies at a significantly slower rate than the faster PWM frequency.

The INA240 bandwidth is defined by the –3-dB bandwidth of the current-sense amplifier inside the device; see the *Electrical Characteristics* table. The device bandwidth provides fast throughput and fast response required for the rapid detection and processing of overcurrent events. Without the higher bandwidth, protection circuitry may not have adequate response time and damage may occur to the monitored application or circuit.

Figure 8-1 shows the performance profile of the device over frequency. Harmonic distortion increases at the upper end of the amplifier bandwidth with no adverse change in detection of overcurrent events. However, increased distortion at the highest frequencies must be considered when the measured current bandwidth begins to approach the INA240 bandwidth.

For applications requiring distortion sensitive signals, Figure 8-1 provides information to show that there is an optimal frequency performance range for the amplifier. The full amplifier bandwidth is always available for fast overcurrent events at the same time that the lower frequency signals are amplified at a low distortion level. The output signal accuracy is reduced for frequencies closer to the maximum bandwidth. Individual requirements determine the acceptable limits of distortion for high-frequency, current-sensing applications. Testing and evaluation in the end application or circuit is required to determine the acceptance criteria and to validate the performance levels meet the system specifications.

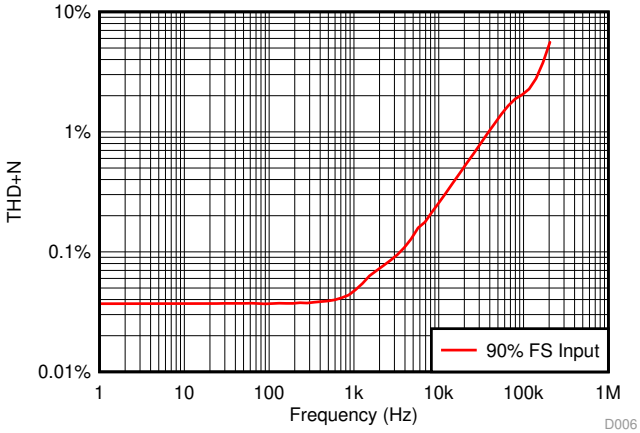


Figure 8-1. Performance Over Frequency

8.3.2 Selecting the Sense Resistor (R_{SENSE})

The INA240 determines the current magnitude from measuring the differential voltage developed across a resistor. This resistor is referred to as a *current-sensing* resistor or a *current-shunt* resistor. The flexible design of the device allows a wide input signal range across this current-sensing resistor.

The current-sensing resistor is ideally chosen solely based on the full-scale current to be measured, the full-scale input range of the circuitry following the device, and the device gain selected. The minimum current-sensing resistor is a design-based decision in order to maximize the input range of the signal chain circuitry. Full-scale output signals that are not maximized to the full input range of the system circuitry limit the ability of the system to exercise the full dynamic range of system control.

Two important factors to consider when finalizing the current-sensing resistor value are: the required current measurement accuracy and the maximum power dissipation across the resistor. A larger resistor voltage provides for a more accurate measurement, but increases the power dissipation in the resistor. The increased power dissipation generates heat, which reduces the sense resistor accuracy because of the temperature coefficient. The voltage signal measurement uncertainty is reduced when the input signal gets larger because any fixed errors become a smaller percentage of the measured signal. The design trade-off to improve measurement accuracy increases the current-sensing resistor value. The increased resistance value results in an increased power dissipation in the system which can additionally decrease the overall system accuracy. Based on these relationships, the measurement accuracy is inversely proportional to both the resistance value and power dissipation contributed by the current-shunt selection.

By increasing the current-shunt resistor, the differential voltage is increased across the resistor. Larger input differential voltages require a smaller amplifier gain to achieve a full-scale amplifier output voltage. Smaller current-shunt resistors are desired but require large amplifier gain settings. The larger gain settings often have increased error and noise parameters, which are not attractive for precision designs. Historically, the design goals for high-performance measurements forced designers to accept selecting larger current-sense resistors and the lower gain amplifier settings. The INA240 provides 100-V/V and 200-V/V gain options that offer the

high-gain setting and maintains high-performance levels with offset values below 25 µV. These devices allow for the use of lower shunt resistor values to achieve lower power dissipation and still meet high system performance specifications.

Table 8-1 shows an example of the different results obtained from using two different gain versions of the INA240. From the table data, the higher gain device allows a smaller current-shunt resistor and decreased power dissipation in the element. The *Calculating Total Error* section provides information on the error calculations that must be considered in addition to the gain and current-shunt value when designing with the INA240.

Table 8-1. R_{SENSE} Selection and Power Dissipation(1)

PARAMETER		EQUATION	RESULTS	
			INA240A1	INA240A4
Gain		—	20 V/V	200 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{DIFF} = V_{OUT}$ / Gain	150 mV	15 mV
R_{SENSE}	Current-sense resistor value	$R_{SENSE} = V_{DIFF} / I_{MAX}$	15 mΩ	1.5 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	1.5 W	0.15 W

(1) Full-scale current = 10 A, and full-scale output voltage = 3 V.

8.4 Device Functional Modes

8.4.1 Adjusting the Output Midpoint With the Reference Pins

Figure 8-2 shows a test circuit for reference-divider accuracy. The INA240 output is configurable to allow for unidirectional or bidirectional operation.

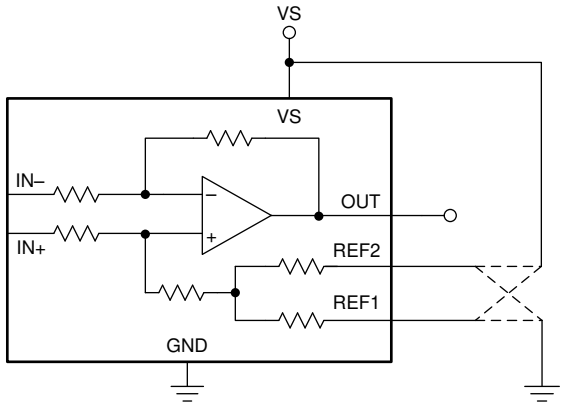


Figure 8-2. Test Circuit For Reference Divider Accuracy

Note

Do not connect the REF1 pin or the REF2 pin to any voltage source lower than GND or higher than V_S.

The output voltage is set by applying a voltage or voltages to the reference voltage inputs, REF1 and REF2. The reference inputs are connected to an internal gain network. There is no operational difference between the two reference pins.

8.4.2 Reference Pin Connections for Unidirectional Current Measurements

Unidirectional operation allows current measurements through a resistive shunt in one direction. For unidirectional operation, connect the device reference pins together and then to the negative rail (see the *Ground Referenced Output* section) or the positive rail (see the *VS Referenced Output* section). The required differential input polarity depends on the output voltage setting. The amplifier output moves away from the referenced rail proportional to the current passing through the external shunt resistor. If the amplifier reference pins are connected to the positive rail, then the input polarity must be negative to move the amplifier output down

(towards ground). If the amplifier reference pins are connected at ground, then the input polarity must be positive to move the amplifier output up (towards supply).

The following sections describe how to configure the output for unidirectional operation cases.

8.4.2.1 Ground Referenced Output

When using the INA240 in a unidirectional mode with a ground referenced output, both reference inputs are connected to ground; this configuration takes the output to ground when there is a 0-V differential at the input (as Figure 8-3 shows).

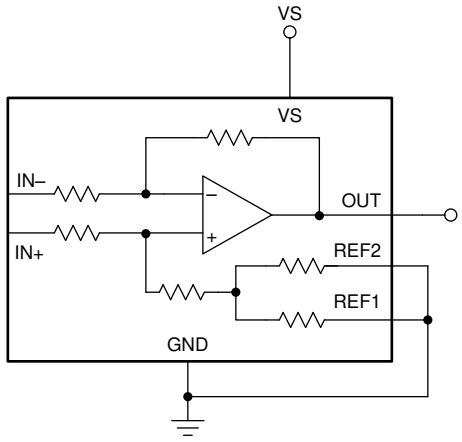


Figure 8-3. Ground Referenced Output

8.4.2.2 VS Referenced Output

Unidirectional mode with a VS referenced output is configured by connecting both reference pins to the positive supply. Use this configuration for circuits that require power-up and stabilization of the amplifier output signal and other control circuitry before power is applied to the load (as shown in Figure 8-4).

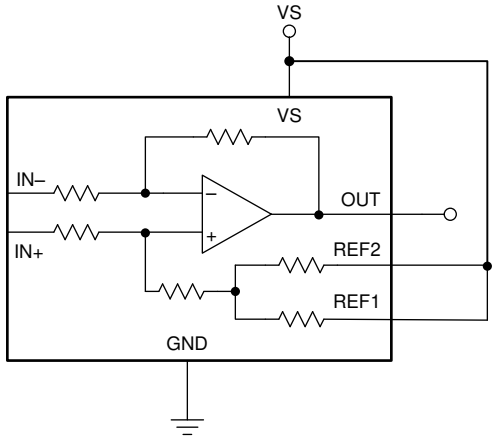


Figure 8-4. VS Referenced Output

8.4.3 Reference Pin Connections for Bidirectional Current Measurements

Bidirectional operation allows the INA240 to measure currents through a resistive shunt in two directions. For this operation case, the output voltage can be set anywhere within the reference input limits. A common configuration is to set the reference inputs at half-scale for equal range in both directions. However, the reference inputs can be set to a voltage other than half-scale when the bidirectional current is non-symmetrical.

8.4.3.1 Output Set to External Reference Voltage

Connecting both pins together and then to a reference voltage results in an output voltage equal to the reference voltage for the condition of shorted input pins or a 0-V differential input; this configuration is shown in Figure 8-5. The output voltage decreases below the reference voltage when the IN+ pin is negative relative to the IN– pin and increases when the IN+ pin is positive relative to the IN– pin. This technique is the most accurate way to bias the output to a precise voltage.

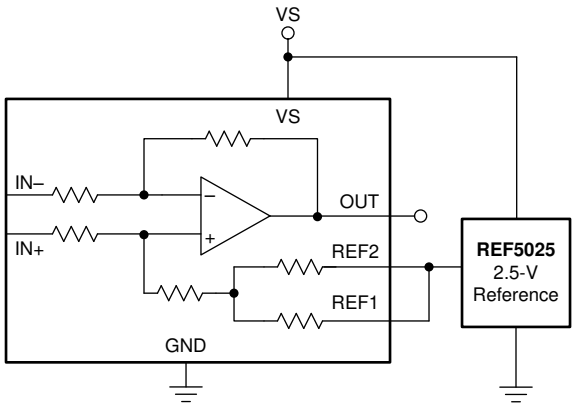


Figure 8-5. External Reference Output

8.4.3.2 Output Set to Midsupply Voltage

By connecting one reference pin to VS and the other to the GND pin, the output is set at half of the supply when there is no differential input, as shown in Figure 8-6. This method creates a ratiometric offset to the supply voltage, where the output voltage remains at VS / 2 for 0 V applied to the inputs.

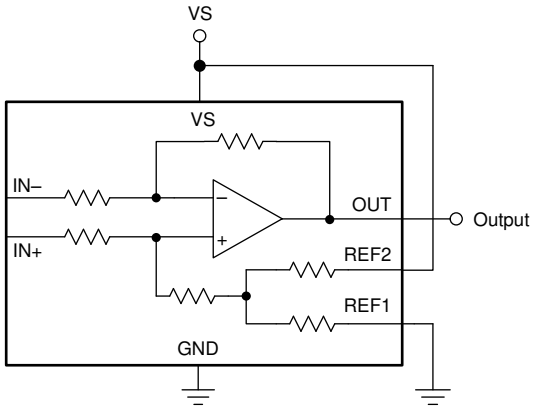


Figure 8-6. Midsupply Voltage Output

8.4.3.3 Output Set to Mid-External Reference

In this case, an external reference is divided by two by connecting one REF pin to ground and the other REF pin to the reference, as shown in Figure 8-7.

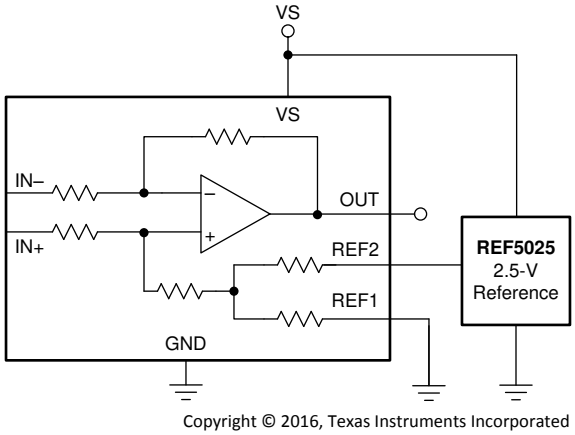


Figure 8-7. Mid-External Reference Output

8.4.3.4 Output Set Using Resistor Divider

The INA240 REF1 and REF2 pins allow for the midpoint of the output voltage to be adjusted for system circuitry connections to analog to digital converters (ADCs) or other amplifiers. The REF pins are designed to be connected directly to supply, ground, or a low-impedance reference voltage. The REF pins can be connected together and biased using a resistor divider to achieve a custom output voltage. If the amplifier is used in this configuration, as shown in Figure 8-8, use the output as a differential signal with respect to the resistor divider voltage. Use of the amplifier output as a single-ended signal in this configuration is not recommended because the internal impedance shifts can adversely affect device performance specifications.

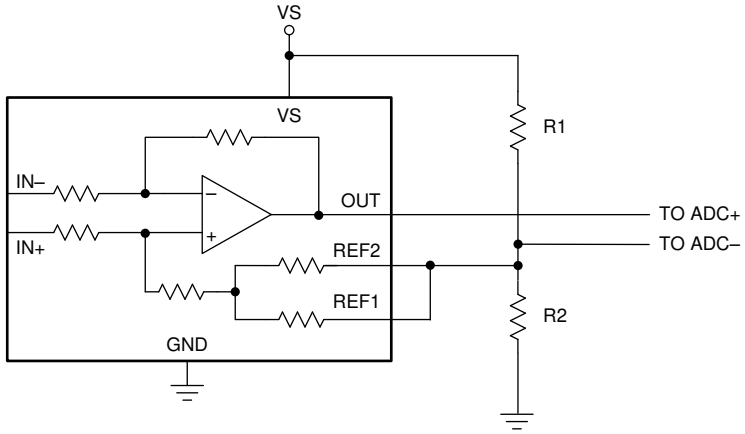


Figure 8-8. Setting the Reference Using a Resistor Divider

8.4.4 Calculating Total Error

The INA240 electrical specifications (see the *Electrical Characteristics* table) include typical individual errors terms (such as gain error, offset error, and nonlinearity error). Total error, including all of these individual error components, is not specified in the *Electrical Characteristics* table. In order to accurately calculate the expected error of the device, the device operating conditions must first be known. Some current-shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this point has limited value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources and how the device total error value can be calculated from the combination of these errors for specific conditions.

Two examples are provided in Table 8-2 and Table 8-3 that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well to provide the user more information on how much error variance is present from device to device.

8.4.4.1 Error Sources

The typical error sources that have the largest effect on the total error of the device are gain error, nonlinearity, common-mode rejection ratio, and input offset voltage error. For the INA240, an additional error source (referred to as the *reference voltage rejection ratio*) is also included in the total error value.

8.4.4.2 Reference Voltage Rejection Ratio Error

Reference voltage rejection ratio refers to the amount of error induced by applying a reference voltage to the INA240 that deviates from the mid-point of the device supply voltage.

8.4.4.2.1 Total Error Example 1

Table 8-2. Total Error Calculation: Example 1(1)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Initial input offset voltage	V_{OS}	—	5 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	0 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times \lvert V_S / 2 - V_{REF} \rvert$	0 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	5 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.05%
Gain error	Error_Gain	—	0.05%
Nonlinearity error	Error_Lin	—	0.01%
Total error	—	$\sqrt{(Error\_V_{OS})^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.07%

(1) The data for Table 8-2 was taken with the INA240A4, V_S = 5 V, V_{CM} = 12 V, $V_{REF1} = V_{REF2} = V_S / 2$, and V_{SENSE} = 10 mV.

8.4.4.2.2 Total Error Example 2

Table 8-3. Total Error Calculation: Example 2(1)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Initial input offset voltage	V_{OS}	—	5 µV
Added input offset voltage because of common-mode voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \times (V_{CM} - 12V)$	12.1 µV
Added input offset voltage because of reference voltage	V_{OS_REF}	$RVRR \times \lvert V_S / 2 - V_{REF} \rvert$	5 µV
Total input offset voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	14 µV
Error from input offset voltage	$Error\_V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.14%
Gain error	Error_Gain	—	0.05%
Nonlinearity error	Error_Lin	—	0.01%

Table 8-3. Total Error Calculation: Example 2(1) (continued)

TERM	SYMBOL	EQUATION	TYPICAL VALUE
Total error	—	$\sqrt{(\text{Error\_V}_{OS})^2 + (\text{Error\_Gain})^2 + (\text{Error\_Lin})^2}$	0.15%

(1) The data for Table 8-3 was taken with the INA240A4, V_S = 5 V, V_{CM} = 60 V, V_{REF1} = V_{REF2} = 0 V, and V_{SENSE} = 10 mV.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA240 measures the voltage developed as current flows across the current-sensing resistor. The device provides reference pins to configure operation as either unidirectional or bidirectional output swing. When using the INA240 for inline motor current sense, the device is commonly configured for bidirectional operation.

9.1.1 Input Filtering

Note

Input filters are not required for accurate measurements using the INA240, and use of filters in this location is not recommended. If filter components are used on the input of the amplifier, follow the guidelines in this section to minimize the effects on performance.

Based strictly on user design requirements, external filtering of the current signal may be desired. The initial location that can be considered for the filter is at the output of the current amplifier. Although placing the filter at the output satisfies the filtering requirements, this location changes the low output impedance measured by any circuitry connected to the output voltage pin. The other location for filter placement is at the current amplifier input pins. This location satisfies the filtering requirement also, however the components must be carefully selected to minimally impact device performance. Figure 9-1 shows a filter placed at the inputs pins.

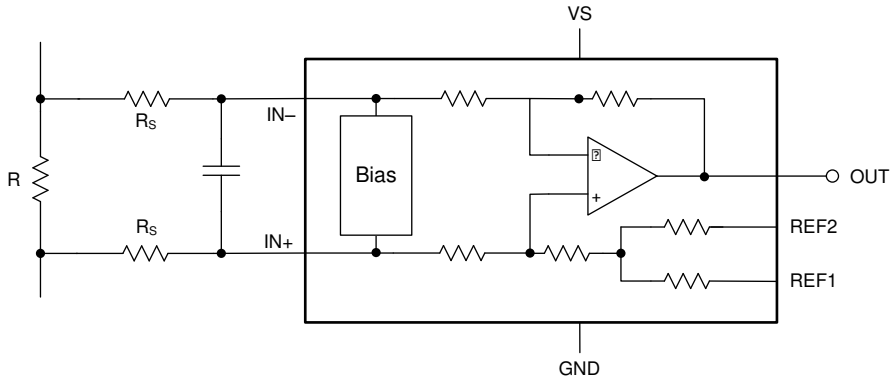


Figure 9-1. Filter at Input Pins

External series resistance provide a source of additional measurement error, so keep the value of these series resistors to 10-Ω or less to reduce loss of accuracy. The internal bias network shown in Figure 9-1 creates a mismatch in input bias currents (see Figure 9-2) when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, a mismatch is created in the voltage drop across the filter resistors. This voltage is a differential error voltage in the shunt resistor voltage. In addition to the absolute resistor value, mismatch resulting from resistor tolerance can significantly impact the error because this value is calculated based on the actual measured resistance.

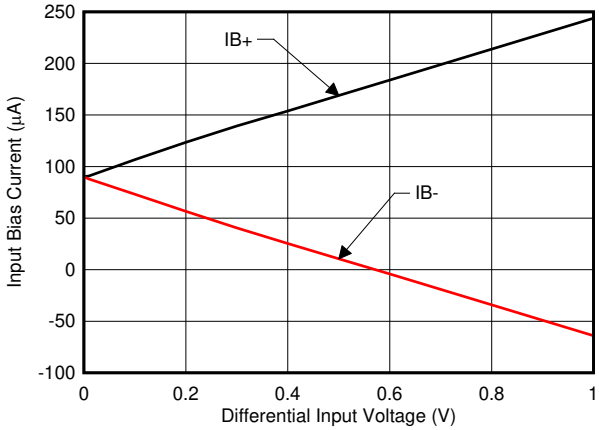


Figure 9-2. Input Bias Current vs Differential Input Voltage

The measurement error expected from the additional external filter resistors can be calculated using Equation 1, where the gain error factor is calculated using Equation 2.

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (1)$$

The gain error factor, shown in Equation 1, can be calculated to determine the gain error introduced by the additional external series resistance. Equation 1 calculates the deviation of the shunt voltage resulting from the attenuation and imbalance created by the added external filter resistance. Table 9-1 provides the gain error factor and gain error for several resistor values.

$$\text{Gain Error Factor} = \frac{3000}{R_S + 3000} \quad (2)$$

Where:

- R_S is the external filter resistance value

Table 9-1. Gain Error Factor and Gain Error For External Input Resistors

EXTERNAL RESISTANCE (Ω)	GAIN ERROR FACTOR	GAIN ERROR (%)
5	0.998	0.17
10	0.997	0.33
100	0.968	3.23

9.2 Typical Applications

The INA240 offers advantages for multiple applications including the following:

- High common-mode range and excellent CMRR enables direct inline sensing
- Ultra-low offset and drift eliminates the necessity of calibration
- Wide supply range enables a direct interface with most microprocessors

Two specific applications are provided and include more detailed information.

9.2.1 Inline Motor Current-Sense Application

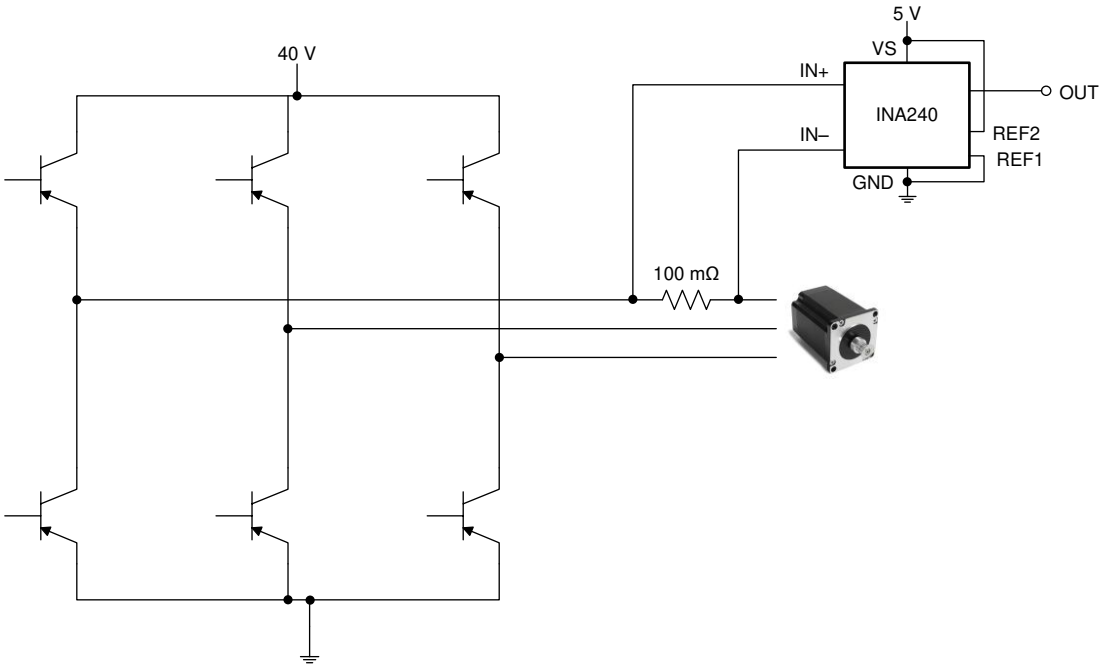


Figure 9-3. Inline Motor Application Circuit

9.2.1.1 Design Requirements

Inline current sensing has many advantages in motor control, from torque ripple reduction to real-time motor health monitoring. However, the full-scale PWM voltage requirements for inline current measurements provide challenges to accurately measure the current. Switching frequencies in the 50-kHz to 100-kHz range create higher ΔV/Δt signal transitions that must be addressed to obtain accurate inline current measurements.

With a superior common-mode rejection capability, high precision, and a high common-mode specification, the INA240 provides performance for a wide range of common-mode voltages.

9.2.1.2 Detailed Design Procedure

For this application, the INA240 measures current in the drive circuitry of a 36-V, 4000-RPM motor.

To demonstrate the performance of the device, the INA240A1 with a gain of 20 V/V was selected for this design and powered from a 5-V supply.

Using the information in the *Adjusting the Output Midpoint With the Reference Pins* section, the reference point is set to midscale by splitting the supply with REF1 connected to ground and REF2 connected to supply. This configuration allows for bipolar current measurements. Alternatively, the reference pins can be tied together and driven with an external precision reference.

The current-sensing resistor is sized so that the output of the INA240 is not saturated. A value of 100-mΩ was selected to maintain the analog input within the device limits.

9.2.1.3 Application Curve

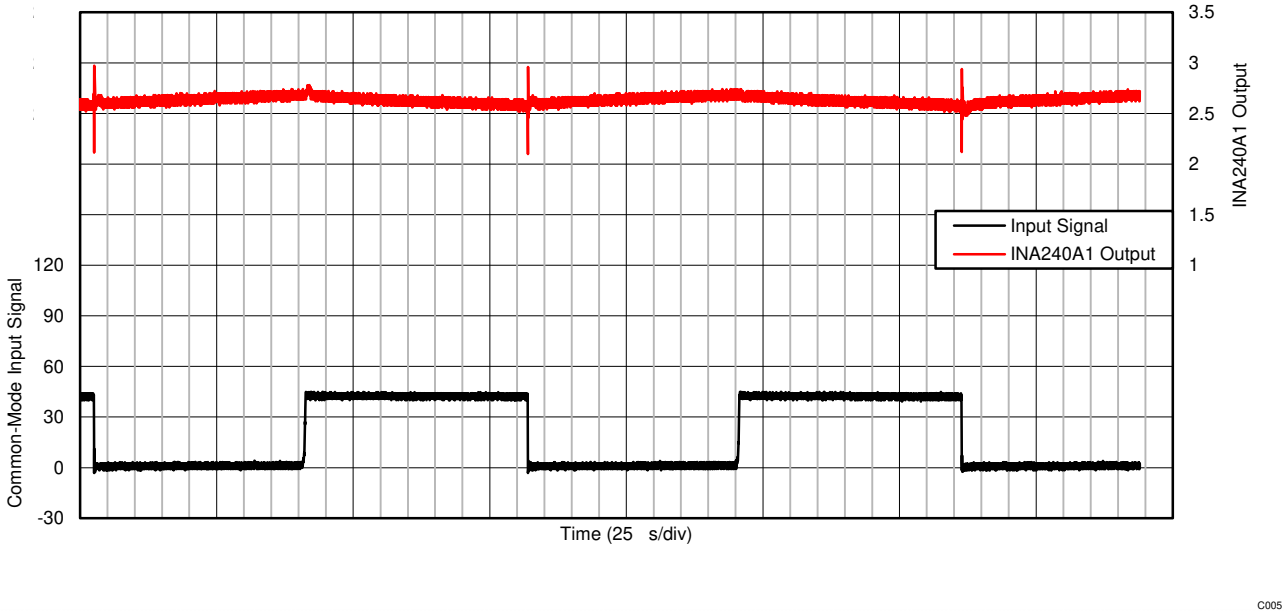


Figure 9-4. Inline Motor Current-Sense Input and Output Signals

9.2.2 Solenoid Drive Current-Sense Application

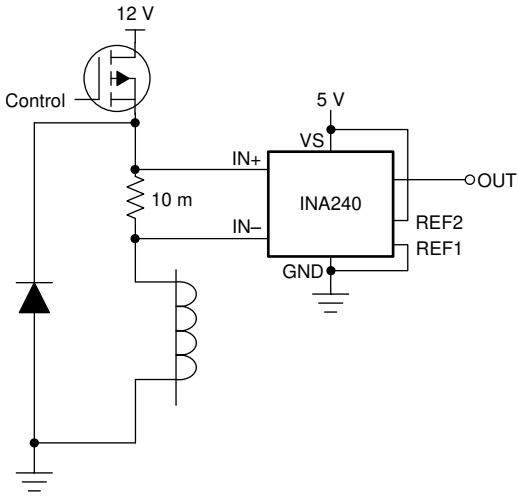


Figure 9-5. Solenoid Drive Application Circuit

9.2.2.1 Design Requirements

Challenges exist in solenoid drive current sensing that are similar to those in motor inline current sensing. In certain topologies, the current-sensing amplifier is exposed to the full-scale PWM voltage between ground and supply. The INA240 is well suited for this type of application.

9.2.2.2 Detailed Design Procedure

For this application, the INA240 measures current in the driver circuit of a 24-V, 500-mA water valve.

To demonstrate the performance of the device, the INA240A4 with a gain of 200 V/V was selected for this design and powered from a 5-V supply.

Using the information in the *Adjusting the Output Midpoint With the Reference Pins* section, the reference point is set to midscale by splitting the supply with REF1 connected to ground and REF2 connected to supply. Alternatively, the reference pins can be tied together and driven with an external precision reference.

A value of 10 mΩ was selected to maintain the analog input within the device limits.

9.2.2.3 Application Curve

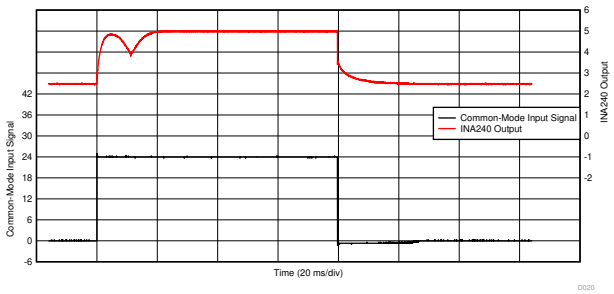


Figure 9-6. Solenoid Drive Current Sense Input and Output Signals

9.3 What to Do and What Not to Do

9.3.1 High-Precision Applications

For high-precision applications, verify accuracy and stability of the amplifier by:

- Providing a precision reference connected to REF1 and REF2
- Optimizing the layout of the power and sensing path of the sense resistor (see the *Layout* section)
- Providing adequate bypass capacitance on the supply pin (see the *Power Supply Decoupling* section)

9.3.2 Kelvin Connection from the Current-Sense Resistor

To provide accurate current measurements, verify the routing between the current-sense resistor and the amplifier uses a Kelvin connection. Use the information provided in Figure 9-7 and the *Connection to the Current-Sense Resistor* section during device layout.

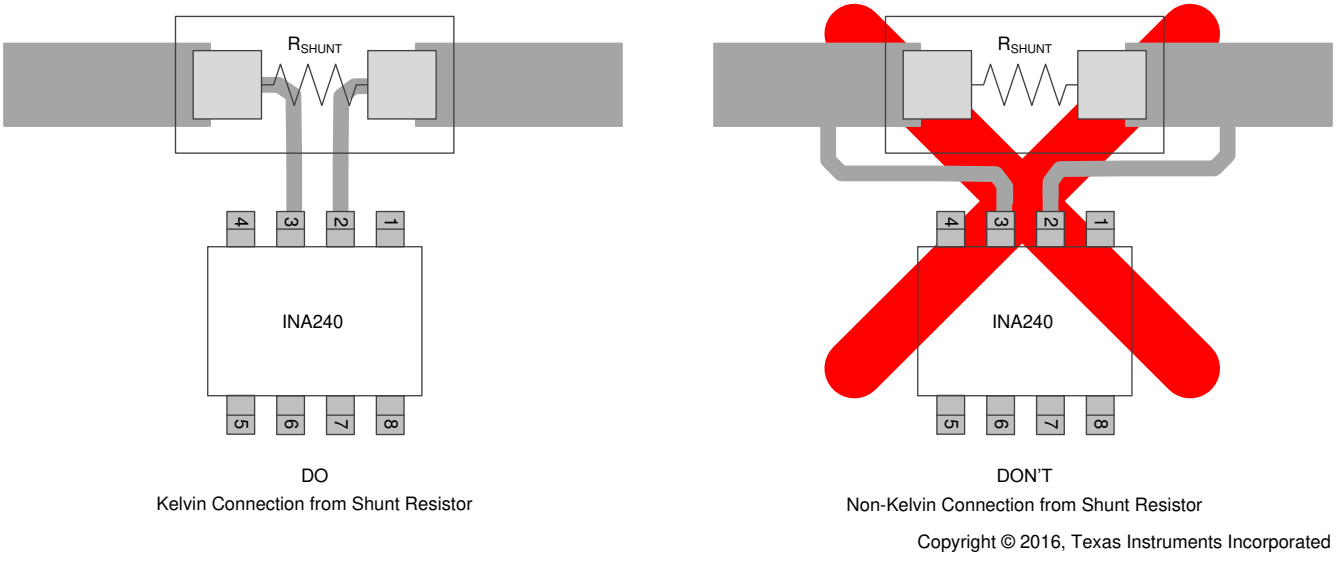


Figure 9-7. Shunt Connections to the INA240

10 Power Supply Recommendations

The INA240 series makes accurate measurements beyond the connected power-supply voltage (V_S) because the inputs (IN+ and IN–) operate anywhere between –4 V and 80 V independent of V_S. For example, the V_S power supply equals 5 V and the common-mode voltage of the measured shunt can be as high as 80 V.

Although the common-mode voltage of the input can be beyond the supply voltage, the output voltage range of the INA240 series is constrained to the supply voltage.

10.1 Power Supply Decoupling

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor value of 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

11.1.1 Connection to the Current-Sense Resistor

Poor routing of the current-sensing resistor can result in additional resistance between the input pins of the amplifier. Any additional high-current carrying impedance can cause significant measurement errors because the current resistor has a very-low-ohmic value. Use a Kelvin or 4-wire connection to connect to the device input pins. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins.

11.2 Layout Example

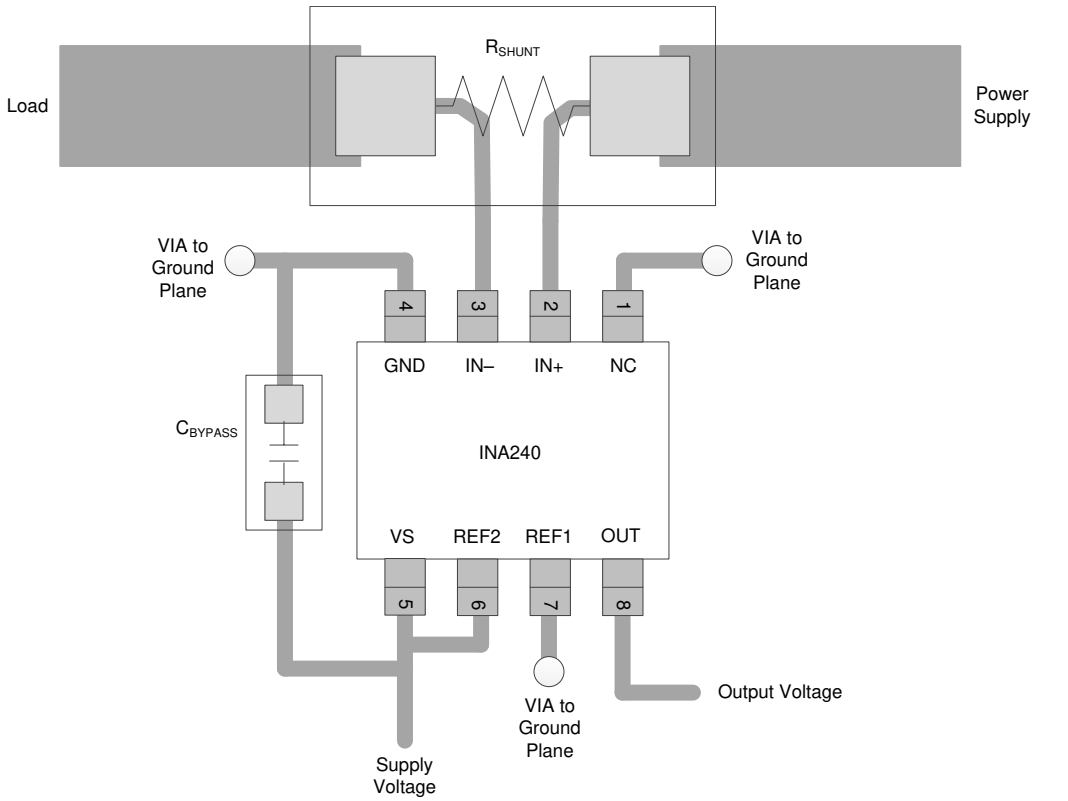


Figure 11-1. Recommended TSSOP Package Layout

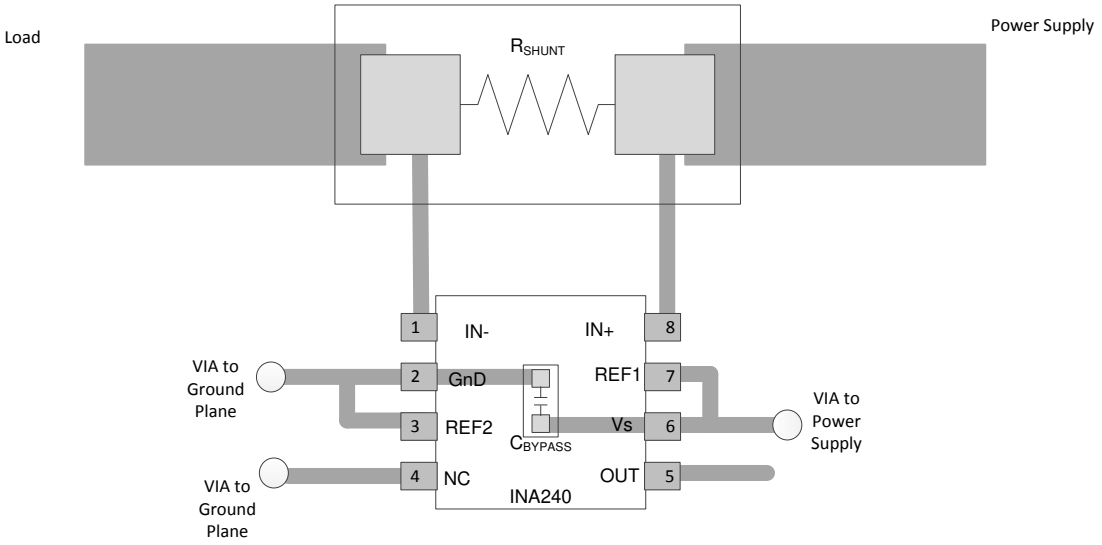


Figure 11-2. Recommended SOIC Package Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA240EVM User's Guide*
- Texas Instruments, *Motor Control Application Report*
- Texas Instruments, *48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Reference Design*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA240A1D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1	Samples
INA240A1DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1	Samples
INA240A1PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1	Samples
INA240A1PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A1	Samples
INA240A2D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2	Samples
INA240A2DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2	Samples
INA240A2PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2	Samples
INA240A2PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A2	Samples
INA240A3D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3	Samples
INA240A3DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3	Samples
INA240A3PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3	Samples
INA240A3PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A3	Samples
INA240A4D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4	Samples
INA240A4DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4	Samples
INA240A4PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4	Samples
INA240A4PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I240A4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA240 :

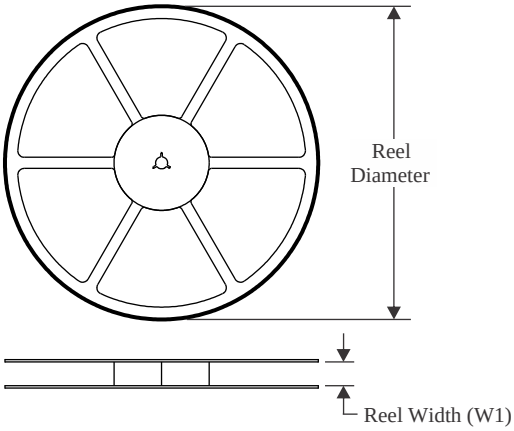
- Automotive : INA240-Q1

NOTE: Qualified Version Definitions:

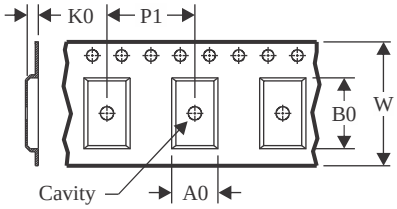
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

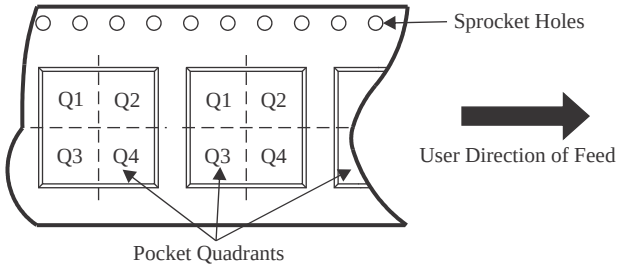


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

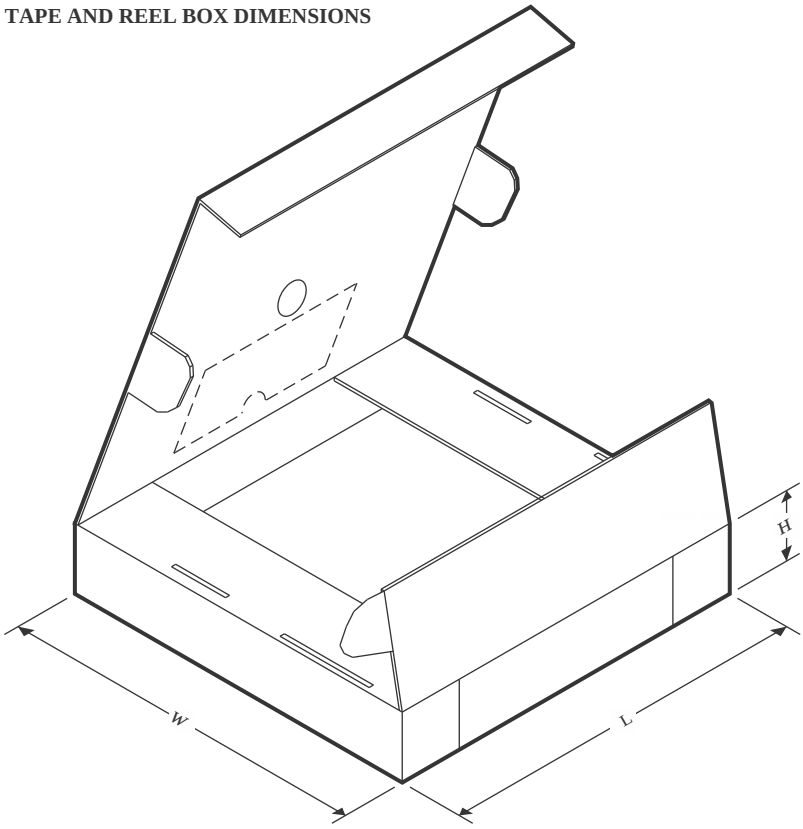
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA240A1DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A1PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A2DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A2PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A3DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A3PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
INA240A4DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA240A4PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

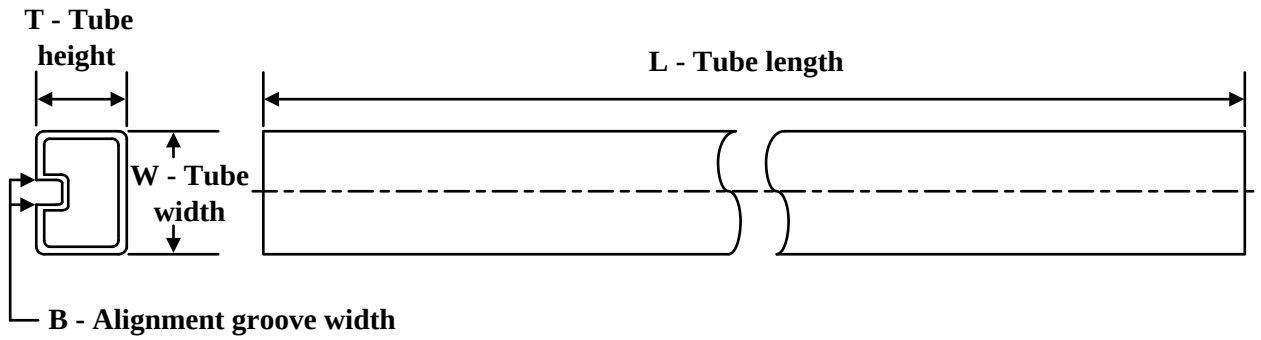
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

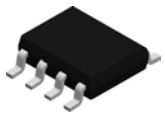
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA240A1DR	SOIC	D	8	2500	340.5	336.1	25.0
INA240A1PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
INA240A2DR	SOIC	D	8	2500	340.5	336.1	25.0
INA240A2PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
INA240A3DR	SOIC	D	8	2500	340.5	336.1	25.0
INA240A3PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
INA240A4DR	SOIC	D	8	2500	340.5	336.1	25.0
INA240A4PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA240A1D	D	SOIC	8	75	507	8	3940	4.32
INA240A1PW	PW	TSSOP	8	150	530	10.2	3600	3.5
INA240A2D	D	SOIC	8	75	507	8	3940	4.32
INA240A2PW	PW	TSSOP	8	150	530	10.2	3600	3.5
INA240A3D	D	SOIC	8	75	507	8	3940	4.32
INA240A3PW	PW	TSSOP	8	150	530	10.2	3600	3.5
INA240A4D	D	SOIC	8	75	507	8	3940	4.32
INA240A4PW	PW	TSSOP	8	150	530	10.2	3600	3.5

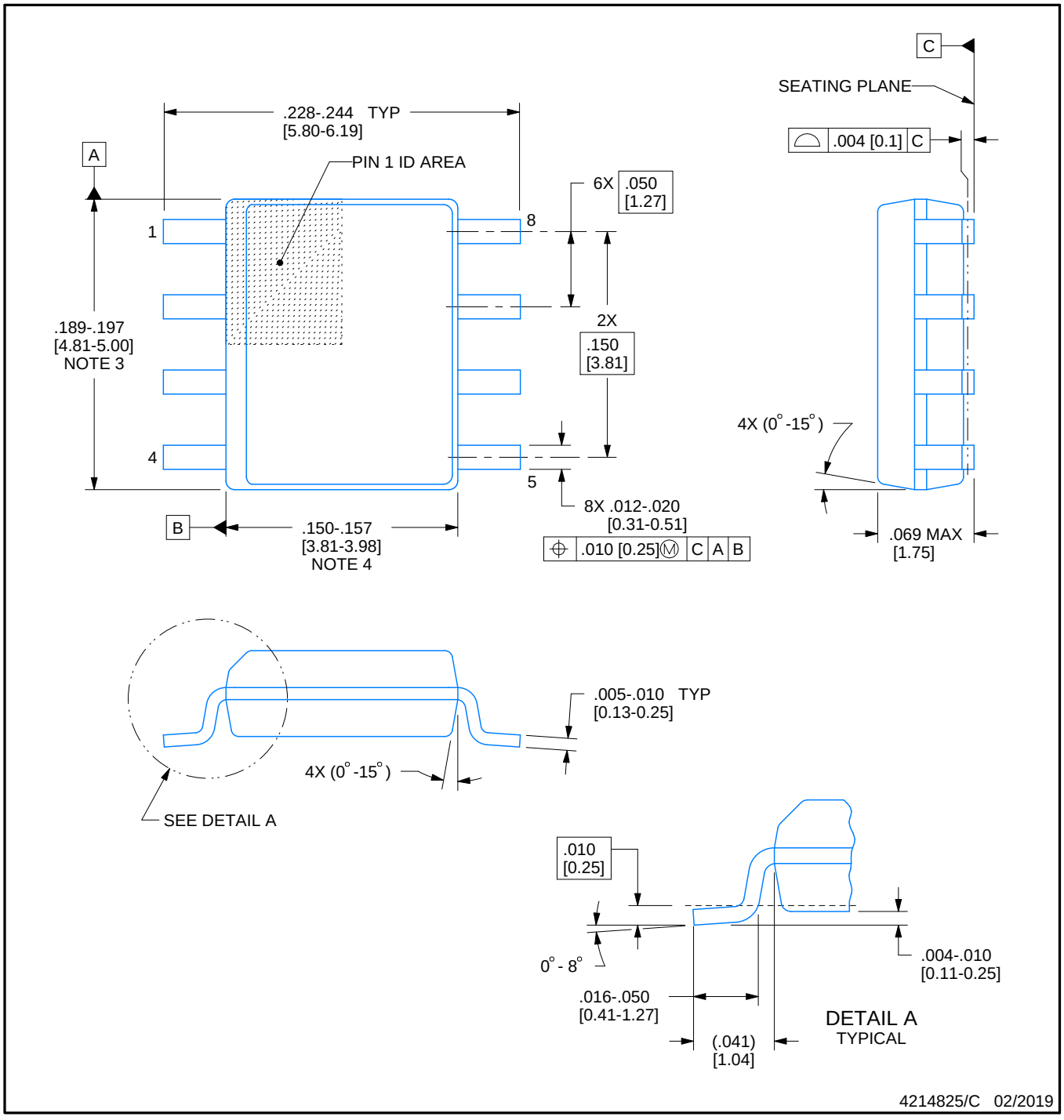


PACKAGE OUTLINE

D0008A

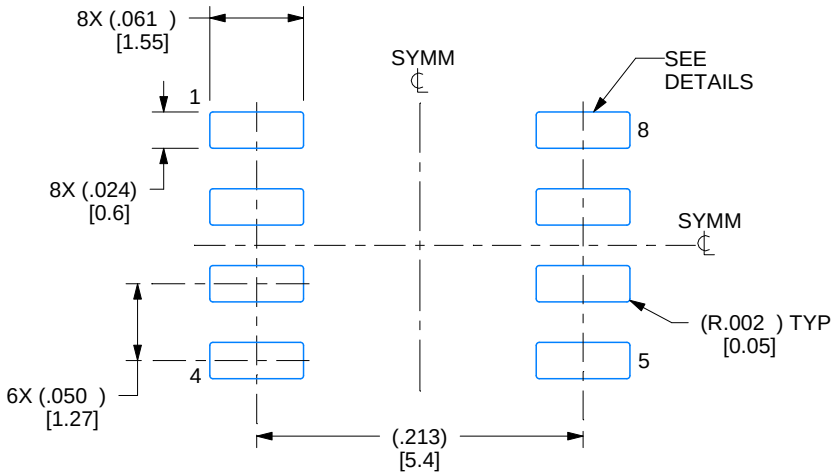
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

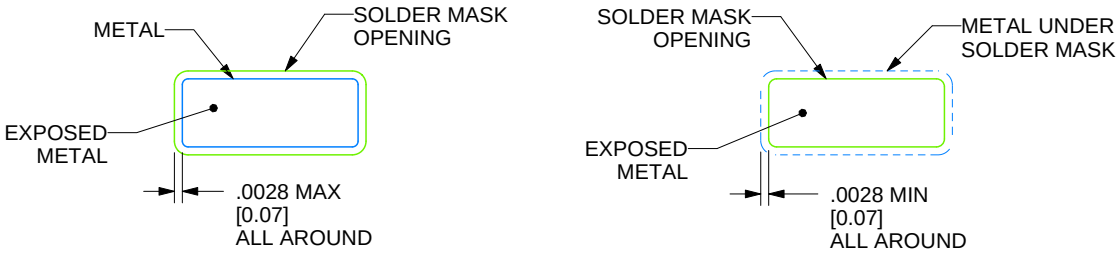


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

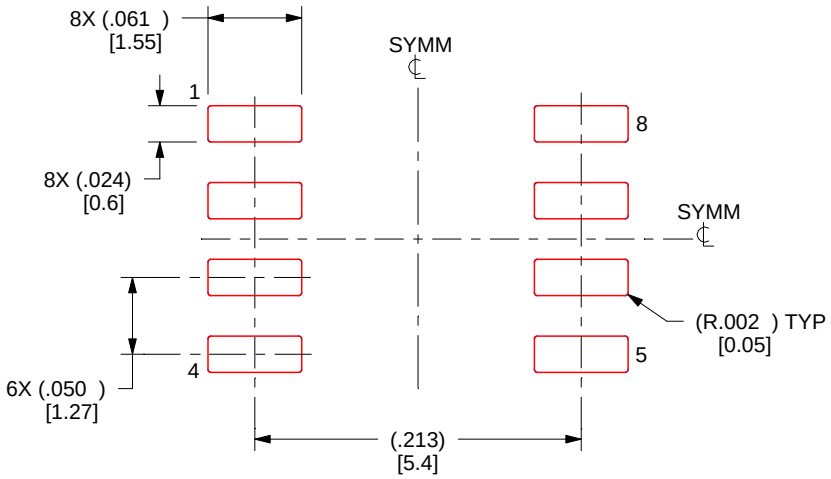
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

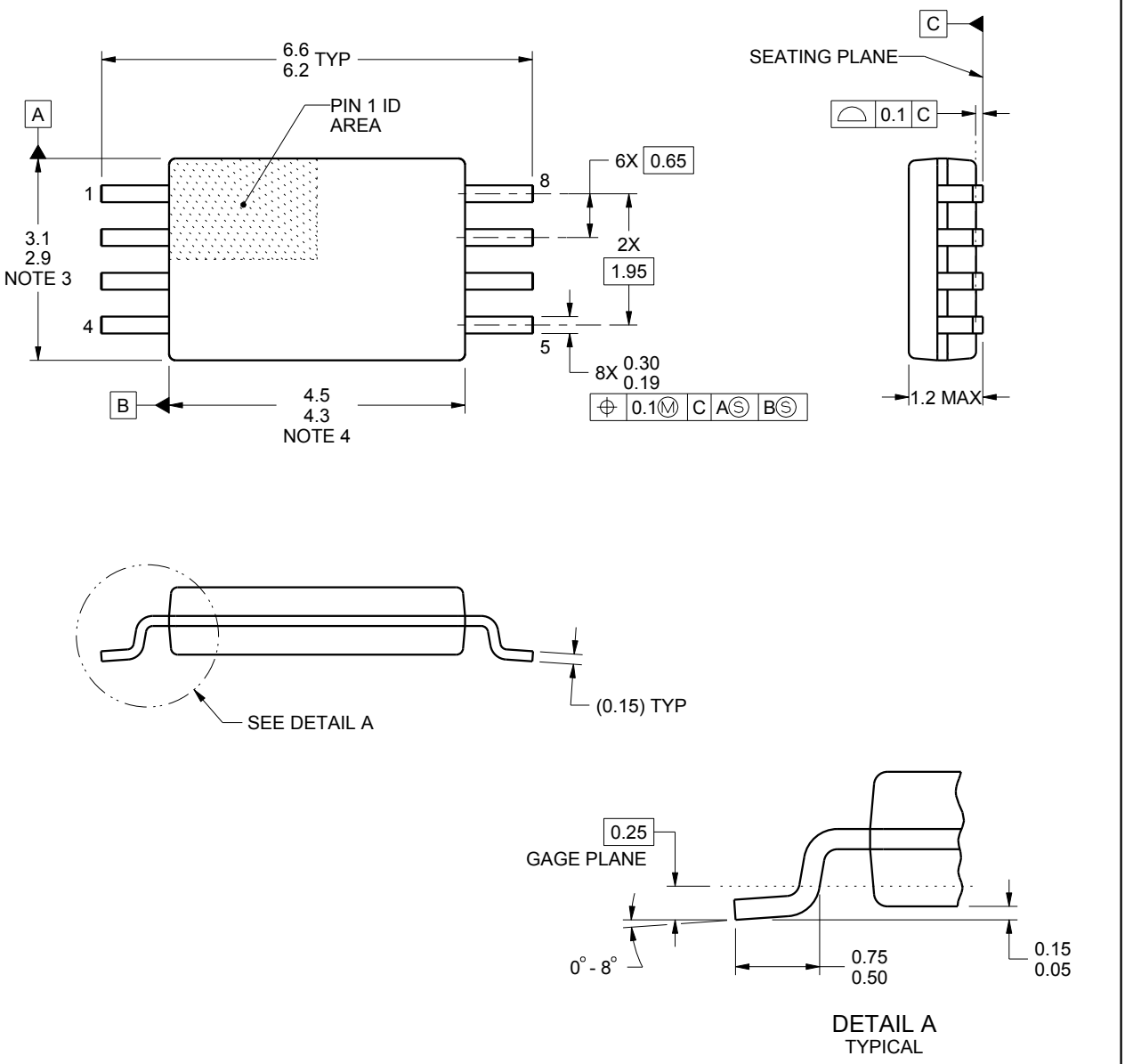
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

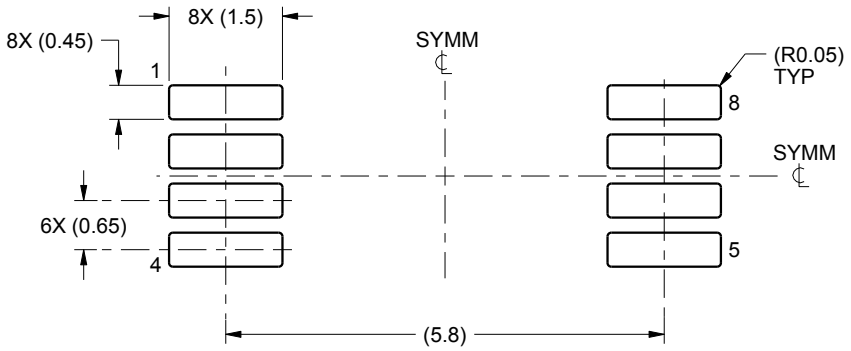
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

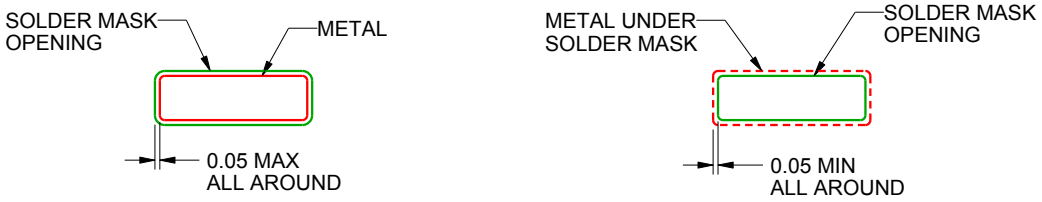


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

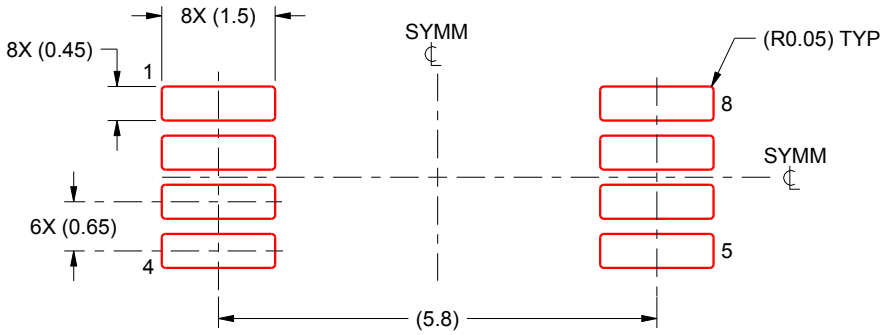


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

INA30x 36-V, Overcurrent Protection, Precision, Current-Sense Amplifiers With Dual Integrated Comparators

1 Features

- Wide common-mode input range: –0.1 V to +36 V
- Dual comparator outputs:
  - INA302: Two independent overlimit alerts
  - INA303: Window comparator
  - Threshold levels set individually
  - Comparator 1 alert response: 1 µs
  - Comparator 2 adjustable delay: 2 µs to 10 s
  - Open-drain outputs with independent latch control modes
- High accuracy amplifier:
  - Offset voltage: 30 µV (max, A3 version)
  - Offset voltage drift: 0.5 µV/°C (max)
  - Gain error: 0.15% (max, A3 version)
  - Gain error drift: 10 ppm/°C
- Available amplifier gains:
  - INA302A1, INA303A1: 20 V/V
  - INA302A2, INA303A2: 50 V/V
  - INA302A3, INA303A3: 100 V/V

2 Applications

- Overcurrent protection
- Motor control
- Power-supply protection
- Computers and servers
- Telecom equipment

3 Description

The INA302 and INA303 (INA30x) devices feature a high common-mode, bidirectional, current-sensing amplifier and two high-speed comparators to detect out-of-range current conditions. The INA302 comparators are configured to detect and respond to overcurrent conditions. The INA303 comparators are configured to respond to both overcurrent and undercurrent conditions in a windowed configuration. These devices feature an adjustable limit threshold range for each comparator set using an external limit-setting resistor. These current-shunt monitors can measure differential voltage signals on common-mode voltages that can vary from –0.1 V up to +36 V, independent of the supply.

The open-drain alert outputs can be configured to operate in either a transparent mode (output status follows the input state), or in a latched mode (alert output is cleared when the latch is reset). The alert response time for comparator 1 is under 1 µs, and the alert response for comparator 2 is set through an external capacitor ranging from 2 µs to 10 s.

These devices operate from a single 2.7-V to 5.5-V supply, drawing a maximum supply current of 950 µA. The devices are specified over the extended operating temperature range of –40°C to +125°C, and are available in a 14-pin TSSOP package.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA302	TSSOP (14)	4.40 mm × 5.00 mm
INA303		

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application

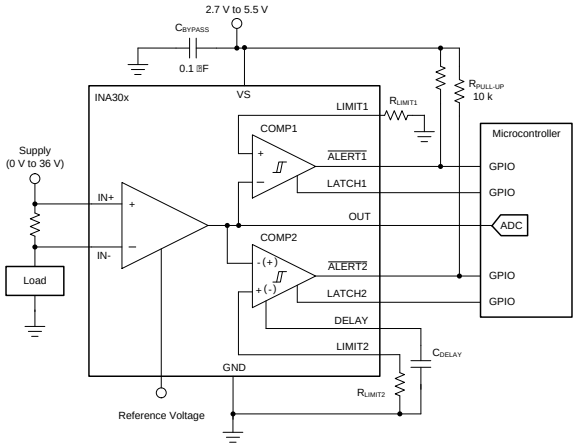


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2017) to Revision C — **Page**

- Changed locations and text of some sections for clarity; no content was changed ... 1
- Added MIN and MAX values to V_{CM} and V_S rows of *Recommended Operating Conditions* table ... 4
- Deleted V_{CM}, V_S, and temperature range rows from *Electrical Characteristics* table; same content listed in *Recommended Operating Conditions* table ... 5

Changes from Revision A (February 2017) to Revision B — **Page**

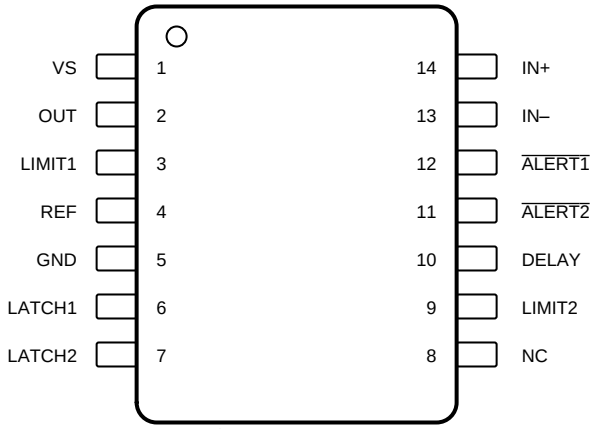
- Changed y-axis units from *0.5 V/div* to *1 V/div* and changed *(INA30xA1)* to *(INA30x)* in title of *Comparator 1 Total Propagation Delay* figure ... 12
- Changed y-axis units from *0.5 V/div* to *1 V/div* and changed *(INA303A1)* to *(INA303)* in title of *Comparator 2 Total Propagation Delay* figure ... 12
- Deleted *Comparator 1 Total Propagation Delay (INA30xA2)*, *Comparator 1 Total Propagation Delay (INA30xA3)*, *Comparator 2 Total Propagation Delay (INA303A2)*, and *Comparator 2 Total Propagation Delay (INA303A3)* figures ... 12
- Changed *(INA303A1)* to *(INA303)* in title of *Comparator 2 Total Propagation Delay* figure ... 12
- Deleted *Comparator 2 Total Propagation Delay (INA303A2)* and *Comparator 2 Total Propagation Delay (INA303A3)* figures ... 12
- Added *Comparator 2 Total Propagation Delay (INA302A1)* and *Comparator 2 Total Propagation Delay (INA302A1)* figures ... 12

Changes from Original (September 2016) to Revision A — **Page**

- Released to production ... 1

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VS	Analog	Power supply, 2.7 V to 5.5 V
2	OUT	Analog output	Output voltage
3	LIMIT1	Analog input	$\overline{\text{ALERT1}}$ threshold limit input; see the *Setting Alert Thresholds* section for details on setting the limit threshold
4	REF	Analog input	Reference voltage, 0 V to VS
5	GND	Analog	Ground
6	LATCH1	Digital input	Transparent or latch mode selection input
7	LATCH2	Digital input	Transparent or latch mode selection input
8	NC	—	No internal connection
9	LIMIT2	Analog input	$\overline{\text{ALERT2}}$ threshold limit input; see the *Setting Alert Thresholds* section for details on setting the limit threshold
10	DELAY	Analog input	Delay timing input; see the *Alert Outputs* section for details on setting the delayed alert response for comparator 2
11	$\overline{\text{ALERT2}}$	Analog output	Open-drain output; active-low. This pin is an overlimit alert for the INA302 and an underlimit alert for the INA303.
12	$\overline{\text{ALERT1}}$	Analog output	Open-drain output, active-low overlimit alert
13	IN–	Analog input	Connect to load side of the current-sensing resistor
14	IN+	Analog input	Connect to supply side of the current-sensing resistor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage			6	V
	Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–40	40	V
		Common-mode(3)	GND – 0.3	40	
	Analog input	LIMIT1, LIMIT2, DELAY, REF	GND – 0.3	(V_S) + 0.3	V
	Analog output	OUT	GND – 0.3	(V_S) + 0.3	V
	Digital input	LATCH1, LATCH2	GND – 0.3	(V_S) + 0.3	V
	Digital output	$\overline{\text{ALERT1}}$, $\overline{\text{ALERT2}}$	GND – 0.3	6	V
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage can exceed the voltage shown without causing damage to the device if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–0.1	12	36	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA30x PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = 0 V, V_{REF} = V_S / 2, V_S = 5 V, V_{IN+} = 12 V, V_{LIMIT1} = 3 V, and V_{LIMIT2} = 3 V (INA302) or 2 V (INA303) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{IN}	Differential input voltage range	V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A1 versions	0		±125	mV
		V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A2 versions	0		±50	
		V_{IN} = V_{IN+} – $V_{IN–}$, V_{REF} = V_S / 2, A3 versions	0		±25	
CMRR	Common-mode rejection ratio	V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C, A1 versions	100	114		dB
		V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C, A2 versions	106	118		
		V_{IN+} = 0 V to 36 V, T_A = –40°C to +125°C, A3 versions	110	120		
V_{OS}	Offset voltage, RTI[1]	A1 versions		±15	±80	µV
		A2 versions		±10	±50	
		A3 versions		±5	±30	
dV_{OS}/dT	Offset voltage drift, RTI[1]	T_A= –40°C to +125°C		0.02	0.25	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A = –40°C to +125°C		±0.3	±5	µV/V
I_B	Input bias current	I_{B+}, $I_{B–}$		115		µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.01		µA
OUTPUT						
G	Gain	A1 versions		20		V/V
		A2 versions		50		
		A3 versions		100		
	Gain error	V_{OUT} = 0.5 V to V_S – 0.5 V, A1 versions		±0.02%	±0.075%	
		V_{OUT} = 0.5 V to V_S – 0.5 V, A2 versions		±0.05%	±0.1%	
		V_{OUT} = 0.5 V to V_S – 0.5 V, A3 versions		±0.1%	±0.15%	
		T_A= –40°C to +125°C		3	10	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		500		pF
VOLTAGE OUTPUT						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_S – 0.05	V_S – 0.1	V
	Swing to GND	R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 15	V_{GND} + 30	mV
FREQUENCY RESPONSE						
BW	Bandwidth	A1 versions, C_{OUT} = 500 pF		550		kHz
		A2 versions, C_{OUT} = 500 pF		440		
		A3 versions, C_{OUT} = 500 pF		400		
SR	Slew rate			4		V/µs
NOISE, RTI[1]						
	Voltage noise density			30		nV/√Hz

(1) RTI = referred-to-input.

Electrical Characteristics (continued)

at T_A = 25°C, V_{SENSE} = 0 V, V_{REF} = V_S / 2, V_S = 5 V, V_{IN+} = 12 V, V_{LIMIT1} = 3 V, and V_{LIMIT2} = 3 V (INA302) or 2 V (INA303) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPARATOR						
t_p	Total alert propagation delay	Comparator 1, input overdrive = 1 mV		0.6	1	µs
		Comparator 2, input overdrive = 1 mV, delay = 100 kΩ to V_S		1.25	2	
	Slew-rate-limited t_p	Comparator 1, V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V		1	1.5	µs
		Comparator 2 (INA302), V_{OUT} step = 0.5 V to 4.5 V, V_{LIMIT} = 4 V, delay = 100 kΩ to V_S		1.5	2.5	
		Comparator 2 (INA303), V_{OUT} step = 4.5 V to 0.5 V, V_{LIMIT} = 1 V, delay = 100 kΩ to V_S		1.5	2.5	
I_{LIMIT1}	Limit threshold output current, comparator 1	T_A = 25°C, V_{LIMIT1} < V_S – 0.6 V	79.2	80	80.8	µA
		T_A = –40°C to +125°C, V_{LIMIT1} < V_S – 0.6 V	78.4		81.6	
I_{LIMIT2}	Limit threshold output current, comparator 2	T_A = 25°C, V_{LIMIT2} < V_S – 0.6 V	79.7	80	80.4	µA
		T_A = –40°C to +125°C, V_{LIMIT2} < V_S – 0.6 V	79.2		80.8	
V_{OS}	Offset voltage, both comparators	A1 versions		0.5	3.5	mV
		A2 versions		0.5	3.5	
		A3 versions		0.5	4.0	
HYS	Hysteresis	comparator 1, comparator 2		100		mV
	Internal programmable delay error	T_A = –40°C to +125°C			4%	
V_{TH}	Delay threshold voltage	T_A = –40°C to +125°C	1.21	1.22	1.23	V
I_D	Delay charging current	T_A = –40°C to +125°C, V_{DELAY} = 0.6 V	4.85	5	5.15	µA
R_D	Delay discharge resistance			70		Ω
V_{IH}	LATCH1, LATCH2 high-level input voltage	T_A = –40°C to +125°C	1.4		6	V
V_{IL}	LATCH1, LATCH2 low-level input voltage	T_A = –40°C to +125°C	0		0.4	V
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA, T_A = –40°C to +125°C		70	400	mV
	$\overline{ALERT1}$, $\overline{ALERT2}$ pin leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	LATCH1, LATCH2 digital leakage input current	0 V ≤ V_{LATCH1} , V_{LATCH2} ≤ V_S		1		µA
POWER SUPPLY						
I_Q	Quiescent current	T_A = 25°C		850	950	µA
		T_A = –40°C to +125°C			1150	

6.6 Typical Characteristics

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

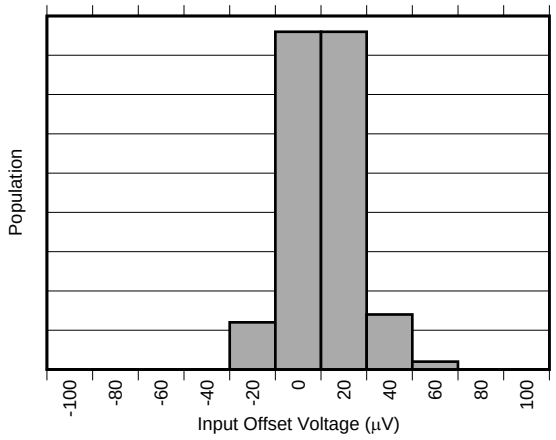


Figure 1. Input Offset Voltage Distribution (INA30xA1)

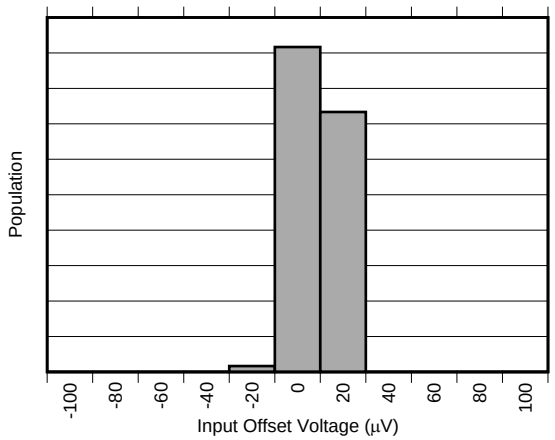


Figure 2. Input Offset Voltage Distribution (INA30xA2)

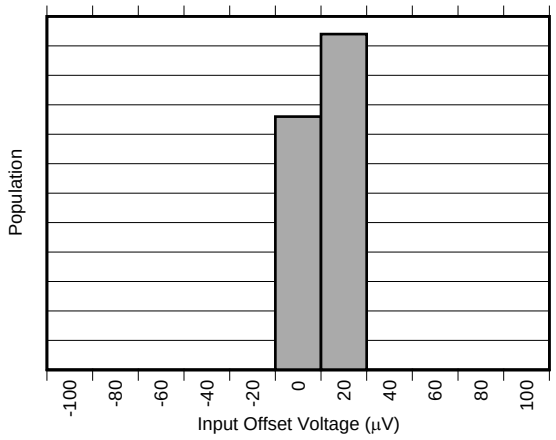


Figure 3. Input Offset Voltage Distribution (INA30xA3)

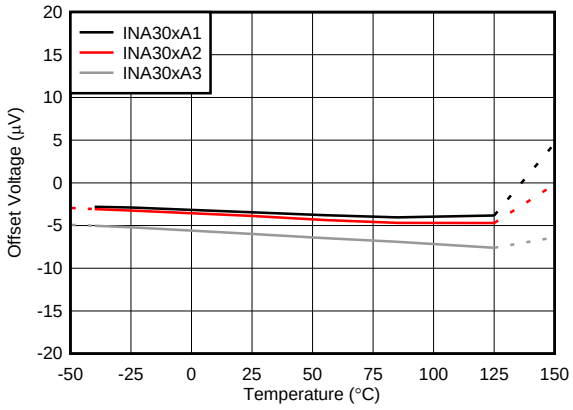


Figure 4. Input Offset Voltage vs Temperature

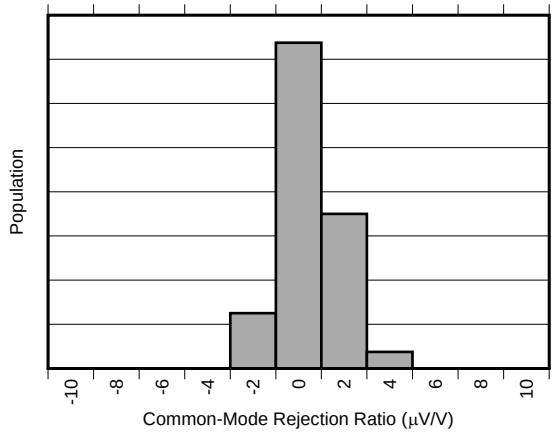


Figure 5. CMRR Distribution (INA30xA1)

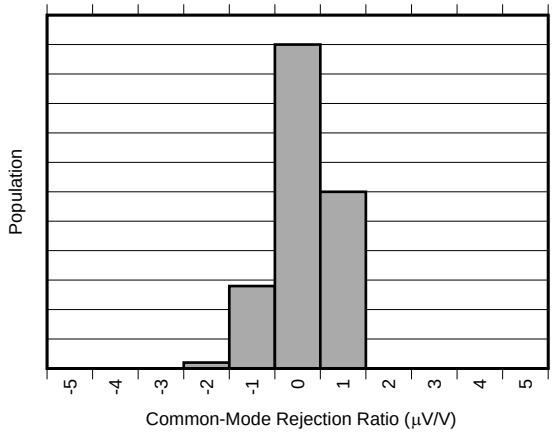


Figure 6. CMRR Distribution (INA30xA2)

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

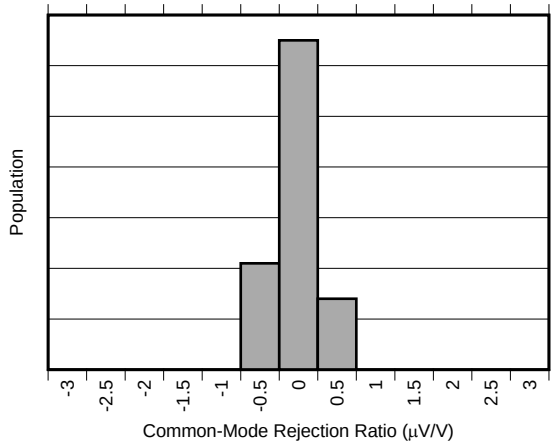


Figure 7. CMRR Distribution (INA30xA3)

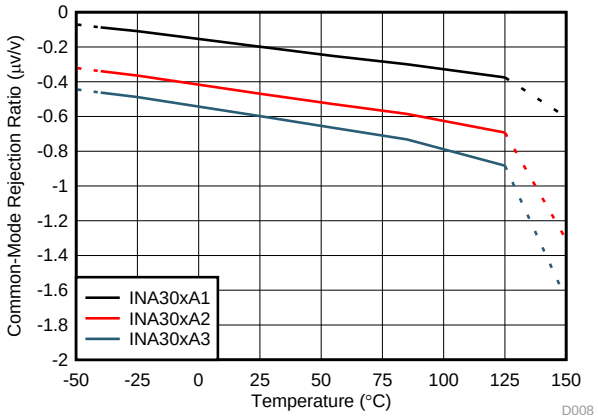


Figure 8. CMRR vs Temperature

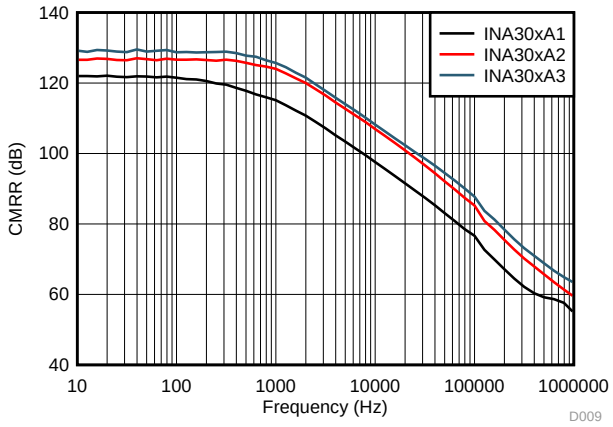


Figure 9. CMRR vs Frequency

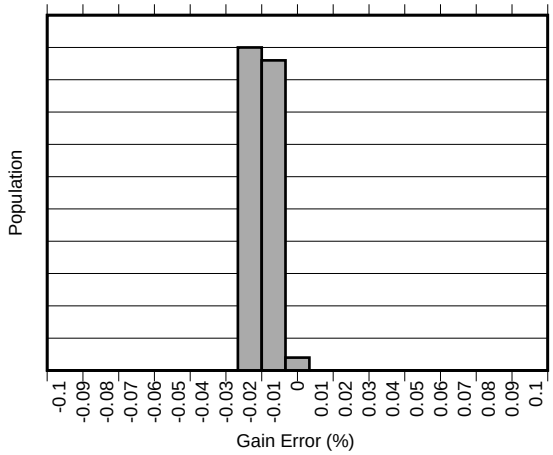


Figure 10. Gain Error Distribution (INA30xA1)

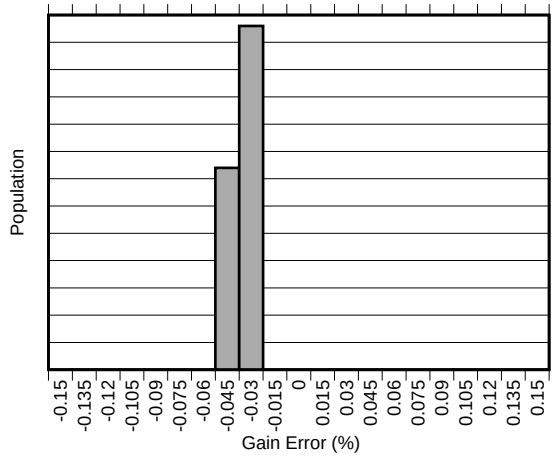


Figure 11. Gain Error Distribution (INA30xA2)

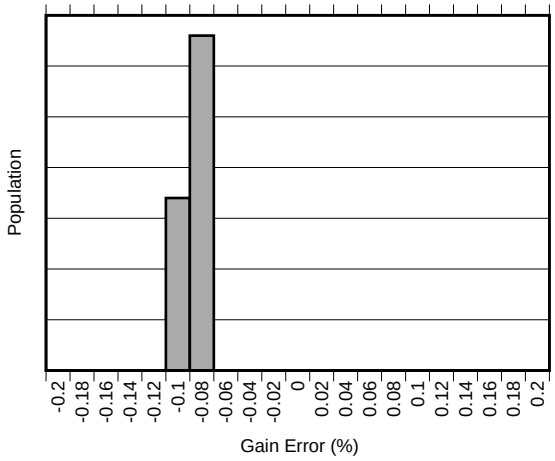


Figure 12. Gain Error Distribution (INA30xA3)

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

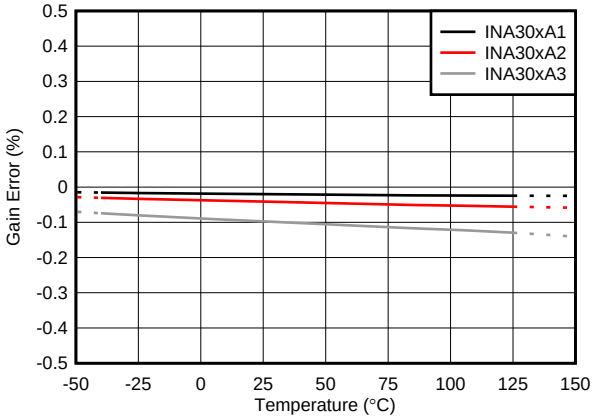


Figure 13. Gain Error vs Temperature

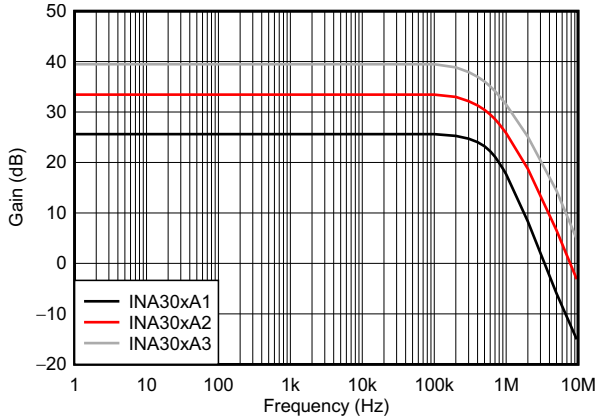


Figure 14. Gain vs Frequency

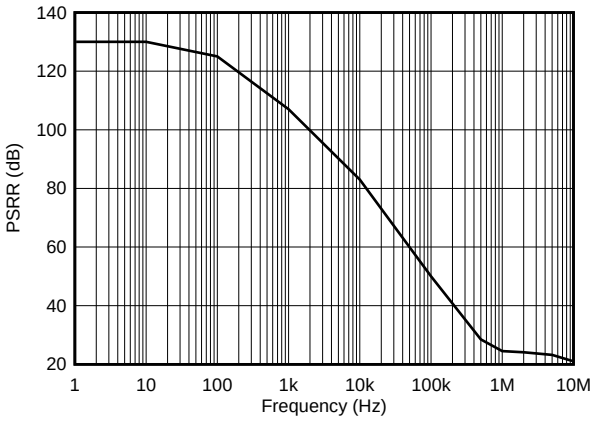


Figure 15. PSRR vs Frequency

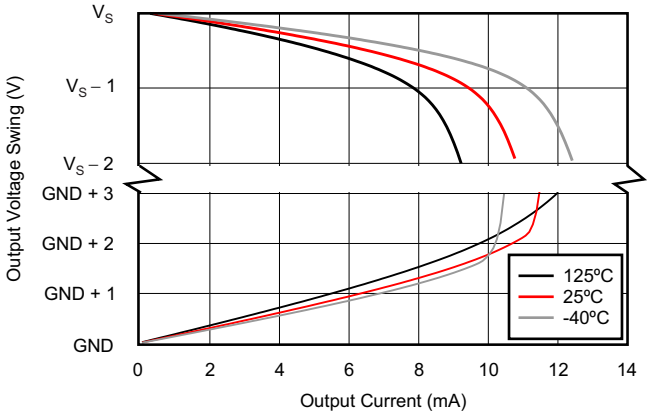


Figure 16. Output Voltage Swing vs Output Current

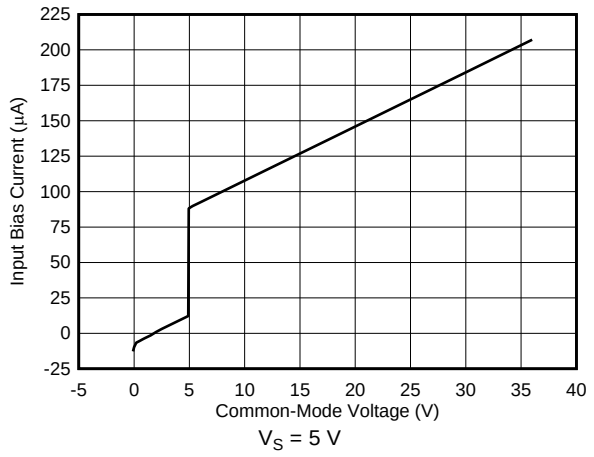


Figure 17. Input Bias Current vs Common-Mode Voltage

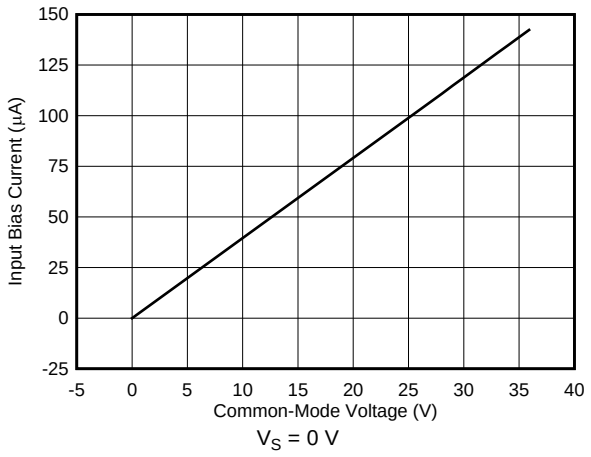


Figure 18. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

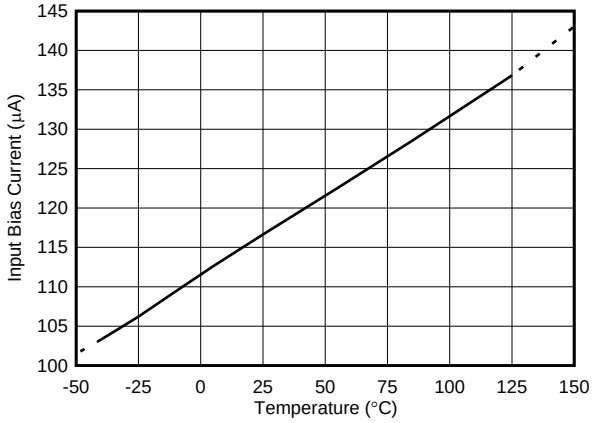


Figure 19. Input Bias Current vs Temperature

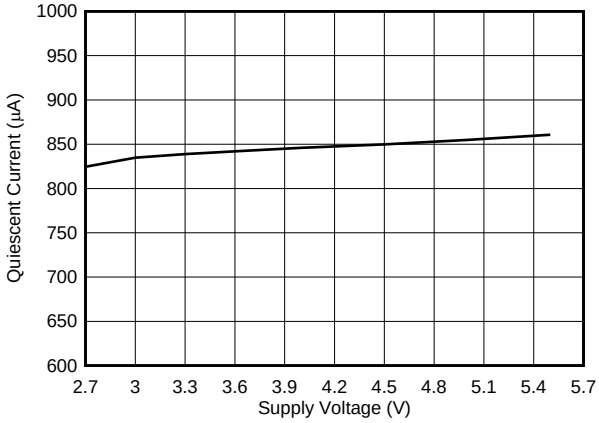


Figure 20. Quiescent Current vs Supply Voltage

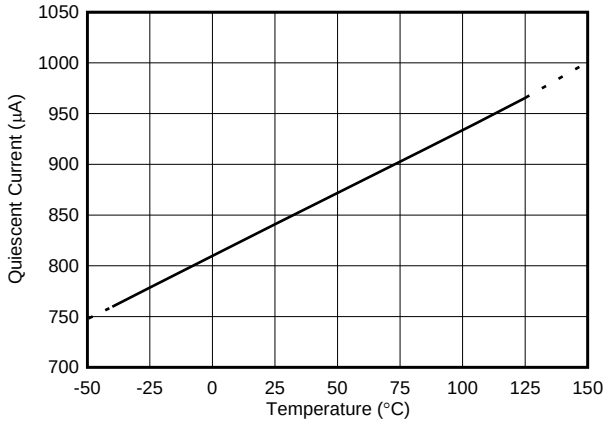


Figure 21. Quiescent Current vs Temperature

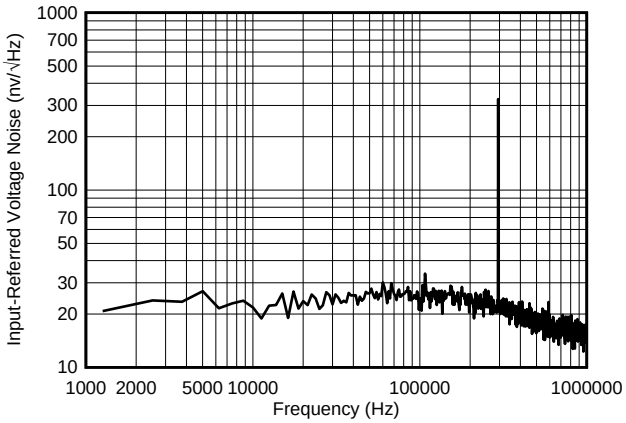


Figure 22. Input-Referred Voltage Noise vs Frequency

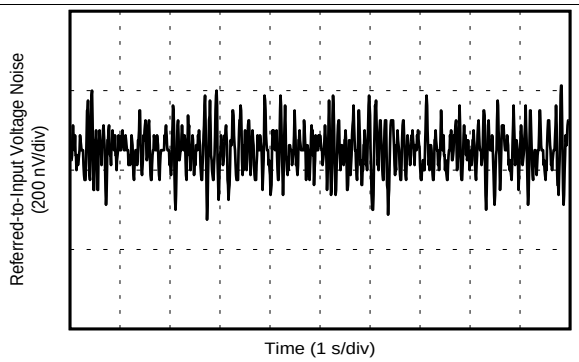


Figure 23. 0.1-Hz to 10-Hz Voltage Noise (Referred to Input)

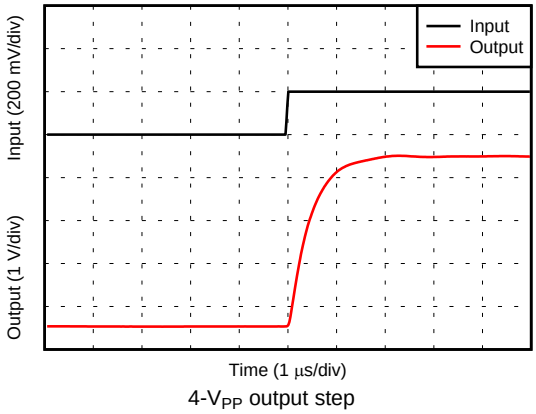


Figure 24. Voltage Output Rising Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

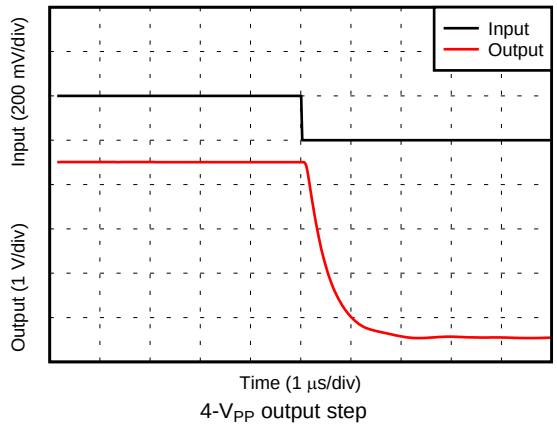


Figure 25. Voltage Output Falling Step Response

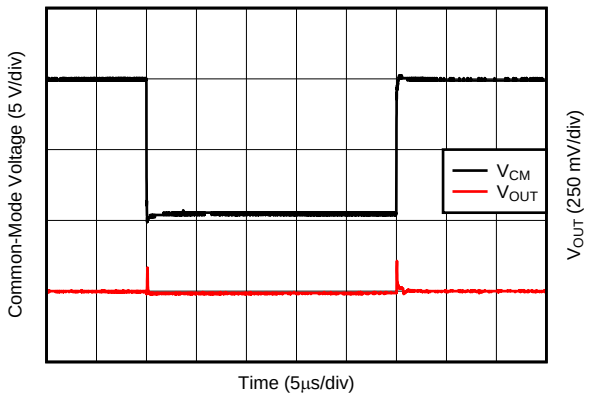


Figure 26. Common-Mode Voltage Transient Response

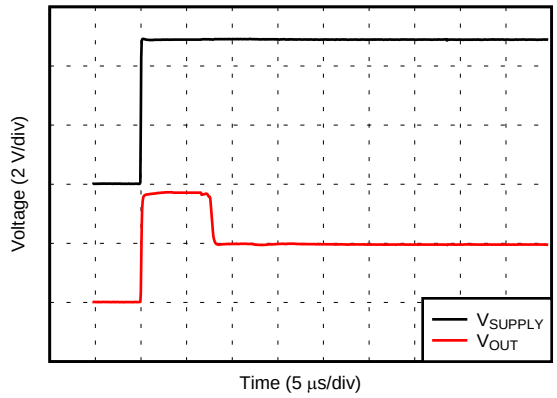


Figure 27. Start-Up Response

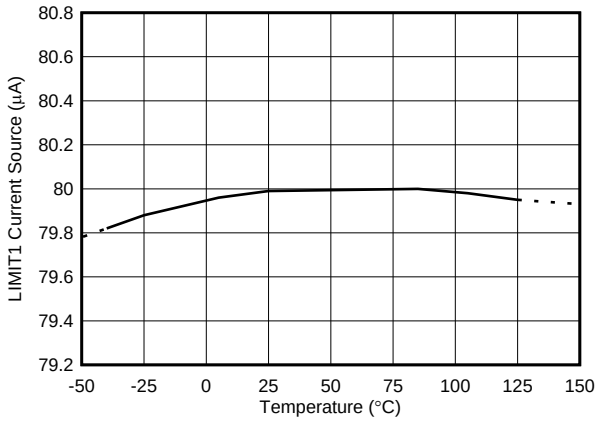


Figure 28. LIMIT1 Current Source vs Temperature

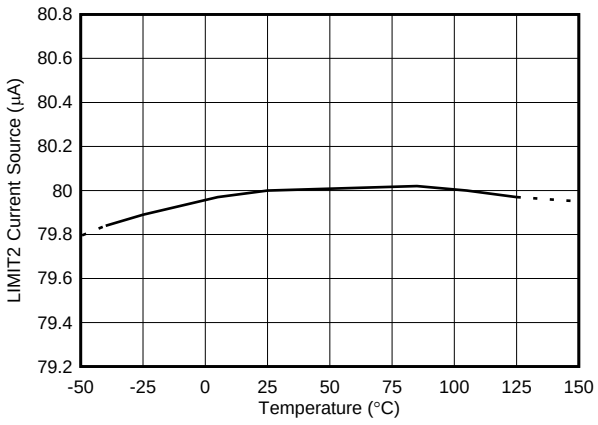


Figure 29. LIMIT2 Current Source vs Temperature

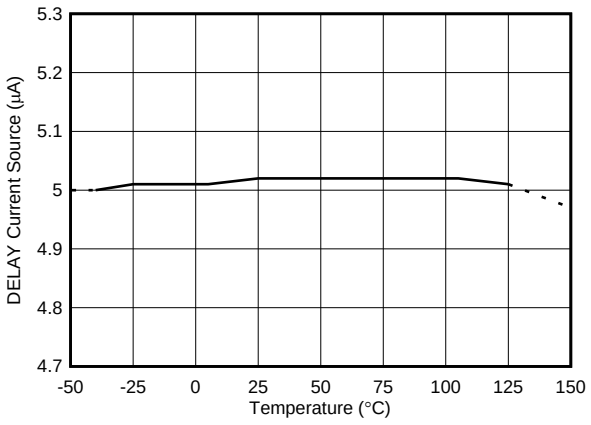


Figure 30. DELAY Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

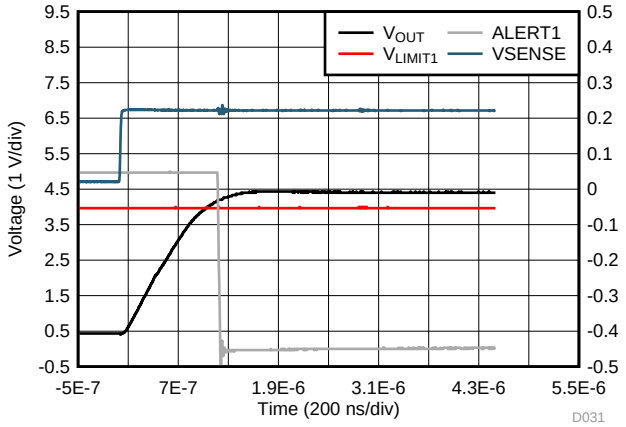


Figure 31. Comparator 1 Total Propagation Delay (INA30x)

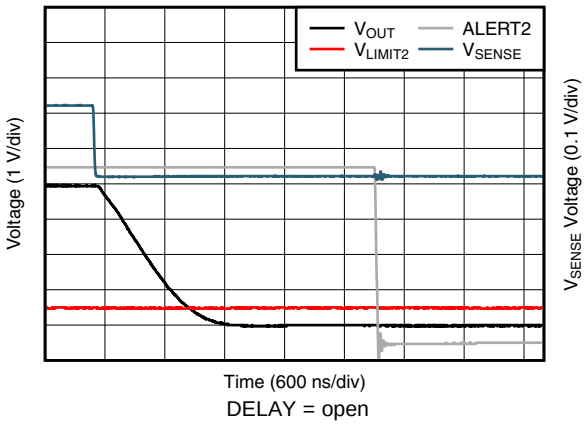


Figure 32. Comparator 2 Total Propagation Delay (INA303)

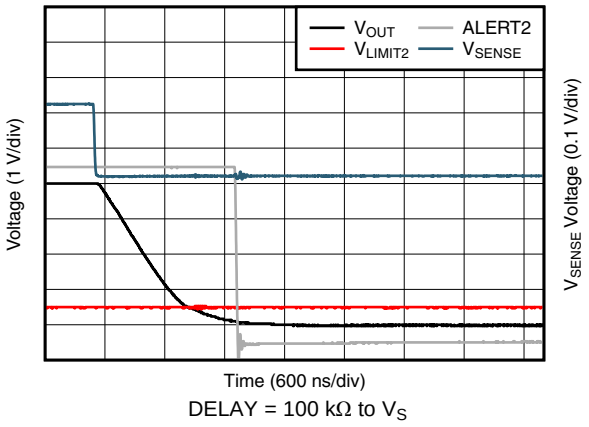


Figure 33. Comparator 2 Total Propagation Delay (INA303)

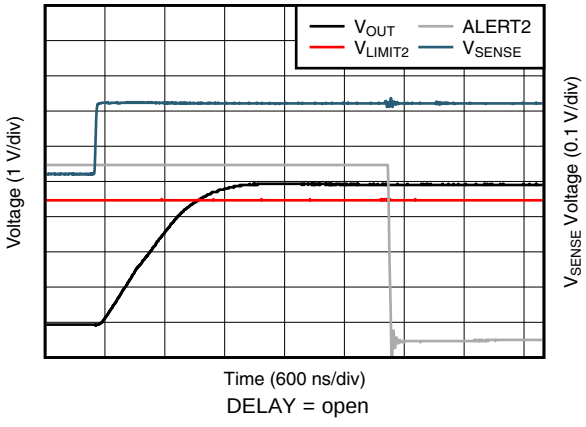


Figure 34. Comparator 2 Total Propagation Delay (INA302)

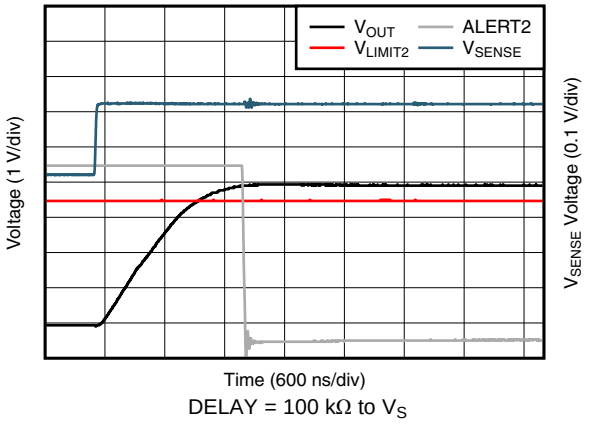


Figure 35. Comparator 2 Total Propagation Delay (INA302)

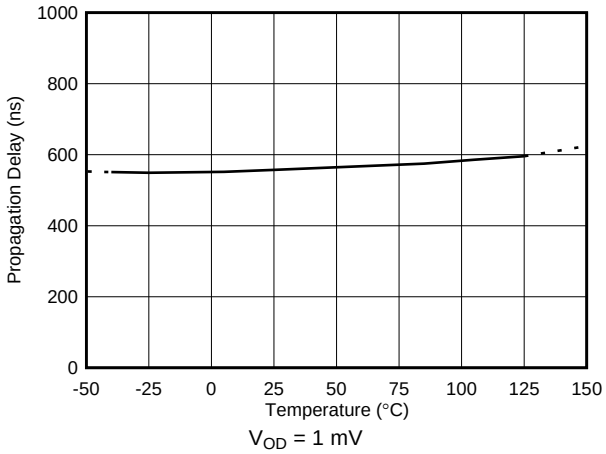


Figure 36. Comparator 1 Propagation Delay vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{REF} = V_S / 2, V_{SENSE} = 0 V, V_S = 5 V, V_{IN+} = 12 V, and $\overline{ALERT1}$, $\overline{ALERT2}$ pullup resistors = 10 kΩ (unless otherwise noted)

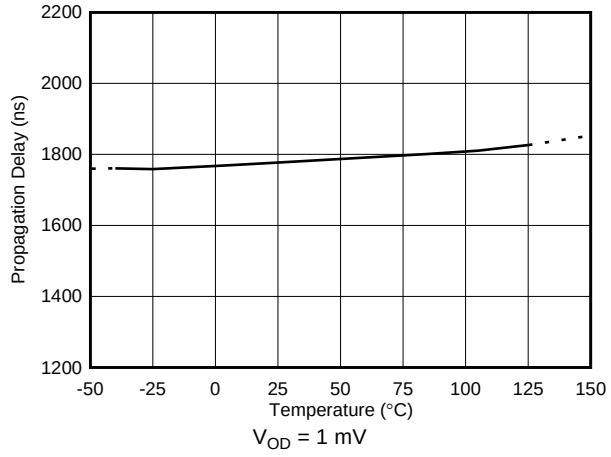


Figure 37. Comparator 2 Propagation Delay vs Temperature

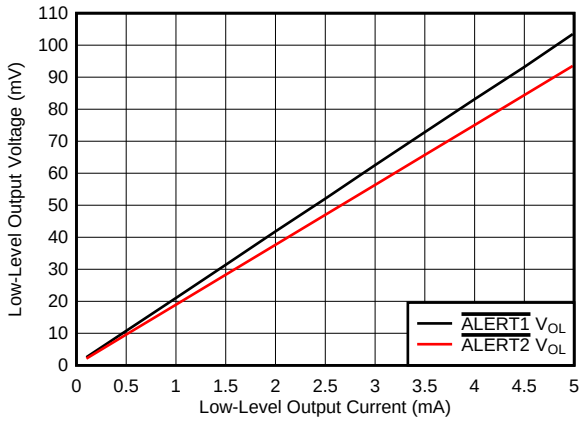


Figure 38. Comparator Alert V_{OL} vs I_{OL}

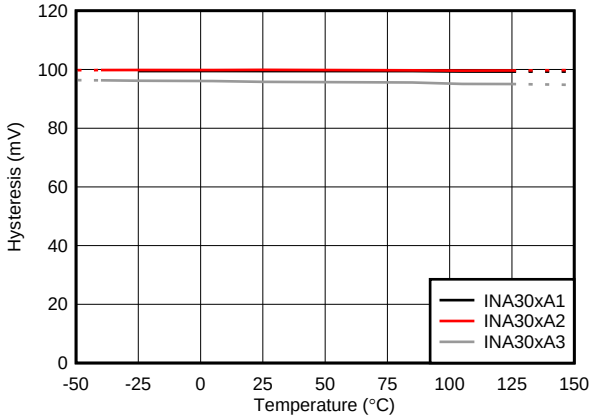


Figure 39. Comparator 1 Hysteresis vs Temperature

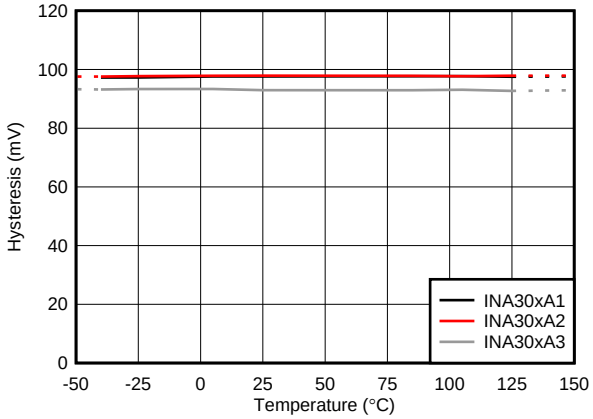


Figure 40. Comparator 2 Hysteresis vs Temperature

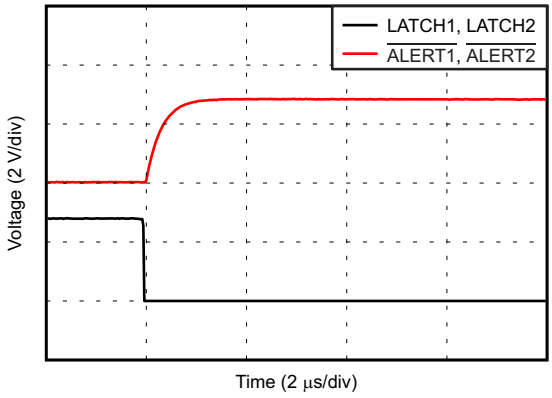


Figure 41. Comparator Latch Response

7 Detailed Description

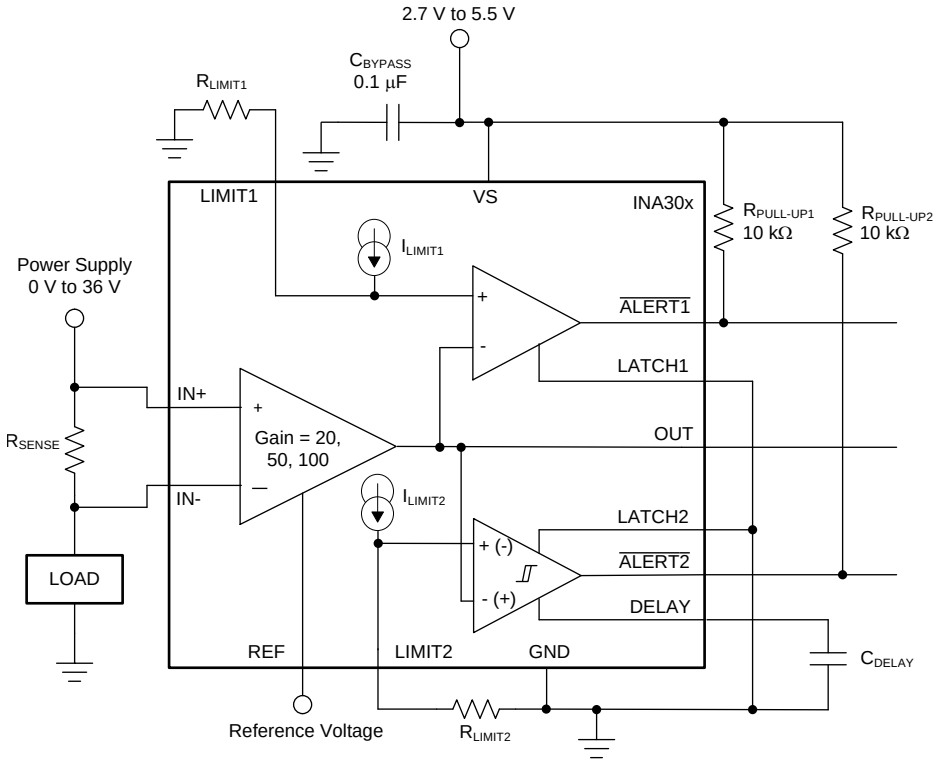
7.1 Overview

The INA30x feature a zero-drift, 36-V, common-mode, bidirectional, current-sensing amplifier, and two high-speed comparators that can detect multiple out-of-range current conditions. These specially designed, current-sensing amplifiers can be used in both low-side or high-side applications where common-mode voltages far exceed the supply voltage of the device. Currents are measured by accurately sensing voltages developed across current-sensing resistors (also known as *current-shunt resistors*). Current can be measured on input voltage rails as high as 36 V, and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 30 μV (max) with a temperature contribution of only 0.25 μV/°C (max) over the full temperature range of –40°C to +125°C. The low total offset voltage of the INA302 enables smaller current-sense resistor values to be used, improving power-efficiency without sacrificing measurement accuracy resulting from the smaller input signal.

Both devices use a single external resistor to set each out-of-range threshold. The INA302 allows for two overcurrent thresholds, and the INA303 allows for both an undercurrent and overcurrent threshold. The response time of the ALERT1 threshold is fixed and is less than 1 μs. The response time of the ALERT2 threshold can be set with an external capacitor. The combination of a precision current-sense amplifier with onboard comparators creates a highly-accurate solution that is capable of fast detection of multiple out-of-range conditions. The ability to detect when currents are out-of-range allows the system to take corrective actions to prevent potential component or system-wide damage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bidirectional Current Sensing

The INA30x sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage. Likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The equation for the output voltage of the current-sense amplifier is shown in Equation 1.

$$V_{OUT} = \left(I_{LOAD} \times R_{SENSE} \times GAIN\right) + V_{REF}$$

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the device selected.
- V_{REF} is the voltage applied to the REF pin. (1)

7.3.2 Out-of-Range Detection

The INA303 detects when negative currents are out-of-range by setting a voltage at the LIMIT2 pin that is less than the applied reference voltage. The limit voltage is set with an external resistor or externally driven by a voltage source or digital-to-analog converter (DAC); see the *Setting Alert Thresholds* section for additional information. A typical application using the INA303 to detect negative overcurrent conditions is illustrated in the *Typical Application* section.

7.3.3 Alert Outputs

Both $\overline{\text{ALERTx}}$ pins are active-low, open-drain outputs that pull low when the sensed current is detected to be out of range. Both open-drain $\overline{\text{ALERTx}}$ pins require an external pullup resistor to an external supply. The external supply for the pullup voltage can exceed the supply voltage, V_S, but is restricted from operating at greater than 5.5 V. The pullup resistance is selected based on the capacitive load and required rise time; however, a 10-kΩ resistor value is typically sufficient for most applications. The response time of the $\overline{\text{ALERT1}}$ output to an out-of-range event is less than 1 µs, and the response time of the $\overline{\text{ALERT2}}$ output is proportional to the value of the external C_{DELAY} capacitor. The equation to calculate the delay time for the $\overline{\text{ALERT2}}$ output is given in Equation 2:

$$t_{DELAY} = \begin{cases} 1.5\ \mu s & \text{If DELAY is connected to VS with 100 k}\Omega \\ \dfrac{C_{DELAY} \times V_{TH}}{I_D} + 2.5\ \mu s & \text{If } C_{DELAY} \geq 47\ pF \end{cases}$$

where

- C_{DELAY} is the external delay capacitor.
- V_{TH} is the delay threshold voltage.
- I_D is the DELAY pin current for comparator 2. (2)

For example, if a delay time of 10 µs is desired, the calculated value for C_{DELAY} is 492 pF. The closest standard capacitor value to the calculated value is 500 pF. If a delay time greater than 2.5 µs on the $\overline{\text{ALERT2}}$ output is not needed, the C_{DELAY} capacitor can be omitted. To achieve minimum delay on the $\overline{\text{ALERT2}}$ output, connect a 100-kΩ resistor from the DELAY pin to the VS pin. Both comparators in the INA30x have hysteresis to avoid oscillations in the $\overline{\text{ALERTx}}$ outputs. The effect hysteresis has on the comparator behavior is described in the *Hysteresis* section.

Feature Description (continued)

Figure 42 shows the alert output response of the internal comparators for the INA302. When the output voltage of the current-sense amplifier is less than the voltage developed on either limit pin, both ALERTx outputs are in the default high state. When the current sense amplifier output is greater than the threshold voltage set by the LIMIT2 pin, the ALERT2 output pulls low after a delay time set by the external delay capacitor. The lower overcurrent threshold is commonly referred to as the *overcurrent warning threshold*. If the current continues to rise until the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin, then the ALERT1 output becomes active and immediately pulls low. The low voltage on ALERT1 indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent condition has occurred. The upper threshold is commonly referred to as the *fault* or *system critical threshold*. Systems often initiate protection procedures (such as a system shutdown) when the current exceeds this threshold.

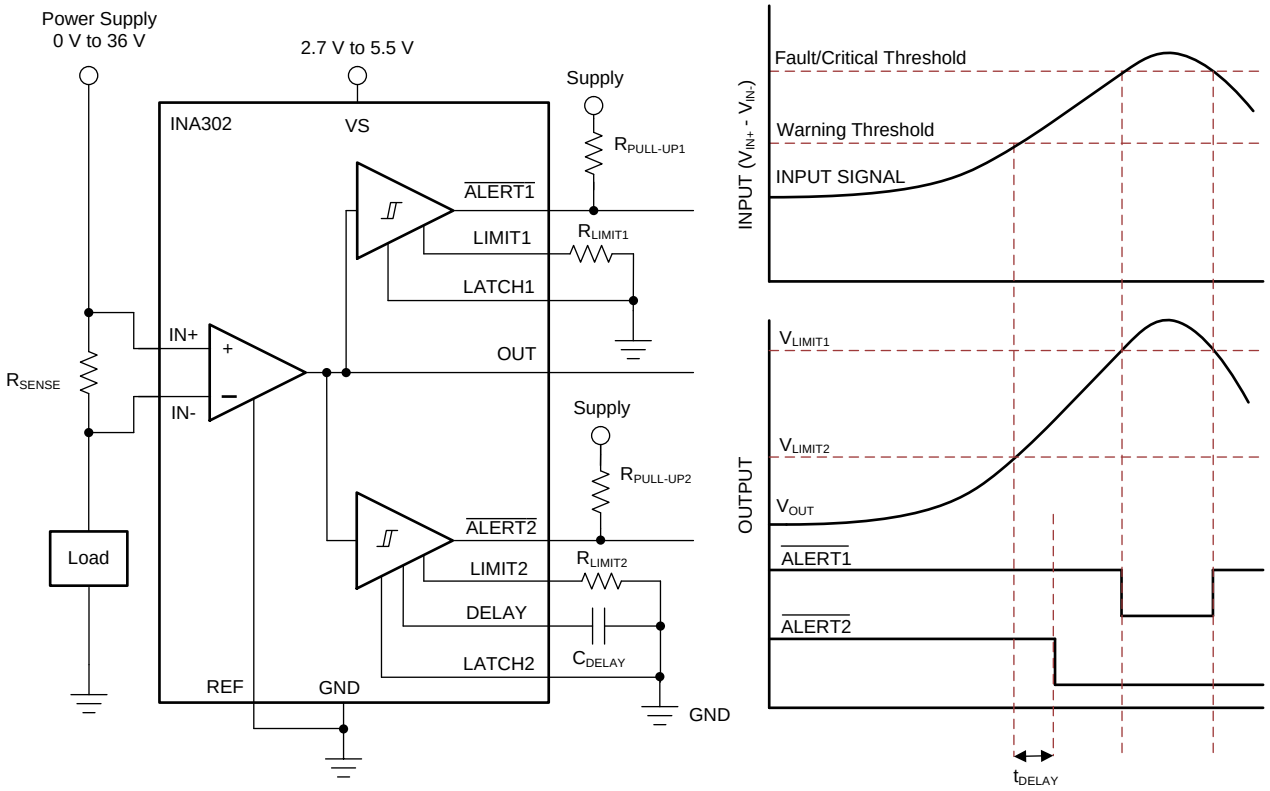


Figure 42. Out-of-Range Alert Responses for the INA302

Feature Description (continued)

Figure 43 shows the alert output response of the internal comparators for the INA303. Both $\overline{\text{ALERT}}$x outputs are in the default high state when the output voltage of the current-sense amplifier is less than the voltage developed at the LIMIT1 pin and is greater than the voltage developed at the LIMIT2 pin. The $\overline{\text{ALERT1}}$ output becomes active and pulls low when the current-sense amplifier output voltage exceeds the threshold voltage set at the LIMIT1 pin. The low voltage on $\overline{\text{ALERT1}}$ indicates that the measured signal at the amplifier input has exceeded the programmed threshold level, indicating an overcurrent or out-of-range condition has occurred. When the current-sense amplifier output is less than the threshold voltage set by the LIMIT2 pin, the $\overline{\text{ALERT2}}$ output pulls low after the delay time set by the external delay capacitor expires. The delay time for the $\overline{\text{ALERT2}}$ output is proportional to the value of the external C_{DELAY} capacitor, and is calculated by Equation 2.

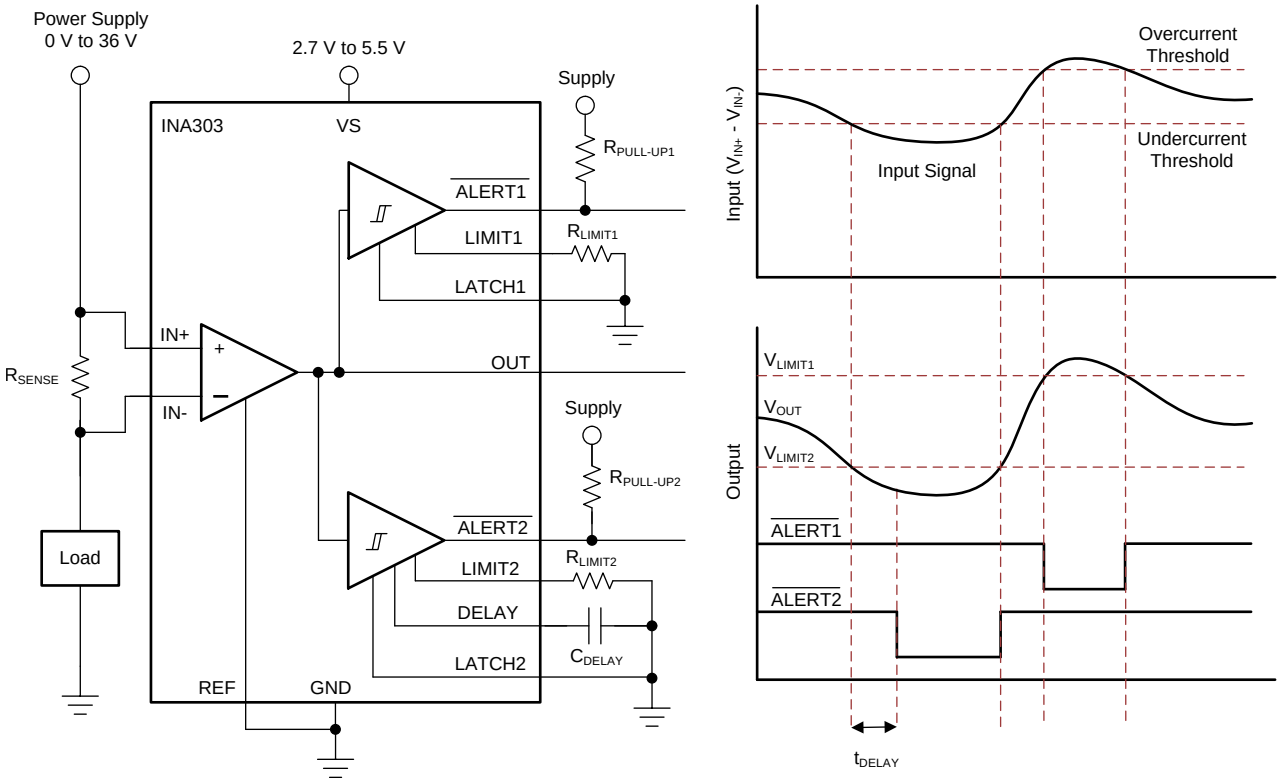


Figure 43. Out-of-Range Alert Responses for the INA303

Feature Description (continued)

Figure 44 shows the alert output response of the INA303 when the two $\overline{\text{ALERT}}$x pins are connected together. When configured in this manner, the INA303 can provide a single signal to indicate when the sensed current is operating either outside the normal operating bands or within a normal operational window. Both $\overline{\text{ALERT1}}$ and $\overline{\text{ALERT2}}$ outputs behave the same in regard to the alert mode. The difference with $\overline{\text{ALERT2}}$ is that the transition of the output state is delayed by the time set by the external delay capacitor. If the overcurrent or undercurrent event is not present when the delay time expires, $\overline{\text{ALERT2}}$ does not respond.

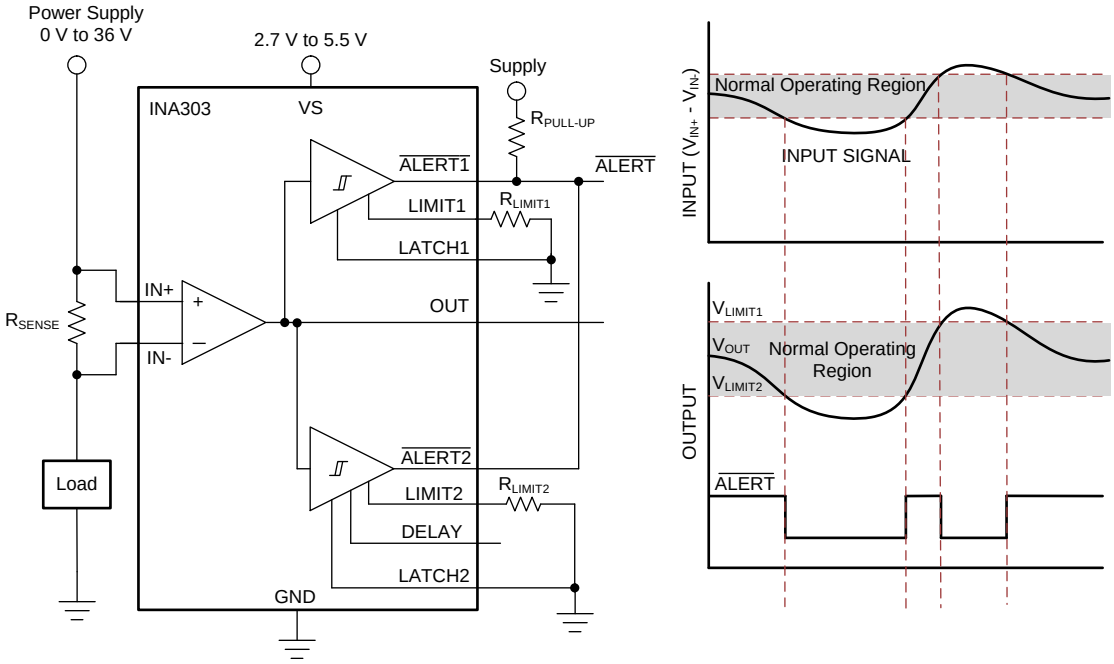


Figure 44. Current Window Comparator Implementation With the INA303

Feature Description (continued)

7.3.3.1 Setting Alert Thresholds

The INA30x family of devices determines if an out-of-range event is present by comparing the amplifier output voltage to the voltage at the corresponding LIMITx pin. The threshold voltage for the LIMITx pins can be set using a single external resistor or by connecting an external voltage source to each pin. The INA302 allows setting limits for two overcurrent conditions. Generally, the lower overcurrent threshold is referred to as a *warning limit* and the higher overcurrent threshold is referred to as the *critical* or *fault limit*. The INA303 allows setting thresholds to detect both undercurrent and overcurrent limit conditions.

7.3.3.1.1 Resistor-Controlled Current Limit

The typical approach to set the limit threshold voltage is to connect resistors from the two LIMITx pins to ground. The voltage developed across the R_{LIMIT1}, R_{LIMIT2} resistors represents the desired fault current value at which the corresponding $\overline{\text{ALERT}}$x pin becomes active. The values for the R_{LIMIT1}, R_{LIMIT2} resistors are calculated using Equation 3:

$$R_{LIMIT} = \frac{\left(I_{TRIP} \times R_{SENSE} \times GAIN\right) + V_{REF}}{I_{LIMIT}} \quad (3)$$

where

- I_{TRIP} is the desired out-of-range current threshold.
- R_{SENSE} is the current-sensing resistor.
- GAIN is the gain option of the device selected.
- V_{REF} is the voltage applied to the REF pin.
- I_{LIMIT} is the limit threshold output current for the selected comparator, typically 80 µA.

NOTE

When solving for the value of R_{LIMIT}, the voltage at the corresponding LIMITx pin as determined by the product of R_{LIMIT} and I_{LIMIT} must not exceed the compliance voltage of V_S – 0.6 V.

7.3.3.1.1.1 Resistor-Controlled Current Limit: Example

For example, if the current level indicating an out-of-range condition (I_{TRIP}) is 20 A and the current-sense resistor value (R_{SENSE}) is 10 mΩ, then the input threshold signal is 200 mV. The INA302A1 has a gain of 20, so the resulting output voltage at the 20-A input condition is 4 V at the output of the current-sense amplifier when the REF pin is grounded. The value for R_{LIMIT} is selected to allow the device to detect this 20-A threshold, indicating that an overcurrent event has occurred. When the INA302 detects this out-of-range condition, the $\overline{\text{ALERT}}$x pin asserts and pulls low. For this example, the value of R_{LIMIT} to detect a 4-V level is calculated to be 50 kΩ.

Feature Description (continued)

7.3.3.1.2 Voltage-Source-Controlled Current Limit

The second method for setting the out-of-range threshold is to directly drive the LIMITx pins with a programmable DAC or other external voltage source. The benefit of this method is the ability to adjust the current-limit threshold to account for different threshold voltages used for different system operating conditions. For example, this method can be used in a system with one current-limit threshold level that must be monitored during a power-up sequence, but different threshold levels must be monitored during other system operating modes.

The voltage applied at the LIMITx pins sets the threshold voltage for out-of-range detection. The value of the voltage for a given desired current trip point is calculated using Equation 4:

$$V_{SOURCE} = \left(I_{TRIP} \times R_{SENSE} \times GAIN\right) + V_{REF} \quad (4)$$

where

- I_{TRIP} is the desired out-of-range current threshold.
- R_{SENSE} is the current-sensing resistor.
- GAIN is the gain option of the device selected.
- V_{REF} is the voltage applied to the REF pin.

NOTE

The maximum voltage that can be applied to the LIMIT2 pin is V_S – 0.6 V and the maximum voltage that can be applied to the LIMIT1 pin must not exceed V_S.

7.3.3.2 Hysteresis

The hysteresis included in the comparators of the INA30x reduces the possibility of oscillations in the alert outputs when the measured signal level is near the overlimit threshold level. For overrange events, the corresponding ALERTx pin is asserted when the output voltage (V_{OUT}) exceeds the threshold set at either LIMITx pin. The output voltage must drop to less than the LIMITx pin threshold voltage by the hysteresis value in order for the ALERTx pin to deassert and return to the nominal high state. Likewise for underrange events, the corresponding ALERTx pin is also pulled low when the output voltage drops to less than the threshold set by either LIMITx pin. The ALERTx pin is released when the output voltage of the current-sense amplifier rises to greater than the set threshold plus hysteresis. Hysteresis functionality for both overrange and underrange events is shown in Figure 45 and Figure 46 for the INA302 and INA303, respectively.

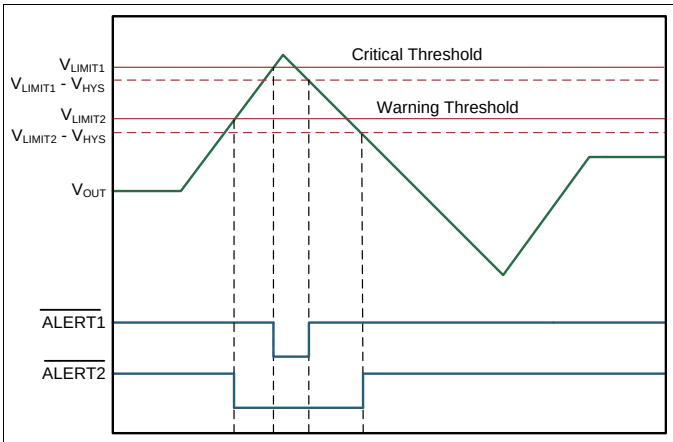


Figure 45. Comparator Hysteresis Behavior (INA302)

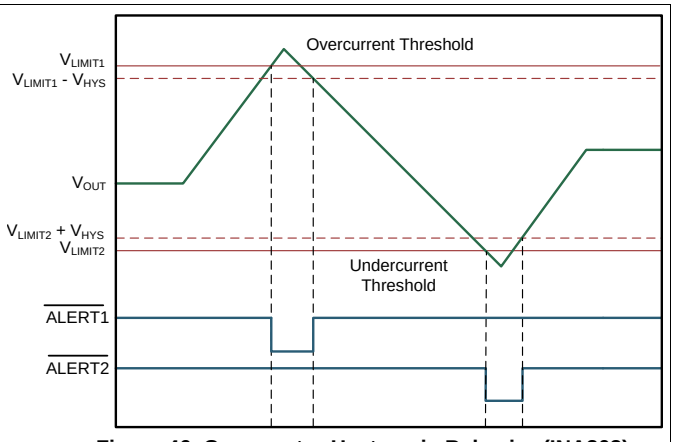


Figure 46. Comparator Hysteresis Behavior (INA303)

7.4 Device Functional Modes

7.4.1 Alert Operating Modes

Each comparator has two output operating modes: transparent and latched. These modes determine how the ALERTx pins respond when an out-of-range condition is removed. The device is placed into either transparent or latched state based on the voltage applied to the corresponding LATCHx pin, as shown in Table 1.

Table 1. Output Mode Settings

OUTPUT MODE	LATCHx PINS SETTINGS
ALERTx transparent mode	LATCHx = low
ALERTx latch mode	LATCHx = high

7.4.1.1 Transparent Output Mode

The comparators are set to transparent output mode when the corresponding LATCHx pin is pulled low. When set to transparent mode, the output of the comparators changes and follows the input signal with respect to the programmed alert threshold. For example, when the amplifier output violates the set limit value, the ALERTx output pin is pulled low. As soon as the differential input signal drops to less than the alert threshold, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the ALERTx pins to a hardware interrupt input on a microcontroller. The ALERTx pin is pulled low as soon as an out-of-range condition is detected, thus notifying the microcontroller. The microcontroller immediately reacts to the alert and takes action to address the overcurrent condition. In transparent output mode, there is no need to latch the state of the alert output because the microcontroller responds as soon as the out-of-range condition occurs.

7.4.1.2 Latch Output Mode

The comparators are set to latch output mode when the corresponding LATCHx pin is pulled high. Some applications do not continuously monitor the state of the ALERTx pins as described in the *Transparent Output Mode* section. For example, if the device is set to transparent output mode in an application that only polls the state of the ALERTx pins periodically, then the transition of the ALERTx pins can be missed when the out-of-range condition is not present during one of these periodic polling events. Latch output mode allows the output of the comparators to latch the output of the range condition so that the transition of the ALERTx pins is not missed when the status of the comparator ALERTx pins is polled.

The difference between latch mode and transparent mode is how the alert output responds when an overcurrent condition is removed. In transparent mode (LATCH1, LATCH2 = low), when the differential input signal drops to within normal operating range, the ALERTx pin returns to the default high setting to indicate that the overcurrent event has ended.

In latch mode (LATCHx = high), when an out-of-range condition is detected and the corresponding ALERTx pin is pulled low; the ALERTx pin does not return to the default high state when the out-of-range condition is removed. In order to clear the alert, the corresponding LATCHx pin must be pulled low for at least 100 ns. Pulling the LATCHx pins low allows the corresponding ALERTx pin to return to the default high level, provided the out-of-range condition is no longer present. If the out-of-range condition is still present when the LATCHx pins are pulled low, then the corresponding ALERTx pin remains low. The ALERTx pins can be cleared (reset to high) by toggling the corresponding LATCHx pin when the alert condition is detected by the system controller.

The latch and transparent modes are illustrated in Figure 47. As illustrated in this figure, at time t_1, the current-sense amplifier exceeds the limit threshold. During this time the LATCH1 pin is toggled with no affect to the ALERT1 output. The state of the LATCH1 pin only matters when the output of the current-sense amplifier returns to the normal operating region, as shown at t_2. At this time the LATCH1 pin is high and the overcurrent condition is latched on the ALERT1 output. As shown in the time interval between t_2 and t_3, the latch condition is cleared when the LATCHx pin is pulled low. At time t_4, the LATCH1 pin is already pulled low when the amplifier output drops below the limit threshold for the second time. The device is set to transparent mode at this point and the ALERT1 pin is pulled back high as soon as the output of the current-sense amplifier drops below the alert threshold.

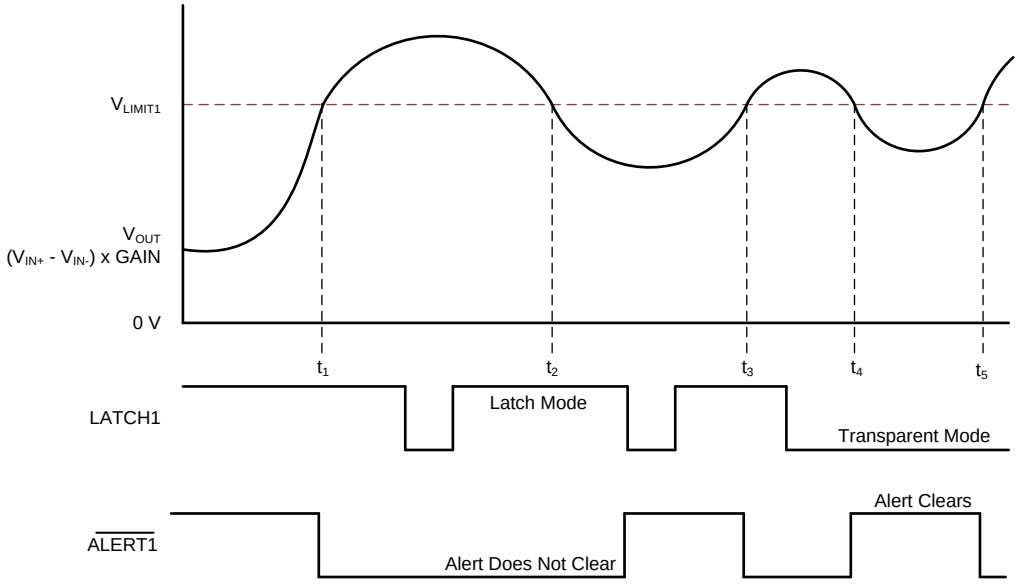


Figure 47. Transparent versus Latch Mode

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Selecting a Current-Sensing Resistor (R_{SENSE})

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow for more accurate measurements to be made. Amplifiers have fixed internal errors that are largely dominated by the inherent input offset voltage. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured. Therefore, the use of larger-value, current-sensing resistors inherently improves measurement accuracy.

However, a system design trade-off must be evaluated through the use of larger input signals for improving measurement accuracy. Increasing the current-sense resistor value results in an increase in power dissipation across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming more widely available with values reaching down to 200 μΩ or lower, with power dissipations of up to 5 W that enable large currents to be accurately monitored with sensing resistors.

8.1.1.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires 2.5% accuracy for detecting a 10-A overcurrent event where only 250 mW is allowed for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit-setting resistor (R_{LIMIT}) is a 1% component, and the maximum tolerance specification for the internal threshold setting current source (1%) is used. Given the total error budget of 2.5%, up to 0.5% of error can be attributed to the measurement error of the device under these conditions.

Application Information (continued)

As shown in Table 2, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 2.5% maximum total overcurrent detection error to reduce the value of the current-sensing resistor and to further reduce power dissipation. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% and stays within the accuracy region.

Table 2. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
DESIGN TARGETS				
I_{MAX}	Maximum current		10	A
P_{D_MAX}	Maximum allowable power dissipation		250	mW
	Allowable current threshold accuracy		2.5%	
DEVICE PARAMETERS				
V_{OS}	Offset voltage		30	µV
E_G	Gain error		0.15%	
CALCULATIONS				
R_{SENSE_MAX}	Maximum allowable R_{SENSE}	P_{D_MAX} / I_{MAX}^2	2.5	mΩ
V_{OS_ERROR}	Initial offset voltage error	$(V_{OS} / (R_{SENSE\_MAX} \times I_{MAX}) \times 100$	0.12%	
$ERROR_{TOTAL}$	Total measurement error	$\sqrt{(V_{OS\_ERROR}^2 + E_G^2)}$	0.19%	
$ERROR_{INITIAL}$	Initial threshold error	I_{LIMIT} tolerance + R_{LIMIT} tolerance	2%	
$ERROR_{AVAILABLE}$	Maximum allowable measurement error	Maximum error – $ERROR_{INITIAL}$	1%	
$V_{OS\_ERROR\_MAX}$	Maximum allowable offset error	$\sqrt{(ERROR_{AVAILABLE}^2 - E_G^2)}$	0.48%	
V_{DIFF_MIN}	Minimum differential voltage	$V_{OS} / V_{OS\_ERROR\_MAX\ (1\%)}$	6.3	mV
R_{SENSE_MIN}	Minimum sense resistor value	V_{DIFF_MIN} / I_{MAX}	0.63	mΩ
P_{D_MIN}	Lowest-possible power dissipation	$R_{SENSE\_MIN} \times I_{MAX}^2$	63	mW

8.1.2 Input Filtering

The integrated comparators in the INA30x are very accurate at detecting out-of-range events because of the low offset voltage; however, noise present at the input of the current-sense amplifier and noise internal to the device can make the offset appear larger than specified. The most obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily falsely interpret this transient as an overrange condition.

External filtering helps reduce the amount of noise that reaches the comparator and reduce the likelihood of a false alert from occurring because of external noise. The trade-off to adding this noise filter is that the alert response time is increased because the input signal and the noise are filtered. Figure 48 shows the implementation of an input filter for the device.

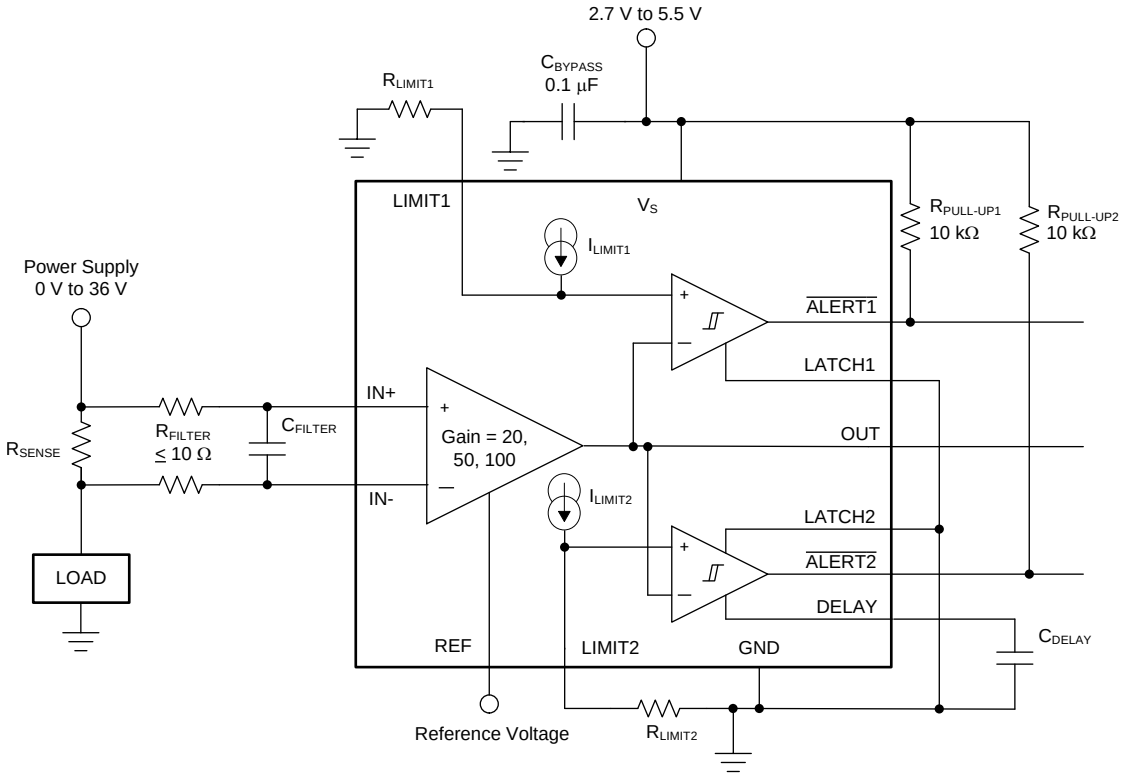


Figure 48. Input Filter Implementation

Limiting the amount of input resistance used in this filter is important because this resistance can have a significant effect on the input signal that reaches the device input pins by adversely affecting the gain error of the device. A typical system implementation involves placing the current-sensing resistor very near the device so the traces are very short and the trace impedance is very small. This layout helps reduce coupling of additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal effect on device performance.

As shown in Figure 49, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device that allows common-mode input voltages to far exceed the device supply voltage range. When input filter resistors are placed in series with the unequal input bias currents, unequal voltage drops are developed across the input resistors. The difference between these two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input pins. Smaller-value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

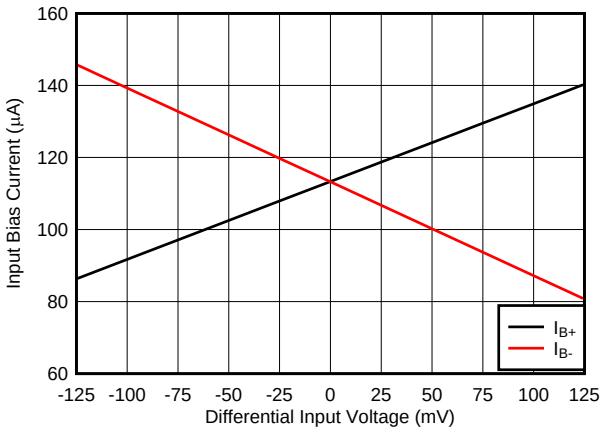
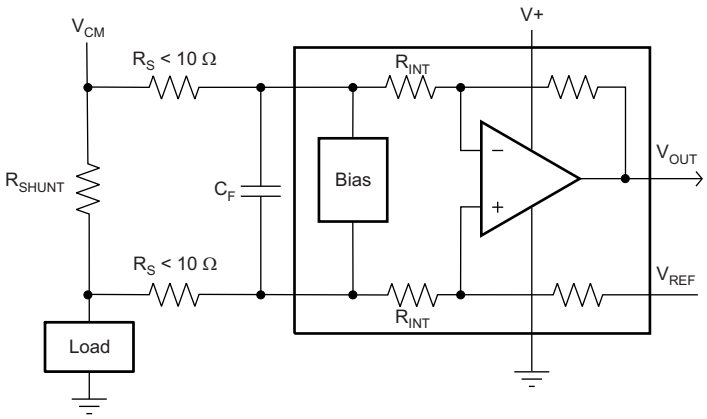


Figure 49. Input Bias Current vs Differential Input Voltage

The internal bias network present at the input pins shown in Figure 50 is responsible for the mismatch in input bias currents that is shown in Figure 49. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement is calculated using Equation 6, where the gain error factor is calculated using Equation 5.



NOTE: Comparators omitted for simplicity.

Figure 50. Filter at Input Pins

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as illustrated in Figure 50). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in Equation 5:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (5)$$

where

- R_{INT} is the internal input resistor (R3 and R4).
- R_S is the external series resistance.

With the adjustment factor from Equation 5, including the device internal input resistance, this factor varies with each gain version, as shown in Table 3. Each individual device gain error factor is shown in Table 4.

Table 3. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA30xA1	20	12.5
INA30xA2	50	5
INA30xA3	100	2.5

Table 4. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA30xA1	$\frac{12{,}500}{(11 \times R_S) + 12{,}500}$
INA30xA2	$\frac{1000}{R_S + 1000}$
INA30xA3	$\frac{2500}{(3 \times R_S) + 2500}$

The gain error that is expected from the addition of the external series resistors is then calculated based on Equation 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

For example, using an INA302A2 and the corresponding gain error equation from Table 4, a series resistance of 10 Ω results in a gain error factor of 0.99. The corresponding gain error is then calculated using Equation 6, resulting in a gain error of approximately 1% solely because of the external 10-Ω series resistors.

8.1.3 Using the INA30x With Common-Mode Transients Greater Than 36 V

With a small amount of additional circuitry, these devices can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the zener diode, as shown in Figure 51. Keep these resistors as small as possible, preferably 10 Ω or less. Larger values can be used with an additional induced error resulting from a reduced signal that actually reaches the device input pins. Many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating available because this circuit limits only short-term transients. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

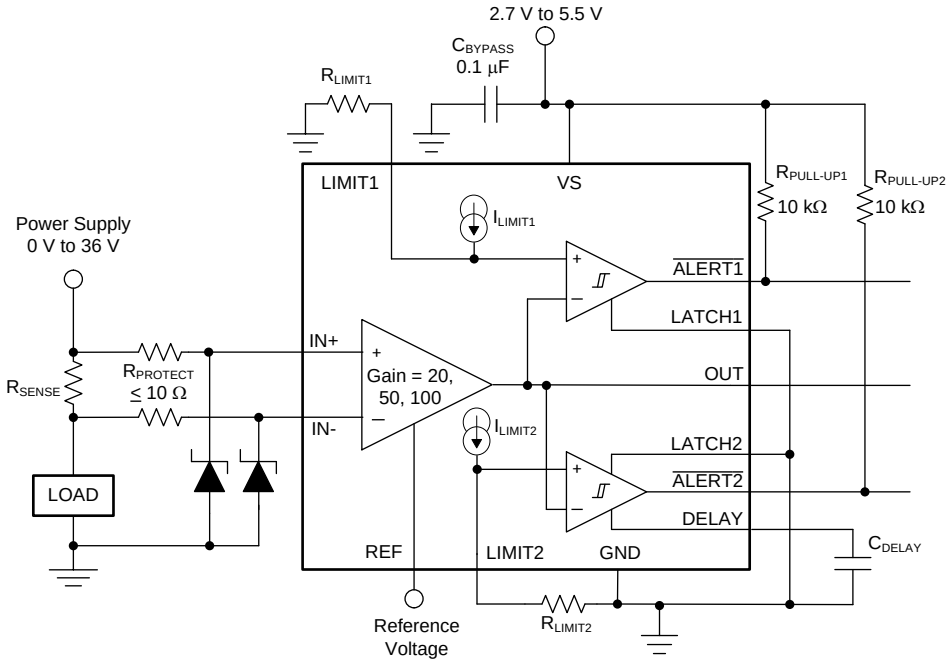


Figure 51. Transient Protection

8.2 Typical Application

The INA30x are designed to be easily configured for detecting multiple out-of-range current conditions in an application. These devices are capable of monitoring and providing overcurrent detection of bidirectional currents. By using the REF pin of the INA303, both positive and negative overcurrent events can be detected.

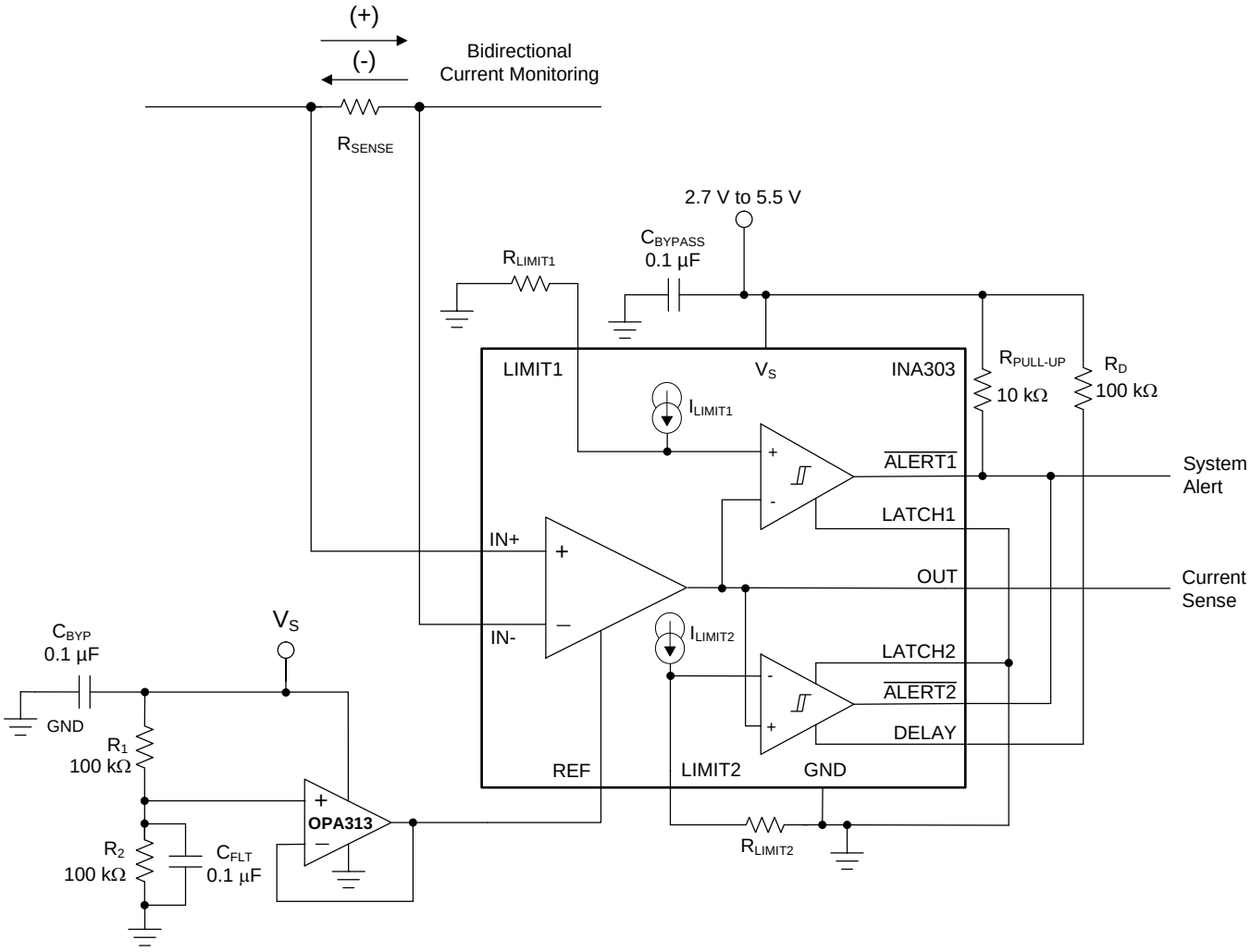


Figure 52. Bidirectional Application

Typical Application (continued)

8.2.1 Design Requirements

To allow for bidirectional monitoring, the INA303 requires a voltage applied to the REF pin. A voltage that is half of the supply voltage is usually preferred to allow for maximum output swing in both the positive and negative current direction. To reduce the errors in the reference voltage, drive the REF pin with a low-impedance source (such as an op amp or external reference). A low-value resistor divider can be used at the expense of quiescent current and accuracy. For this design, a single alert output is preferred, so both $\overline{\text{ALERT1}}$ and $\overline{\text{ALERT2}}$ are connected together and use a single pullup resistor.

8.2.2 Detailed Design Procedure

To achieve bidirectional monitoring, drive the reference pin halfway between the supply with a resistor divider buffered by an op amp, as shown in Table 5. To reduce the current draw from the supply, use 100-kΩ resistors to create the divide-by-two voltage divider. The TLV313-Q1 is selected to buffer the voltage divider because this device can operate from a single-supply rail with low I_Q and offset voltage. To minimize the response time of the $\overline{\text{ALERT2}}$ output, a 100-kΩ pullup resistor was added from the DELAY pin to the VS pin. Select values for R_{SENSE}, R_{LIMIT2}, and R_{LIMIT1} based on the desired current-sense levels and trip thresholds using the information in the *Resistor-Controlled Current Limit* and *Selecting a Current-Sensing Resistor (R_{SENSE})* sections. For this example, the values of R_{LIMIT1} and R_{LIMIT2} were selected so that the positive and negative overcurrent thresholds are the same. Table 5 shows the alert output of the INA303 application circuit with the capability to detect both positive and negative overcurrent conditions.

Table 5. Bidirectional Overcurrent Output Status

OVERCURRENT PROTECTION (OCP) STATUS	OUTPUT
Positive overcurrent detection (OCP+)	0
Negative overcurrent detection (OCP–)	0
Normal operation (no OCP)	1

8.2.3 Application Curve

Figure 53 shows the INA303 device being used in a bidirectional configuration to detect both negative and positive overcurrent events.

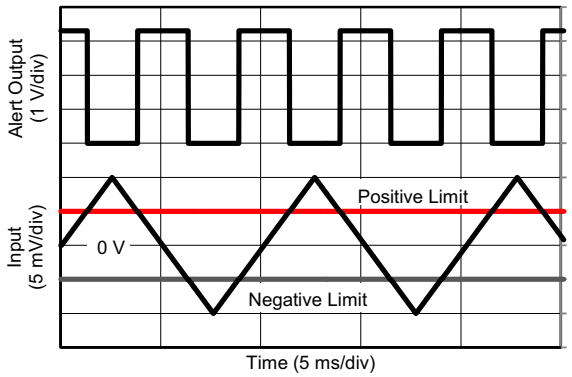


Figure 53. Bidirectional Application Curve

9 Power Supply Recommendations

The device input circuitry accurately measures signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply pin can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as 36 V. At power-up, for applications where the common-mode voltage (V_{CM}) slew rate is greater than 6 V/µs with a final common-mode voltage greater than 20 V, the V_S supply is recommended to be present before V_{CM}. If the use case requires V_{CM} to be present before V_S with V_{CM} under these same slewing conditions, then a 331-Ω resistor must be added between the V_S supply and the VS pin bypass capacitor.

Power-supply bypass capacitors are required for stability, and must be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

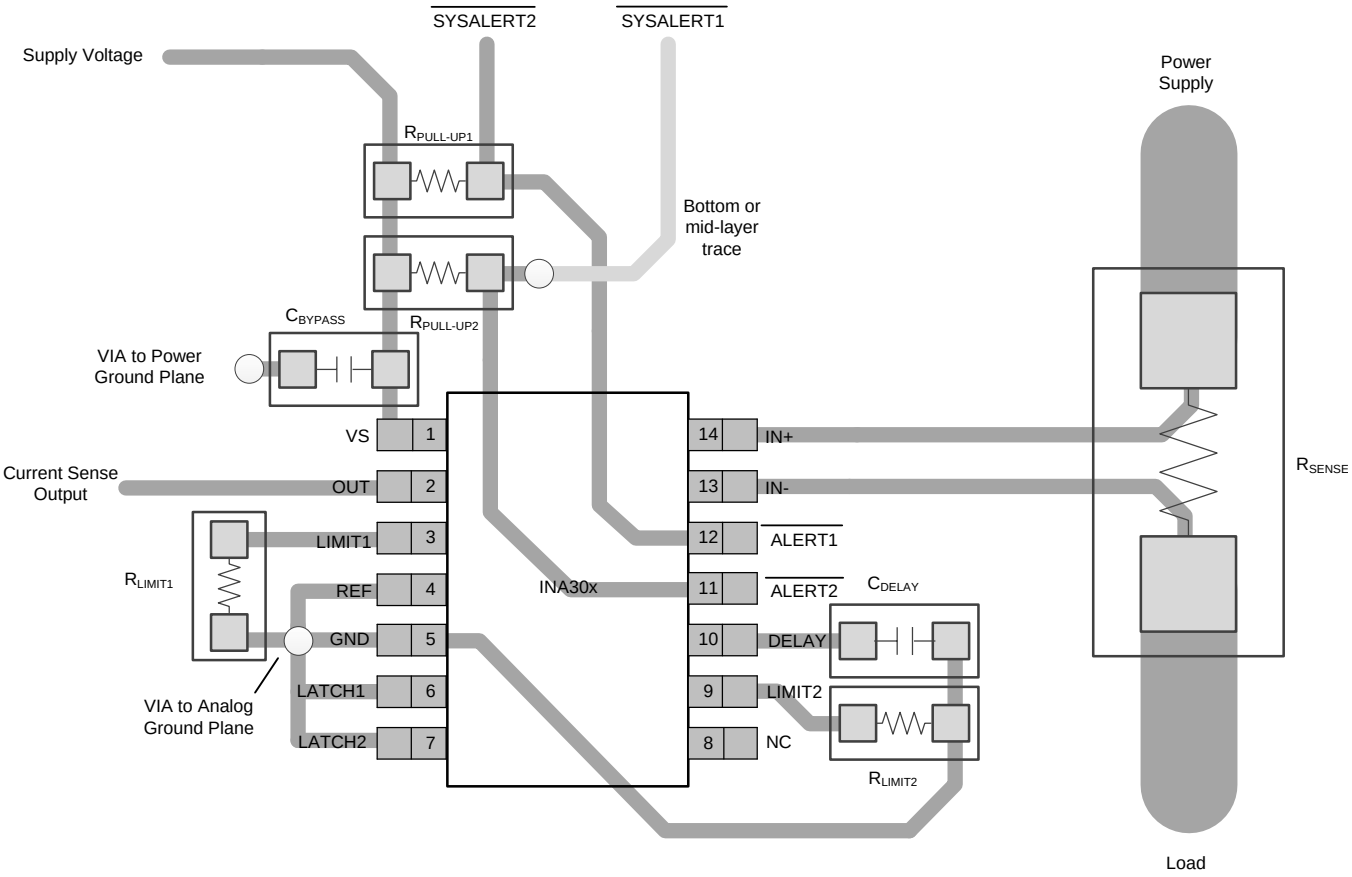
During slow power-up events, current flow through the sense resistor or voltage applied to the REF pin can result in the output voltage momentarily exceeding the voltage at the LIMITx pins, resulting in an erroneous indication of an out-of-range event on the ALERTx output. When powering the device with a slow ramping power rail where an input signal is already present, all alert indications should be disregarded until the supply voltage has reached the final value.

10 Layout

10.1 Layout Guidelines

- Apply connections to the current-sense resistor, R_{SENSE}, on the inside of the resistor pads to avoid additional voltage losses incurred by the high current traces to the resistor. Route the traces from the current-sense resistor symmetrically and side-by-side back to the input of the INA to minimize common-mode errors and noise pickup.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Make the connection of R_{LIMIT} to the ground pin as direct as possible to limit additional capacitance on this node. Routing this connection must be limited to the same plane if possible to avoid vias to internal planes. If the routing can not be made on the same plane and must pass through vias, make sure that a path is routed from R_{LIMIT} back to the ground pin, and that R_{LIMIT} is not simply connected directly to a ground plane.
- Routing to the delay capacitor must be short and direct. Keep the routing trace from the DELAY pin to the delay capacitor away from the ALERT2 trace (or any other noisy signals) to minimize any coupling effects. If no delay capacitor is used do not have any connection to the DELAY pin. Long trace lengths on the DELAY pin can cause noise to couple to the device, resulting in false trips.
- Pull up the open-drain output pins to the supply voltage rail; a 10-kΩ pullup resistor is recommended.

10.2 Layout Example



NOTE: Connect the limit resistors and delay capacitors directly to the GND pin; leave the DELAY pin unconnected or connected to VS through a pullup resistor if no delay is needed.

Figure 54. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLVx313-Q1 Low Power Rail-to-Rail In/Out 750-µV Typical Offset Op Amps* data sheet
- Texas Instruments, *Monitoring Current for Multiple Out-of-Range Conditions* application report

11.2 Related Links

Table 6 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 6. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA302	Click here	Click here	Click here	Click here	Click here
INA303	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA302A1IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1	Samples
INA302A1IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A1	Samples
INA302A2IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2	Samples
INA302A2IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A2	Samples
INA302A3IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3	Samples
INA302A3IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I302A3	Samples
INA303A1IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1	Samples
INA303A1IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A1	Samples
INA303A2IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2	Samples
INA303A2IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A2	Samples
INA303A3IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3	Samples
INA303A3IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I303A3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA302, INA303 :

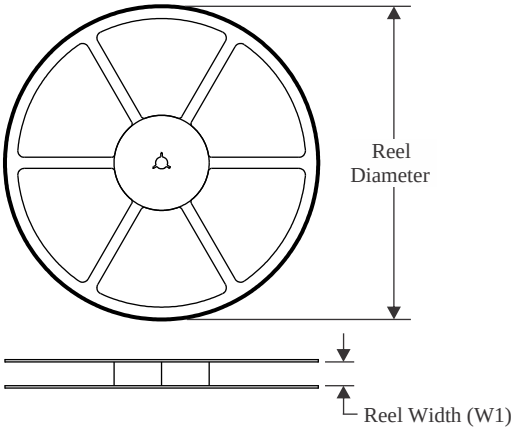
- Automotive: INA302-Q1, INA303-Q1

NOTE: Qualified Version Definitions:

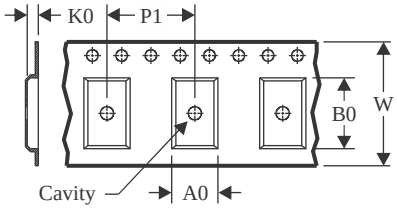
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

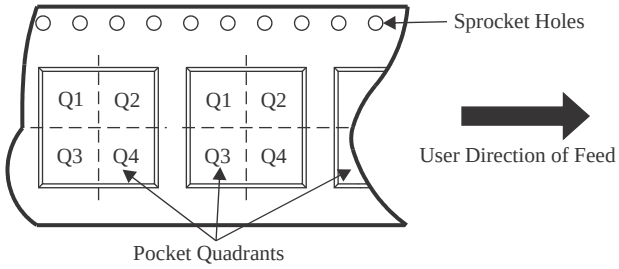


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

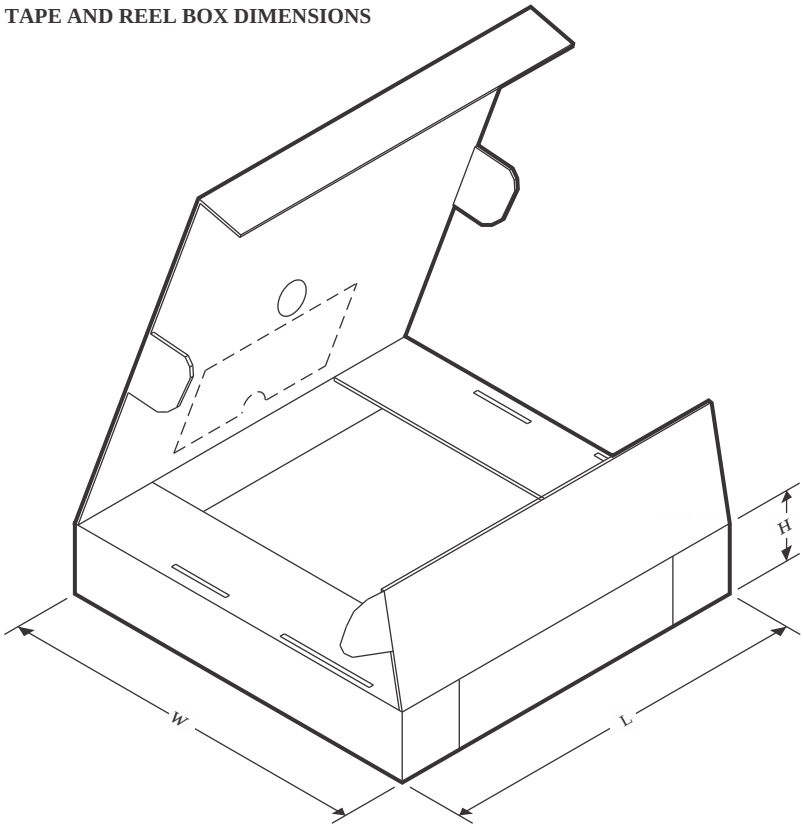
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA302A1IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA302A2IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA302A3IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A1IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A2IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA303A3IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

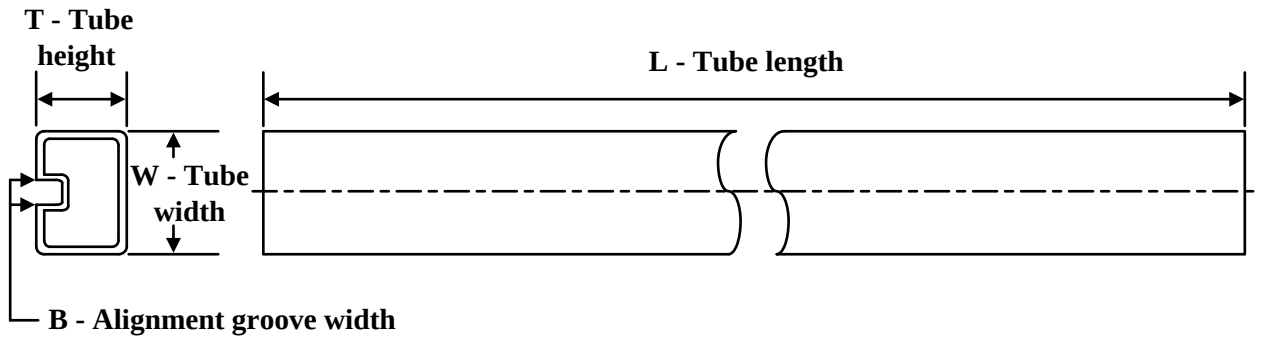
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA302A1IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
INA302A2IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
INA302A3IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
INA303A1IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
INA303A2IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
INA303A3IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

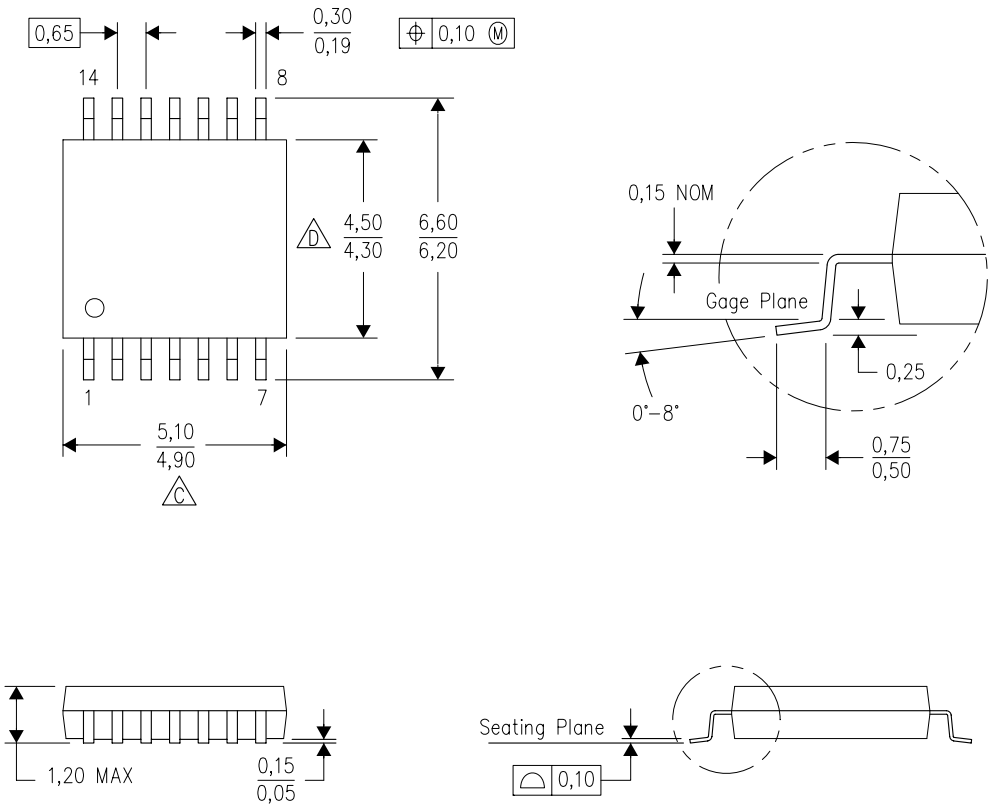
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA302A1IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA302A2IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA302A3IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA303A1IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA303A2IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
INA303A3IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

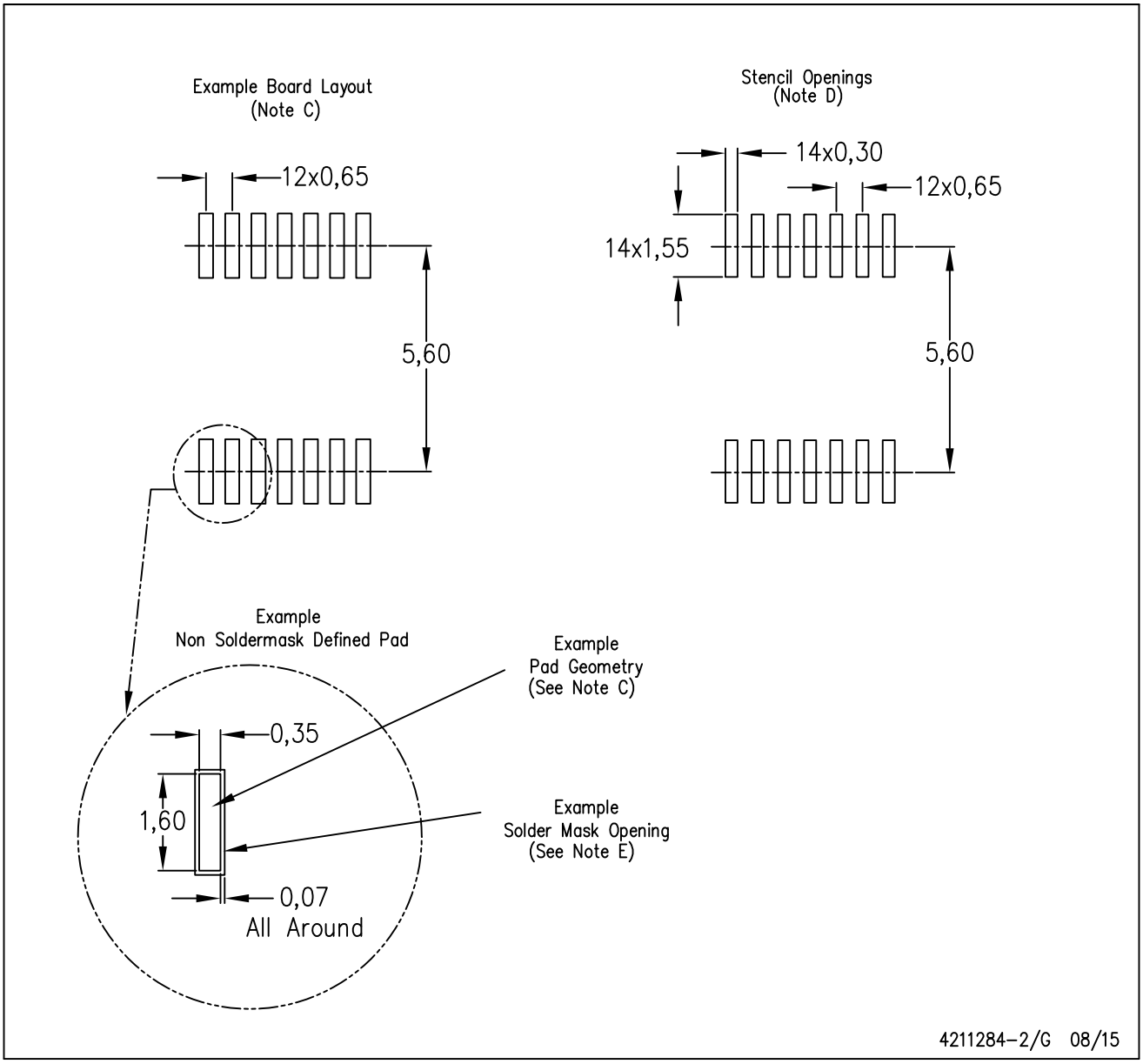
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

INAx181 Bidirectional, Low- and High-Side Voltage Output, Current-Sense Amplifiers

1 Features

- Common-mode range (V_{CM}): –0.2 V to +26 V
- High bandwidth: 350 kHz (A1 devices)
- Offset voltage:
  - ±150 µV (maximum) at V_{CM} = 0 V
  - ±500 µV (maximum) at V_{CM} = 12 V
- Output slew rate: 2 V/µs
- Bidirectional current-sensing capability
- Accuracy:
  - ±1% gain error (maximum)
  - 1-µV/°C offset drift (maximum)
- Gain options:
  - 20 V/V (A1 devices)
  - 50 V/V (A2 devices)
  - 100 V/V (A3 devices)
  - 200 V/V (A4 devices)
- Quiescent current: 260 µA maximum (INA181)

2 Applications

- Motor control
- Battery monitoring
- Power management
- Lighting control
- Overcurrent detection
- Solar inverters

3 Description

The INA181, INA2181, and INA4181 (INAx181) current sense amplifiers are designed for cost-optimized applications. These devices are part of a family of bidirectional, current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2 V to +26 V, independent of the supply voltage. The INAx181 family integrates a matched resistor gain network in four, fixed-gain device options: 20 V/V, 50 V/V, 100 V/V, or 200 V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

These devices operate from a single 2.7-V to 5.5-V power supply. The single-channel INA181 draws a maximum supply current of 260 µA; whereas, the dual-channel INA2181 draws a maximum supply current of 500 µA, and the quad-channel INA4181 draws a maximum supply current of 900 µA.

The INA181 is available in a 6-pin, SOT-23 package. The INA2181 is available in 10-pin, VSSOP and WSON packages. The INA4181 is available in a 20-pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA181	SOT-23 (6)	2.90 mm × 1.60 mm
INA2181	VSSOP (10)	3.00 mm × 3.00 mm
	WSON (10)	2.00 mm × 2.00 mm
INA4181	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Circuit

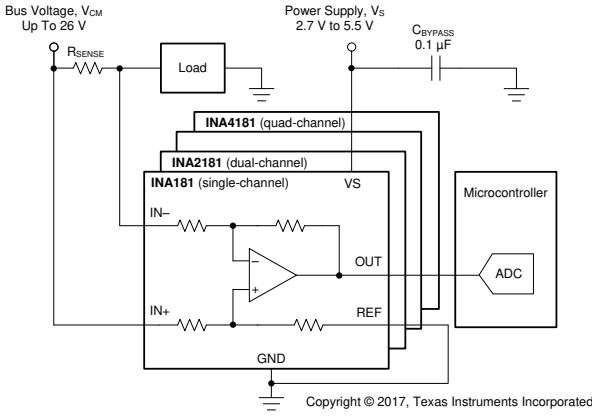


Table of Contents

4 Revision History

Changes from Revision F (March 2019) to Revision G — **Page**

- Added INA2181 10-pin WSON package to the data sheet ... 1

Changes from Revision E (July 2018) to Revision F — **Page**

- Added new paragraph regarding phase reversal to end of *Input Differential Overload* section ... 21
- Changed Figure 57 to fix pin number typos ... 33
- Changed Figure 58 to fix pin number typos ... 34

Changes from Revision D (March 2018) to Revision E — **Page**

- Changed instances of INAx180 to INAx181 (typos) ... 1

Changes from Revision C (December 2017) to Revision D — **Page**

- Changed INA4181 device from preview to production data (active) ... 1
- Added new Figure 25 for INA4181 ... 12
- Added new Figure 28 for INA4181 ... 12
- Added "other" to first sentence after Figure 49 to clarify channel connection in *Summing Multiple Currents* section ... 27

Changes from Revision B (November 2017) to Revision C — **Page**

- Changed INA2181 device from preview to production data (active) ... 1
- Added "Both Inputs" to Figure 21 title ... 11
- Added new Figure 24 for INA2181 ... 11
- Added new Figure 25 placeholder for INA4181 ... 12
- Added new Figure 27 for INA2181 ... 12

Changes from Revision A (August 2017) to Revision B **Page**

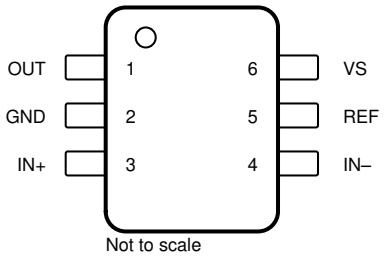
Changes from Original (April 2017) to Revision A **Page**

5 Device Comparison Table

PRODUCT	NUMBER OF CHANNELS	GAIN (V/V)
INA181A1	1	20
INA181A2	1	50
INA181A3	1	100
INA181A4	1	200
INA2181A1	2	20
INA2181A2	2	50
INA2181A3	2	100
INA2181A4	2	200
INA4181A1	4	20
INA4181A2	4	50
INA4181A3	4	100
INA4181A4	4	200

6 Pin Configuration and Functions

INA181: DBV Package
6-Pin SOT-23
Top View

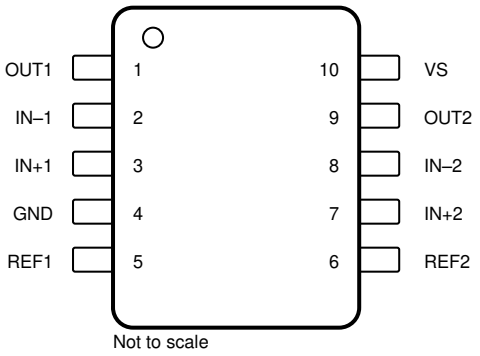


Not to scale

Pin Functions: INA181 (Single Channel)

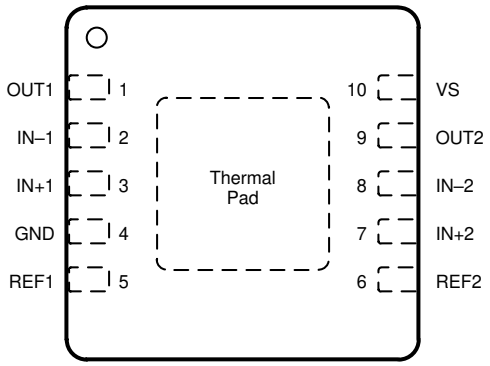
PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Analog	Ground
IN–	4	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	3	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
OUT	1	Analog output	Output voltage
REF	5	Analog input	Reference input
VS	6	Analog	Power supply, 2.7 V to 5.5 V

INA2181-Q1: DGS Package
10-Pin VSSOP
Top View



Not to scale

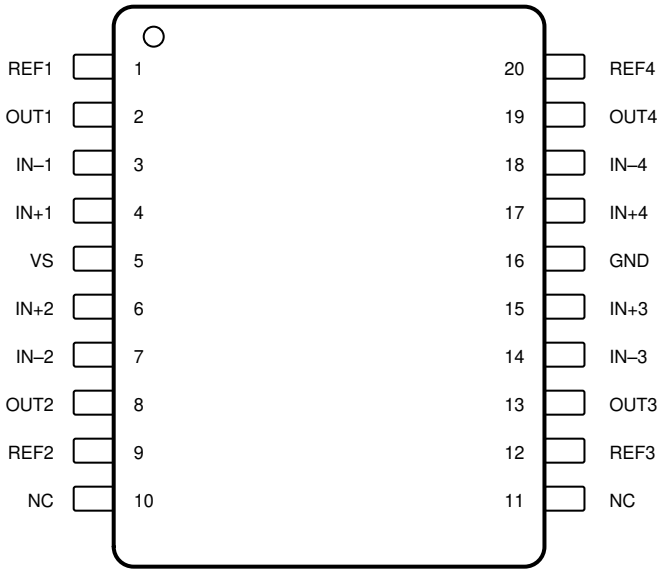
INA2181: DSQ Package
10-Pin WSON
Top View



Not to scale

(1) Thermal Pad can be left floating or connected to GND.

INA4181: PW Package
20-Pin TSSOP
Top View



Not to scale

Pin Functions: INA2181 (Dual Channel) and INA4181 (Quad Channel)

PIN			TYPE	DESCRIPTION
NAME	INA2181	INA4181		
GND	4	16	Analog	Ground
IN–1	2	3	Analog input	Current-sense amplifier negative input for channel 1. For high-side applications, connect to load side of channel-1 sense resistor. For low-side applications, connect to ground side of channel-1 sense resistor.
IN+1	3	4	Analog input	Current-sense amplifier positive input for channel 1. For high-side applications, connect to bus-voltage side of channel-1 sense resistor. For low-side applications, connect to load side of channel-1 sense resistor.
IN–2	8	7	Analog input	Current-sense amplifier negative input for channel 2. For high-side applications, connect to load side of channel-2 sense resistor. For low-side applications, connect to ground side of channel-2 sense resistor.

Pin Functions: INA2181 (Dual Channel) and INA4181 (Quad Channel) (continued)

PIN			TYPE	DESCRIPTION
NAME	INA2181	INA4181		
IN+2	7	6	Analog input	Current-sense amplifier positive input for channel 2. For high-side applications, connect to bus-voltage side of channel-2 sense resistor. For low-side applications, connect to load side of channel-2 sense resistor.
IN–3	—	14	Analog input	Current-sense amplifier negative input for channel 3. For high-side applications, connect to load side of channel-3 sense resistor. For low-side applications, connect to ground side of channel-3 sense resistor.
IN+3	—	15	Analog input	Current-sense amplifier positive input for channel 3. For high-side applications, connect to bus-voltage side of channel-3 sense resistor. For low-side applications, connect to load side of channel-3 sense resistor.
IN–4	—	18	Analog input	Current-sense amplifier negative input for channel 4. For high-side applications, connect to load side of channel-4 sense resistor. For low-side applications, connect to ground side of channel-4 sense resistor.
IN+4	—	17	Analog input	Current-sense amplifier positive input for channel 4. For high-side applications, connect to bus-voltage side of channel-4 sense resistor. For low-side applications, connect to load side of channel-4 sense resistor.
NC	—	10, 11	—	NC denotes no internal connection. These pins can be left floating or connected to any voltage between V_S and ground.
OUT1	1	2	Analog output	Channel 1 output voltage
OUT2	9	8	Analog output	Channel 2 output voltage
OUT3	—	13	Analog output	Channel 3 output voltage
OUT4	—	19	Analog output	Channel 4 output voltage
REF1	5	1	Analog input	Channel 1 reference voltage, 0 to V_S
REF2	6	9	Analog input	Channel 2 reference voltage, 0 to V_S
REF3	—	12	Analog input	Channel 3 reference voltage, 0 to V_S
REF4	—	20	Analog input	Channel 4 reference voltage, 0 to V_S
VS	10	5	Analog	Power supply pin, 2.7 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs, IN+, IN– (2)	Differential (V_{IN+}) – ($V_{IN–}$)	–26	26	V
	Common-mode (3)	GND – 0.3	26	
Input voltage range	at REF pin	GND – 0.3	V_S + 0.3	V
Output Voltage		GND – 0.3	V_S + 0.3	V
Maximum output current, I_{OUT}			8	mA
Operating fee-air temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage (IN+ and IN–)	–0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		INA181	INA2181		INA4181	UNIT
		DBV (SOT-23)	DSQ (WSON)	DGS (VSSOP)	PW (TSSOP)	
		6 PINS	10 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	198.7	74.5	177.3	97.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.9	89.7	68.7	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	39.8	98.4	48.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.3	3.7	12.6	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.0	39.7	96.9	47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	16.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, V_{IN+} = 12 V, and V_{SENSE} = V_{IN+} – $V_{IN–}$ (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
CMRR	Common-mode rejection ratio, RTI (1)		V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C	84	100		dB
V_{OS}	Offset voltage, RTI		V_{SENSE} = 0 mV, V_{IN+} = 0 V		±25	±150	µV
			V_{SENSE} = 0 mV		±100	±500	µV
dV_{OS}/dT	Offset drift, RTI		V_{SENSE} = 0 mV, T_A = –40°C to +125°C		0.2	1	µV/°C
PSRR	RTI vs power supply ratio		V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, V_{SENSE} = 0 mV		±8	±40	µV/V
I_{IB}	Input bias current		V_{SENSE} = 0 mV, V_{IN+} = 0 V		-6		µA
			V_{SENSE} = 0 mV		75		µA
I_{IO}	Input offset current		V_{SENSE} = 0 mV		±0.05		µA
OUTPUT							
G	Gain		A1 devices		20		V/V
			A2 devices		50		V/V
			A3 devices		100		V/V
			A4 devices		200		V/V
E_G	Gain error		V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C		±0.1%	±1%	
	Gain error vs temperature		T_A = –40°C to +125°C		1.5	20	ppm/°C
	Nonlinearity error		V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF
VOLTAGE OUTPUT (2)							
V_{SP}	Swing to V_S power-supply rail (3)		R_L = 10 kΩ to GND, T_A = –40°C to +125°C		(V_S) – 0.02	(V_S) – 0.03	V
V_{SN}	Swing to GND (3)		R_L = 10 kΩ to GND, T_A = –40°C to +125°C		(V_{GND}) + 0.0005	(V_{GND}) + 0.005	V
FREQUENCY RESPONSE							
BW	Bandwidth		A1 devices, C_{LOAD} = 10 pF		350		kHz
			A2 devices, C_{LOAD} = 10 pF		210		kHz
			A3 devices, C_{LOAD} = 10 pF		150		kHz
			A4 devices, C_{LOAD} = 10 pF		105		kHz
SR	Slew rate				2		V/µs
NOISE, RTI (1)							
	Voltage noise density				40		nV/√Hz
POWER SUPPLY							
I_Q	Quiescent current	INA181	V_{SENSE} = 0 mV		195	260	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			300	
		INA2181	V_{SENSE} = 0 mV		356	500	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			520	
		INA4181	V_{SENSE} = 0 mV		690	900	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			1000	

(1) RTI = referred-to-input.
(2) See Figure 19.
(3) Swing specifications are tested with an overdriven input condition.

7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

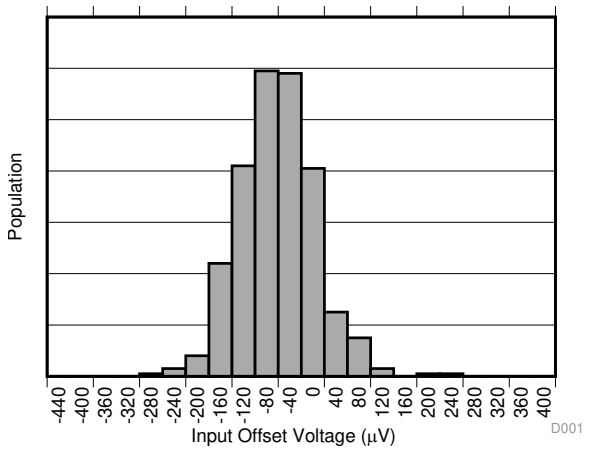


Figure 1. Input Offset Voltage Production Distribution A1

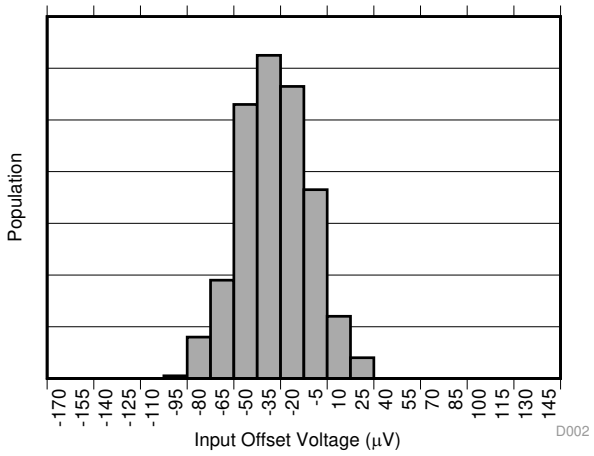


Figure 2. Input Offset Voltage Production Distribution A2

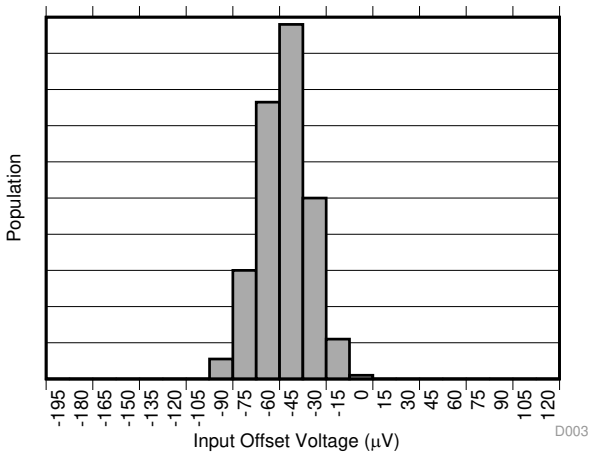


Figure 3. Input Offset Voltage Production Distribution A3

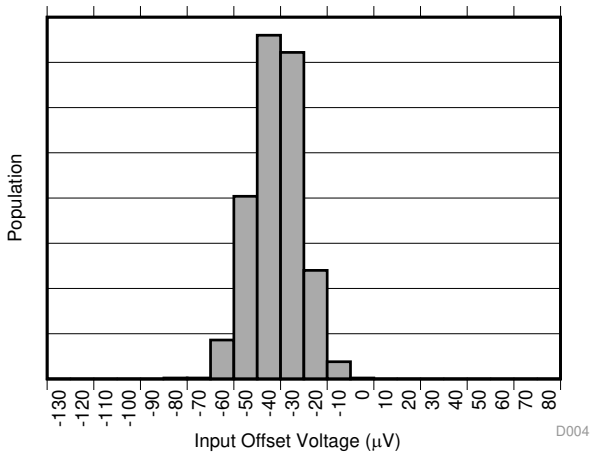


Figure 4. Input Offset Voltage Production Distribution A4

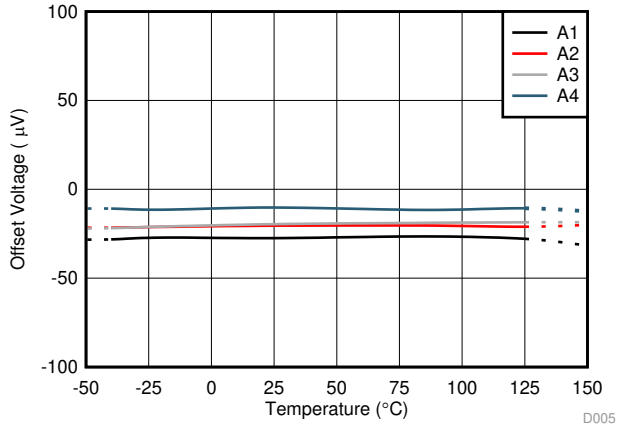


Figure 5. Offset Voltage vs Temperature

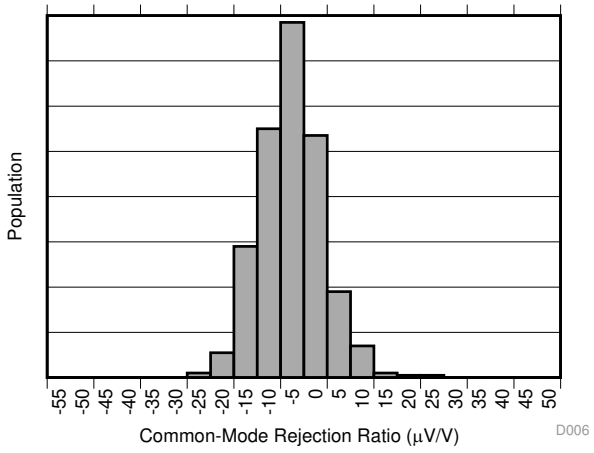


Figure 6. Common-Mode Rejection Production Distribution A1

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

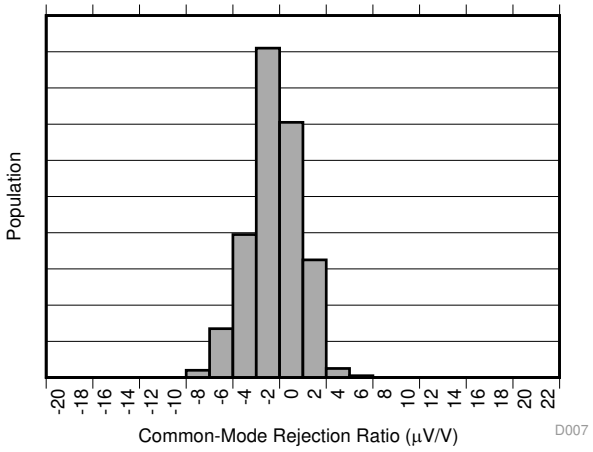


Figure 7. Common-Mode Rejection Production Distribution A2

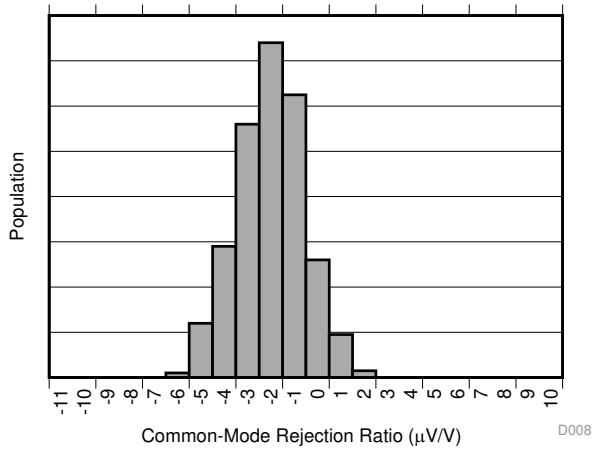


Figure 8. Common-Mode Rejection Production Distribution A3

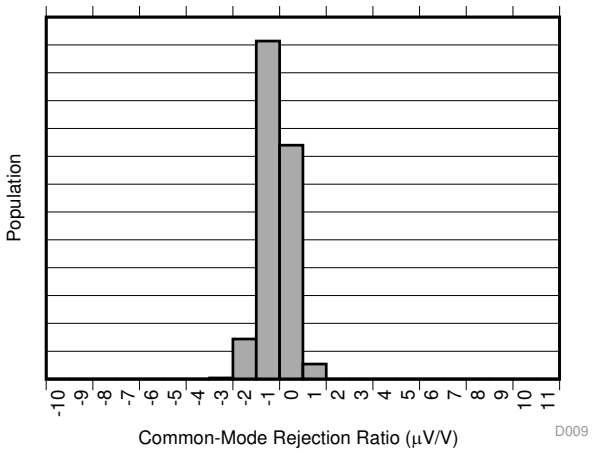


Figure 9. Common-Mode Rejection Production Distribution A4

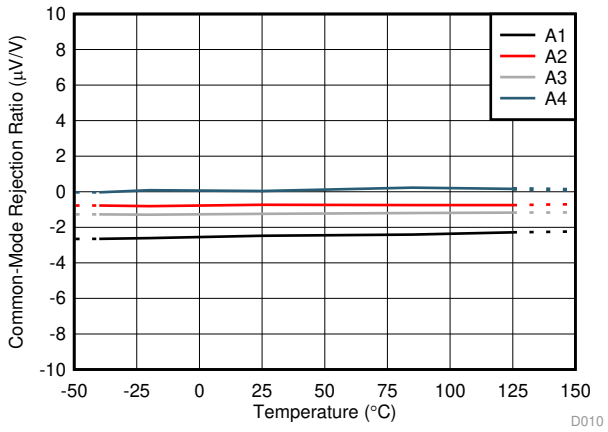


Figure 10. Common-Mode Rejection Ratio vs Temperature

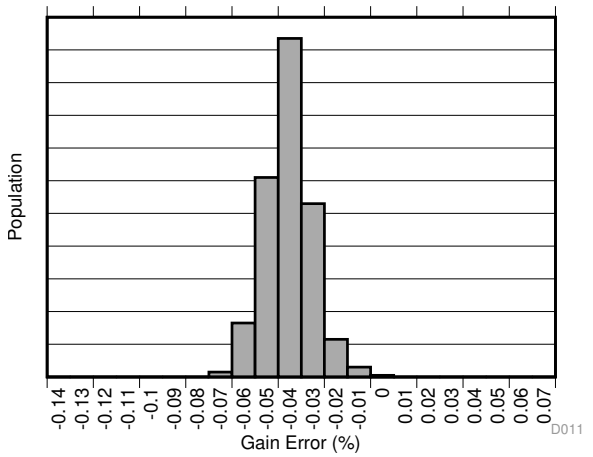


Figure 11. Gain Error Production Distribution A1

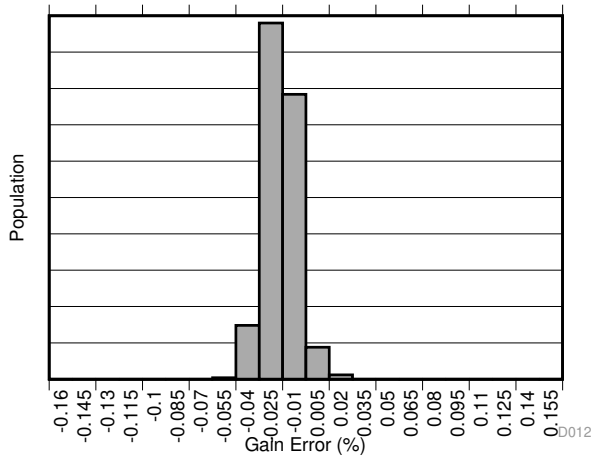


Figure 12. Gain Error Production Distribution A2

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

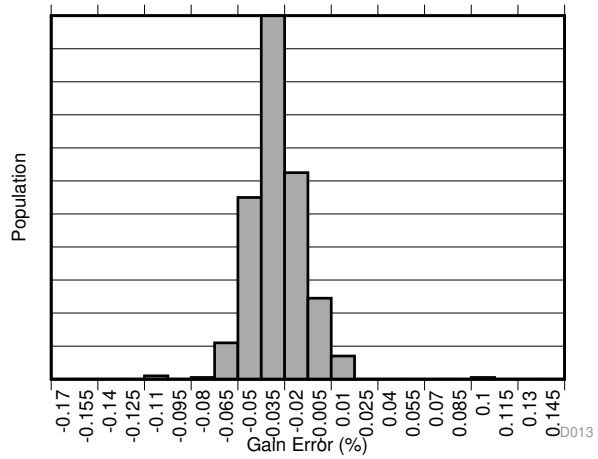


Figure 13. Gain Error Production Distribution A3

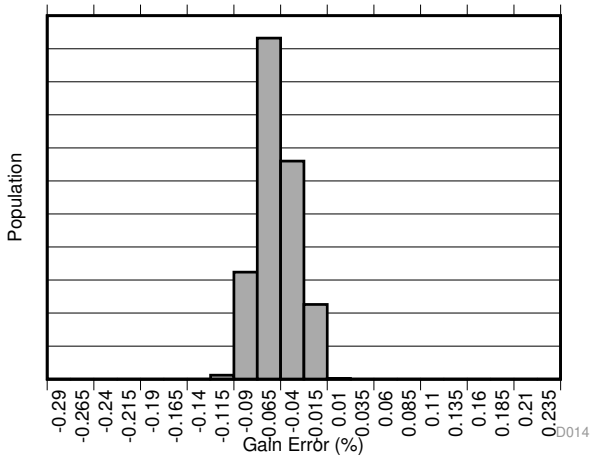


Figure 14. Gain Error Production Distribution A4

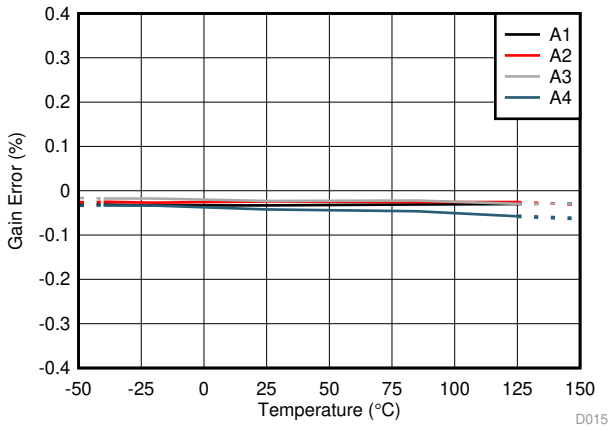


Figure 15. Gain Error vs Temperature

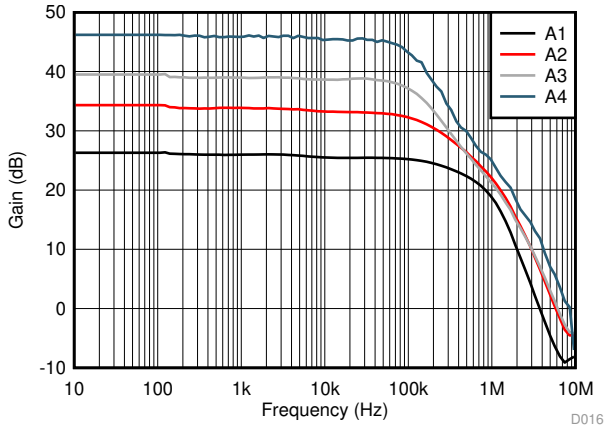


Figure 16. Gain vs Frequency

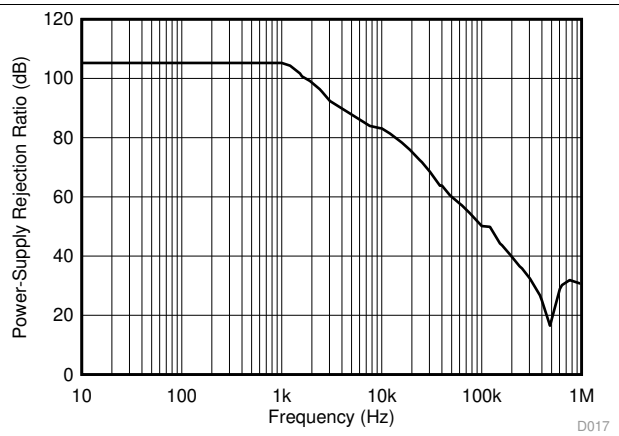


Figure 17. Power-Supply Rejection Ratio vs Frequency

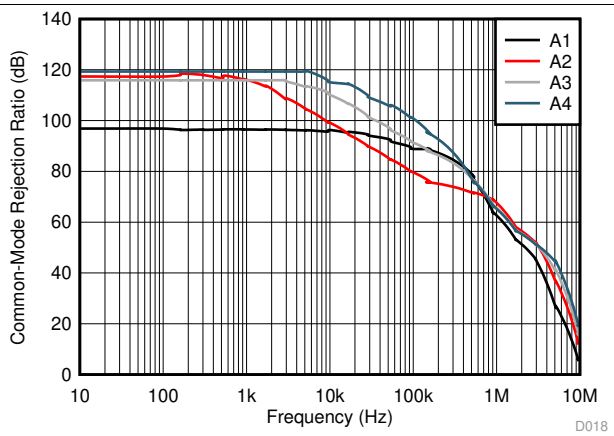


Figure 18. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

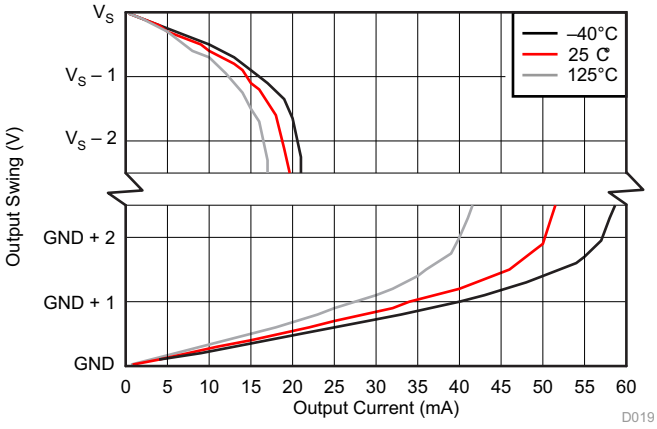


Figure 19. Output Voltage Swing vs Output Current

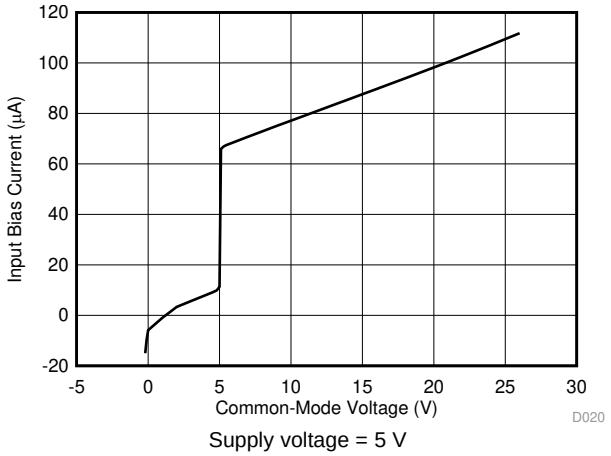


Figure 20. Input Bias Current vs Common-Mode Voltage

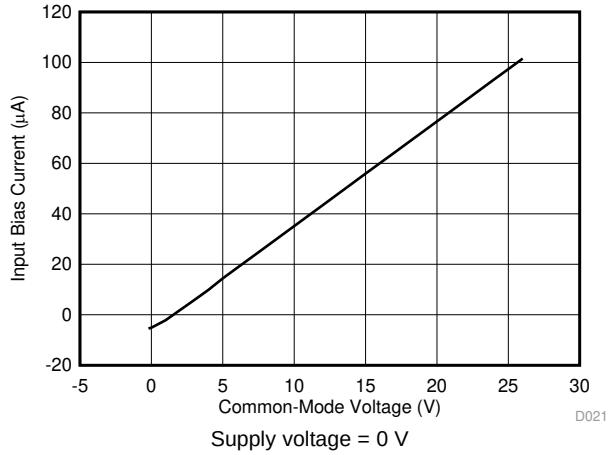


Figure 21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

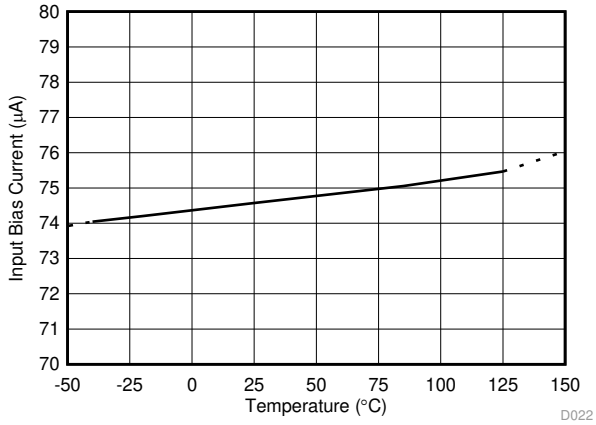


Figure 22. Input Bias Current vs Temperature

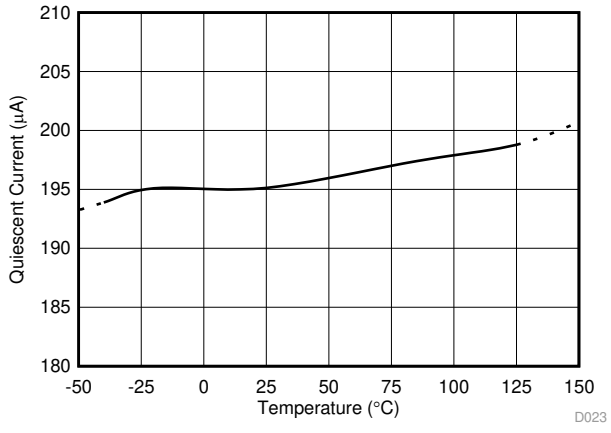


Figure 23. Quiescent Current vs Temperature (INA181)

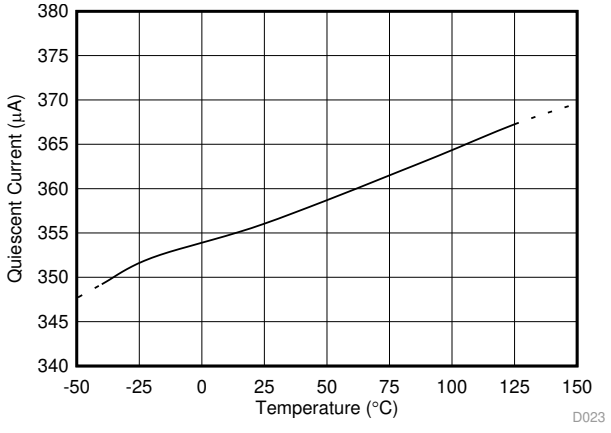


Figure 24. Quiescent Current vs Temperature (INA2181)

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

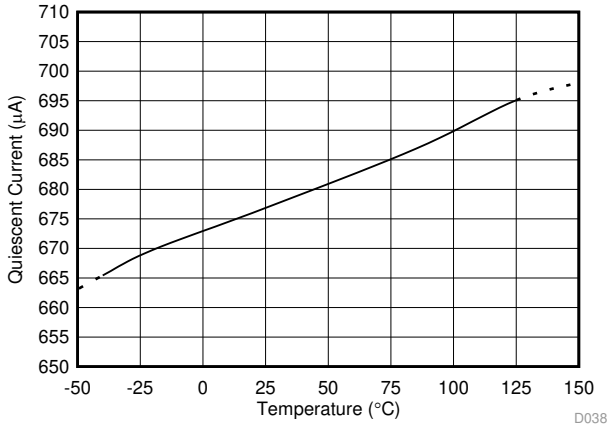


Figure 25. Quiescent Current vs Temperature (INA4181)

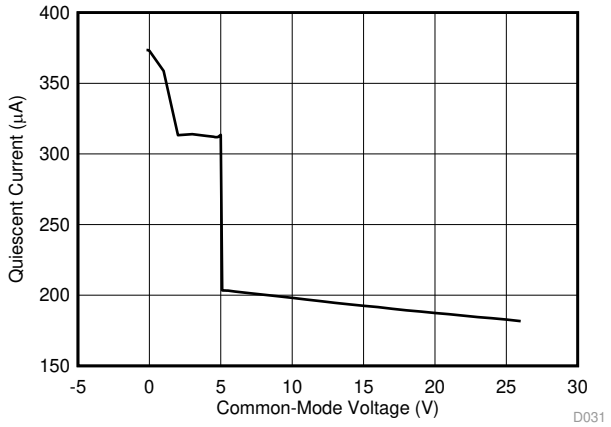


Figure 26. I_Q vs Common-Mode Voltage (INA181)

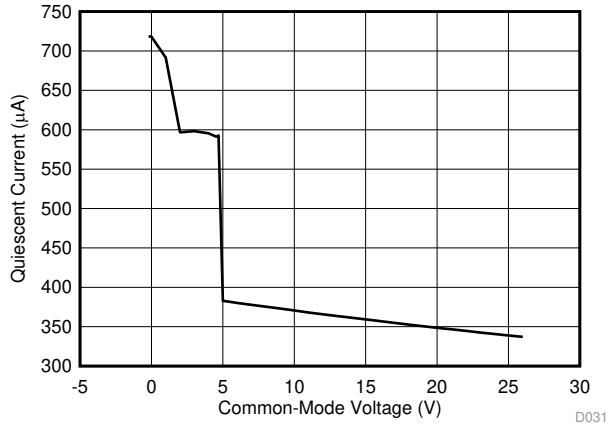


Figure 27. I_Q vs Common-Mode Voltage (INA2181)

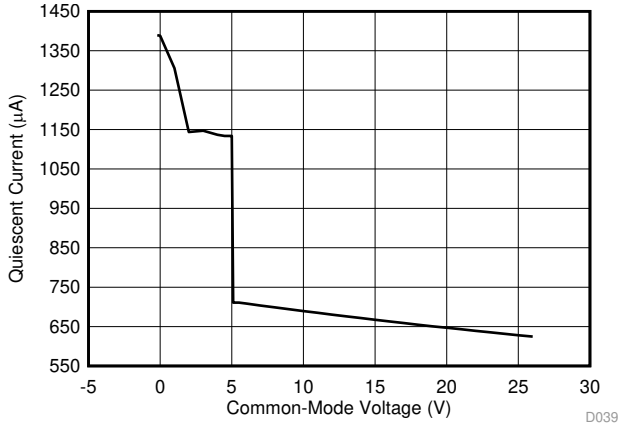


Figure 28. I_Q vs Common-Mode Voltage (INA4181)

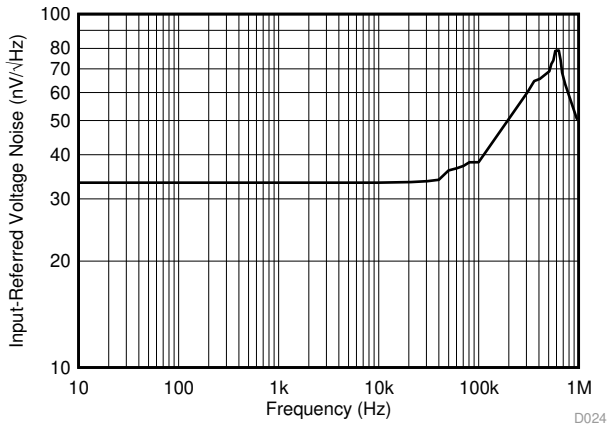


Figure 29. Input-Referred Voltage Noise vs Frequency (A3 Devices)

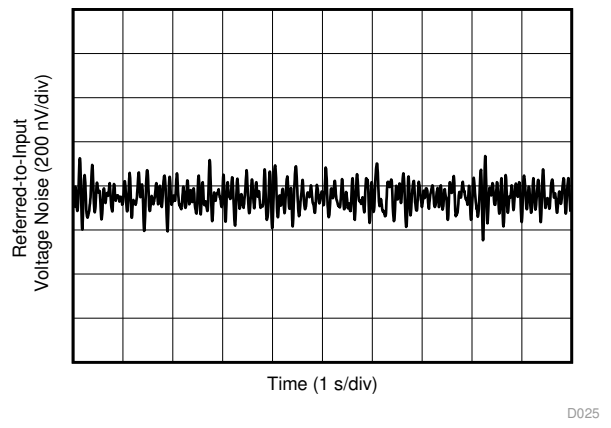
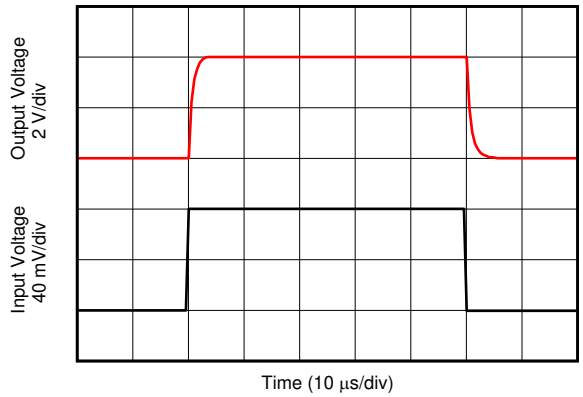


Figure 30. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)



80-mV_{PP} input step

Figure 31. Step Response

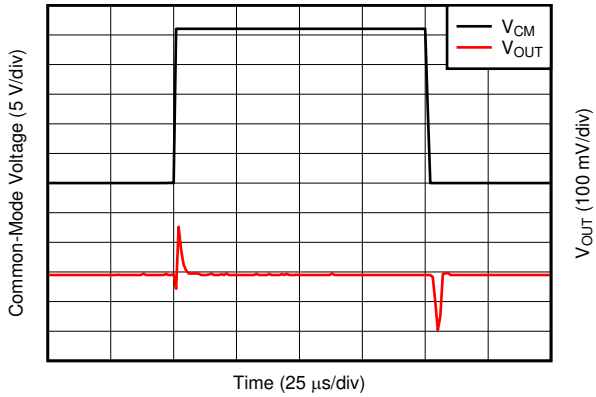


Figure 32. Common-Mode Voltage Transient Response

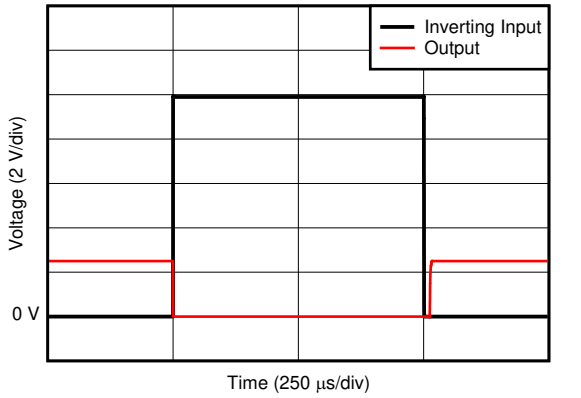


Figure 33. Inverting Differential Input Overload

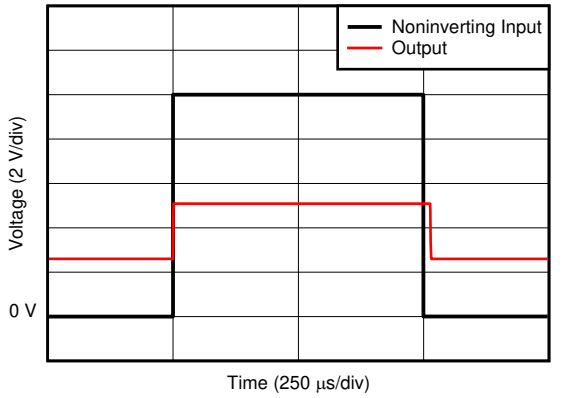


Figure 34. Noninverting Differential Input Overload

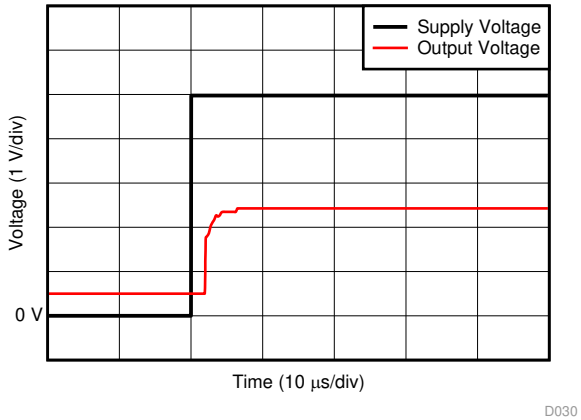


Figure 35. Start-Up Response

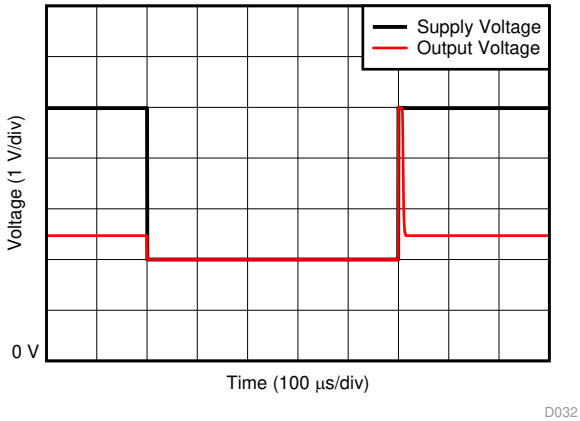


Figure 36. Brownout Recovery

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

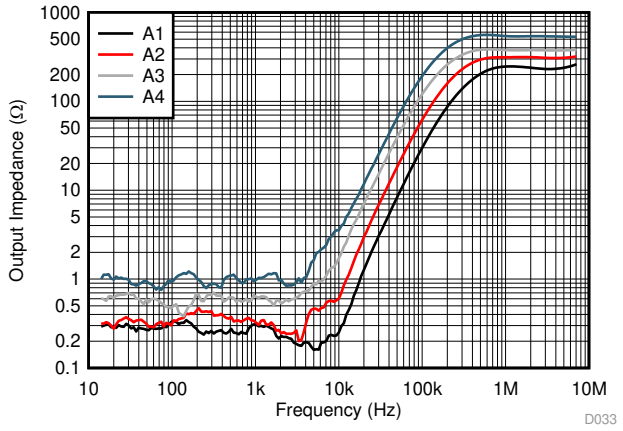


Figure 37. Output Impedance vs Frequency

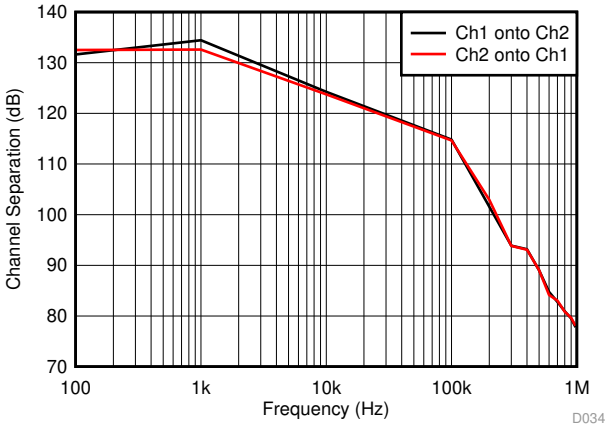


Figure 38. Channel Separation vs Frequency (INA2181)

8 Detailed Description

8.1 Overview

The INA181, INA2181, and INA4181 (INAx181) are 26-V common-mode, current-sensing amplifiers used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the devices can be powered from supply voltages as low as 2.7 V.

8.2 Functional Block Diagrams

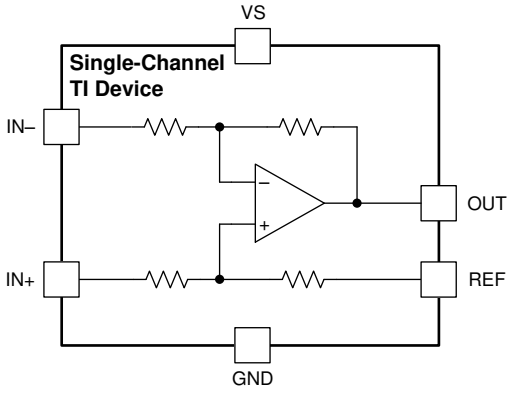


Figure 39. INA181 Functional Block Diagram

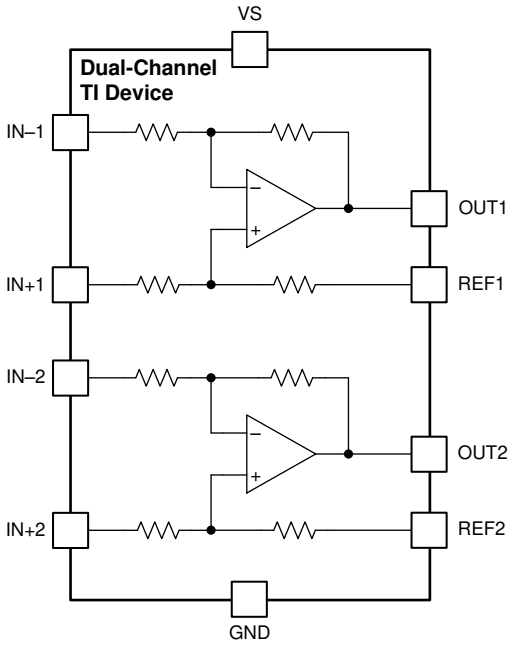


Figure 40. INA2181 Functional Block Diagram

Functional Block Diagrams (continued)

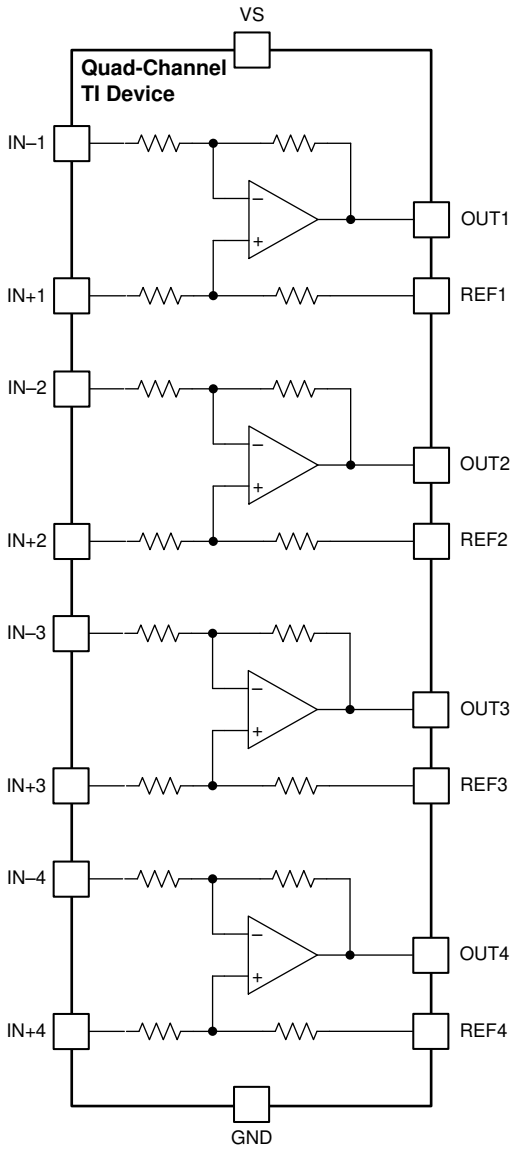


Figure 41. INA4181 Functional Block Diagram

8.3 Feature Description

8.3.1 High Bandwidth and Slew Rate

The INAx181 support small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, make the INAx181 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection, where the INAx181 are used with an external comparator and a reference to quickly detect when the sensed current is out of range.

8.3.2 Bidirectional Current Monitoring

The INA181 senses current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The output voltage of the current-sense amplifier is shown in Equation 1.

$$V_{OUT} = \left(I_{LOAD} \times R_{SENSE} \times GAIN\right) + V_{REF} \quad (1)$$

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the selected device.
- V_{REF} is the voltage applied to the REF pin.

8.3.3 Wide Input Common-Mode Voltage Range

The INAx181 support input common-mode voltages from –0.2 V to +26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. The ability to operate with common-mode voltages greater or less than V_S allow the INAx181 to be used in high-side, as well as low-side, current-sensing applications, as shown in Figure 42.

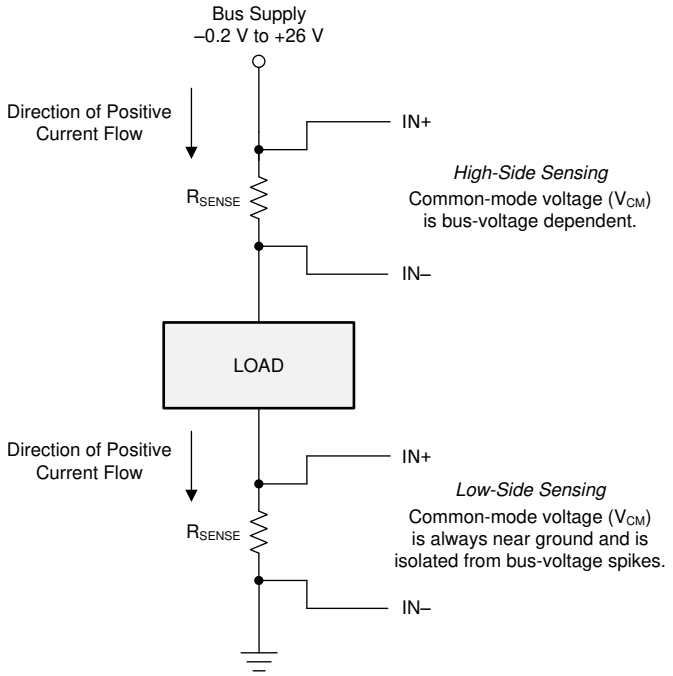


Figure 42. High-Side and Low-Side Sensing Connections

Feature Description (continued)

8.3.4 Precise Low-Side Current Sensing

When used in low-side current sensing applications the offset voltage of the INAx181 is within ±150 µV. The low offset performance of the INAx181 has several benefits. First, the low offset allows these devices to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the INAx181 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.

8.3.5 Rail-to-Rail Output Swing

The INAx181 allow linear current sensing operation with the output close to the supply rail and GND. The maximum specified output swing to the positive rail is 30 mV, and the maximum specified output swing to GND is only 5 mV. In order to compare the output swing of the INAx181 to an equivalent operational amplifier (op amp), the inputs are overdriven to approximate the open-loop condition specified in op amp data sheets. The current-sense amplifier is a closed-loop system; therefore, the output swing to GND can be limited by the product of the offset voltage and amplifier gain during unidirectional operation (V_{REF} = 0 V).

For devices that have positive offset voltages, the swing to GND is limited by the larger of either the offset voltage multiplied by the gain or the swing to GND specified in the *Electrical Characteristics* table.

For example, in an application where the INA181A4 (gain = 200 V/V) is used for low-side current sensing and the device has an offset of 40 µV, the product of the device offset and gain results in a value of 8 mV, greater than the specified negative swing value. Therefore, the swing to GND for this example is 8 mV. If the same device has an offset of –40 µV, then the calculated zero differential signal is –8 mV. In this case, the offset helps overdrive the swing in the negative direction, and swing performance is consistent with the value specified in the *Electrical Characteristics* table.

The offset voltage is a function of the common-mode voltage as determined by the CMRR specification; therefore, the offset voltage increases when higher common-mode voltages are present. The increase in offset voltage limits how low the output voltage can go during a zero-current condition when operating at higher common-mode voltages with V_{REF} = 0 V . The typical limitation of the zero-current output voltage vs common-mode voltage for each gain option is shown in Figure 43.

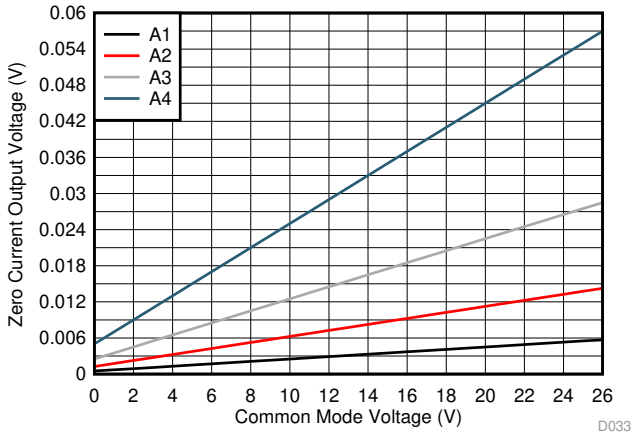


Figure 43. Zero-Current Output Voltage vs Common-Mode Voltage

8.4 Device Functional Modes

8.4.1 Normal Mode

The INAx181 are in normal operation when the following conditions are met:

- The power supply voltage (V_S) is between 2.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +26 V.
- The maximum differential input signal times gain plus V_{REF} is less than V_S minus the output voltage swing to V_S.
- The minimum differential input signal times gain plus V_{REF} is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, these devices produce an output voltage that is the *gained-up* representation of the difference voltage from IN+ to IN– plus the reference voltage at V_{REF}.

8.4.2 Unidirectional Mode

These devices can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 44. When the current flows from the bus supply to the load, the input signal across IN+ to IN– increases, and causes the output voltage at the OUT pin to increase.

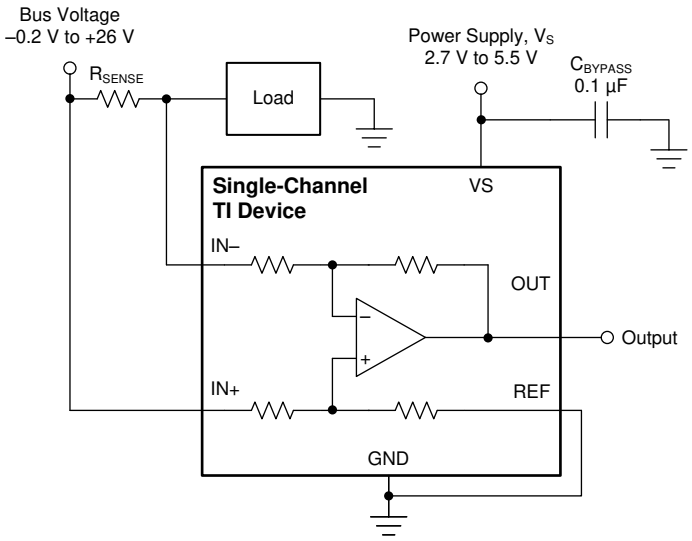


Figure 44. Unidirectional Application

The linear range of the output stage is limited by how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, buffer the reference voltage connected to the REF pin.

A less-frequently used output biasing method is to connect the REF pin to the power-supply voltage, V_S. This method results in the output voltage saturating at 200 mV less than the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed V_S.

Device Functional Modes (continued)

8.4.3 Bidirectional Mode

The INAx181 are bidirectional, current-sense amplifiers capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flowing through the resistor can change directions.

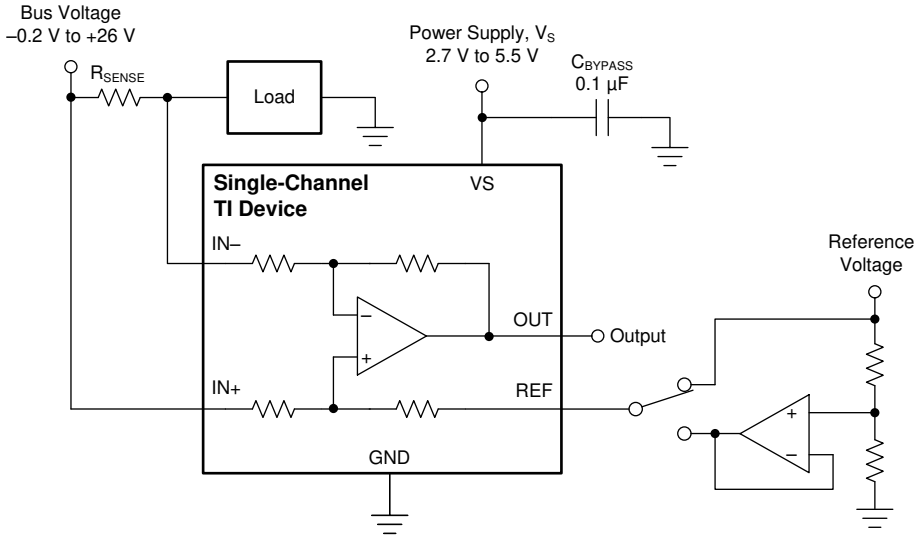


Figure 45. Bidirectional Application

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 45. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

8.4.4 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INAx181 drive the output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INAx181 returns to the expected value approximately 20 µs after the fault condition is removed.

When the INAx181 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not violated. Following these guidelines, the INAx181 output maintains polarity, and does not suffer from phase reversal.

Device Functional Modes (continued)

8.4.5 Shutdown Mode

Although the INAx181 do not have a shutdown pin, the low power consumption of these devices allows the output of a logic gate or transistor switch to power the INAx181. This gate or switch turns on and off the INAx181 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INAx181 in shutdown mode, as shown in Figure 46.

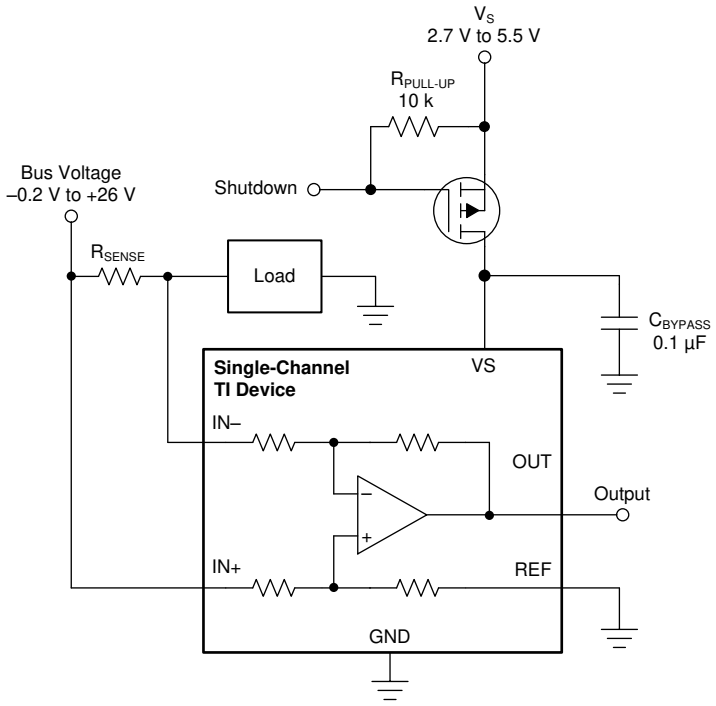


Figure 46. Basic Circuit to Shut Down the INA181 With a Grounded Reference

There is typically more than 500 kΩ of impedance (from the combination of 500-kΩ feedback and input gain set resistors) from each input of the INAx181 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the voltage at the connection. For example, if the REF pin is grounded, the calculation of the effect of the 500 kΩ impedance from the shunt to ground is straightforward. However, if the reference is powered while the INAx181 is in shutdown mode, instead of assuming 500 kΩ to ground, assume 500 kΩ to the reference voltage.

Regarding the 500-kΩ path to the output pin, the output stage of a disabled INAx181 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 500-kΩ resistor.

As a final note, as long as the shunt common-mode voltage is greater than V_S when the device is powered up, there is an additional and well-matched 55-µA typical current that flows in each of the inputs. If less than V_S, the common-mode input currents are negligible, and the only current effects are the result of the 500-kΩ resistors.

9 Application and Implementation

NOTE

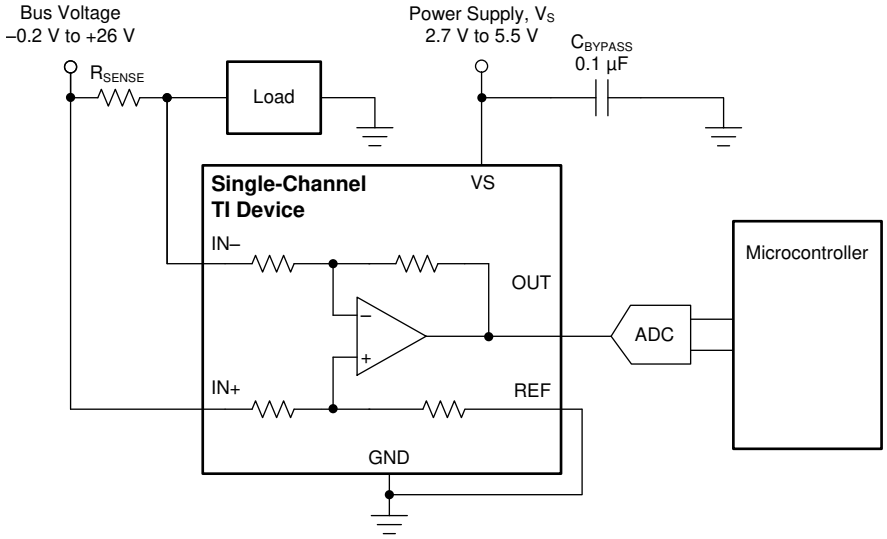
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INAx181 amplify the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed in previous sections.

9.1.1 Basic Connections

Figure 47 shows the basic connections of the INA181. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.



NOTE: To help eliminate ground offset errors between the device and the analog-to-digital converter (ADC), connect the REF pin to the ADC reference input and then to ground. For best performance, use an RC filter between the output of the INAx181 and the ADC. See *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* for more details.

Figure 47. Basic Connections for the INA181

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

Application Information (continued)

9.1.2 R_{SENSE} and Device Gain Selection

The accuracy of the INAx181 is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application. The INAx181 have typical input bias currents of 75 µA for each input when operated at a 12-V common-mode voltage input. When large current-sense resistors are used, these bias currents cause increased offset error and reduced common-mode rejection. Therefore, using current-sense resistors larger than a few ohms is generally not recommended for applications that require current-monitoring accuracy. A second common restriction on the value of the current-sense resistor is the maximum allowable power dissipation that is budgeted for the resistor. Equation 2 gives the maximum value for the current sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (2)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that will flow through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing to rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 3 provides the maximum values of R_{SENSE} and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} - V_{REF} \quad (3)$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense-amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.
- V_{REF} is the externally applied voltage on the REF pin.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small of a sense resistor can be used in a given application. Equation 4 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} - V_{REF} \quad (4)$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense amplifier.
- V_{SN} is the negative output swing of the device (see Rail-to-Rail Output Swing).
- V_{REF} is the externally applied voltage on the REF pin.

In addition to adjusting the offset and gain, the voltage applied to the REF pin can be slightly increased to avoid negative swing limitations.

Application Information (continued)

9.1.3 Signal Filtering

Provided that the INAx181 output is connected to a high impedance input, the best location to filter is at the device output using a simple RC network from OUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INAx181 power-supply voltage. If filtering at the output is not possible, or filtering of only the differential input signal is required, it is possible to apply a filter at the input pins of the device. Figure 48 provides an example of how a filter can be used on the input pins of the device.

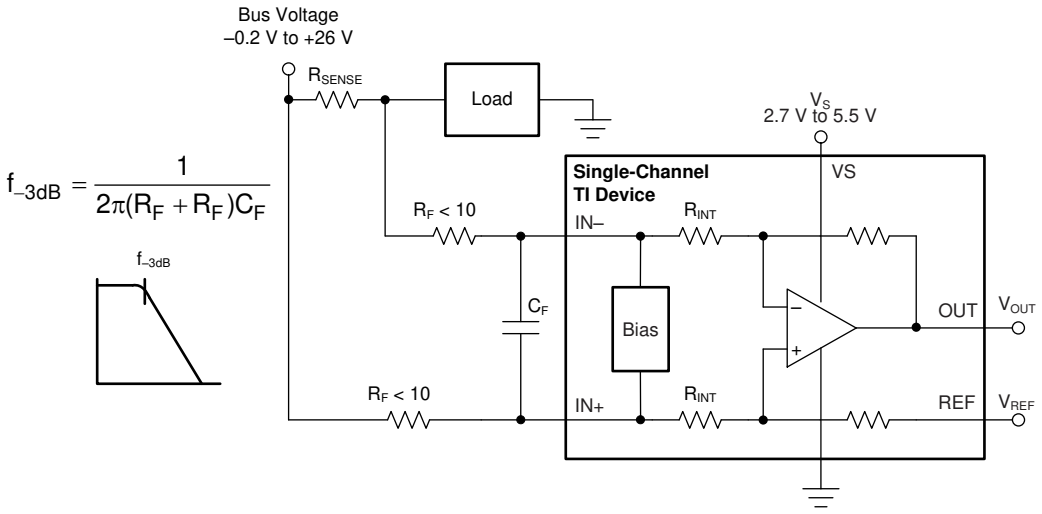


Figure 48. Filter at Input Pins

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in Figure 48 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using Equation 6, where the gain error factor is calculated using Equation 5.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}, as shown in Figure 48. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given using Equation 5:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \quad (5)$$

where:

- R_{INT} is the internal input resistor.
- R_F is the external series resistance.

Application Information (continued)

With the adjustment factor from Equation 5, including the device internal input resistance, this factor varies with each gain version, as shown in Table 1. Each individual device gain error factor is shown in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INAx181A1	20	25
INAx181A2	50	10
INAx181A3	100	5
INAx181A4	200	2.5

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INAx181A1	$\frac{25000}{(21 \times R_F) + 25000}$
INAx181A2	$\frac{10000}{(9 \times R_F) + 10000}$
INAx181A3	$\frac{1000}{R_F + 1000}$
INAx181A4	$\frac{2500}{(3 \times R_F) + 2500}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

For example, using an INA181A2 and the corresponding gain error equation from Table 2, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 6, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

9.1.4 Summing Multiple Currents

The outputs of the INA2181 are easily summed by connecting the output of one channel to the reference input of a second channel. The circuit configuration shown in Figure 49 is an easy way to achieve current summing. To correctly sum multiple output currents the values for the current sense resistor R_{SENSE} must be the same for all channels.

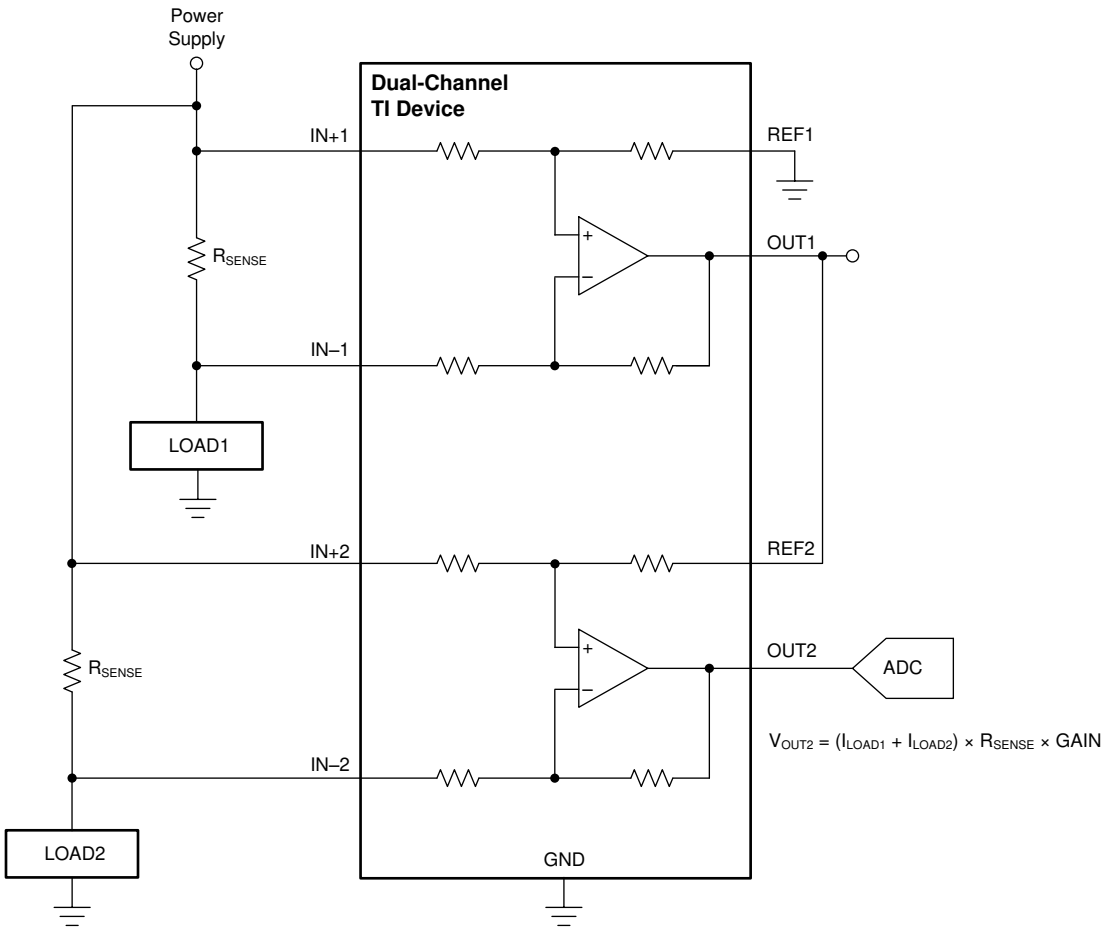
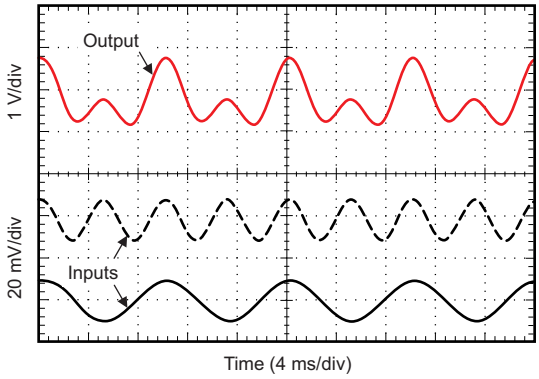


Figure 49. Summing Multiple Currents

Connect the output of one channel of the INA2181 to the reference input of the other channel. Use the reference input of the first circuit to set the reference of the final summed output operating point. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

An example output response of a summing configuration is shown in Figure 50. The reference pin of the first circuit is connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.



V_{REF} = 0 V

Figure 50. Current Summing Application Output Response (A2 Devices)

9.1.5 Detecting Leakage Currents

Occasionally, the need arises to confirm that the current going into a load is identical to the current coming out of a load; usually, as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing, except that the two amplifiers have the inputs connected opposite of each other. To correctly detect leakage currents, the values for the current sense resistor R_{SENSE} must be the same for all channels. Also an external reference voltage must be provided to the REF1 input to allow bidirectional leakage current detection.

If the current into a load is equal to the current out of the load, then the voltage at OUT2 is the same as the applied voltage to REF1. To enable accurate differences between the two currents, a reference voltage must be applied. The reference voltage prevents the output of the device from being driven to ground, and also enables detection if the current into the load is either greater than or less than the current coming out of the load.

For current differencing, the dual-channel INA2181 must have the inputs connected opposite to each other, as shown in Figure 51. The reference input of the first channel sets the output quiescent level for all the devices in the string. Connect the output of the first channel to the reference input of the second channel. The reference input of the first channel sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current in to and out of a load do not match.

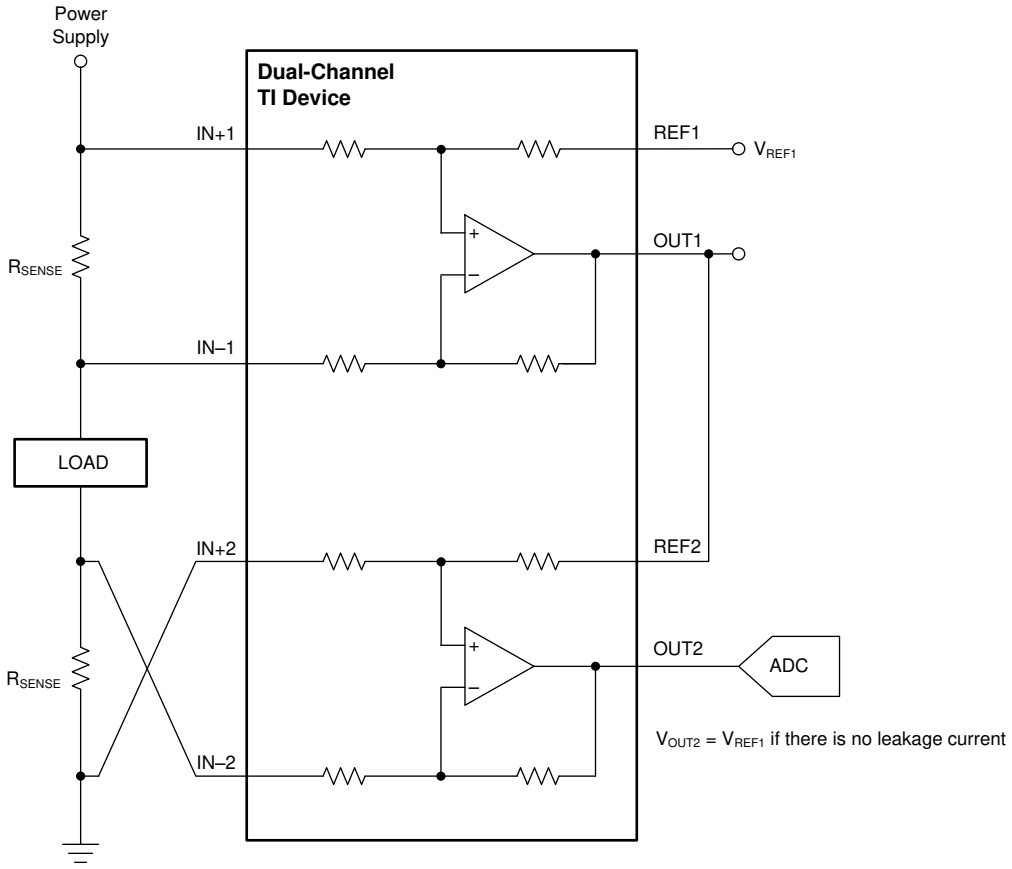
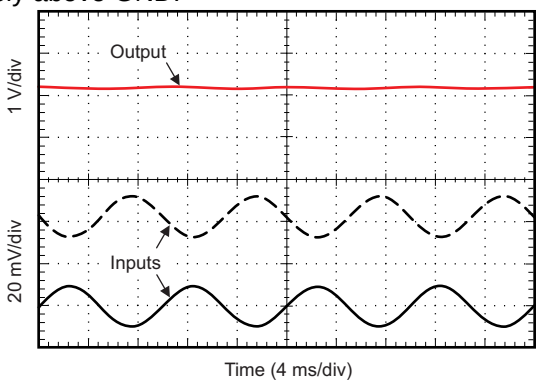


Figure 51. Detecting Leakage Currents

An example output response of a difference configuration is shown in Figure 52. The reference pin of the first channel is connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out-of-phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.



V_{REF} = 2.048 V

Figure 52. Current Differencing Application Output Response (A2 Devices)

9.2 Typical Application

One application for the INAx181 is to monitor bidirectional currents. Bidirectional currents are present in systems that have to monitor currents in both directions; common examples are monitoring the charging and discharging of batteries and bidirectional current monitoring in motor control. The device configuration for bidirectional current monitoring is shown in Figure 53. Applying stable REF pin voltage closer to the middle of device supply voltage allows both positive- and negative-current monitoring, as shown in this configuration. Configure the INAx181 to monitor unidirectional currents by grounding the REF pin.

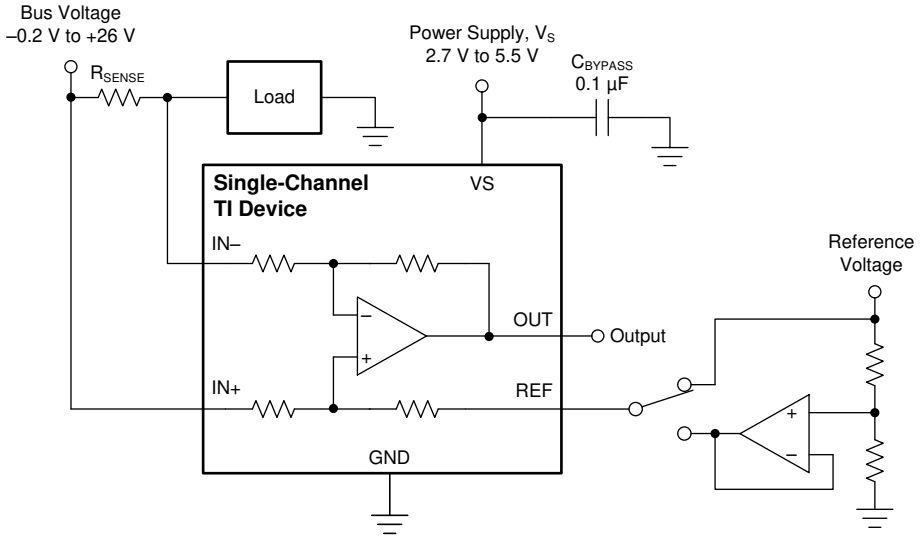


Figure 53. Measuring Bidirectional Current

9.2.1 Design Requirements

The design requirements for the circuit shown in Figure 53, are listed in Table 3

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage, V_S	5 V
Bus supply rail, V_{CM}	12 V
R_{SENSE} power loss	< 450 mW
Maximum sense current, I_{MAX}	±20 A
Current sensing error	Less than 3.5% at maximum current, T_J = 25°C
Small-signal bandwidth	> 100 kHz

9.2.2 Detailed Design Procedure

The maximum value of the current sense resistor is calculated based on the maximum power loss requirement. By applying Equation 2, the maximum value of the current-sense resistor is calculated to be 1.125 mΩ. This is the maximum value for sense resistor R_{SENSE}; therefore, select R_{SENSE} to be 1 mΩ because it is the closest standard resistor value that meets the power-loss requirement.

The next step is to select the appropriate gain and reduce R_{SENSE}, if needed, to keep the output signal swing within the V_S range. The design requirements call for bidirectional current monitoring; therefore, a voltage between 0 and V_S must be applied to the REF pin. The bidirectional currents monitored are symmetric around 0 (that is, ±20 A); therefore, the ideal voltage to apply to V_{REF} is V_S / 2 or 2.5 V. If the positive current is greater than the negative current, using a lower voltage on V_{REF} has the benefit of maximizing the output swing for the given range of expected currents. Using Equation 3, and given that I_{MAX} = 20 A , R_{SENSE} = 1 mΩ, and V_{REF} = 2.5

V, the maximum current-sense gain calculated to avoid the positive swing-to-rail limitations on the output is 122.5. Likewise, using Equation 4 for the negative-swing limitation results in a maximum gain of 124.75. Selecting the gain-of-100 device maximizes the output range while staying within the output swing range. If the maximum calculated gains are slightly less than 100, the value of the current-sense resistor can be reduced to keep the output from hitting the output-swing limitations.

To calculate the accuracy at peak current, the two factors that must be determined are the gain error and the offset error. The gain error of the INAx181 is specified to be a maximum of 1%. The error due to the offset is constant, and is specified to be 500 µV (maximum) for the conditions where V_{CM} = 12 V and V_S = 5 V. Using Equation 7, the percentage error contribution of the offset voltage is calculated to be 2.5%, with total offset error = 500 µV, R_{SENSE} = 1 mΩ, and I_{SENSE} = 20 A.

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \tag{7}$$

One method of calculating the total error is to add the gain error to the percentage contribution of the offset error. However, in this case, the gain error and the offset error do not have an influence or correlation to each other. A more statistically accurate method of calculating the total error is to use the RSS sum of the errors, as shown in Equation 8:

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \tag{8}$$

After applying Equation 8, the total current sense error at maximum current is calculated to be 2.7%, and that is less than the design example requirement of 3.5%.

The INA181A3 (gain = 100) also has a bandwidth of 150 kHz that meets the small-signal bandwidth requirement of 100 kHz. If higher bandwidth is required, lower-gain devices can be used at the expense of either reduced output voltage range or an increased value of R_{SENSE}.

9.2.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 54. With the REF pin connected to a reference voltage (2.5 V in this case), the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals, and falls below the reference voltage for negative differential input signals.

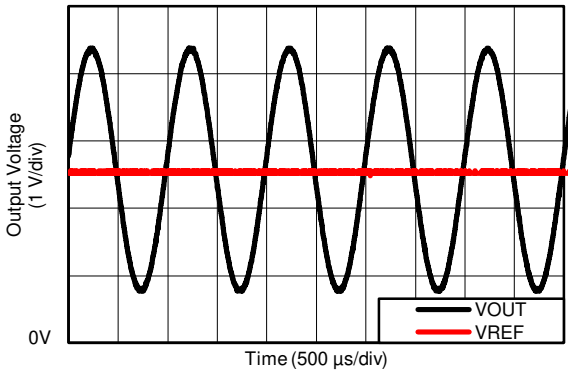


Figure 54. Bidirectional Application Output Response

10 Power Supply Recommendations

The input circuitry of the INAx181 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the VS pin. The INAx181 also withstand the full differential input signal range up to 26 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin.

10.1 Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INAx181 can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode; see Figure 55. Keep these resistors as small as possible; most often, around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Filtering* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

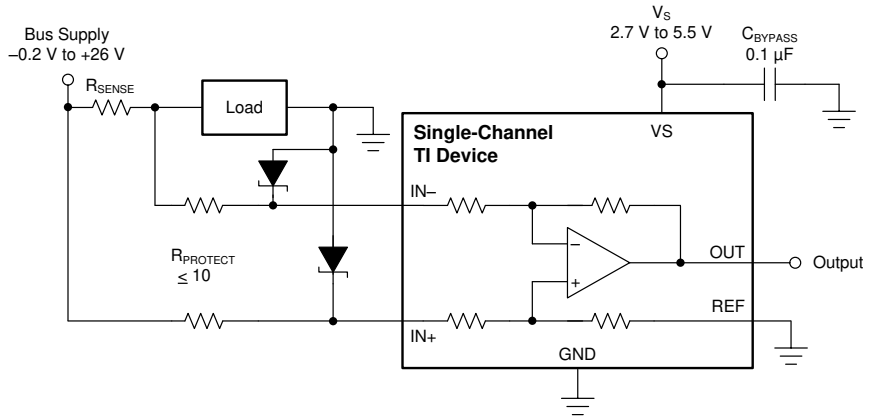


Figure 55. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in Figure 56. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in Figure 55 and Figure 56, the total board area required by the INAx181 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

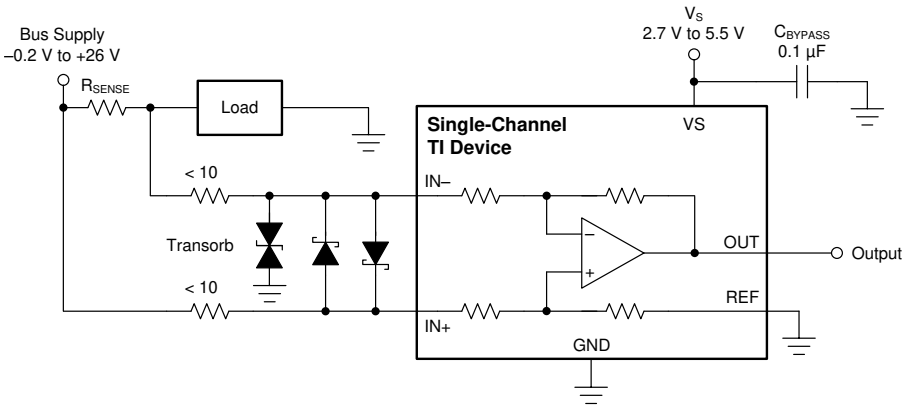


Figure 56. Transient Protection Using a Single Transzorb and Input Clamps

Common-Mode Transients Greater Than 26 V (continued)

For more information, see *Current Shunt Monitor With Transient Robustness Reference Design*.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current sense resistor to the device, keep the trace lengths as close as possible in order to minimize any impedance mismatch..

11.2 Layout Example

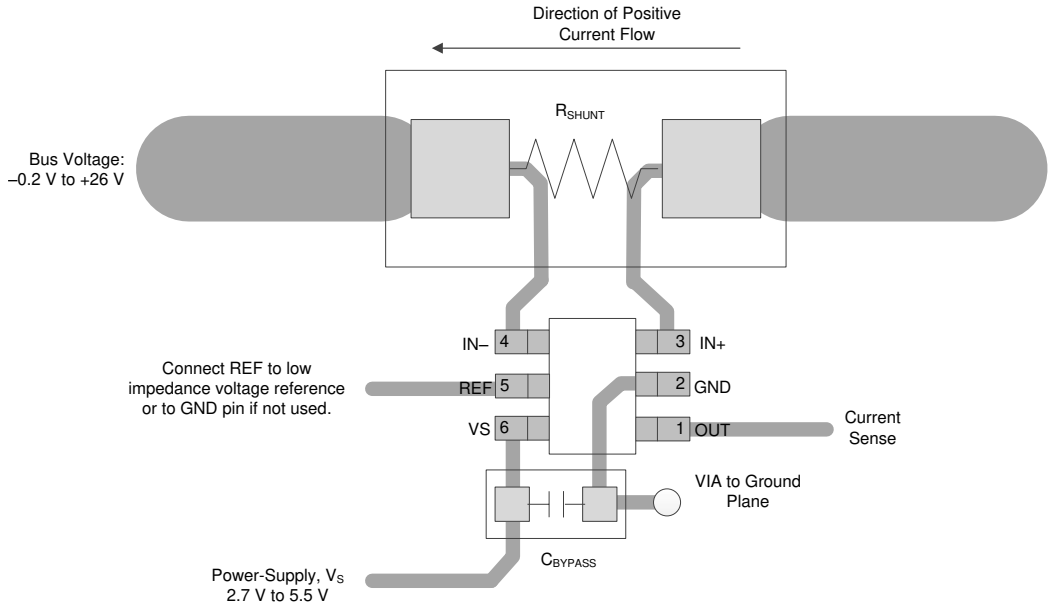


Figure 57. Single-Channel Recommended Layout

Layout Example (continued)

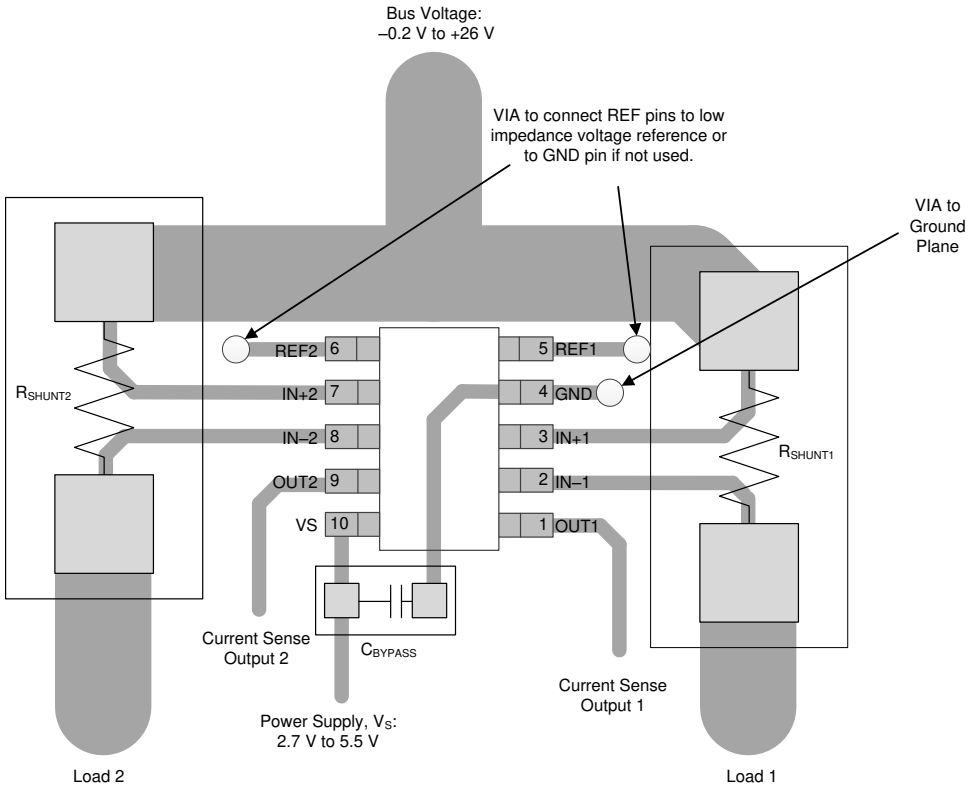


Figure 58. Dual-Channel Recommended Layout (VSSOP)

Layout Example (continued)

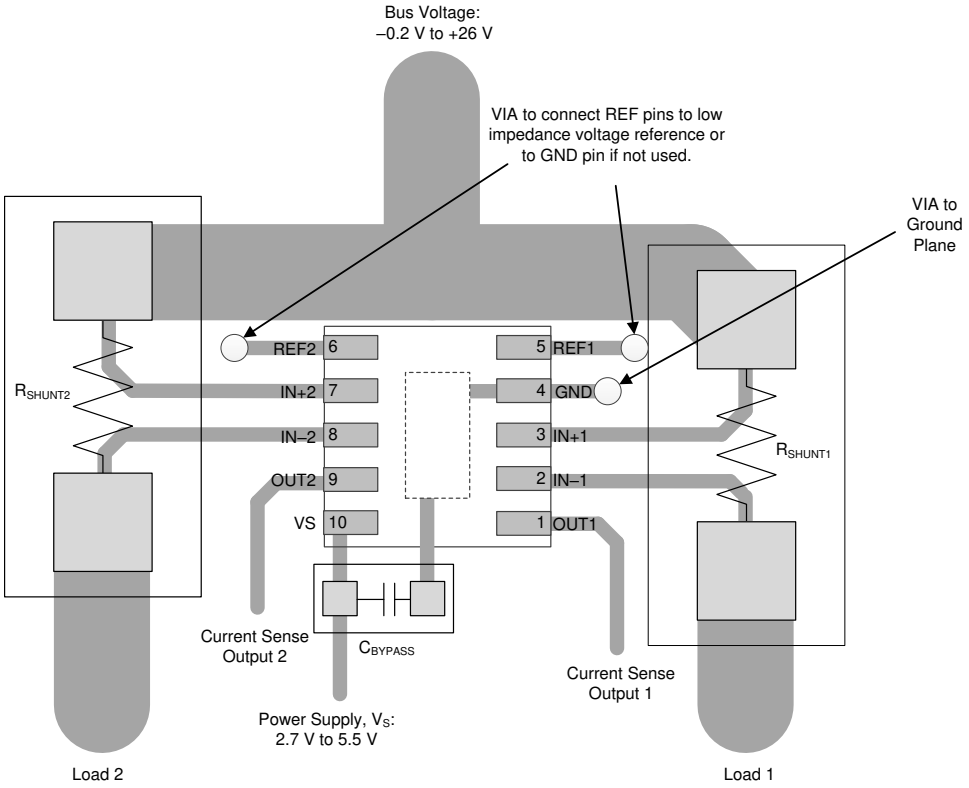


Figure 59. Dual-Channel Recommended Layout (WSON)

Layout Example (continued)

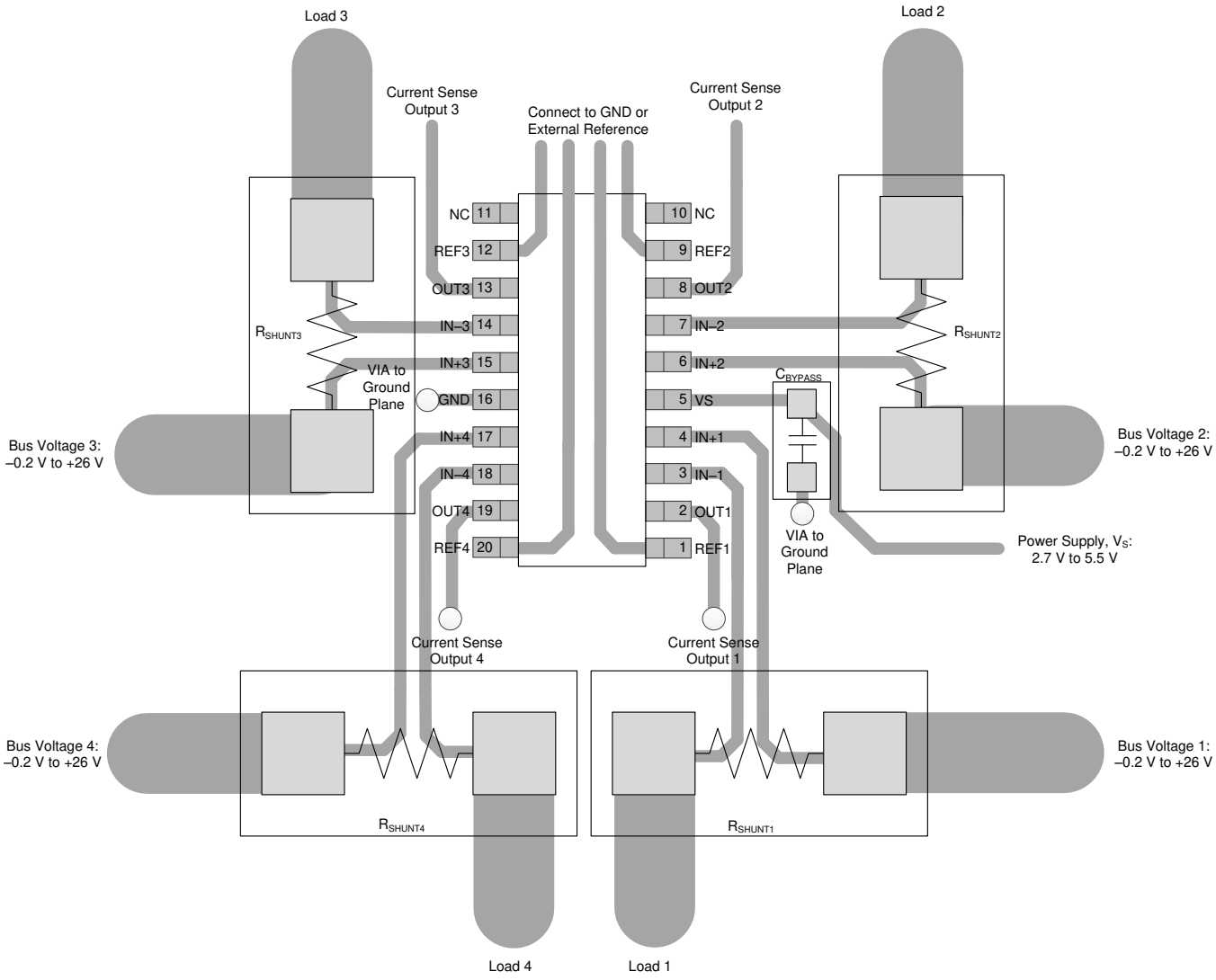


Figure 60. Quad-Channel Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Current Shunt Monitor With Transient Robustness Reference Design

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA180-181EVM User's Guide*
- Texas Instruments, *INA2180-2181EVM User's Guide*
- Texas Instruments, *INA4180-4181EVM User's Guide*

12.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA181	Click here	Click here	Click here	Click here	Click here
INA2181	Click here	Click here	Click here	Click here	Click here
INA4181	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA181A1IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	18JD	Samples
INA181A1IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	18JD	Samples
INA181A2IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AED	Samples
INA181A2IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AED	Samples
INA181A3IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AFD	Samples
INA181A3IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AFD	Samples
INA181A4IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AGD	Samples
INA181A4IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AGD	Samples
INA2181A1IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CW6	Samples
INA2181A1IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CW6	Samples
INA2181A1IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25IY	Samples
INA2181A1IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25IY	Samples
INA2181A2IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DR6	Samples
INA2181A2IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DR6	Samples
INA2181A2IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25JY	Samples
INA2181A2IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25JY	Samples
INA2181A3IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DS6	Samples
INA2181A3IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DS6	Samples
INA2181A3IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25KY	Samples
INA2181A3IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25KY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2181A4IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DT6	Samples
INA2181A4IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DT6	Samples
INA2181A4IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25LY	Samples
INA2181A4IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25LY	Samples
INA4181A1IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A1	Samples
INA4181A2IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A2	Samples
INA4181A3IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A3	Samples
INA4181A4IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA181, INA2181, INA4181 :

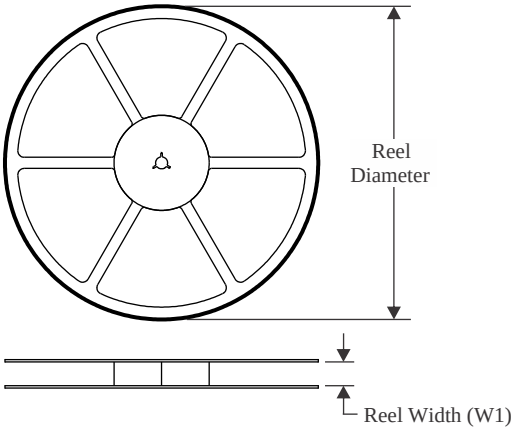
- Automotive : INA181-Q1, INA2181-Q1, INA4181-Q1

NOTE: Qualified Version Definitions:

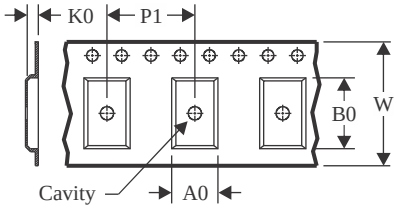
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

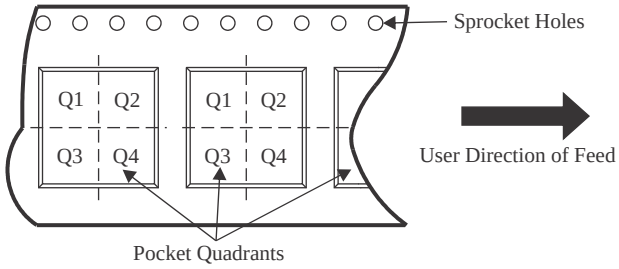


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

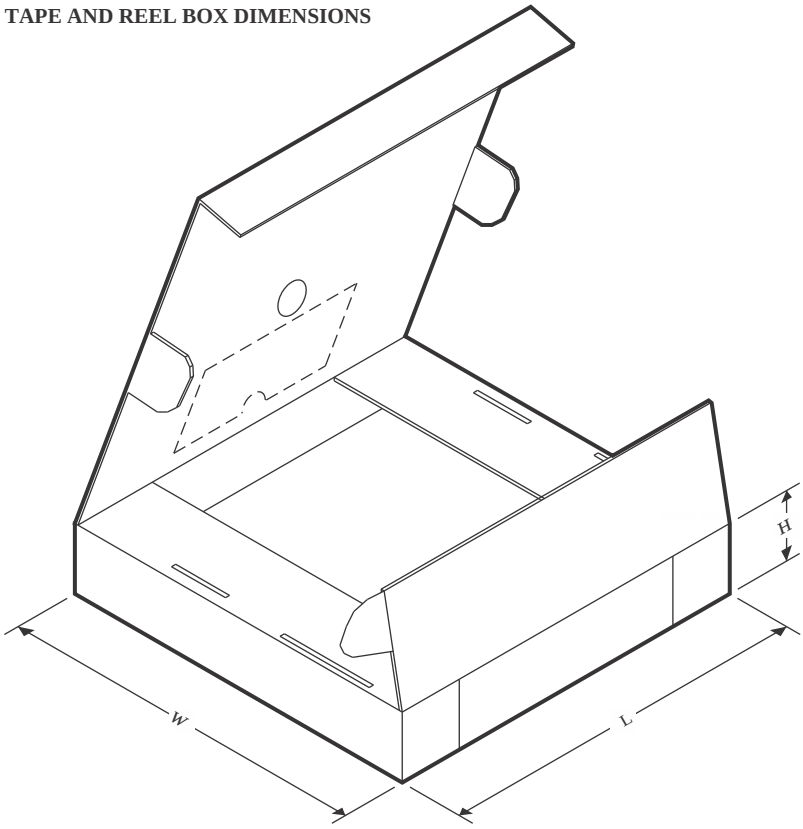


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA181A1IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A1IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A2IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A2IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A3IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A3IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A4IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A4IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA2181A1IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A1IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A1IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A1IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A2IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A2IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A2IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A2IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2181A3IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A3IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A4IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A4IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A4IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A4IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA4181A1IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A2IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A3IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A4IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA181A1IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A1IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A2IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A2IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A3IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A3IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A4IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A4IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA2181A1IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A1IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A1IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A1IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A2IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A2IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A2IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A2IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A3IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A3IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0

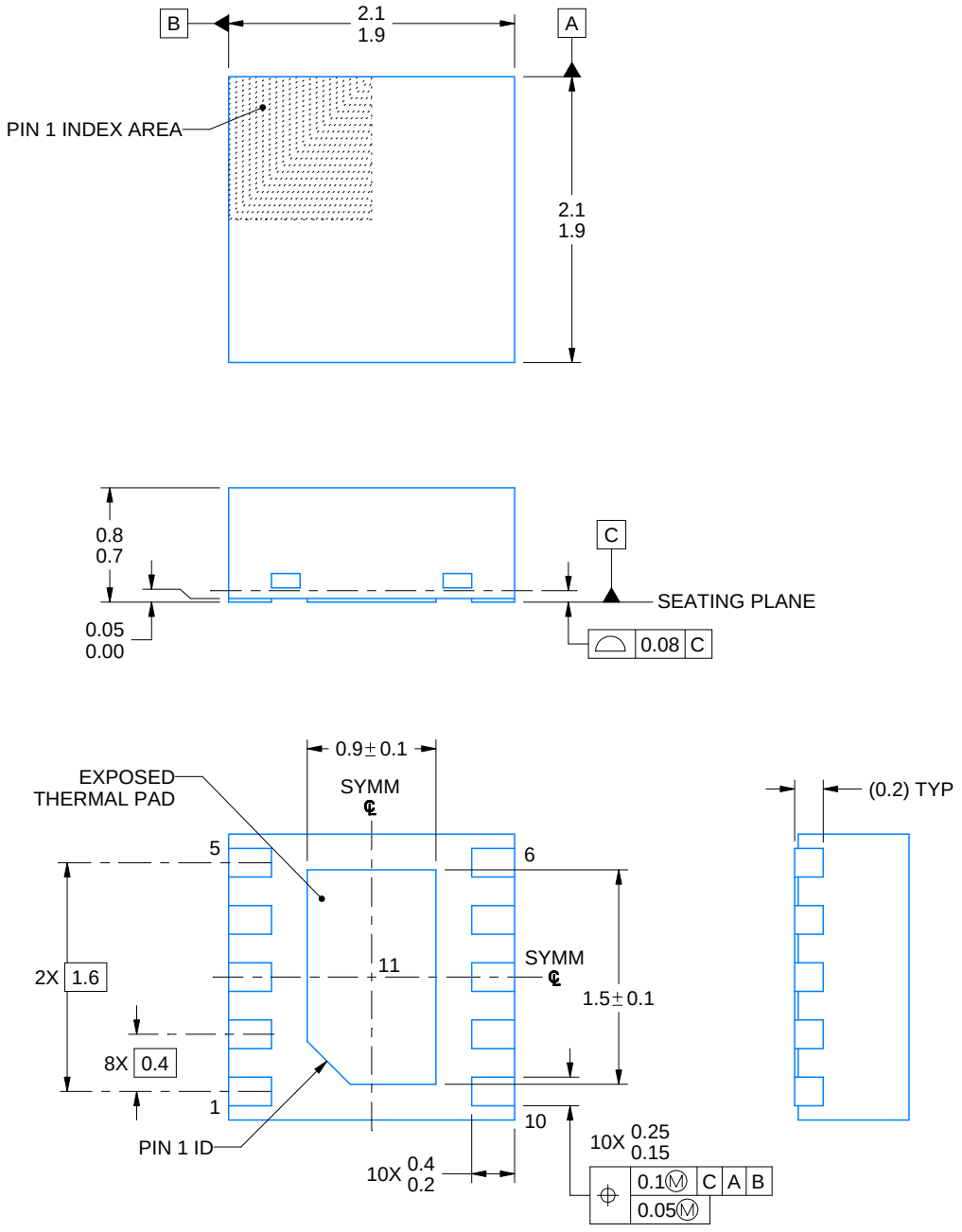
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2181A3IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A3IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A4IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A4IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A4IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A4IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA4181A1IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A2IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A3IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A4IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DSQ0010A

WSON - 0.8 mm max height

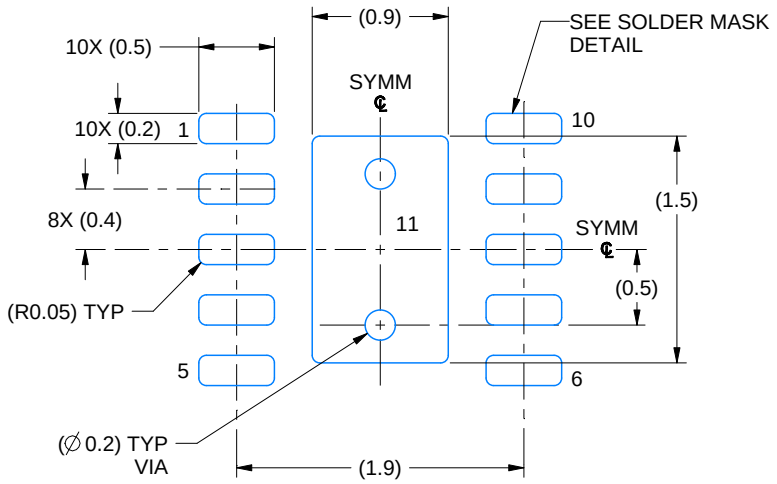
PLASTIC SMALL OUTLINE - NO LEAD



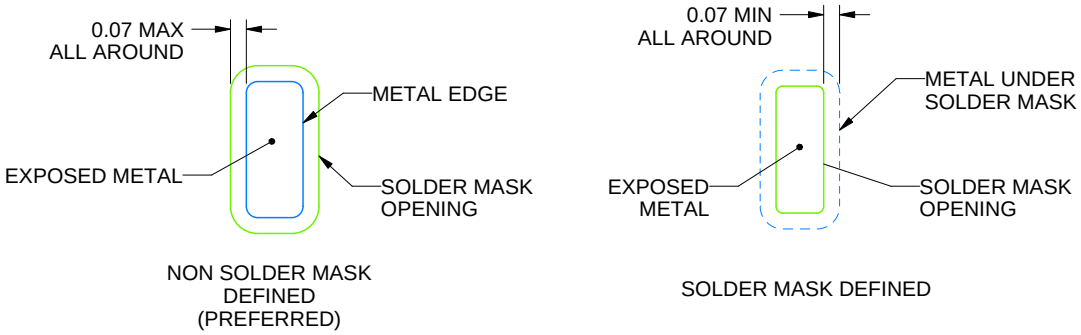
4218906/A 04/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

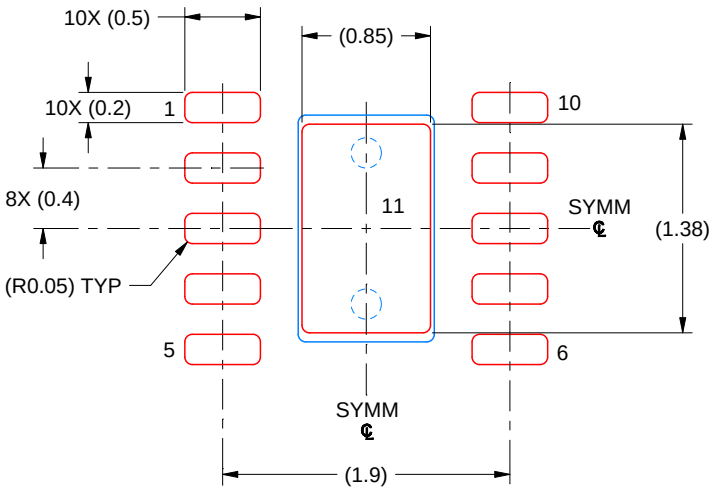


SOLDER MASK DETAILS

4218906/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

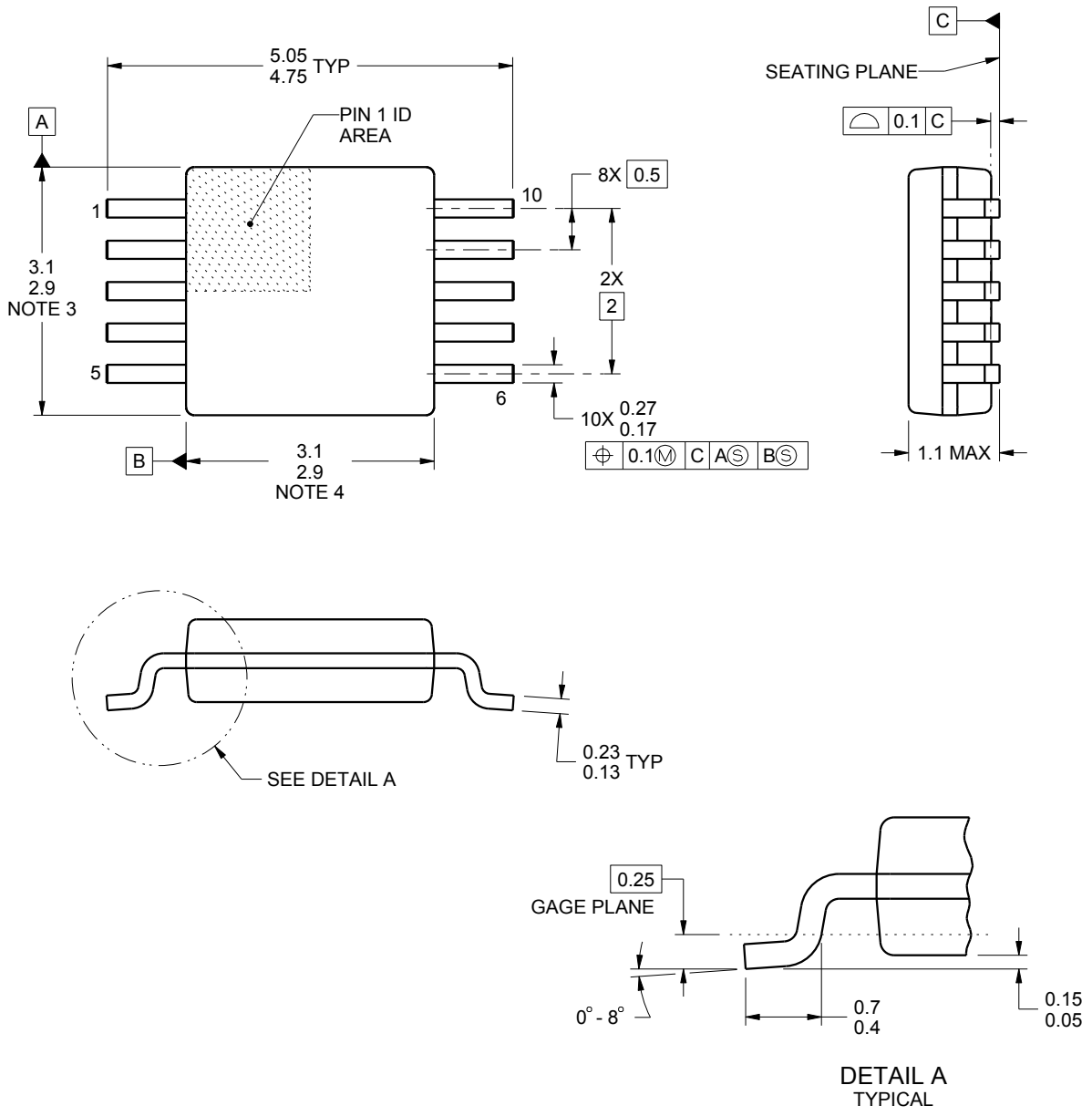
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

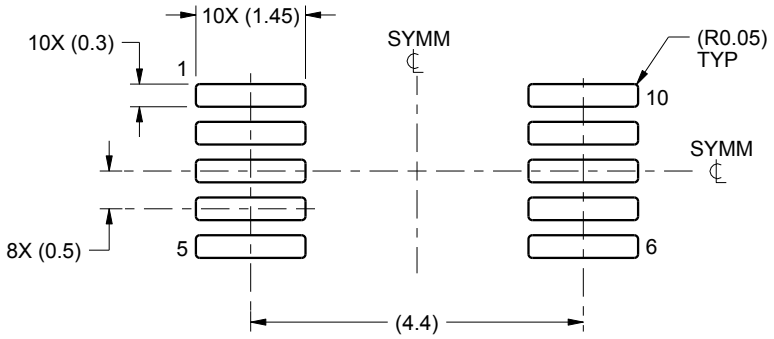
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

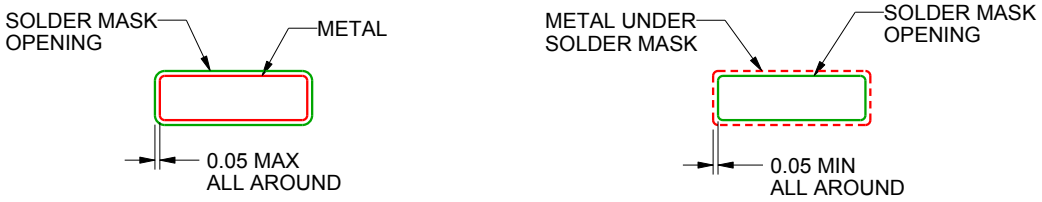


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

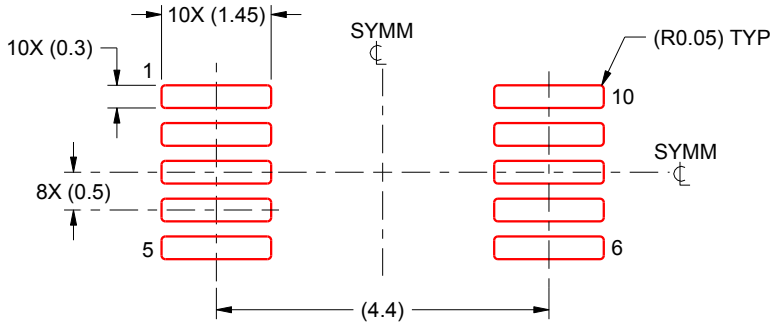


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

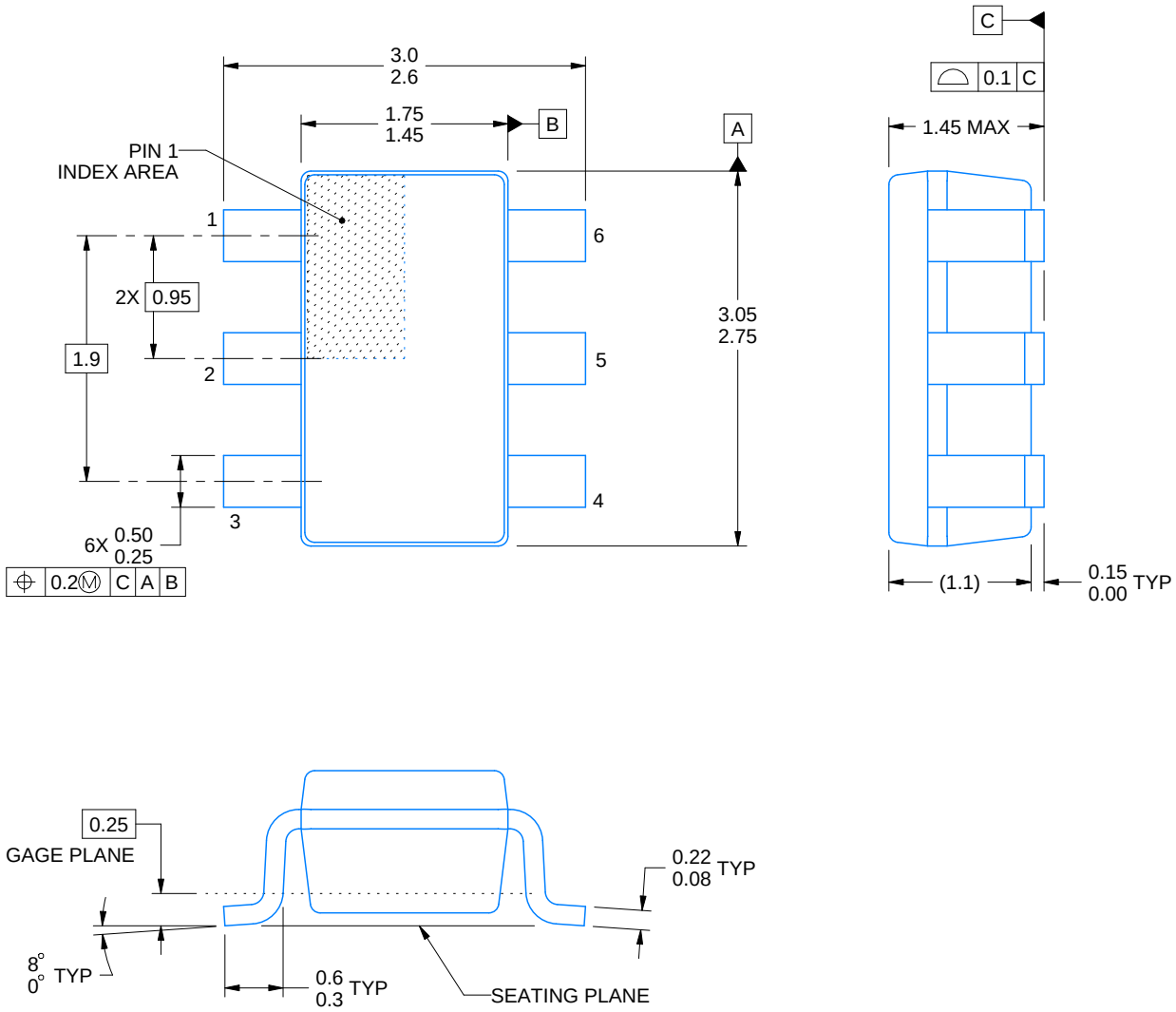
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

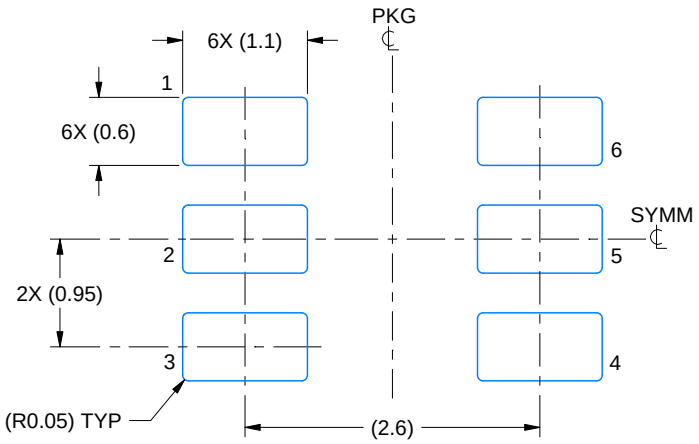
SMALL OUTLINE TRANSISTOR



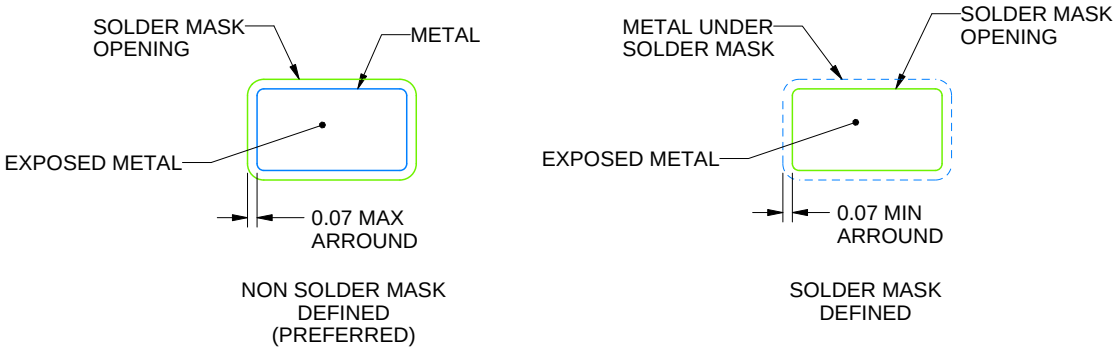
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

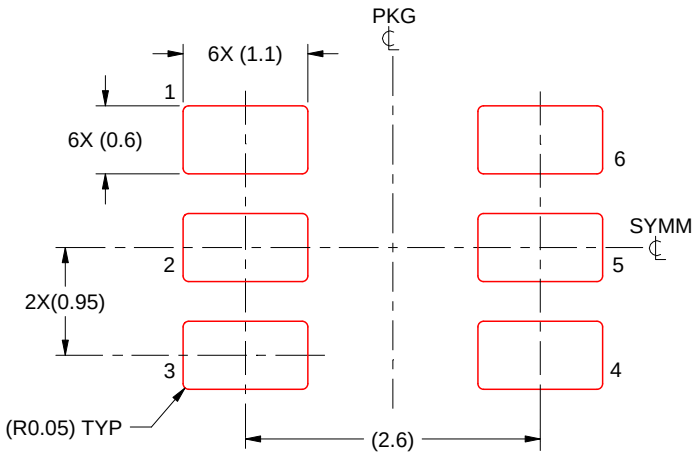


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

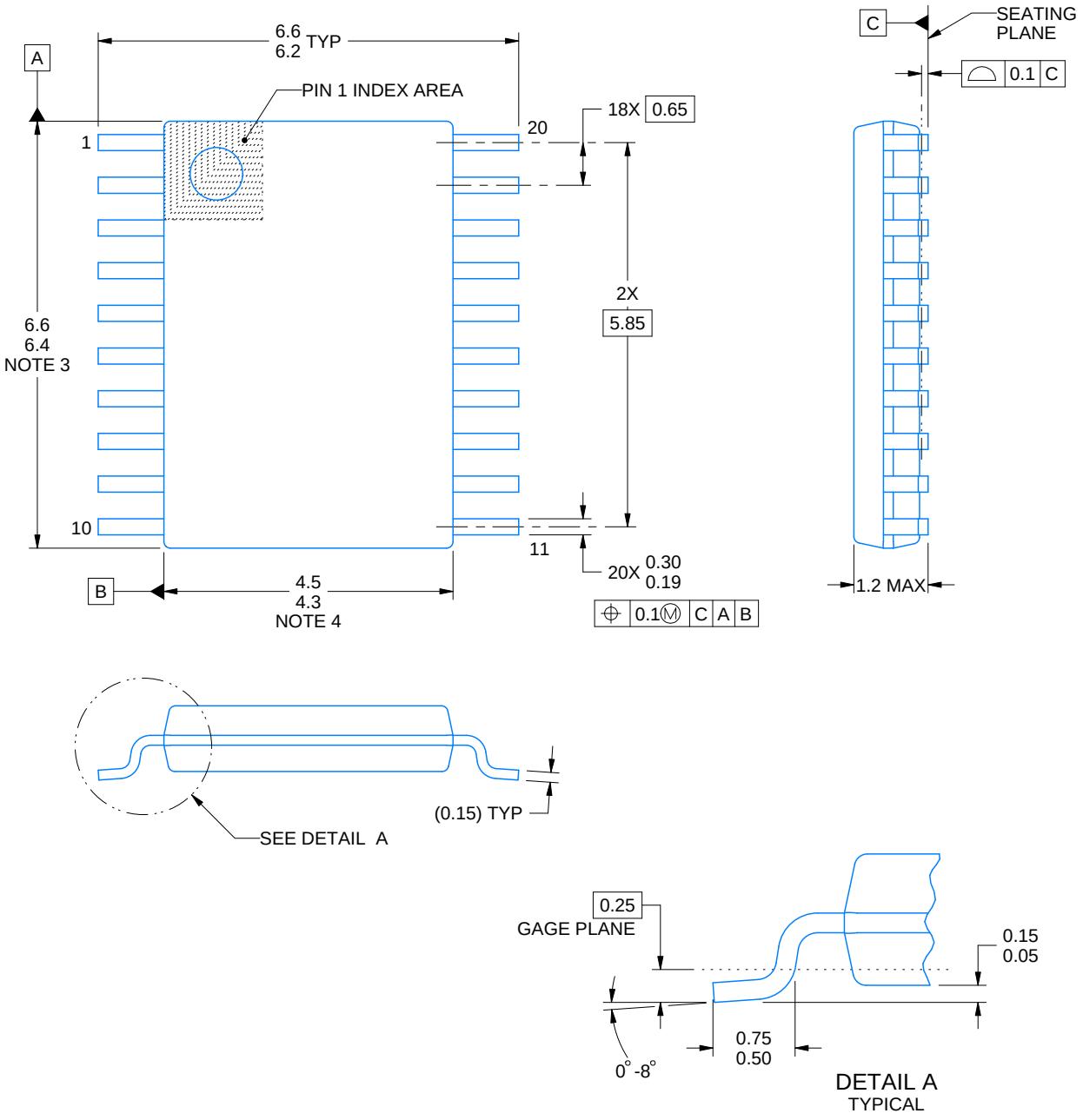
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

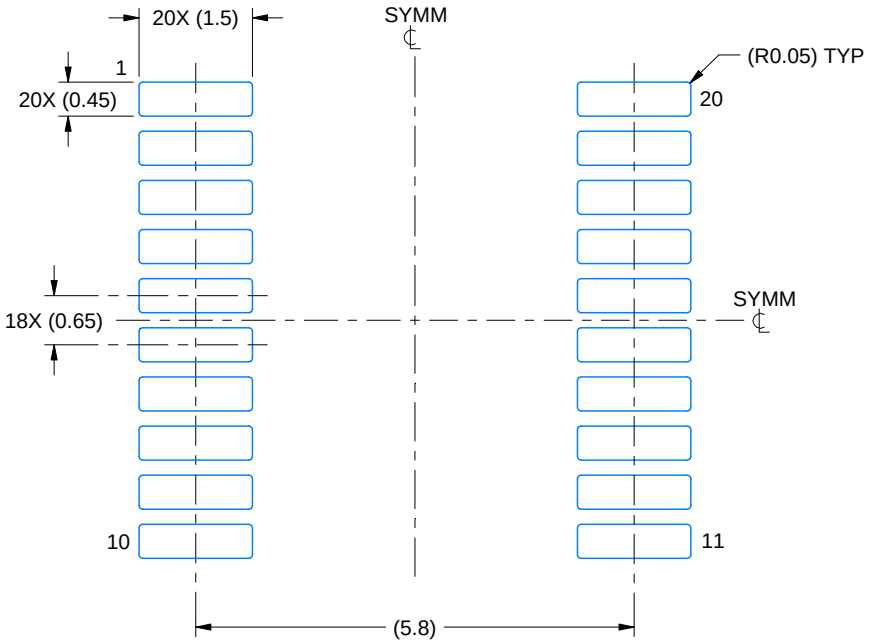
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

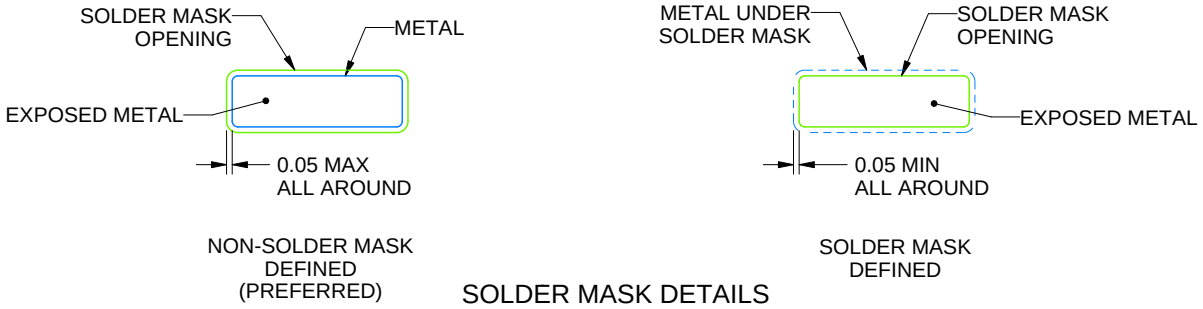


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

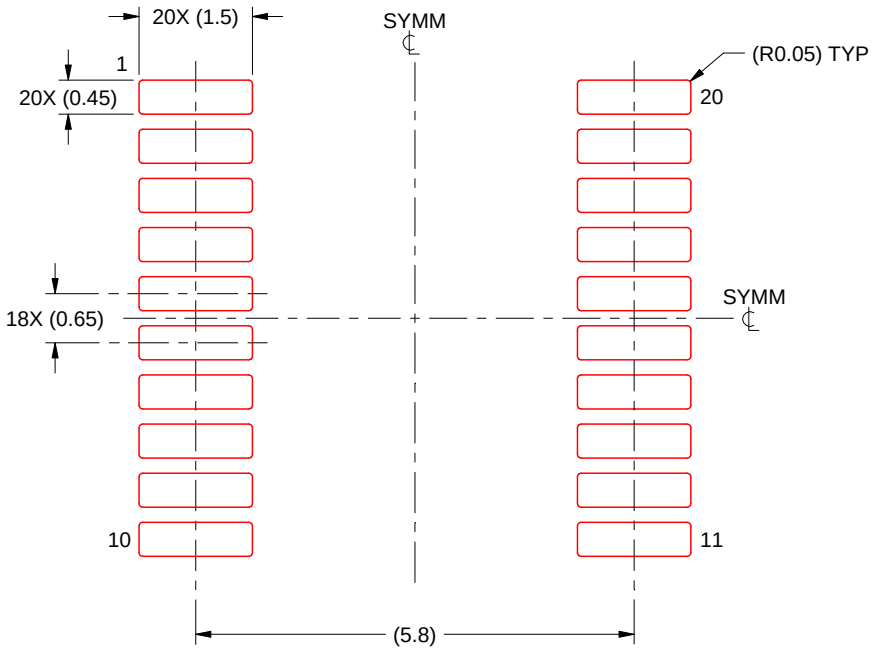


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



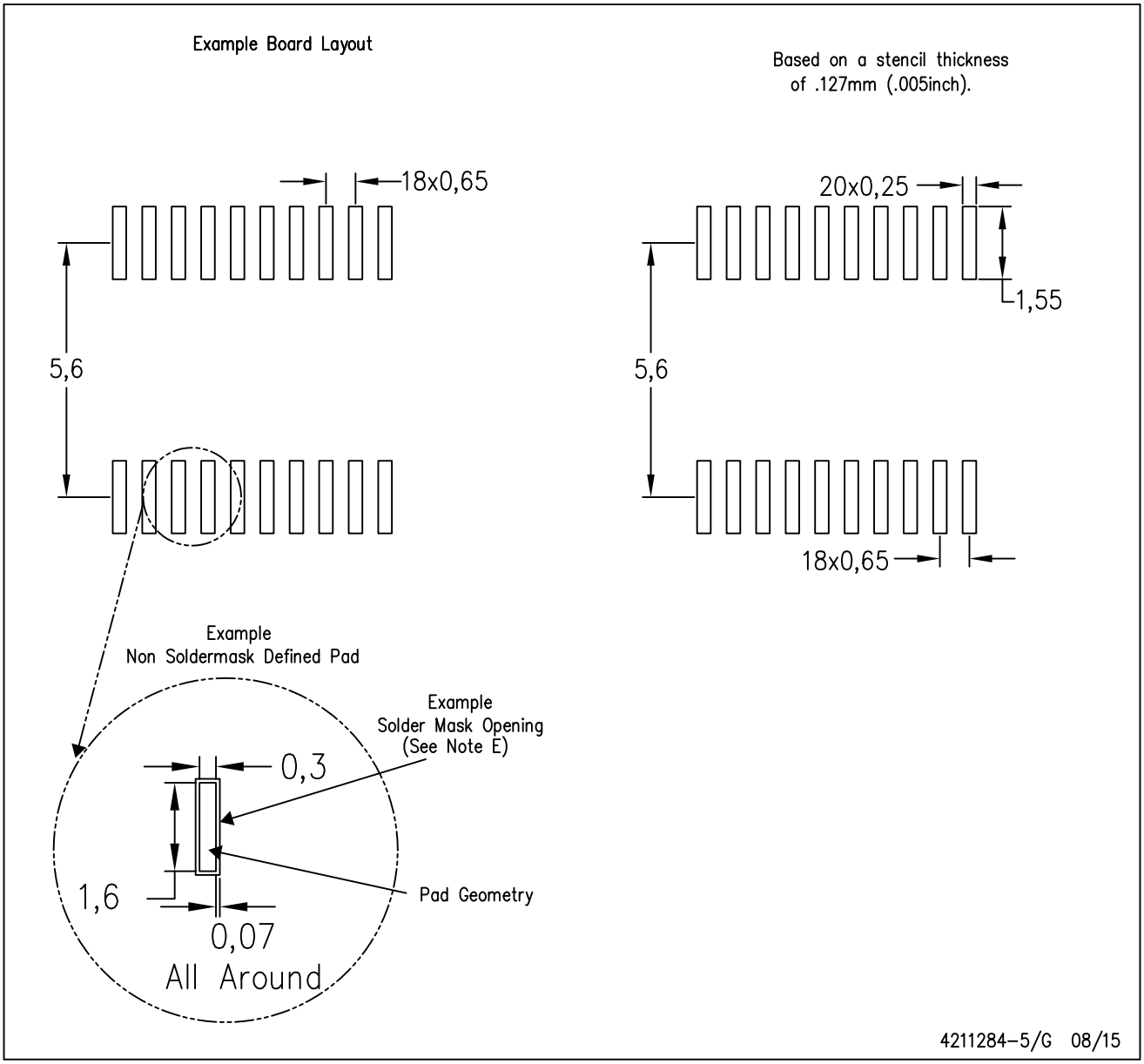
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

INA225 36-V, Programmable-Gain, Voltage-Output, Bidirectional, Zero-Drift Series, Current-Shunt Monitor

1 Features

- Wide Common-Mode Range: 0 V to 36 V
- Offset Voltage: ±150 µV (Max, All Gains)
- Offset Voltage Drift: 0.5 µV/°C (Max)
- Gain Accuracy, Over Temperature (Max):
  - 25 V/V, 50 V/V: ±0.15%
  - 100 V/V: ±0.2%
  - 200 V/V: ±0.3%
  - 10-ppm/°C Gain Drift
- 250-kHz Bandwidth (Gain = 25 V/V)
- Programmable Gains:
  - G1 = 25 V/V
  - G2 = 50 V/V
  - G3 = 100 V/V
  - G4 = 200 V/V
- Quiescent Current: 350 µA (Max)
- Package: MSOP-8

2 Applications

- Power Supplies
- Motor Control
- Computers
- Telecom Equipment
- Power Management
- Test and Measurement

3 Description

The INA225 is a voltage-output, current-sense amplifier that senses drops across current-sensing resistors at common-mode voltages that can vary from 0 V to 36 V, independent of the supply voltage. The device is a bidirectional, current-shunt monitor that allows an external reference to be used to measure current flowing in both directions across a current-sensing resistor.

Four discrete gain levels are selectable using the two gain-select terminals (GS0 and GS1) to program gains of 25 V/V, 50 V/V, 100 V/V, and 200 V/V. The low-offset, zero-drift architecture and precision gain values enable current-sensing with maximum drops across the shunt as low as 10 mV of full-scale while maintaining very high accuracy measurements over the entire operating temperature range.

The device operates from a single +2.7-V to +36-V power supply, drawing a maximum of 350 µA of supply current. The device is specified over the extended operating temperature range (–40°C to +125°C), and is offered in an MSOP-8 package.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
INA225AIDGK	MSOP (8)	3,0 mm x 3,0 mm

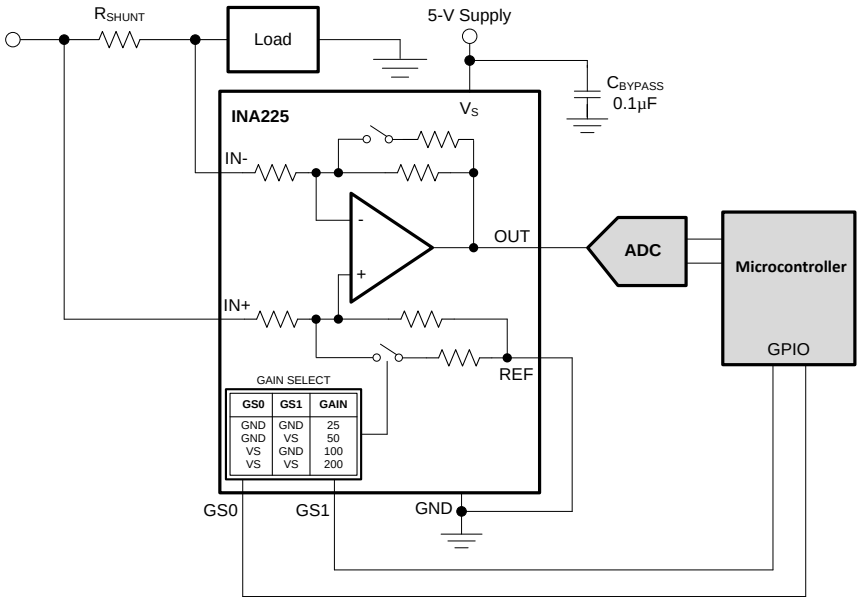


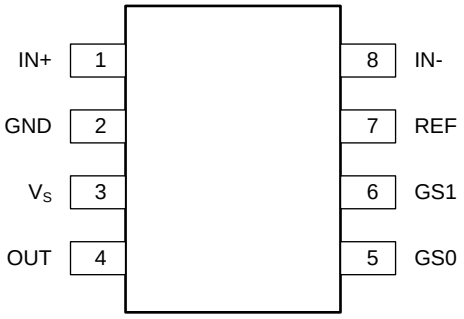
Table of Contents

4 Revision History

Changes from Original (February 2014) to Revision A	Page
• Made changes to product preview data sheet	1

5 Terminal Configuration and Functions

DGK Package
MSOP-8
(Top View)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN+	1	Analog input	Connect to supply side of shunt resistor.
GND	2	Analog	Ground
V_S	3	Analog	Power supply, 2.7 V to 36 V
OUT	4	Analog output	Output voltage
GS0	5	Digital input	Gain select. Connect to V_S or GND. Table 3 lists terminal settings and the corresponding gain value.
GS1	6	Digital input	Gain select. Connect to V_S or GND. Table 3 lists terminal settings and the corresponding gain value.
REF	7	Analog input	Reference voltage, 0 V to V_S
IN–	8	Analog input	Connect to load side of shunt resistor.

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Supply voltage			+40	V
Analog inputs, V_{IN+}, V_{IN-}(2)	Differential (V_{IN+}) – (V_{IN-})	–40	+40	V
	Common-mode(3)	GND – 0.3	+40	V
REF, GS0, and GS1 inputs		GND – 0.3	(V_S) + 0.3	V
Output		GND – 0.3	(V_S) + 0.3	V
Temperature	Operating, T_A	–55	+150	°C
	Junction, T_J		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage at any terminal may exceed the voltage shown if the current at that terminal is limited to 5 mA.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	+150	°C
V_{ESD} (1)	Human body model (HBM) stress voltage(2)		4	kV
	Charged device model (CDM) stress voltage(3)		1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 4-kV HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 1-kV CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		+125	°C

6.4 Thermal Information

THERMAL METRIC		INA225 DGK (MSOP) 8 TERMINALS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	163.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	57.7	
θ_{JB}	Junction-to-board thermal resistance	84.7	
ψ_{JT}	Junction-to-top characterization parameter	6.5	
ψ_{JB}	Junction-to-board characterization parameter	83.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

6.5 Electrical Characteristics

At T_A = +25°C, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_S = +5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	T_A = –40°C to +125°C	0		36	V
CMR	Common-mode rejection	V_{IN+} = 0 V to +36 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C	95	105		dB
V_{OS}	Offset voltage, RTI(1)	V_{SENSE} = 0 mV		±75	±150	µV
dV_{OS}/dT	RTI vs temperature	T_A = –40°C to +125°C		0.2	0.5	µV/°C
PSRR	Power-supply rejection ratio	V_{SENSE} = 0 mV, V_{REF} = 2.5 V, V_S = 2.7 V to 36 V		±0.1	±1	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV	55	72	85	µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.5		µA
V_{REF}	Reference input range	T_A = –40°C to +125°C	0		V_S	V
OUTPUT						
G	Gain			25, 50, 100, 200		V/V
E_G	Gain error	Gain = 25 V/V and 50 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C		±0.05%	±0.15%	
		Gain = 100 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C		±0.1%	±0.2%	
		Gain = 200 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C		±0.1%	±0.3%	
	Gain error vs temperature	G = 25 V/V, 50 V/V, 100 V/V, T_A = –40°C to +125°C		3	10	ppm/°C
		G = 200 V/V, T_A = –40°C to +125°C		5	15	
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_S – 0.05	V_S – 0.2	V
	Swing to GND(3)	$V_{REF} = V_S / 2$, all gains, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 5	V_{GND} + 10	mV
		V_{REF} = GND, gain = 25 V/V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 7		mV
		V_{REF} = GND, gain = 50 V/V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 15		mV
		V_{REF} = GND, gain = 100 V/V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 30		mV
		V_{REF} = GND, gain = 200 V/V, R_L = 10 kΩ to GND, T_A = –40°C to +125°C		V_{GND} + 60		mV
FREQUENCY RESPONSE						
BW	Bandwidth	Gain = 25 V/V, C_{LOAD} = 10 pF		250		kHz
		Gain = 50 V/V, C_{LOAD} = 10 pF		200		kHz
		Gain = 100 V/V, C_{LOAD} = 10 pF		125		kHz
		Gain = 200 V/V, C_{LOAD} = 10 pF		70		kHz
SR	Slew rate			0.4		V/µs
NOISE, RTI(1)						
	Voltage noise density			50		nV/√Hz

(1) RTI = referred-to-input.
(2) See Typical Characteristic curve, *Output Voltage Swing vs Output Current* (Figure 10).
(3) See Typical Characteristic curve, *Unidirectional Output Voltage Swing vs. Temperature* (*Figure 14*)

Electrical Characteristics (continued)

At T_A = +25°C, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_S = +5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
C_i	Input capacitance			3		pF
	Leakage input current	$0 \le V_{IN} \le V_S$		1	2	µA
V_{IL}	Low-level input logic level		0		0.6	V
V_{IH}	High-level input logic level		2		V_S	V
POWER SUPPLY						
V_S	Operating voltage range	T_A = –40°C to +125°C	+2.7		+36	V
I_Q	Quiescent current	V_{SENSE} = 0 mV		300	350	µA
	I_Q over temperature	T_A = –40°C to +125°C			375	µA
TEMPERATURE RANGE						
	Specified range		–40		+125	°C
	Operating range		–55		+150	°C

6.6 Typical Characteristics

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

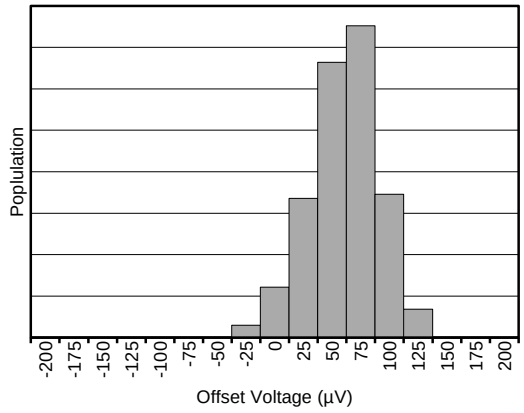


Figure 1. Input Offset Voltage Production Distribution

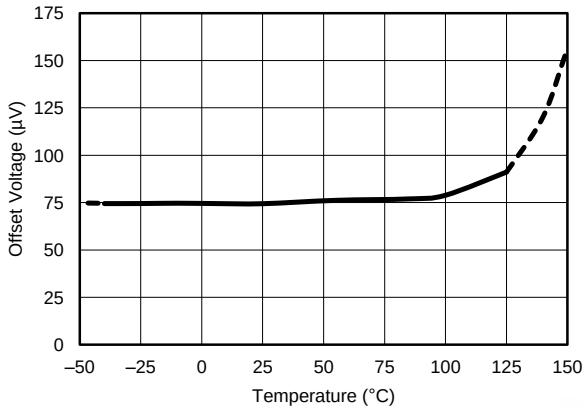


Figure 2. Input Offset Voltage vs Temperature

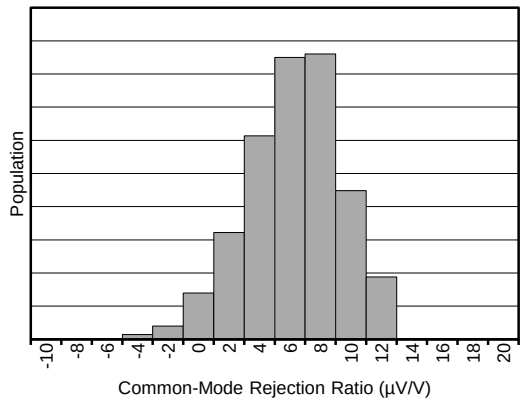


Figure 3. Common-Mode Rejection Production Distribution

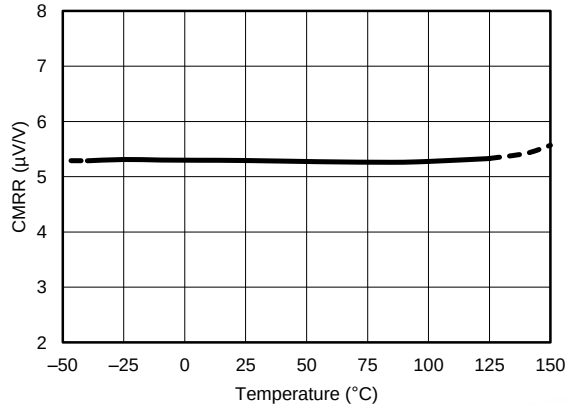


Figure 4. Common-Mode Rejection Ratio vs Temperature

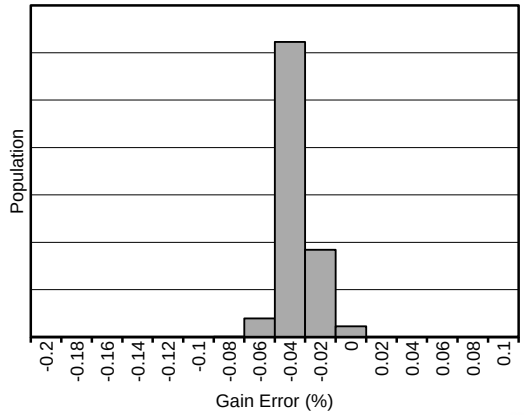


Figure 5. Gain Error Production Distribution (Gain = 25 V/V)

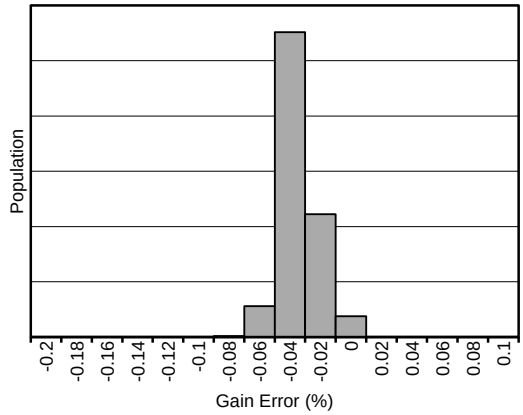


Figure 6. Gain Error Production Distribution (Gain = 50 V/V)

Typical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

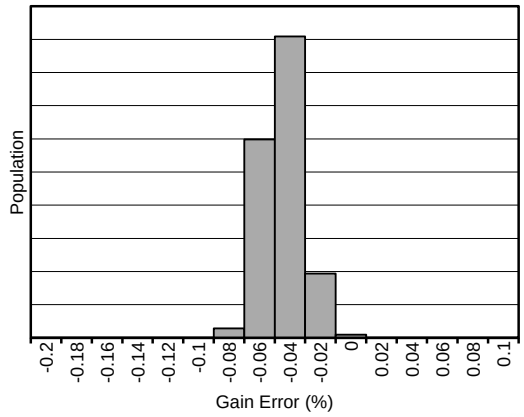


Figure 7. Gain Error Production Distribution (Gain = 100 V/V)

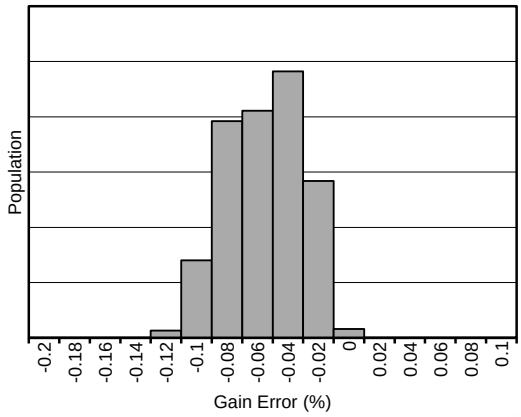


Figure 8. Gain Error Production Distribution (Gain = 200 V/V)

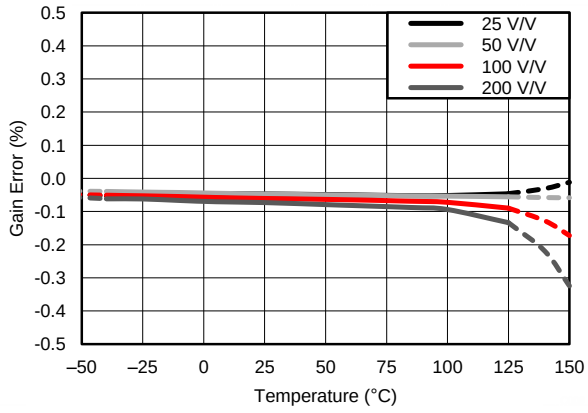
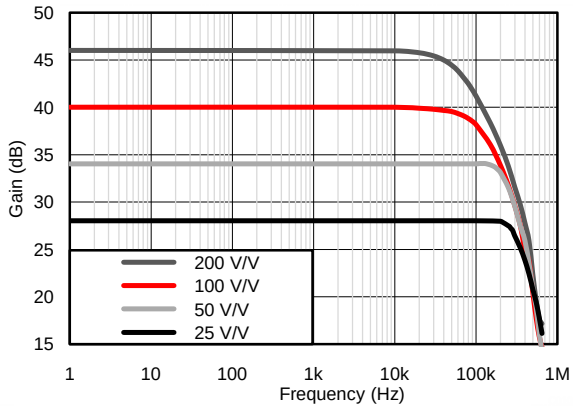
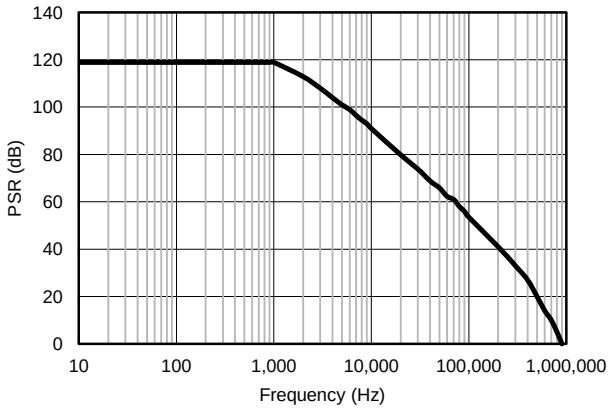


Figure 9. Gain Error vs Temperature



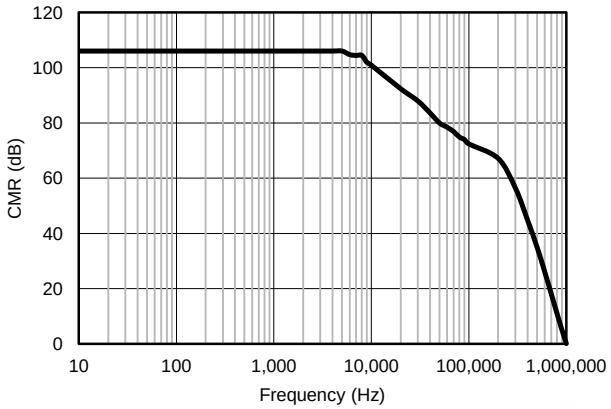
V_{CM} = 0 V V_{SENSE} = 15 mV_{PP}

Figure 10. Gain vs Frequency



V_{CM} = 0 V V_{REF} = 2.5 V V_{SENSE} = 0 mV, Shorted
V_S = 5 V + 250-mV Sine Disturbance

Figure 11. Power-Supply Rejection Ratio vs Frequency



V_S = 5 V V_{REF} = 2.5 V V_{SENSE} = 0 mV, Shorted
V_{CM} = 1-V Sine Wave

Figure 12. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

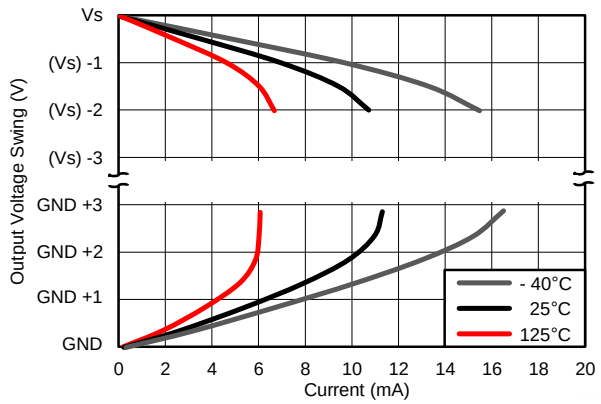
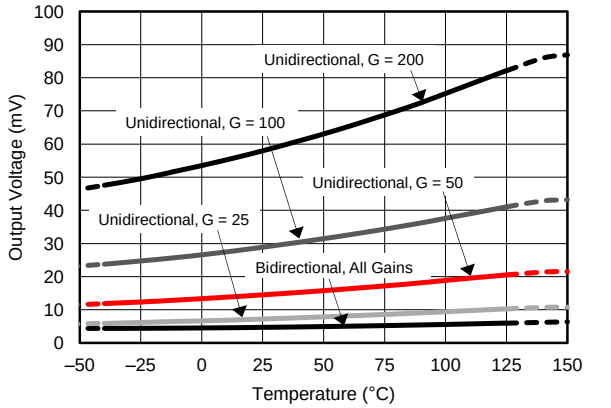


Figure 13. Output Voltage Swing vs Output Current



Unidirectional, REF = GND Bidirectional, REF > GND

Figure 14. Unidirectional Output Voltage Swing vs. Temperature

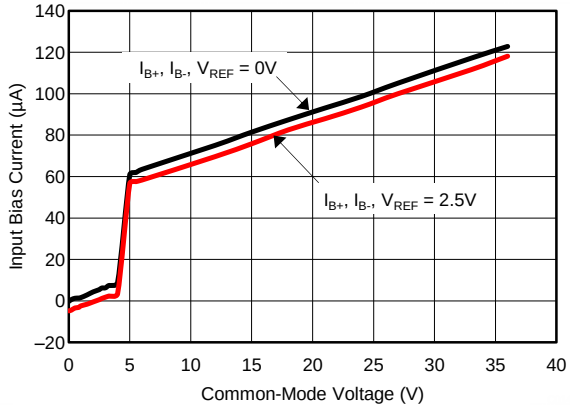


Figure 15. Input Bias Current vs Common-Mode Voltage (Supply Voltage = +5 V)

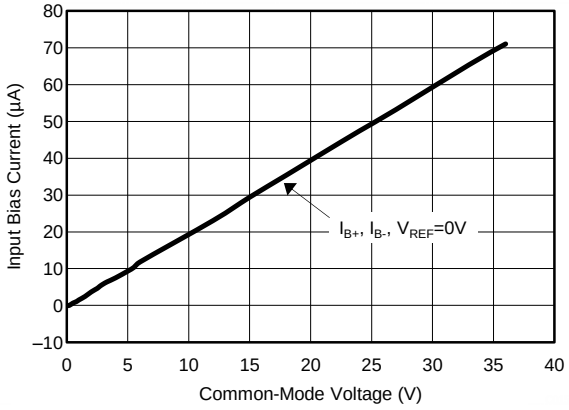


Figure 16. Input Bias Current vs Common-Mode Voltage (Supply Voltage = 0 V, Shutdown)

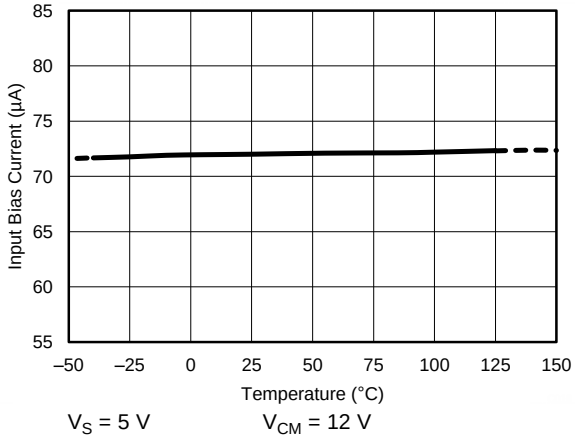


Figure 17. Input Bias Current vs Temperature

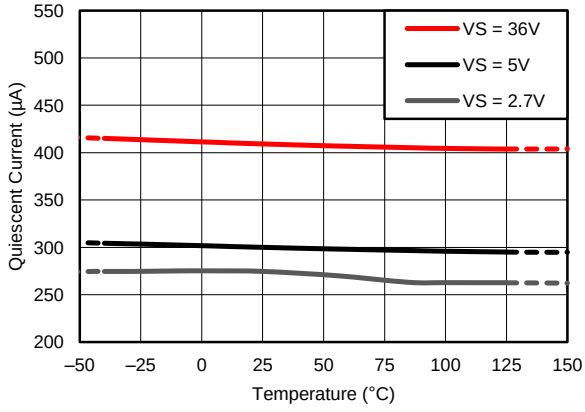


Figure 18. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

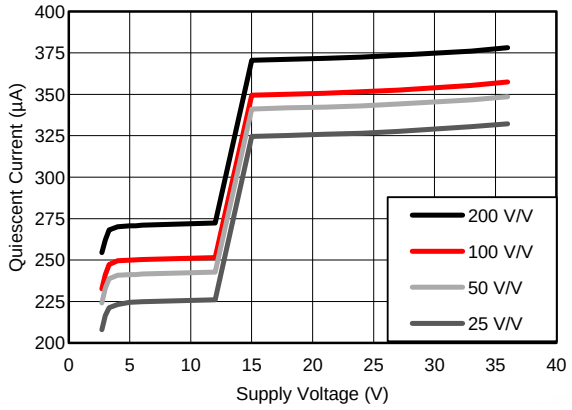
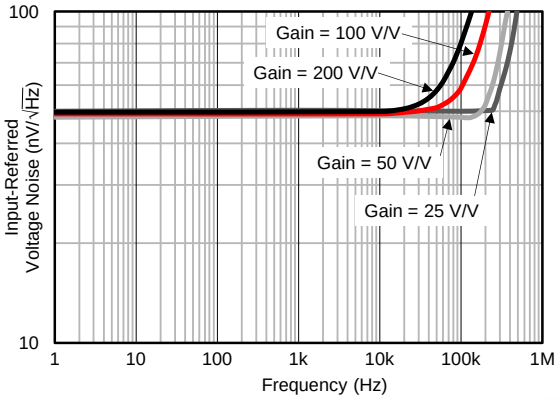
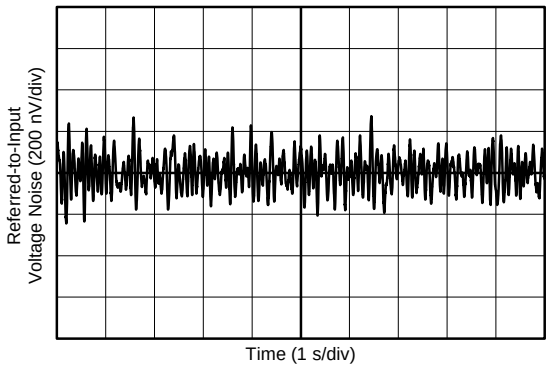


Figure 19. Quiescent Current vs Supply Voltage



V_S = ± 2.5 V V_{REF} = 0 V V_{SENSE} = 0 mV, Shorted

Figure 20. Input-Referred Voltage Noise vs Frequency



V_S = ± 2.5 V V_{CM} = 0 V V_{SENSE} = 0 mV, Shorted

Figure 21. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

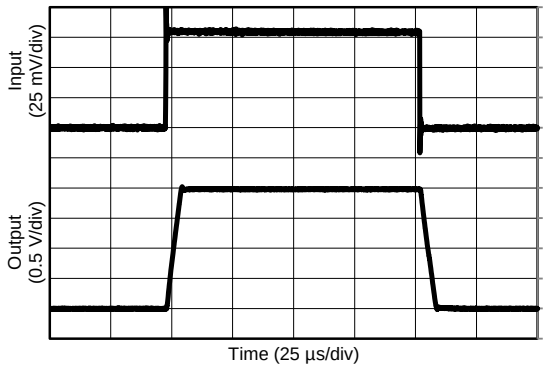


Figure 22. Step Response (Gain = 25 V/V, 2-V_{PP} Output Step)

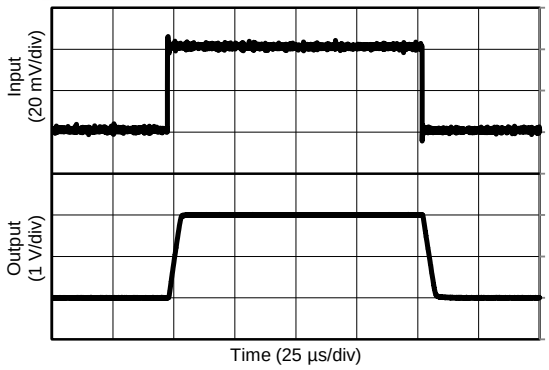


Figure 23. Step Response (Gain = 50 V/V, 2-V_{PP} Output Step)

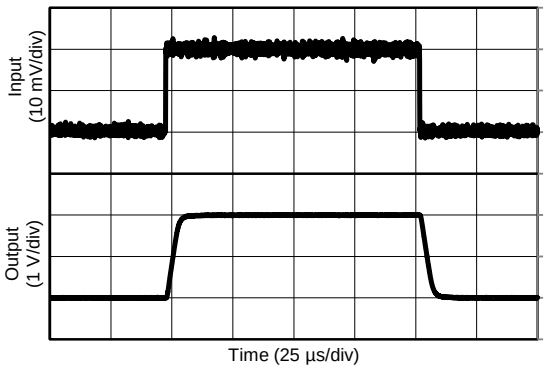


Figure 24. Step Response (Gain = 100 V/V, 2-V_{PP} Output Step)

Typical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

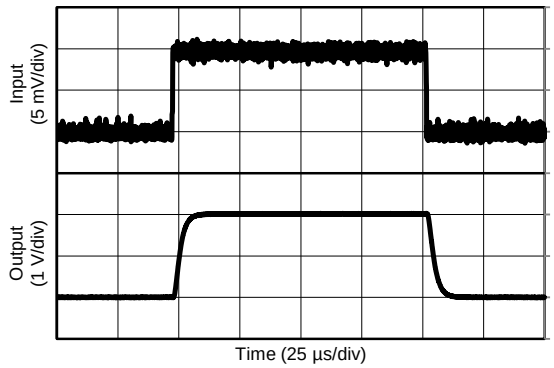
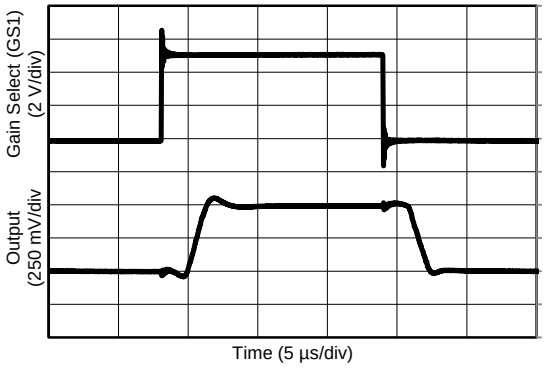
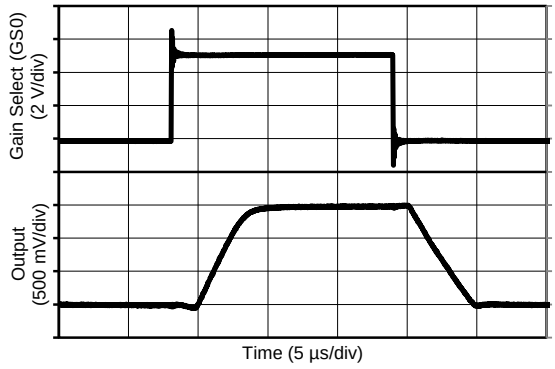


Figure 25. Step Response
(Gain = 200 V/V, 2-V_{PP} Output Step)



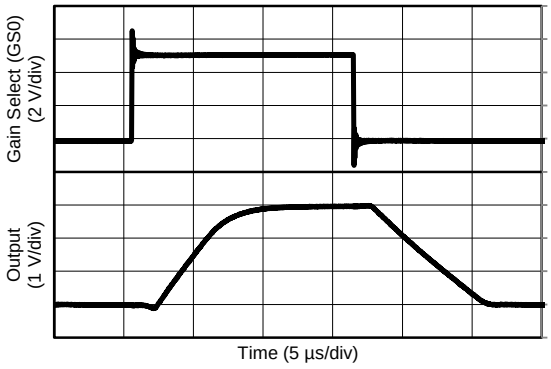
V_{DIFF} = 20 mV
V_{OUT} at 25-V/V Gain = 500 mV
V_{OUT} at 50-V/V Gain = 1 V

Figure 26. Gain Change Output Response
(Gain = 25 V/V to 50 V/V)



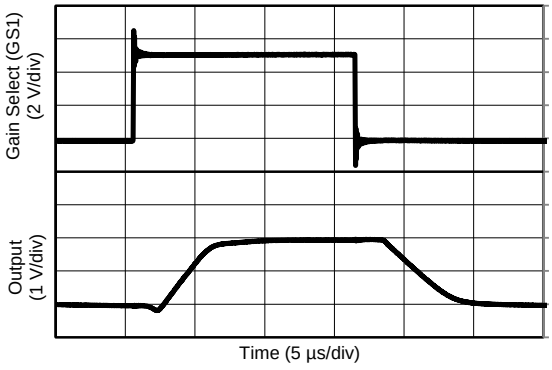
V_{DIFF} = 20 mV
V_{OUT} at 25-V/V Gain = 500 mV
V_{OUT} at 100-V/V Gain = 2 V

Figure 27. Gain Change Output Response
(Gain = 25 V/V to 100 V/V)



V_{DIFF} = 20 mV
V_{OUT} at 50-V/V Gain = 1 V
V_{OUT} at 200-V/V Gain = 4 V

Figure 28. Gain Change Output Response
(Gain = 50 V/V to 200 V/V)



V_{DIFF} = 20 mV
V_{OUT} at 100-V/V Gain = 2 V
V_{OUT} at 200-V/V Gain = 4 V

Figure 29. Gain Change Output Response
(Gain = 100 V/V to 200 V/V)

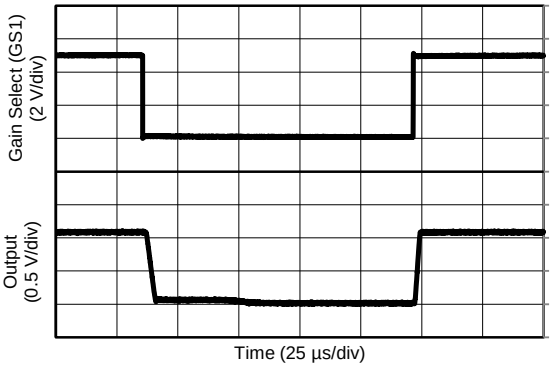


Figure 30. Gain Change Output Response From Saturation
(Gain = 50 V/V to 25 V/V)

Typical Characteristics (continued)

At T_A = +25°C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

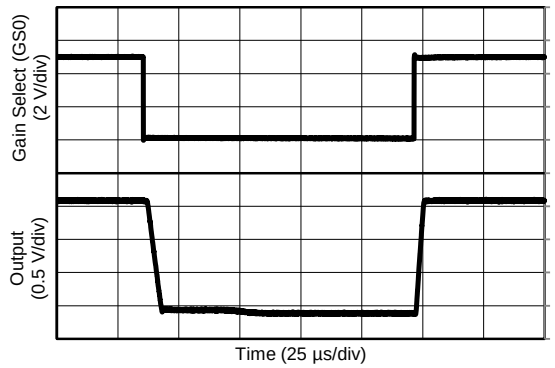


Figure 31. Gain Change Output Response From Saturation (Gain = 100 V/V to 25 V/V)

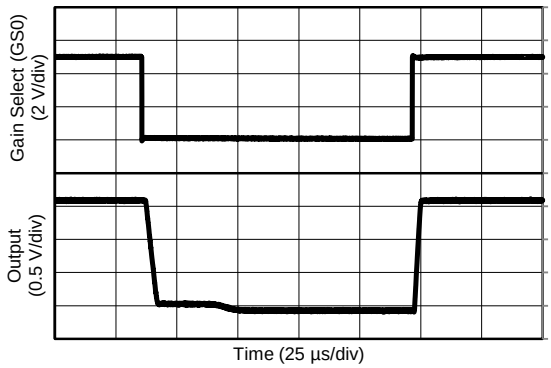


Figure 32. Gain Change Output Response From Saturation (Gain = 200 V/V to 50 V/V)

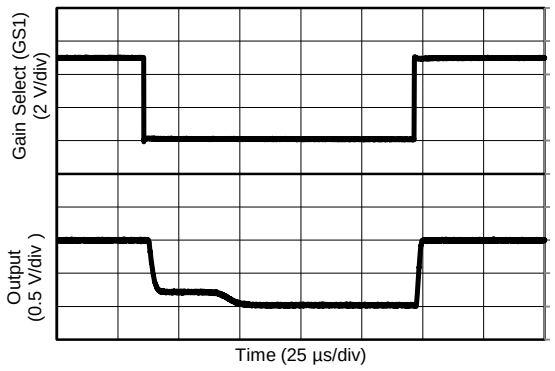


Figure 33. Gain Change Output Response From Saturation (Gain = 200 V/V to 100 V/V)

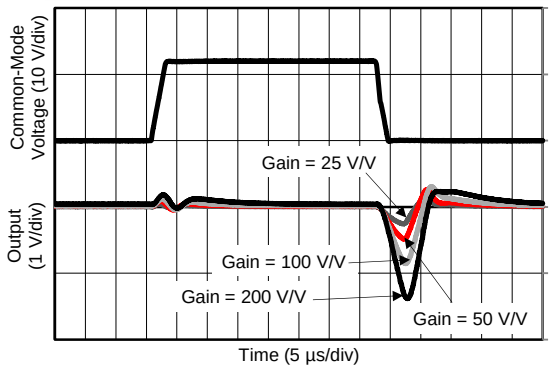


Figure 34. Common-Mode Voltage Transient Response

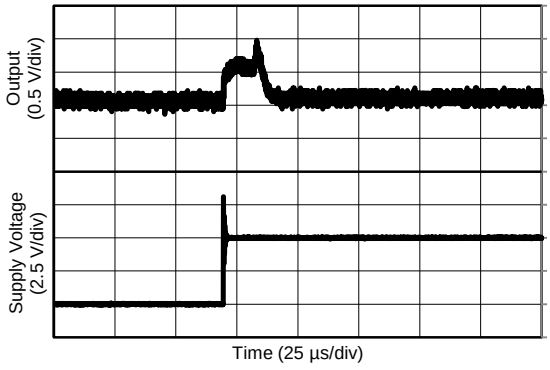


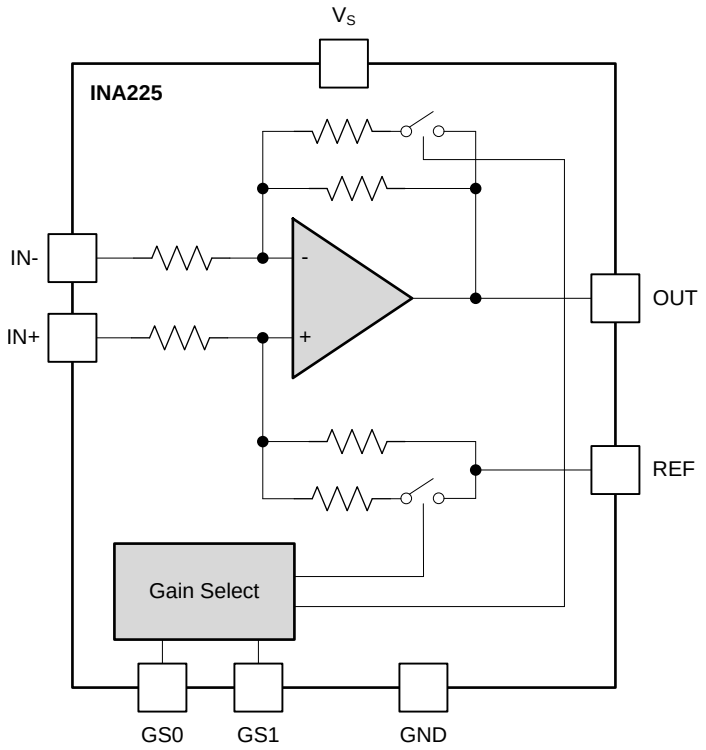
Figure 35. Start-Up Response

7 Detailed Description

7.1 Overview

The INA225 is a 36-V, common-mode, zero-drift topology, current-sensing amplifier. This device features a significantly higher signal bandwidth than most comparable precision, current-sensing amplifiers, reaching up to 125 kHz at a gain of 100 V/V. A very useful feature present in the device is the built-in programmable gain selection. To increase design flexibility with the device, a programmable gain feature is added that allows changing device gain during operation in order to accurately monitor wider dynamic input signal ranges. Four discrete gain levels (25 V/V, 50 V/V, 100 V/V, and 200 V/V) are available in the device and are selected using the two gain-select terminals, GS0 and GS1.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Selecting A Shunt Resistor

The device measures the differential voltage developed across a resistor when current flows through it. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows a wide range of input signals to be measured across this current-sensing resistor.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the resistor. The larger the voltage developed across this resistor the more accurate of a measurement that can be made because of the fixed internal amplifier errors. These fixed internal amplifier errors, which are dominated by the internal offset voltage of the device, result in a larger measurement uncertainty when the input signal gets smaller. When the input signal gets larger, the measurement uncertainty is reduced because the fixed errors become a smaller percentage of the signal being measured.

Feature Description (continued)

A system design trade-off for improving the measurement accuracy through the use of the larger input signals is the increase in the power dissipated across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through it. However, the power that is then dissipated across this component also increases. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreasing input signal. Finding the optimal value for the shunt resistor requires factoring both the accuracy requirement of the application and allowable power dissipation into the selection of the component. An increasing amount of very low ohmic value resistors are becoming available with values reaching down to 200 µΩ with power dissipations of up to 5 W, thus enabling very large currents to be accurately monitored using sensing resistors.

The maximum value for the current-sensing resistor that can be chosen is based on the full-scale current to be measured, the full-scale input range of the circuitry following the device, and the device gain selected. The minimum value for the current-sensing resistor is typically a design-based decision because maximizing the input range of the circuitry following the device is commonly preferred. Full-scale output signals that are significantly less than the full input range of the circuitry following the device output can limit the ability of the system to exercise the full dynamic range of system control based on the current measurement.

7.3.1.1 Selecting A Current-Sense Resistor Example

The example in Table 1 is based on a set of application characteristics, including a 10-A full-scale current range and a 4-V full-scale output requirement. The calculations for selecting a current-sensing resistor of an appropriate value are shown in Table 1.

Table 1. Calculating the Current-Sense Resistor, R_{SENSE}

PARAMETER		EQUATION	RESULT
I_{MAX}	Full-scale current		10 A
V_{OUT}	Full-scale output voltage		4 V
Gain	Gain selected	Initial selection based on default gain setting.	25 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{Diff} = V_{OUT} / Gain$	160 mV
R_{SHUNT}	Shunt resistor value	$R_{SHUNT} = V_{Diff} / I_{MAX}$	16 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	1.6 W
V_{OS} Error	Offset voltage error	$(V_{OS} / V_{DIFF}) \times 100$	0.094%

7.3.1.2 Optimizing Power Dissipation versus Measurement Accuracy

The example shown in Table 1 results in a maximum current-sensing resistor value of 16 mΩ to develop the 160 mV required to achieve the 4-V full-scale output with the gain set to 25 V/V. The power dissipated across this 16-mΩ resistor at the 10-A current level is 1.6 W, which is a fairly high power dissipation for this component. Adjusting the device gain allows alternate current-sense resistor values to be selected to ease the power dissipation requirement of this component.

Changing the gain setting from 25 V/V to 100 V/V, as shown in Table 2, decreases the maximum differential input voltage from 160 mV down to 40 mV, thus requiring only a 4-mΩ current-sensing resistor to achieve the 4-V output at the 10-A current level. The power dissipated across this resistor at the 10-A current level is 400 mW, significantly increasing the availability of component options to select from.

The increase in gain by a factor of four reduces the power dissipation requirement of the current-sensing resistor by this same factor of four. However, with this smaller full-scale signal, the measurement uncertainty resulting from the device fixed input offset voltage increases by the same factor of four. The measurement error resulting from the device input offset voltage is approximately 0.1% at the 160-mV full-scale input signal for the 25-V/V gain setting. Increasing the gain to 100 V/V and decreasing the full-scale input signal to 40 mV increases the offset induced measurement error to 0.38%.

Table 2. Accuracy and R_{SENSE} Power Dissipation vs Gain Setting

PARAMETER		EQUATION	RESULT
I_{MAX}	Full-scale current		10 A
V_{OUT}	Full-scale output voltage		4 V
Gain	Gain selected		100 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{Diff} = V_{OUT} / Gain$	40 mV
R_{SENSE}	Current-sense resistor value	$R_{SENSE} = V_{Diff} / I_{MAX}$	4 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	0.4 W
V_{OS} Error	Offset voltage error	$(V_{OS} / V_{DIFF}) \times 100$	0.375%

7.3.2 Programmable Gain Select

The device features a terminal-controlled gain selection in determining the device gain setting. Four discrete gain options are available (25 V/V, 50 V/V, 100 V/V, and 200 V/V) on the device and are selected based on the voltage levels applied to the gain-select terminals (GS0 and GS1). These terminals are typically fixed settings for most applications but the programmable gain feature can be used to adjust the gain setting to enable wider dynamic input range monitoring as well as to create an automatic gain control (AGC) network.

Table 3 shows the corresponding gain values and gain-select terminal values for the device.

Table 3. Gain Select Settings

GAIN	GS0	GS1
25 V/V	GND	GND
50 V/V	GND	V_S
100 V/V	V_S	GND
200 V/V	V_S	V_S

7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the device output; however, this location negates the advantage of the low output impedance of the internal buffer. The input then represents the best location for implementing external filtering. Figure 36 shows the typical implementation of the input filter for the device.

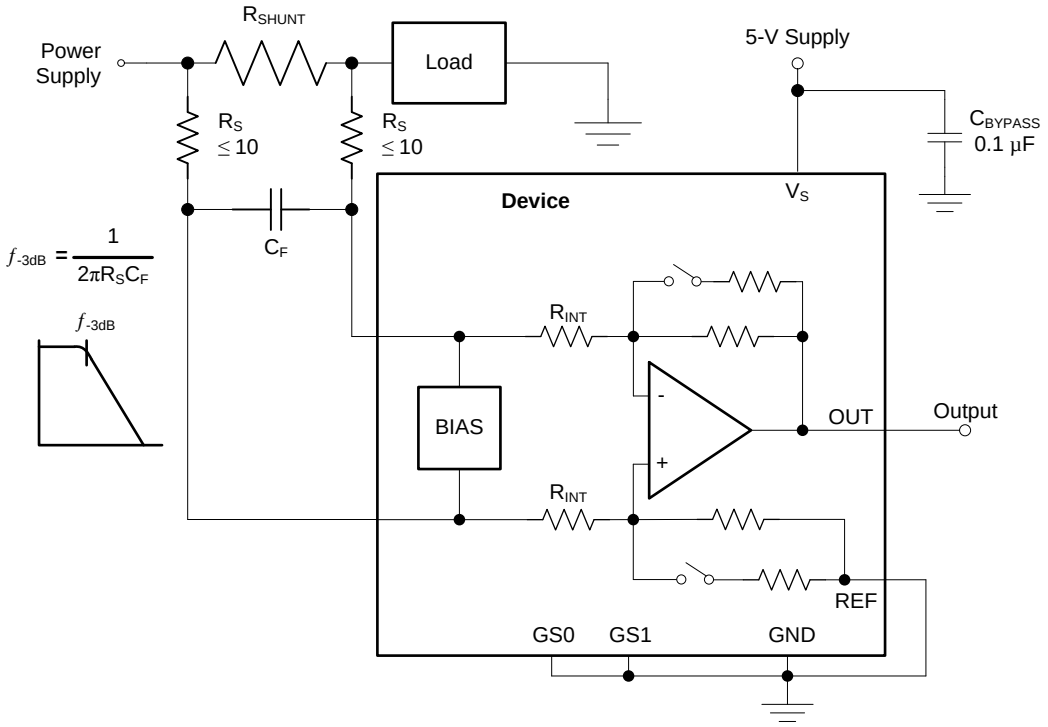


Figure 36. Input Filter

Care must be taken in the selection of the external filter component values because these components can affect device measurement accuracy. Placing external resistance in series with the input terminals creates an additional error so these resistors should be kept as low of a value as possible with a recommended maximum value of 10 Ω or less. Increasing the value of the input filter resistance beyond 10 Ω results in a smaller voltage signal present at the device input terminals than what is developed across the current-sense shunt resistor.

The internal bias network shown in Figure 36 creates a mismatch in the two input bias current paths when a differential voltage is applied between the input terminals. Under normal conditions, where no external resistance is added to the input paths, this mismatch of input bias currents has little effect on device operation or accuracy. However, when additional external resistance is added (such as for input filtering), the mismatch of input bias currents creates unequal voltage drops across these external components. The mismatched voltages result in a signal reaching the input terminals that is lower in value than the signal developed directly across the current-sensing resistor.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value (R_S) and the internal input resistors (R_{INT}). The reduction of the shunt voltage reaching the device input terminals appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance.

Device Functional Modes (continued)

The amount of error these external filter resistors introduce into the measurement can be calculated using the simplified gain error factor in Equation 1, where the gain error factor is calculated with Equation 2.

$$\text{Gain Error Factor} = \frac{50{,}000}{(41 \times R_S) + 50{,}000} \quad (1)$$

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (2)$$

where:

- R_{INT} is the internal input impedance, and
- R_S is the external series resistance.

For example, using the gain error factor (Equation 1), a 10-Ω series resistance results in a gain error factor of 0.992. The corresponding gain error is then calculated using Equation 3, resulting in a gain error of approximately 0.81% solely because of the external 10-Ω series resistors. Using 100-Ω filter resistors increases this gain error to approximately 7.58% from these resistors alone.

$$\text{Gain Error (\%)} = 1 - \text{Gain Error Factor} \quad (3)$$

7.4.2 Shutting Down the Device

Although the device does not have a shutdown terminal, the low-power consumption allows for the device to be powered from the output of a logic gate or transistor switch that can turn on and turn off the voltage connected to the device power-supply terminal.

However, in current-shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the device simplified schematic in shutdown mode, as shown in Figure 37.

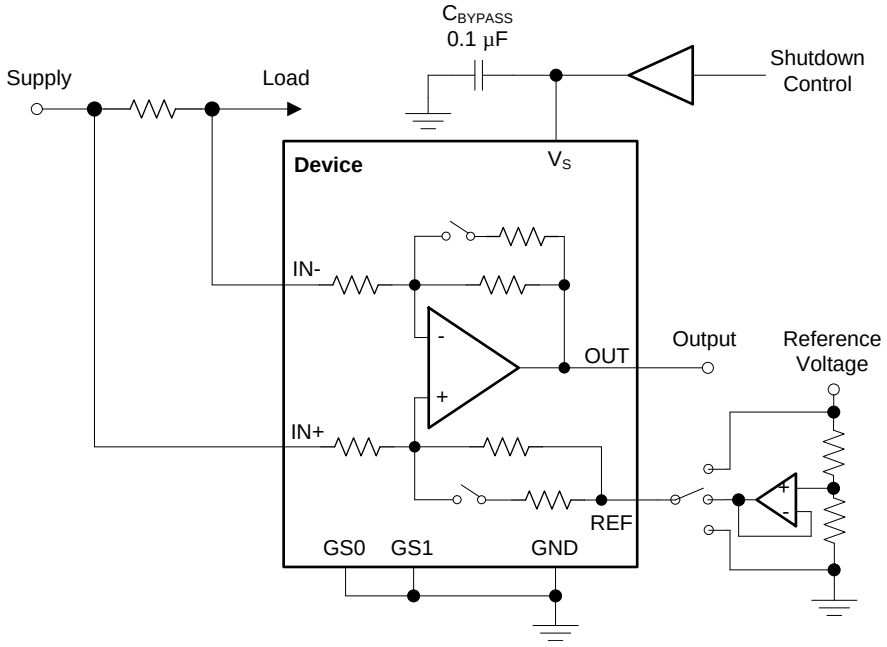


Figure 37. Shutting Down the Device

Device Functional Modes (continued)

Note that there is typically a 525-kΩ impedance (from the combination of the 500-kΩ feedback and 25-kΩ input resistors) from each device input to the REF terminal. The amount of current flowing through these terminals depends on the respective configuration. For example, if the REF terminal is grounded, calculating the effect of the 525-kΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the device is shut down, the calculation is direct. Instead of assuming 525 kΩ to ground, assume 525 kΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves similar to an open circuit when un-powered, little or no current flows through the 525-kΩ path.

7.4.3 Using the Device with Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V (such as automotive applications). Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in Figure 38, as a working impedance for the zener. Keeping these resistors as small as possible is preferable, most often around 10 Ω. This value limits the impact on accuracy with the addition of these external components, as described in the *Input Filtering* section. Larger values can be used if necessary with the result having an impact on gain error. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

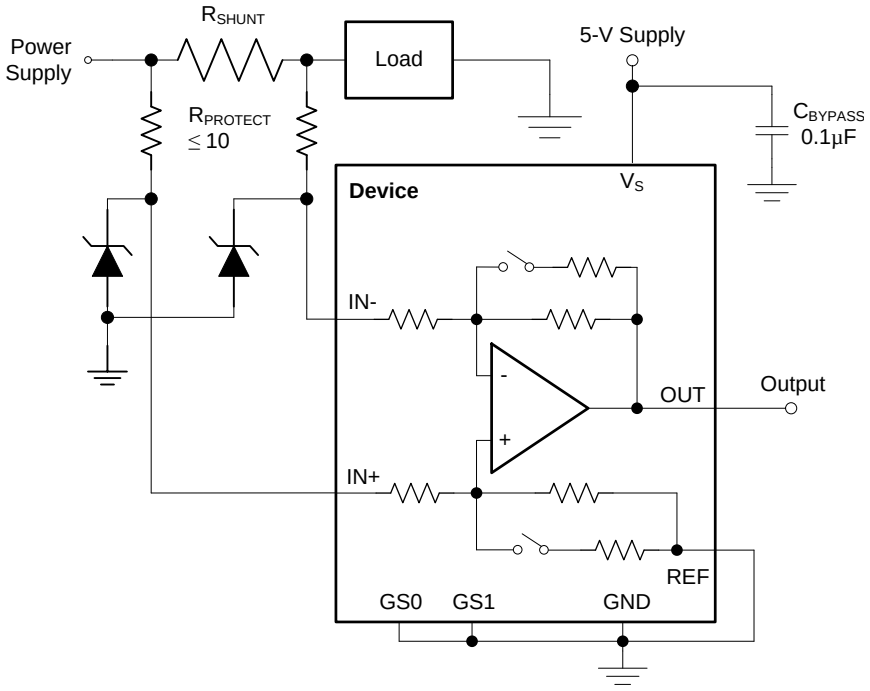


Figure 38. Device Transient Protection

8 Applications and Implementation

8.1 Application Information

The INA225 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference terminal to adjust the functionality of the output signal offers multiple configurations discussed throughout this section.

8.2 Typical Applications

8.2.1 Microcontroller-Configured Gain Selection

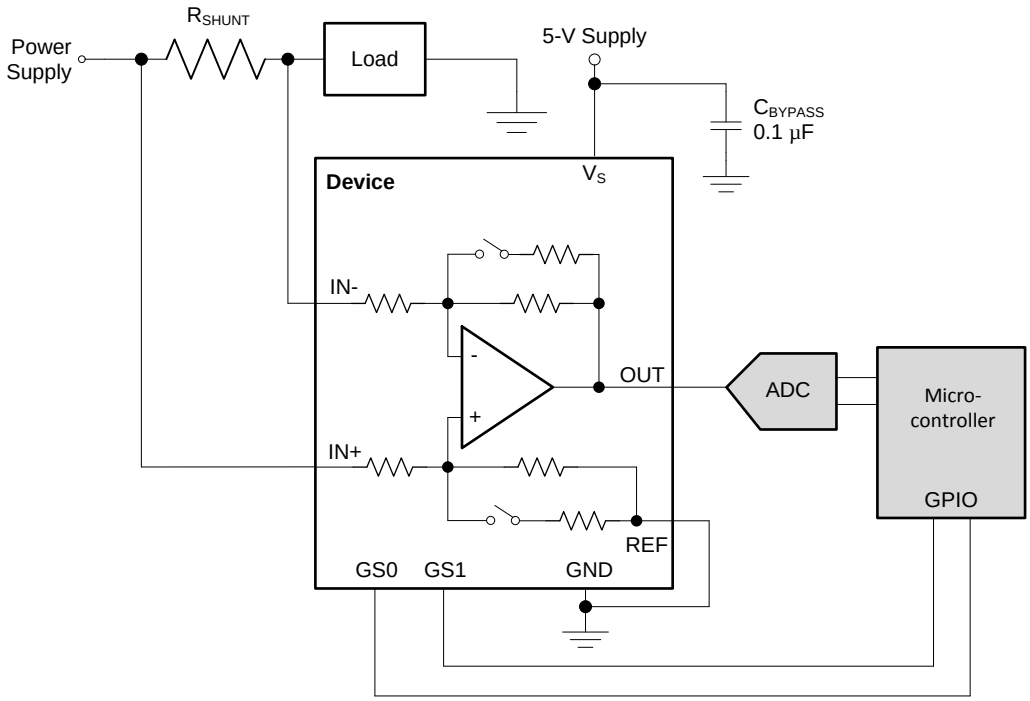


Figure 39. Microcontroller-Configured Gain Selection Schematic

8.2.1.1 Design Requirements

Figure 39 shows the typical implementation of the device interfacing with an analog-to-digital converter (ADC) and microcontroller.

8.2.1.2 Detailed Design Procedure

In this application, the device gain setting is selected and controlled by the microcontroller to ensure the device output is within the linear input range of the ADC. Because the output range of the device under a specific gain setting approaches the linear output range of the INA225 itself or the linear input range of the ADC, the microcontroller can adjust the device gain setting to ensure the signal remains within both the device and the ADC linear signal range.

Typical Applications (continued)

8.2.1.3 Application Curve

Figure 40 illustrates how the microcontroller can monitor the ADC measurements to determine if the device gain setting should be adjusted to ensure the output of the device remains within the linear output range as well as the linear input range of the ADC. When the output of the device rises to a level near the desired maximum voltage level, the microcontroller can change the GPIO settings connected to the G0 and G1 gain-select terminals to adjust the device gain setting, thus resulting in the output voltage dropping to a lower output range. When the input current increases, the output voltage increases again to the desired maximum voltage level. The microcontroller can again change the device gain setting to drop the output voltage back to a lower range.

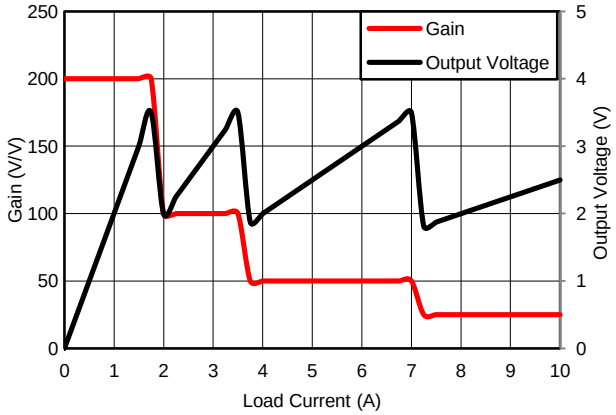


Figure 40. Microcontroller-Configured Gain Selection Response

Typical Applications (continued)

8.2.2 Unidirectional Operation

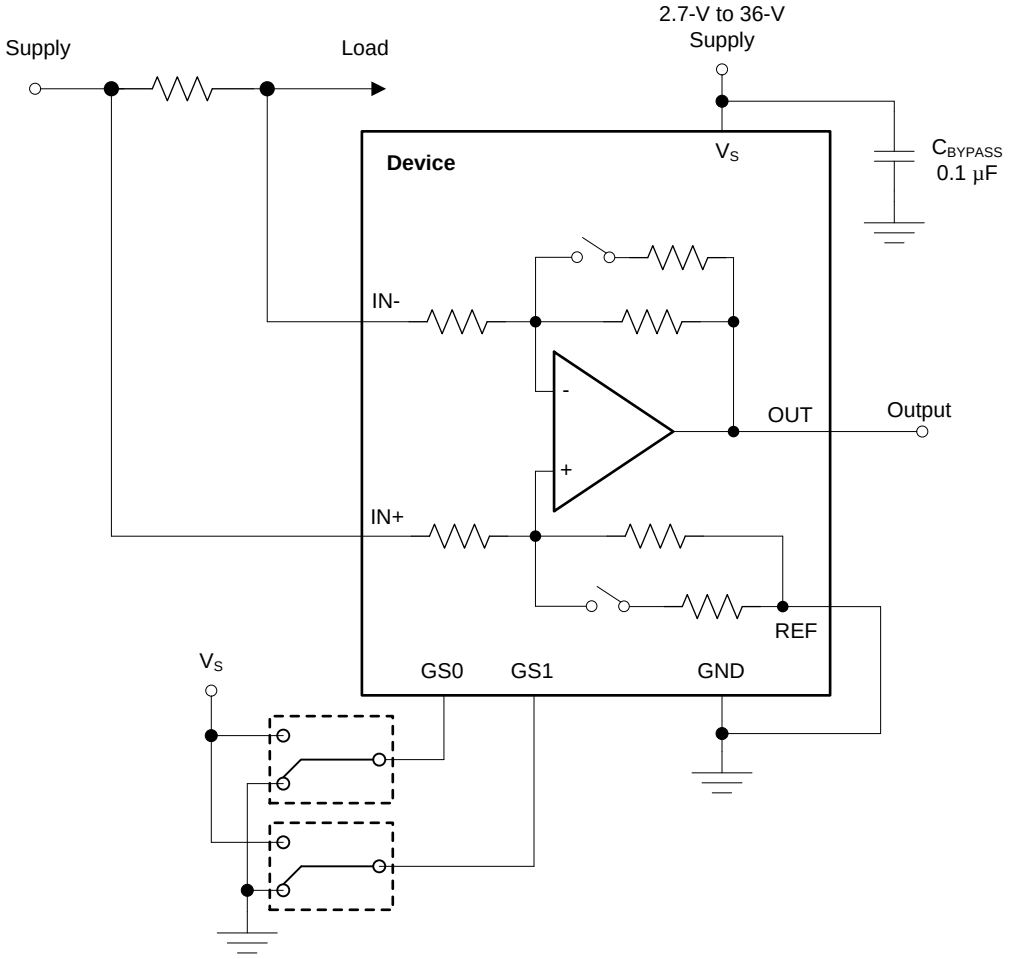


Figure 41. Unidirectional Application Schematic

8.2.2.1 Design Requirements

The device can be configured to monitor current flowing in one direction or in both directions, depending on how the REF terminal is configured. For measuring current in one direction, only the REF terminal is typically connected to ground as shown in Figure 41. With the REF terminal connected to ground, the output is low with no differential input signal applied. When the input signal increases, the output voltage at the OUT terminal increases above ground based on the device gain setting.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. Resulting from an internal node limitation when the REF terminal is grounded (unidirectional configuration) the device gain setting determines how close to ground the device output voltage can achieve when no signal is applied; see Figure 14. To overcome this internal node limitation, a small reference voltage (approximately 10 mV) can be applied to the REF terminal to bias the output voltage above this voltage level. The device output swing capability returns to the 10-mV saturation level with this small reference voltage present.

At the lowest gain setting, 25 V/V, the device is capable of accurately measuring input signals that result in output voltages below this 10-mV saturation level of the output stage. For these gain settings, a reference voltage can be applied to bias the output voltage above this lower saturation level to allow the device to monitor these smaller input signals. To avoid common-mode rejection errors, buffer the reference voltage connected to the REF terminal.

A less frequently-used output biasing method is to connect the REF terminal to the supply voltage, V_S. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF terminal is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– terminal. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF terminal must not exceed the device supply voltage.

8.2.2.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 42. With the REF terminal connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

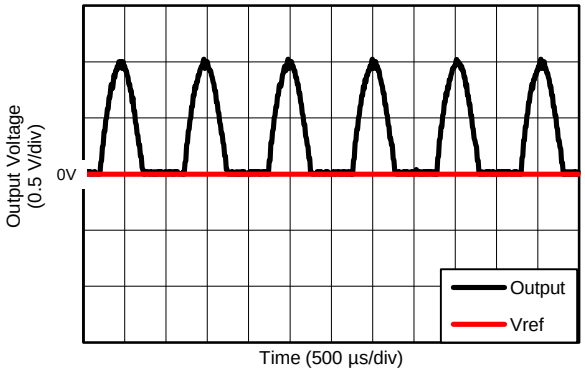


Figure 42. Unidirectional Application Output Response

Typical Applications (continued)

8.2.3 Bidirectional Operation

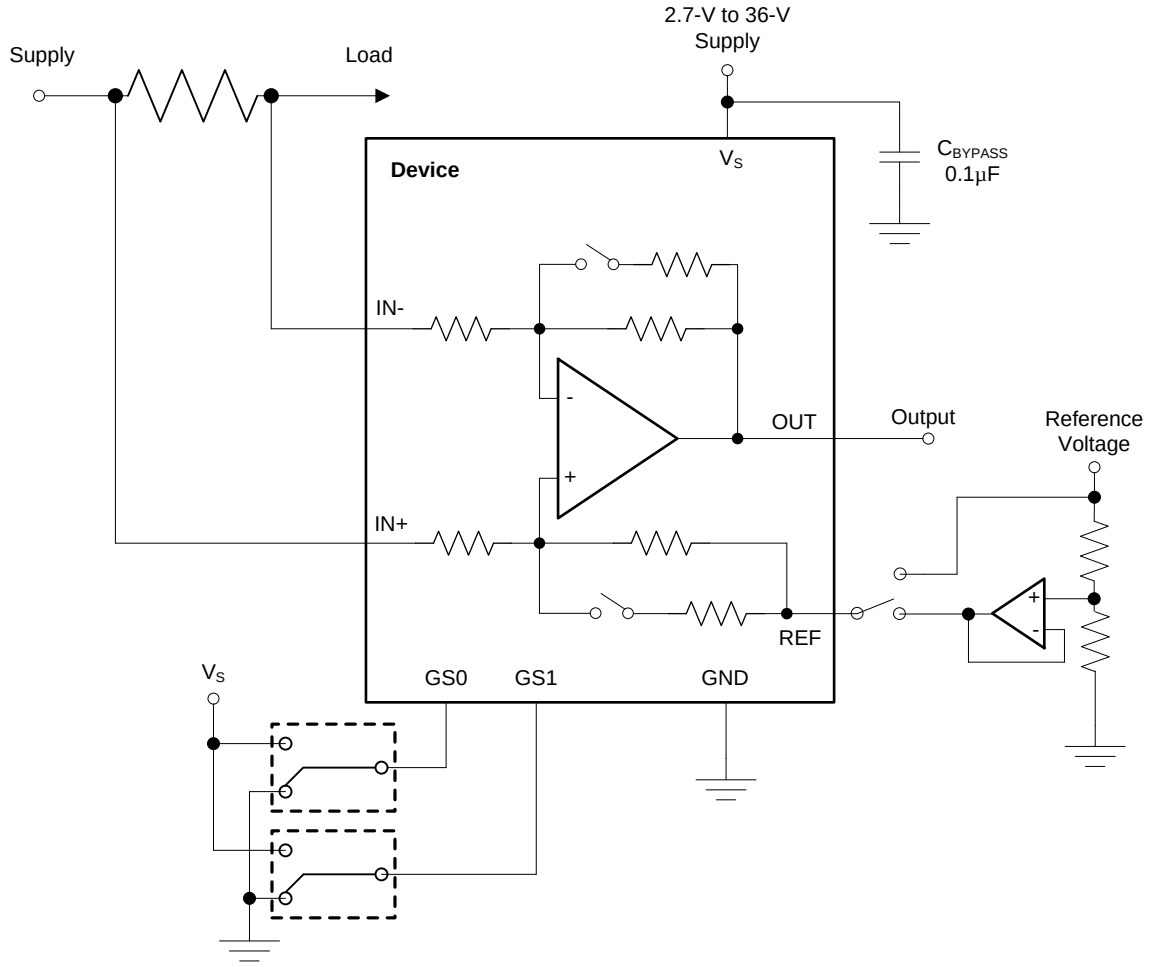


Figure 43. Bidirectional Application Schematic

8.2.3.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

8.2.3.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF terminal, as shown in Figure 43. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– terminal) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF terminal can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at mid-scale for equal range in both directions. In some cases, however, V_{REF} is set at a voltage other than half-scale when the bidirectional current is non-symmetrical.

Typical Applications (continued)

8.2.3.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 44. With the REF terminal connected to a reference voltage, 2.5 V in this case, the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

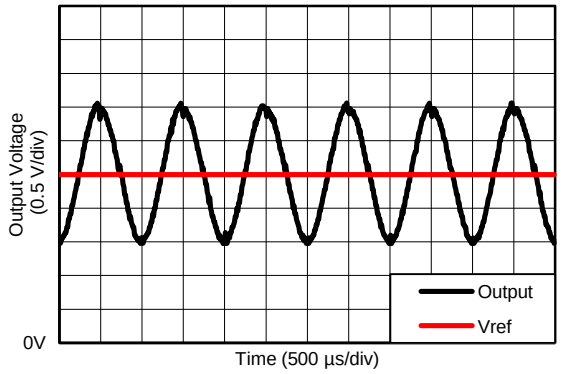


Figure 44. Bidirectional Application Output Response

9 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as +36 V. Note also that the device can withstand the full –0.3-V to +36-V range at the input terminals, regardless of whether the device has power applied or not.

Power-supply bypass capacitors are required for stability and should be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

- Connect the input terminals to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input terminals. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input terminals. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

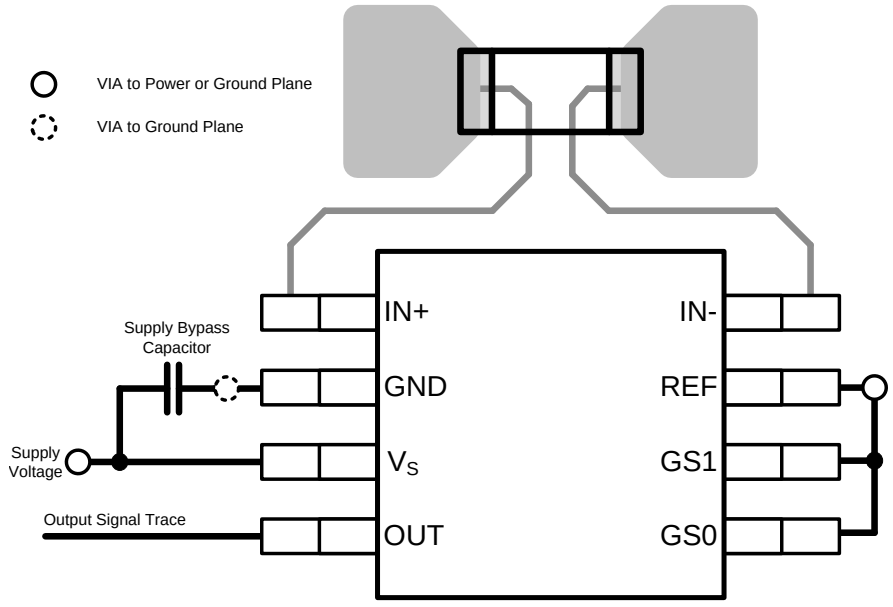


Figure 45. Recommended Layout

NOTE

The layout shown has REF connected to ground for unidirectional operation. Gain-select terminals (GS0 and GS1) are also connected to ground, indicating a 25-V/V gain setting.

11 Device and Documentation Support

11.1 Related Documentation

For related documentation see the following:

- INA225EVM User's Guide, SBOU140

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA225AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	B32	Samples
INA225AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	B32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA225 :

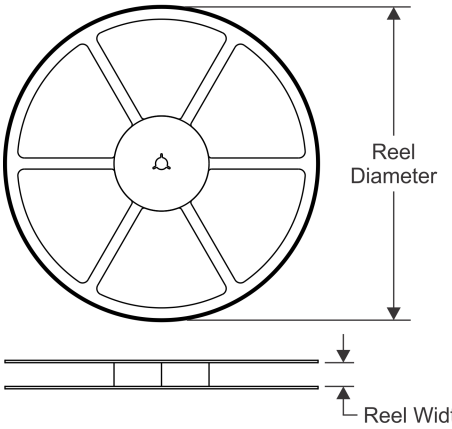
- Automotive : INA225-Q1

NOTE: Qualified Version Definitions:

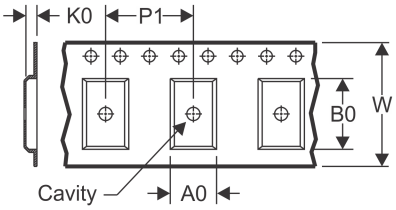
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

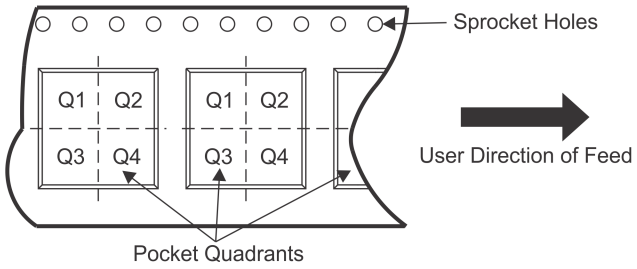


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

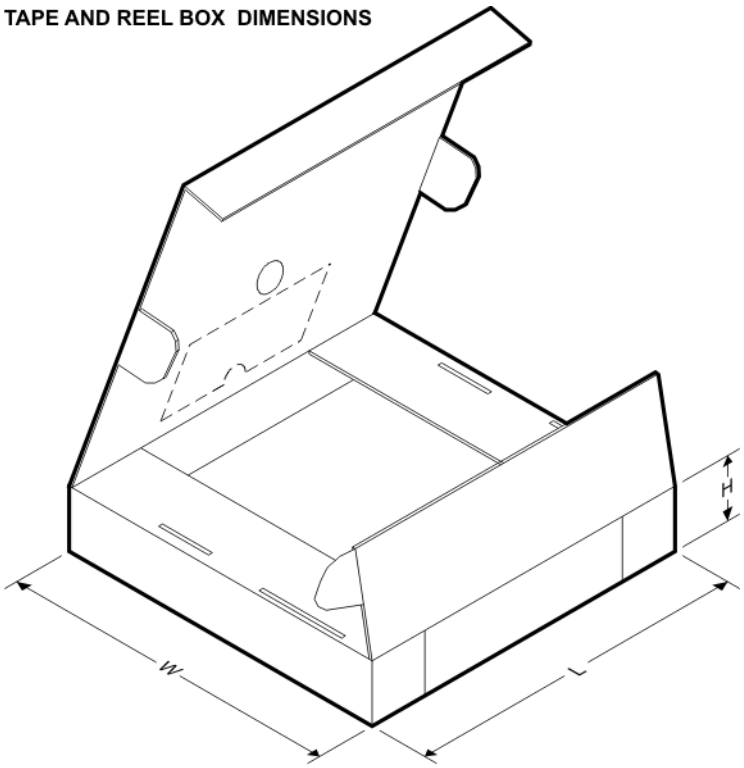
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA225AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA225AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA225AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA225AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

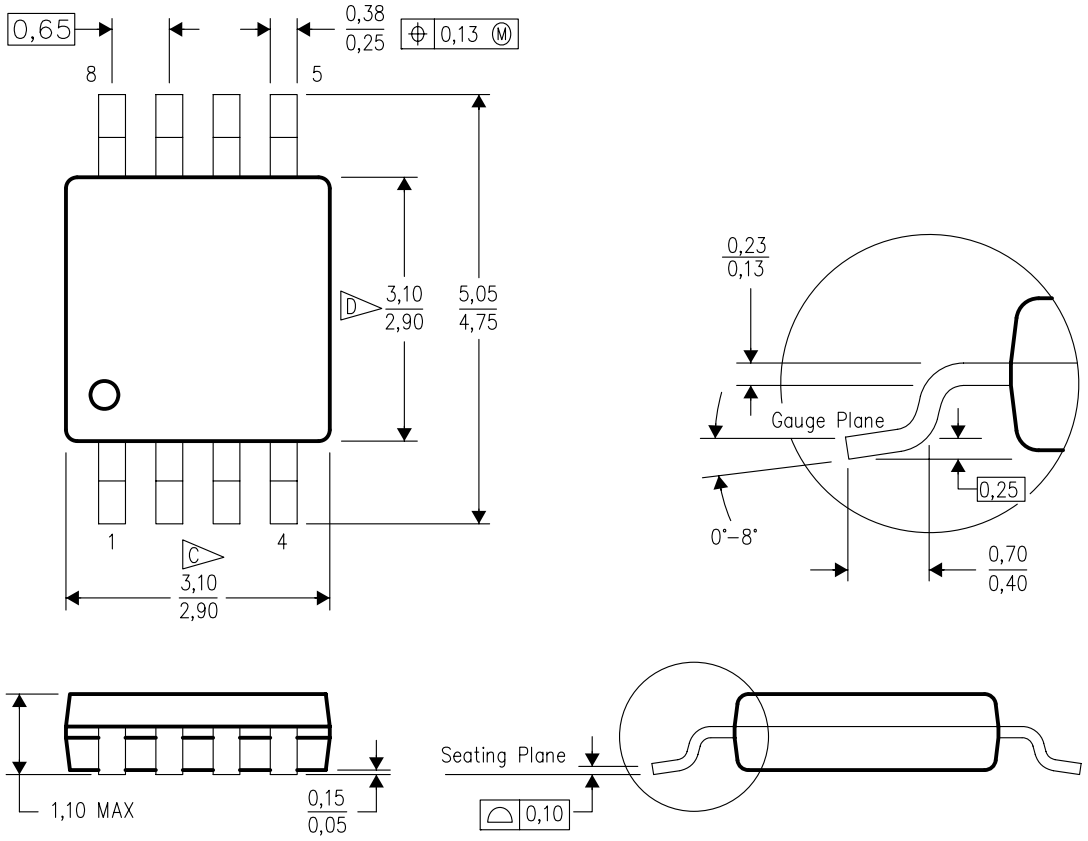
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA225AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA225AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA225AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA225AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

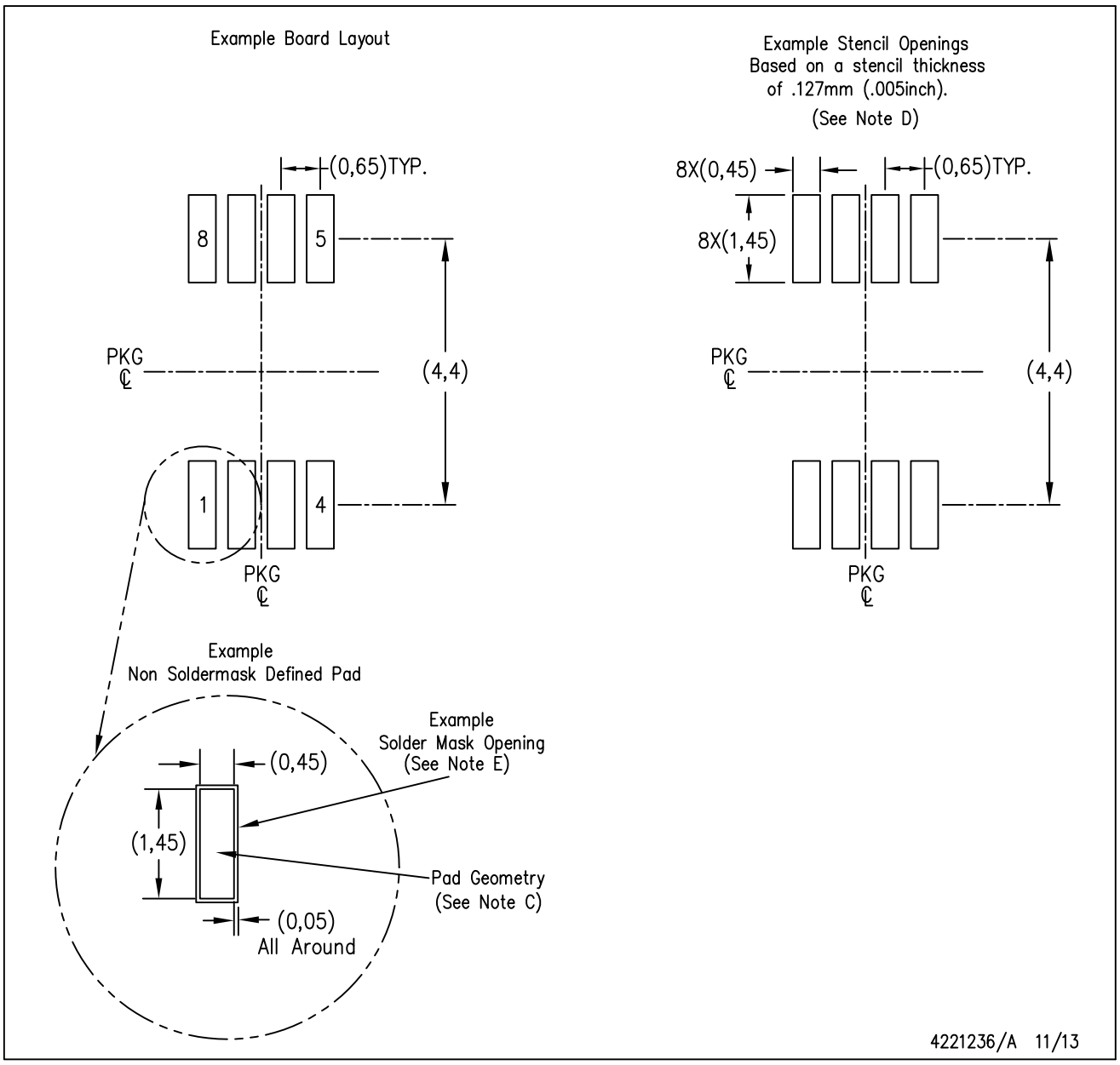
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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