80C51 MICROCONTROLLER FAMILY

Introduction

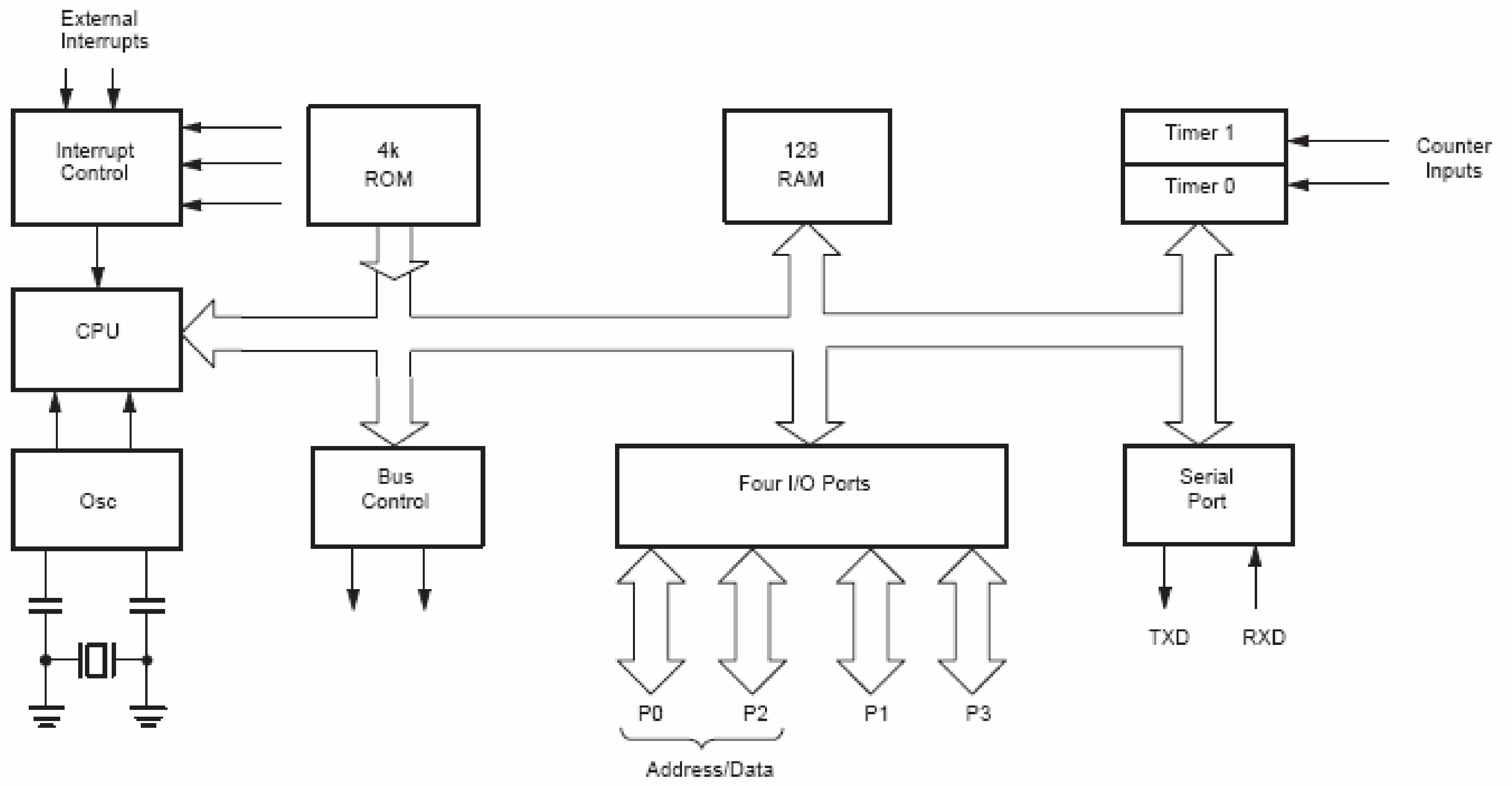
Microcontrollers are embedding all circuits needed by any general-use computer:

- Boolean processor
- memory
- counters/timers
- Interrupt system
- Input/output system

80C51 FEATURES

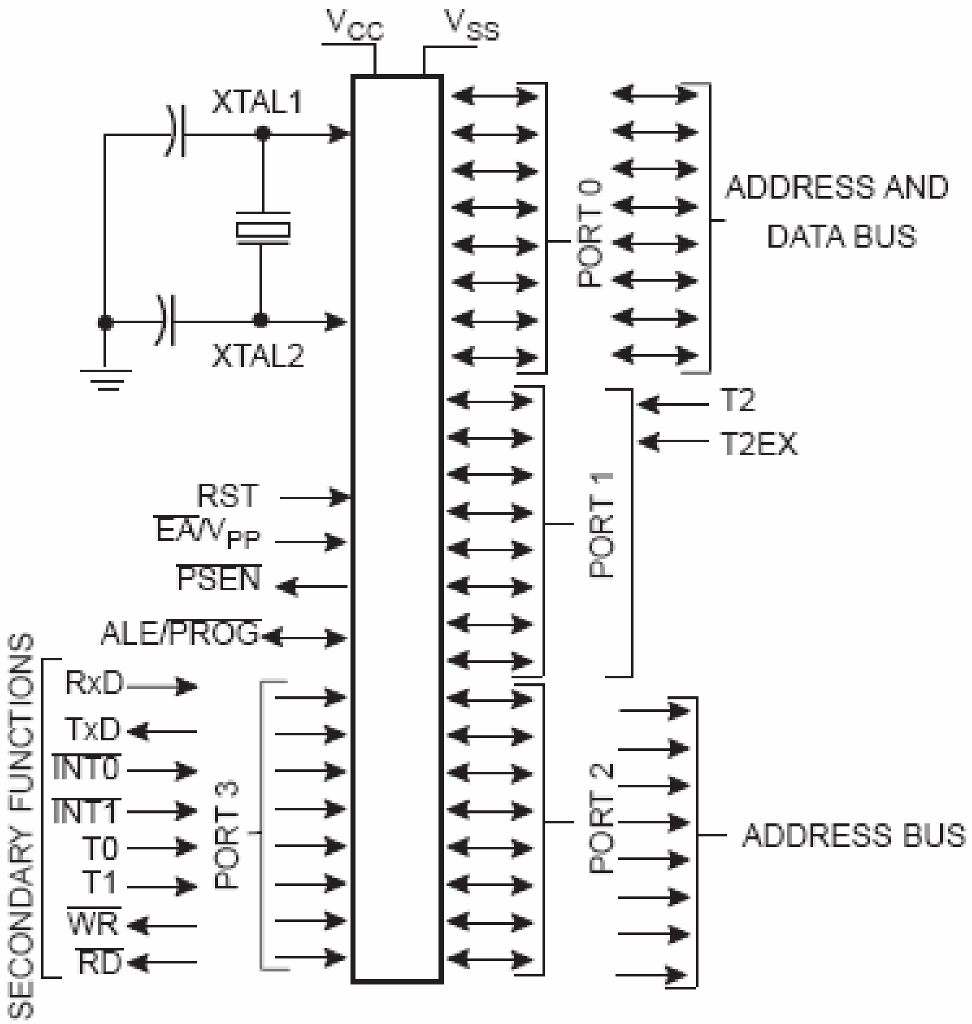
- 8051 Central Processing Unit
  - 4k*8 ROM
  - 128*8 RAM
  - 3*16-bit counter/timers
  - Boolean processor
- External memory addressing capability
  - 64k*8 ROM (program)
  - 64k*8 RAM (data)
- 6 interrupts with 2 level priority
- 4*8-bit I/O ports
- Full–duplex UART
- Asynchronous port reset
- Data, address and control buses

BLOCK DIAGRAM



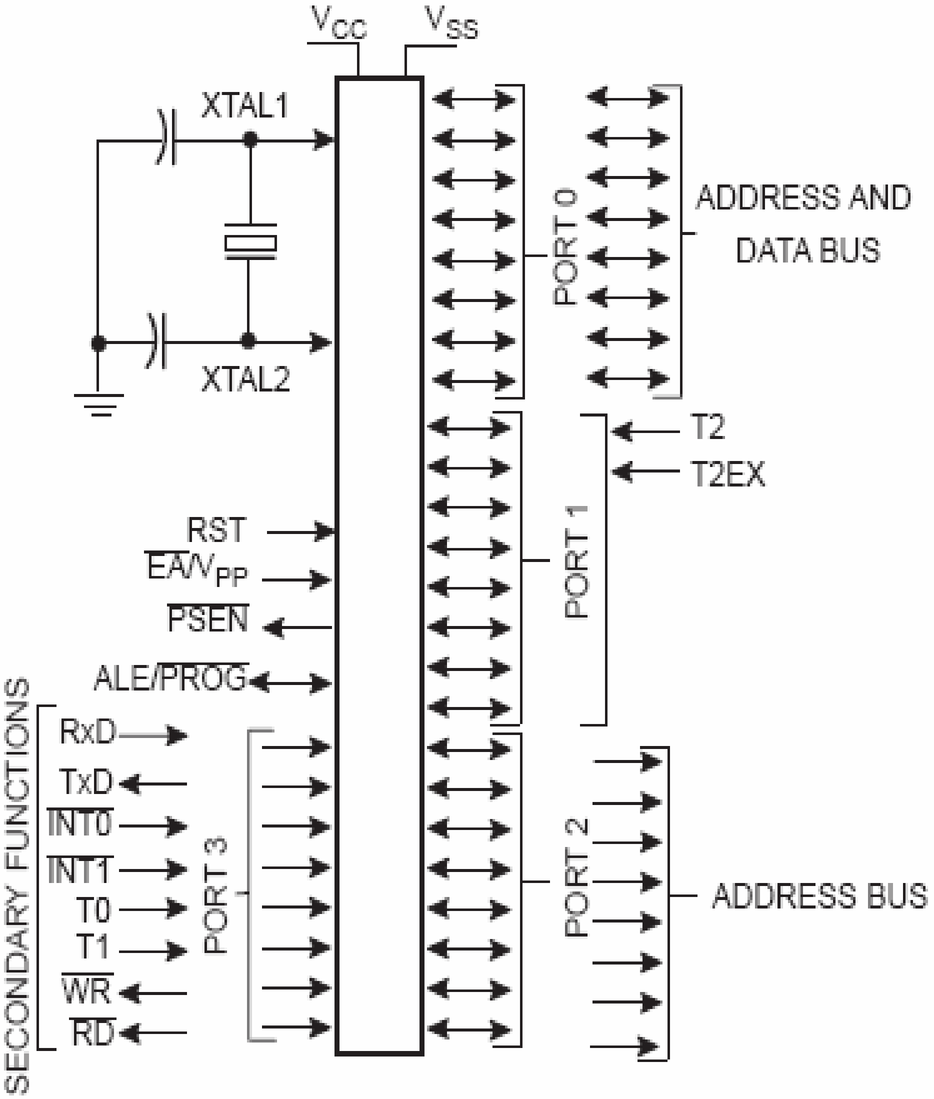
LOGIC SYMBOL AND PIN DESCRIPTION

- **V_{SS}, I**nput**, Ground:** 0 V reference
- **V_{CC}, I, Power Supply:** Power supply voltage
- **P0.0–0.7, I/O, Port 0:** Can have the function of 8-bit open-drain bidirectional port with Schmitt trigger inputs. Pins that have 1s written to them are floating and can be used as high-impedance inputs. Can have the function of multiplexed low-order address and data bus during accesses to external program and data memory using internal pull-ups.

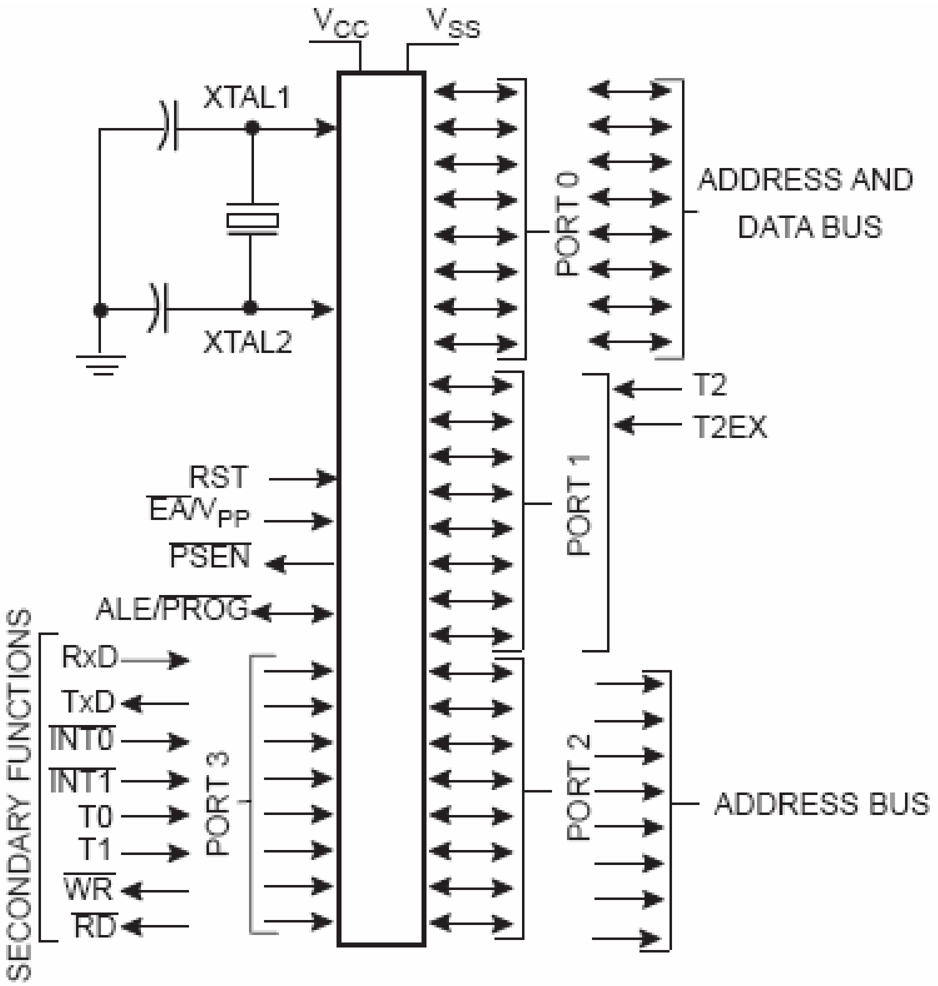


- **P1.0–P1.7, I/O, Port 1:** Can have the function of 8-bit bidirectional port with internal pull-ups and Schmitt trigger inputs. Pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. Also, two pins can have alternate functions. **T2, I/O, (P1.0):** Timer/Counter 2. **T2EX, I, (P1.1):** Timer/Counter 2 with capture function.

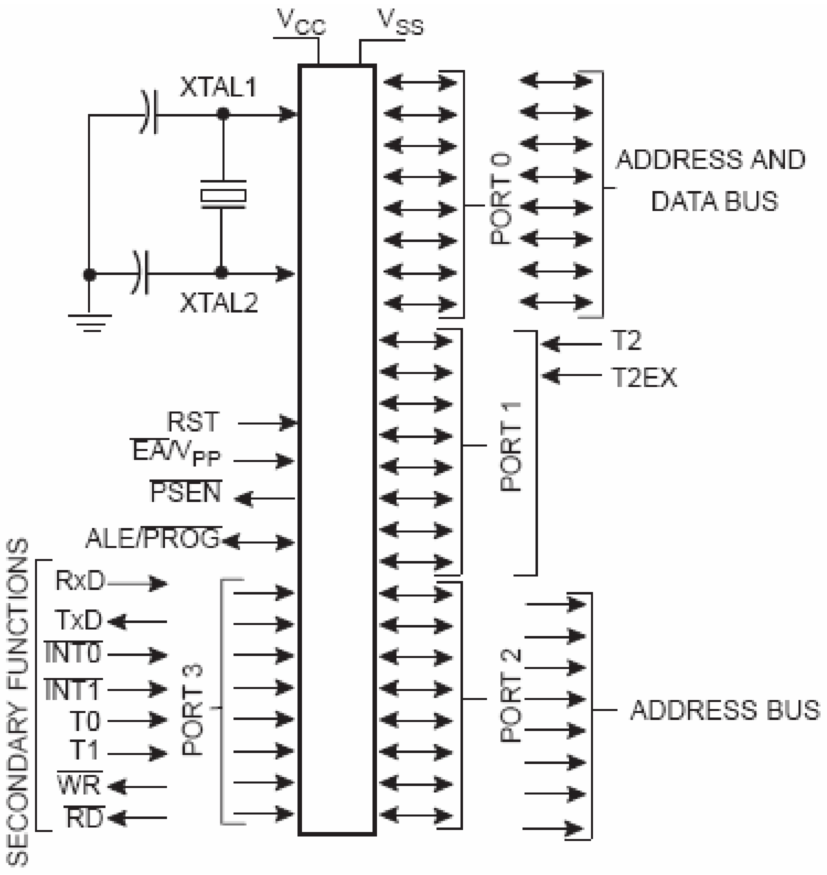
- **P2.0–P2.7, I/O, Port 2:** Can have the function of 8-bit bidirectional port with internal pull-ups and Schmitt trigger inputs. Pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As alternate function, generates the high-order address byte during accesses to external program and data memory.
- **P3.0–P3.7, I/O, Port 3:** Can have the function of 8-bit bidirectional port with internal pull-ups and Schmitt trigger inputs. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. Also, each pin can have alternate function. **RxD, I, (P3.0):** Serial input port. **TxD, O, (P3.1):** Serial output port. **INT0\, I, (P3.2):** External interrupt. **INT1\, I, (P3.3):** External interrupt. **T0, I, (P3.4):** Timer 0 external input. **T1, I, (P3.5):** Timer 1 external input. **WR\, O, (P3.6):** External data memory write strobe. **RD\, O, (P3.7):** External data memory read strobe

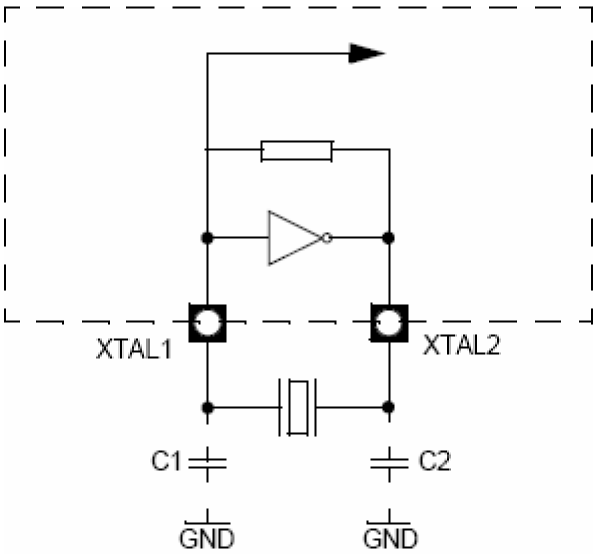


- **RST, I, Reset:** A high on this pin resets the microcontroller.
- **ALE/PROG\, I/O, Address Latch Enable/Program Pulse:** ALE output pulse is used for latching the low byte of the address during an access to external memory. PROG pin is the program pulse input during EPROM programming.
- **PSEN, O, Program Store Enable:** External program memory read strobe.



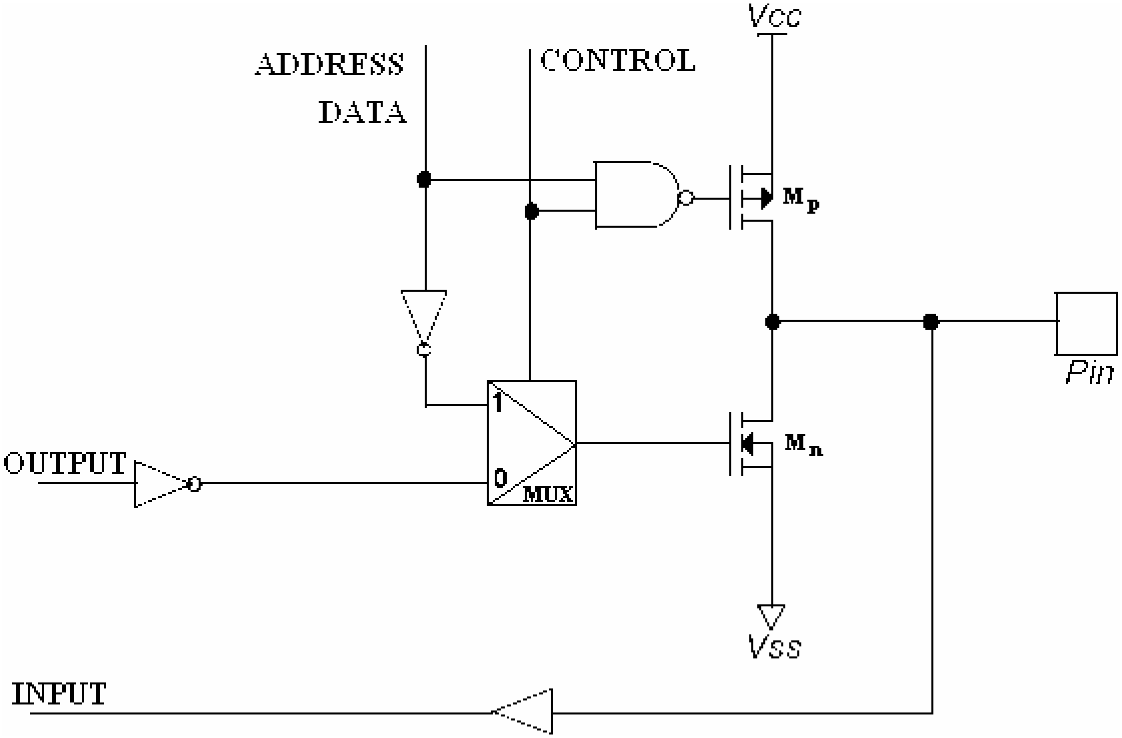
- **EA\ / V_{PP}, I, External Access Enable/Programming Supply Voltage:** If EA\ is externally held low, the microcontroller executes the entire code from external program memory. If EA\ is externally held high, the microcontroller executes the code located at memory locations 0000H to 0FFFH from the internal ROM. V_{PP} pin receives the programming supply voltage during EPROM programming.
- **XTAL1, I, Crystal 1:** Input to the inverting oscillator amplifier and clock generator circuit.
- **XTAL2, O, Crystal 2:** Output from the inverting oscillator amplifier.





Port 0 layout

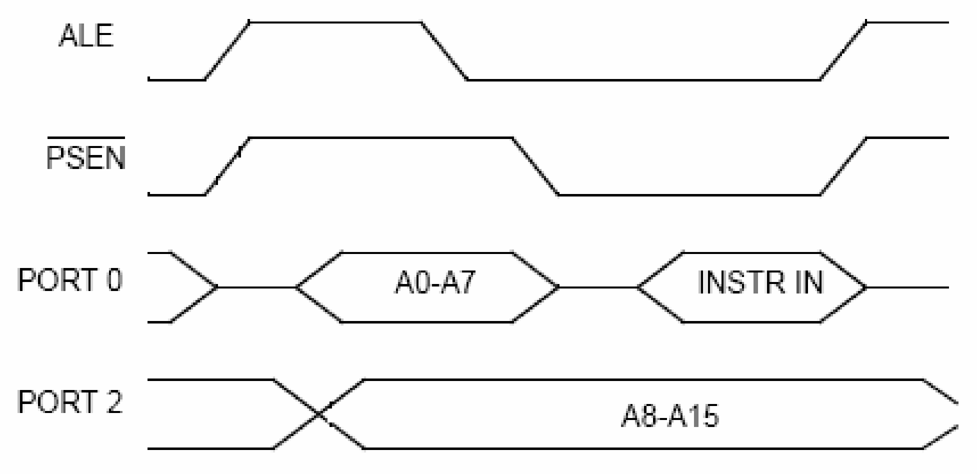
If CONTROL=1, P0 is used for address and data bus using internal pull-ups. The output of the NAND gate isn't influenced by the CONTROL signal, so, the state of the M_p transistor is determined only by the logical state of the address or data transmitted.

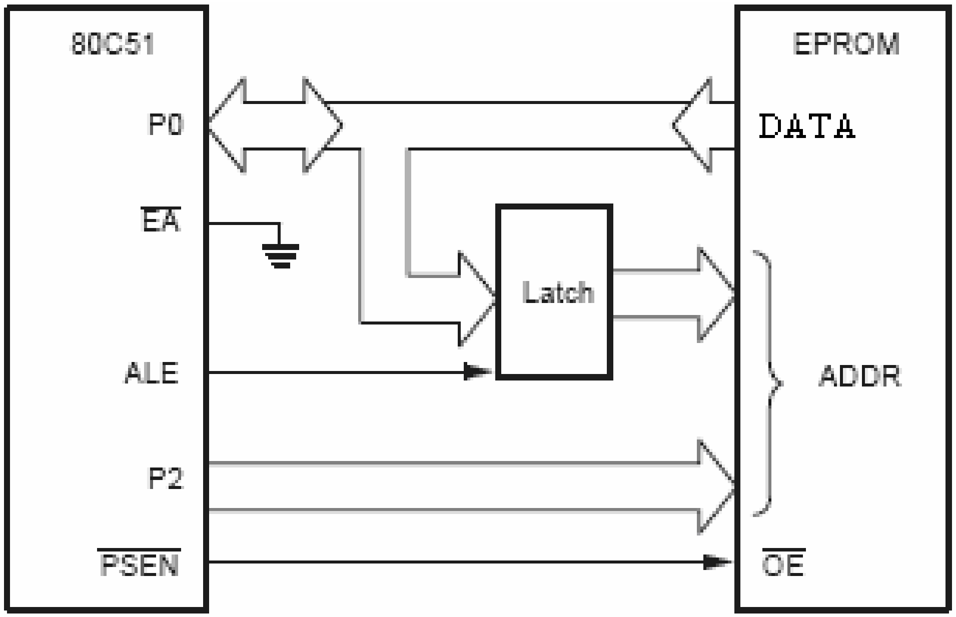


If CONTROL=0, P0 is an open-drain bidirectional port. The output of the NAND gate is 1, so, the M_p transistor is in cut-off stage, determining the open-drain configuration of the port. So, if the port is used for output, external pull-ups are used. If the port is used as an input port, logical value 1 is software set to the pin, so, the M_n transistor is in cut-off stage and the input floats.

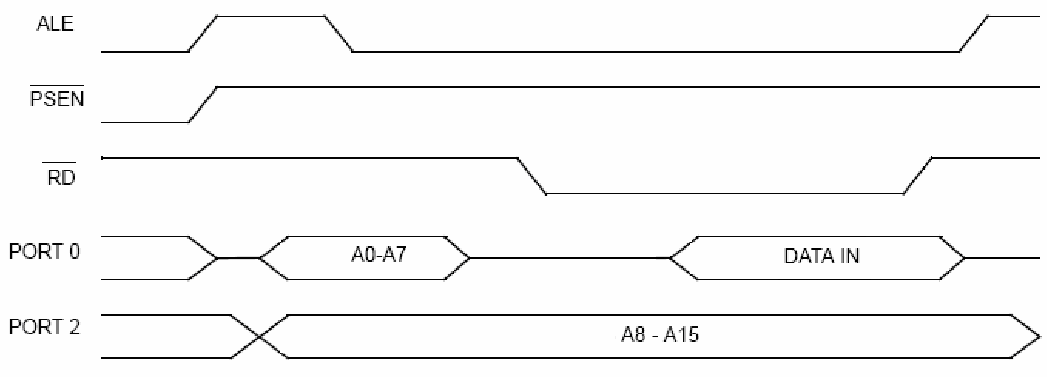
EXTERNAL PROGRAM MEMORY READ CYCLE AND CONFIGURATION

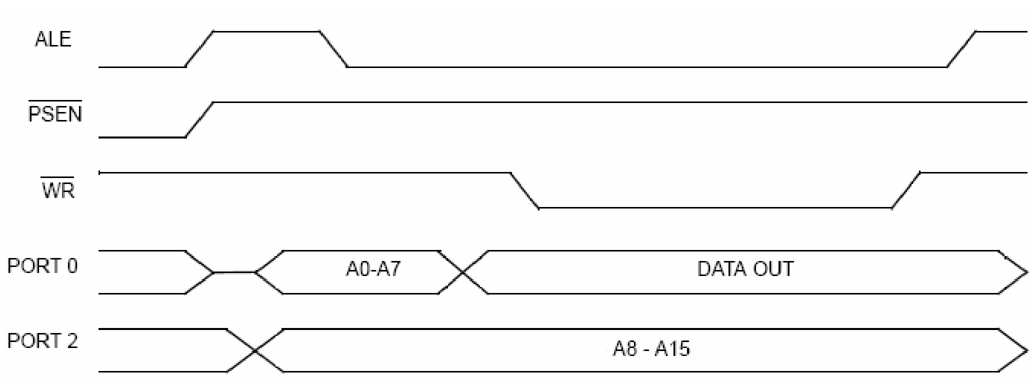
- Address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. PSEN\ signal becomes active and the information in the program memory is transmitted on the data bus being received through P0 port.

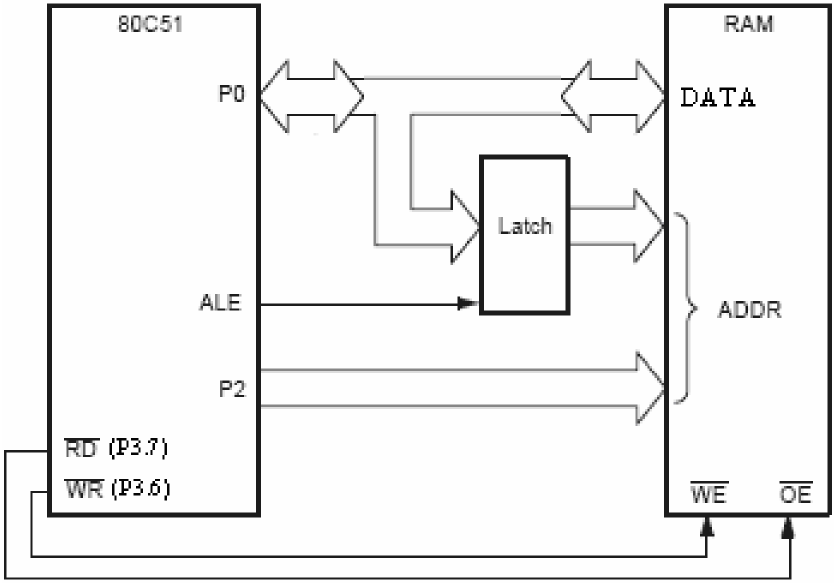




EXTERNAL DATA MEMORY READ AND WRITE CYCLES







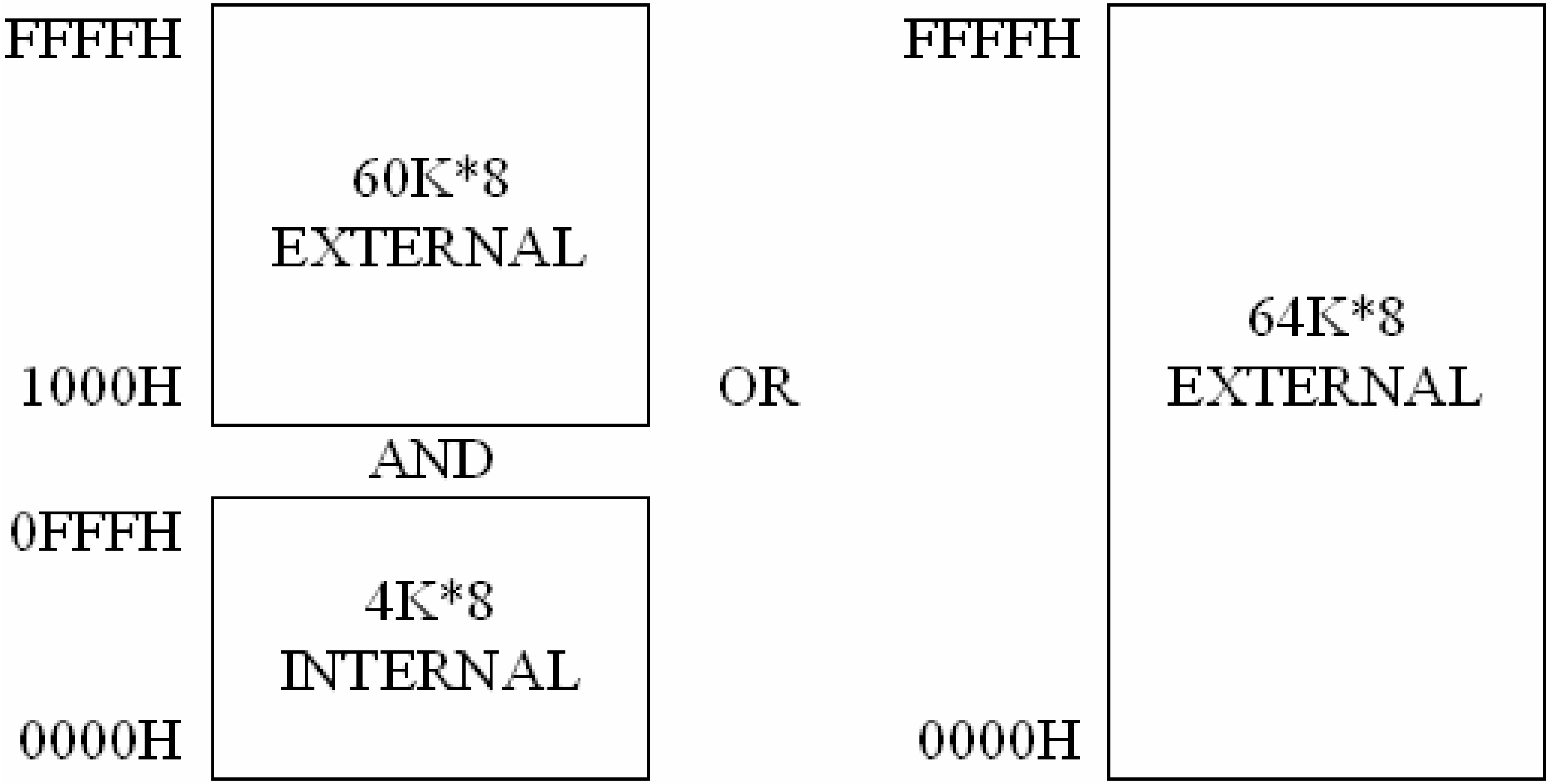
- For the read cycle, address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. RD\ signal becomes active and the information in the data memory is transmitted on the data bus being received through P0 port.
- For the write, cycle address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. Data is transmitted through P0 port on the data bus and when WR\ signal becomes active is stored in the data memory.

MEMORY ORGANIZATION

- 80C51 has separate address spaces for program and data memory.

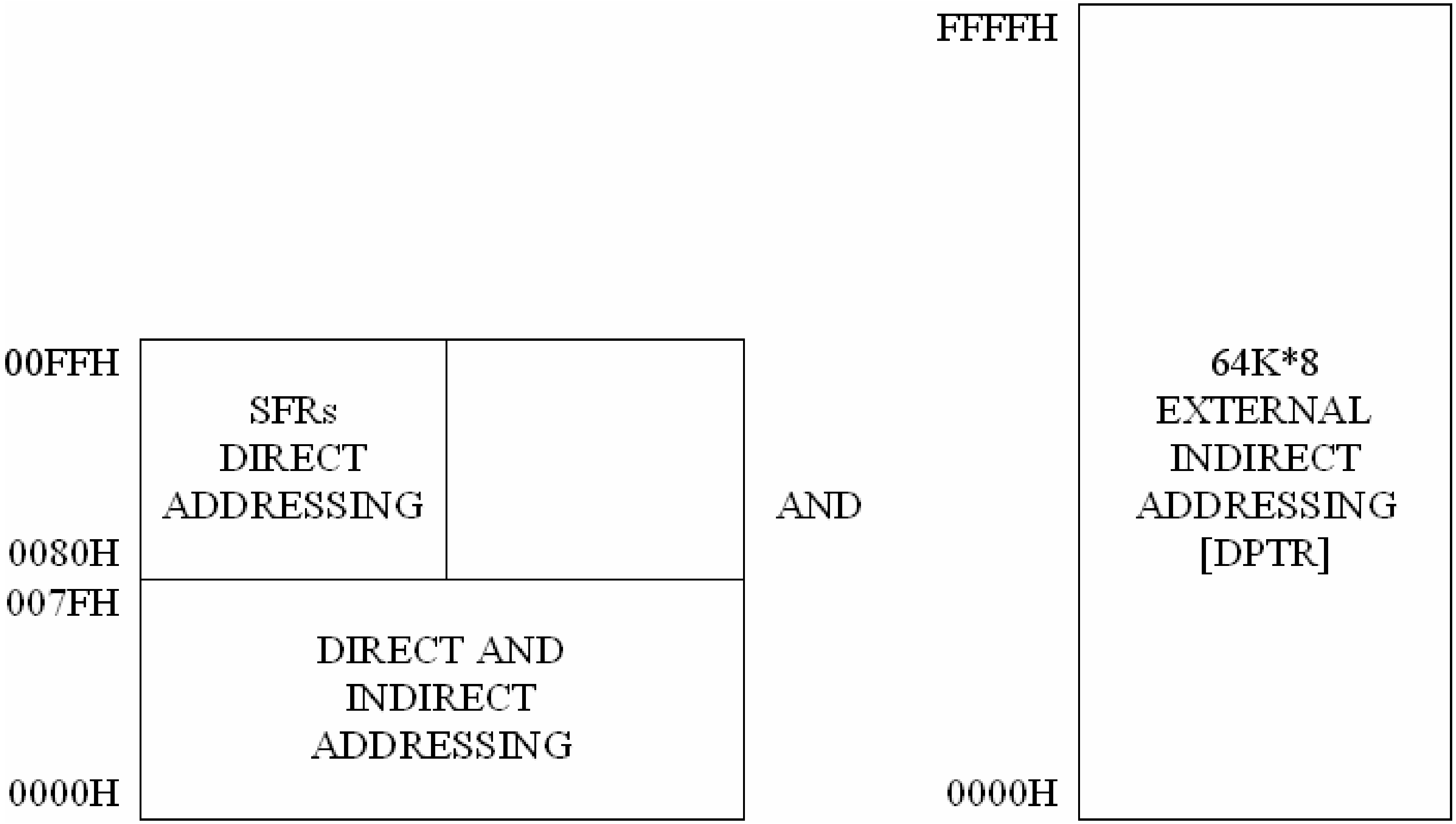
PROGRAM MEMORY

- The program memory can be up to 64K*8 long. If EA\ is externally held high, the lower 4K*8 addresses reside on chip. If EA\ is externally held low, the entire memory is external.



DATA MEMORY

- 80C51 has 128*8 internal RAM plus a number of Special Function Registers (SFRs). The lower 128*8 RAM addresses can be accessed either by direct or indirect addressing. SFRs can be accessed only by direct addressing. Direct addressing specifies the address through a number, indirect addressing specifies the address through a register.
- External data memory can be up to 64K*8 long.



00FFH

SFRs
DIRECT
ADDRESSING

0080H

007FH

DIRECT AND
INDIRECT
ADDRESSING

0000H

AND

FFFFH

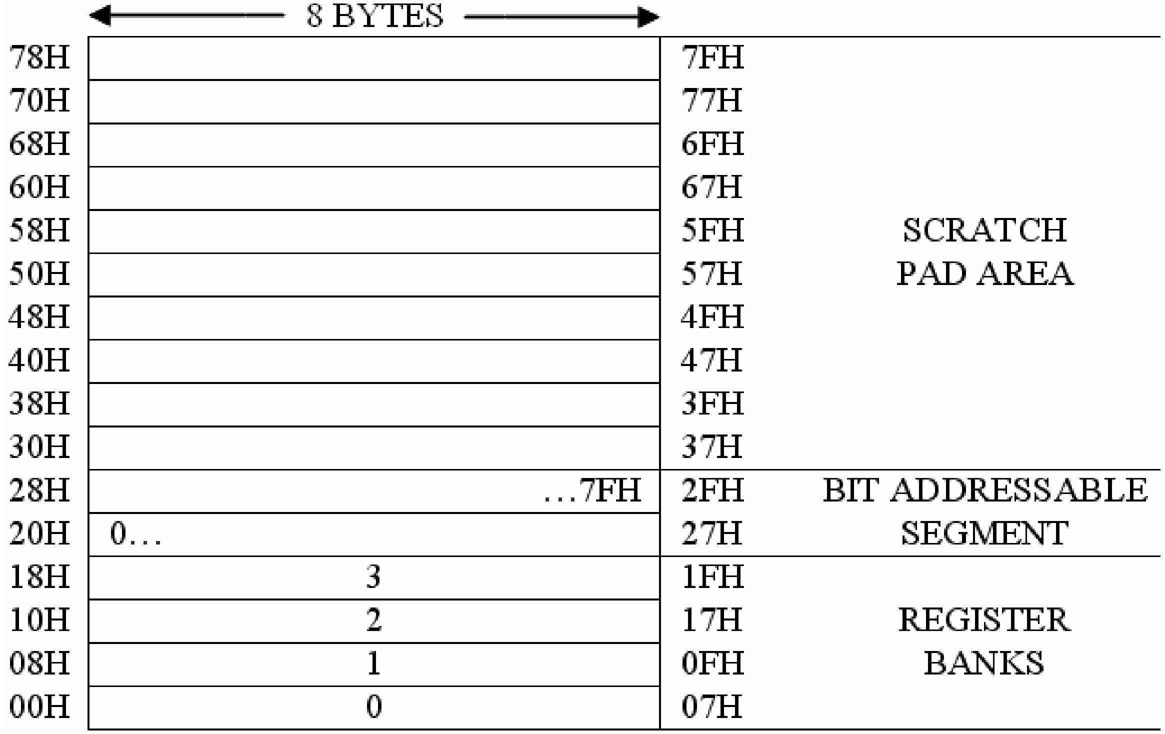
64K*8
EXTERNAL
INDIRECT
ADDRESSING
[DPTR]

0000H

DIRECT AND INDIRECT ADDRESS AREA

- The lower 128*8 addresses can be divided into 3 segments:

- Register Banks 0-3: 00H through 1FH (32 bytes). The microcontroller after reset default to register bank 0. Register bank selection is done by software. Each register bank contains 8 one-byte registers, 0 through 7.



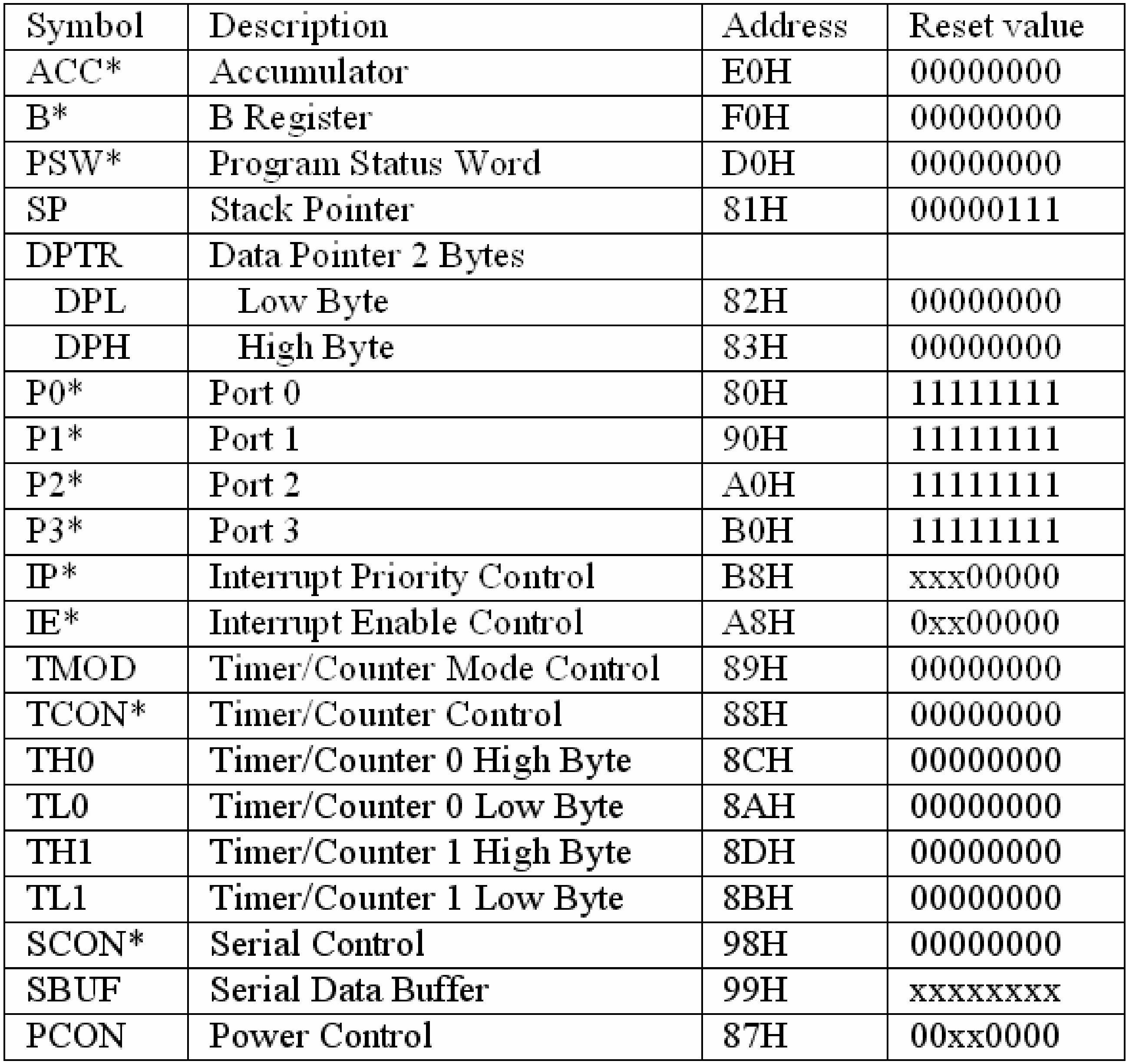
8 BYTES

78H		7FH	SCRATCH PAD AREA
70H		77H	
68H		6FH	
60H		67H	
58H		5FH	
50H		57H	
48H		4FH	
40H		47H	
38H		3FH	
30H		37H	
28H	…7FH	2FH	BIT ADDRESSABLE SEGMENT
20H	0…	27H	
18H	3	1FH	REGISTER BANKS
10H	2	17H	
08H	1	0FH	
00H	0	07H	

- Bit Addressable Area: 20H through 2FH (16 bytes). Each one of the 128 bits can be directly addressed (00H through 7FH). Each of the 16 bytes can be addressed as a byte.
- Scratch Pad Area: 30H through 7FH (80 bytes). Used for data RAM.

SPECIAL FUNCTION REGISTERS

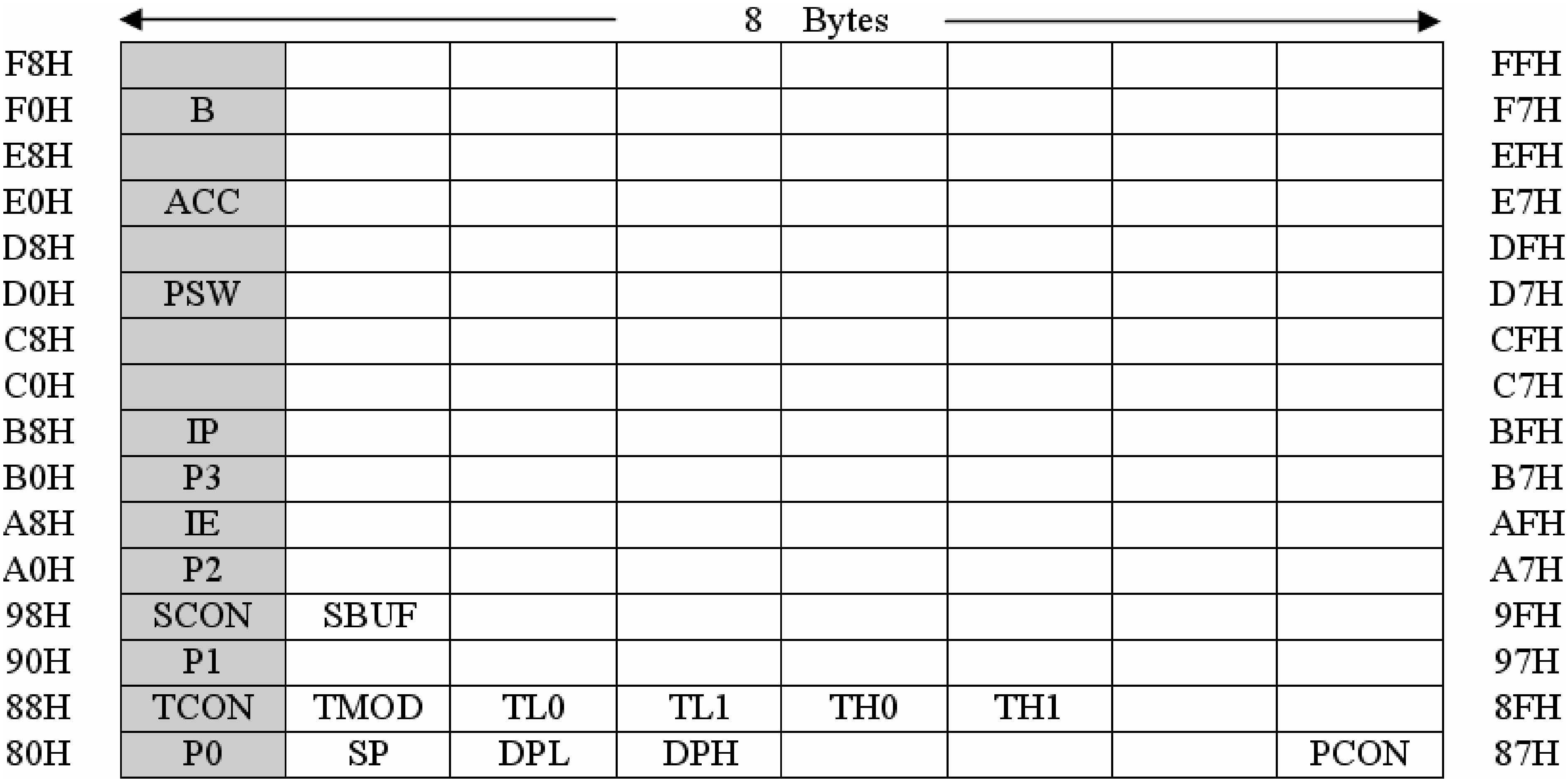
- The SFRs marked with * are both bit and byte addressable
- The other are only byte addressable.
- After reset, each SFR is loaded with a value that doesn't interfere with possible user values.



Symbol	Description	Address	Reset value
ACC*	Accumulator	E0H	00000000
B*	B Register	F0H	00000000
PSW*	Program Status Word	D0H	00000000
SP	Stack Pointer	81H	00000111
DPTR	Data Pointer 2 Bytes		
DPL	Low Byte	82H	00000000
DPH	High Byte	83H	00000000
P0*	Port 0	80H	11111111
P1*	Port 1	90H	11111111
P2*	Port 2	A0H	11111111
P3*	Port 3	B0H	11111111
IP*	Interrupt Priority Control	B8H	xxx00000
IE*	Interrupt Enable Control	A8H	0xx00000
TMOD	Timer/Counter Mode Control	89H	00000000
TCON*	Timer/Counter Control	88H	00000000
TH0	Timer/Counter 0 High Byte	8CH	00000000
TL0	Timer/Counter 0 Low Byte	8AH	00000000
TH1	Timer/Counter 1 High Byte	8DH	00000000
TL1	Timer/Counter 1 Low Byte	8BH	00000000
SCON*	Serial Control	98H	00000000
SBUF	Serial Data Buffer	99H	xxxxxxxx
PCON	Power Control	87H	00xx0000

SFR MEMORY MAP

- Byte and bit addressable SFRs are located on the first column.



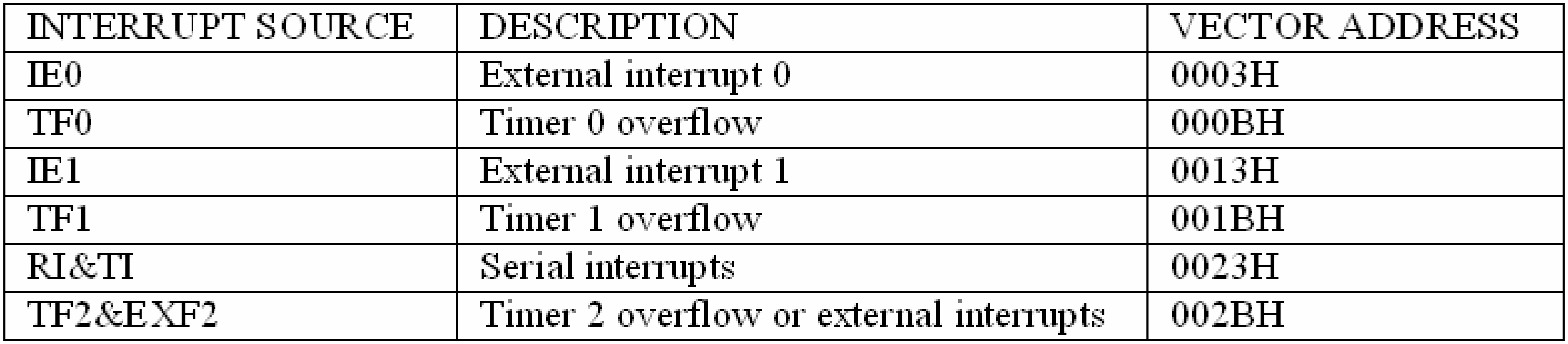
8 Bytes

F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H									DFH
D0H	PSW								D7H
C8H									CFH
C0H									C7H
B8H	IP								BFH
B0H	P3								B7H
A8H	IE								AFH
A0H	P2								A7H
98H	SCON	SBUF							9FH
90H	P1								97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	P0	SP	DPL	DPH				PCON	87H

Interrupts System

- When an interrupt occurs, the microcontroller suspends temporarly the program execution and starts running the specific interrupt routine
- For execution of interrupt routine the following steps are needed:
  - Save on stack the address of the next program instruction (2 octets) and of the PSW (2 octets).
  - Determine source of interrupt (interrupr number). Any interrupt source has an interrupt vector, keeping the jump instruction at the address when starts the interrupt routine. Vector address is calculated by microcontroller. Interrupt vectors (8 octets) are stored into a specific table.
  - Accesses the interrupt vector table and finds the routine address.
  - Executes the interrupr routine.
  - Interrupt routine ends with IRET instruction, loading from stack the location of the next program instruction (2 octets) and PSW (2 octets)

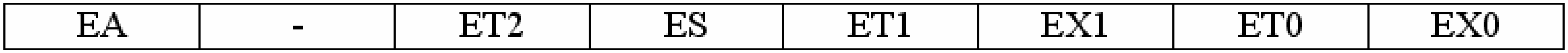
- Interrupts implementation :
  - Bit EA from register IE set to 1; means interrupts enabling
  - Set to 1 all bits in register IE for interrupts will be used
  - Each interrupt vector will be loaded with a long jump instruction to the address of the interrupt routine
  - For external interrupts, pins INT0\ (P3.2) and INT1\ (P3.3) must be set to 1, and corresponding bits (IT0 şi IT1) from TCON register must be set or reset for activating interrupts on level or edge basis.
- 80C51 microcontroller interrupts



INTERRUPT SOURCE	DESCRIPTION	VECTOR ADDRESS
IE0	External interrupt 0	0003H
TF0	Timer 0 overflow	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 overflow	001BH
RI&TI	Serial interrupts	0023H
TF2&EXF2	Timer 2 overflow or external interrupts	002BH

IE Register structure

- Bit or byte addressable. If EA is 0, all interrupts are disabled. If EA is 1, any interrupt is enabled by setting its bit to 1.
- Bit functions:
  - EA, IE.7: if EA=0, neither interrupt will be acknowledged. If EA=1, each interrupt source may be individually enabled or disabled.
  - ET2, IE.5: timer 2 overflow
  - ES, IE.4: interrupt serial port
  - ET1, IE.3: Timer 1 overflow
  - EX1, IE.2: external interrupt 1
  - ET0, IE.1: Timer 0 overflow
  - EX0, IE.0: external interrupt 0



EA	-	ET2	ES	ET1	EX1	ET0	EX0

Interrupts priorities

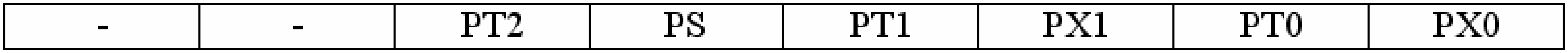
- Two priority levels. The higher one may interrupt the other. For priority assignement corresponding bit from IP register must be set to 1 or 0.
- Priorities from high to low are: IE0, TF0, IE1, TF1, RI or TI and TF2 or EXF2.

IP register

- Bit or byte addressable.

Bit functions:

  - PT2, IP.5: Timer 2 interrupt priority level (only 8052)
  - PS, IP.4: serial port priority level
  - PT1, IP.3: Timer 1 interrupt priority level
  - PX1,IP.2: external interrupt 1 priority level
  - PT0, IP.1: Timer 0 interrupt priority level
  - PX0, IP.0: external interrupt 0 priority level

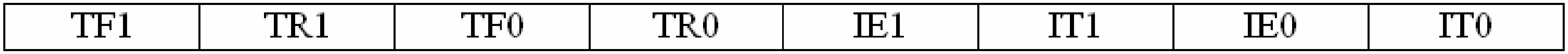


-	-	PT2	PS	PT1	PX1	PT0	PX0

Registry of the Timer System

TCON register

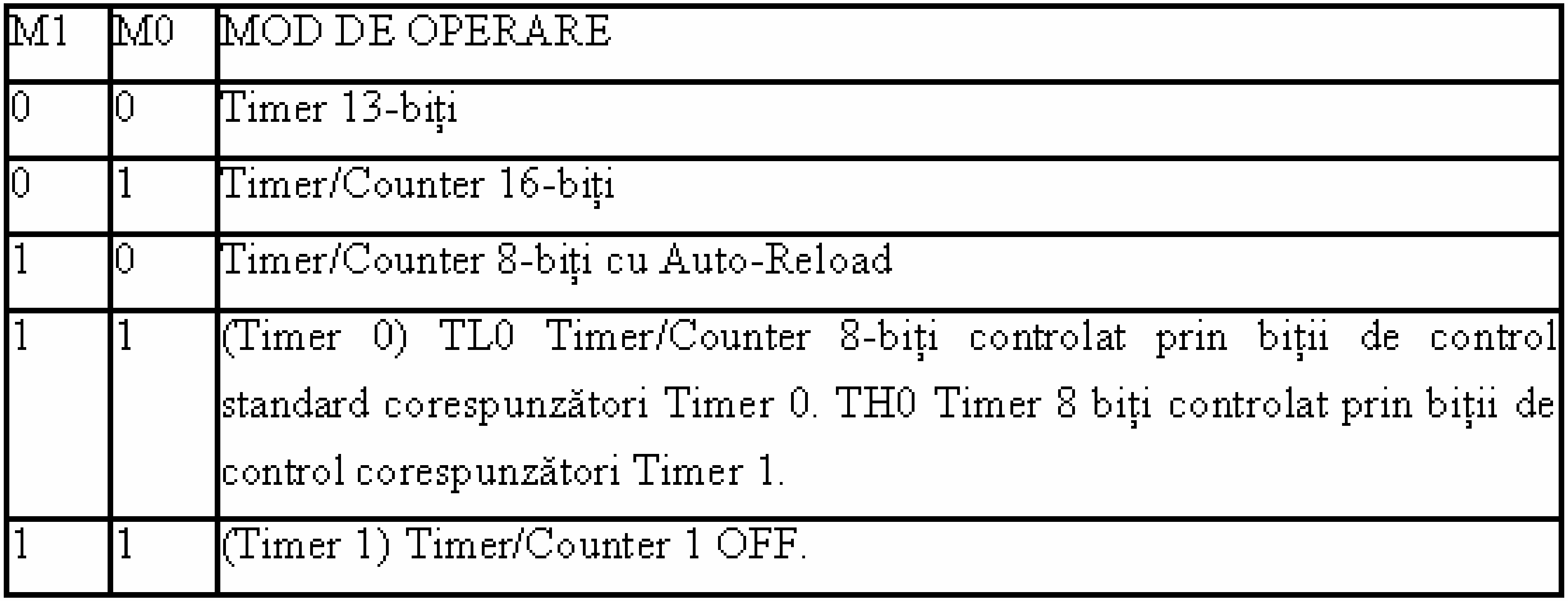
- Bit or byte addressable. Bit functions:
  - TF1, TCON.7: Flag Timer 1 overflow. Hardware erased when interrupt routine is running
  - TR1, TCON.6: Timer 1 control bit. if TR1=1, Timer 1 ON. if TR1=0, Timer 1 OFF.
  - TF0, TCON.5: Flag Timer 0 overflow. Same as Flag Timer 1 overflow.
  - TR0, TCON.4: Timer 0 control bit.Same as for Timer 1.
  - IE1, TCON.3: Flag for external interrupt 1. Set hardware when external interrupt 1 edge detected; hardware reset when processing interrupt.
  - IT1, TCON.2: Interrupt 1 type control bit. If IT1=1, interrupt 1 is triggered by a falling down edge. If IT1=0, interrupt 1 is triggered by level 0.
  - IE0, TCON.1: Flag for external interrupt 0. Set hardware when interrupt edge detected, hardware erased when interrupt processing.
  - IT0, TCON.0: Interrupt 0 type control bit . If IT0=1, interrupt 0 is triggered by falling edge. If IT0=0, interrupt 0 is treiggered by logic level 0.



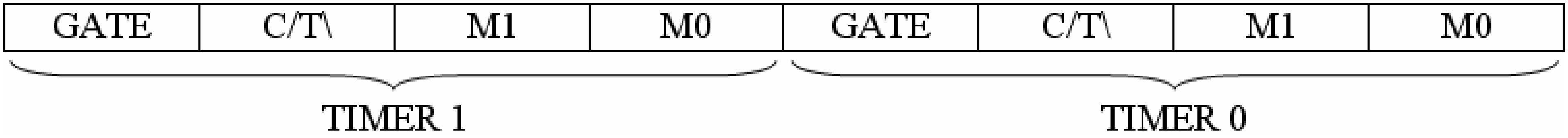
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TMOD Register

- Byte addressable. Bit functiones:
- GATE: If GATE=1, TIMERx will run if TRx=1 and INTx=1 (hardware control). If GATE=0, TIMERx will run as TRx=1 (software control).
- C/T\, Timer or Counter Selector. If C/T\=0, Timer operation (input from internal clock). If C/T\=1, Counter operation (input from Tx).
- M1, M0: operation mode selection



M1	M0	MOD DE OPERARE
0	0	Timer 13-biţi
0	1	Timer/Counter 16-biţi
1	0	Timer/Counter 8-biţi cu Auto-Reload
1	1	(Timer 0) TL0 Timer/Counter 8-biţi controlat prin biţii de control standard corespunzători Timer 0. TH0 Timer 8 biţi controlat prin biţii de control corespunzători Timer 1.
1	1	(Timer 1) Timer/Counter 1 OFF.

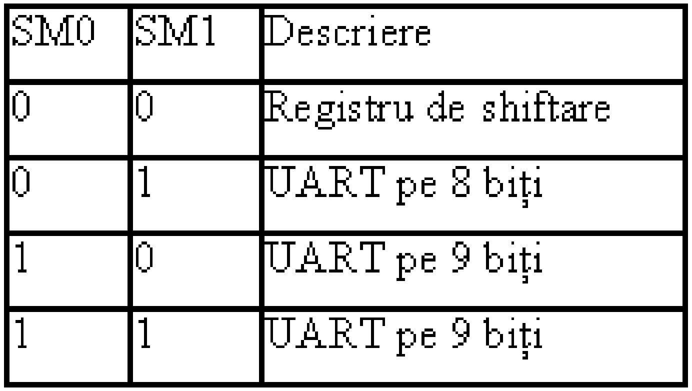


GATE	C/T\	M1	M0	GATE	C/T\	M1	M0
TIMER 1				TIMER 0			

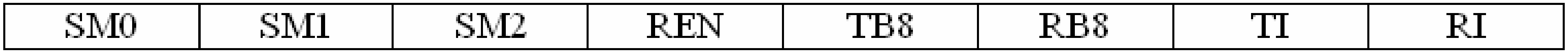
Serial Communication

SCON Register

- Bit or byte addressable. Bit functions:
  – SM0: Bit 0 Serial Port mode (MSB).
  – SM1: Bit 1 Serial Port mode(LSB).
  – SM2: Activates communications modes
  – REN: Software set or reset for Reception enable/disable
  – TB8, RB8: Special role in operation modes 2 and 3
  – TI: Transmission interrupt
  – RI: Reception interrupt



SM0	SM1	Descriere
0	0	Registru de shiftare
0	1	UART pe 8 biți
1	0	UART pe 9 biți
1	1	UART pe 9 biți



SM0	SM1	SM2	REN	TB8	RB8	TI	RI

mode 0: port communicates with fixed baud rate

- Baud rate = Osc Freq/12
- Port acts as a 8bit shift register; data sent with LSB first through RXD pin.

mode 1: variable baud rate, generated by Timer 1

- Baud rate = (K * Osc Freq)/{32 * 12 * [256 - (TH1)]}
- Bit SMOD from PCON register determines K value. If SMOD = 0, K = 1, if SMOD = 1, K = 2.
- TH1 = 256 – (K * Osc Freq) / (384 * Baud Rate)
- Frame format: 1 start bit, 8 data bit, 1 stop bit.
- Interrupts TI şi RI are activated when a frame was sent or received

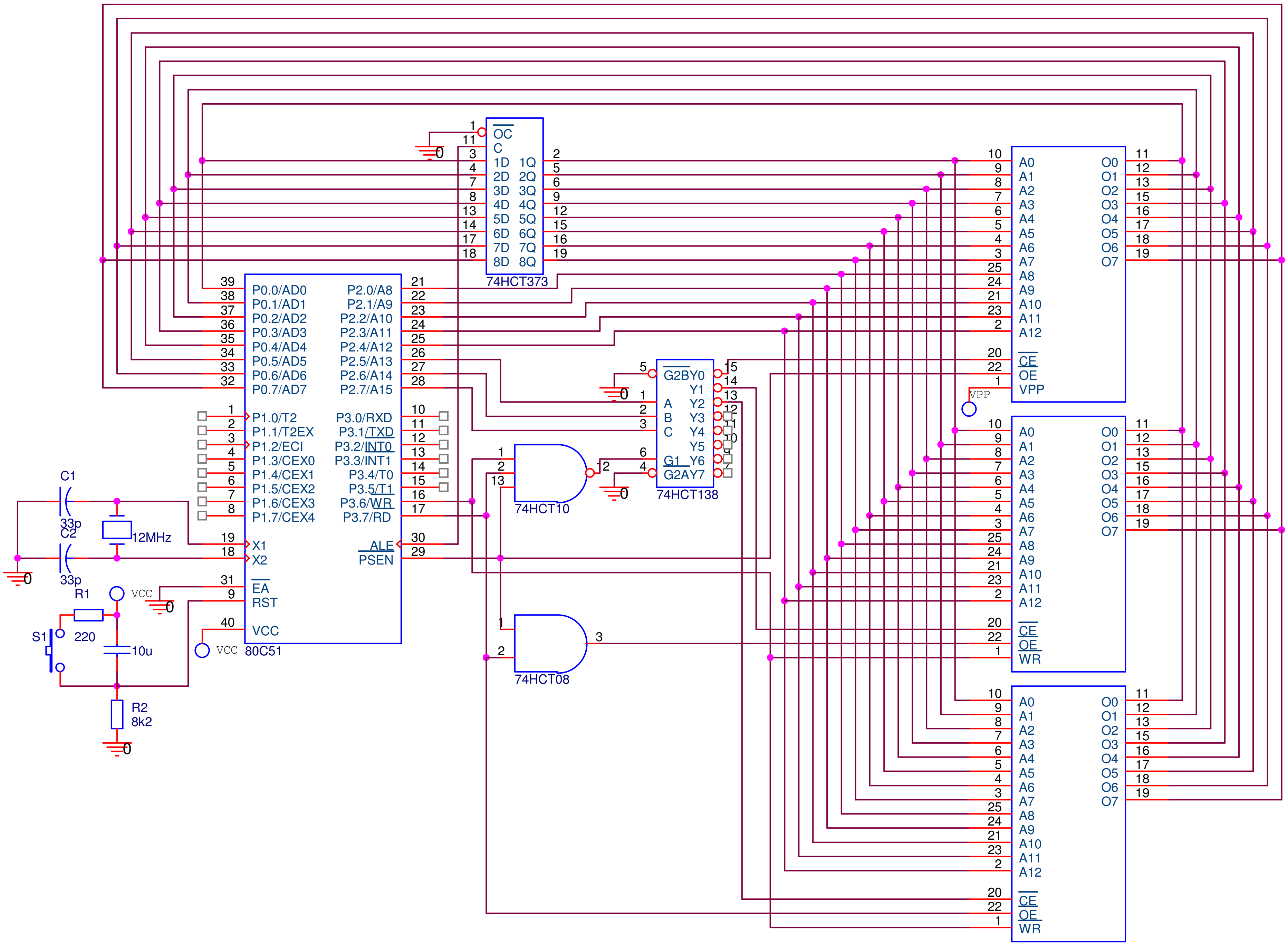
mode 2: fixed baud rate communication

- SMOD = 1, Baud rate = 1/32*Osc Freq.
- SMOD = 0, Baud rate = 1/64*Osc Freq.
- Frame format: 1 start bit, 8 data bit, 1(stick) bit, 1 stop bit. The 9th bit (stick bit) is used for interprocessor communications

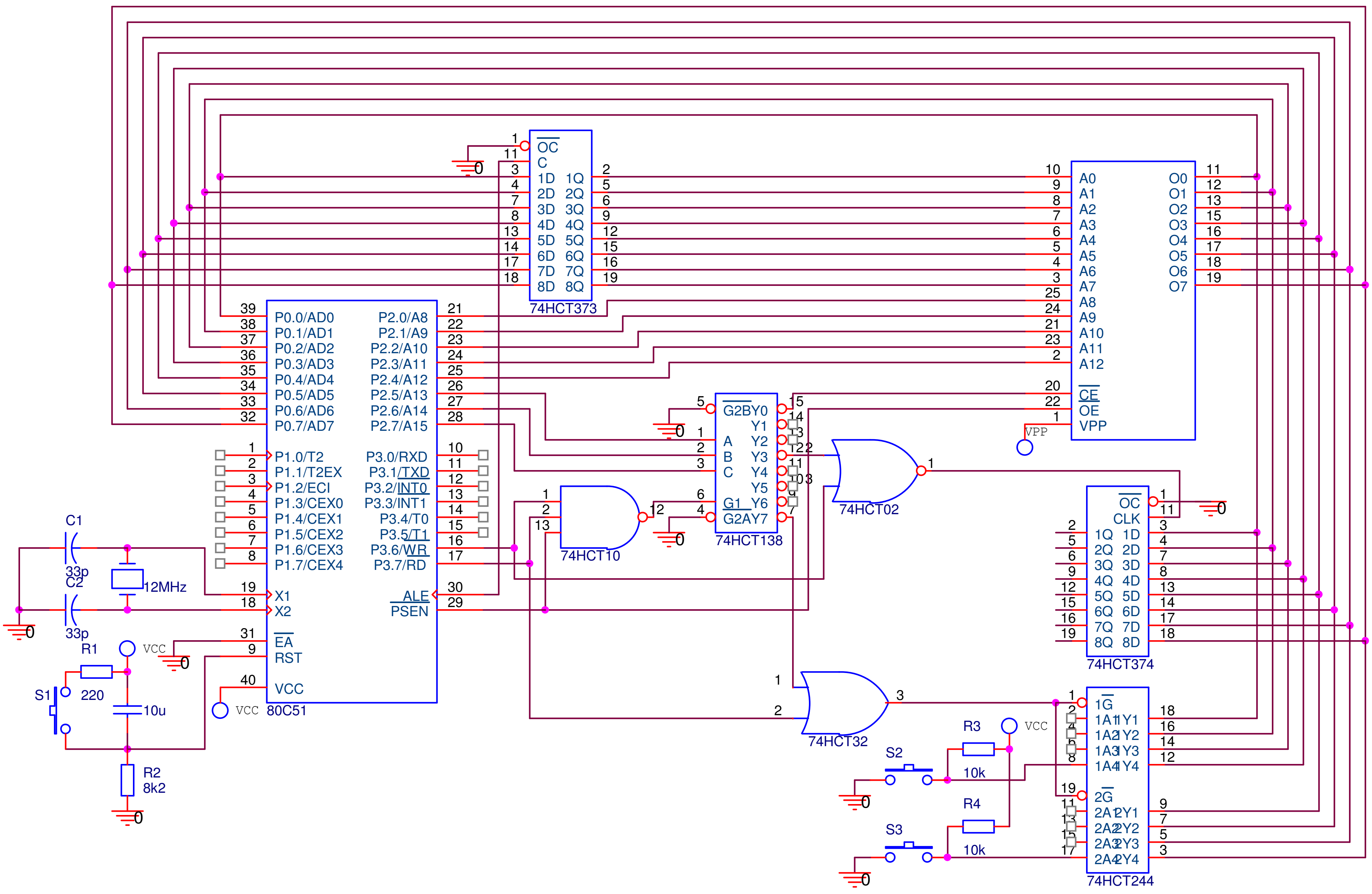
mode 3: similar to mode 2 as frame format and the role of stick bit, and as baud rates is similar to mode 1

Proposed Problems

- Design a system based on a 80C51 microcontroller, with the following blocks:
  - quartz oscillator with a 12MHz frequency
  - Reset circuit
  - 8k*8 bit external program memory with the low (base) address 0000H
  - 8k*8 bit data & program external memory with low address of 2000H
  - 8k*8 bit external data memory with the base address 4000H


80C51
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P1.0/T2
P1.1/T2EX
P1.2/ECI
P1.3/CEX0
P1.4/CEX1
P1.5/CEX2
P1.6/CEX3
P1.7/CEX4
X1
X2
EA
RST
VCC
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
P2.4/A12
P2.5/A13
P2.6/A14
P2.7/A15
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P3.6/WR
P3.7/RD
ALE
PSEN
74HCT373
OC
C
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
7D 7Q
8D 8Q
74HCT138
G2B Y0
Y1
A Y2
B Y3
C Y4
Y5
G1 Y6
G2A Y7
74HCT10
74HCT08
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
O0 O1 O2 O3 O4 O5 O6 O7
CE
OE
VPP
WR
VPP
VCC
0
C1
33p
C2
33p
12MHz
R1
220
10u
S1
R2
8k2

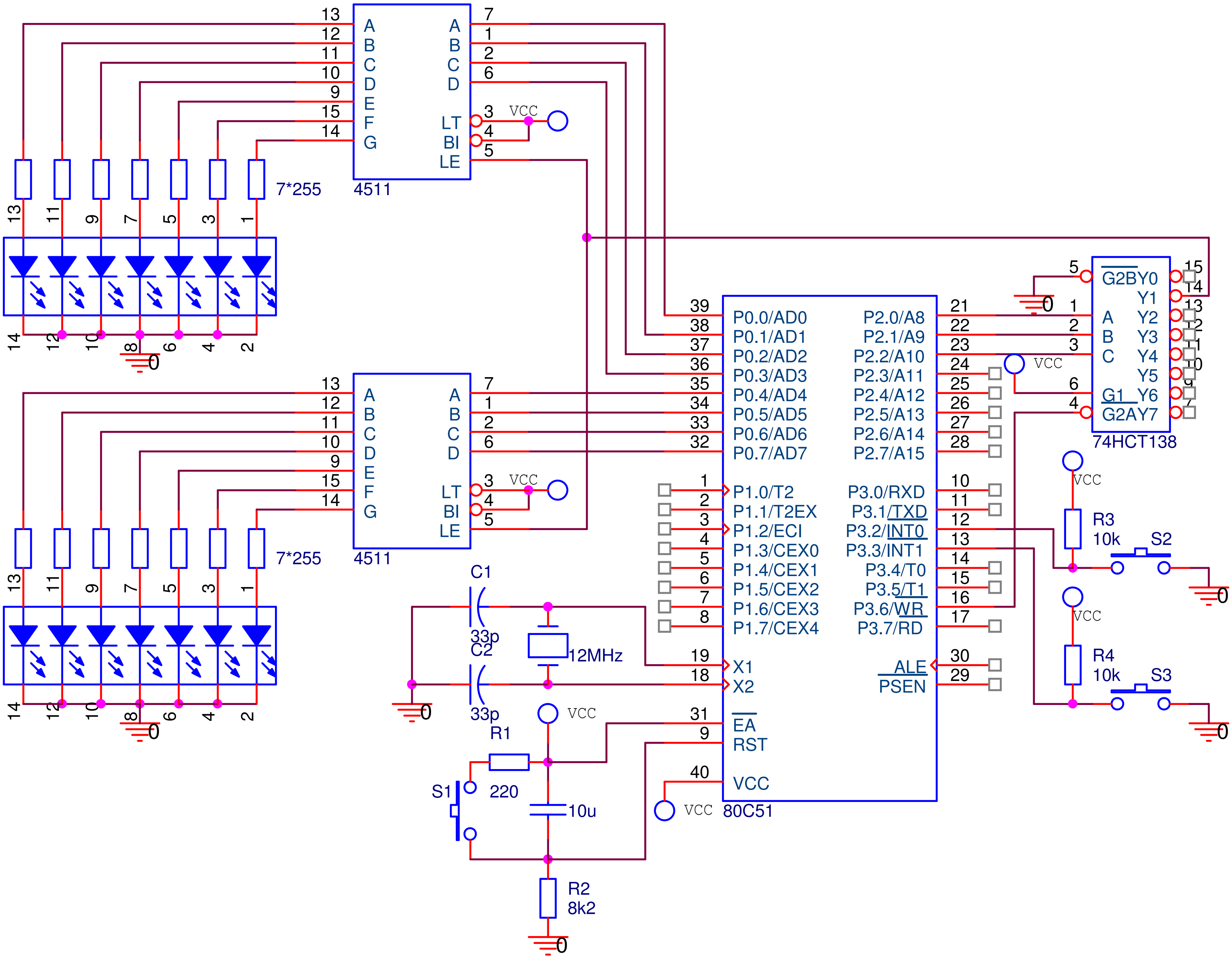
- Design a system based on a 80C51 microcontroller, with the following blocks:
  - – quartz oscillator with a 12MHz frequency
  - – Reset circuit
  - – 8k*8 bit external program memory with the low (base) address 0000H
  - – Output port at address 011XXXXXXXXXXXXXb
  - – Input port at address 111XXXXXXXXXXXXXb , here having connected two keys


74HCT373
OC
C
1D 1Q
2D 2Q
3D 3Q
4D 4Q
5D 5Q
6D 6Q
7D 7Q
8D 8Q
A0 O0
A1 O1
A2 O2
A3 O3
A4 O4
A5 O5
A6 O6
A7 O7
A8
A9
A10
A11
A12
CE
OE
VPP
80C51
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
P2.4/A12
P2.5/A13
P2.6/A14
P2.7/A15
P1.0/T2
P1.1/T2EX
P1.2/ECI
P1.3/CEX0
P1.4/CEX1
P1.5/CEX2
P1.6/CEX3
P1.7/CEX4
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P3.6/WR
P3.7/RD
X1
X2
ALE
PSEN
EA
RST
VCC
C1
33p
C2
33p
12MHz
R1
220
S1
10u
R2
8k2
VCC
74HCT138
G2B Y0
Y1
A Y2
B Y3
C Y4
Y5
G1 Y6
G2A Y7
74HCT10
74HCT02
74HCT32
74HCT374
OC
CLK
1Q 1D
2Q 2D
3Q 3D
4Q 4D
5Q 5D
6Q 6D
7Q 7D
8Q 8D
74HCT244
1G
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2G
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
R3
10k
R4
10k
S2
S3
VCC
VPP
0

- Design a system based on a 80C51 microcontroller, with the following blocks:
  - quartz oscillator with a 12MHz frequency
  - Reset circuit
  - Output port at address XXXXX001XXXXXXXXb having connected two 7-segments LED displays using common cathode, with: V_{LED}=1,7V and I_{LED}=10mA
  - 2 keys connected at interrupt input lines
  - Only internal program memory is used

Hint: Calculus for resistor values (for the LED based display) is given by::

$R=(V_{OHTYP}-V_{LED})/I_{LED}=(4,25V-1,7V)/10mA=255\Omega$


4511
A
B
C
D
E
F
G
LT
BI
LE
VCC
7*255
4511
80C51
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P1.0/T2
P1.1/T2EX
P1.2/ECI
P1.3/CEX0
P1.4/CEX1
P1.5/CEX2
P1.6/CEX3
P1.7/CEX4
X1
X2
EA
RST
VCC
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
P2.4/A12
P2.5/A13
P2.6/A14
P2.7/A15
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P3.6/WR
P3.7/RD
ALE
PSEN
74HCT138
G2BY0
Y1
A Y2
B Y3
C Y4
Y5
G1 Y6
G2AY7
C1
33p
C2
33p
12MHz
R1
220
S1
10u
R2
8k2
R3
10k
S2
R4
10k
S3
0