AN1326

Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications

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INTRODUCTION

The LDMOS transistors are CMOS devices, designed for high frequency and high power operation. These devices are widely used for RF power amplifier applications such as GSM and CDMA cellular base stations, radar, CATV, and portable radio devices. A limiting factor of these devices is the significant drifts of quiescent current (I_{DQ}) at a fixed gate bias voltage (V_{GS}) over temperature, due to the charge build-up in the Drain-Gate region, that is caused by hot carrier injection effects.

The I_{DQ} changes proportionally with both the gate bias voltage and temperature.

In order to maintain the maximum output power with high linearity, the I_{DQ} needs to be constant over time across all operating temperature ranges. To achieve this goal, the gate bias voltage needs to be adjusted during operation to compensate the temperature changes.

The Digital-to-Analog Converter (DAC) is favorably used in the bias control circuit for the base station power amplifier module (PAM). In practical applications, the bias control circuit maintains the I_{DQ} within a ±4% range. This application note shows an example of how the Digital-to-Analog (DAC) converter is used for this purpose.

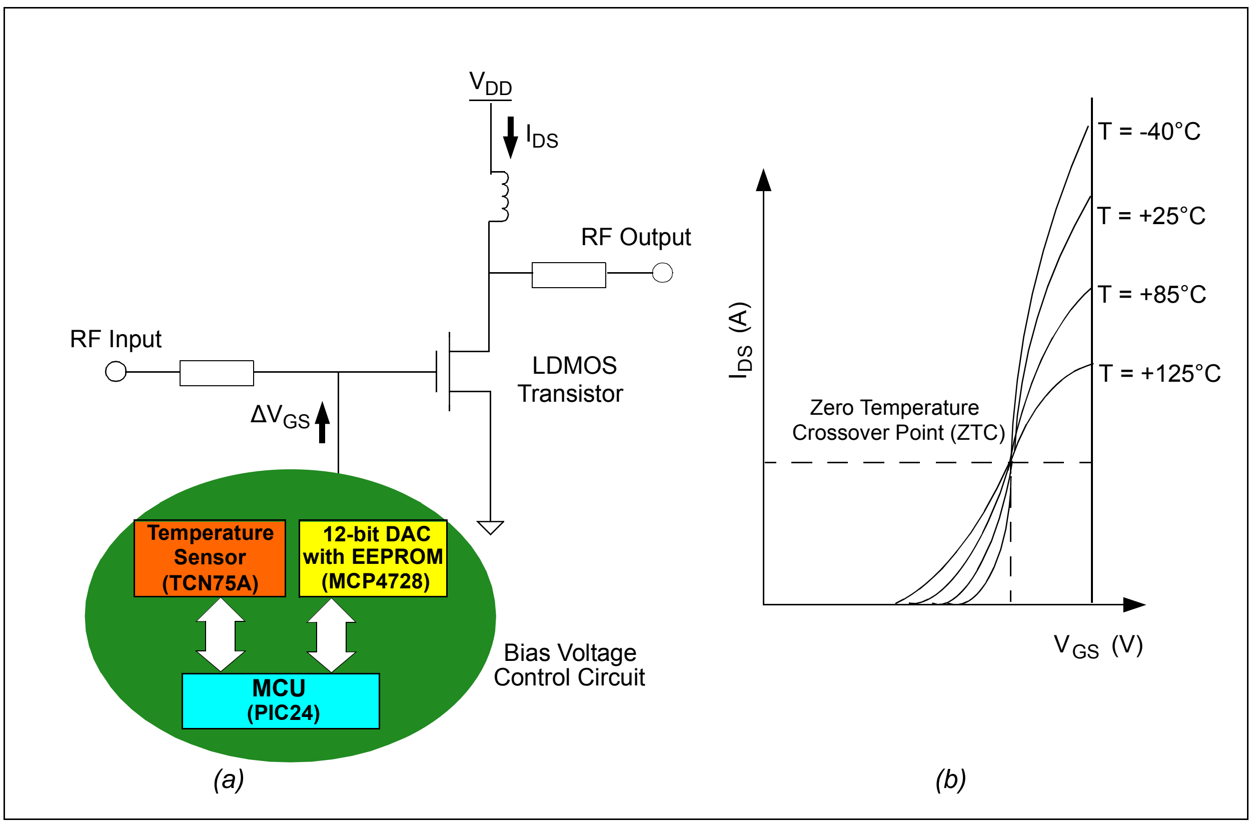


FIGURE 1: *(a) Simplified LDMOS RF Power Amplifier with Temperature-Monitored Bias Control Schematics. (b) Typical I_{DS} vs. V_{GS} Characteristics over Temperature.*

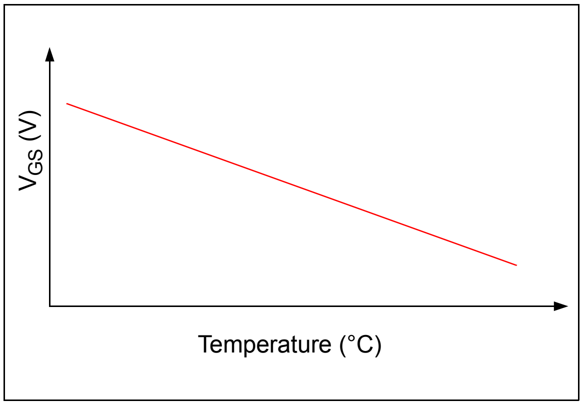


FIGURE 2: *Example of V_{GS} vs. Temperature for Constant I_{DQ}.*

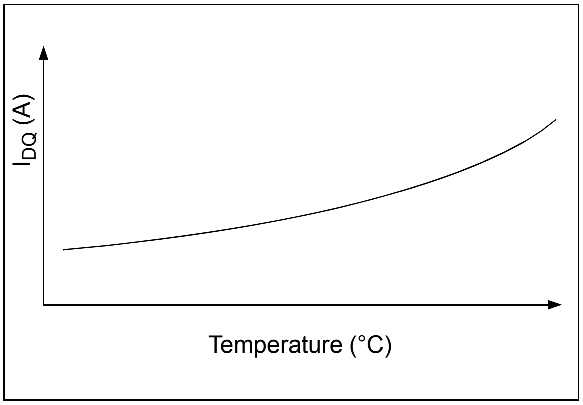


FIGURE 3: *Example of I_{DQ} vs. Temperature of Typical LDMOS Amplifier with Constant V_{GS}.*

Figure 1 shows (a) a simplified diagram for the LDMOS bias control using a 12-bit DAC device and a temperature sensor, and (b) a general behavior of I_{DS} vs. V_{GS} over temperature for class AB LDMOS amplifier. At a fixed gate bias voltage (V_{GS}), the I_{DS} drifts as temperature changes. Below the zero temperature crossover point (ZTC), I_{DS} is higher with higher temperature. But, above the ZTC point, I_{DS} is higher with lower temperature.

Figure 2 shows the gate bias voltage over temperature for constant quiescent current (I_{DQ}), and Figure 3 shows the I_{DQ} over temperature with constant V_{GS}.

BIAS VOLTAGE CONTROL USING DAC

In order to keep I_{DQ} constant over the operating temperature range, the MCU measures the temperature changes using the temperature sensor and sets a new bias voltage, using the 12-bit DAC device. This process can be done by using a look-up table of the V_{GS} value vs. I_{DS} vs. temperature.

The smallest step size (LSB size) for the bias control voltage depends on the DAC resolution and full scale range. For the 12-bit DAC (MCP4728), the smallest resolution is about 1 mV when the full scale range is set from 0V to 4.096V.

The procedure is summarized below:

a) Pre-store the I_{DS} vs. V_{GS} vs. temperature data in the look-up table in the control device (PIC24 microcontroller).

b) Measure temperature periodically during operation.

c) Control the DAC output voltage for a new V_{GS} voltage using the look-up table.

Selecting DAC Device

The users have many options in selecting a right DAC device for their specific applications:

- DAC resolutions (8 to 12 bits)
- Accuracy
- Internal or external reference
- Digital interface type
- Number of output channels
- Device cost, etc.

For the cellular base station applications, a 12-bit resolution DAC with multiple channel outputs is suitable. The DAC performance parameters are temperature-dependent, and most of the parameter errors can be corrected using an appropriate algorithm.

Review of the MCP4728 Features

The MCP4728 is a 4-channel 12-bit voltage output Digital-to-Analog Converter (DAC) from Microchip Technology. Each channel output is individually controlled and can use an internal voltage reference (2.048V) or V_{DD} as reference. Each channel output has an op amp. Therefore, it does not require external output buffers.

The device also has EEPROM memory for each channel. The user can store channel configuration settings in the EEPROM. When the device is first powered up, or recovering from a power failure, the device can immediately provide the same output voltage with the settings in the previous operation. Table 1 summarizes the features of the MCP4728 and Figure 4 shows the functional diagram of the device.

TABLE 1: KEY PARAMETERS OF MCP4728

Parameters	Description
Resolution, N	12 Bits
Number of output channel	4 Analog Outputs
Reference Voltage (V_{REF})	The user can select internal or external V_{REF} individually for each channel. • If internal reference is selected: V_{REF} = 2.048V • If external reference is selected: $V_{REF} = V_{DD}$
LSB (Least Significant Bit)	LSB is the step size resolution between consecutive DAC inputs. LSB of the MCP4728 is defined as: $LSB = \frac{V_{REF}}{2^N} Gx$ = 500 µV when Gain = 1x and internal reference is used, = 1 mV when Gain = 2x and internal reference is used. where Gx is the output op amplifier gain setting.
Output Voltage	The DAC output voltage is defined by the DAC input code, LSB and output op amp gain setting. Its minimum is the offset voltage and the maximum is the reference voltage times the gain setting. The output voltage is given by: $V_{OUT} = (DAC\ Input\ Code) \bullet (LSB) \bullet (Gx)$ $DAC\ Input\ Code = \frac{V_{OUT}}{LSB} \bullet (Gx)$ **Example:** Output voltage range • When internal reference is selected: V_{OUT} = V_{OFFSET} to 2.048V with Gain = 1x setting = 2* V_{OFFSET} to 4.096V with Gain = 2x setting • When external reference is selected: V_{OUT} = V_{OFFSET} to V_{DD}, regardless of gain setting **Note:** When external reference is selected, only gain setting of 1x is used and 2x is ignored.
Serial Interface	**I^2C^{TM}** Three I^2C address bits are stored in EEPROM. • I^2C address bit programming: (a) The user can reprogram the address bits on the user's application PCB board by using a simple I^2C address write command, (b) or the address bits can be pre-programmed for the customer, during the device final test, at the factory before shipping.

TABLE 1: KEY PARAMETERS OF MCP4728 (CONTINUED)

Parameters	Description
Output Settling Time	**6 µs** **Note:** This delay time tells how soon the analog DAC output is settled after the user sends a write command for a new output voltage. This is the time delay between the moment when the DAC input code is loaded to the output DAC register and the DAC analog output has reached the new analog output voltage. Assuming the $\overline{\text{LDAC}}$ pin is grounded, the total delay time for the new output is approximately as follows: • Total Time Delay = 6 µs + 8 * number of bytes in I^2C command * 1/I^2C speed **Example:** If the user updates the V_{OUT} with the Fast Write command, the output can be updated after the following time delay from the beginning of the Fast Write command: • When I^2C clock speed = 3.4 MHz: Time delay for V_{OUT} A = 6 µs + 8 * 3 * 1/3.4 MHz = 6 µs + 7.06 µs = 13.06 µs • When I^2C clock speed = 400 kHz: Time delay for V_{OUT} A = 6 µs + 8 * 3 * 1/400 kHz = 6 µs + 60 µs = 66 µs
DC Accuracy:	
INL	**+/- 2 LSB (typical), +/- 13 LSB (maximum)** **Note:** Integral non-linearity error tells the linearity of the output vs. input code. This INL error can be calibrated.
DNL	**+/- 0.2 (typical), +/- 0.75 LSB (maximum)** **Note:** Differential non-linearity error tells the difference in output step size as input code change by 1 LSB. The output changes monotonically if the DNL error is less than +/- 1 LSB.
Output Offset Voltage	**5 mV (typical), 20 mV (maximum)** **Note:** The output voltage at code 0x000h is called offset error. For the DAC with output op amplifier, the output offset error is mostly contributed by the op amp's V_{OS} voltage. When the output offset voltage is 5 mV and 1 LSB = 1 mV, the DAC analog output does not change until the input code is greater than 5 LSB. See Figure 5 for more details.
EEPROM	The device has non-volatile EEPROM memory for the DAC input code, configuration bit settings, and I^2C address bits. The user can reprogram the EEPROM any time. Once the device powers-up, it uploads the EEPROM contents to the output DAC registers. Therefore, the output is immediately available with the programmed data, without help from the MCU. This feature is very useful in the system where accidental power shutdown occurs occasionally. The DAC can provide correct outputs immediately with the previous settings by itself when the power is restored.

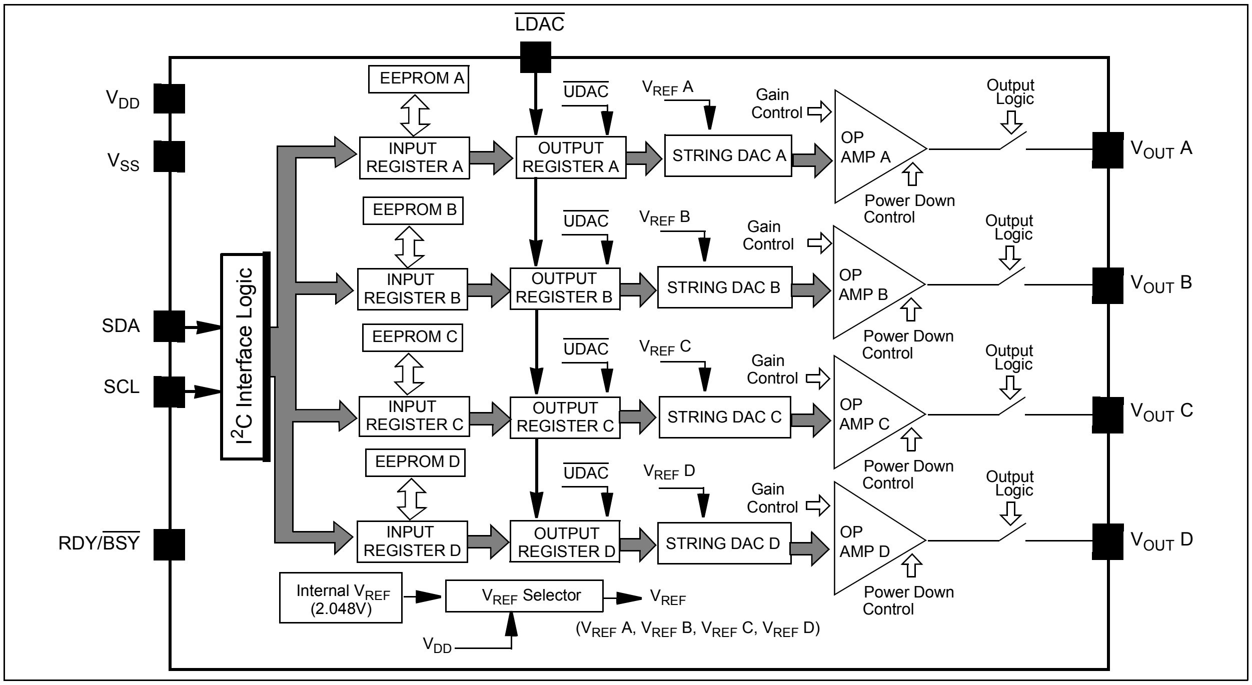


FIGURE 4: *MCP4728 Functional Block Diagram.*

USING THE MCP4728

Figure 5 shows the Output Voltage vs. Digital Input Code of the MCP4728 with the internal V_{REF} and gain of 2x options. The offset voltage (V_{OFFSET} in Figure 5) is a combination of all offsets, including the DAC converter and output op amp. The user must be aware that the output voltage does not increase until the input code exceeds the value for the total offset voltage. This is shown in details in Figure 5.

Figure 6 shows the absolute output error for each channel without corrections. The data is taken only from code 100 to 3500. This represents the 100 mV to 3.5V range. The output voltage error is between 6.5 to 15 LSB (or 6.5 mV to 15 mV) for all 4 channels. The error is mostly due to the offset error which can be easily calibrated. By removing the offset, V_{OUT} will only vary within about 6 LSB or 6 mV. There is a minor variation between channel to channel outputs at the same input code, but the difference is only a few LSBs.

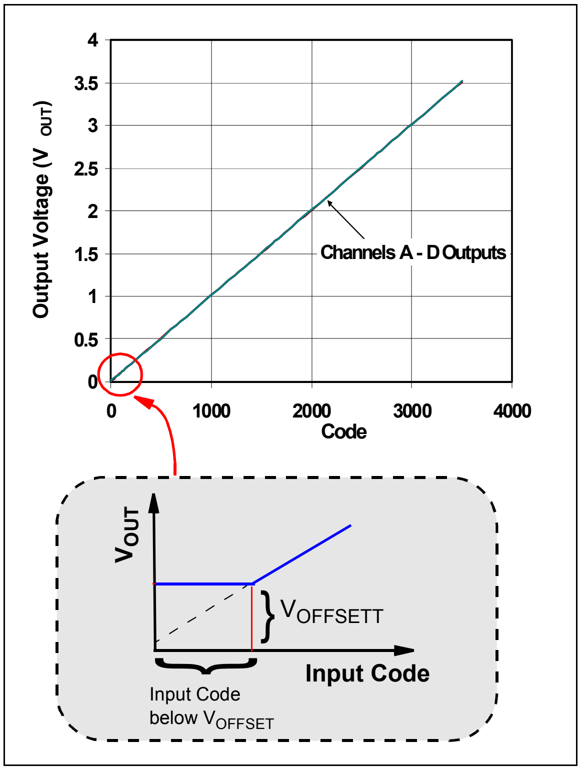


FIGURE 5: Output Voltage vs. Code. Note that the V_{OFFSET} is mostly contributed by the V_{OS} of the output amplifier.

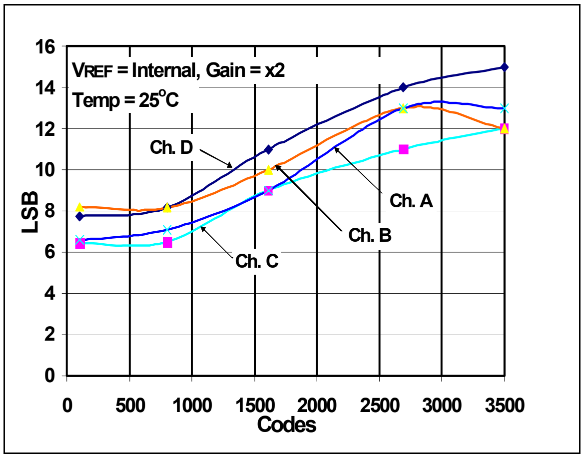


FIGURE 6: Absolute Output Error of the MCP4728.

Figure 7 shows the MCP4728 external circuit configuration for the applications. Figure 8 shows another example for 8 output channels using two MCP4728 devices.

I^2C Address of the MCP4728

The device has three reprogrammable I^2C address bits. Using the 3 bits, the user can have 8 unique I^2C device addresses. The I^2C address bits are programmed into the EEPROM before the device is shipped to the customer, and are reprogrammable by the customer. When the user programs the I^2C address bits, the $\overline{LDAC}$ pin is used to select the device for programming. In that case, do not ground the $\overline{LDAC}$ pin, but connect to the MCU I/O pin as shown in option line in Figure 7 and Figure 8. See the MCP4728 data sheet for more details of the I^2C address bit programming options.

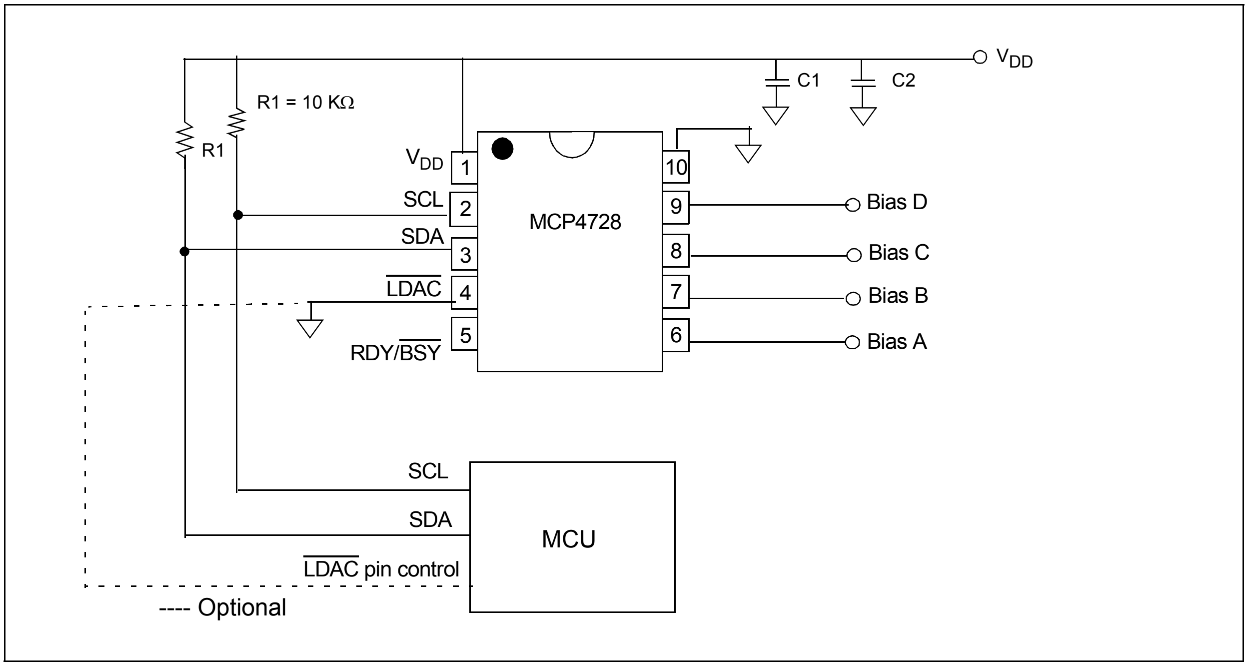


FIGURE 7: *Using the MCP4728 for the Bias Voltage Control Circuit.*

Note:	For more details on the $\overline{\text{LDAC}}$ and RDY/$\overline{\text{BSY}}$ pin functions, see the MCP4728 data sheet, *12-Bit, Quad Digital-to-Analog Converter with EEPROM Memory*, DS22187. The data sheet is available on the Microchip Technology web site, www.microchip.com.

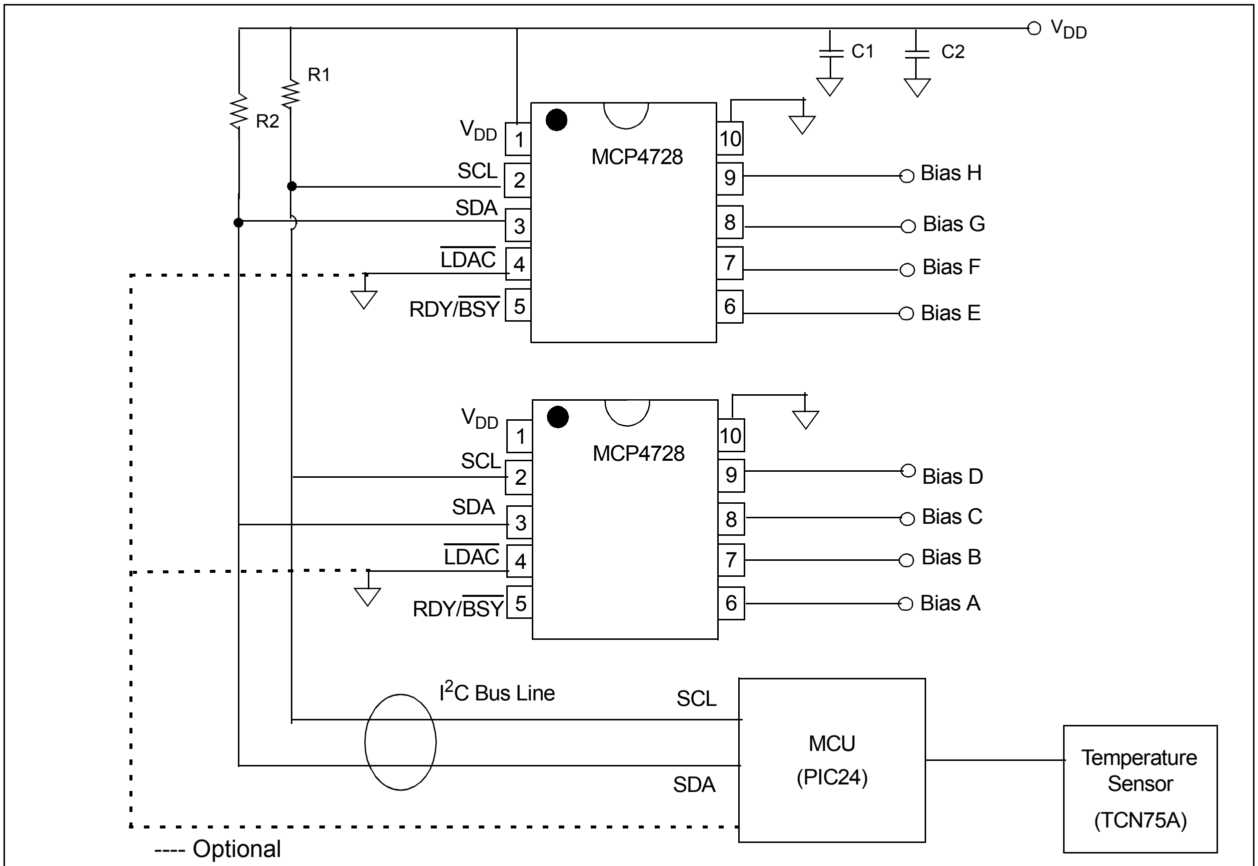
USING THE MCP4728 FOR MORE THAN QUAD OUTPUTS

A typical power amplifier module for the cellular base station has at least 8 to 16 bias voltage control points. Typically, multiple DAC devices are used for these control points.

The MCP4728 has three I^2C address bits. The combination of these three bits allows eight distinct addresses. Therefore, the user can connect up to eight MCP4728 devices on the same I^2C bus line. By connecting eight devices, 32 DAC channel outputs are available. It needs two MCP4728 devices for octal outputs, and four MCP4728 devices for 16 outputs.

Figure 8 shows an example of using two MCP4728 devices for octal outputs.

The $\overline{\text{LDAC}}$ pin in the MCP4728 is used for two purposes: (a) Loading the DAC input registers to the output registers synchronously and (b) Device selection input when reprogramming I^2C address bits at the user's application PCB board. If the above are not needed, then the user can simply ground the $\overline{\text{LDAC}}$ pin instead of connecting it to the MCU. In this case, the output of each channel will be updated whenever the DAC input register is updated by the user's write command.



R1 and R2	=	Pull-up resistors for SCL and SDA, respectively
5 kΩ - 10 kΩ for f_{SCL}	=	100 kHz to 400 kHz
~700Ω for f_{SCL}	=	3.4 MHz
C1: 0.1 µF, Ceramic capacitor		
C2: 10 µF, Tantalum capacitor		

FIGURE 8: *Using the MCP4728 for Octal Outputs.*

Note: The user can connect up to eight MCP4728 devices on the same I^2C Bus line.

CONCLUSION

There are many ways to design a bias voltage control circuit for the LDMOS power amplifier. One of the most effective solutions is using a stand-alone DAC and a temperature sensor. The MCP4728, a 12-bit voltage output DAC, is suitable for the LDMOS bias voltage control applications. The device provides stable and consistent performance over the wide temperature range from -40°C to +125°C. Multiple MCP4728 devices can be connected to the same I^2C bus line if an application needs more than 4 independent control voltages.

Note:	Microchip will continuously release new DAC devices for multiple output channels with SPI and I^2C serial interface options. Please contact the Microchip office near you for further update of the product availability.

REFERENCES

[1] MCP4728 Data Sheet, *12-Bit, Quad Digital-to-Analog Converter with EEPROM Memory,* DS22187, Microchip Technology Inc., 2009.

[2] *MCP4728 Evaluation Board User's Guide*, DS51837, Microchip Technology Inc., 2009.

[3] TCN75A Data Sheet, *M2-Wire Serial Temperature Sensor*, DS21935, Microchip Technology Inc., 2006.

[4] 16-bit brochure, *PIC24 Microcontroller Brochure*, DS39754, Microchip Technology Inc., 2009.

[5] *LDMOS Bias Temperature Compensation*, AN067, Sirenza Microdevices.

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ISBN: 978-1-60932-265-6

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